A FAST TRANSIENT RESPONSE ESR-CONTROLLED FIXED FREQUENCY HYSTERETIC BUCK CONVERTER

A Thesis

by

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ABSTRACT

Modern application processors (microprocessors and Digital Signal Processors) are power hungry and demand power management solutions that can withstand their frequent and high slew-rate load transients while regulating their supply in a tight voltage tolerance. Hysteretic converter has excellent transient response performance but its variable switching frequency causes concern for electromagnetic interference in noise sensitive applications. A new frequency stabilization scheme for hysteretic buck dc-dc converters is proposed in this thesis. The equivalent series resistance (ESR) of the output capacitor is regulated by a phase-locked loop (PLL) to stabilize the operating frequency of the converter.

The proposed fixed frequency ESR-controlled converter achieves a fixed 2MHz switching frequency, with less than 1μs response time to a 500mA load step while limiting undershoot and overshoot on the output voltage to 50mV and 40mV respectively.

The performance of the presented work shows that the ESR of the output capacitor of a Hysteretic Buck Converter can be controlled to stabilize the switching frequency of the Hysteretic DC-DC Converter.

DEDICATION

To my mentor Tuli Dake

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1. INTRODUCTION

Microprocessors and digital signal processors (DSPs) are ubiquitous in today's mobile devices and internet of things (IoT). Voltage regulator modules (VRMs) for modern high performance processors are designed to supply the high power demand. To meet the demand for high supply current, multiphase converter solutions are designed to share the load demand of processors and the phases are interleaved for ripple cancellation. Most processors operate with dynamic voltage and frequency scaling (DVFS) which allow them to actively control their power consumptions for their varying load demands. Under DVFS control, processors automatically adjust their clock frequency and supply voltage depending on their mode of operation; sleep mode, deep sleep, stop grant or maximum. DVFS therefore demand that voltage regulation modules for processor applications have good reference tracking [1].

Processors have frequent, high slew-rate load transients and stringent voltage tolerance. For instance the Table 1 shows some regulator specifications for the Intel Xeon 5500 series of processors [2]. Voltage and current mode pulse width modulation (PWM) dc-dc converters have been used in many power management solutions but their slow feedback loop make them unreliable for frequent load transient applications. Though this class of dc converters have constant switching frequency, they have phase compensation network due to the phase delay the feedback signal experiences through the high-gain error amplifier. During load transients the capacitors in the phase compensation network restrains the controller from fully sensing the transient load effect. Also the phase delay

through the high-gain error amplifier increases the overall loop delay of the controller making it slow to respond to load transients. Also they need auxiliary circuitry to sense inductor current.

Table 1: Intel Xeon 5500 Series VRM Specification

Symbol	Parameter	Min.	Max.	Unit
I_{CCTDC}	Continuous load current		130	A
I_{CC}	Load current		150	A
I_{CCSTEP}	Current step		120	A
dI_{CC}/dt	Current slew-rate		300	A/µs
	Dynamic voltage identification	0.5	1.6	V
	Frequency of load transients		2	MHz
V_{OS}	Overshoot voltage		50	mV
T_{OS}	Overshoot settling time		25	µs

A second class of dc-dc converters called ripple-based controllers have better transient performance compared to the previous class. The ripple based converters directly sense inductor current and load changes through the equivalent series resistance (ESR) of the output capacitor. Moreover the do not use phase compensation network because there is no high gain error amplifier to cause phase delay through the feedback network. But their variable switching frequency is a major drawback. Modifying this class of VRMs would make them an excellent choice for frequent, high slew-rate load applications.

2. PREVIOUS WORKS

DC converters with ripple based control (hysteretic and V^2 control) have excellent load transient response since they directly sense load changes through the equivalent series resistance (ESR) of the output filtering capacitor of power stage. This makes them good candidates for power management application which have frequent and high slew-rate load transients. Unfortunately the conventional ripple based controllers have variable switching frequency which might cause electromagnetic interference in noise sensitive applications. This class of controller can be made ideal for high slew-rate applications by modifying the controller to stabilize the switching frequency.

Several works have implemented different schemes to control the operating frequency and make it fixed. Most of the published frequency stabilization schemes can be grouped under one of the following classes of control

1. Delay-Controlled Frequency Synchronization
2. Hysteretic Window Controlled Frequency Synchronization
3. Frequency Synchronization by Adjusting Sensed Inductor Ripple
4. Frequency Stabilization by On-Time adjustment
5. Frequency Stabilization by Signal Injection

2.1 Delay-Controlled Frequency Synchronization

The works presented in [3 - 7] stabilize the switching frequency of ripple based converters by inserting adjustable delay elements in the voltage regulation loop. The delay

element is tuned to lock the converter's operating frequency at a fixed reference. Each work presents a unique technique of delay tuning. But the synchronized frequency of delay-controlled frequency stabilization is always less than the free running switching frequency of the dc converter due to the added delay as shown in (1). Also the added delay increases the response time of the converter.

2.1.1. A 90–240 MHz Hysteretic Controlled DC-DC Buck Converter with Digital Phase Locked Loop Synchronization

The design in [3] achieves a good transient response by sensing the inductor current using an RC-filter (R_F, C_F) and feeds the translated voltage signal to a comparator with hysteresis to realize a hysteretic voltage controller as shown in Figure 1. The switching frequency of its power stage is shown to be dependent on the input voltage V_{IN}, duty ratio D, time constant τ_{RC} of the R_FC_F sense filter, hysteresis window V_H and the controller's loop delay τ_D as shown in (1)

$$f_S = \frac{D(1-D)}{\tau_{RC}.\left(V_H/V_{IN}\right) + \tau_D} \quad (1)$$

Current sensing with R_FC_F network eliminates the dependence of converter's switching frequency on output capacitor's parasitic ESR and ESL. The proposed architecture adds a voltage controlled delay line to the controller to adjust the loop delay so as to regulate the switching frequency to a constant. The comparator's output signal is frequency divided and compared to a clock reference by a phase/frequency detector

(PFD). The output of the PFD is averaged by charge pump with loop filter to generate a voltage control signal for the delay line.

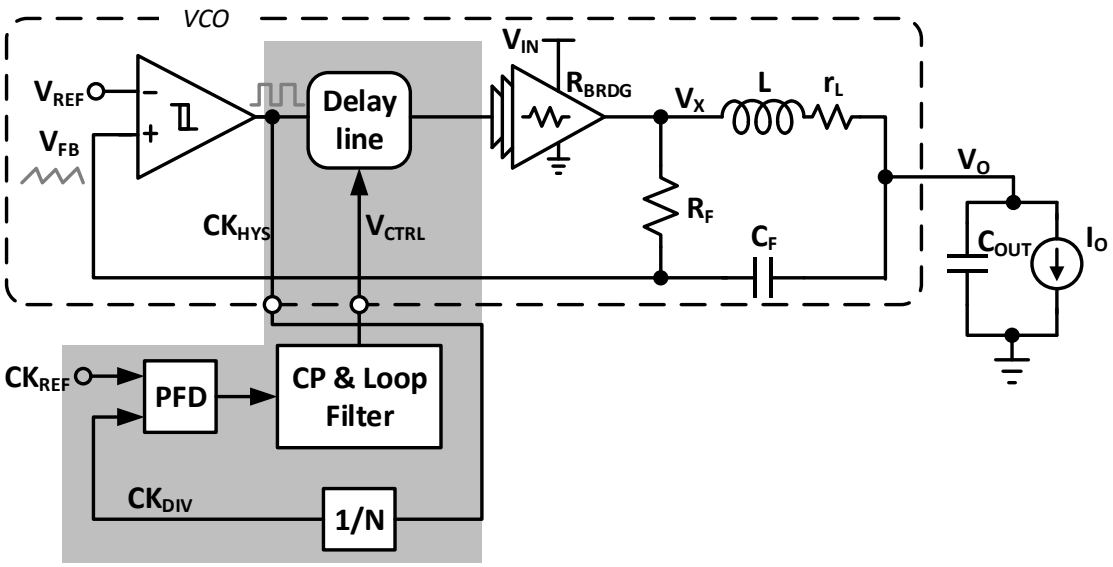

Figure 1: A 90–240 MHz Hysteretic Controlled DC-DC Buck Converter. Reprinted from [3]

2.1.2. A Delay-Locked Loop Synchronization Scheme for High-Frequency Multiphase Hysteretic DC-DC Converters

Like [3], [4] uses RC-filter to sense the inductor current and eliminate the effect of capacitor ESR and ESL on frequency variation but [3] is a single phase solution while [4] is a multiphase converter. A multiphase hysteretic converter with all phases well synchronized would have a fast response to load transients and the regulated output

voltage would have less ripple due to ripple cancellation effect of interleaved phases. The phases are phase and frequency synchronized by a delay-locked loop (DLL). A four-phase hysteretic buck converter, as shown in Figure 2, is used to validate the proposed design.

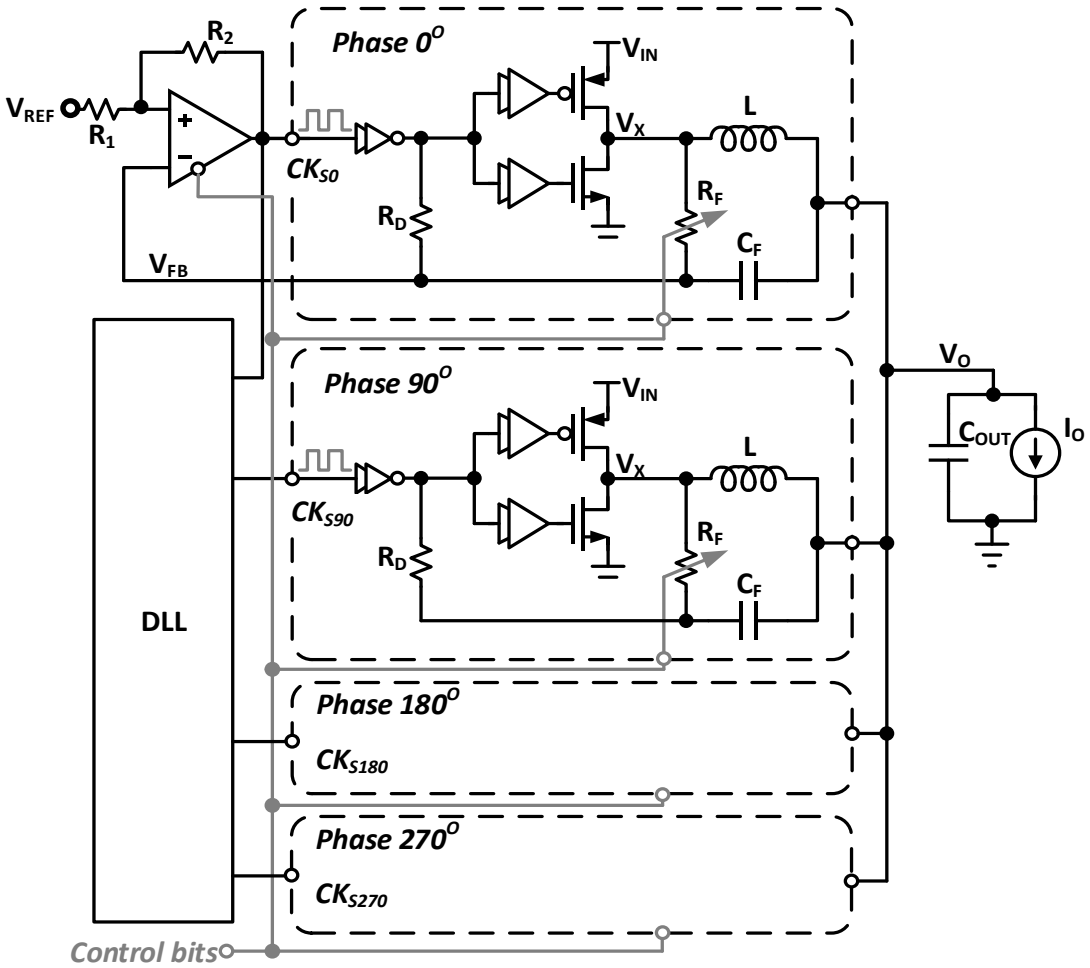

Figure 2: A Delay-Locked Loop Synchronization Scheme.
Reprinted from [4]

Only the first phase is used to regulate the output voltage to the desired value. The DLL locks the switching frequency of the first stage to the reference clock. The locked DLL synchronizes the gate control signals of the other three phases to the same frequency and duty ratio as the first phase but at 90^o, 180^o and 270^o phase offsets respectively. Thus all the four phases have the same duty ratio, switching frequency, average output voltage and they are interleaved for current sharing and output ripple reduction.

2.1.3. Digitally Assisted Quasi-V^2 Hysteretic Buck Converter with Fixed Frequency and without Using Large-ESR Capacitor

The work in [5] proposes a converter that resembles a V^2-controller but operates like a hysteretic controller as shown in Figure 3. Like V^2-control the presented work has an error correction path for precise voltage control and a feedforward path for pulse width modulation. The feedforward path uses an RC network to sense the inductor current like [3] and [4].

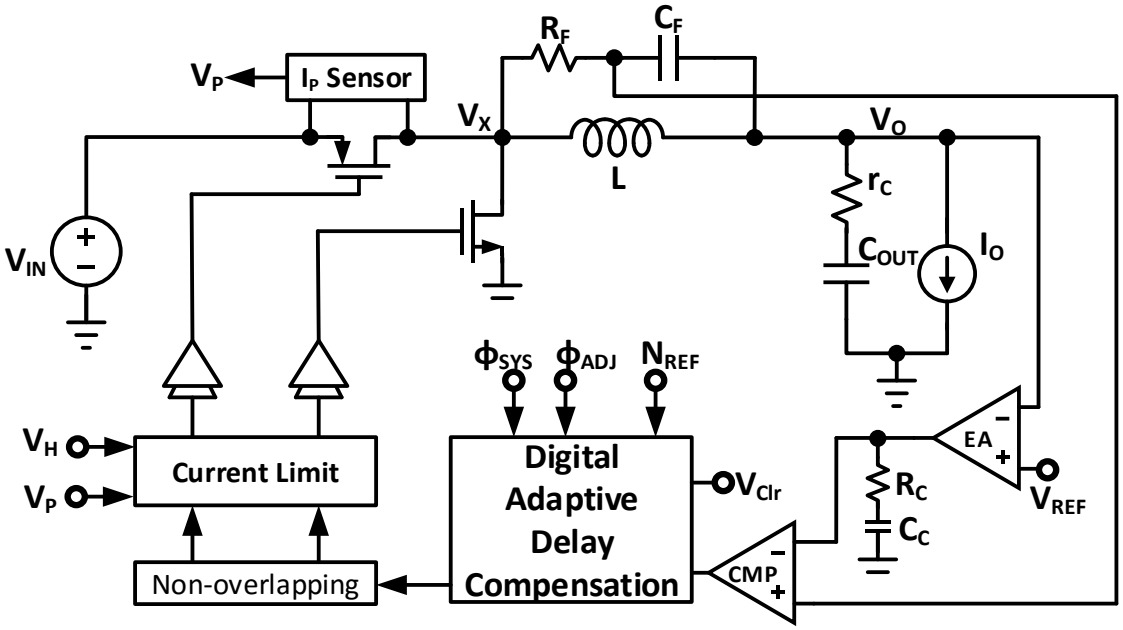

Figure 3: Digitally Assisted Quasi-V^2 Hysteretic Buck Converter.
Reprinted from [5]

A digital adaptive delay compensator (DADC) is inserted into the voltage control loop to adjust the loop delay when the converter's switching period is different from the period of the reference clock. An 8-bit counter driven by a reference clock is used to measure the converter's switching period.

2.1.4. Ultra-Fast Fixed-Frequency Hysteretic Buck Converter with Maximum Charging Current Control and Adaptive Delay Compensation for DVS Applications

The scheme in [6] uses an adaptive delay compensation to regulate the switching frequency of a bang-bang controller with a frequency error detector and a voltage

controlled delay circuitry as shown in Figure 4. The frequency error detector compares the output of the hysteretic comparator with a frequency reference and generates a voltage control signal V_{CTRL} to adjust the controlled delay to stabilize the operating frequency.

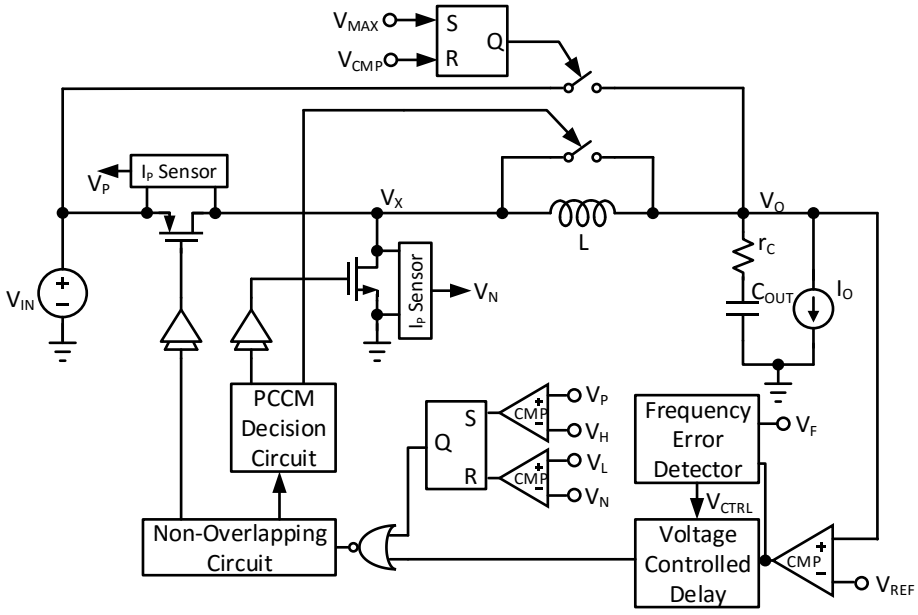

Figure 4: Ultra-Fast Fixed-Frequency Hysteretic Buck Converter.
Reprinted from [6]

The design in [6] senses switch currents (V_P, V_N) to ensure continuous conduction mode of operation using the pseudo-continuous conduction mode (PCCM) decision circuit and implement overcurrent protection. This work has an auxiliary direct charging path

from the input to output to improve up-tracking response for dynamic voltage scaling but this circuitry degrades efficiency due to the switch losses.

2.1.5. A Ripple Control Buck Regulator with Fixed Output Frequency

The architecture in [7] synchronizes the switching frequency of a hysteretic converter to a reference clock through a voltage controlled delay, as shown in Figure 5, similar to [2 - 6] but the implementation of its voltage controlled delay makes it unique. Figure 6 shows the delay block which can be controlled by either the charging current I_C or the voltage threshold V_{TH}. In this work, I_C is held constant while V_{TH} voltage level controls the delay proportionally.

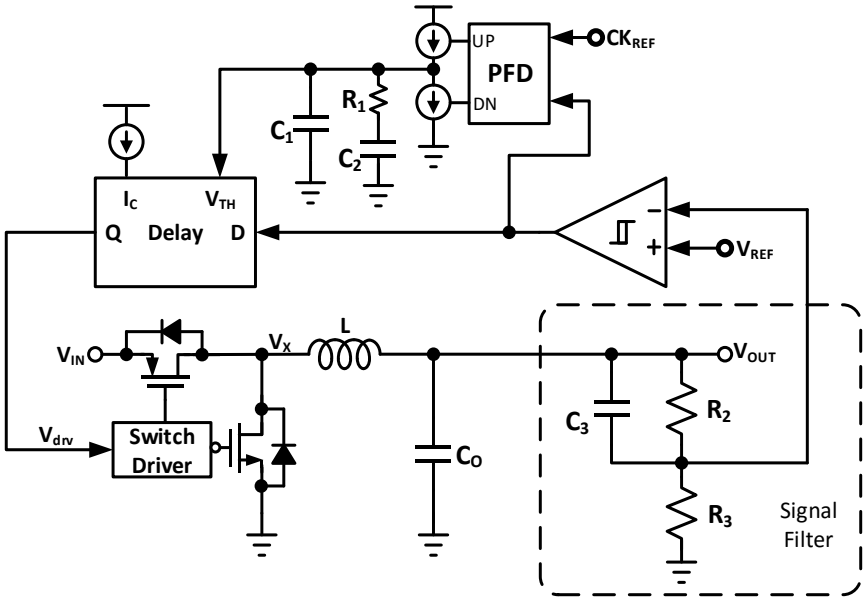

Figure 5: A Ripple Control Buck Regulator with Fixed Output Frequency. Reprinted from [7]

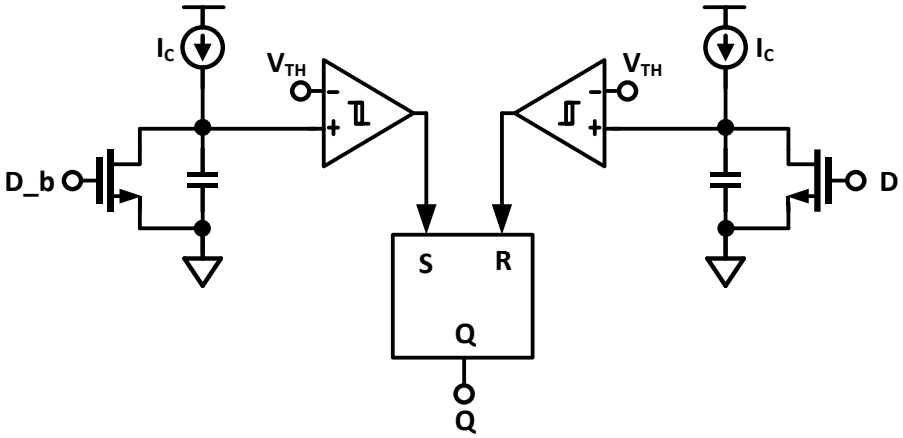

Figure 6: Delay Element.
Reprinted from [7]

2.2 Hysteretic Window Controlled Frequency Synchronization

A second approach to frequency stabilization in ripple based dc converters is by controlling hysteresis window size. Hysteresis can be implement in voltage or current domain and its size could be adjusted by controlling the low or high threshold or both. One major drawback to this scheme is it causes variation in output voltage ripple which might increase and exceed the desired voltage tolerance of the design.

2.2.1 A Fast-Response Pseudo-PWM Buck Converter with PLL-Based Hysteresis Control

The design in [8] uses a PLL to lock the switching frequency of the power stage by adjusting the size of the hysteresis window ($V_{HYS} = V_H - V_L$); low threshold level V_L is fixed while the high threshold voltage V_H is controlled by the PLL control voltage as

shown in Figure 7. The design uses a very low capacitor ESR which makes the output ripple very small. A high-pass filter (zero generator) with high gain is used to amplify the output ripple for voltage regulation.

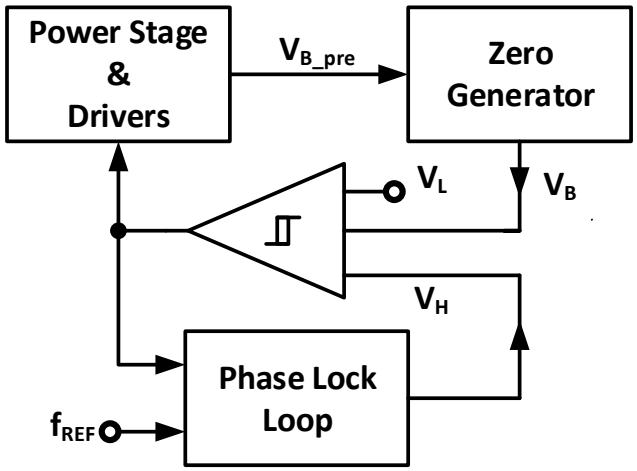

Figure 7: A Fast-Response Pseudo-PWM Buck Converter.
Reprinted from [8]

2.2.2 A 6A 40MHz four-phase ZDS Hysteretic DC-DC Converter with 118mV Droop and 230ns Response Time for a 5A/5ns Load Transient

A zero-delay synchronization (ZDS) scheme is used in [9] to adaptively adjust the hysteresis window and thus stabilize the switching frequency of the converter. The zero delay synchronization allows the output voltage to sharply exit the hysteresis window during load transients and give the converter a fast transient response.

The proposed controller has an adaptive transistor sizing (ATS) which uses the average inductor current I_{L_AVG} to control the power FETs partitions to optimize efficiency over a wide load range. An RC low pass filter is used to sense the DC value of the inductor current while an RC high pass filter with a different time constant senses the AC ripple of the inductor current which permits the use of an inductor with low DC resistance.

Figure 8 shows an interleaved four-phase converter of the proposed controller with a clock synchronizer for ripple cancellation and current sharing. The systematic offsets and mismatches among the phases is compensated by the error compensator.

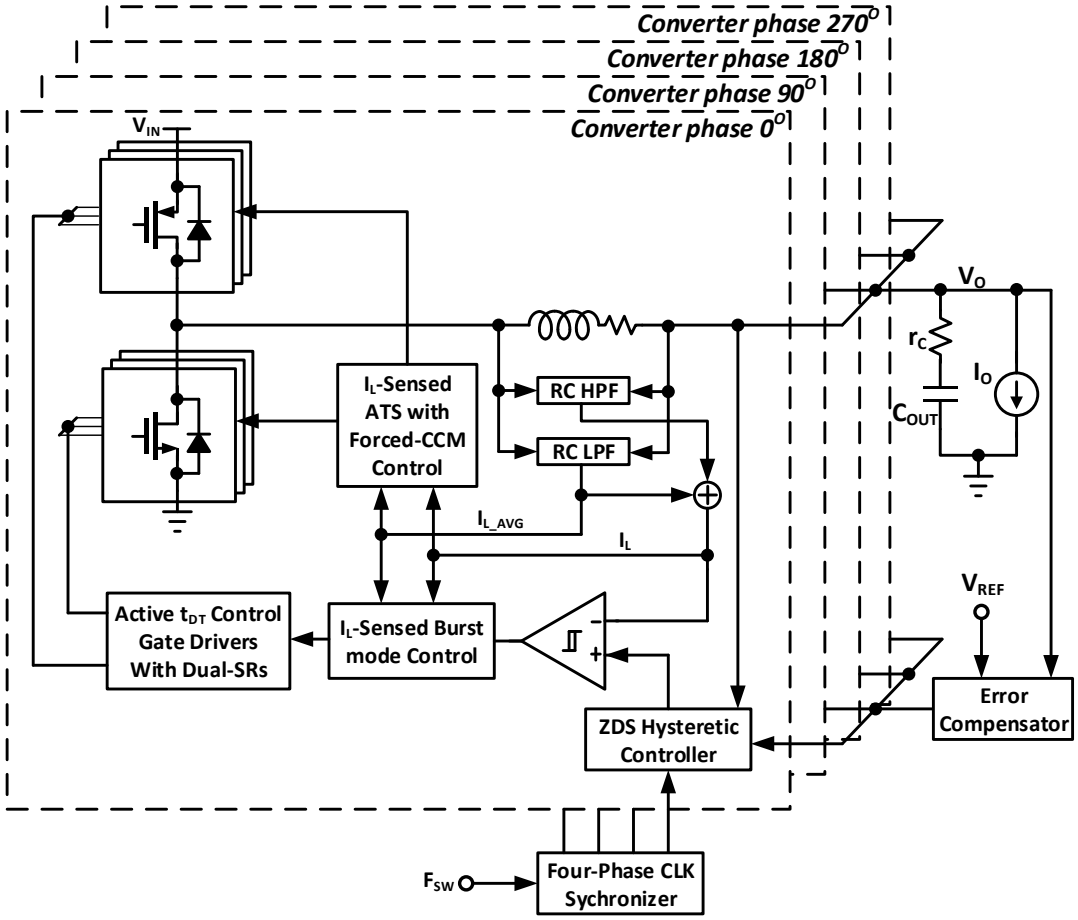

Figure 8: A 6A 40MHz Four-Phase ZDS Hysteretic DC-DC Converter. Reprinted from [9]

2.2.3 A Fixed-Frequency Hysteretic Controlled Buck DC-DC Converter with Improved Load Regulation

The work in [10] controls the variable resistor R_1 to adjust the hysteresis window and stabilize the frequency of a hysteretic converter. A PFD/CP/LPF block compares the switching frequency of the voltage regulator to a reference clock and generates the control signal for the variable resistor R1 as shown in Figure 9.

The RC feedback network for voltage regulation is modified by adding resistor R_{F2} to reduce the output voltage error that comes with conventional inductor current RC sense filter. There is still an error due to the voltage drop across the inductor DC resistance (r_L) and the added R_{F2} increases the conduction losses of the converter.

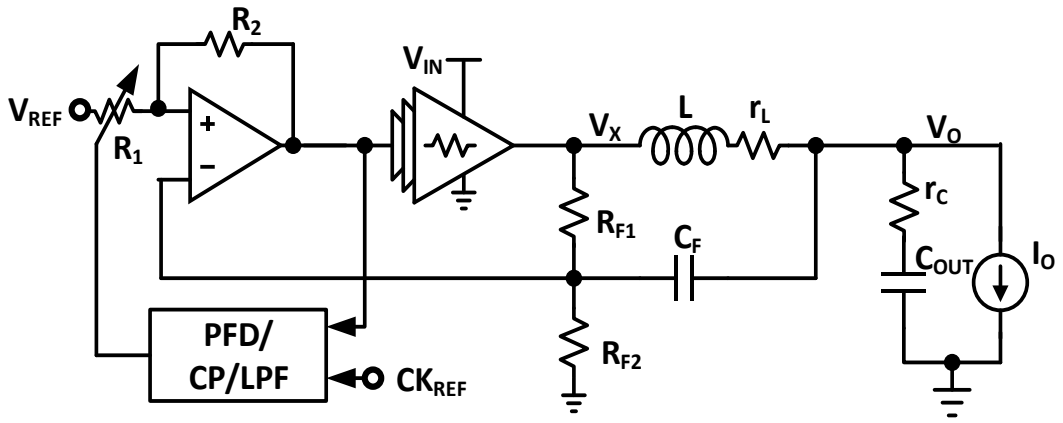

Figure 9: A Fixed-Frequency Hysteretic Controlled Buck.
Reprinted from [10]

2.2.4 Stabilizing the Frequency of Hysteretic Current-Mode DC/DC Converters

The hysteretic buck converter presented in [11] senses the inductor current with a series resistor R_S and stabilizes the switching frequency by controlling the hysteresis current I_{HYS} as shown in Fig 10. The hysteresis current I_{HYS} realized by the converter can be derived by equating the input voltages of the comparator CMP.

$$V_N = V_P$$

$$V_N = V_N - I_L R_S + I_P R_H$$

$$I_L = I_P . \frac{R_H}{R_S}$$

When COUT is high, $I_P = I_C$ and $I_{L1} = I_C . \frac{R_H}{R_S}$

When COUT is low, $I_P = I_C - I_H$ and $I_{L2} = (I_C - I_H) . \frac{R_H}{R_S}$

$$I_{HYS} = I_{L1} - I_{L2}$$

$$I_{HYS} = I_H . \frac{R_H}{R_S} \quad (2)$$

During the switch S off-time, the inductor ripple (hysteresis current) is expressed as

$$\Delta i_L = I_{HYS} = \frac{V_O}{L} . (1 - D) t_S$$

$$I_{HYS} = \frac{1}{L . f_S} . V_O . \left(1 - \frac{V_O}{V_{IN}}\right) \quad (3)$$

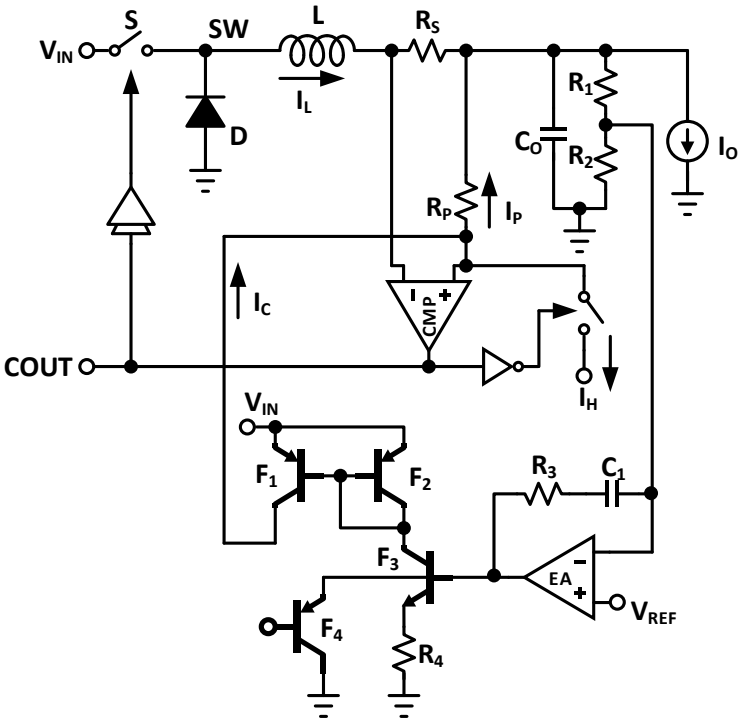

Figure 10: Stabilizing the Frequency of Hysteretic Current-Mode.
Reprinted from [11]

The control law in (3) shows that the switching frequency (f_S) of the converter can be controlled by adjusting current hysteresis I_{HYS}. The paper presents four different ways of generating the control current I_H to stabilize the converter's switching frequency:

1. Direct Nonlinear Control
2. Duty-Cycle Proportional Control
3. Frequency Locked Loop
4. Phase Locked Loop

2.2.4.1 Direct Nonlinear Control

The direct nonlinear control uses nonlinear circuits (voltage controlled current sources, BJTs) to generate the control current I_H needed to realize hysteresis (2) and stabilize the switching frequency (4). Figure 11 shows a nonlinear circuit which produces the control current I_H. The voltage controlled current sources can be realized with operational trans-conductance amplifiers (OTAs) for precision or simple transistor implementation.

From Figure 11, $I_H = I_{H0} - I_{HV}$

$$I_{H0} = V_O.\frac{R_i}{{R_o}^2}, I_{HV} = \frac{{I_2}^2}{I_1}, I_1 = \frac{V_{IN}}{R_i}, and\ I_2 = \frac{V_O}{R_o}$$

$$I_H = V_O.\frac{R_i}{{R_o}^2} - \frac{{V_O}^2}{{R_o}^2}.\frac{R_i}{V_{IN}}$$

$$I_{HYS} = I_H.\frac{R_H}{R_S} = V_O.\frac{R_i}{{R_o}^2}.\frac{R_H}{R_S}\left(1 - \frac{V_O}{V_{IN}}\right) \quad (4)$$

Comparing equation 4 and to 3,

$$L.F_S = \frac{{R_o}^2}{R_i}.\frac{R_S}{R_H} \quad (5)$$

This control scheme needs no reference clock, the expected switching frequency can be set by circuit parameters R_o and R_i. Though frequency stabilization is achievable, precision is not assured as in the case of PLL synchronization schemes.

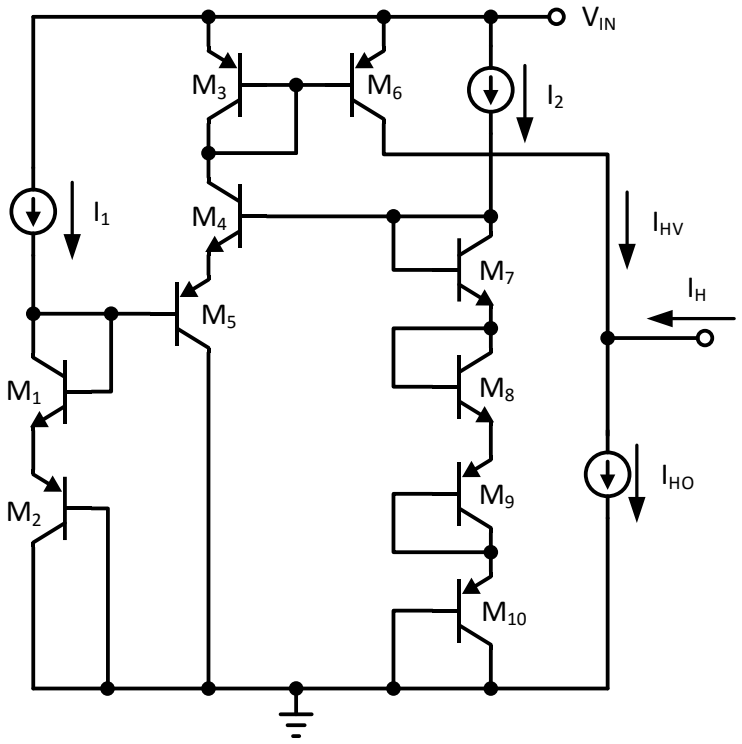

Figure 11: Direct Nonlinear Control.
Reprinted from [11]

2.2.4.2 Duty-Cycle Proportional Control

This control scheme generates $V_O.\left(1-\frac{V_O}{V_{IN}}\right)$ in (3) using the signal at the switching node SW and averages the signal with an R_2C_2 low pass filter as shown in Figure 12. The averaged signal is buffered to generate a duty-cycle dependent current I_H which is used to controls the hysteretic current (2) for constant frequency operation (3). Resistor R_H is selected to be equal to the product $L.f_S$ so as to obey the control law in (3). Like the direct nonlinear control, this control scheme needs no reference clock for frequency stabilization

but the precision is better than the direct nonlinear control since the operating frequency depends on resistor R_H only. Also this frequency stabilization scheme includes the switching non-ideality in its control by using the switching node signal SW and the control scheme is very simple.

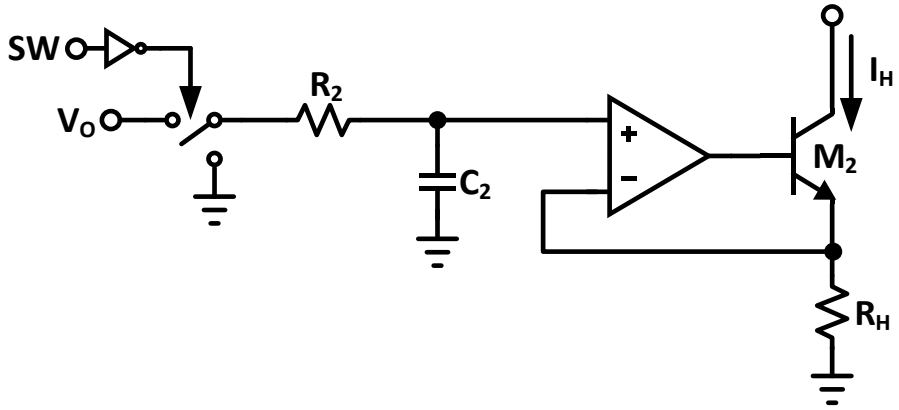

Figure 12: Duty-Cycle Proportional Control.
Reprinted from [11]

2.2.4.3 Frequency Locked Loop

The frequency locking loop shown in Figure 13 is a closed loop frequency control from port COUT to I_H for the hysteretic converter in Figure 10. The integrator ensures the average of the one-shot output is set by the reference voltage for accurate voltage regulation. Similar to the duty-cycle proportional control, a BJT regulates the voltage across a fixed resistance RH to stabilize the switching frequency.

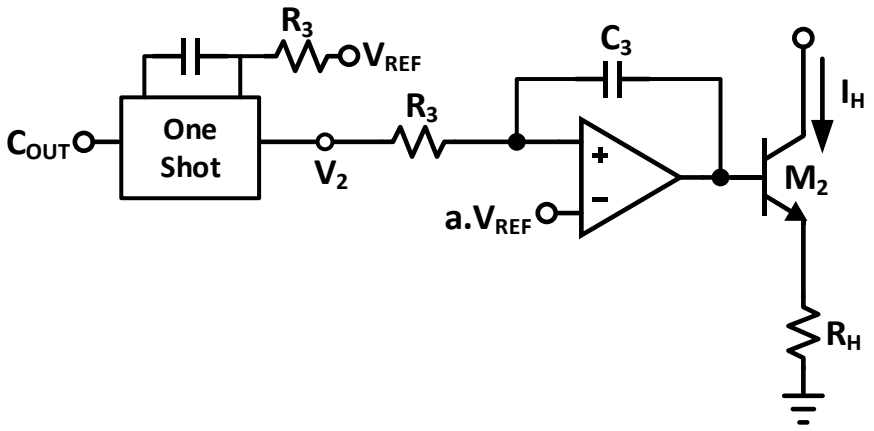

Figure 13: Frequency Locked Loop.
Reprinted from [11]

2.2.4.4 Phase Locked Loop (PLL)

The fourth frequency stabilization scheme synchronizes the switching frequency to an external clock using a third order Type II PLL and it is the most precise method. The gate control signal of switch S is phase and frequency synchronized to the clock reference. The control voltage of the PLL is converted to a corresponding hysteresis current using the trans-conductance *gm* as shown in Figure 14.

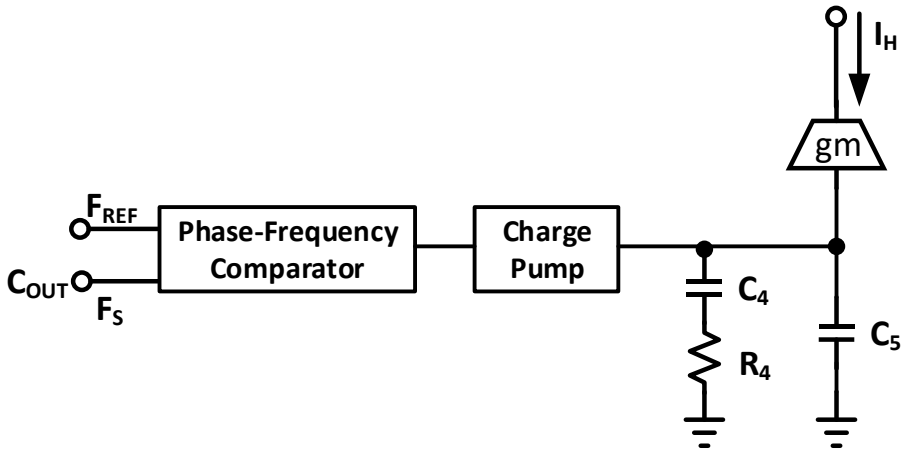

Figure 14: Phase Locked Loop.
Reprinted from [11]

2.3 Frequency Synchronization by Adjusting Sensed Inductor Ripple

The works in [12] – [14] stabilize the operating frequency of ripple based converters by modulating the slope of sensed inductor ripple. Like the hysteretic window control, this control scheme will cause variation in output ripple size.

2.3.1 A PLL-Based High-Stability Single-Inductor 6-Channel Output DC-DC Buck Converter

A single inductor multiple outputs (SIMO) is presented in [12] with fixed frequency hysteretic control as shown in Figure 15.

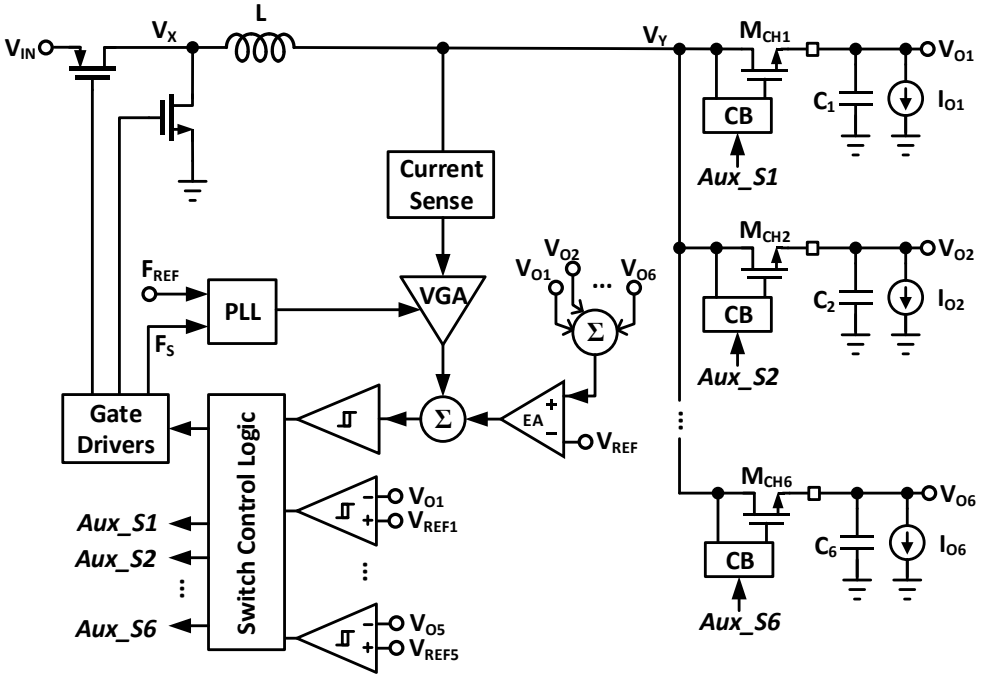

Figure 15: A PLL-Based High-Stability SIMO.
Reprinted from [12]

The controller senses the inductor current and adds it to the average error of the multiple outputs to generate the gate control signals for the main FETs and the auxiliary FETs of the individual output channels to regulate the channels to their respective desired voltages. The control voltage of the PLL regulates the variable gain amplifier (VGA) to control the slope of the sensed inductor current so as to stabilize the switching frequency of the SIMO converter at F_{REF}.

2.3.2 A 0.518mm^2 Quasi-Current-Mode Hysteretic Buck DC-DC Converter with 3μs Load Transient Response in 0.35μm BCDMOS

This design in [13] stabilizes the switching frequency of the power converter by tuning the slope of the sensed inductor ripple as depicted in Figure 16. It senses the inductor current using an OTA, and controls the resistance of R_{SEN2} to adjust the slope of the sensed ripple. The sensed ripple is added to the output voltage through capacitor C_{SEN}.

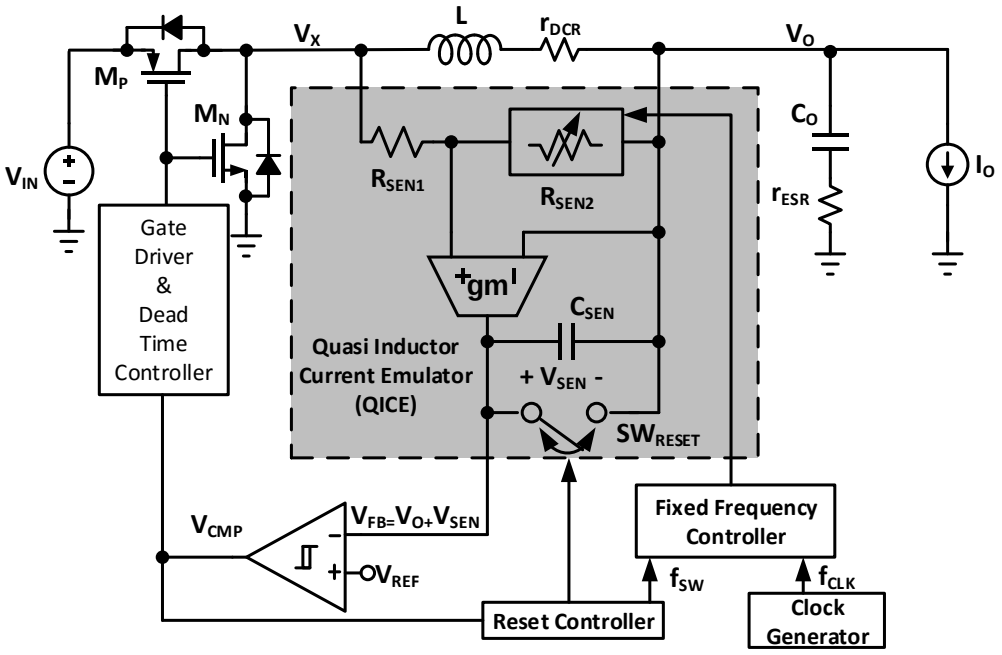

Figure 16: A Quasi-Current-Mode Hysteretic Buck DC-DC Converter. Reprinted from [13]

CSEN is reset whenever V_{FB} reaches any of the two hysteresis thresholds to prevent saturation and minimize the capacitor size required. But resetting CSEN makes the current sensing inaccurate and makes the controller less able to detect load transients.

2.3.3 A Fixed Frequency Hysteretic Buck Converter Using a Highly Digital Hybrid Voltage and Current-Mode Control

An RC network is used to sense the inductor ripple in [14] and the slope of the current ripple is tuned to lock the switching frequency by tuning resistors R_P and R_I. The frequency regulation loop uses a digital word to control the resistance R_I while R_P is linearly controlled (linear phase control) by an analog voltage signal to finely synchronize the switching frequency to the reference and prevent dithering. Figure 17 shows the block diagram of the proposed design.

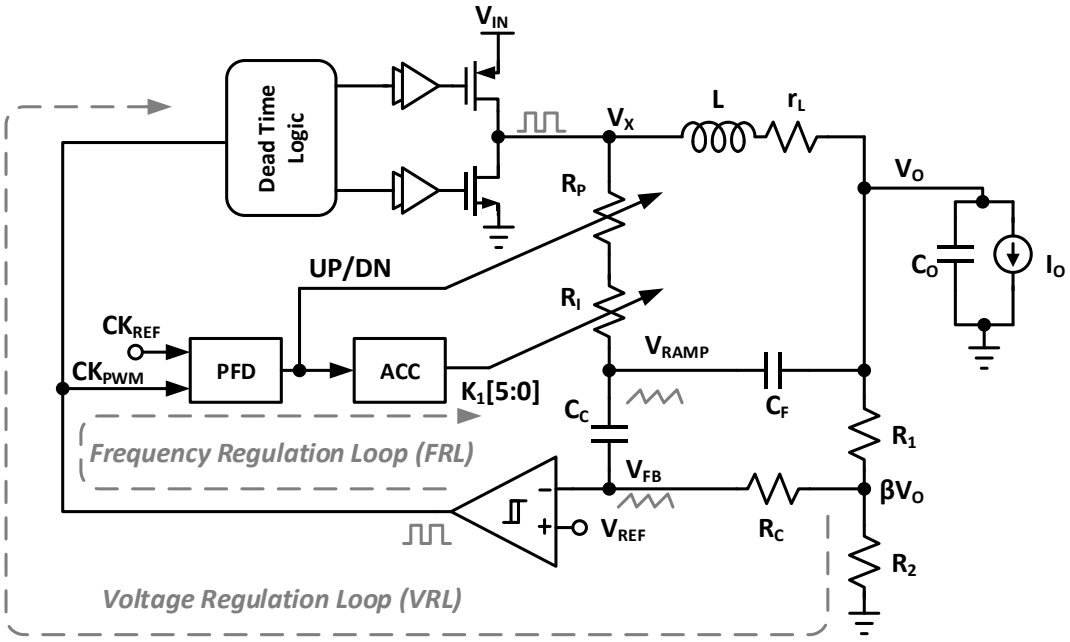

Figure 17: A Highly Digital Hybrid Hysteretic Converter.
Reprinted from [14]

2.4 Frequency Stabilization by On-Time adjustment

2.4.1 Ripple-Based Control of Switching Regulators

This work [15] modifies a constant on-time regulator to operate with a constant switching frequency as shown in Figure 18. For a constant on-time ripple regulator, the switching frequency of the converter in inversely proportional to the input voltage level as expressed in (6). Thus the variable switching frequency (f_S) can be stabilized by generating an on-time which is inversely proportional to the input voltage (V_{IN}).

$$f_S = \frac{V_{OUT}}{V_{IN}.T_{ON}} \tag{6}$$

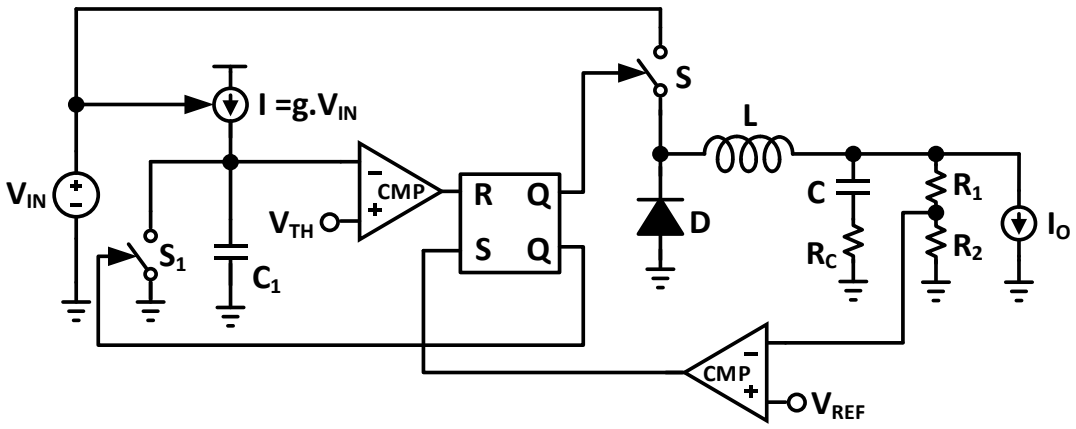

Figure 18: Modified On-Time Ripple Regulator.
Reprinted from [15]

2.4.2 Pseudo-Constant Switching Frequency in On-Time Controlled Buck Converter with Predicting Correction Techniques

Like [15], the design presented in [16] adjusts the on-time to stabilize the switching frequency of the ripple based converter. From (6) both input and output voltages affect how the on-time controls the switching frequency, also the output voltage level is dependent on the load and converter parasitic resistances. As shown in Figure 19 the

proposed work generates an equivalent output voltage V_{OUT_eq} using the EOVS (Equivalent Output-Voltage Synthesizer) and a fully linear voltage-to-current generator translates the input voltage level into current i_{ON}. The on-time modulator sets the duty ratio using i_{ON} and V_{OUT_eq} in order to stabilize the switching frequency. This frequency stabilization scheme will be more effective in dynamic voltage scaling where the output tracks a changing reference voltage.

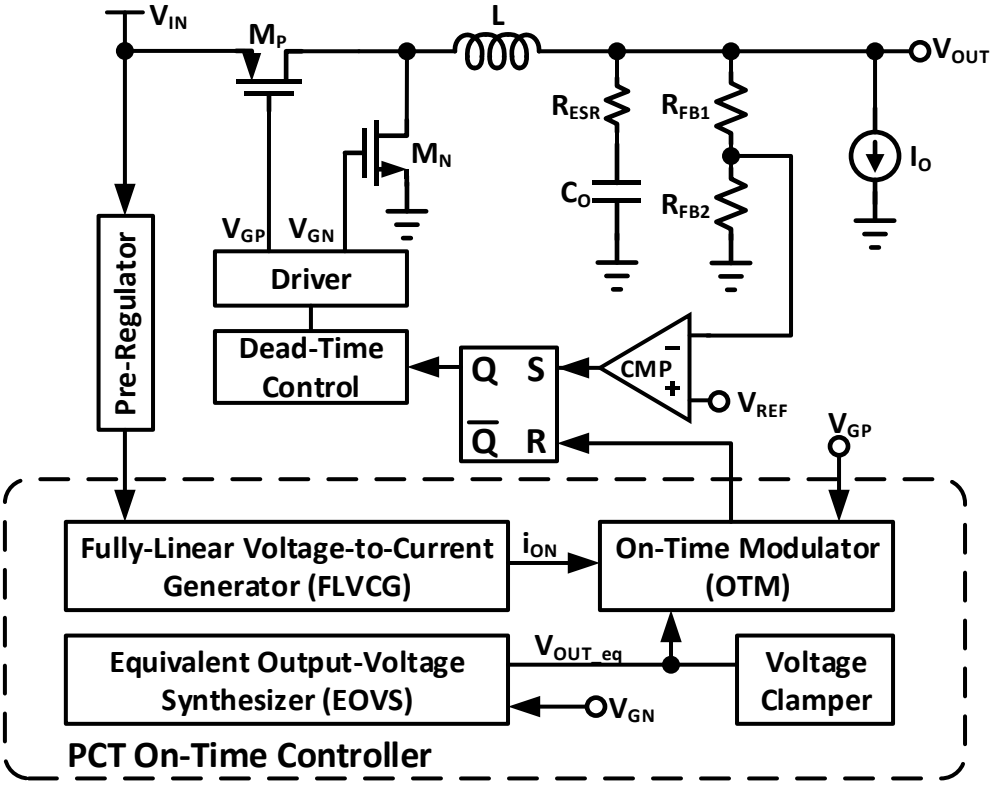

Figure 19: Pseudo-Constant Switching Frequency with On-Time Control. Reprinted from [16]

2.5 Frequency Stabilization by Signal Injection

2.5.1 A 233-MHz 80%-87% Efficient Four-Phase DC-DC Converter

The controller presented in [17] locks the switching frequency of the converter by injecting a synchronizing signal I_{SYNC} with the reference voltage at the non-inverting input of the comparator. The synchronizing signal ensures that the switching instants follow the envelope of the hysteresis window. Frequency synchronization will only be possible if the frequency of the synchronizing signal is lower than the free-running frequency of the converter. Also the amplitude of injected signal (V_{SYNC}) must satisfy the condition:

$$V_H + V_{SYNC} > V_{IN}(1-D).D.\frac{T_{SYNC}}{R_F C_F} \quad and \quad V_H = V_{IN}(1-D).D.\frac{T_O}{R_F C_F}$$

$$V_{SYNC} > V_{IN}(1-D).D.\frac{(T_{SYNC}-T_O)}{R_F C_F} \quad Where\ V_{SYNC} = I_{SYNC}(R_1||R_2)$$

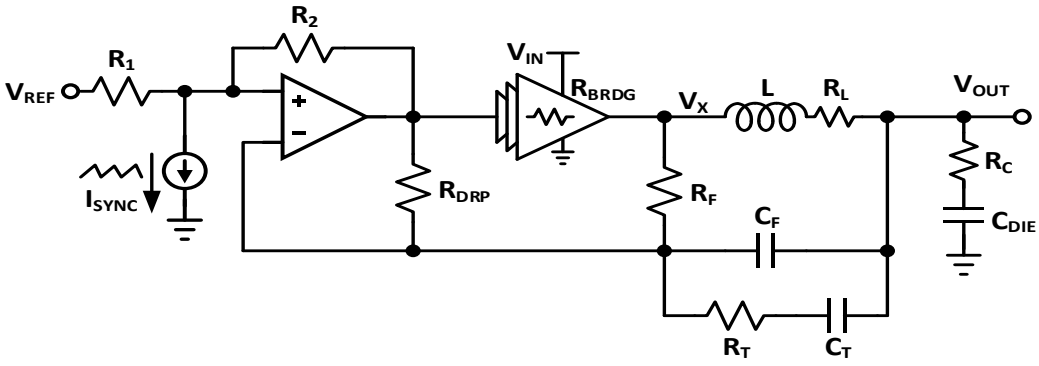

Figure 20: A Four-Phase DC-DC Converter Using Air-Core Inductors. Reprinted from [17]

3. PROPOSED ARCHITECTURE

Ripple based converters (hysteretic and V^2 controls) directly sense changes in load current through the ESR of the output capacitor which gives them fast response to frequent and high slew-rate load transients. As discussed in section 2 several works [3] – [17] have proposed schemes to stabilize the variable switching frequency of conventional ripple based converters. This work proposes a new frequency stabilization control that uses a phase-locked loop (PLL) to synchronize the switching frequency of a hysteretic buck converter to a reference clock.

The proposed design preserves the inherent fast transient response of conventional hysteretic controllers; responding to load transients within the switching cycle which transients occur. Unlike delay-controlled frequency stabilization, the proposed ESR-controlled frequency stabilization achieves operating frequency higher than the free running frequency and maintains the fast transient response of conventional hysteretic control. Also the output ripple of the proposed architecture is fixed mainly by its constant hysteresis window contrast to the variable output ripple of the hysteresis window controlled frequency stabilization scheme. The characteristics considered make the proposed ESR controlled scheme more effective compared to the reported delay-controlled and hysteresis window controlled schemes.

3.1 Concept and Operational Principle

Phase-Locked Loop (PLL) is the most precise way of stabilizing the switching frequency of ripple based controllers since PLL synchronizes the phase and frequency of an oscillating signal to a reference clock. The design in [18] is one of the early works that synchronizes the switching frequency of a converter to a reference clock using a PLL.

Figure 21 shows a basic block diagram of a PLL and Figure 22 shows the proposed fixed frequency ESR-controlled hysteretic buck converter. Comparing Figure 22 to 21, the entire hysteretic buck converter is modeled as a voltage-controlled oscillator (VCO) with the gate control signal of the converter representing the oscillating signal (OSC) of a PLL and the ESR control signal being the PLL control voltage (V_{CTRL}).

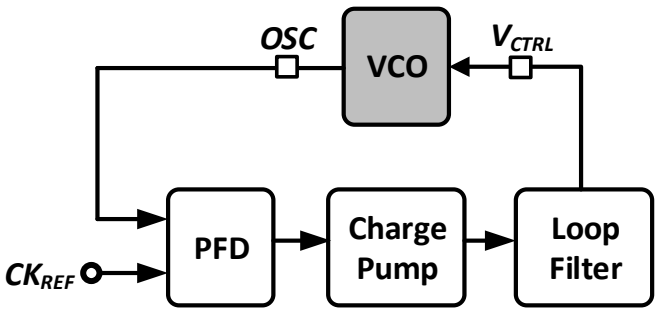

Figure 21: Block Diagram of a Simple PLL

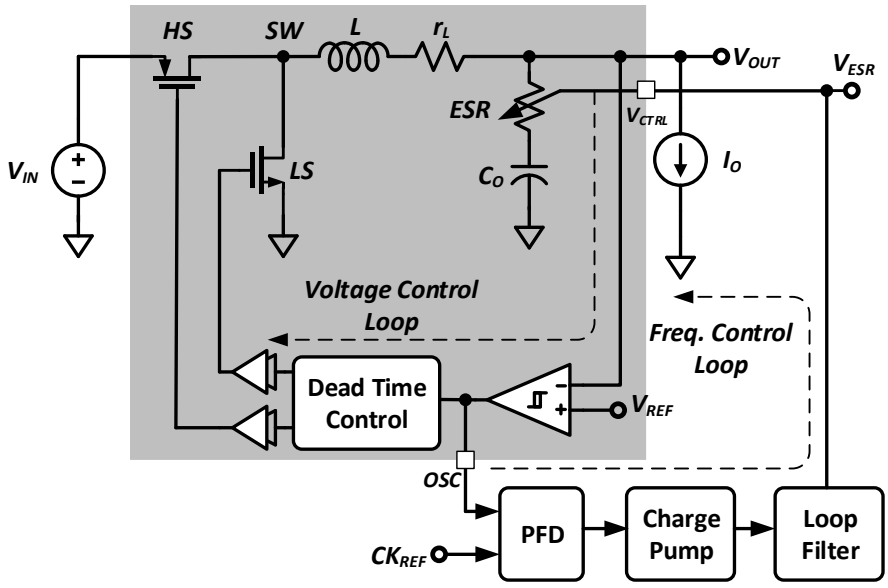

Figure 22: Proposed ESR-Controlled Hysteretic Buck Converter

Figure 23 shows how the ESR tuning is realized: An NMOS device in triode region is connected in series with the output capacitor to introduce a variable resistance $\boldsymbol{ESR_{VAR}}$. The phase/frequency detector (PFD) compares the converter switching frequency with the clock reference and generates an error signal. The charge pump with loop filter averages the error signal and generates a voltage control signal to tune $\boldsymbol{ESR_{VAR}}$ in order to synchronize the operating frequency to the reference clock.

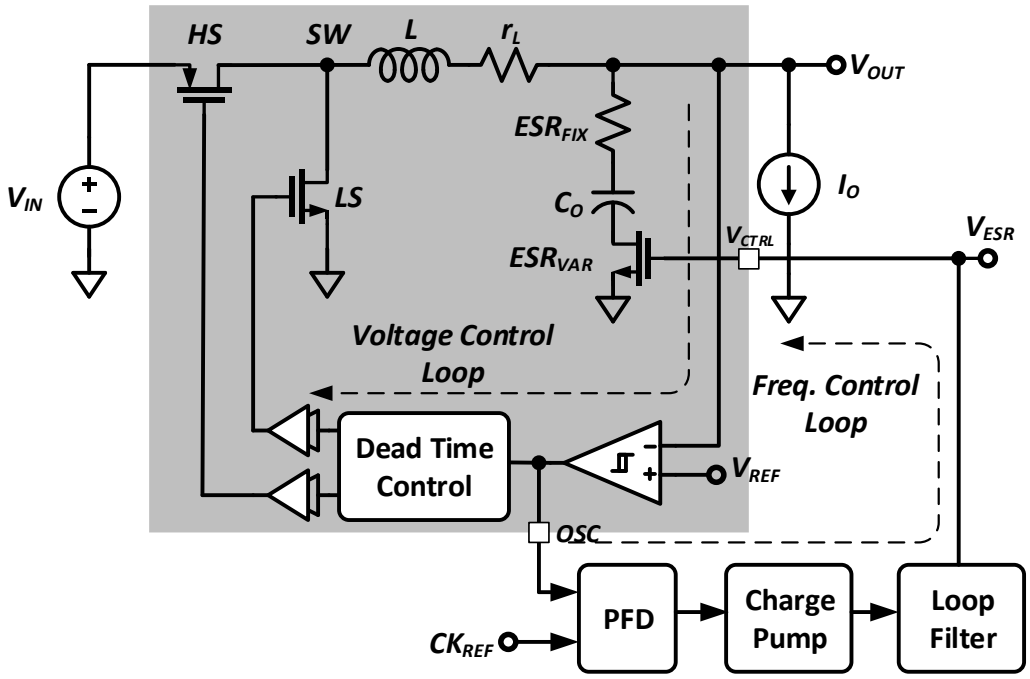

Figure 23: Proposed Architecture with NMOS ESR Tuning

From (7), converter switching frequency can be controlled by adjusting loop delay ($\boldsymbol{t_D}$), size of hysteresis window ($\boldsymbol{V_H}$), ***ESR*** and ***ESL*** of output capacitor. Many works have controlled the delay ($\boldsymbol{t_D}$) and size of hysteresis window ($\boldsymbol{V_H}$) to stabilize the switching frequency.

$$f_S = \frac{V_O}{V_{IN}} . \frac{(V_{IN} - V_O).(\boldsymbol{ESR} - {}^{\boldsymbol{t_D}}/_{C_O})}{(V_{IN}.\boldsymbol{ESR}.\boldsymbol{t_D} + \boldsymbol{V_H}.\{L - \boldsymbol{ESL}\}.V_{IN})} \tag{7}$$

None of the reported works have controlled the capacitor ***ESR*** to stabilize the operating frequency since it is a good practice to keep ***ESR*** low in most converters. But the proposed design adjusts the ***ESR*** since hysteretic converters need significant ***ESR*** to

be able to sense changes in load current; thus ESR tuning would not be a drawback in hysteretic converters.

3.2 Circuit Implementation

The proposed design as shown in Figure 23 consists of a voltage control loop and a frequency stabilization control loop. The voltage control loop is a buck converter with hysteretic mode control and the frequency control loop is a phase-locked loop which synchronizes the phase-frequency of ***OSC*** to a reference clock.

3.2.1 Voltage Control Loop

The hysteretic converter is also referred to as a bang-bang or ripple based controller because it regulates the output voltage in a voltage window. The controller has a hysteretic comparator which uses a voltage reference to generate low and high voltage thresholds to define the hysteresis window. During load transients, an overshoot or undershoot causes the output voltage to exit the hysteresis window. The hysteretic controller keeps the high side switch HS on (off) and the low side switch LS off (on) when an undershoot (overshoot) occurs till the output voltage returns to the hysteresis window. This operation gives the ripple based controller a fast transient response and a wide duty ratio range from 0.0 to 1.0. Also the response time of this controller depends on the delay due to the comparator and gate drivers only.

Also the hysteretic controller is simple and needs no phase compensation network because the control signal does not experience the phase change that comes with using high-gain error amplifier.

The controller uses the output ripple to sense load transients. During load changes, the output capacitor either sinks or source the transient current (i_T). The output voltage experiences an overshoot or undershoot ($i_T . ESR$) if the capacitor ESR is significant and the controller thus sense the load transient through the output voltage feedback. The output voltage feedback is not restrict by any compensation network.

All the benefits of the hysteretic control considered makes it the faster than the other conventional controllers and suitable for the frequent high-slew rate load applications. But the controller has one major downside; its switching frequency is variable and depends on almost all the parameters of the converter. The switching frequency of the hysteretic converter is shown in (7) to depend on the input voltage (V_{IN}), the expected output voltage (V_O), controller delay (t_D), and parameters of the output filter: inductance (L), output capacitance (C_{OUT}), equivalent series resistance (ESR), and equivalent series inductance (ESL), and to a small extent on load I_O [19].

MOSFETs (metal-oxide-semiconductor field-effect transistor) are used to realize the two switches of the power stage of a converter in active or synchronous rectification. This technique reduces the conduction losses of the switches and thus improve the overall efficiency of the converter especially for low voltage applications. Diode rectification on the other hand uses an actively controlled device for the high side switch and a diode for the low side switch. Synchronous rectification achieves less losses and higher efficiency

compared to diode rectification since actively controlled devices have less voltage drop than the built-in voltage of diodes.

The LC low-pass filter of the power stage must be designed to assist and relax the fast response of the high-slew rate behavior of the load while considering the switching frequency of the converter.

3.2.1.1 Output Capacitance Selection

With the conventional controllers such as voltage and current mode PWM controllers, the size of the output filter capacitor is determined using the specified maximum output voltage ripple. But in hysteretic controllers, the size of the output ripple is predetermined mainly by the comparator's hysteresis window. Thus the output capacitor is designed to optimize the transient response of the converter and not to set the output ripple.

The filtering capacitor must be sized to limit the overshoots and undershoots during load transients to the specified voltage tolerance. This requires that the rate of change of capacitor voltage during load transient be as small as possible. From (8) the rate of change of capacitor voltage is inversely proportional to the capacitance, thus a large capacitor will be desired for good transient response.

$$\frac{dv_C(t)}{dt} = \frac{i_C(t)}{C} \tag{8}$$

Intuitively, the filtering capacitor should be large enough for the capacitor current to complement the inductor current in sourcing the load current during load step-up transients. Likewise, a large capacitance would be able to sink more current during load

step-down transients and still have a small change in voltage. Thus large capacitance is desired for good load transient performance.

3.2.1.2 Output Inductance Selection

Similar to the output capacitance, the output filter inductance is selected to satisfy the required transient response specifications. During load transients, the LC filter should be able to sink or source the transient load. To source load transients during load step-up, the rate of change of inductor current must be high so as to quickly supply the new high load current.

In similar fashion, during load step-down transients, a high rate of change of inductor current would allow the inductor current to quickly drop to the new low load in a short response time. Small inductance is desired since the rate of change of inductor current is inversely proportional to the size of inductance as shown in (9).

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} \tag{9}$$

3.2.1.3 Hysteretic Comparator

Figure 24 show a schematic diagram of a hysteretic comparator. The comparator has a first stage differential amplifier and a Schmitt trigger to generate sharp output transitions. The hysteresis window (v_{TH}) of the comparator is realized by changing the bias current of the input transistor M2b. When the output signal (OUT) is low, the bias currents of the input transistors are equal and the comparator trips when $v_P > v_N$ or vice versa. On

the other hand, when OUT is high the bias current of M2b increases by I_H and the comparator trips at (v_P + v_{TH}) > v_N or vice versa.

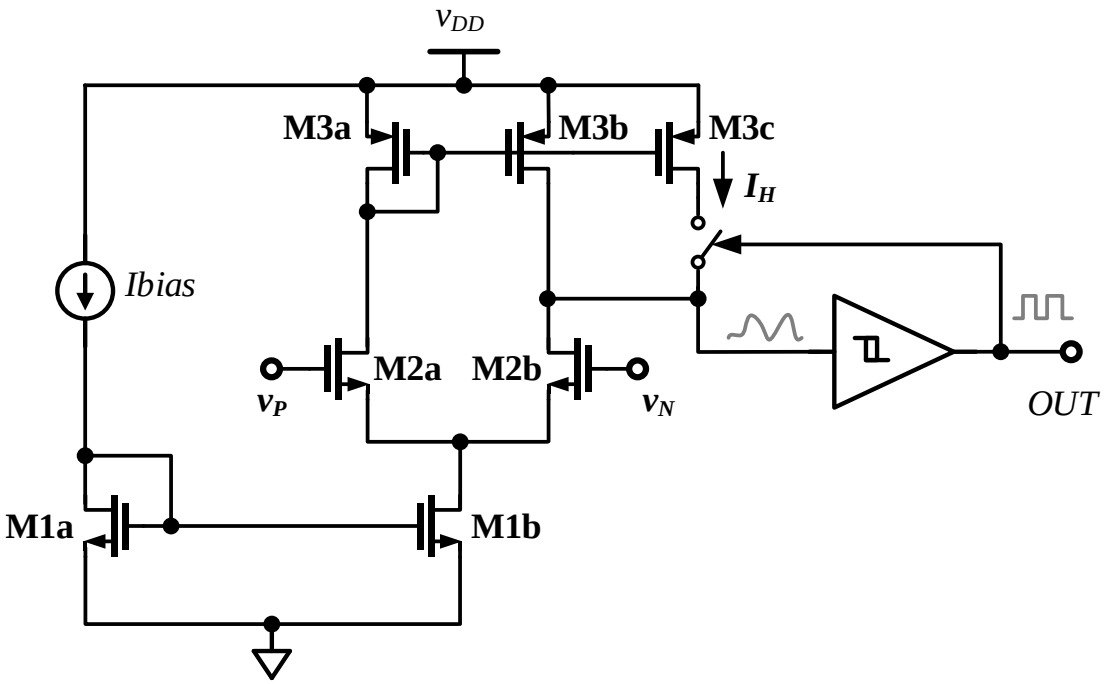

Figure 24: Comparator with Hysteresis

The Schmitt trigger translates the slow edges of the comparator's first stage into a fast-switching clock signal. If a simple buffer (two cascaded inverters) was used instead of the Schmitt trigger, the rising and falling trip points would occur at the same threshold

as shown in Figure 25. This makes a simple buffer undesirable; the comparator would produce glitches at the output if there is any noise on the input(s). The Schmitt trigger solves this problem by separating the rising threshold from the falling threshold and maintaining a reasonable hysteresis window between the two thresholds as shown in Figure 26.

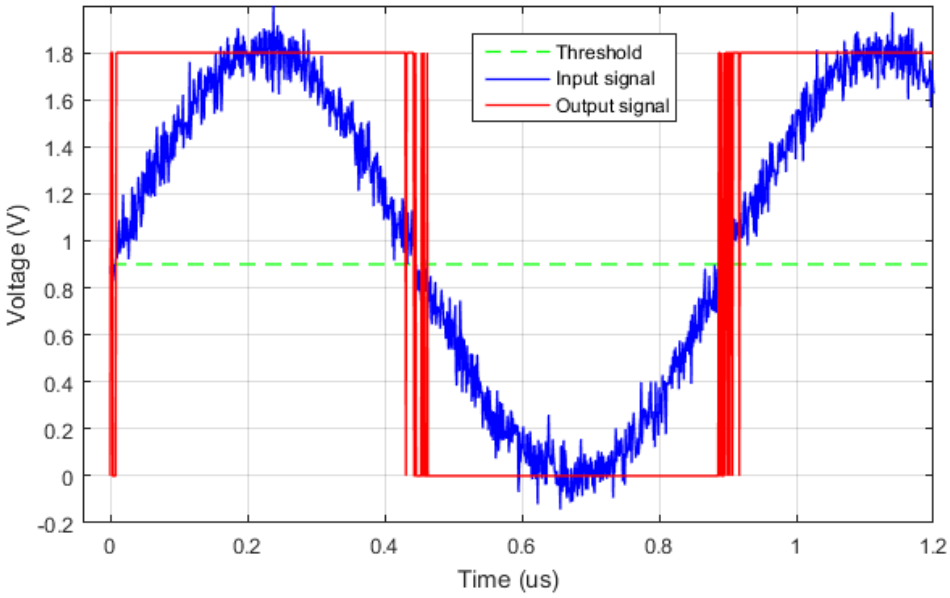

Figure 25: Dynamic Behavior of a Simple Buffer

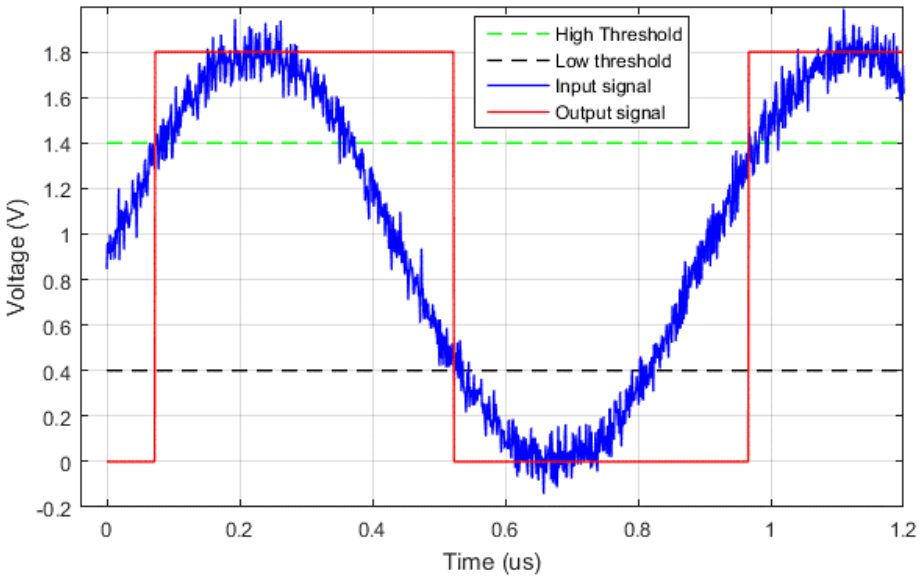

Figure 26: Dynamic Behavior of Schmitt Trigger

The Schmitt trigger was realized using MOSEFET devices only as shown in Figure 27. The concept of drain induced barrier lowering (DIBL) was implemented to reduce the threshold voltages of devices P3 and N3. Drain induced barrier lowering is a short-channel effect which reduces the threshold voltage of a device due to a high drain to source voltage.

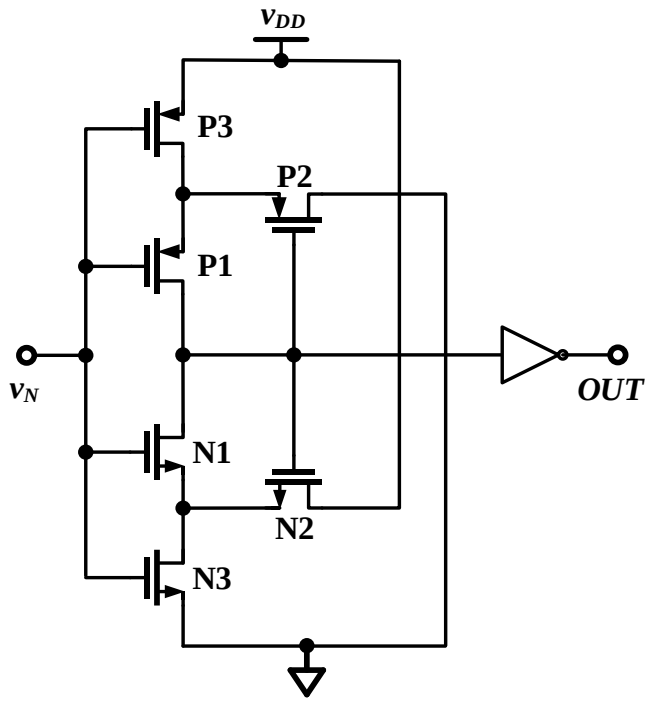

Figure 27: Schematic of Schmitt Trigger

In both the Schmitt trigger and the simple buffer the first stage determines the rising and falling thresholds. The cascode devices (P3, P1) and (N3, N1) help the Schmitt trigger to separate its rising and falling thresholds. Before the output of the Schmitt trigger switches from low to high, (P1, P3 and N2) will be on while (N1, N3 and P2) are off. And N2 pulls the drain of N3 to v_{DD} which makes N3 ready to turn on at a lower threshold than normal due to the effect of DIBL. Similarly just before the output switches from high to low, (N1, N3 and P2) will be on while devices (P1, P3 and N2) are off with P2 pulling the drain of P3 to ground. P3 is conditioned to turn on at a lower threshold due to DIBL effect.

3.2.1.4 Adaptive Dead Time Control

Adaptive dead-time control ensures that the main switches of the power stage are controlled so as to prevent high shoot-through current during transitions. The low-side FET is turned on only when the voltage at the switching node SW is low. Likewise the high-side FET turns on only when the low-side FET is off. The diagram in Figure 28 shows how the signals for the high-side and low-side drivers are conditioned to avoid overlap and shoot-through current.

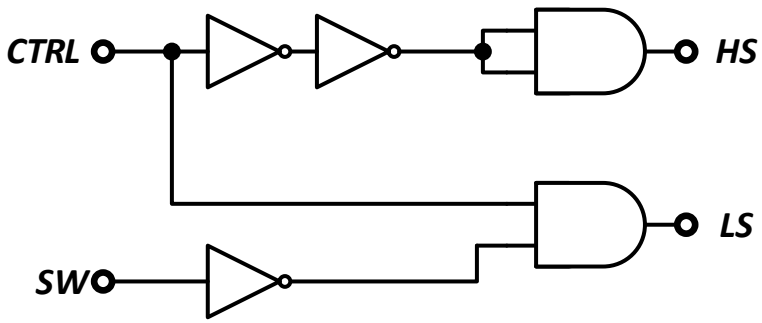

Figure 28: Adaptive Dead Time Control

3.2.1.5 Gate Drivers

The high side switch (HS) and low side switch (LS) of the power stage are driven by separate gate drivers in order to optimize the dead time control and reduce switching losses during turn-on/turn-off transitions. Each gate driver is made of four inverter stages

with increasing amplification factor from the input to output as shown in Figure 29. The design of each stage depends on the load that stage drives. For instance the last stage (P4, N4) drives the large parasitic gate capacitance of the switching FETs hence the last stage's transistors are designed to have small on-resistance to charge (discharge) the gate capacitance fast enough to switch the FETs.

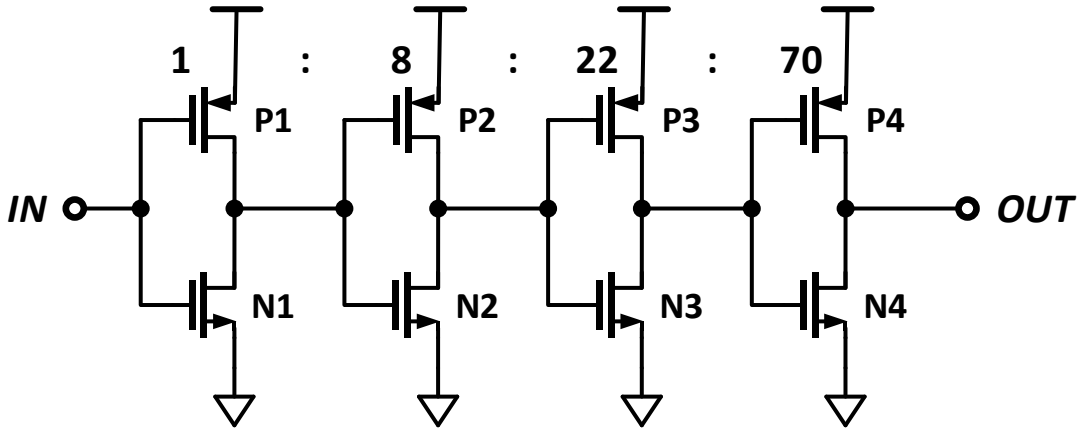

Figure 29: Gate Driver Schematic

3.2.2 Frequency Control Loop

The frequency control loop is a third-order Type II charge pump PLL with the hysteretic converter controlled as a VCO (voltage controlled oscillator). During frequency transients, such as start-up or load transients, the PLL regulates the ESR to first of all lock the switching frequency to the reference clock. When the PLL is frequency locked, the

PFD acts as a phase detector to phase-lock the converter's gate control signal to the reference clock.

3.2.2.1 Phase-Frequency Detector

The phase-frequency detector compares the clock reference to the converter's gate control signal and generates an error pulse whose average corresponds to the difference in phase($\Delta\emptyset$) and frequency($\Delta\omega$) between the two signals. Figure 30 shows a digital implementation of the PFD with two resettable D flip-flops and an AND gate to reset the flip-flops [22]. The flip-flops are edge-triggered with their D inputs tied to the power supply and the signals to be compared serve as clock inputs. Each D flip-flops can be replaced by the digital circuit in Figure 31 with two SR latches cross-coupled. Latch 1 and 2 respond to the rising edge of *Clk* and *Reset* respectively. Figure 32 shows the modified PFD with cross-coupled latches. A charge pump with loop filter averages the two error pulses (Q_A, Q_B) from the PFD as shown in Figure 33.

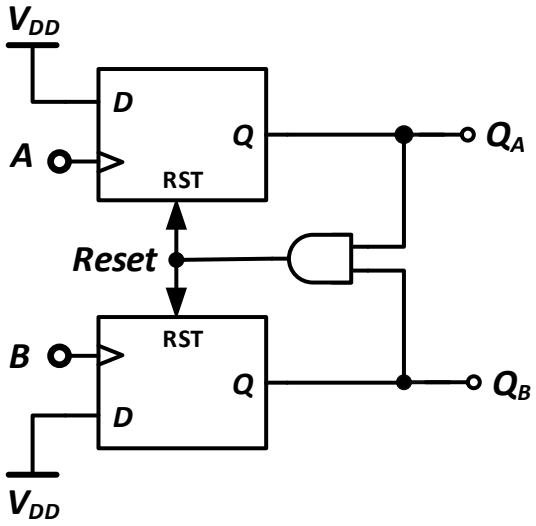

Figure 30: PFD with DFF.
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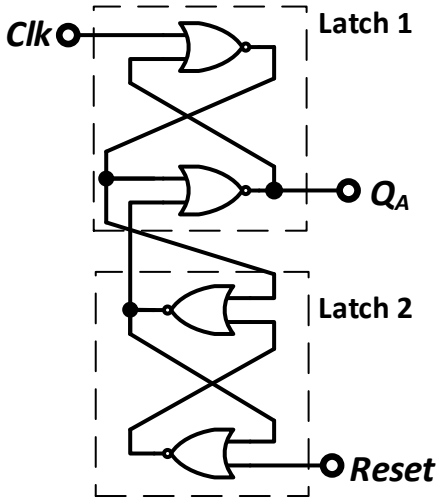

Figure 31: DFF with Cross-Coupled SR Latches.
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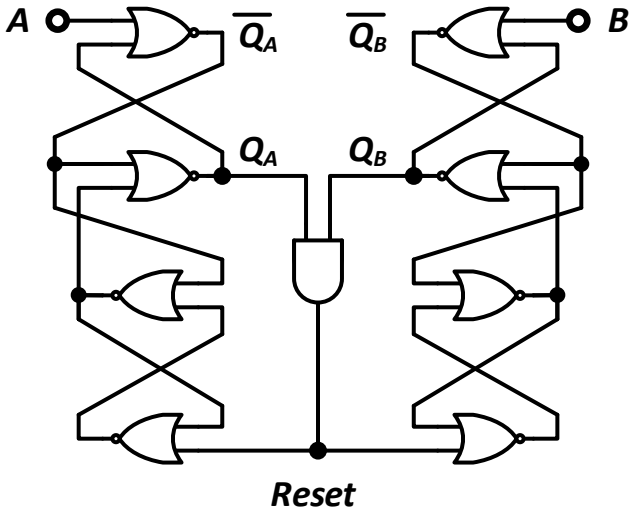

Figure 32: PFD with Cross-Coupled Latches.
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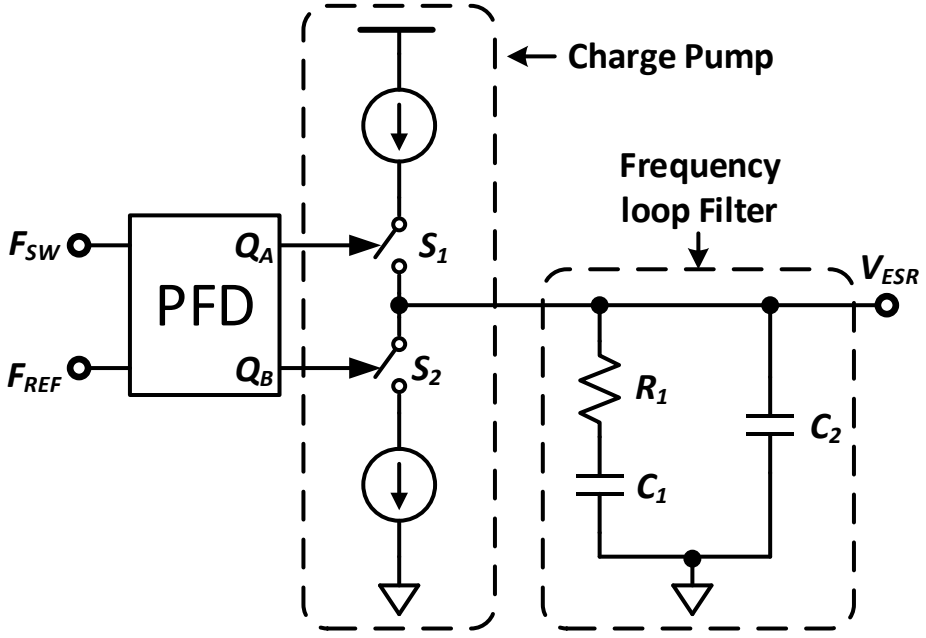

Figure 33: Charge Pump PLL

3.2.2.2 Charge Pump

The charge pump sinks or sources current into or out of the frequency loop filter depending on the error pulses it receives from the PFD. Figure 34 is a transistor level implementation of the charge pump. The 30µA sink and source currents through devices M1a and M4a are copied from a 10µA source using current mirrors. Switches S1 and S2 in Figure 33 are realized with transistors M2a and M3a respectively. Since S1 was realized with a PMOS device, $\overline{Q_A}$ an inverted signal of Q_A from the PFD is used to control transistor M2a. Complementary devices M2b and M3b turn on when M2a and M3a turn off to keep the source and sink currents through M1a and M4a actively on and reduce transient glitches.

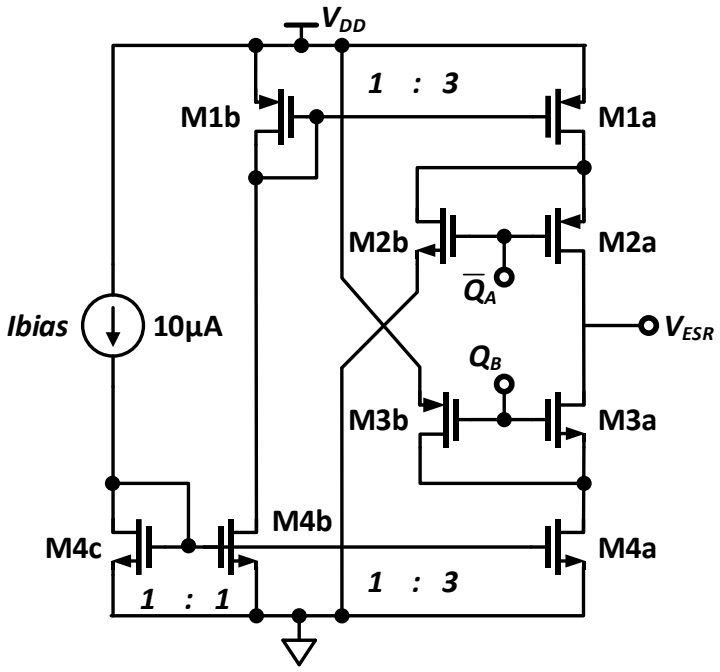

Figure 34: Transistor Level of Charge Pump

3.2.2.3 Loop Filter

A second order loop filter is used in the frequency control loop to ensure closed loop stability and integrate the error due to changes in phase/frequency for frequency control voltage V_{ESR} Generation. Capacitor C1 is the main integrating capacitor and resistor R1 is connected in series with C1 to introduce a zero in the loop for stability. When the PLL locks, non-idealities such as mismatches between sink-source currents of charge pump adds a ripple to the control voltage V_{ESR}. A secondary capacitor C2 is added to further filter the control voltage ripple.

In this work the second order filter had C_1 = 396pF, C_2 = 24pF, and R1 = 54.2k**Ω**. The area needed by C_1 was reduced by impedance scaling: - a small capacitor C_S is impedance scaled to realize the large capacitor C_1 and reduce the area C_1 would have occupied. Figure 35 shows the concept of impedance scaling or capacitor multiplier. The equivalent impedance seen at node V_{in} is inversely proportional to the current at constant voltage. Thus the impedance ($^1/_{C_S}$) at node V_{in} can be reduced by a factor of M if a current source could sink an M-times amplified current of the capacitor current (i_C) as expressed in (10). The impedance scaler multiplies capacitance C_S by a (1+M) factor. [20]

$$Z_{in} = \frac{V_{in}}{i_{in}} = \frac{1}{s(1+M)C_S} \tag{10}$$

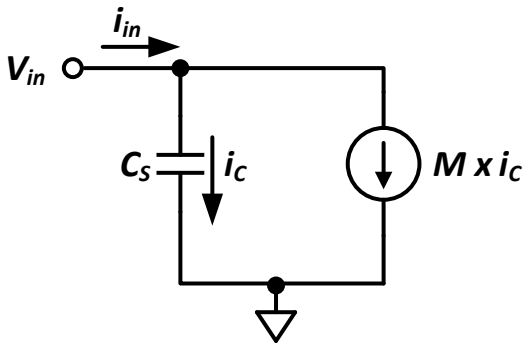

Figure 35: Impedance Scaling Concept.
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The schematic in Figure 36 is a transistor level implementation of the capacitance multiplier. The capacitor current is mirrored and amplified by a factor of 10. The amplified current is sourced from the same voltage node as the capacitor to reduce the effective impedance and thus amplify the capacitance seen at the node by a factor of 11. Cascode current mirrors with long devices are used to reduce current mismatches and leakage current at nodes A and B. [21]

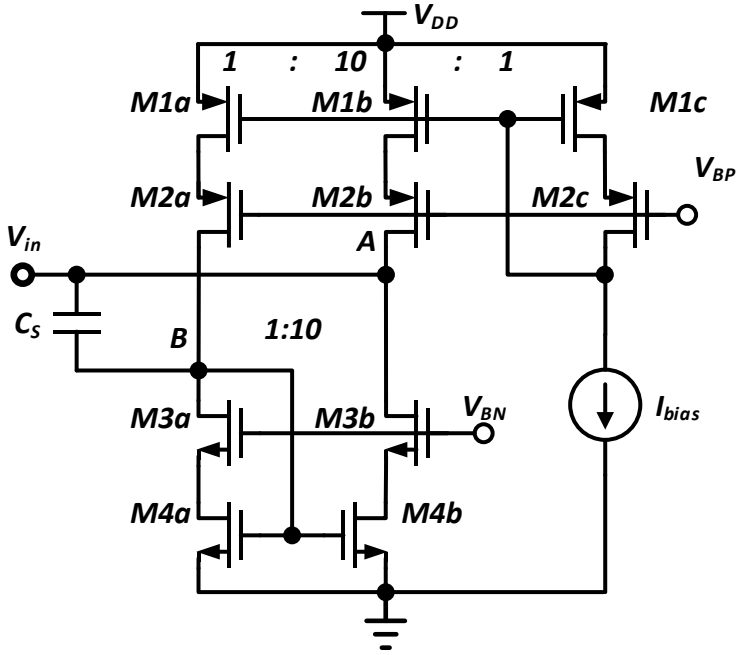

Figure 36: Transistor Level of Capacitor Multiplier.
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3.2.3 Auxiliary Circuits

3.2.3.1 External Clock Synchronizer

An external clock is used to realize the reference clock of the Frequency Control Loop since all microprocessor applications inherently have clocks. External synchronization of the reference clock to the processor clock eliminates the need of designing a clock generator on the power management chip; thus it saves chip area and

power. A frequency divider can be used to scale down high clock frequency into the megahertz (MHz) range for the frequency control loop.

Figure 37 shows a diagram of the external clock synchronizer. The basic concept is to generate a triangle wave signal whose frequency is equal to the external clock frequency, compare the generated triangle wave with two voltage levels, and regenerate a clock on chip with frequency equal to the external clock frequency.

A clean triangle wave can be generated if the time-constant $R_{RC}C_{RC} << 1/f_{REF}$. Resistance R_{RC} is selected so as to keep the discharge current < 10µA.

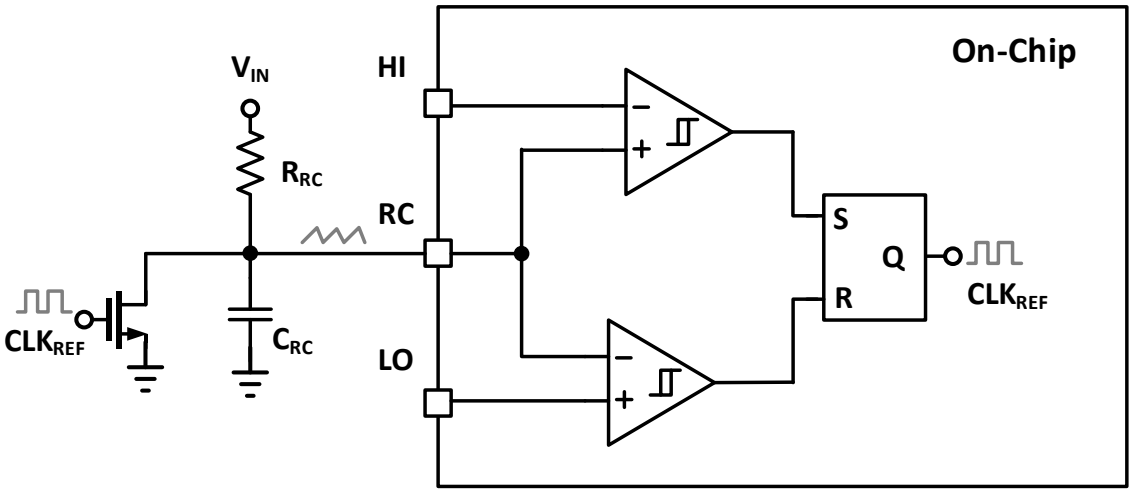

Figure 37: External Clock Synchronizer

3.2.3.2 Bias Current Generator

The bias currents of the various schematic blocks are generated by the Bias Current Generator. Figure 38 shows a schematic of a simple bias current generator. A 1µA source current is generated and mirrored to give five bias currents for the comparators, charge pump and capacitor multiplier. A cascode of long channel devices M4 – M7 is used to realize a resistance of ~1.8MΩ to generate the 1µA current source.

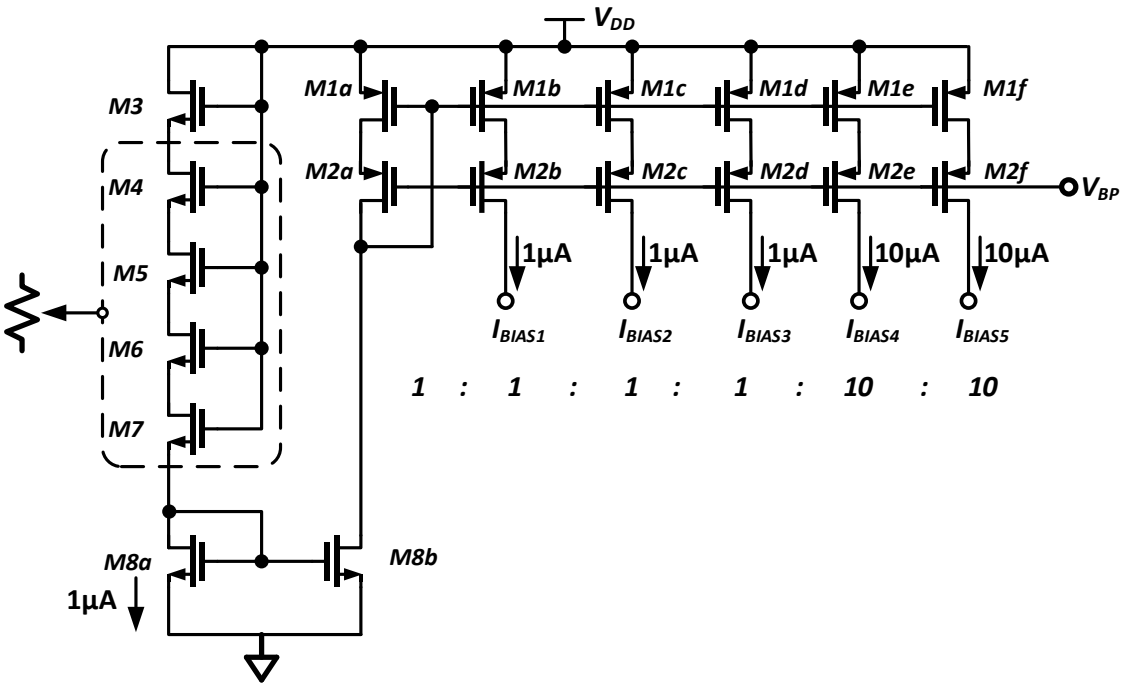

Figure 38: Bias Current Generator

3.3 Stability Analysis

Figure 39 shows a model of the closed loop synchronized third-order type-II analog charge-pump PLL.

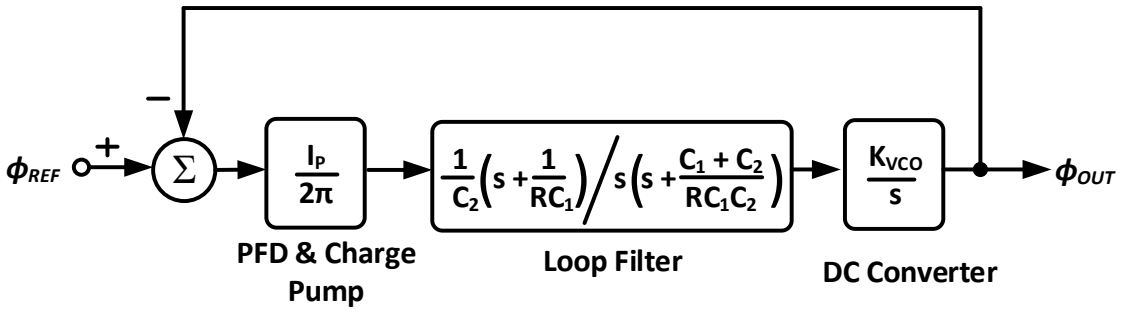

Figure 39: Third-Order Type-2 Charge Pump PLL Model

The closed loop response relating the output phase ϕ_{OUT} and reference phase ϕ_{REF} using the model in Figure 39 is derived.

Forward Path Gain:

$$G(s) = \frac{K_{PD}K_{VCO}F(s)}{s}$$

Where $F(s)$=Loop filter transfer function

K_{PD}= Gain of PFD and Charge Pump

K_{VCO}= DC Gain of DC converter

Closed loop transfer function: $H(s) = \frac{\phi_{OUT}(s)}{\phi_{REF}(s)} = \frac{G(s)}{1+G(s)}$

$$H(s) = \frac{K_{PD}K_{VCO}.{}^{1}/_{C_2}.(s + {}^{1}/_{R_1C_1})}{s^3 + s^2\left(\frac{C_1 + C_2}{R_1C_1C_2}\right) + s\left(\frac{K_{PD}K_{VCO}}{C_2}\right) + \frac{K_{PD}K_{VCO}}{R_1C_1C_2}}$$

Since the third pole is at high frequency, the denominator H(s) can be approximated as a second-order system. In control theory the denominator can be expressed by (11)

$$Denominator = s^2 + 2\zeta\omega_n s + \omega_n^2 \tag{11}$$

Where ζ = damping factor, and ω_n = natural frequency = loop bandwidth

Using the approximated second-order system, the loop bandwidth is expressed by (12) and dependent on K_{VCO} of converter while the damping factor as expressed in (13) is proportional to the loop bandwidth. It is desired for the system to have large loop bandwidth to enhance the dynamic response and give the system a critical damping response to transients with less ringing.

$$\omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{C_2}} \tag{12}$$

$$\zeta = \frac{\omega_n}{2} RC_1 \tag{13}$$

Using the expression of the switching frequency in (14), the nominal switching frequency (ω_O) and the desired synchronizing switching frequency (ω_s) are given by (15) and (16) respectively

$$f_S = \frac{V_O}{V_{IN}}.\frac{(V_{IN} - V_O).(\boldsymbol{ESR} - {}^{\boldsymbol{t_D}}/_{C_O})}{(V_{IN}.\boldsymbol{ESR}.\boldsymbol{t_D} + \boldsymbol{V_H}.\{L - \boldsymbol{ESL}\}.V_{IN})} \tag{14}$$

$$\omega_O = \frac{2\pi D(1 - D).(\boldsymbol{ESR} - {}^{t_D}/_{C_O})}{(\boldsymbol{ESR}.t_D + V_H.\{L - ESL\})} \tag{15}$$

$$\omega_s = \frac{2\pi D(1-\ D).(\boldsymbol{ESR} + \Delta\boldsymbol{esr} - {}^{t_D}/_{C_O})}{(\{\boldsymbol{ESR} + \Delta\boldsymbol{esr}\}.t_D + V_H.\{L - ESL\})} \quad (16)$$

Where duty ratio $D = {}^{V_O}/_{V_{IN}}$, $\Delta\boldsymbol{esr} = K_{ESR}V_{ESR}$, K_{ESR}= Gain of ESR, and V_{ESR}= ESR control voltage.

For the voltage controlled oscillator,

$$\omega_s = \omega_o + K_{VCO}.V_{ESR} \quad (17)$$

From equations (15), (16) and (17)

$$\omega_s - \omega_o = \frac{2\pi D(1-\ D).\Delta\boldsymbol{esr}.({}^{t_D{}^2}/_{C_O} + V_H.\{L - ESL\})}{(\{\boldsymbol{ESR} + \Delta\boldsymbol{esr}\}.t_D + V_H.\{L - ESL\}).(\boldsymbol{ESR}.t_D + V_H.\{L - ESL\})}$$

$$K_{VCO} = \frac{2\pi D(1-\ D).K_{ESR}.({}^{t_D{}^2}/_{C_O} + V_H.\{L - ESL\})}{(\{\boldsymbol{ESR} + \Delta\boldsymbol{esr}\}.t_D + V_H.\{L - ESL\}).(\boldsymbol{ESR}.t_D + V_H.\{L - ESL\})} \quad (18)$$

From (18) with constant converter parasitic and fixed switching frequency, K_{VCO} depends on the operating duty ratio (D) and thus K_{VCO} will vary with varying input and output voltages.

The open loop transfer function of the frequency control loop in (19) is analyzed for stability of the closed loop PLL. There are two poles at the origin, a zero at ${}^{1}/_{R_1C_1}$ and a third pole at $\frac{C_1+C_2}{R_1C_1C_2}$. Figures 40 and 41 show bode plots of the open loop transfer function with their stability characteristics. The plots show that the closed loop PLL will be stable for the range $K_{VCO1} \leq K_{VCO} \leq K_{VCO3}$ with loop bandwidth $13kHz \leq \omega_n \leq 103kHz$ and phase margin $47.3° \leq \emptyset_m \leq 63°$. Though K_{VCO1} can be reduced to widen

the K_{VCO} range and still achieve a good phase margin of about $45°$, the loop bandwidth would decrease and degrade the dynamic response.

$$G(s) = \frac{K_{PD}K_{VCO}F(s)}{s}$$

$$G(s) = \frac{K_{PD}K_{VCO}.{}^{1}/_{C_2}.(s + {}^{1}/_{R_1C_1})}{s^2.(s + \frac{C_1 + C_2}{R_1C_1C_2})} \tag{19}$$

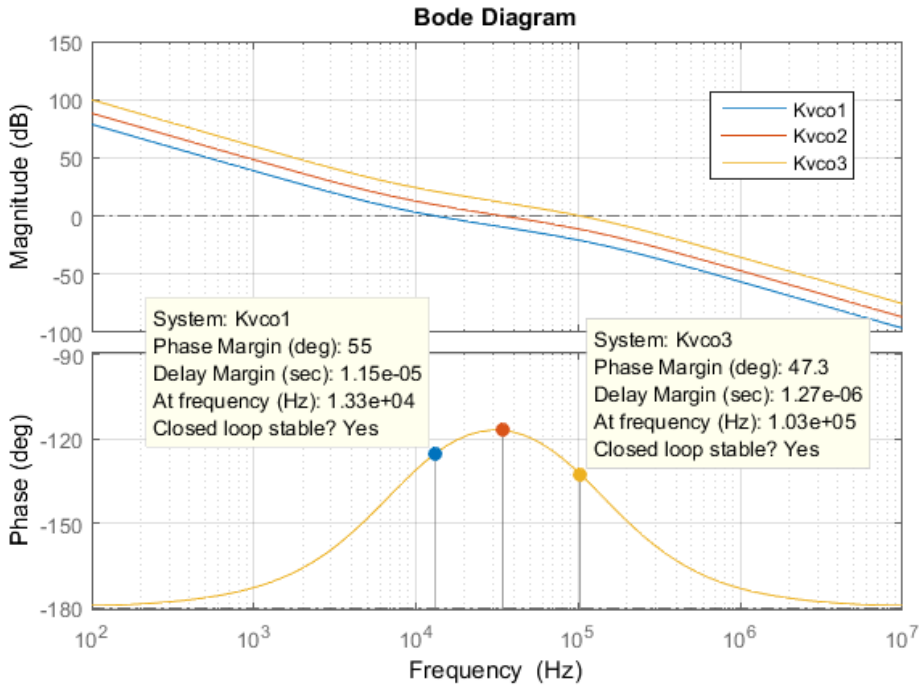

Figure 40: PLL Bode Plots with Bandwidth Range

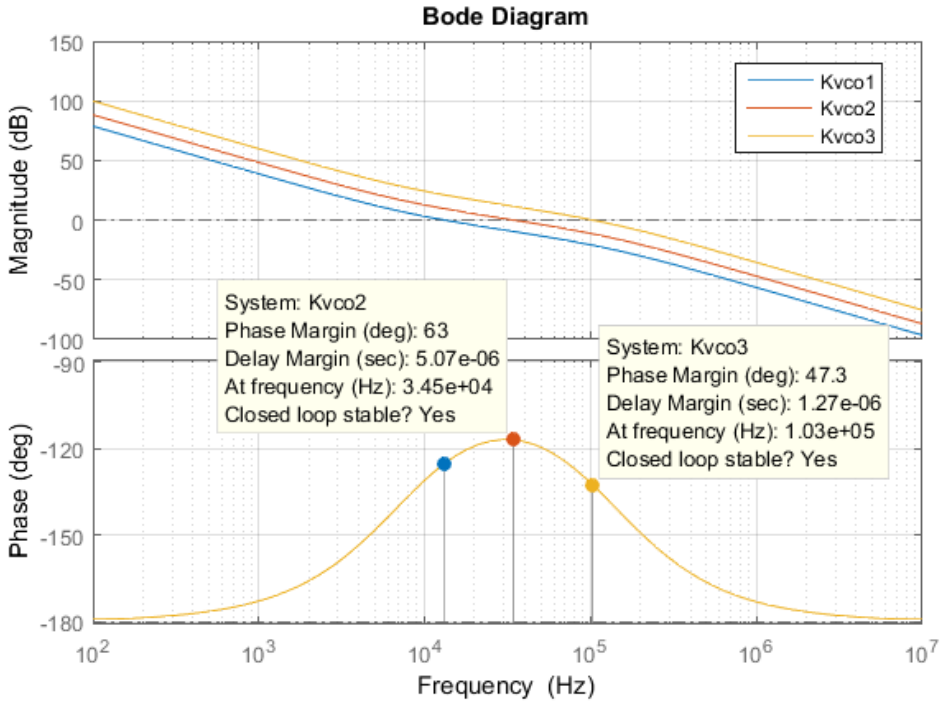

Figure 41: PLL Bode Plots with Phase Margin Range

3.4 Results

The proposed fast transient response fixed frequency converter was designed in 0.18µm IBM CMOS process.

3.4.1 Steady State Performance

The steady state of converter operating frequency after 40µs shows a 1.6% variation in frequency as shown in Figure 42 for $3.9mA \leq I_{OUT} \leq 500mA$ and a refernce tracking range of $0.7V \leq V_{REF} \leq 1.0V$. Figure 43 shows the switching frequency

stabilization with time. It can be observed from Figures 42 and 44 that the switching frequency had not settled yet at 40µs for $V_{REF} = 0.8V$. Thus the frequency variation is expected to reduce with operating time. The delayed settling time in the case of $V_{REF} = 0.8V$ is due to the limit on K_{VCO} stability range as discussed in section 3.3.

Figures 44 and 45 show the stabilization of switching feequency with load and varying input voltage with 0.1% frequency variation. Figures 42 – 45 confirms the independence of the synchronized frequency on load, input and output voltage.

The voltage regulation module achieves a 95.9% maximum efficincy at 232mA of load currrent as shown in Figure 46.

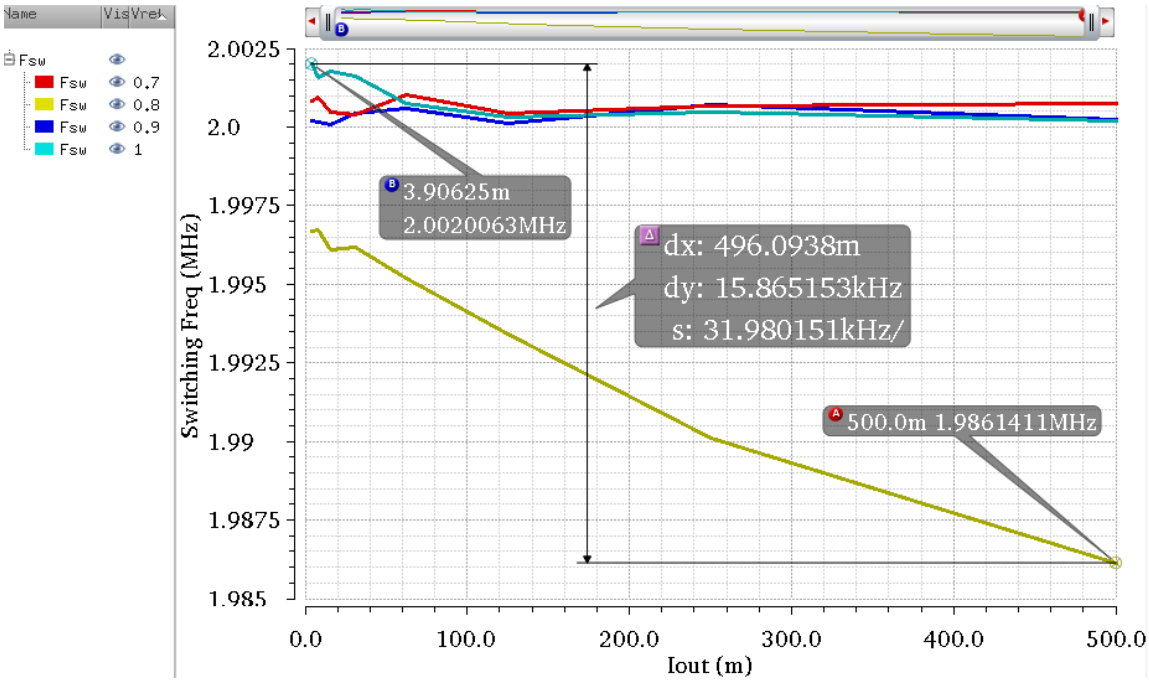

Figure 42: Steady State Frequency with Varying Load and Reference Tracking

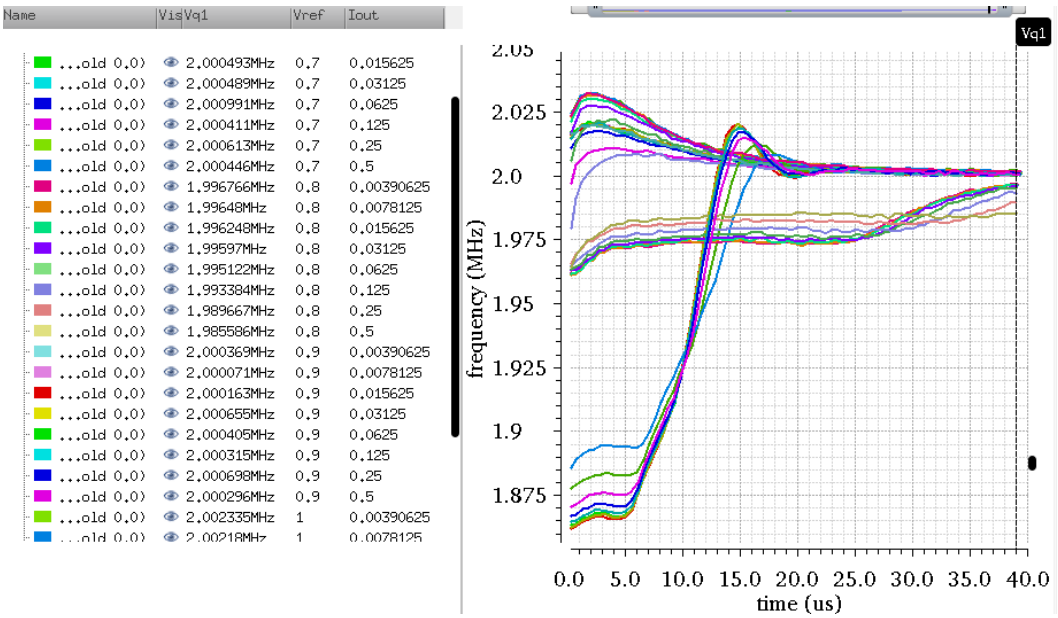

Figure 43: Switching Frequency Stabilization with Varying Load

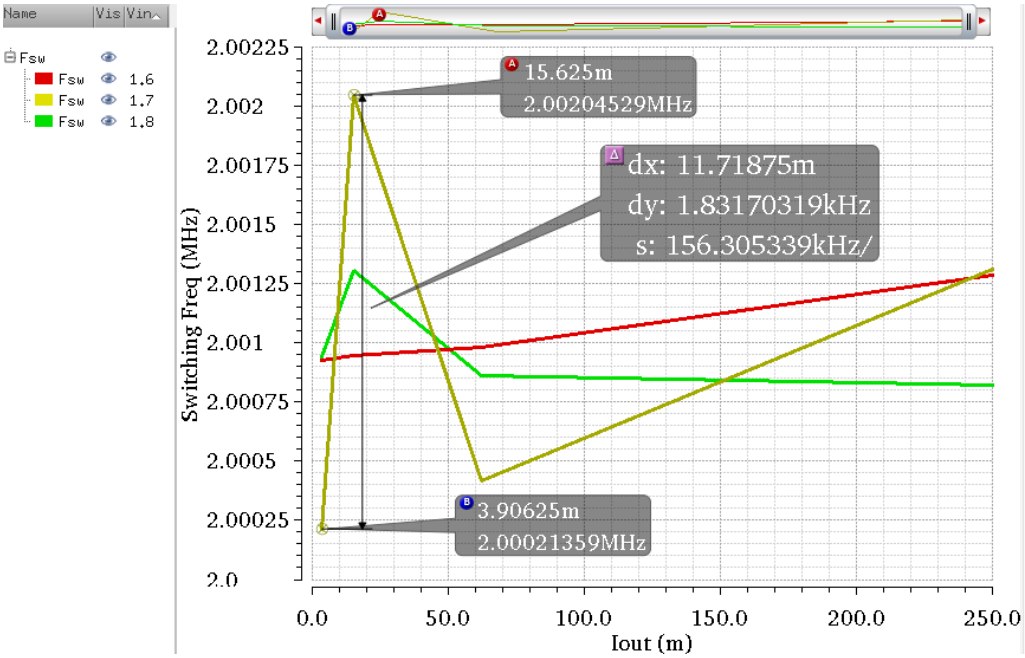

Figure 44: Steady State Frequency with Varying Load and Input Voltage

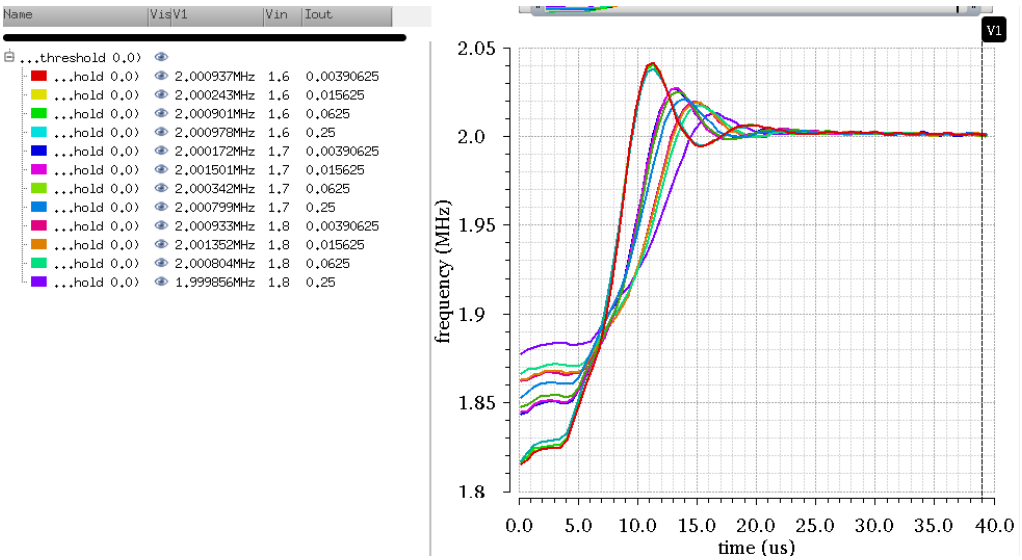

Figure 45: Switching Frequency Stabilization with Varying Load

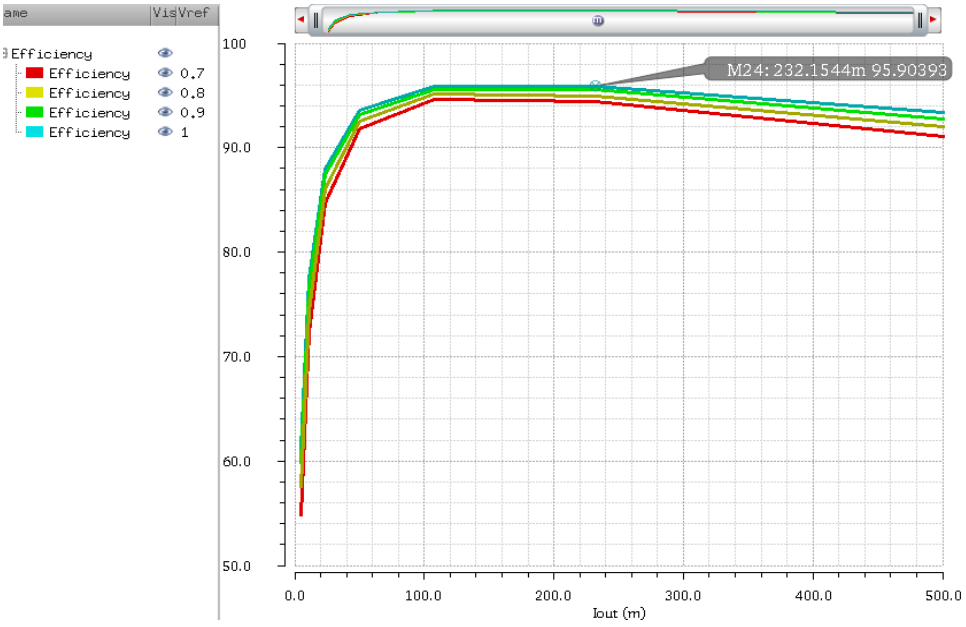

Figure 46: Converter Efficiency

3.4.2 Dynamic Performance

Figure 47 shows the reference tracking performance of the proposed converter with < 2µs of transient response time and <50mV voltage excursions. This shows the ability of the converter solution to perform dynamic voltage scaling (DVS) for power management. The regulator's line transient response shown in Figure 48 at $V_{REF} = 0.8V$ and $1.6V \leq V_{IN} \leq 1.8V$ has almost zero voltage droop at input voltage transitions.

Also for a 500mA load step at $V_{REF} = 0.9V$ and $V_{IN} = 1.8V$, the converter achieves overshoot and undershoot voltages of 37mV and 45mV with 0.44µs and 0.51 µs transient response time respectively as shown in Figures 49 and 50.

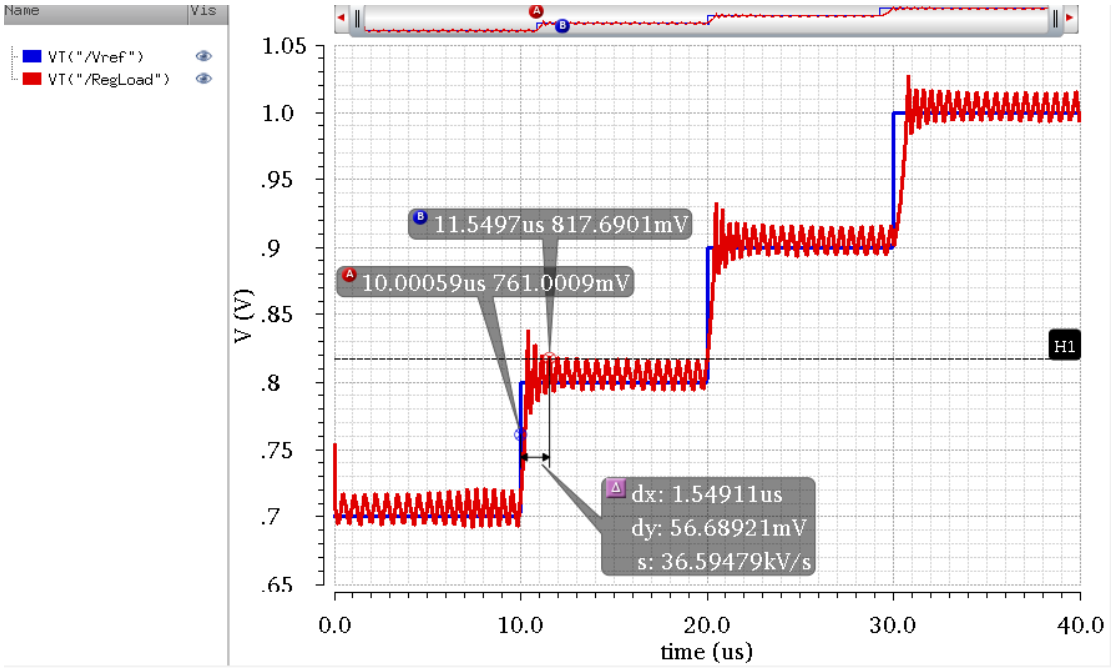

Figure 47: Dynamic Reference Tracking Response

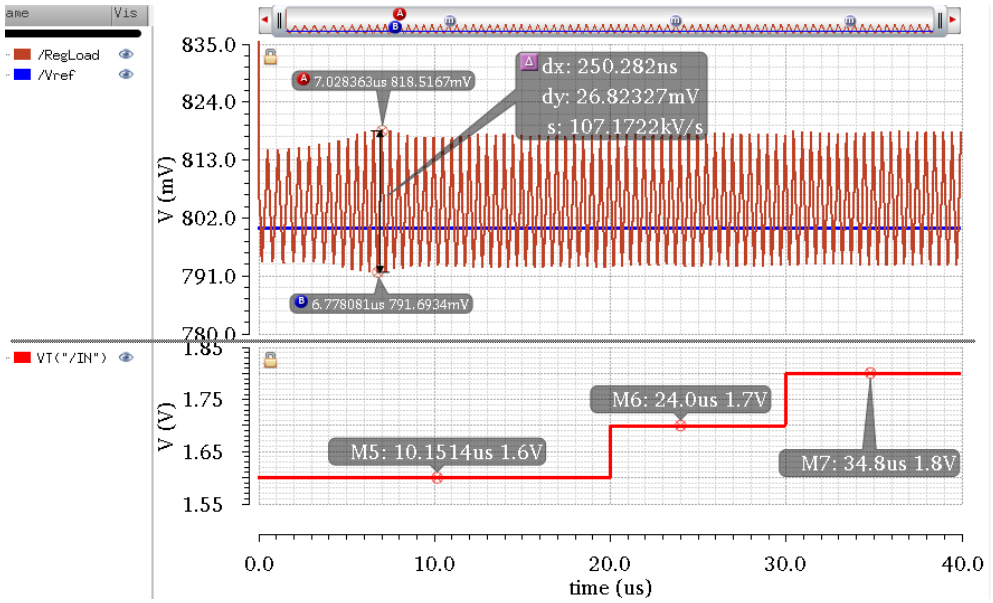

Figure 48: Line Transient Response

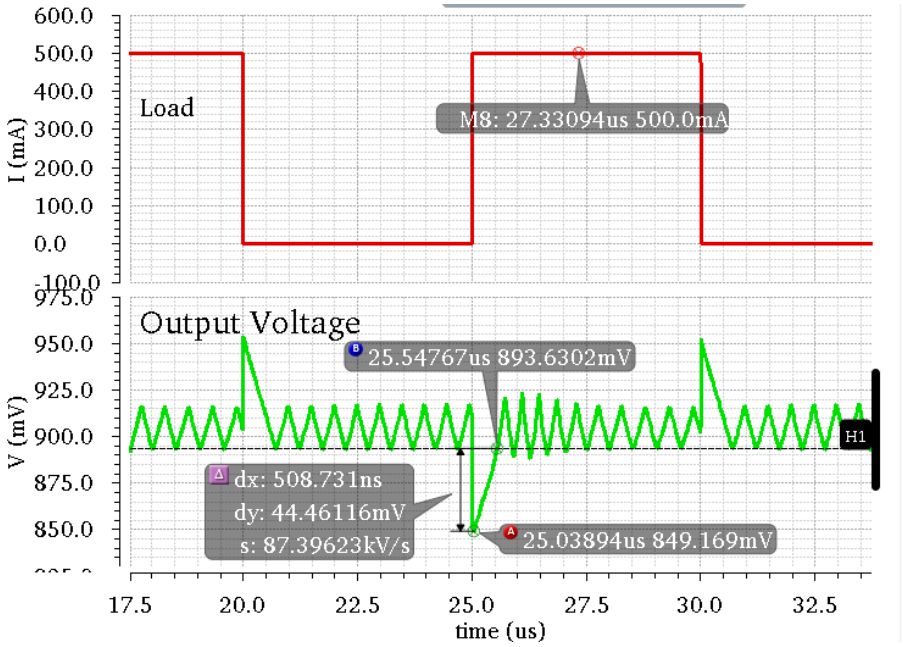

Figure 49: 500mA Load Step Response Showing Undershoot Excursion

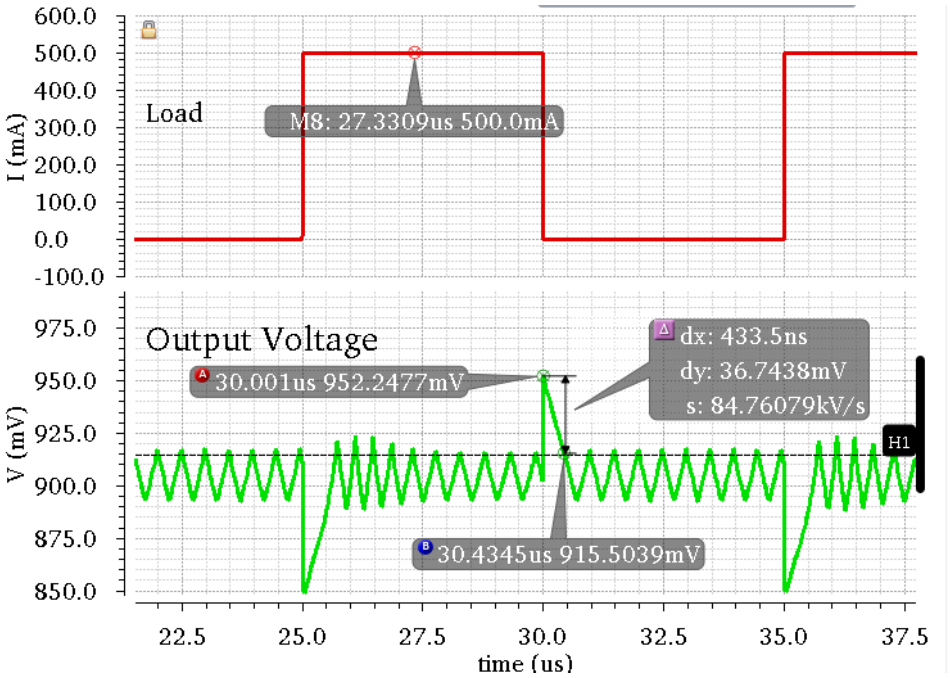

Figure 50: 500mA Load Step Response Showing Overshoot Excursion

3.4.3 Comparison of Results

As discussed in section 2 many state of the art designs have presented different frequency stabilization schemes for ripple based converters. Table 2 compares the performance and converter parameters of the presented ESR-controlled hysteretic buck with four other published works. Among the compared designs this work uses the smallest filtering inductance (1.0 µH) to improve the transient performance: small inductance have high current slew rate. Also the large output capacitance was optimized to reduce the voltage excursions on the output voltage.

The proposed work settles load transients in the switching cycle in which they occur. Hence this work achieves the least response time of <1.0 µs.

Table 2: Comparison Table

	[2] ISSCC 2009	[3] TVLSI 2012	[5] SOVC 2012	This Work
Frequency Synchronization	Delay Controlled	Hyst. window Controlled	Inductor ripple Controlled	ESR Controlled
Technology	0.35µmCMOS	0.35µmCMOS	0.13µmCMOS	0.18µmCMOS
Input Voltage	2.7 – 3.3 V	2.4 – 4.2 V	2.5 V	1.8 V
Output Voltage	0.9 – 2.1 V	1.8 V	0.7 – 1.8 V	0.7 – 1.0 V
Inductor	2.2 µH	4.7 µH	1.0 – 5.0 µH	1.0 µH
Output Capacitor	4.4 µF	4.7 µF	10 µF	20 µF
Switching Frequency (Deviation)	3 MHz (3.3%)	1 MHz (1.0%)	1 MHz (0.5%)	2 MHz (1.6%)
Max. Efficiency	93%	95%	93%	95.9%
Load Step	450 mA	200 mA	600 mA	500 mA
Response Time	2.4 /2.8 µs	5.0 / 5.0 µs	<10.0 µs	**0.53 / 0.45µs**
Undershoot/Overshoot	38mV / 45mV	40 / 40mV	61 / 72mV	50 / 40mV

4. CONCLUSION

A novel deign has been presented to stabilize the switching frequency of hysteretic dc-dc buck converter for frequent and high slew-rate transient loads. The new frequency control scheme uses a phase-locked loop (PLL) to adjust the equivalent series resistance (ESR) of the output capacitor and synchronizes the switching frequency of a ripple based regulator to a reference clock.

The design concept and principle of operation of the proposed work is presented in section 3.1. While section 3.2 discusses the transistor level implementation of the sub-blocks. Stability analysis of the closed loop system is discussed in section 3.3. Prior to this work other works have presented different frequency control schemes. Some of these previous designs have been presented with their merits and drawbacks in section 2.

The proposed work was designed in 0.18µm IBM CMOS process and achieves <1 µs response time to 500mA load transient within a tight voltage tolerance. The converter has dynamic voltage scaling (DVS) to allow microprocessors to regulate their power consumption.

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