MODELING OF PHOTONIC DEVICES AND PHOTONIC INTEGRATED CIRCUITS FOR OPTICAL INTERCONNECT AND RF PHOTONIC FRONT-END APPLICATIONS

A Dissertation

by

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ABSTRACT

Photonic integrated circuits (PICs) offer compelling solutions for applications in many areas due to the sufficient functionality and excellent performance. Optical interconnects and radio frequency (RF) photonics are two areas in which PICs have potential to be widely used. Optical interconnect system efficiency is dependent on the ability to optimize the transceiver circuitry for low-power and high-bandwidth operation, motivating co-simulation environments with compact optical device simulation models. Compact models for vertical-cavity surface-emitting lasers (VCSELs) and silicon carrier-injection/depletion ring modulators which include both non-linear electrical and optical dynamics are presented, and excellent matching between co-simulated and measured optical eye diagrams is achieved.

Advanced modulation schemes, such as four-level pulse-amplitude modulation (PAM4), are currently under consideration in both high-speed electrical and optical interconnect systems. How NRZ and PAM4 modulation impacts the energy efficiency of an optical link architecture based on silicon photonic microring resonator modulators and drop filters is analyzed. Two ring modulator device structures are proposed for PAM4 modulation, including a single-segment device driven with a multi-level PAM4 transmitter and a two-segment device driven by two simple NRZ (MSB/LSB) transmitters. Modeling results show that the PAM4 architectures achieve superior energy efficiency at higher data rates due to the relaxed circuit bandwidth.

While RF photonics offer the promise of chip-scale opto-electrical systems with high levels of functionality, in order to avoid long and unsuccessful design cycles, efficient models that allow for co-simulation are necessary. In order to address this, an optical element modeling framework is proposed based on Verilog-A which allows

for the co-simulation of optical elements with transistor-level circuits in a Cadence design environment. Three components in the RF photonic system, Mach Zehnder (MZ) modulators, 4^{th} order all pass filter (APF)-based optical filters, and jammer-suppression notch filters are presented to demonstrate the capability of efficient system design in co-simulation environments.

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1. INTRODUCTION

Photonic integrated circuit (PIC) [1, 2] is a technology that integrates photonic devices to achieve functionality for information signals. The PIC is associated with signal generation, processing, transmission and detection where the signal is carried by photons. There are a number of applications that are emerging for silicon photonic systems such as optical interconnects, microwave photonics, biosensing, LIDAR systems, nonlinear optics, and so on. Optical interconnects and microwave photonics are two areas that have potential to be widely used.

Dramatic requirements in high-speed interconnect capacity and transmission distance are demanded by mega data centers and supercomputers [3, 4]. Although transceiver circuits scaling has enabled the increased communication bandwidth in electrical link systems, electrical channel has not scaled to match CMOS technology speed [5]. Optical interconnects are well suited to address the demand due to low channel loss over a long distance and the potential for high bandwidth density with wavelength division multiplexing (WDM) [6]. The reduced link system complexity and power consumption also make optical interconnects popular and applicable.

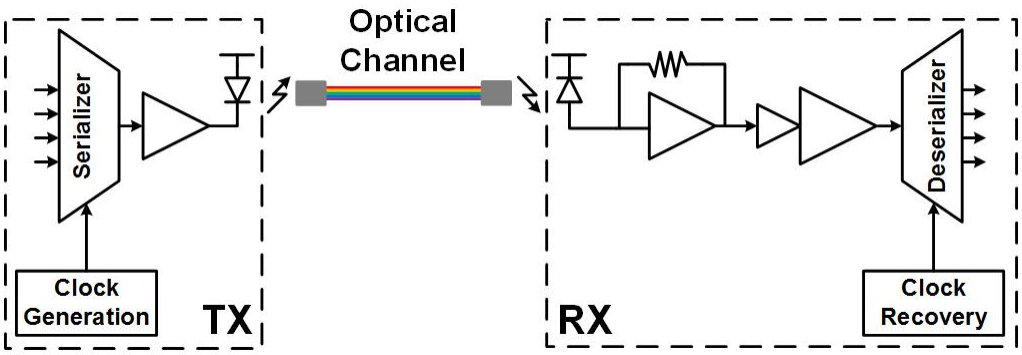


Figure 1.1: High speed optical link system.

A general high speed optical link system is shown in Fig. 1.1. The optical transmitter module converts signals from electrical domain to optical domain with lasers or modulators by drivers, which are transmitted through optical channels to the receiver side. Typically, the optical channels are photonic waveguides or optical fibers, which provide the capability for WDM to achieve high bandwidth density and energy efficiency. The optical receiver side converts signals back to electrical domain with photodetectors and amplifies signals with a transimpedance amplifier (TIA) and main amplifier gain.

Direct modulation of lasers and external modulation of continuous-wave (CW) laser with modulators are two common modulation techniques for optical transmitters [7]. VCSEL-based optical interconnects [8–12] are well suited for data center and supercomputing applications [13, 14] due to their simple direct modulation, excellent energy efficiency, high data rate, and low-cost packaging. However, this technique has limits for long haul communication since the laser chirp causes unwanted pulse dispersion. The other modulation technique with modulators is an approach for either short distance or long haul communication. Silicon photonic platforms [15, 16] are attractive due to their large-scale photonic device integration capabilities and potential manufacturing advantages, and silicon photonic microring resonator modulator based optical interconnects [17–20] have significant improvements in bandwidth density and energy efficiency due to the small footprint and the devices' high quality (Q) factor.

In order to optimize optical link system for low-power and high-bandwidth operation, the transceiver circuity must be carefully designed. This motivates co-simulation environments with compact optical device simulation models that accurately capture optical and electrical dynamics. Chapter 3-5 present modeling for VCSELs and two silicon modulators, carrier-injection and carrier-depletion ring mod-

ulators, in Verilog-A.

Advanced modulation schemes, such as PAM4, are currently under consideration in both high-speed electrical and optical interconnect systems. Chapter 6 analyzes how NRZ and PAM4 modulation impacts the energy efficiency of an optical link architecture based on silicon photonic microring resonator modulators and drop filters, and how this changes as CMOS technology scales from a 65nm to a 16nm node.

Microwave photonics [21, 22] enables to provide functions in microwave systems which are difficult to achieve in radio frequency (RF) domain. For RF signals processing, there are fundamental limitations to obtain the required level of frequency selectivity and tuning range and speed with conventional electrical filters. However, RF photonics filters can achieve high selectivity over a broad range of the spectrum with rapid dynamic tuning [23, 24].

A general RF photonic system [25] is shown in Fig. 1.2. The RF input signal is converted to optical domain with a CW laser and a modulator, and then the optical signal is processed with an optical filter. Finally, the optical output is converted back to RF domain with an optical receiver. In order to provide co-simulation environments for efficient design of RF photonic systems, modeling of PICs in Verilog-A is proposed in Chapter 7.

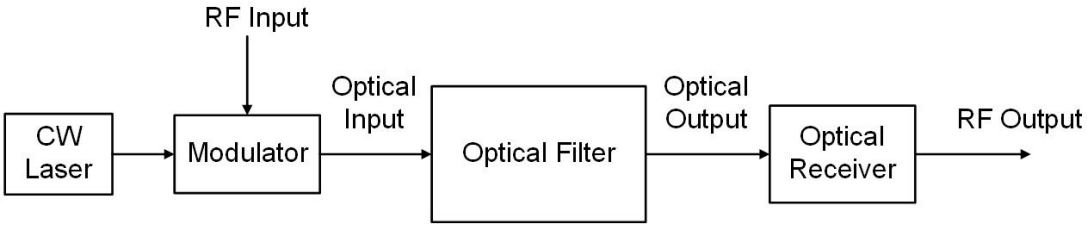


Figure 1.2: RF photonic system.

The dissertation is organized as below. Chapter 2 describes the background of integrated photonic devices, high speed optical interconnect systems, and silicon photonic RF front-end. A compact comprehensive VCSEL model that captures thermally-dependent electrical and optical dynamics and provides dc, small signal, and large-signal simulation capabilities is discussed in Chapter 3. Chapter 4 and 5 present a compact Verilog-A model for carrier-injection and carrier-depletion ring modulators including both non-linear electrical and optical dynamics, respectively. Chapter 6 analyzes a ring-resonator-based silicon photonic link model for comparisons of NRZ and PAM4 modulation. A Verilog-A model for silicon photonic RF front-end is proposed in Chapter 7, allowing for the co-simulation of PIC with transistor-level circuits in a Cadence design environment. Finally, Chapter 8 concludes the thesis.

2. BACKGROUND

This chapter briefly describes basic photonic devices, high speed optical link systems, and silicon photonic RF front-end. It begins with an overview of photonic devices including laser sources, optical modulators, optical channels, optical filters, and photodetectors. Then VCSEL-based and silicon photonic ring modulator based high speed optical link systems are discussed. The section ends with a brief introduction of silicon photonic RF front-end.

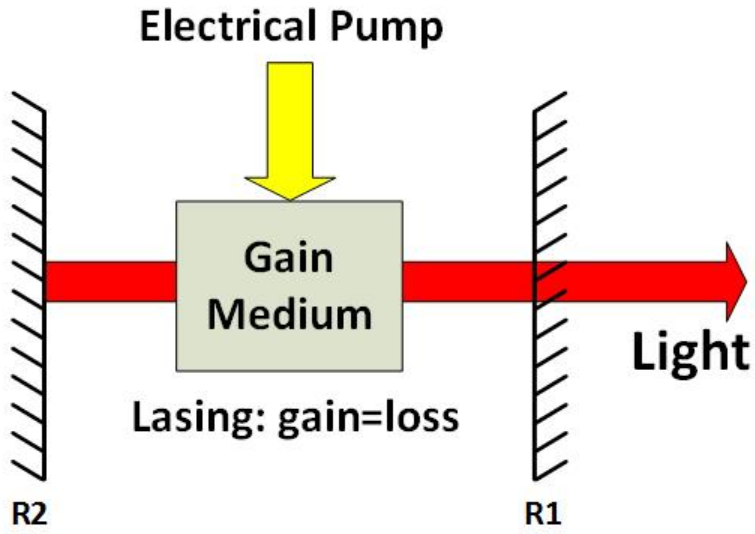


Figure 2.1: General laser cavity structure.

2.1 Integrated Photonic Devices

2.1.1 Light Sources

Light sources are where optical signals from in high speed optical link systems based on either direct modulation of lasers or external modulation of CW laser with

modulators. A general laser cavity structure is shown in Fig. 2.1. Two mirrors form a laser cavity. There is a gain medium inside the cavity, and an electrical pump inputs energy into the gain medium to overcome cavity losses. The lasing happens when the gain is equal to the losses.

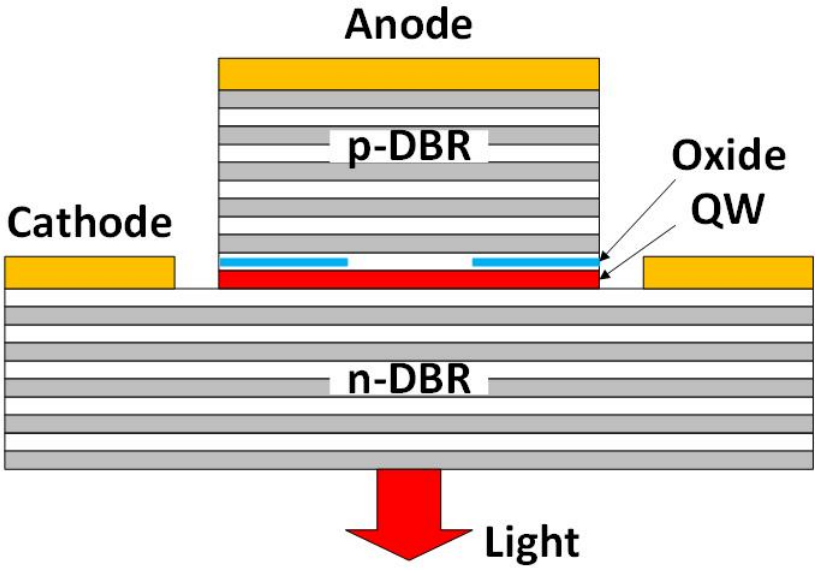


Figure 2.2: A schematic of a typical VCSEL.

2.1.1.1 Vertical-Cavity Surface-Emitting Lasers

A schematic of a typical VCSEL [26] is shown in Fig. 2.2. Both mirrors are distributed Bragg reflectors (DBRs). One is at the top and the other is at the bottom. InP and GaAs containing compounds are common VCSEL mirror materials. A DBR is a stack of $\lambda/4$ layers with alternating high and low refractive index. The anode and cathode are utilized for electrical pump. The active region consists of oxide layers and strained quantum wells (QWs), where the oxide layers constrain the output light aperture and the QWs provide the gain. The lasing light emits

vertically. Two common lasing wavelengths are 850nm and 980nm based on different QW materials. Most VCSELs are multi-mode due to the relative long cavity length comparing to Distribute Feedback Lasers (DFBs). Longer wavelength (1310nm and 1550nm) and single-mode VCSELs are being developed for Mega data centers and long-haul communication.

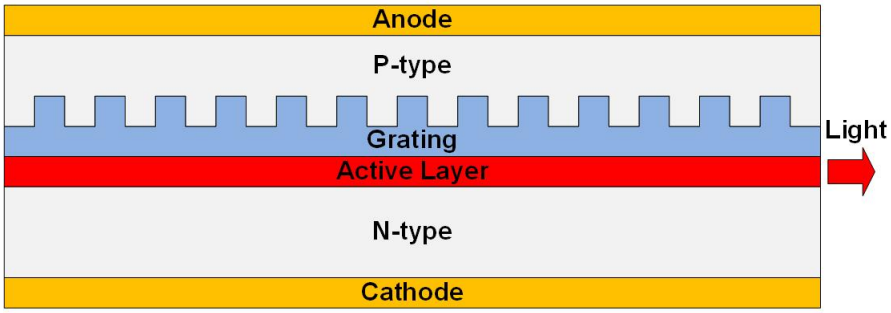


Figure 2.3: A schematic of a typical DFB.

2.1.1.2 Distribute Feedback Lasers

A schematic of a DFB [27] is shown in Fig. 2.3. DFBs also use grating mirrors, but the gain is included in the gratings. The active region length is typically a portion of a wavelength, and therefore single-frequency operation is easily achieved, which is attractive for using in photonic integrated circuits and systems.

2.1.2 Optical Modulators

Although direct modulation is simple and cheap, external modulation has more advantages of low chirping effect and high extinction ratio (ER). There are three common types of optical modulators based on different effects: the electro-optic effect, the electro-absorption effect, and the plasma dispersion effect. Due to weak electro-optic and electro-absorption effects in silicon, optical modulators in silicon photonic

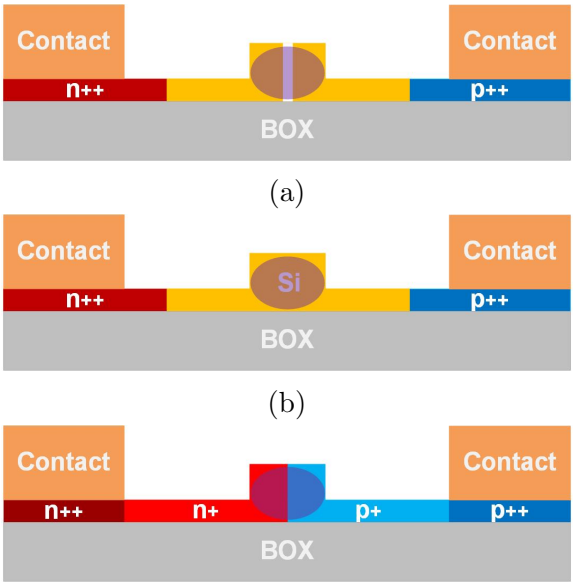


Figure 2.4: Cross section views of three silicon photonic modulators, (a) carrier accumulation, (b) carrier injection, and (c) carrier depletion.

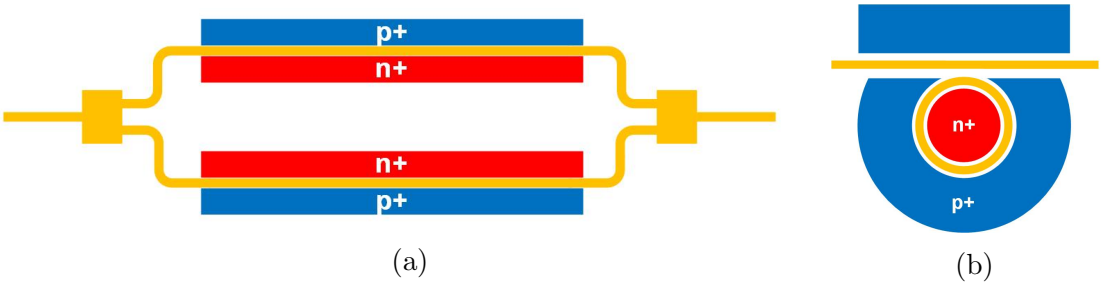
platform are mainly based on plasma dispersion effect: the change in refractive index and optical absorption coefficient induced by free carriers in a semiconductor.

Three common types of silicon photonic modulators [28], carrier-accumulation, carrier-injection, and carrier-depletion modulators, are shown in Fig. 2.4. Carrier-accumulation modulators (Fig. 2.4(a)) have a silicon oxide thin layer as an isolator in waveguides to form a capacitor. In carrier-injection modulators (Fig. 2.4(b)), n-type and p-type doped regions are separated by intrinsic silicon which form a p-i-n diode. For carrier-depletion modulators (Fig. 2.4(c)), n-type and p-type doped regions are abut in the waveguide which form a p-n diode. Carrier-accumulation modulators can achieve tens Gb/s modulation speed, but the relative complex and uncontrollable fabrication process make them less applicable. Carrier-injection and carrier-depletion modulators are more often being used. Table 2.1 compares these two modulators

in four figures of merit. Carrier-injection modulators are more advantageous than carrier-depletion modulators except the modulation bandwidth.

Table 2.1: Comparison of carrier-injection and carrier-depletion modulators.

Figure of merit	**Carrier-injection**	**Carrier-depletion**
Modulation bandwith	Low	High
Extinction ratio (ER)	Large	Small
Modulation efficiency	High	Low
Insertion loss	Low	High



(a) (b)

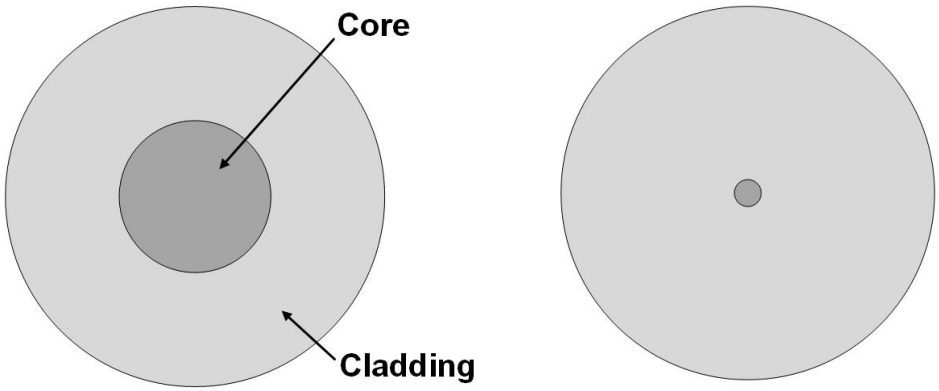
Figure 2.5: Top views of (a) MZ modulators and (b) ring modulators

Mach Zehnder modulators (MZMs) (Fig. 2.5(a)) and ring modulators (Fig. 2.5(b)) are two modulators based on different modulation schemes. MZMs are based on MZ interferometers (MZIs). A coupler divides the laser light equally into two arms, one of which is a phase modulator. The beams are then recombined with another coupler. Ring modulators consist of coupling between ring resonators with electro-optical modulation and straight waveguides. The comparisons in four figures of merit between these two modulators are listed in Table 2.2. Typically, MZMs have a length of few millimeters due to the large figure of merit V_{π}·L, and the diameter

of ring modualtors are tens of micrometers. Therefore, the insertion loss of MZMs is much larger than ring modulators due to the waveguide propagation loss. Ring modulators are high Q devices, which have trade-offs between the extinction ratio (ER) and the wavelength sensitivity.

Table 2.2: Comparison of MZ and ring modulators.

Figure of merit	**MZ modulator**	**Ring modulator**
Footprint	Large	Small
Extinction ratio (ER)	Small	Large
Insertion loss	High	Low
Wavelength sensitivity	Low	High



(a) (b)

Figure 2.6: Cross section views of (a) multi-mode and (b) single-mode fibers

2.1.3 Optical Channels

Optical fibers and waveguides are commonly used optical channels for optical link systems. Both of them can have multi-mode and single-mode. Optical fibers [29] can

Figure 2.7: Cross section views of (a) multi-mode rib waveguides, (b) multi-mode strip waveguides, (c) single-mode rib waveguides and (d) single-mode strip waveguides.

be made of many materials, and the most common one in communication systems is silica. As shown in Fig. 2.6, an optical fiber consists of a core with higher refractive index and a cladding with lower refractive index to achieve total internal reflection. Either multi-mode or single-mode fiber has the same cladding diameter $\sim$125μm but different core diameters. The core diameter of multi-mode fibers is 50μm or 62.5μm, which is much larger than the core diameter of single-mode fibers $\sim$9μm.

Waveguides [30] can be made on different PIC platforms, such as Si, Si_3N_4, and InP. They also consist of cores with higher refractive index and claddings with lower refractive index. Silicon photonic waveguides allow for compact PICs due to the

high index contrast between Si (∼3.5) and SiO_2 (∼1.5). Typically, there are two types of waveguides, rib (ridge) waveguides and strip (channel) waveguides. Fig. 2.7 shows typical dimensions of rib and strip waveguides for multi-mode and single-mode transmissions at 1550nm in silicon photonics.

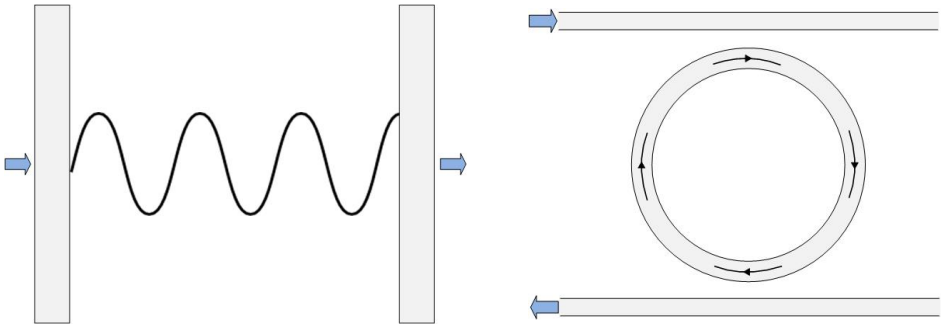


Figure 2.8: Schematics of (a) FP filters and (b) ring resonator filters

2.1.4 Optical Filters

Optical filters are essential components in WDM based optical link systems. Two common optical filters for high speed optical interconnects, Fabry-Perot (FP) filters [31] and ring resonator filters [32], are shown in Fig. 2.8. FP filters (Fig. 2.8(a)) consist of two parallel mirrors with a fixed spacing apart. Ring resonator filters (Fig. 2.8(b)) consist of two straight waveguides sandwiched with a ring waveguide. As shown in Fig. 2.9, the transmission of an optical filter is a function of wavelength. Both optical filters can be described by certain figures of merit, such as free spectral range (FSR), full width at half maximum (FWHM), finesse (F), and quality factor (Q). The FSR is defined as the distance between resonance peaks , the FWHM is defined as the resonance width equal to half of its maximum value or 3dB bandwidth,

the F is defined as the ratio of the FSR and the FWHM, and the Q is defined as the ratio of the operation wavelength and the FWHM [32].

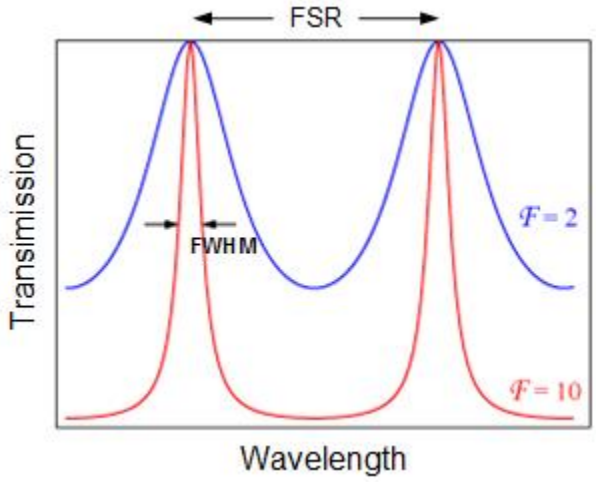
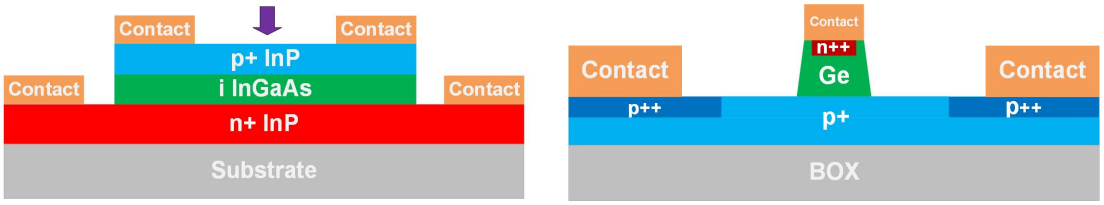


Figure 2.9: Transmission of an optical filter as a function of wavelength.

2.1.5 Photodetectors

A photodetector [33] is an optoelectronic device that absorbs optical energy and generates a photocurrent. There are many types of photodetectors, in which photodiodes (PDs) are the most common ones. Typically, three often used photodiodes are p-n photodiodes, p-i-n photodiodes, and avalauche photodiodes (APDs), where p-i-n photodiodes are commonly used for high speed optical interconnects due to the high bandwidth (BW) and sensitivity. p-i-n photodiodes need a reverse bias for operation. Several figures of merit can be utilized to describe a photodiode, such as operating wavelength range, responsivity (R), BW, dark current and noise. The responsivity is the ratio of the photocurrent and the input optical power. There are two types of p-i-n photodiodes based on different platforms, III-V compound p-i-n

photodiodes and silicon p-i-n photodiodes (Fig. 2.10). A cross section view of a III-V p-i-n photodiode is shown in Fig. 2.10(a), where the light goes into the photodiode vertically. InGaAs/InP is the often used material for 1.31μm and 1.55μm wavelength operation. Waveguide photodiodes are often used in silicon photonic platform due to the much easier integration. As shown in Fig. 2.10(b), the intrinsic region of silicon p-i-n photodiodes is doped with germanium for optical energy absorption and photocurrent generation.



(a) (b)

Figure 2.10: Cross-section views of (a) a silicon p-i-n waveguide photodiode and (b) a InGaAs/InP III-V p-i-n photodiode

2.2 High Speed Optical Interconnects

High speed optical link systems [34] consist of optical transmitters, optical channels, and optical receivers. Optical channels are typically either waveguide (fiber)-based or free-space. Two high speed optical link architectures will be introduced. One is VCSEL based optical interconnects and the other one is silicon ring modulator based optical interconnects.

2.2.1 VCSEL Based Optical Interconnects

Fig. 2.11 shows a VCSEL based optical link architecture. VCSEL array driven with TX IC work as transmitters. The receiver module consists of PD array and

RX IC. Both VCSEL array and PD array are vertically coupled out and in with fiber array. Each fiber has multi-channel data due to the WDM, where FP filters are commonly used for wavelength multiplexer and demultiplexer. multi-mode VCSELs are most often used in optical link systems for data centers due to the easy fabrication and low-cost packaging. However, single-mode VCSELs will be widely used due to the growing link distance demand.

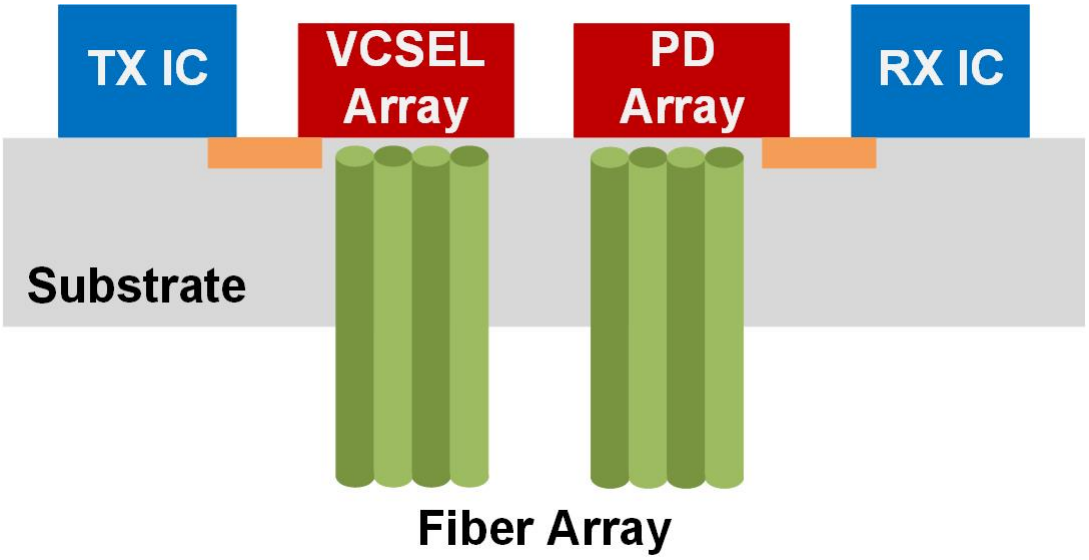


Figure 2.11: VCSEL based optical interconnects.

2.2.2 Silicon Ring Modulator Based Optical Interconnects

A ring based wavelength division multiplexing optical interconnect architecture is shown in Fig. 2.12. Multi-channel data can be transmitted in single waveguide due to ring resonators' inherent wavelength multiplexing feature. A multi-wavelength laser (comb laser or DFBs) is coupled to the silicon photonic chip. In the transmitter module, microring modulators driven by CMOS drivers convert signals from electrical

domain to optical domain. Optical filers are utilized for data center, metro or long-haul communication. On the receiver side, each channel data is filtered out by a ring resonator and goes into a photodetector to convert signals back to electrical domain then to CMOS receivers. The link architecture has significant improvements in bandwidth density and energy efficiency due to the small footprint and devices' high-Q factor.

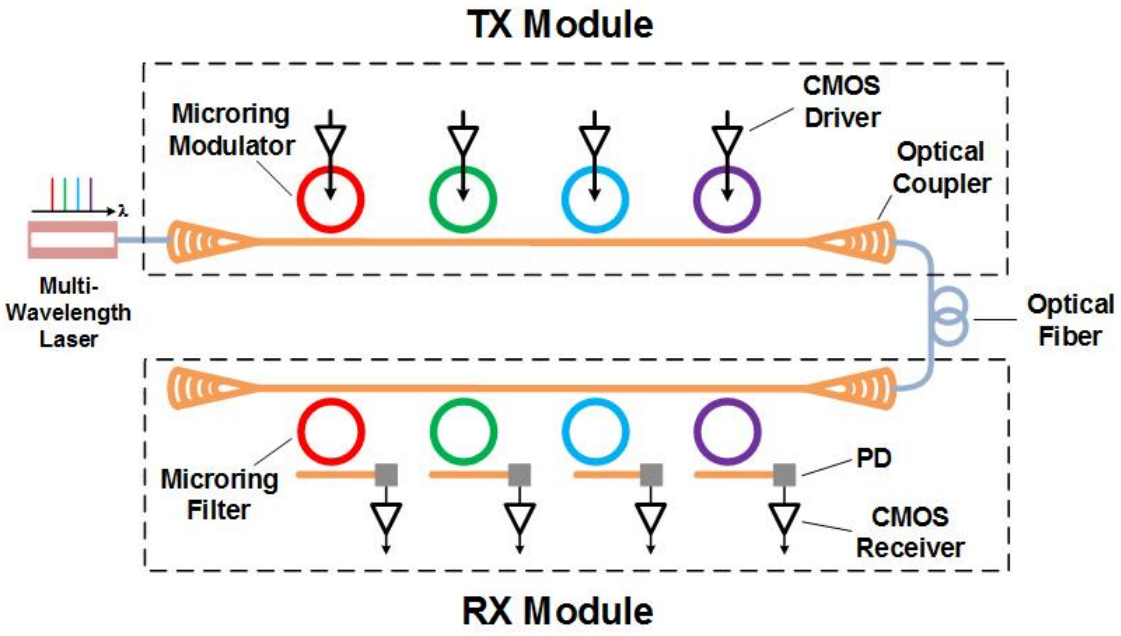


Figure 2.12: Silicon ring resonator based optical interconnects.

2.3 Silicon Photonic RF Front-End

Fig. 2.13 shows a chip-scale wideband frequency-agile silicon photonic mm-wave receiver for spread spectrum communication that utilizes high-performance band-pass photonic filtering along with automatic jammer suppression via reconfigurable optical notch filters. It consists of two main parts. (1) The 65nm CMOS chip

includes the antenna interface, MZM pre-distortion linearization stage, optical RF front-end (TIA), as well as the electrical circuitry for tuning the filter responses. (2) The 130nm SOI silicon photonic chip includes MZMs for E-O conversion, a 5GHz reconfigurable channel-select 4th order bandpass filter (BPF), ring resonator filters for jammer suppression and spectrum sensing, and waveguide photodetectors for O-E down-conversion and filter monitoring.

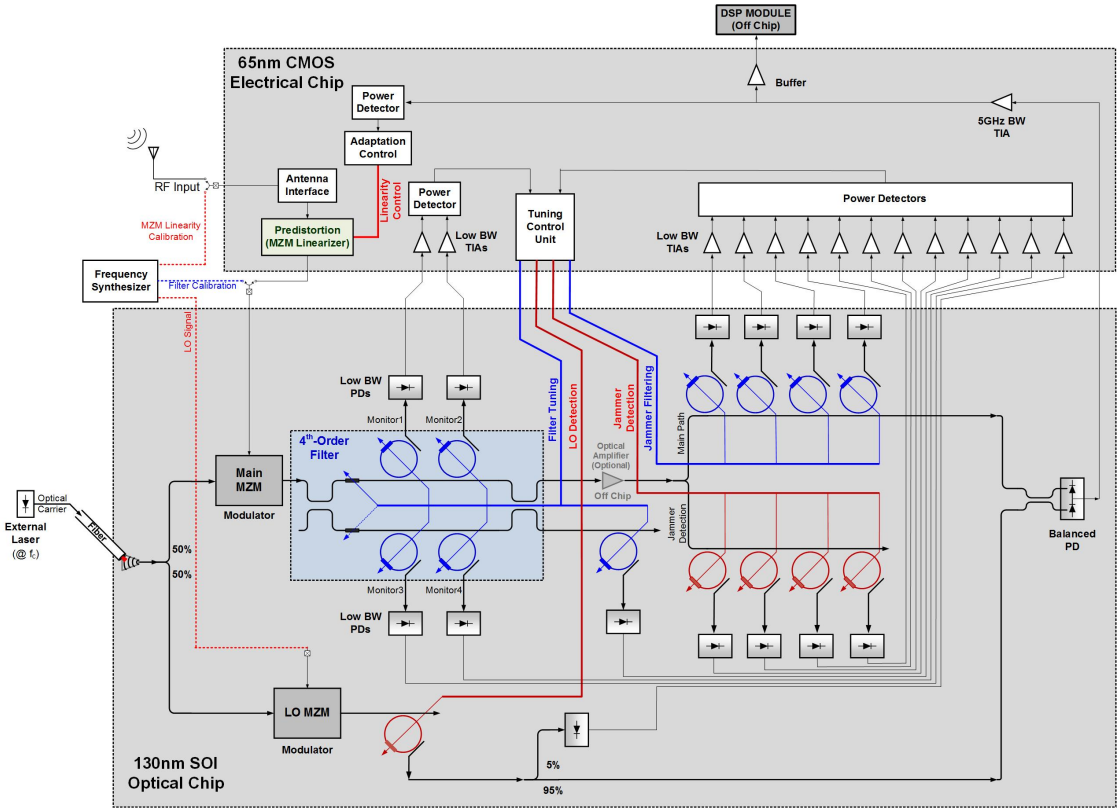


Figure 2.13: Hybrid-integrated silicon photonic RF front-end.

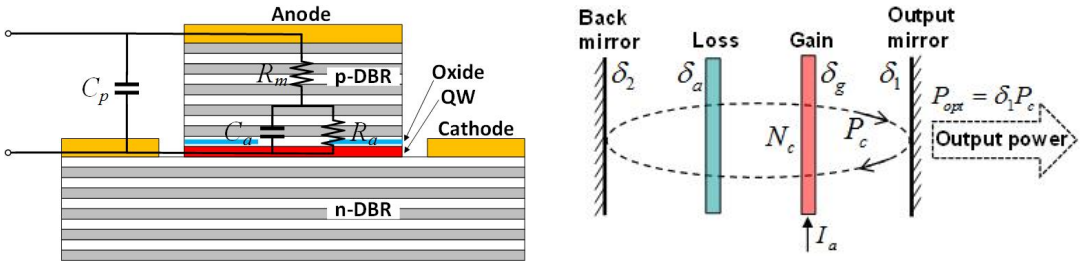
3. VERTICAL-CAVITY SURFACE-EMITTING LASER MODEL

In order to support the bandwidth demands of future data centers and supercomputers, it is essential to improve the data rate, energy efficiency, and cost of the optical interconnects employed in these systems [35, 36]. Vertical-cavity surface-emitting laser (VCSEL)-based optical interconnects [8–12] are well suited for these applications [13,14] due to their simple direct modulation, excellent energy efficiency, high data rate, and low-cost packaging. Potential solutions to address the growing link distances in these systems include the use of advanced modulation schemes, such as four-level pulse-amplitude modulation (PAM4) [37,38] and discrete multitone [39], and/or single-mode VCSELs [40–43].

VCSEL bandwidth, which is bias and temperature dependent, is limited by a combination of electrical parasitics and the electron-photon interaction described by a set of second-order rate equations [26]. This results in optical interconnect systems often incorporating equalization circuitry, which may be non-linear, embedded in either the transmitter drivers or optical front-ends to extend the data rate [8–12]. A VCSELs large-signal temperature-dependent static optical power-current-voltage (L-I-V) response is also important, particularly for advanced modulation schemes where linearity is a concern, such as PAM4. Due to these non-linear dynamics and thermal dependencies of VCSELs, transmitter circuity must be carefully designed to supply the required signals at high data rates with relatively low-power consumption. This motivates co-simulation environments with a compact comprehensive VCSEL model that captures thermally-dependent electrical and optical dynamics and provides dc, small signal, and large-signal simulation capabilities.

While numerous VCSEL models have been developed, some of the previous

models have not included thermal effects [44–48]. Other work which has included temperature effects have neglected either bias and temperature-dependent electrical parasitics [49–53] or the rate-equation-based electrical-to-optical conversion dynamics [54]. This chapter presents a compact Verilog-A VCSEL model which comprehensively captures the large- and small-signal dynamic response combined with the dc thermal effects on both the electrical and optical behavior. The model is described in Section 1 and consists of an accurate large- and small-signal electrical input stage coupled to a rate-equation-based optical output stage formulated for efficient Verilog-A implementation. To provide a more intuitive model for the case of a VCSEL cavity the general laser rate equations have been reformulated. Section 2 presents 25Gb/s experimental verification of the VCSEL model, which was performed both at 23°C and 80°C for varying bias current levels. Finally, Section 3 concludes the chapter.



(a) (b)

Figure 3.1: (a) VCSEL cross section view with the equivalent electrical small-signal model overlaid, (b) General laser cavity structure.

3.1 Model Description and Parameter Extraction

Fig. 3.1 shows both a typical VCSEL cross section view with the equivalent electrical small-signal model placed where the circuit elements physically originate and a general laser cavity structure. This electrical model consists of a parasitic

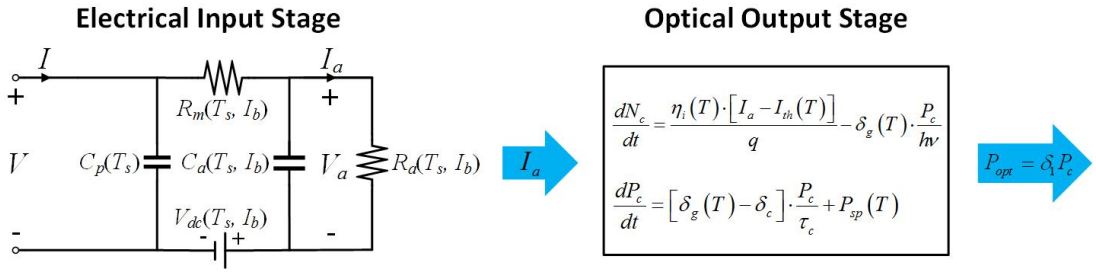


Figure 3.2: Comprehensive VCSEL model which includes bias and thermal dependent dc, small-signal, and large-signal dynamics.

capacitor C_p between the laser diodes anode and cathode terminals, a resistor Rm that models the p- and n-type distributed Bragg reflectors (DBRs), and the active region resistance R_a and capacitance C_a. While this model is suitable for small-signal behavior, an accurate comprehensive model requires inclusion of both bias- and thermal-dependent large-signal and optical dynamics formed by the interaction of the active region carriers N_c and the cavity power P_c and key gain and loss parameters. Fig. 3.2 shows the proposed VCSEL model which consists of an electrical input stage and a rate-equation-based optical output stage. When a driving current is applied to the electrical input stage, large-signal behavior is captured with the inclusion of the bias-dependent voltage source V_{dc}. Linking the electrical and optical stages is the active region current through R_a, which serves as the key input to the carrier rate equation. The optical stages two coupled differential equations describe the dynamic carrier and photon interaction to capture the nonlinear transient behavior of the optical output power P_{opt}. Both the electrical and optical stages have thermally-dependent elements to model how the VCSELs performance varies with temperature. All circuit elements in the electrical stage are functions of both substrate temperature T_s and bias current I_b, except for C_p which is modeled as being only temperature dependent due to its negligible change with bias current. While in

the optical stage, the injection efficiency η_i, threshold current I_{th}, round trip cavity gain δ_g, and spontaneous emission power P_{sp} are modeled as temperature dependent.

The model parameters are extracted from curve fitting measurements of VCSEL dc, small-signal, and large-signal dynamic behavior, with polynomial-based curve fitting employed to allow for an efficient realization in the Verilog-A model. Both the large-signal voltage-current (V-I) characteristic and the small-signal S_{11} data are utilized to extract the electrical model parameters. While the optical model parameters are extracted from the VCSELs physical design, large-signal optical power-current (L-I) characteristic, small-signal S_{21} data, and high-speed pulse response measurements.

3.1.1 DC Characteristics

Since VCSELs are operated above the threshold current in high data rate optical interconnect systems, the temperature-dependent optical power-current-voltage (L-I-V) characteristics are modeled as

$$V(T) = V_{on} + R_d(T) \cdot I = V_{dc}(T_s, I_b) + [R_m(T_s, I_b) + R_a(T_s, I_b)] \cdot I \tag{3.1}$$

$$P_{opt}(T) = \eta(T) \cdot [I - I_{th}(T)], \tag{3.2}$$

where V_{on} is the turn-on lasing voltage, R_d is the differential resistance, and η is the slope efficiency. These characteristics are functions of the active region temperature T, which is

$$T = T_s + (V I - P_{opt}) \cdot R_{th}, \tag{3.3}$$

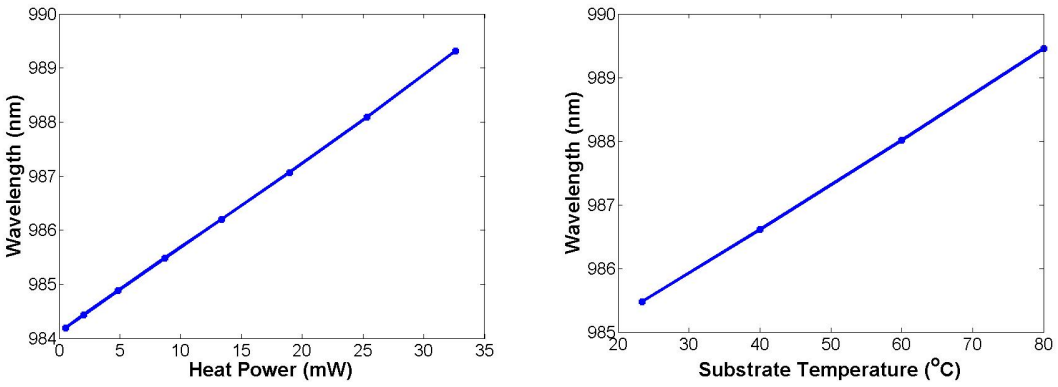
where R_{th} is the thermal resistance. This can be measured indirectly through the lasing wavelength [55] by

$$R_{th} = \frac{\Delta T}{\Delta P_h} = \frac{(\Delta\lambda/\Delta P_h)}{(\Delta\lambda/\Delta T)}, \tag{3.4}$$

where the heat power is

$$P_h = VI - P_{opt}, \tag{3.5}$$

and $\Delta\lambda/\Delta P_h$ and $\Delta\lambda/\Delta T$ are the wavelength change with heat power and substrate temperature, respectively. Utilizing an optical spectrum analyzer (OSA) to measure a 990nm 25Gb/s-class VCSELs fundamental mode wavelength change with heat power and substrate temperature yields values of $\Delta\lambda/\Delta P_h$=0.159nm/mW (Fig. 3.3(a)) and $\Delta\lambda/\Delta T$=0.070nm/°C (Fig. 3.3(b)), and therefore R_{th}=2.27°C/mW.



(a) (b)

Figure 3.3: Measured wavelength shift with (a) heat power and (b) substrate temperature.

In order to obtain the remaining parameters for the dc characteristics, η is first

decomposed into parameters used in the rate-equation-based optical output stage

$$\eta(T) = \eta_i(T) \frac{\delta_1}{\delta_1 + \delta_a} \frac{h v_0}{q}, \tag{3.6}$$

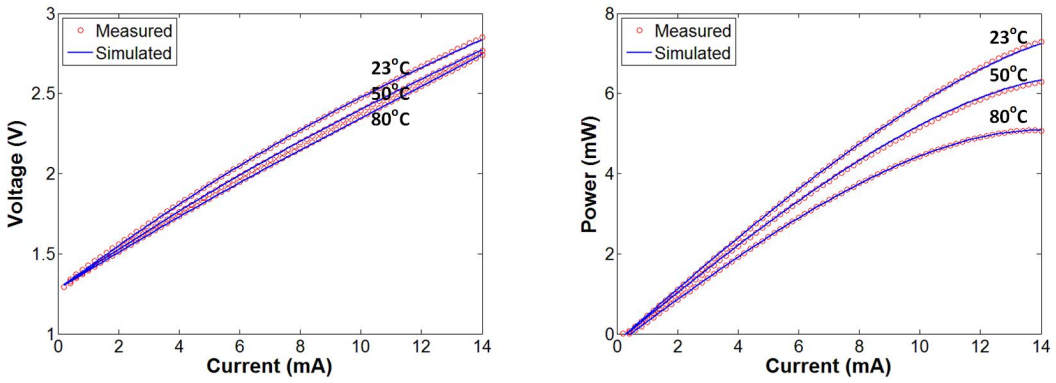
where η_i is the injection efficiency, $\delta_1 = 1 - R_1$ is the output mirror (DBR) transmissivity, R_1 is the reflectivity, δ_a is the round trip internal absorpsion loss, h_0 is the photon energy, and q is the electron charge. By curve fitting the Fig. 3.4 measured L-I-V characteristics, the three parameters R_d, δ_a, and I_{th} are then extracted as a polynomial function of temperature.

$$f(T) = b_0 + b_1 \cdot (T - T_0) + b_2 \cdot (T - T_0)^2 \tag{3.7}$$

Table 3.1 gives the $b_0 - b_2$ are coefficients, with $\delta_1 = 3.8 \times 10^{-3}$, $\delta_a = 2.7 \times 10^{-3}$, and $V_{on} = 1.28V$ assumed fixed and a room temperature $T_0 = 23^oC$ is utilized. Excellent matching is achieved with the measured Fig. 3.4 characteristics, with the differential resistance and slope efficiency decreasing with substrate temperature and the VCSELs thermal rollover point appearing near a bias of 14mA at 80°C.

Table 3.1: Polynomial coefficients of R_d, η_i, and I_{th}.

Parameter	Unit	b_0	b_1	b_2
R_d	Ω	137.0	-0.4836	0.0018
η_i	-	0.90	1.80×10^{-3}	-8.54×10^{-6}
I_{th}	mA	0.30	1.79×10^{-5}	4.20×10^{-5}



(a) (b)

Figure 3.4: Measured and simulated (a) V-I and (b) L-I characteristics.

3.1.2 Small-Signal Characteristics

The remaining parameters in the electrical model and the small-signal response of the optical model are extracted by curve fitting the Fig. 3.5 small-signal electrical input impedance and VCSEL magnitude transfer function measurements. As these responses are functions of the large-signal operating point, responses for three different bias points corresponding to the nominal 6mA swing centered at a 6mA bias level are utilized.

In order to accurately describe the VCSELs electrical parasitic elements dependency on bias and temperature, R_m, R_a, and C_a are modeled as a third-order function of bias current with first-order coefficients which change with substrate temperature.

$$\begin{aligned} Z\left(T_s, I_b\right) = &\left[c_0 + c_1 \cdot \left(T_s - T_0\right)\right] + \left[c_2 + c_3 \cdot \left(T_s - T_0\right)\right] \cdot \left(I_b - I_0\right) \\ &+ \left[c_4 + c_5 \cdot \left(T_s - T_0\right)\right] \cdot \left(I_b - I_0\right)^2 + \left[c_6 + c_7 \cdot \left(T_s - T_0\right)\right] \cdot \left(I_b - I_0\right)^3 \end{aligned} \tag{3.8}$$

As C_p is a weak function of the bias current, it is modeled as having only a first-order dependency on substrate temperature. Table 3.2 gives the c_0-c_7 coefficients for

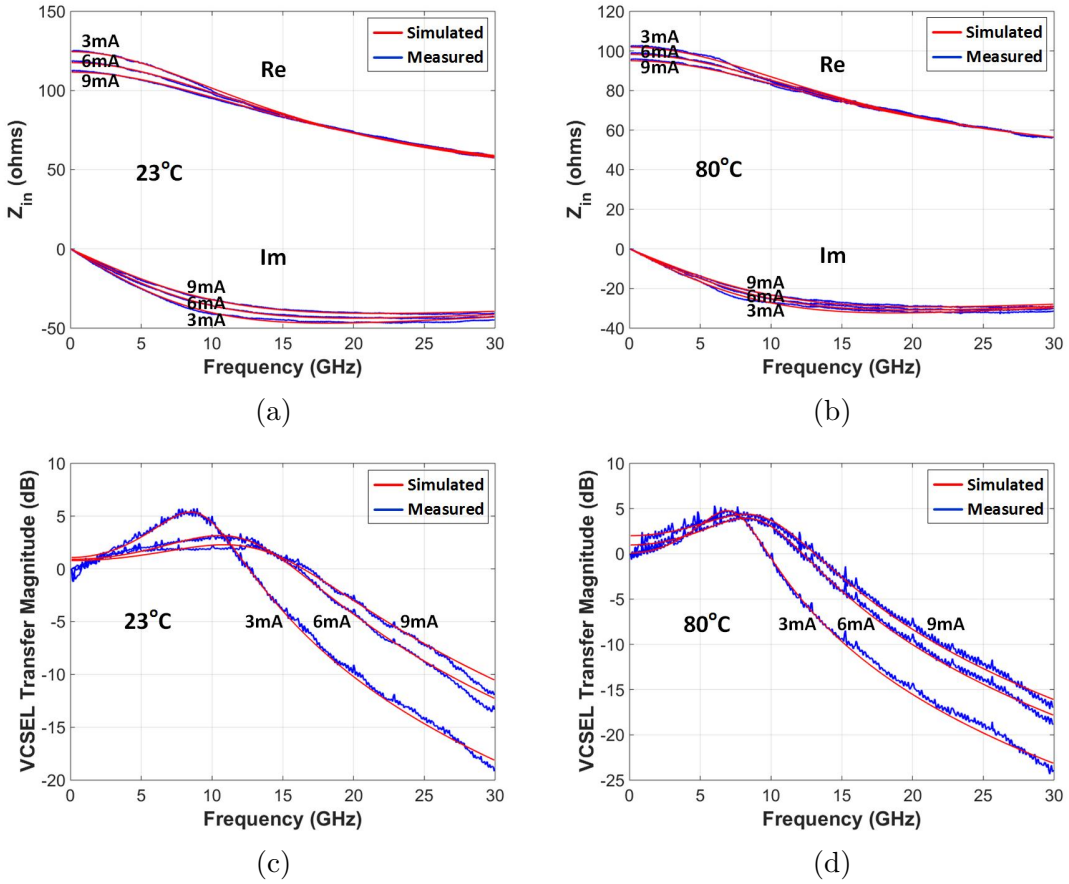


Figure 3.5: Measured and simulated electrical input impedance at (a) 23°C (room temperature) and (b) 80°C substrate temperatures, and normalized optical magnitude transfer response at (c) 23°C and (d) 80°C substrate temperatures.

T_0 = 23°C and I_0 = 6mA. The electrical model is completed by utilizing the R_m and R_a values at a given temperature and bias to compute the dc voltage source V_{dc} from Equation 3.1, providing flexibility to match both the large signal and small-signal characteristics. Excellent matching is achieved for both the real and imaginary components of the measured Fig. 3.5 electrical input impedance data, with the modeled response achieving the expected low-pass characteristic at both 23°C and 80°C.

A two-pole transfer function, derived from the VCSEL rate equations, models the

Table 3.2: Polynomial coefficients of R_m, R_a, C_a and C_p.

Parameter	Unit	c_0	c_1	c_2	c_3	c_4	c_5	c_6	c_7
R_m	Ω	49.41	-0.048	-88.663	-0.106	-8.127 $\times 10^4$	-634.2	-6.947 $\times 10^6$	4.392 $\times 10^4$
R_a	Ω	67.94	-0.290	-2.319 $\times 10^3$	22.030	2.830 $\times 10^4$	-324.0	8.817 $\times 10^4$	4.714 $\times 10^3$
C_a	fF	114.1	0.735	1.84 $\times 10^3$	-17.47	3.70 $\times 10^5$	-521.6	-1.981 $\times 10^7$	2.228 $\times 10^5$
C_p	fF	20	-0.175	0	0	0	0	0	0

optical small-signal response

$$H(f,T) = \frac{1}{1-\left[\frac{f}{f_r(T)}\right]^2 + j\cdot\left\{\frac{f}{[f_r(T)]^2/f_d(T)}\right\}} \tag{3.9}$$

where f_r is the resonance frequency and f_d is the damping frequency.

$$f_r(T) = D(T)\cdot\sqrt{(I - I_{th}(T))} \tag{3.10}$$

$$2\pi f_d(T) = \gamma(T) = K(T)\cdot f_r^2 + \gamma_0 \tag{3.11}$$

Expressing the small-signal transfer function in this manner allows easy identification of the quality factor $Q_e = f_r/f_d$, which is useful in the analysis of relative intensity noise (RIN) and modulation overshoot. In the f_r and f_d equations, the D-factor quantifies the resonance frequency increase with current, the K-factor defines the VCSELs intrinsic modulation bandwidth capabilities, γ is the damping factor and γ_0 is the damping factor offset [17]. These D- and K- factors are modeled as second-order functions of temperature (Equation 3.7). Table 3.3 gives the b_0-b_2 coefficients with T_0=23°C and γ_0 fixed at 3.76ns^{-1}. As shown in Fig. 3.5, the modeled VCSEL

Table 3.3: Polynomial coefficients of D and K.

Parameter	Unit	b_0	b_1	b_2
D	$GHz/mA^{0.5}$	6.02	-2.58×10^{-2}	-1.60×10^{-5}
K	ns	0.40	-9.95×10^{-5}	1.37×10^{-5}

small-signal transfer characteristics match well with the measured results, with an increased bias level resulting in both higher bandwidth and damping and an increased temperature yielding a reduction in bandwidth.

3.1.3 Large-Signal Dynamics

Finally, curve fitting of large-signal optical pulse responses is utilized to extract the remaining parameters for the rate equations which describe the VCSEL large-signal electro-optical dynamics.

$$\frac{dN_c}{dt} = \frac{\eta_i\left(T\right)\cdot\left[I_a - I_{th}\left(T\right)\right]}{q} - \delta_g\left(T\right)\cdot\frac{P_c}{h\nu} \tag{3.12}$$

$$\frac{dP_c}{dt} = \left[\delta_g\left(T\right) - \delta_c\right]\cdot\frac{P_c}{\tau_c} + P_{sp}\left(T\right), \tag{3.13}$$

where N_c is the total carriers in the active region and P_c is the one-way recirculating power in the cavity. Equation 3.12 and 3.13 are a reformulation of the more typical and detailed rate equations [48].

The round trip cavity gain δ_g, spontaneous emission power P_{sp}, and round trip cavity time τ_c are

$$\delta_g\left(T\right) = \frac{4g_0\left(T\right)\cdot L_a}{\left[1+\frac{4P_c}{P_{sat}(T)}\right]}\cdot\ln\left(\frac{N}{N_{tr}}\right) \tag{3.14}$$

$$P_{sp}\left(T\right) = \frac{h\nu}{\tau_c}\cdot\beta\cdot V_a\cdot B\left(T\right)\cdot N^2 \tag{3.15}$$

$$\tau_c = m_c/v_0\ , \tag{3.16}$$

where g_0 is the gain coefficient, L_a is the length of the active region, P_{sat} is the saturation power, $N = N_c/V_a$ is the carrier density, V_a is the active region volume, N_{tr} is the transparency carrier density, β is the spontaneous capture efficiency, B is the radiative recombination coefficient, m_c is the round trip cavity delay normalized by the optical period $\tau_0 = 1/v_0$, and v_0 is the resonant cavity photon frequency. Note that the factor of four in Equation 3.14 consists of a factor of two from the power traveling in both the forward and reverse directions and another factor of two is from the standing wave at the quantum wells.

All of these expressions contain parameters fixed by the VCSELs physical design, including

$$m_c = \frac{2n_g L_c}{\lambda_0} = \frac{2n\Delta L_c}{\Delta\lambda} \tag{3.17}$$

and

$$V_a = \frac{1}{4}\pi L_a d_{ox}^2, \tag{3.18}$$

where n_g is the average group index, n is the average refractive index, L_c is the cavity length, and d_{ox} is the oxide diameter. Parameters δ_1, n_g, υ_o, d_{ox}, and L_a come directly from the VCSEL design, while m_c is estimated by DBR design simulations that extract the the output wavelength shift with the cavity length change.

The round trip cavity loss δ_c and threshold current I_{th} are expressed as

$$\delta_c = \delta_1 + \delta_a \tag{3.19}$$

$$I_{th}(T) = \frac{q \cdot V_a}{\eta_i(T)} \cdot \left\{ A \cdot N_{th}(T) + B(T) \cdot [N_{th}(T)]^2 + C \cdot [N_{th}(T)]^3 \right\} \tag{3.20}$$

with

$$N_{th}(T) = N_{tr} e^{\frac{\delta_c}{4g_0(T) \cdot L_a}}, \tag{3.21}$$

where N_{th} is the threshold carrier density, A is the non-radiative recombination coefficient, and C is the Auger recombination coefficient. Here the loss from the back mirror R_2 is negligible for typical VCSELs, but if needed can be included into δ_a. η_i and δ_a are obtained from previous dc parameter extraction, while the A and C parameters are approximated as zero to simplify parameter extraction since their values are commonly quite small for VCSELs. This allows the B value to be resolved from Equation 3.19-3.21 once the gain coefficient g_0 and the transparency carrier density N_{tr} are determined.

The gain coefficient g_0 and saturation power P_{sat} are described by

$$g_0(T) = a_0(T) \cdot N_{tr} \tag{3.22}$$

$$P_{sat}(T) = V_a \cdot v_g \cdot h \cdot \nu_0 / \varepsilon\ (T), \tag{3.23}$$

where a_0 is the differential gain, $v_g = c/n_g$ is the group velocity, and ε is the gain compression factor. As the differential gain a_0 and gain compression ε are related to the D- and K-factors, the VCSEL small-signal characteristics are utilized to determine their values.

$$a_0(T) = \frac{\pi^3 \cdot q \cdot \tau_c}{2\eta_i(T)} \cdot d_{ox}^2 \cdot [D(T)]^2 \tag{3.24}$$

$$\varepsilon(T) = v_g \cdot \tau_p \cdot a_0(T) \cdot \left[\frac{K(T)}{4\pi^2 \cdot \tau_p} - 1\right] \tag{3.25}$$

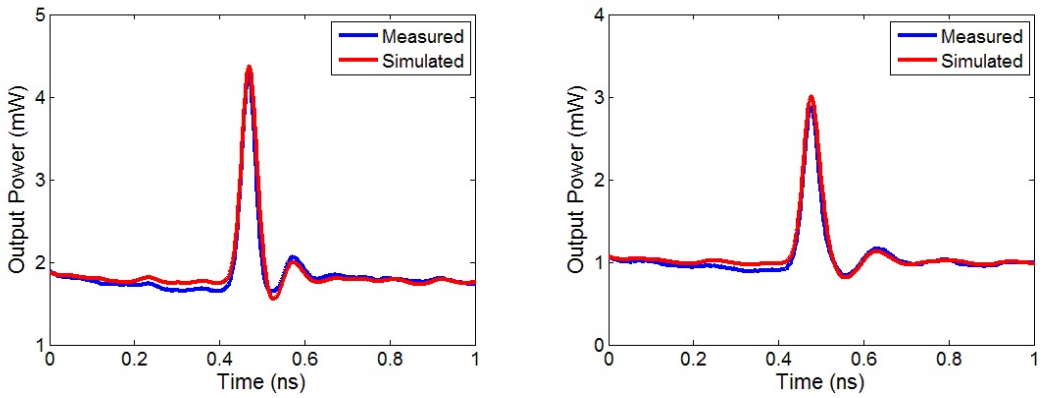
with

$$\tau_p = \tau_c / \delta_c\ , \tag{3.26}$$

where τ_p is the photon lifetime.

Parameters N_{tr}, β, and B are extracted by curve fitting the Fig. 3.6 40ps optical output pulse responses with a 6mA swing centered at a 6mA bias level at 23°C.

In order to describe the parameters thermal dependency, they are modeled as a second-order function of temperature (Equation 3.7). Table 3.4 gives the b_0-b_2 coefficients with T_0=23°C. Comparing the modeled and measured Fig. 3.6 high-speed large-signal pulse responses, the model accurately captures the reduction in pulse amplitude and change in relaxation oscillation behavior as the temperature changes from 23°C to 80°C.



(a) (b)

Figure 3.6: Measured and simulated 40ps optical output pulse responses with 6mA swing centered at a 6mA bias level at (a) 23°C and (b) 80°C.

3.2 Model Verification

Experimental verification of the model is performed at 25Gb/s over different bias and temperature conditions with the Fig. 3.7 test setup. An arbitrary waveform generator (AWG) produces a 2^{15}-1 PRBS data pattern that is applied to the VCSEL through a bias tee for bias tuning. The AWG voltage swing is set to achieve 5dB ER at 6mA bias current and 23°C substrate temperature, and is kept the same for all measurements. An oscilloscope with a 26GHz optical module is utilized to record the

Table 3.4: Rate equation parameters.

Parameter	Unit	Description	b_0	b_1	b_2
δ_c	-	Round trip cavity loss	6.5×10^{-3}	0	0
δ_1	-	Output DBR transmissivity	3.8×10^{-3}	0	0
v_0	Hz	Photon frequency	3.0×10^{14}	0	0
n_g	-	Group index	3.55	0	0
m_c	-	Cavity mode parameter	8.0	0	0
η_i	-	Injection efficiency	0.90	-1.8×10^{-3}	-8.5×10^{-6}
a_0	cm^2	Differential gain	1.3×10^{-15}	-8.3×10^{-18}	8.7×10^{-21}
L_a	cm	Active region length	1.8×10^{-6}	0	0
d_{ox}	cm	Oxide diameter	7.0×10^{-4}	0	0
N_{tr}	cm^{-3}	Transparency carrier density	3.6×10^{18}	0	0
ε	cm^3	Gain compression factor	6.8×10^{-19}	-6.6×10^{-21}	8.9×10^{-24}
β	-	Spontaneous capture efficiency	4.0×10^{-3}	0	0
A	s^{-1}	Non-radiative recombination coefficient	0	0	0
B	cm^3/s	Radiative recombination coefficient	1.3×10^{-10}	-6.2×10^{-13}	-1.3×10^{-15}
C	cm^6/s	Auger recombination coefficient	0	0	0

25Gb/s eye diagrams. VCSEL performance over temperature is observed by placing the device under test (DUT) on a heater. Transition times of 23ps are used in all the modeling results, which matches the equipment used in the measurements.

As shown in the 25Gb/s eye diagrams of Fig. 3.8, excellent matching is achieved between the simulated and measured results at bias currents of 4mA, 5mA, and 6mA for substrate temperatures of 23°C (left column) and 80°C (right column). Note that the same modeling parameters are used in all the simulations, with the coefficients automatically updated as the substrate temperature and bias conditions are varied for the different cases. While the 25Gb/s eye is open at 23°C for a low 4mA

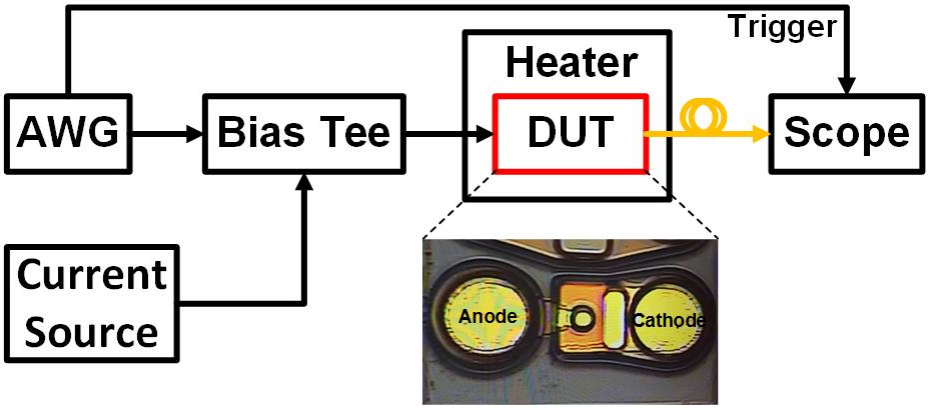


Figure 3.7: Experimental setup for 25Gb/s VCSEL testing.

bias (Fig. 3.8(a)), a relatively large rising-edge overshoot and deterministic jitter is observed both in the measurement and modeling results. For this bias condition, the performance degrades to an unacceptable level at 80°C (Fig. 3.8(b)) due to the degraded slope efficiency and bandwidth. The model correctly captures the reduced jitter and overshoot for the eye diagrams with an increased 5mA bias. While a good eye opening is observed at 23°C (Fig. 3.8(c)), again the performance degrades at 80°C (Fig. 3.8(d)). Operating the device with a 6mA bias provides excellent eye opening at 23°C (Fig. 3.8(e)) and adequate performance at 80°C (Fig. 3.8(f)), with the model correctly displaying small overshoot and deterministic jitter at this bias level. Overall, the Fig. 3.8 results show excellent correlation between the proposed VCSEL model and measurements over varying bias level and temperature.

3.3 Summary

Co-simulation environments which allow for the optimization of driver circuitry with accurate compact VCSEL models are necessary in order to enable efficient optical interconnect transceiver systems operating at data rates in excess of 20Gb/s. The presented compact comprehensive Verilog-A VCSEL model captures thermally-

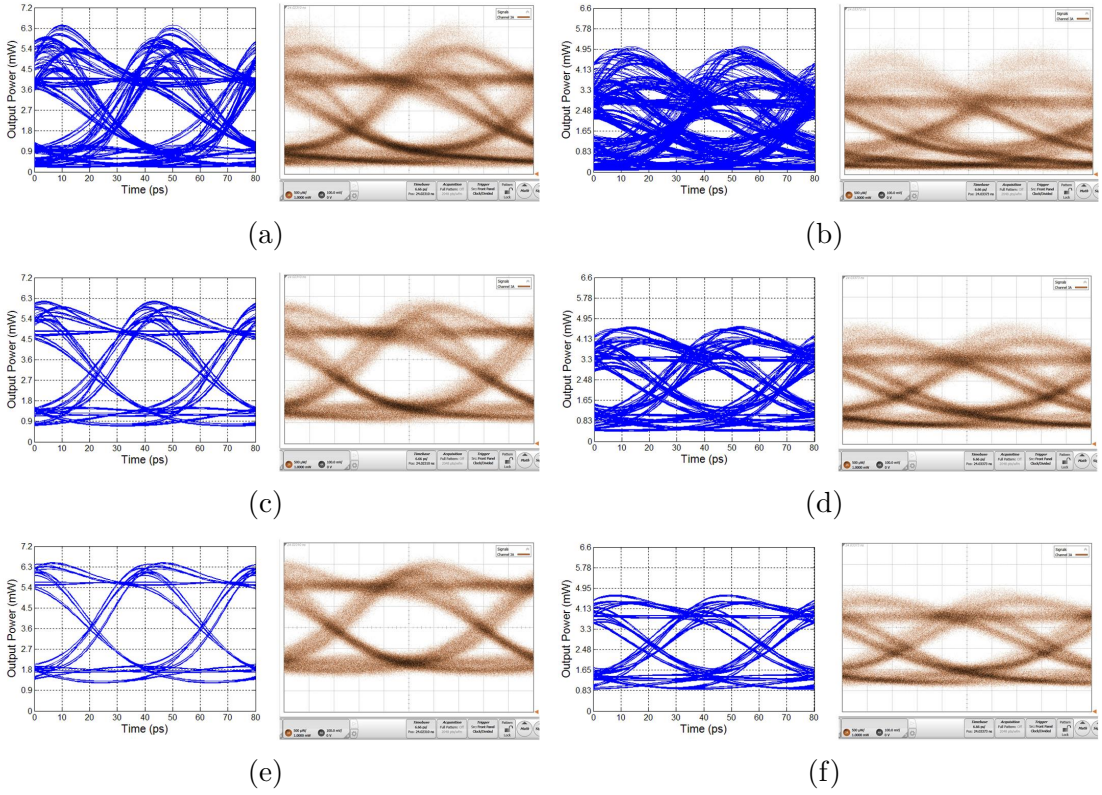


Figure 3.8: Measured and simulated 25Gb/s eye diagrams with 4mA bias current at (a) 23°C and (b) 80°C, 5mA bias current at (c) 23°C and (d) 80°C, and 6mA bias current at (e) 23°C and (f) 80°C.

dependent electrical and optical dynamics and provides dc, small signal, and large-signal simulation capabilities. Model parameters are extracted utilizing dc, small-signal electrical and optical responses, and large-signal high-speed optical pulse responses over a set of bias and temperature conditions. Excellent matching between simulated and measured 25Gb/s eye diagrams at different bias currents and substrate temperatures is achieved.

4. SILICON CARRIER-INJECTION RING MODULATOR MODEL*

Compact and energy efficient WDM interconnect architectures are possible with silicon photonic microring resonator modulators and drop filters [56], as these high-Q devices occupy smaller footprints than large-area Mach-Zehnder modulators [57] and offer inherent wavelength multiplexing without extra device structures, such as array waveguide gratings. The most common high-speed silicon ring modulators operate based on the plasma dispersion effect, with devices based on carrier accumulation, depletion, and injection which display various trade-offs. Accumulation-mode modulators based on metal-oxide-semiconductor (MOS) capacitors can achieve high extinction ratios, but their modulation bandwidth is limited by the relatively high device capacitance [58]. Depletion-mode modulators based on reverse-biased p-n junctions can achieve high speed (40Gb/s) [59], but require large drive voltages [60]. At data rates near 10Gb/s, injection-mode modulators based on forward-biased p-i-n junctions are an attractive device due to their high modulation depths and rapid bias-based resonance wavelength tuning capabilities [61, 62], but their speed with simple non-return-to-zero (NRZ) modulation is limited by both long minority carrier lifetimes and series resistance effects [63].

Pre-emphasis signaling, which improves optical transition times, is necessary in order to achieve data rates near 10Gb/s with carrier-injection ring modulators [18, 19,62,63]. As the effective device time constant is different during a rising transition, where it is limited by long minority carrier lifetimes, versus a falling transition, where it is limited by series resistance, nonlinear pre-emphasis waveforms are often used

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[18, 19]. In addition, the devices optical dynamics must be considered in optimizing the pre-emphasis waveforms [64,65]. The optical bandwidth is limited by the photon lifetime, which is related to the ring resonators Q factor, and the rings phase delay during modulation should be considered to capture the non-linear optical dynamics. In order to compensate for these electrical and optical dynamics, the transmitter circuit must be carefully designed to supply a high-speed pre-emphasis signal with the proper pulse depth, pulse duration, and DC bias. This motivates co-simulation environments with compact optical device simulation models that accurately capture optical and electrical dynamics.

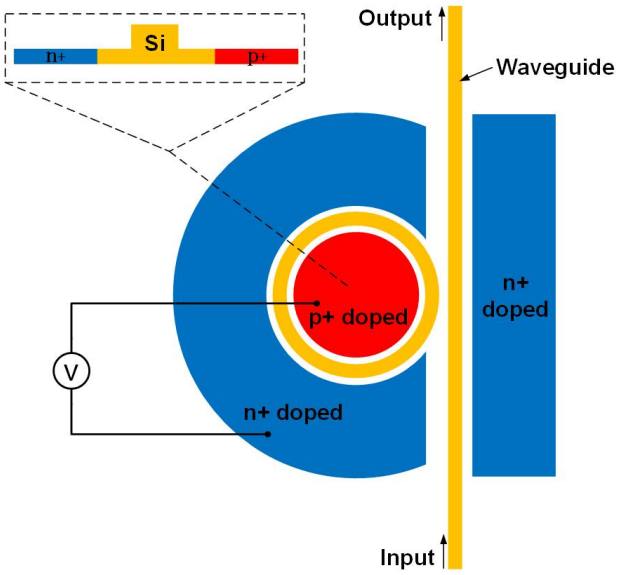


Figure 4.1: Top and cross section views of a carrier-injection ring resonator modulator.

While previous models have been developed for accumulation-mode [66] and depletion-mode [17] ring modulators, previous models for injection-mode ring devices [63, 67] have lacked accurate modeling of the large-signal p-i-n forward-bias

behavior [68] and non-linear optical dynamics in a format suitable for efficient co-simulation. This chaper presents a compact Verilog-A model for carrier-injection ring modulators which includes both non-linear electrical and optical dynamics [69]. The model, which combines an accurate p-i-n electrical [66] and a dynamic ring resonator model [64], is described in Section 1. Section 2 presents experimental verification of the carrier-injection ring resonator model, which was performed both at 8Gb/s with symmetric drive signals to study the impact of pre-emphasis pulse duration, pulse depth, and dc bias, and at 9Gb/s with a 65nm CMOS driver capable of asymmetric pre-emphasis pulse duration. The potential for 15Gb/s operation is shown by utilizing the presented model for optimization of the asymmetric pre-emphasis signal waveform in Section 3. Finally, Section 4 concludes the chapter.

4.1 Model Description

As shown in Fig. 4.1, the modeled carrier-injection ring modulator consists of a ring waveguide coupled to a straight waveguide, with p+ and n+ doping in the inner and outer ring regions, respectively. Accurate high-speed modeling requires inclusion of both electrical and optical dynamics, with Fig. 4.2 showing a flow chart of the model implementation. When a driving voltage is applied, the dynamic current response is determined by a p-i-n diode SPICE model based on a moment-matching approximation of the ambipolar diffusion equation [68]. After obtaining the current dynamics, the total carriers are calculated by integrating this diode current. However, as some of the carriers recombine and remain inside the waveguide during signal transients, only a portion act as free carriers and impact the effective ring index [70]. Utilizing a subsequent high-pass filter with a time constant equal to the carrier lifetime allows extraction of the free carriers used to calculate the ring index and loss changes due to the plasma dispersion effect [71]. Finally, the optical output

power is related to the changes in refractive index and absorption coefficient by a dynamic ring resonator model which accurately considers the rings cumulative phase shift [64].

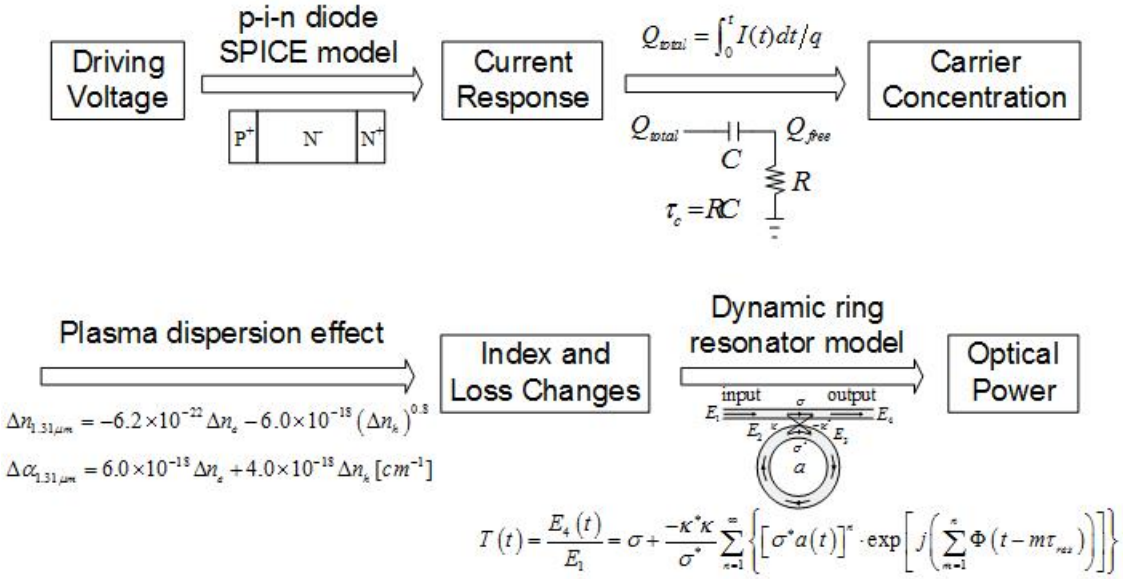


Figure 4.2: Model flow chart.

The electrical SPICE model is described in Fig. 4.3. Electrically, the carrier injection ring modulator is treated as a p-i-n diode (Fig. 4.3(a)). As shown in Fig. 4.3(b), the total voltage across the device is distributed across the diodes intrinsic region, $V_{epi}(V(10,12))$, two junctions, $V_j(V(12,20))$, and the two terminal contact resistances, V_c. The charge, q_0, required for the total current response, is given by modeling the junction characteristics with the applied voltage, V_j, shown in Fig. 4.3(c). In order to accurately model both the dc and dynamic I-V characteristics, the total current I consists of the current injected into the intrinsic region, I_{epi}, and the current due to the anode recombination effect, I_r. As shown in Fig. 4.3(d),

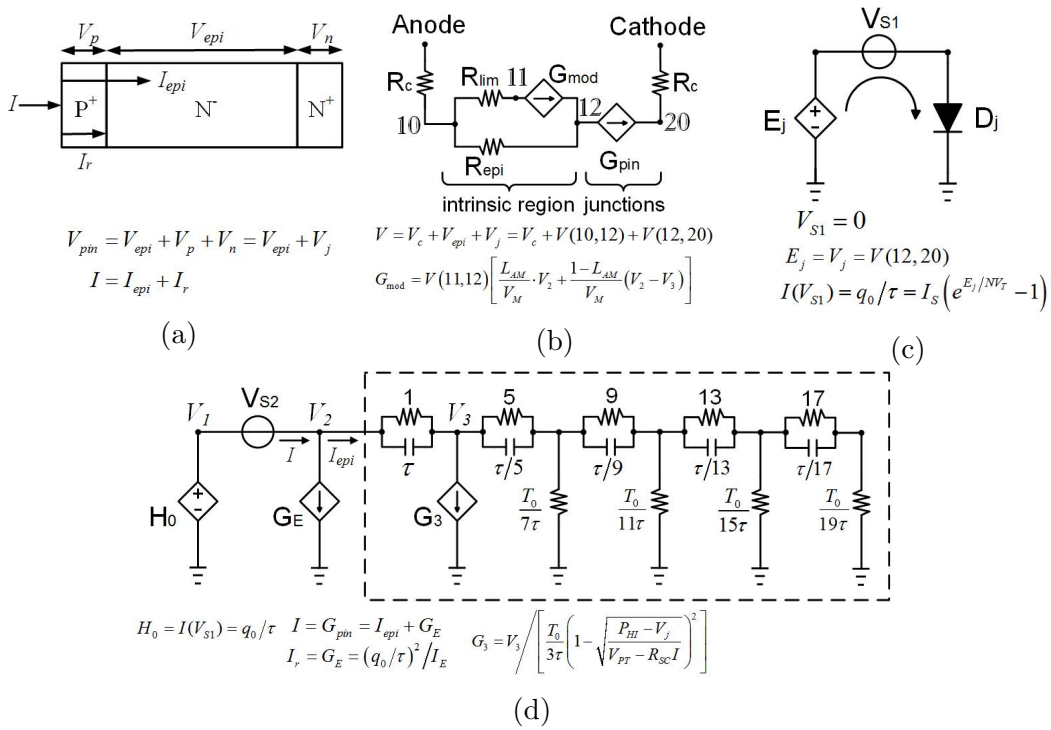


Figure 4.3: p-i-n diode and SPICE model schematic: (a) p-i-n diode cross section, (b) p-i-n voltage distribution model, (c) junction I-V characteristic model, and (d) p-i-n current distribution model.

I_r is calculated via q_0 and I_{epi} is modeled by a tenth-order network, modified from [68] for enhanced accuracy. The tenth order network is designed according to an approximation of the transfer function (the ratio of the intrinsic region current, I_{epi}, and charge, q_0) via asymptotic waveform evaluation (AWE), which is deducted from the ambipolar diffusion equation [72]. The current through the diode D_j, equal to q_0/τ, is converted to a voltage via the current-controlled voltage source H_0 to drive a network which models the current dynamics in the intrinsic region. Three important non-linear effects, described by current sources G_{mod}, G_E, and G_3, are included. G_{mod}, which is a function of $V(11,12)$, represents the conductivity modulation in the intrinsic region, G_E expresses the anode recombination effect, and G_3 implements

the moving boundary effect during reverse recovery.

Table 4.1: Model parameters of the p-i-n diode, with values for a 5μm device.

Parameter	Unit	Description	Empirical Range	Value
R_C		Contact resistance	10-100	50
I_S	A	Saturation current	1×10^{-14}-1×10^{-12}	5.78×10^{-14}
N	-	Emission coefficient	1-2	1.46
P_{HI}	V	Build-in voltage	0.5-1	0.7
T_0	s	Transit time	1×10^{-10}-1×10^{-9}	1.046×10^{-10}
I_E	A	Emitter recombination knee current	1.0×10^{-4}-1.0×10^{-2}	1.0×10^{-3}
V_M	V	High-injection voltage drop on the base	0-0.5	0.12
R_{lim}	Ω	Carrier-scattering series resistance	1×10^{-3}-3×10^{-3}	1.8×10^{-3}
L_{AM}	-	Forward-recovery coefficient	0-0.1	0.03
τ	s	Carrier Lifetime in the base	1.0×10^{-10}-1.0×10^{-8}	1.0×10^{-9}
R_{epi}	Ω	Base region resistance	1.0×10^{2}-1.0×10^{3}	300
V_{PT}	V	Reverse-recovery coefficient	5-20	10
R_{SC}	Ω	Reverse-recovery coefficient	1-100	18

Table 4.1 summarizes the electrical model parameters and shows values for a 5μm radius device. The extraction procedure for these parameters is described by Fig. 4.4. After initializing the parameters with reasonable empirical values, their values are obtained via curve fitting to dc and high frequency measurements. Eight of the parameters are extracted from the dc characteristic of Fig. 4.5. An iterative process is used to curve fit this data, with high sensitivity parameters R_C, I_S, and N first estimated, followed by the low-sensitivity parameters P_{HI}, I_E, V_M, R_{lim}, and R_{epi} related to the previously mentioned non-linear effects. In the parameter extraction procedure, current levels above 100μA are given higher weight in the curve fitting

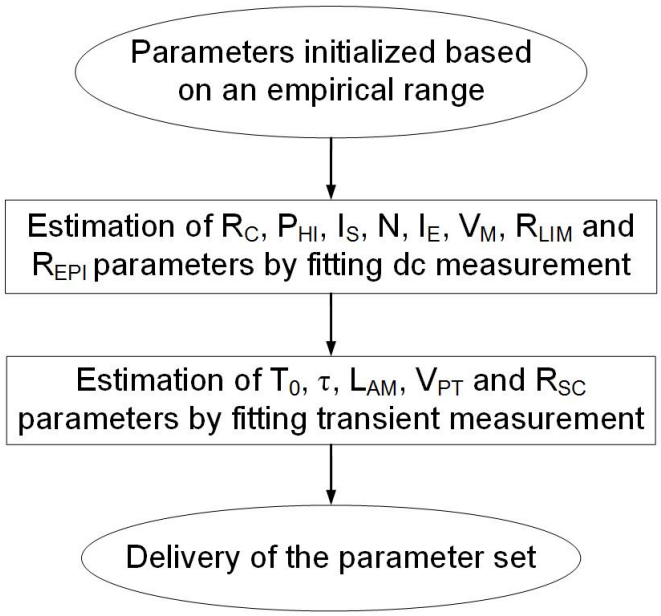


Figure 4.4: Electrical p-i-n diode parameter extraction procedure.

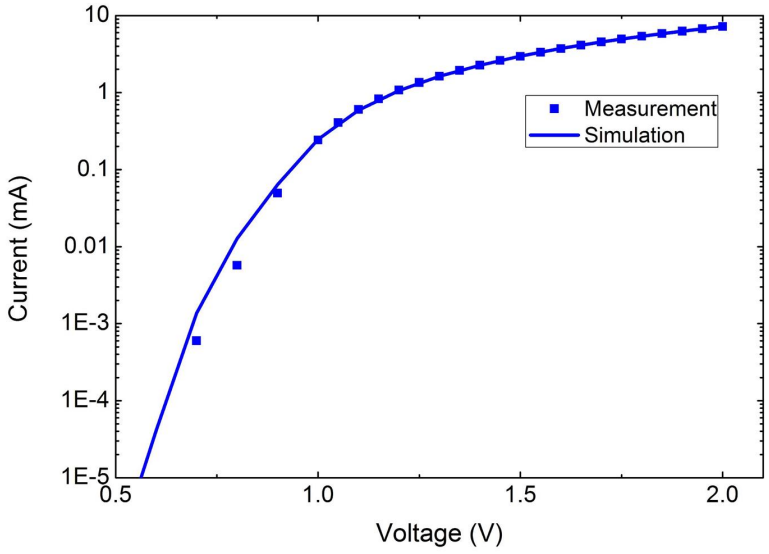


Figure 4.5: Measured and simulated dc I-V characteristic.

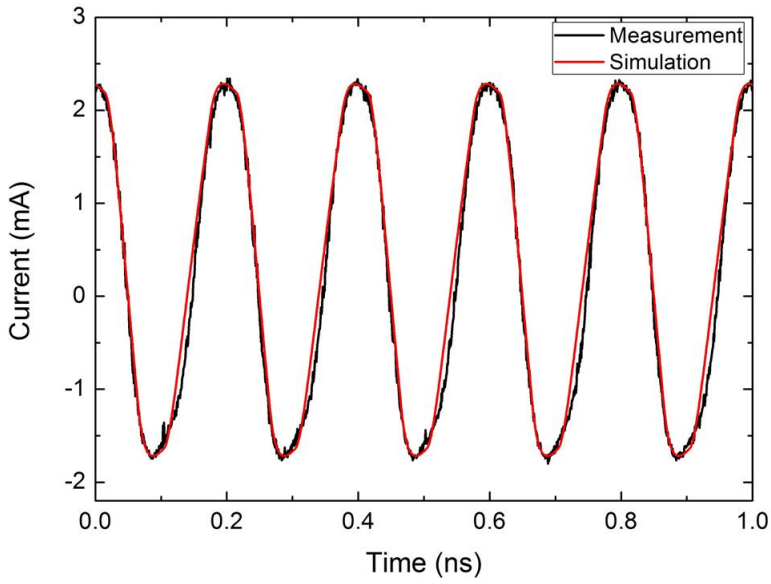
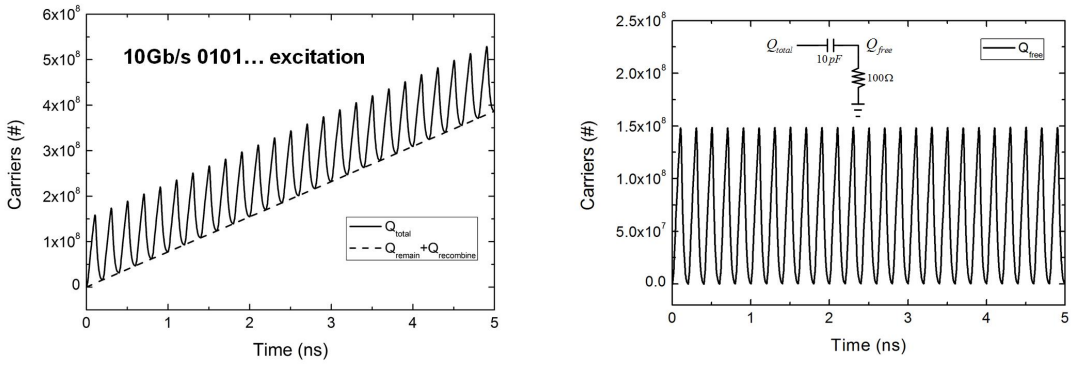


Figure 4.6: Measured and simulated transient response with a 10Gb/s clock pattern with voltage swing between -0.5V and 1.5V.

since the model is targeted for optical interconnect applications with NRZ modulation. As shown in Fig. 4.5, excellent matching is achieved at these current levels at the cost of some minor error at low current conditions. The remaining five parameters are extracted from the Fig. 4.6 dynamic current response to a 10Gb/s clock pattern with a voltage swing between -0.5V and 1.5V. In a similar manner, high sensitivity parameters T_0 and τ are first estimated, followed by the low-sensitivity parameters L_{AM}, V_{PT} and R_{SC}. Excellent amplitude matching is achieved between the transient simulation and measured results, implying that the current dynamics are captured well. While there is slightly more harmonic content in the measured results, this small error is not deemed critical for NRZ modulation applications. Overall, utilizing the measured dc I-V characteristic and transient response for parameter extraction allows for parameters R_C, I_S, N, P_{HI}, T_0, τ, R_{lim}, and R_{epi} to be

well defined, while low-sensitivity parameters I_E, V_M, L_{AM}, V_{PT}, and R_{SC} are more softly defined.



(a) (b)

Figure 4.7: Carriers obtained from the electrical model with a 10Gb/s clock pattern with voltage swing between -0.5V and 1.5V: (a) total carriers and (b) free carriers extracted utilizing a high-pass filter with a time constant equal to the carrier lifetime.

After obtaining the dynamic current response, the total carriers are calculated by integrating the diode current with $Q = \int_0^t I\,(t)\,dt/q$. The total carriers consist of the following components [70]

$$Q_{total}\,(t) = Q_{remain}\,(t) + Q_{recombine}\,(t) + Q_{free}\,(t)\,, \tag{4.1}$$

which correspond to carriers remaining in the waveguide during signal transients, Q_{remain}, carriers recombining inside the p-i-n diode, $Q_{recombine}$, and the free carriers, Q_{free}, which impact the effective ring index and loss [71]. As shown in Fig. 4.7, the remaining and recombining carriers increase with time, while the free carriers can be extracted utilizing a high-pass filter with a time constant equal to the carrier lifetime. These free carriers are then used to calculate the ring index and loss changes due to

the plasma dispersion effect. At a wavelength of 1.31μm, which is near the resonance wavelength of the devices characterized in this work,

$$\Delta n_{1.31\mu m} = -6.2 \times 10^{-22} \Delta n_e - 6.0 \times 10^{-18} (\Delta n_h)^{0.8} \tag{4.2}$$

$$\Delta \alpha_{1.31\mu m} = 6.0 \times 10^{-18} \Delta n_e + 4.0 \times 10^{-18} \Delta n_h \ [cm^{-1}], \tag{4.3}$$

where Δn_e and Δn_h are the electron and hole carrier densities $[cm^{-3}]$, respectively. This model assumes $\Delta n_e = \Delta n_h$.

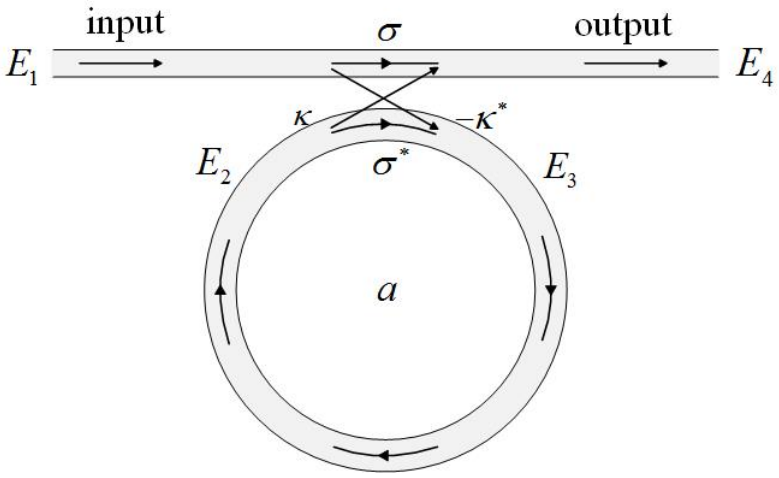


Figure 4.8: Microring resonator optical model.

The optical output power is related to the change in refractive index and absorption coefficient by a dynamic ring resonator model which assumes lossless coupling and a single polarization (Fig. 4.8). Considering the ring resonator's index dynamics, its time-dependent transmission is described by

$$T(t) = \frac{E_4(t)}{E_1} = \sigma + \frac{-\kappa^* \kappa}{\sigma^*} \sum_{n=1}^{\infty} \left\{ [\sigma^* a(t)]^n \cdot \exp\left[j \left(\sum_{m=1}^{n} \Phi(t - m\tau_{res}) \right) \right] \right\}, \tag{4.4}$$

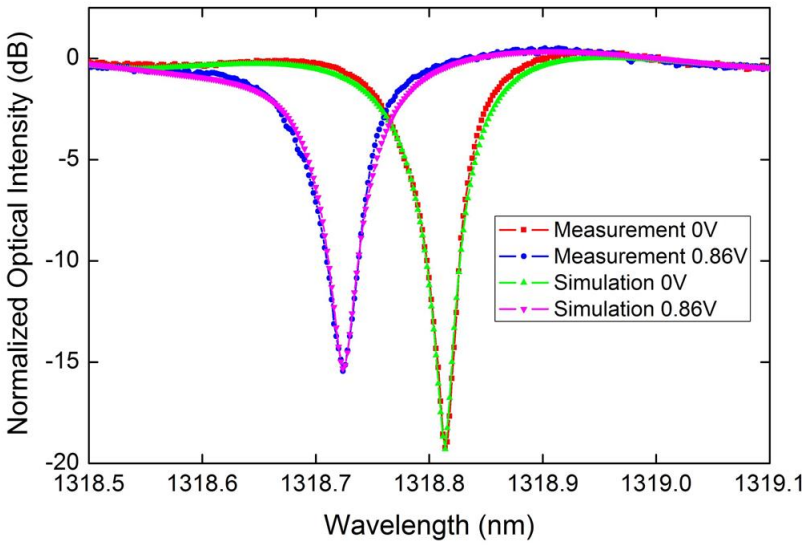


Figure 4.9: Measured and simulated ring resonator through port optical spectrums. These curves are normalized to the input laser power, accounting for 10dB of grating coupler loss.

where σ and κ are coupling coefficients, $|\kappa^2| + |\sigma^2| = 1$, a is the ring loss coefficient with zero loss corresponding to $a = 1$ and which relates to the absorption coefficient α as $a^2 = exp(-\alpha L)$, L is the ring circumference, Φ is the phase shift, τ_{res} is the resonator round-trip time, and $|T(t)|^2$ is the optical transmission power [64]. The three critical model parameters σ, a, and n_{eff} are extracted by curve fitting the steady-state transmission

$$T(t) = \sigma + \frac{-\kappa^* \kappa}{\sigma^*} \sum_{n=1}^{\infty} \left\{ \left[\sigma^* a(t) \right]^n \cdot \exp\left[jn\Phi(t) \right] \right\} = \frac{\sigma - a(t) \cdot \exp\left[j\left(\Phi(t)\right) \right]}{1 - \sigma^* a(t) \cdot \exp\left[j\left(\Phi(t)\right) \right]} \quad (4.5)$$

where

$$\Phi(t) = \frac{2\pi}{\lambda} n_{eff}(t) L, \quad (4.6)$$

λ is the optical wavelength, and n_{eff} is the effective index. As shown in Fig. 4.9, by

fitting the measured through port optical spectrum from a 5μm ring resonator with applied bias voltages of 0V and 0.86V, $\sigma = 0.9944$, $a = 0.9931$, and $n_{eff} = 2.5188$, are obtained. Utilizing these values in the model described by Equation 4.4 allows for excellent matching with measured optical responses with large signal high-speed modulation, which is detailed in Section 2.

4.2 Comparison of Simulated and Measured Results

This section presents a comparison of the presented model simulation results with high-speed large-signal measurements. Experimental verification of the model is performed both at 8Gb/s with symmetric drive signals to study the impact of pre-emphasis pulse duration, pulse depth, and dc bias, and at 9Gb/s with a 65nm CMOS driver capable of asymmetric pre-emphasis pulse duration.

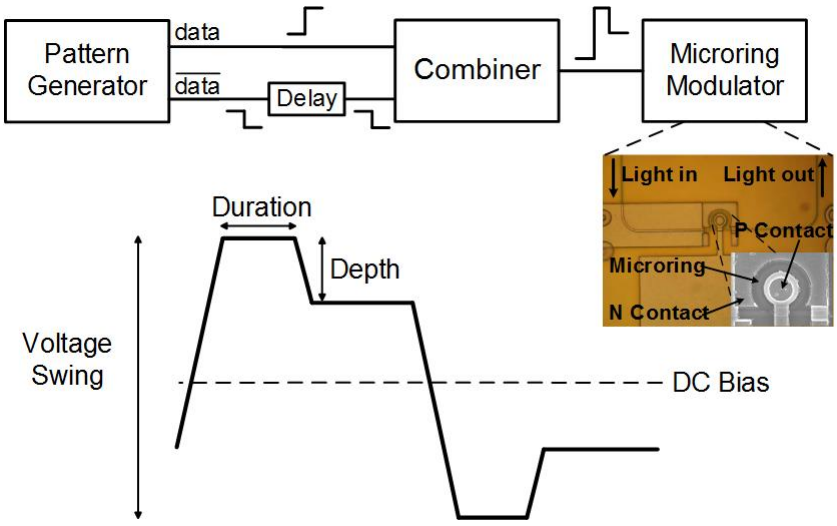


Figure 4.10: Pre-emphasis NRZ signal generation and waveform.

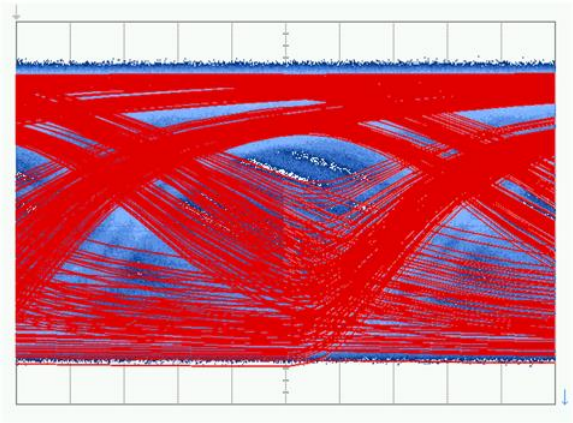
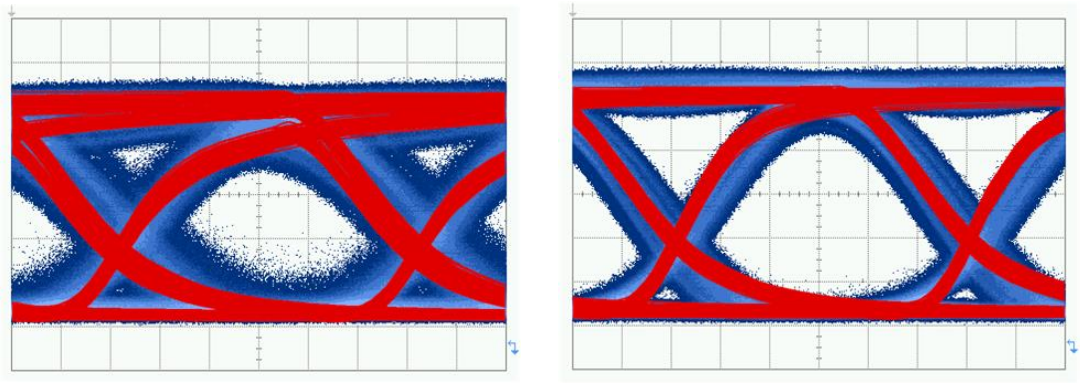


Figure 4.11: 8Gb/s measured (blue) and simulated (red) optical eye diagrams with simple NRZ modulation without pre-emphasis.

4.2.1 Symmetric Pre-Emphasis Modulation with External Driver

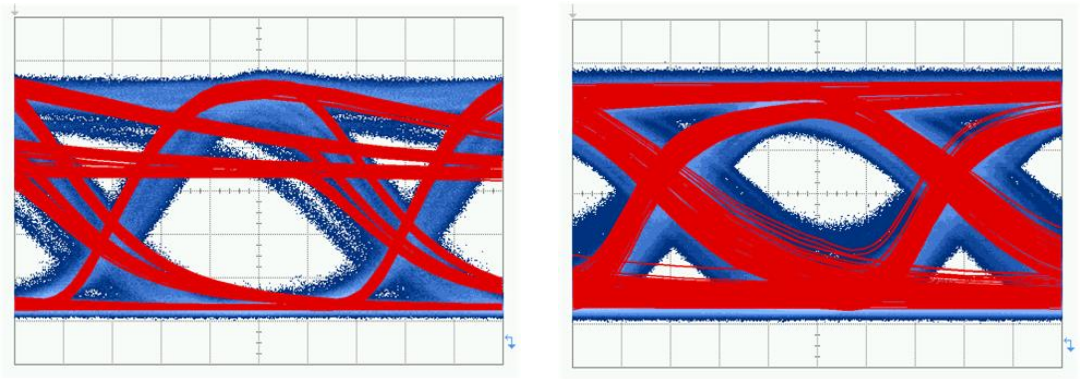
In order to demonstrate the ring modulator model accuracy, comparisons are made with the measured responses of a 5μm radius carrier-injection ring modulator operating at 8Gb/s with pre-emphasis modulation. As shown in the experimental setup of Fig. 4.10, differential outputs of a high-speed pattern generator are combined to generate a pre-emphasis NRZ drive signal. The impact of pre-emphasis pulse duration, pulse depth, and dc bias are investigated, with a constant $2V_{pp}$ swing maintained as these parameters are varied. Vertical couplers are used to provide light from a CW laser to the ring modulator input port and direct the modulated light out to a fiber connected to an optical oscilloscope for eye diagram generation. In all the measured eye diagrams, the CW laser wavelength is tuned to align with the 0V ring modulator resonance wavelength. Transition times of 40ps are used in all the external modeling results, which matches the equipment used in the measurements.

As predicted by the proposed ring model, utilizing a simple drive signal that is centered at a 0.7V bias without pre-emphasis results in a very poor eye diagram



(a) (b)

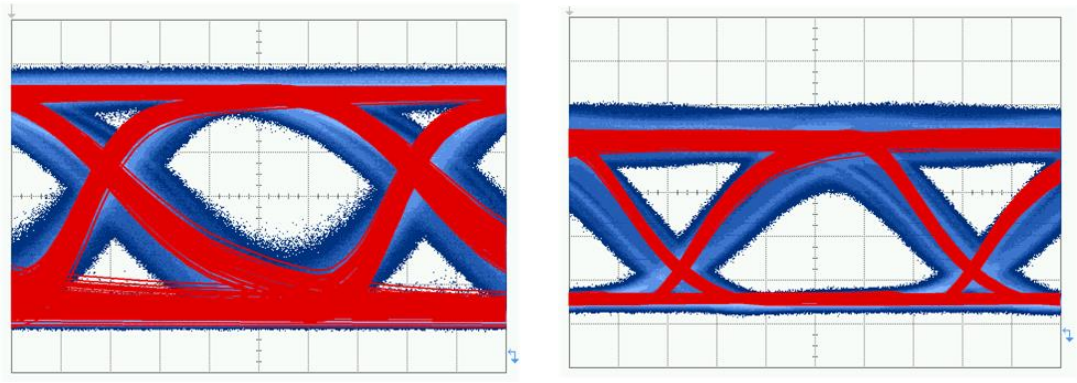
Figure 4.12: Impact of pre-emphasis pulse duration on 8Gb/s measured and simulated optical eye diagrams with 0.8V pulse depth, 0.7V dc bias, and pulse duration of (a) 40ps and (b) optimal 80ps.



(a) (b)

Figure 4.13: Impact of pre-emphasis pulse depth on 8Gb/s measured and simulated optical eye diagrams with 80ps pulse duration, 0.7V dc bias, and pulse depth of (a) 0.9V and (b) 0.7V.

with a $2^7 - 1$ PRBS data pattern (Fig. 4.11). Here the measured eye is completely closed by the systems random jitter, which is not included in the modeling results. Utilizing an optimal 0.8V pre-emphasis pulse depth, the impact of pulse duration is shown in Fig. 4.12. While a 40ps duration allows the eye to partially open, the



(a) (b)

Figure 4.14: Impact of pre-emphasis dc bias on 8Gb/s measured and simulated optical eye diagrams with 80ps pulse duration, 0.8V pulse depth, and dc bias of (a) 0.75V and (b) 0.65V.

height and width are still degraded due to the long rise time caused by the minority carrier lifetime. Increasing the pulse duration to 80ps provides optimal eye opening, with excellent matching between the simulated and measured eyes observed.

Relative to the optimal eye diagram of Fig. 4.12(b), Fig. 4.13 shows how the modeling results correlate with measurements as the pre-emphasis pulse depth is varied. An increase in pulse depth to 0.9V results in excessive overshoot during a rising transition and slow settling to the steady-stage high level due to the relatively low amount of injected carriers after the pre-emphasis pulse. While the models transfer function approximation does introduce some error in these low-carrier recombination dynamics, which results in some offset in the precise positioning of the falling edge transitions, both the Fig. 4.13(a) simulated and measured results show similar significant falling-edge deterministic jitter. A decrease in pulse depth to 0.7V produces excessive charge for the steady-state high level, which results in slow fall times due to the modulators series resistance limiting carrier extraction (Fig. 4.13(b)).

Fig. 4.14 shows the impact of dc bias. As shown in Fig. 4.14(a), an increase in

dc bias to 0.75V produces excessive charge for the steady-state high level which is similar to a decrease in pulse depth to 0.7V. A decrease in DC bias to 0.65V results in slower carrier injection and degraded rising transitions (Fig. 4.14(b)). Overall, the Fig. 4.12, 4.13, and 4.14 results show excellent correlation between the proposed ring modulator model and measurements over varying pre-emphasis pulse duration, pulse depth, and dc bias.

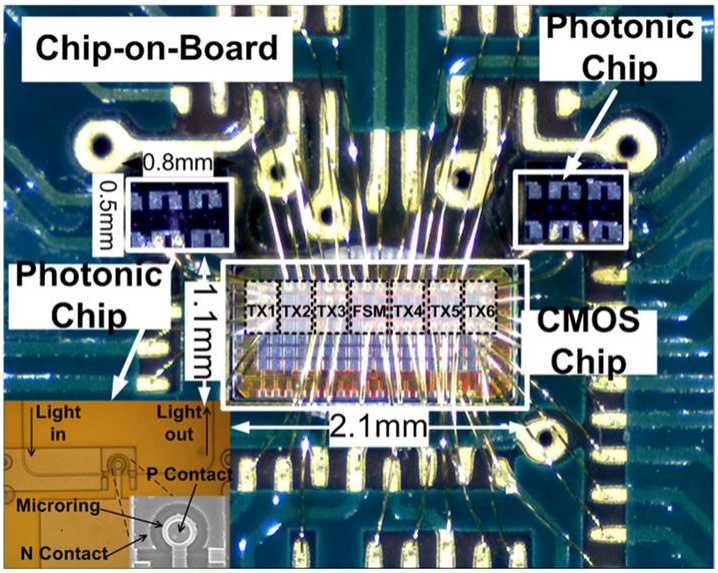


Figure 4.15: Hybrid-integrated optical transmitter prototype bonded for optical testing.

4.2.2 Asymmetric Pre-Emphasis Modulation with CMOS Driver

A key objective of the model is to enable an opto-electronic co-simulation environment which allows for both the optimization of transceiver circuitry and the ability to study the impact of optical device parameters. The co-simulation capabilities are demonstrated by comparing simulated modeling results with the measured responses of the 5μm radius carrier-injection ring modulator driven with a custom

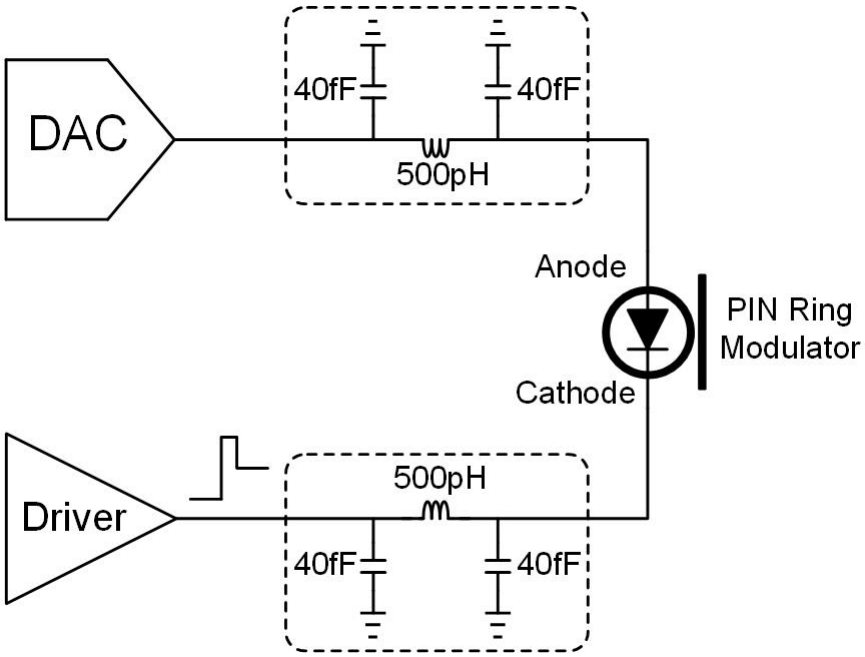


Figure 4.16: Co-simulation schematic with 65nm CMOS high-speed CMOS driver, bias DAC, and Verilog-A carrier-injection ring resonator modulator model.

designed CMOS driver. As shown in hybrid-integrated prototype in Fig. 4.15 the pre-emphasis NRZ driver implemented in a 65nm CMOS technology [19] is wire bonded both to the PCB and the silicon ring modulator for testing. While the pre-emphasis pulse depth is fixed in this CMOS driver implementation, the prototype does have the ability to adjust the dc bias and the pre-emphasis pulse duration in an asymmetric manner for independent optimization of the rising and falling responses.

Fig. 4.16 shows the co-simulation schematic in a CADENCE environment, with transistor-level schematics for the high-speed driver and bias digital-to-analog converter (DAC), lumped elements for the wirebond interconnect, and the Verilog-A carrier-injection ring resonator modulator model. The single-ended driver provides a high-speed $2V_{pp}$ output swing with independent dual-edge pre-emphasis duration tuning on the cathode of the ring modulator, while the 9-bit bias tuning DAC is

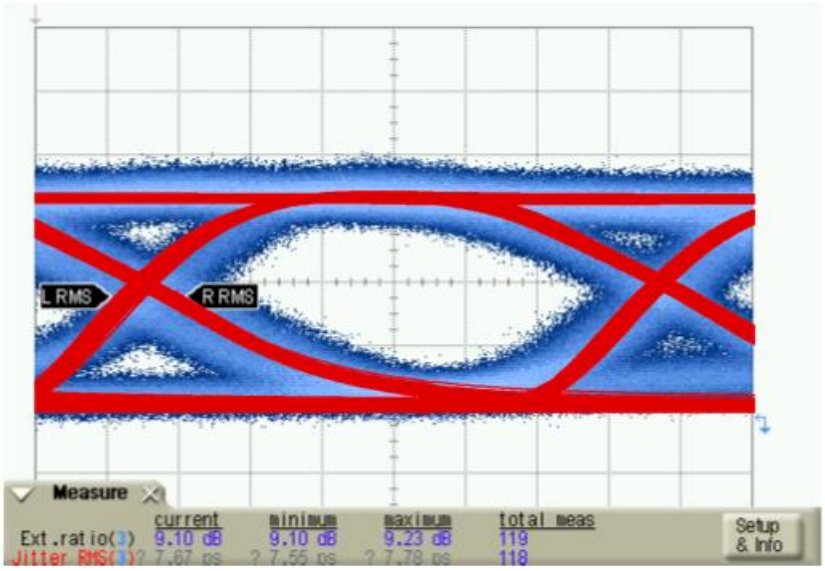


Figure 4.17: 9Gb/s measured and co-simulated optical eye diagrams with the ring resonator modulator driven by the 65nm CMOS driver.

connected to the anode for dc bias adjustment [19]. 500pH inductors are used to model the 0.5mm bondwires that connect the high-speed driver and DAC to the modulator, while 40fF capacitors model the chips bondpads. Fig. 4.17 shows that the optimal 9Gb/s measured and co-simulated eye diagrams, balancing extinction ratio and eye opening, are achieved when the anode bias is 1.45V and asymmetric pulse durations for rising and falling transitions are 70ps and 50ps, respectively.

4.3 Asymmetric Pre-Emphasis Optimization

The results of Section 2 showed that pre-emphasis NRZ signaling can significantly improve achievable date rates of carrier-injection ring resonator modulator-based optical interconnect systems. While the CMOS prototype of [19] showed the effectiveness of asymmetric pre-emphasis pulse duration, it lacked the ability to independently optimize the high and low-level pulse depth. Thus, the presented model is utilized to explore the potential for further speed improvements with a driver capable

of asymmetric pre-emphasis pulse depth.

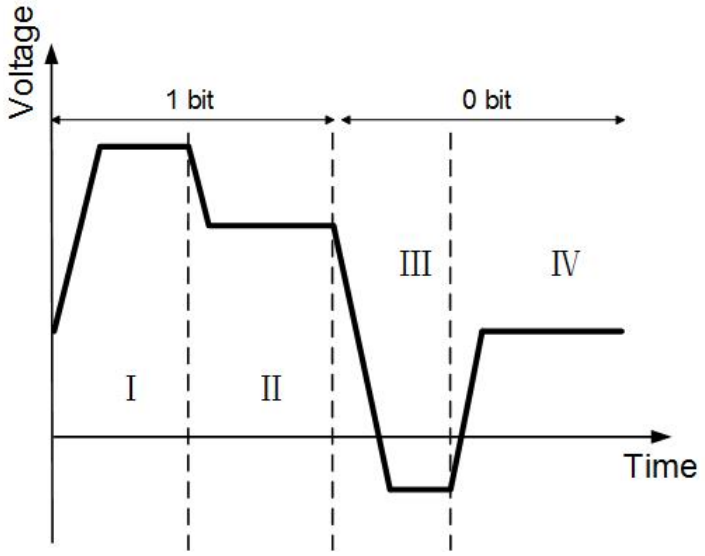
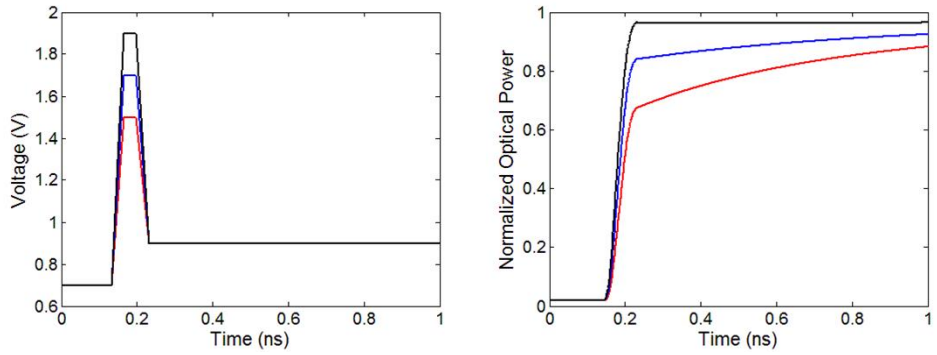


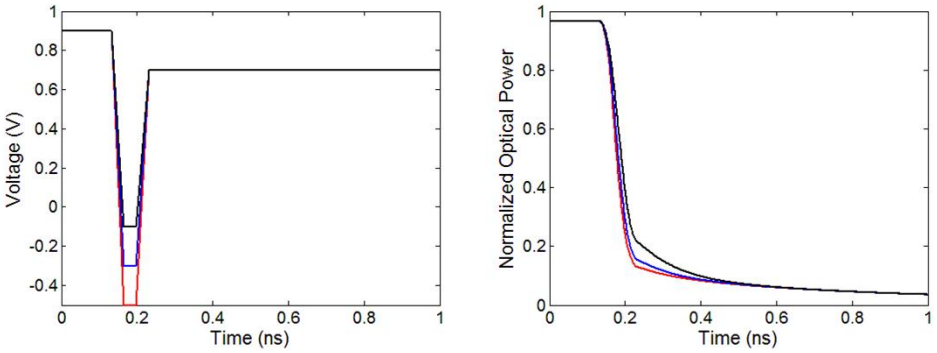
Figure 4.18: An asymmetric pre-emphasis NRZ signal with independent peak (I) and steady-state (II) high levels and peak (III) and steady-state (IV) low levels.

Fig. 4.18 shows that a pre-emphasis NRZ signal can be classified as having four independent levels, with peak (I) and steady-state (II) high levels and peak (III) and steady-state (IV) low levels [11]. In order to optimize the transient response of the rising edge, the peak value pulse duration (I) should be set such that the amount of injected carriers is enough to obtain maximum optical output power, while the pulse depth (II) should be tuned to where the injected carriers and the carriers lost due to recombination have dynamic equilibrium. During the falling edge, the peak value pulse duration (III) should be set such that the carriers inside the waveguide are sufficiently extracted to obtain minimum optical output power, while the pulse depth (IV) should be tuned to the sub-threshold voltage of the p-i-n diode for a subsequent faster rising transition. Note, given the devices non-linear response and

a certain maximum peak-to-peak swing constraint, the peak levels in (I) and (III) may need to slightly sub-optimal relative to the optimal rising-edge or falling-edge step responses in order to balance the achievable extinction ratio and intersymbol interference (ISI) at a certain data rate.



(a)



(b)

Figure 4.19: Asymmetric pre-emphasis waveforms and modulator (a) rising-edge step response with 1.9V (black), 1.7V (blue), and 1.5V (red) peak high levels, and b (b) falling-edge step response with -0.1V (black), -0.3V (blue), and -0.5V (red) peak low levels.

As an example, consider the modeled ring resonator 15Gb/s step responses shown in Fig. 4.19. At this high data rate, a maximum pulse duration close to the 66.7ps bit period is utilized to maximize charge injection and extraction. For the steady-

state low value (IV), 0.7V is chosen to introduce minimal carriers and allow for a subsequent fast rising transition, while 0.9V is selected for the steady-state high value (II) to achieve close to the maximum extinction ratio. As shown in the rising-edge step response of Fig. 4.19(a), a 1.9V peak high voltage (I) injects charge in one bit period close to the 0.9V steady-state high level amount and achieves a near-optimal step response. However, given the 2V peak-to-peak swing constraint, excessive ISI results in the falling-edge step response (Fig. 4.19(b)) with a -0.1V peak low-level voltage (III) due to the contact resistance-limited extraction of carriers. While a -0.5V peak low-level voltage improves the falling-edge response, this results in a slow rising-edge response. Overall, a balance in the high-level and low-level ISI is achieved with peak levels of 1.7V and -0.3V. Note that this asymmetric waveform has a higher steady-state low level of 0.7V, relative to the symmetric pre-emphasis signals of 1.7V, 0.9V, -0.3V, and 0.5V. This results in a significant improvement in the rising edge response and a larger dynamic extinction ratio (ER), as shown in the modeled 15Gb/s optical eye diagrams of Fig. 4.20(a).

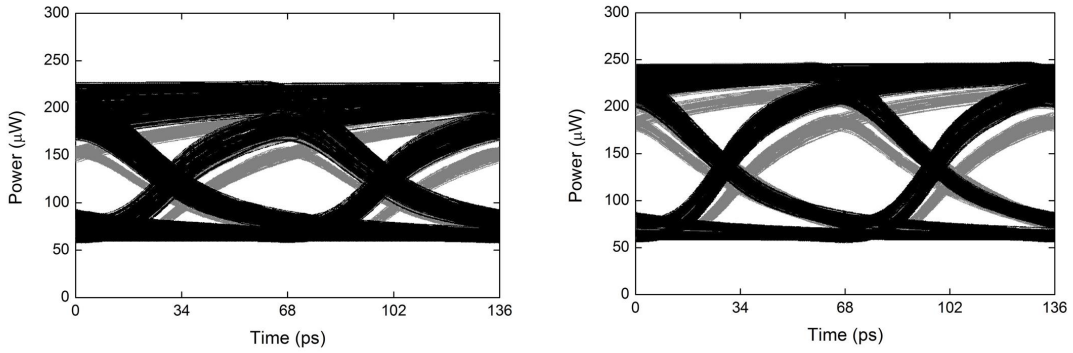


Figure 4.20: 15Gb/s simulated optical eye diagrams with symmetric (gray) and asymmetric (black) pre-emphasis pulse depth. Device per-terminal contact resistance is (a) the measured 50Ω value and (b) reduced to 25Ω.

The proposed model can also be utilized to investigate the impact of critical optical device parameters to guide future device development. One key device parameter is the contact resistance, as a device with lower contact resistance can support larger current values to inject/extract an increased amount of charge with a given voltage swing. As shown in Fig. 4.20(b), reducing the per-terminal contact resistance to 25Ω from its current 50Ω value results in further improvements in both eye height and width, with the asymmetric pre-emphasis waveform maintaining superior performance. Another key device design parameter is the doping profile, as the p- and n-doped regions should be in close proximity to allow for fast charge injection, while maintaining a sufficient intrinsic region and low transmission loss. For example, impressive 25Gb/s modulation was recently achieved with a 1.25V swing CMOS driver with a carrier-injection ring modulator utilizing an optimized doping profile and side-wall-grating waveguides [73]. By extracting the relevant model parameters of advanced modulator structures from semiconductor device solvers, such as Sentaurus or Lumerical, the proposed Verilog-A model allows for rapid co-simulation and co-optimization of both high-speed driver circuits and optical devices in the device development phase.

4.4 Summary

Optical interconnect system efficiency is dependent on the ability to optimize the transceiver circuitry for low-power and high-bandwidth operation, motivating accurate co-simulation environments. The presented compact Verilog-A model for carrier-injection ring resonator modulators includes both non-linear electrical and optical dynamics, allowing for efficient optimization of transmitter signal levels and pre-emphasis settings. Excellent matching between simulated and measured optical eye diagrams is achieved both at 8Gb/s with symmetric drive signals with varying

amounts of pre-emphasis pulse duration, pulse depth, and dc bias, and at 9Gb/s with a 65nm CMOS driver capable of asymmetric pre-emphasis pulse duration. Modeling results also show the potential for 15Gb/s operation by both optimizing the pre-emphasis waveforms with asymmetric pulse depth and reducing device contact resistance.

5. SILICON CARRIER-DEPLETION RING MODULATOR MODEL

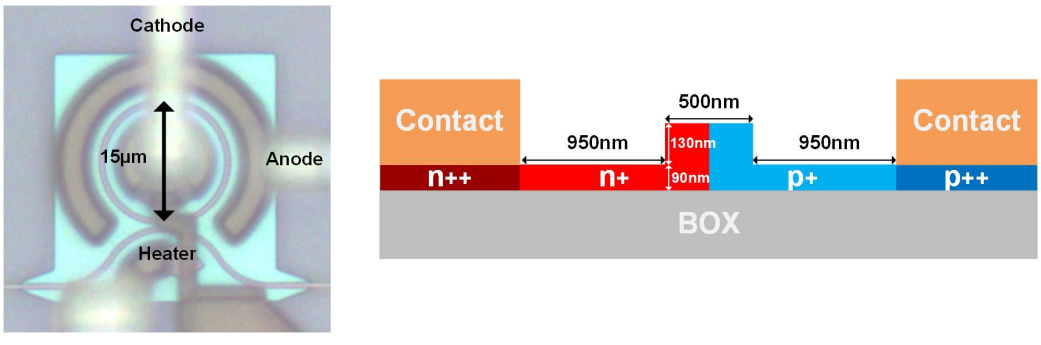
The most common Electro-Optic modulators on SOI platform are carrier-injection and carrier-depletion modulators. For carrier-injection ring modulators, large modulation depth and efficiency are achieved at the cost of modulation bandwidth [19], which limits the application in ultra-high speed data communication. In contrast, carrier-depletion modulators have higher modulation speed ∼40Gb/s. An 320Gb/s 8-channel WDM transmitter based on carrier-depletion ring modulators was demonstrated in [59]. The modulation speed of carrier-depletion ring modulators is limited by electrical and optical bandwidth. The electrical bandwidth is determined by the RC bandwidth of the ring modulator where the voltage-controlled capacitance results in a non-linear frequency response with a large signal. The optical bandwidth is limited by photon lifetime related to the Q factor of ring resonators where the time rate of change in ring energy during modulation indicates non-linear optical dynamics [74]. Therefore, an accurate carrier-depletion ring modulator model is essential to optimize transmitter circuitry while ring modulator models in [17, 66, 75, 76, 82] did not demonstrate both non-linear electrical dynamics and optical dynamics.

To design and optimize an optical interconnect transceiver circuitry, an accurate co-simulation environment is required for low-power and high-bandwidth operation. Photonic device models developed in Verilog-A provide the advantage of model compatibility with commercial SPICE circuit simulators. This chapter presents a Verilog-A carrier-depletion ring modulator model including non-linear electrical and optical dynamics, which provides a co-simulation environment for optical interconnect systems design. The model is described in Section 1. Section 2 verifies the model by comparisons of measured and co-simulated 25Gb/s eye diagrams with a

AC-coupled high swing 65nm CMOS driver capable of asymmetric equalization circuitry to study the device non-linearity. Section 3 implements PAM4 modulation with carrier-depletion ring modulators showing measured and co-simulated PAM4 modulation results at 32Gb/s and 40Gb/s with a 65nm CMOS PAM4 driver. Finally, Section 4 concludes the chapter.

5.1 Model Description

The structure of the carrier-depletion ring modulator is shown in Fig. 5.1. It consists of a ring resonator with radius of 7.5μm coupled to a rib waveguide of 500nm width, 220nm height, and 90nm slab height, outer p+ and inner n+ type doping with doping level near $2\times10^{18}cm^{-3}$ on approximately 75% the ring waveguide to form p-n junction, respectively, p++ and n++ type doping are utilized for ohmic contact formation, and an integrated heater with 550Ω resistance formed by doping 15% of the ring with n+ type doping [76]. The ring modulator was fabricated at the IME A*STAR Singapore through OpSIS.



(a) (b)

Figure 5.1: (a) Die photo and (b) cross-section view of carrier-depletion ring modulators.

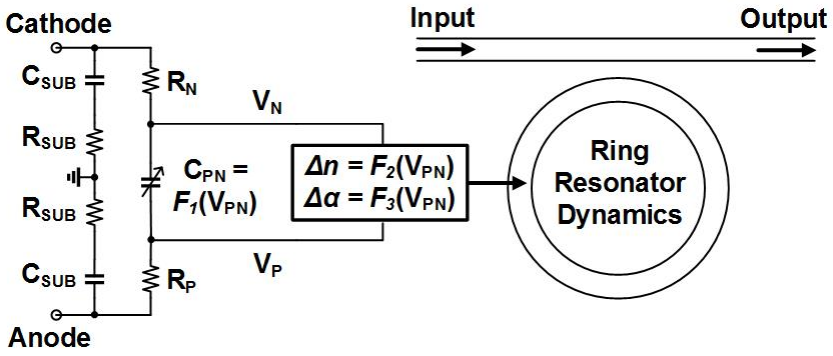
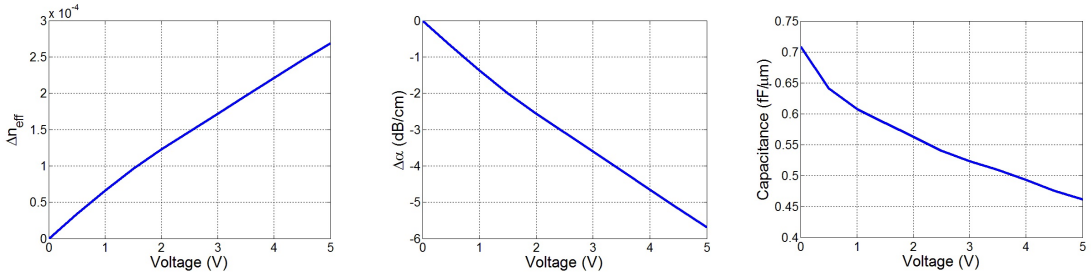


Figure 5.2: Carrier-depletion ring modulator model.



(a) (b) (c)

Figure 5.3: (a) The change in refractive index, (b) the change in absorption coefficient, and (c) the junction capacitance versus applied reverse-bias voltage.

The proposed carrier-depletion ring modulator model is shown in Fig. 5.2. The left side is the equivalent circuit to capture the device's electrical dynamics which is dominantly determined by resistances from the electrodes to the junction region and the junction capacitance. The right side is the dynamic ring resonator model, which is related to the equivalent circuit by functions of refractive index and absorption coefficient changes versus voltage drop on the junction. By fitting S_{11} data of the device, C_{sub} is 2.5fF, R_{sub} is 750-cm, C_{pn} with no bias voltage is 25fF, and R_p and R_n are both 30Ω [59]. Extracting the devices carrier densities versus applied voltage with Lumerical allows calculation of the changes in the refractive index, n, and

absorption coefficient, α, by the plasma dispersion effect [71], which for a λ=1.55μm input wavelength are

$$\Delta n_{1.55\mu m} = -8.8 \times 10^{-22} \Delta n_e - 8.5 \times 10^{-18} (\Delta n_h)^{0.8} \tag{5.1}$$

$$\Delta \alpha_{1.55\mu m} = 8.5 \times 10^{-18} \Delta n_e + 6.0 \times 10^{-18} \Delta n_h \ [cm^{-1}], \tag{5.2}$$

where Δn_e and Δn_h are the electron and hole carrier densities. Fig. 5.3 shows the single phase shifter ring modulator's effective index change, absorption coefficient change, and junction capacitance with applied reverse-bias voltage where $C = \Delta Q / \Delta V$. By curve fitting the Fig. 5.3, the three parameters Δn, $\Delta \alpha$, and C are then extracted as a polynomial function of voltage.

$$f(V) = a_0 + a_1 V + a_2 V^2 + a_3 V^3 + a_4 V^4 \tag{5.3}$$

Table 5.1 gives the a_0-a_4 coefficients, where the valid voltage range is 0-5V.

Table 5.1: Polynomial coefficients of Δn_{eff}, $\Delta \alpha$, and C.

Parameter	Unit	a_0	a_1	a_2	a_3	a_4
Δn_{eff}	-	-4.3×10^{-7}	7.3×10^{-5}	8.0×10^{-6}	1.1×10^{-6}	5.2×10^{-8}
$\Delta \alpha$	dB/cm	0.01	1.5	0.17	-2.3×10^{-2}	1.0×10^{-3}
C	fF/μm	0.71	-0.14	5.5×10^{-2}	-1.2×10^{-2}	1.0×10^{-3}

The dynamic optical output power is related to the changes in refractive index and absorption coefficient by a ring resonator model [74]

$$\frac{\partial A}{\partial t} = \left(2\pi c j \left(\frac{1}{\lambda} - \frac{1}{\lambda_0} \right) - \frac{1}{\tau} \right) A + j\mu S_i \tag{5.4}$$

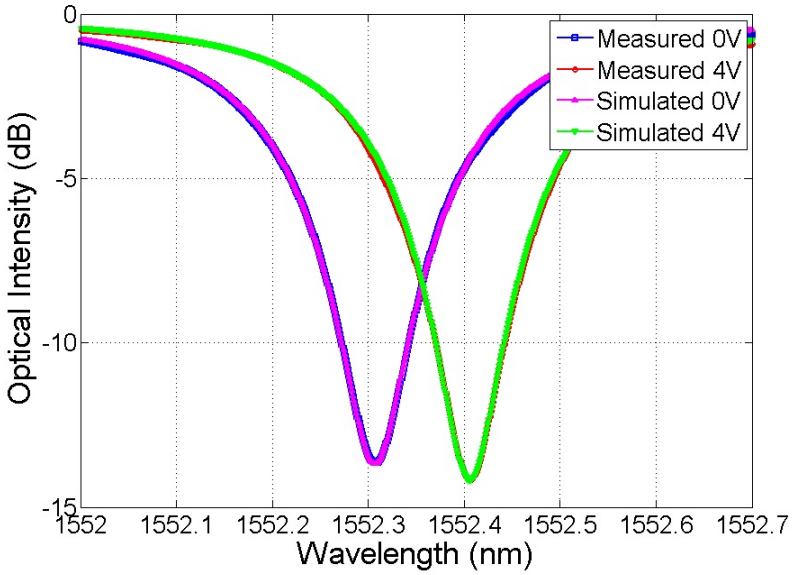


Figure 5.4: Measured and simulated optical spectrum at through port.

$$S_o = S_i + j\mu A, \tag{5.5}$$

where $1/\tau = 1/\tau_c + 1/\tau_l$ is an amplitude decay time constant associated with power coupling to bus waveguide τ_c and power lost due to absorption and scattering τ_l, c is the light velocity, λ is the laser wavelength, λ_0 is the ring resonant wavelength, A is the energy stored in the ring, μ is the mutual coupling between the ring and the bus waveguide, and S_i and S_o are incident and transmitted waves. The coupling factor μ satisfies $\mu^2 = \kappa^2 v_g/2\pi R = 2/\tau_c$, where κ is the coupling ratio, v_g is the ring group velocity, and R is the radius of the ring. The equivalent circuit and ring resonator model are related by

$$2\pi(n_0 + \Delta n)R = m\lambda_0 \tag{5.6}$$

$$\tau_l = 1/[v_g e^{(\alpha_0 + 0.75\Delta\alpha)2\pi R}], \tag{5.7}$$

where the coefficient 0.75 is due to the PN phase shifter effective length, ring effective

index with no bias ∼2.57 and ring group index ∼3.89 are extracted from Lumerical simulation, and the mode number m=28 when R=7.5m and λ=1552.3nm. By fitting the measured optical spectrum at through port applied with reverse bias voltages 0V and 4V shown in Fig. 5.4, three parameters of the model, τ=9.07ps, κ^2=0.0354, and n_0=2.5694, are obtained. The laser wavelength is set to be the resonant wavelength of the ring resonator at 1552.31nm to maximize the extinction ratio (ER) for NRZ modulation.

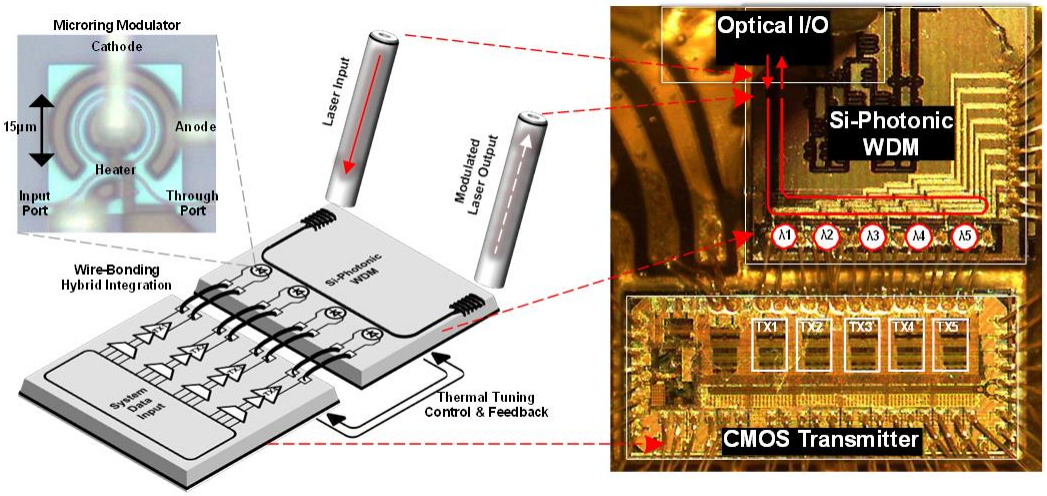


Figure 5.5: Optical transmitter prototype assembly.

5.2 Model Verification

A key objective of the model is to enable an opto-electronic co-simulation environment which allows for both the optimization of transceiver circuitry and the ability to study the impact of optical device parameters. The co-simulation capabilities are demonstrated by comparing measured and co-simulated eye diagrams at 25Gb/s with a custom designed CMOS driver. As shown in hybrid-integrated pro-

totype in Fig. 5.5, the AC-coupled differential driver implemented in a 65nm CMOS technology [20] is wire bonded both to the PCB and the silicon ring modulator for testing. The prototype has the ability to adjust the equalization to optimize high data rate performance.

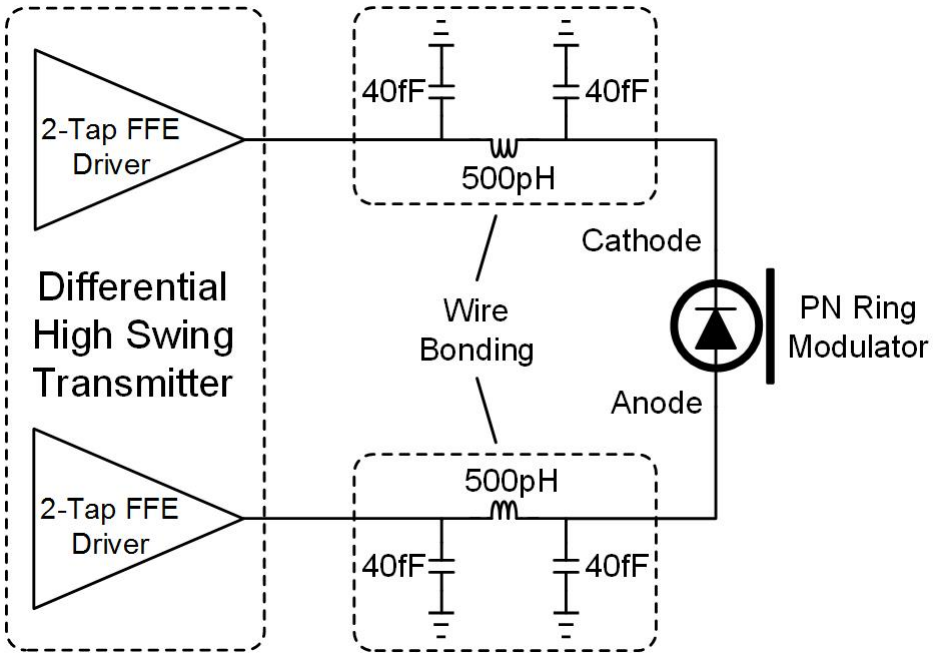


Figure 5.6: Co-simulation schematic with 65nm high-speed differential CMOS driver and carrier-depletion ring resonator modulator model.

Fig. 5.6 shows the co-simulation schematic in a CADENCE environment, with transistor-level schematics for the high-speed differential driver, lumped elements for the wirebond interconnect, and the carrier-depletion ring resonator modulator model. The differential driver provides a high-speed $4.4V_{pp}$ output swing with an asymmetrical feed-forward equalizer (FFE) to compensate the device nonlinearity [20]. 500pH inductors are used to model the ∼0.5mm bondwires that connect the high-speed differential driver to the modulator, while 40fF capacitors model the chips'

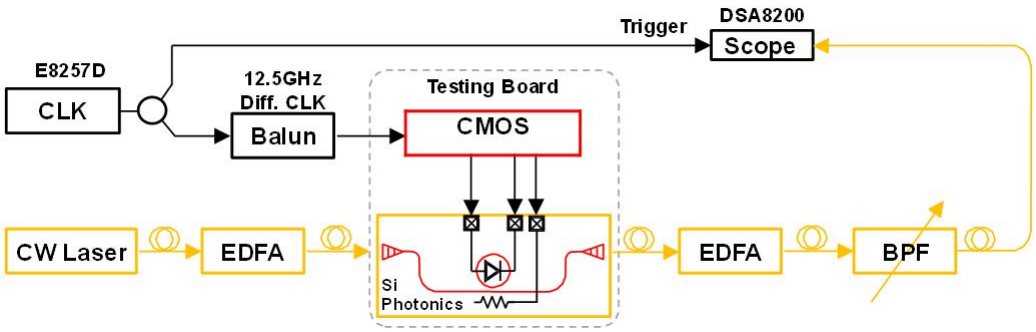


Figure 5.7: Co-simulation schematic with 65nm high-speed differential CMOS driver and carrier-depletion ring resonator modulator model.

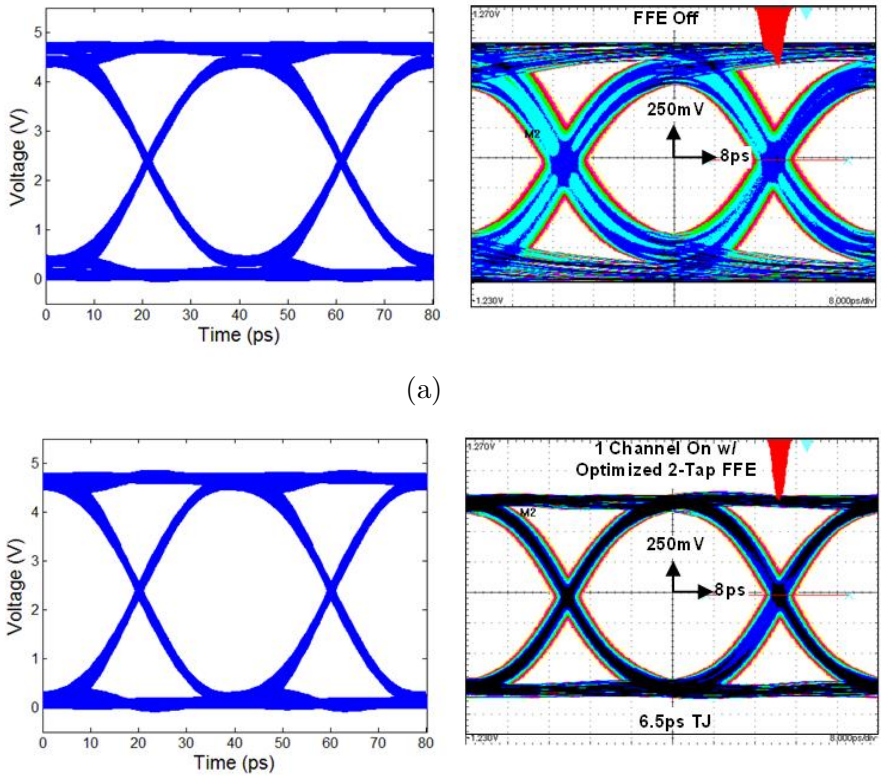


Figure 5.8: Measured and simulated 25Gb/s electrical input eye diagrams (a) without equalization and (a) with optimized symmetric equalization.

bondpads.

25Gb/s measured and co-simulated eye diagrams are compared for model verification. The experimental setup is shown in Fig. 5.7. The optical output from the CW laser is amplified by two erbium doped fiber amplifiers (EDFAs) before and after the photonic chip to compensate input and output insertion losses due to the fiber-to-grating coupler coupling. A bandpass filter is utilized after EDFAs to suppress the amplified noise to increase the signal-to-noise ratio. A clock is utilized for a trigger of an oscilloscope and the input of the CMOS driver. The optical output is received by the oscilloscope.

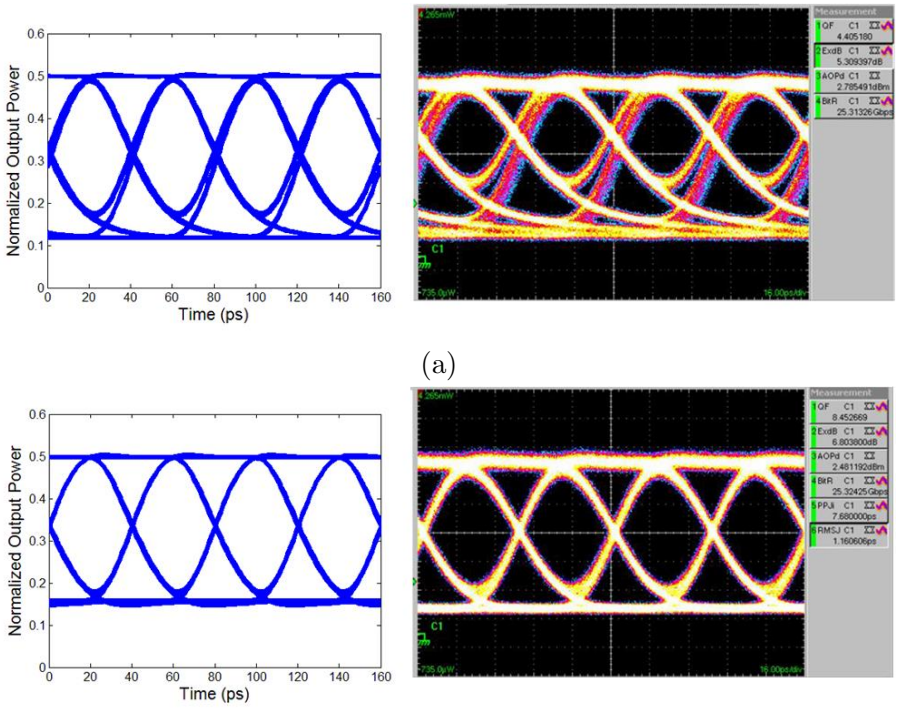


Figure 5.9: Measured and co-simulated 25Gb/s optical output eye diagrams (a) without equalization and (b) with the same optimized asymmetric equalization.

Fig. 5.8 shows the 25Gb/s $2^7 - 1$ PRBS CMOS driver signal for model simulation, which matches excellent with the measured eye diagrams. As shown in Fig. 5.9, excellent matching is achieved between the measured and co-simulated results with and without equalizations. Due to the device bandwidth limitation and nonlinearity, the optical output power is distorted with an unequal amount of inter-symbol-interference (ISI) (Fig. 5.9(a)), which degrades the effective extinction ratio (ER). This asymmetrical ISI are compensated by an optimized nonlinear equalizer (Fig. 5.9(b)).

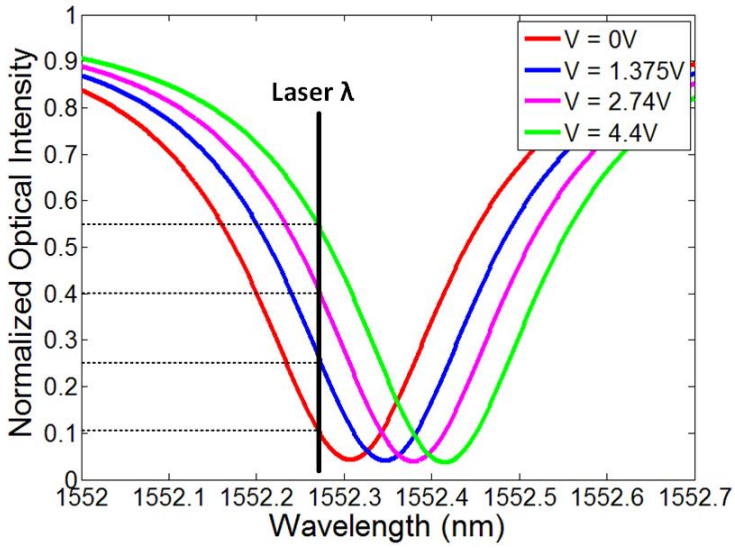


Figure 5.10: Optical transmission spectrum with PAM-4 signaling levels.

5.3 PAM4 Implementation

A straightforward way involves driving a single-segment device with different DAC-generated voltage levels [77]. Ring modulator transmission curves for PAM4 modulation are shown in Fig. 5.10, with a maximum $4.4V_{pp\text{-}diff}$ swing considered due

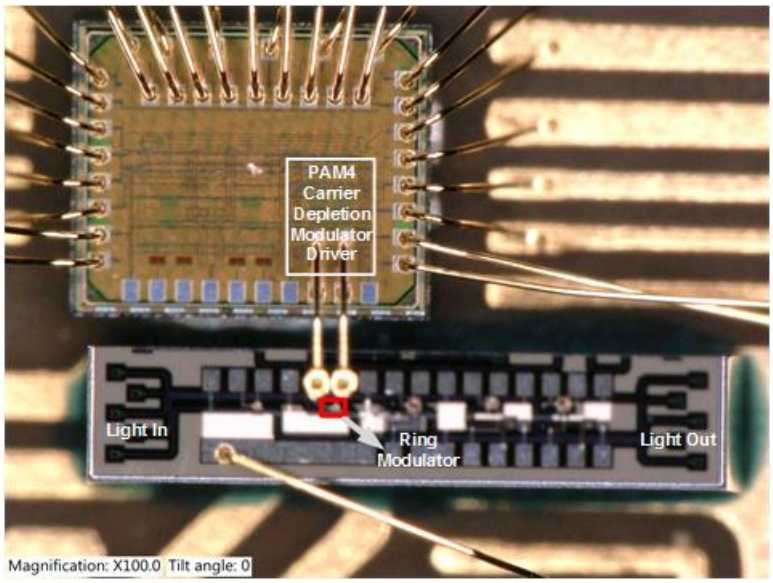


Figure 5.11: PAM4 optical transmitter prototype assembly.

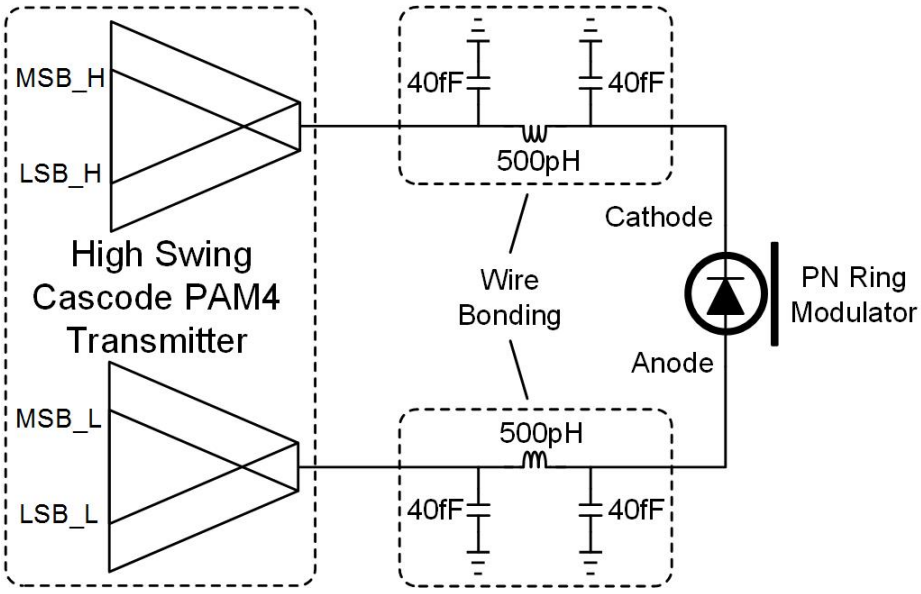
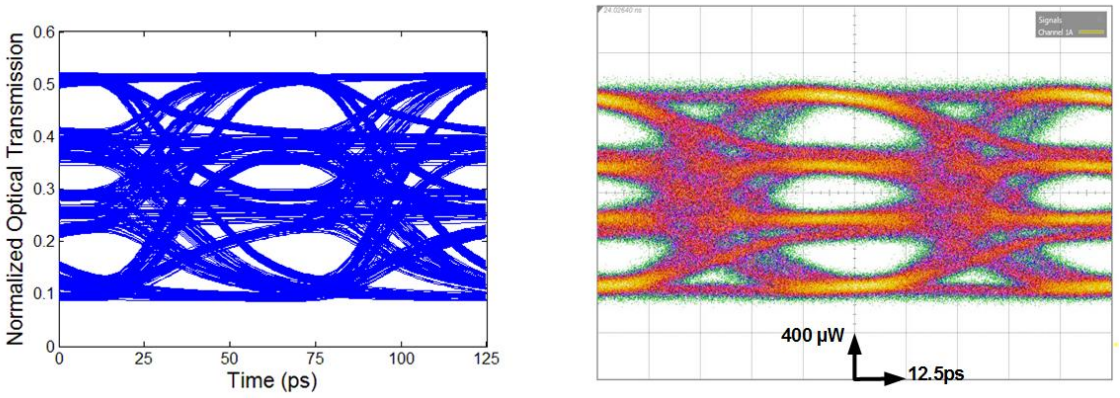
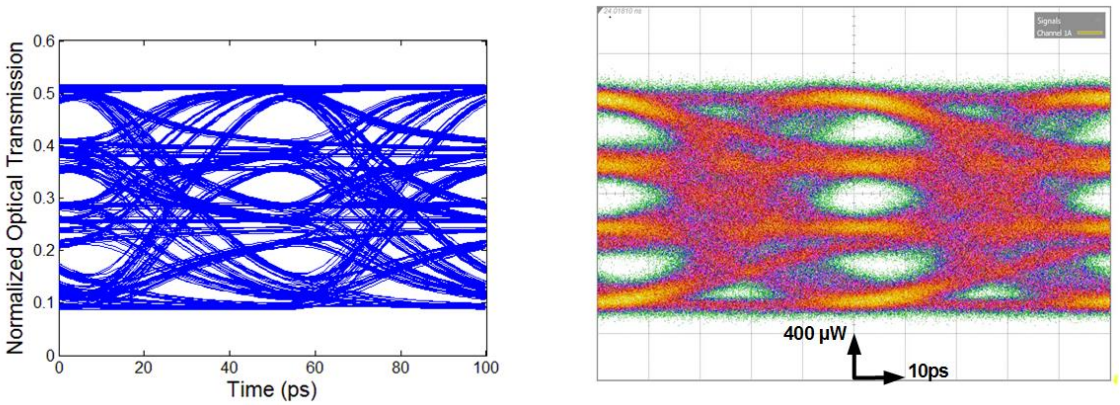


Figure 5.12: Co-simulation schematic with 65nm high-speed PAM4 CMOS driver and carrier-depletion ring resonator modulator model.

to the capacitive voltage division associated with the AC-coupling that maintains reverse-bias operation [20]. The total modulator non-linearity due to the voltage-to-index and index-to-intensity responses must be considered for uniform PAM4 level spacing, with the input laser wavelength slightly offset from the resonant wavelength to optimize the linearity of the optical output response with different bias voltages.



(a)



(b)

Figure 5.13: Measured and co-simulated (a) 32Gb/s and (b) 40Gb/s PAM4 optical eye diagrams.

As shown in hybrid-integrated prototype in Fig. 5.11, the PAM4 driver is wire

bonded both to the PCB and the silicon ring modulator for testing. Fig. 5.12 shows the co-simulation schematic in a CADENCE environment, with transistor-level schematics for the high-speed cascode PAM4 driver, lumped elements for the wirebond interconnect, and the carrier-depletion ring resonator modulator model. The PAM4 driver provides a high-speed $4.4V_{pp}$ output swing and the flexibility to generate the necessary voltage levels with a four-bit voltage divider, which is modified from [20].

As shown in the 32Gb/s and 40Gb/s PAM4 optical eye diagrams of Fig. 5.13, excellent matching is achieved between the measured and co-simulated results. The 40Gb/s eye diagrams are degraded relative to the 32Gb/s eyes due to the transmitter bandwidth limitation, which could be improved by adding pre-emphasis functionality into the driver.

5.4 Summary

Optical interconnect system efficiency is dependent on the ability to optimize the transceiver circuitry for low-power and high-bandwidth operation, motivating accurate co-simulation environments. The presented compact Verilog-A model for carrier-depletion ring resonator modulators includes both non-linear electrical and optical dynamics, allowing for efficient optimization of transmitter signal levels and equalization settings. Excellent matching between simulated and measured optical NRZ and PAM4 eye diagrams is achieved both at 25Gb/s with a 65nm CMOS NRZ driver capable of asymmetric equalization, and at 32Gb/s and 40Gb/s with a 65nm CMOS PAM4 driver flexible of output voltage levels, respectively.

6. RING-RESONATOR-BASED SILICON PHOTONIC LINK MODEL*

Increased data rates have motivated the investigation of advanced modulation schemes, such as four-level pulse-amplitude modulation (PAM4), in optical interconnect systems in order to enable longer transmission distances and operation with reduced circuit bandwidth relative to non-return-to-zero (NRZ) modulation. A straightforward way to implement PAM4 modulation for both MZM and ring resonator modulators involves driving a single-segment device with different DAC-generated voltage levels [77]. Alternatively, reduced transmitter complexity is possible by segmenting the modulator into two MSB and LSB phase shifters of different lengths that are driven by two simple NRZ drivers. This approach was recently demonstrated with a multi-segment silicon-insulator-silicon capacitor MZM operating at 20Gb/s [78], and also shown with a carrier-injection ring modulator which was limited by slow carrier dynamics to 120Mb/s [79].

This chapter analyzes how NRZ and PAM4 modulation impacts the energy efficiency of an optical link architecture based on silicon photonic microring resonator modulators and drop filters, and how this changes as CMOS technology scales from a 65nm to a 16nm node. Section 1 describes models of the NRZ and PAM4 transmitter drivers, receiver front-end circuitry, and high-speed carrier-depletion ring modulators, where PAM4 modulation is analyzed both with single- and two-segment devices. Energy efficiency performance comparisons are made utilizing both 65nm and 16nm CMOS technology nodes in Section 2. Finally, Section 3 concludes the chapter.

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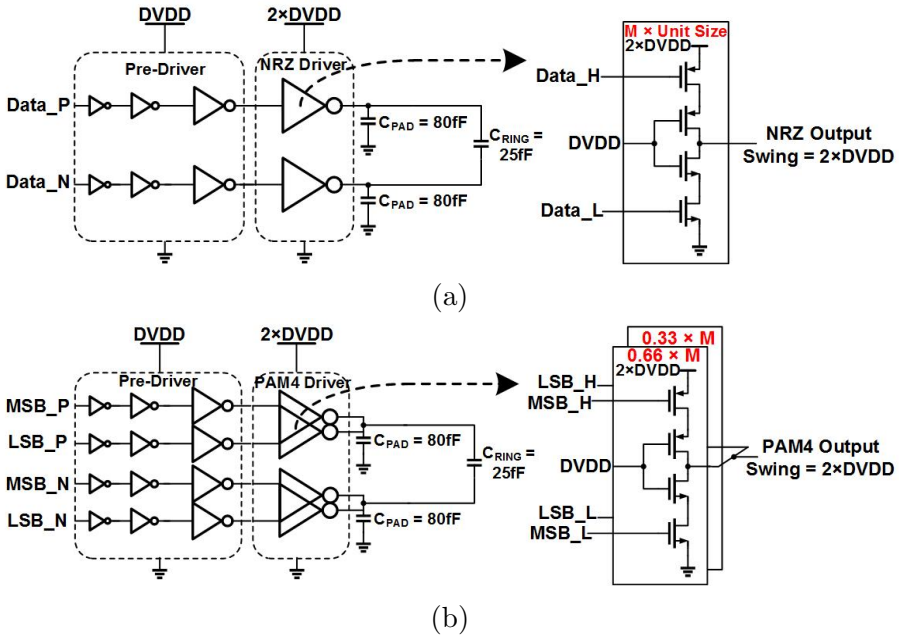


Figure 6.1: Differential high swing ring modulator drivers for (a) NRZ and (b) PAM4 modulation.

6.1 Model Description

6.1.1 Transmitter Drivers

While the depletion-mode ring resonator modulators in this study are capable of 40Gb/s operation [59], due to the low pn-junction tunability they require high modulation voltages to provide >6dB ER. Fig. 6.1(a) shows a differential cascode modulator driver capable of outputting NRZ modulation with $4.8V_{\text{pp-diff}}$ swing when implemented in a 1.2V 65nm CMOS technology [60]. At each side of the differential driver is a cascode output stage powered by a supply that is twice the nominal CMOS supply, allowing a 2.4V swing per modulator terminal in the 65nm node without transistor overstress. Scaling this design to the 0.9V 16nm node results in a $3.6V_{\text{pp-diff}}$ output swing. As shown in Fig. 6.1(b), in order realize PAM4 modulation for a ring modulator with a single phase shifter, this output stage is segmented into

MSB and LSB drivers whose outputs combine to generate the four signal levels. These output stages are driven by pseudo-differential pre-driver inverter chains with a fan-out ratio that is a function of the system data rate. The driver load consists of the ring modulator PN junction capacitance, which is 25fF for a single segment device, and the interconnect capacitance, which is assumed at 80fF with flip-chip bonding integration.

In order to compare how the energy efficiency of the NRZ and PAM4 drivers scale with data rate and technology, the circuit sizing is optimized at each considered data rate. An important parameter is the unit-sized cascode output stage intrinsic bandwidth, which is defined as the Nyquist frequency corresponding to the highest achievable ISI-free NRZ data rate without any load capacitance. This intrinsic bandwidth is 25GHz in the 65 nm node and scales to 40GHz in the 16nm node. For a unit-sized cascode output stage, this can be expressed as a function of its on-resistance R_{Unit} and self-loading capacitance C_{Unit}.

$$BW_{Int} = \frac{1}{\alpha \times R_{Unit} \times C_{Unit}}, \tag{6.1}$$

where α is the correcting coefficient. Including the load capacitance, C_{Load}, the relative output stage sizing factor, M, can be calculated for the Nyquist frequency of the desired data rate, BW_{Driver}.

$$BW_{Driver} = \frac{1}{\alpha \times R_{Unit} \times (M \times C_{Unit} + C_{Load})} \tag{6.2}$$

Then the number of the pre-driver inverter stages can also be calculated for a given

fan-out ratio which changes with data rate.

$$N_{Stages} = \log_{Fanout}\left(\frac{C_{Driver}}{C_{In}}\right) \tag{6.3}$$

The dynamic transmitter power from the output and pre-driver stages is

$$P_{Driver} = 2 \times (C_{Load} + M \times C_{Unit}) \times V_{Driver}^2 \times BW \tag{6.4}$$

$$P_{\mathrm{Pr}e-Driver} = 2 \times C_{\mathrm{Pr}e-Driver} \times V_{\mathrm{Pr}e-Driver}^2 \times BW. \tag{6.5}$$

While this is the total power for the NRZ transmitter, there exists an additional power component in the PAM4 driver due to the output stage short-circuit current present in the generation of the multiple output levels. In this case, which has a 50% occurrence probability, the effective resistance between the output stage supplies is 4.5X the total driver on-resistance and this power component is

$$P_{Short-Current} = 0.5 \times \frac{V_{Driver}^2}{4.5R_{Driver}}. \tag{6.6}$$

6.1.2 Carrier-Depletion Ring Modulators

Fig. 6.2 shows the carrier-depletion ring modulator device structures, which consist of a ring waveguide coupled to a straight waveguide. As shown by the left structure, a conventional ring resonator modulator utilizes a single pn-junction phase shifter in the ring waveguide which is formed by outer p+ and inner n+ doping and additional p++ and n++ regions for ohmic contacts. Splitting this phase shifter into multiple segments allows multi-level modulation with reduced complexity transmitter drivers, as shown by the right PAM4 structure which has longer MSB and shorter LSB segments. As some separation is required between these segments, the PAM4

modulator has about 90% modulation efficiency relative to the single segment design.

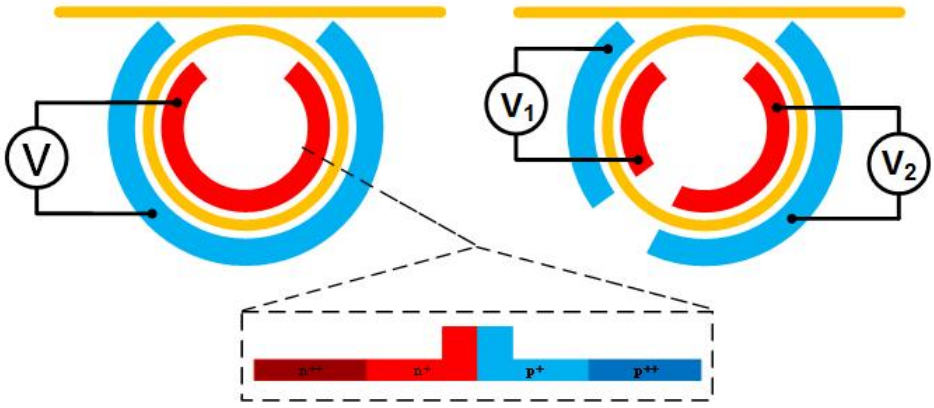
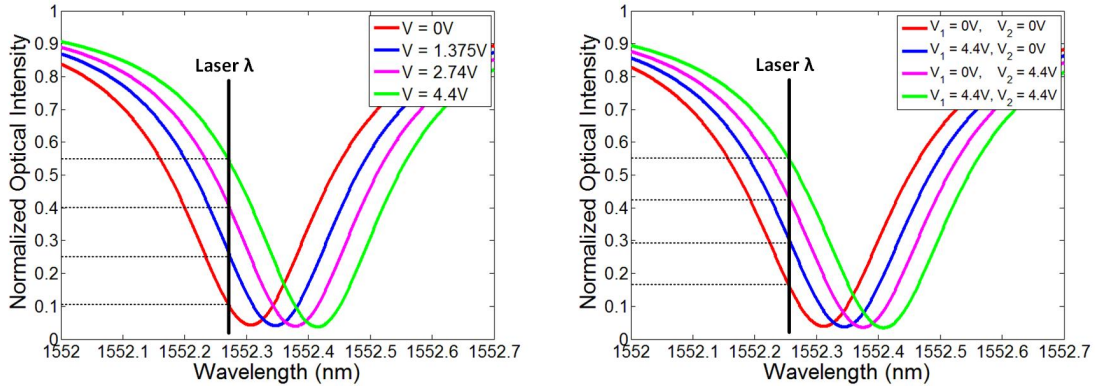


Figure 6.2: Top and cross section views of carrier-depletion ring modulators with a single phase shifter segment (left) and segmented for PAM4 modulation with MSB and LSB phase shifters (right).

The device model was described in Chapter 5. Ring modulator transmission curves are shown in Fig. 6.3, with a maximum $4.4V_{pp\text{-}diff}$ swing considered due



(a) (b)

Figure 6.3: Optical transmission spectrum with PAM-4 signaling levels: (a) one-segment ring modulator and (b) two-segment ring modulator.

to the capacitive voltage division associated with the AC-coupling that maintains reverse-bias operation [60]. The total modulator non-linearity due to the voltage-to-index and index-to-intensity responses must be considered for uniform PAM4 level spacing, with the input laser wavelength optimized separately for the single and two-segment devices. Also, device nonlinearity is compensated for in the two-segment design by adjusting the MSB:LSB length ratio to 1.9:1 from the ideal 2:1 ratio.

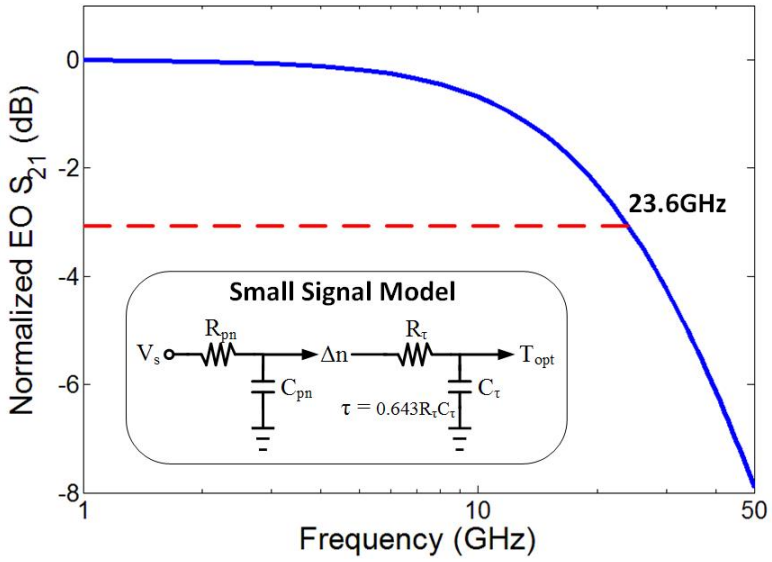


Figure 6.4: Ring modulator electro-optic frequency response.

Fig. 6.4 shows an equivalent small signal circuit used to model the ring modulators electro-optic (EO) bandwidth, which is limited both by electrical parasitics and photon lifetime τ. The dominant electrical parasitics are the 25fF junction capacitance, C_{pn}, and the 60Ω electrode resistance [59]. From [80], the optical bandwidth

due to the photon lifetime is

$$f_\tau = \sqrt{\sqrt{2}-1}\frac{1}{2\pi\tau} = 0.643\frac{1}{2\pi\tau}, \tag{6.7}$$

which can be modelled as a simple first-order RC circuit with $\tau = 0.643 R_\tau C_\tau$. The photon lifetime τ is related to the resonator quality factor Q by $\tau = Q/\omega_0$, where ω_0 is the optical frequency and Q=5000 for the modelled ring resonators. Considering both electrical and optical bandwidth limitations, the total EO bandwidth is 23.6 GHz.

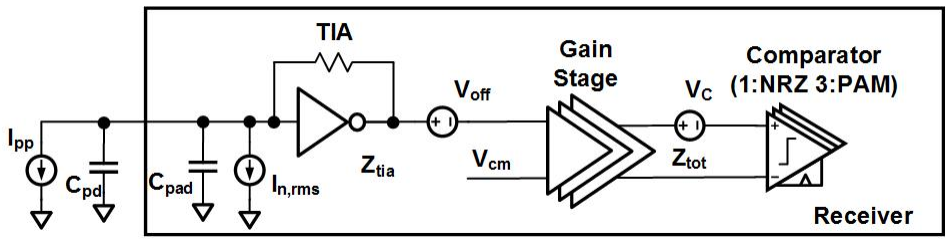


Figure 6.5: Receiver front-end model.

6.1.3 Receiver Front-End

At the receiver side, a waveguide photodetector (PD) converts the modulated optical signal into an electrical current which is amplified by a transimpedance amplifier (TIA) and subsequent gain stages before sampling by comparators to determine the NRZ or PAM4 symbol value (Fig. 6.5). The minimum photocurrent is determined by the circuits input-referred current noise, $I_{n,rms}$, the gain stages offset, V_{off}, and the comparators minimum peak-to-peak voltage for a correct decision, V_C. This minimum comparator voltage consists both of a fixed un-corrected offset and a component which scales with data rate due to the finite regeneration gain. Combining

these terms together yields the following minimum photocurrent for a BER=10^{-12}.

$$I_{in}^{pp} = 14 \times I_{n,rms} + \frac{V_{off}}{Z_{tia}} + \frac{V_C}{Z_{tot}} \tag{6.8}$$

$$I_{n,rms} = \sqrt{I_{tia,rms}^2 + \left(\frac{V_{post,rms}}{Z_{tia}}\right)^2 + \left(\frac{V_{c,rms}}{Z_{tot}}\right)^2} \tag{6.9}$$

In the subsequent modeling results, 5mV$_{pp}$ is assumed for both the gain stage and comparator offsets, while SPICE simulations are used to extract the input referred noise and minimum comparator voltage at a given data rate. The photodetector is modeled with a responsivity of 0.7A/W, while 80fF is assumed for the total PD and interconnect capacitance.

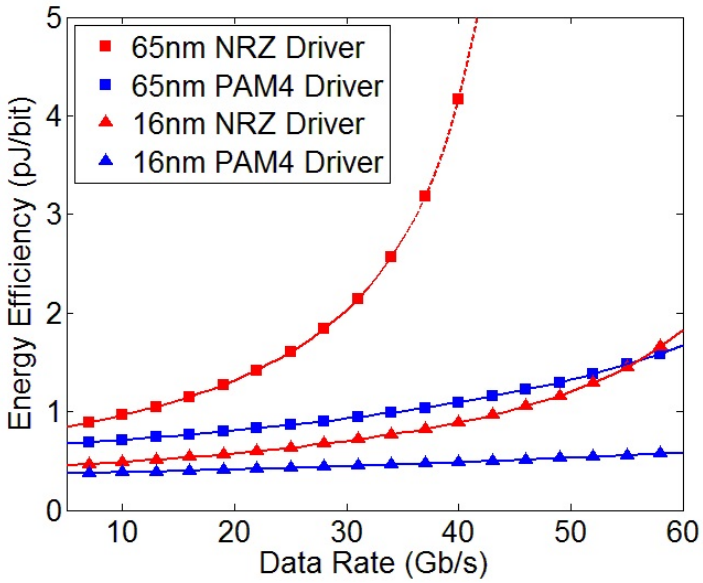
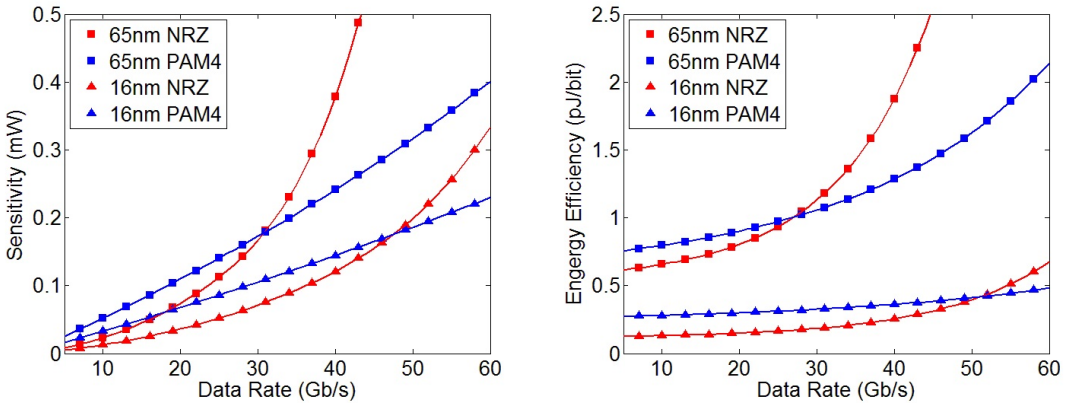


Figure 6.6: Transmitter energy efficiency.

6.2 Photonic Link Results

6.2.1 Transmitter Analysis

Fig. 6.6 shows the calculated transmitter energy efficiency versus data rate with output swings of $4.8V_{pp\text{-}diff}$ and $3.6V_{pp\text{-}diff}$ for the 65nm and 16nm implementations, respectively. The NRZ driver energy efficiency degrades significantly beyond 35Gb/s in the 65nm node due to the relatively high symbol rate causing dramatic increases in output stage sizing and low pre-driver fan-out, while scaling to 16nm allows sub 2pJ/b operation up to 60Gb/s. Relaxing the symbol rate by a factor of two with PAM4 modulation allows for improved energy efficiency and the support of 60Gb/s in the 65nm node.



(a) (b)

Figure 6.7: Receiver (a) OMA sensitivity and (b) energy efficiency.

6.2.2 Receiver Analysis

At the receiver side, in comparing NRZ and PAM4 modulation there are trade-offs in circuit bandwidth, sensitivity, and hardware complexity. As shown in Fig.

6.7, at lower data rates the NRZ receiver displays both superior OMA sensitivity, due to the effective PAM4 eyes being reduced by 3X, and energy efficiency due to the PAM4 receivers increased comparator count. As the data rate increases to a significant fraction of the technologys fT both the NRZ sensitivity and energy efficiency rapidly degrade as the 2X bandwidth requirement causes increased input-referred noise due to smaller input-stage feedback resistors and the additional gain stages. The crossover point where the PAM4 receiver achieves superior energy efficiency is 28Gb/s in the 65nm node and scales to 51Gb/s for the higher fT 16nm node.

Table 6.1: Photonic link parameters.

Parameter	Value
Wavelength	1550 nm
Laser Efficiency (Plaser/Pelec)	0.25
PD Responsivity	0.7 A/W
Insertion Loss (3 Grating couplers)	9 dB
Bit Error Rate (BER)	10^{-12}

6.2.3 Photonic Link Analysis

Table 6.1 shows key parameters used in the total photonic link energy efficiency analysis, which includes laser power. Due to reduced voltage swings with CMOS technology scaling, the OMA as a fraction of the input power for NRZ, one-, and two-segment PAM4 are respectively 0.44, 0.15, and 0.13 for the 65nm node, and these scale to 0.33, 0.11, and 0.1 for the 16nm node. Considering all link losses, modulator/circuit bandwidth, and the different load capacitances of the one and two-segment modulators, Fig. 6.8 shows the total link energy efficiency including the laser, driver, and receiver power at different data rates. At lower data rates, the NRZ

link achieves superior energy efficiency due to the increased transmitter OMA. As the data rate increases the rapid degradation in NRZ receiver sensitivity, modulator bandwidth, and circuit power cause the PAM4 link to display better energy efficiency. The crossover where the PAM4 links achieve superior energy efficiency is near 30Gb/s in the 65nm node and scales to 50Gb/s for the higher fT 16nm node. As the energy efficiency of the two PAM4 links is comparable, with the power saved from the two-terminal drivers offset by the extra laser power required from the reduced total phase shifter length, the simplified transmitter design merits future consideration of the two-terminal approach.

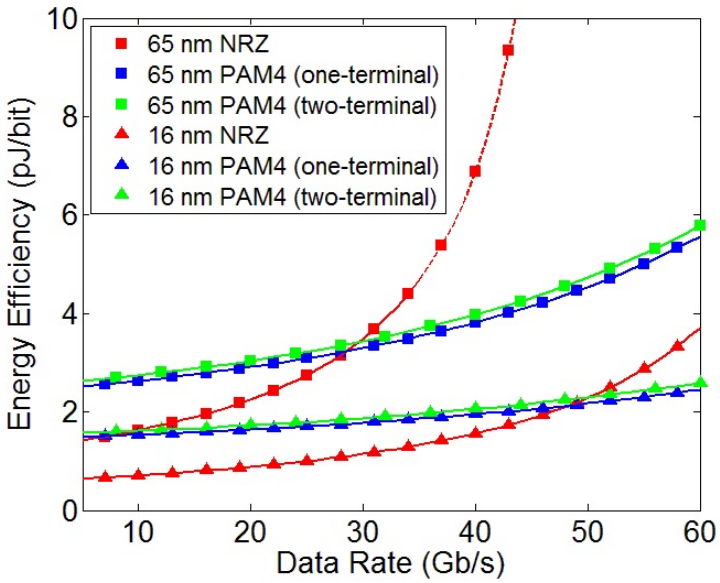


Figure 6.8: Total photonic link energy efficiency.

6.3 Summary

This chapter analyzed how NRZ and PAM4 modulation impacts the energy efficiency of an optical link based on silicon photonic microring resonator modulators and

drop filters. Two PAM4 modulator device structures were proposed, a single-segment device driven with a multi-level transmitter and a two-segment device driven by two NRZ transmitters. Modeling results show that the PAM4 architectures achieve superior energy efficiency at higher data rates due to relaxed circuit bandwidth, with the cross-over point scaling from 30Gb/s in the 65nm node to 50Gb/s in the 16nm node.

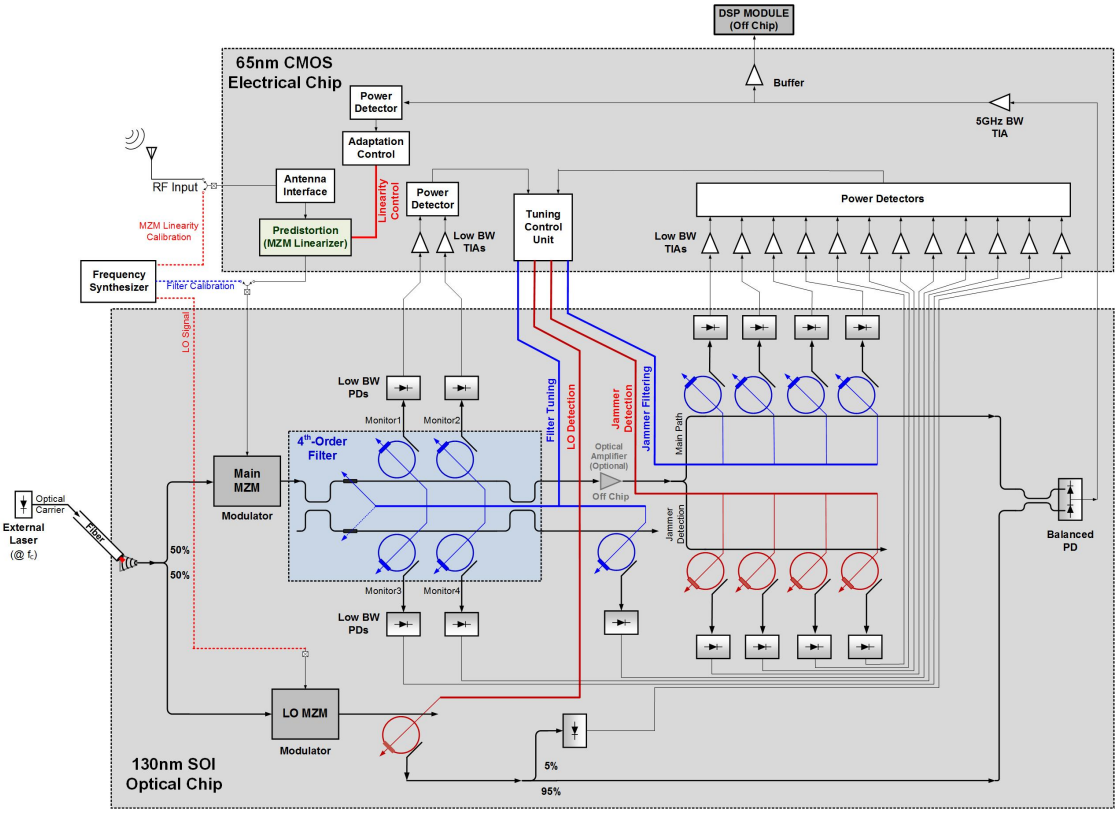


Figure 7.1: Hybrid-integrated silicon photonic RF front-end.

Fig. 7.1 shows the proposed receiver which is designed to operate in a spread-spectrum communication system for inherent security and robustness to jammers [81], given the presence of high-Q filters that are capable of high-speed reconfiguration. Note that this is something that is impossible with conventional electrical filtering over the proposed wideband operation range. As shown in the frequency spectrum diagram of Figure 7.2, the system is capable of receiving a 5GHz spread spectrum signal in any of 5 channels ranging from 32.5GHz to 57.5GHz (25GHz

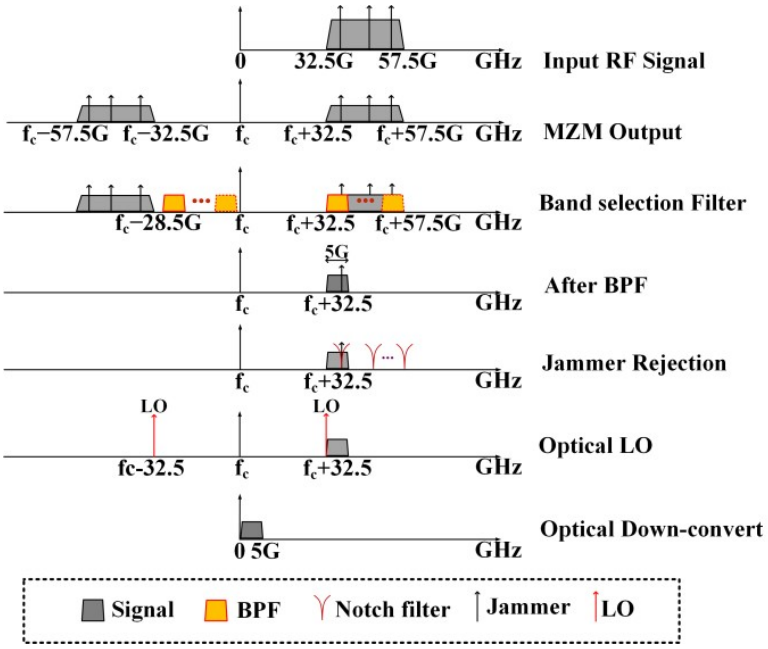


Figure 7.2: Frequency spectrums in the mm-wave silicon photonic receiver with the 5GHz optical BPF centered at 35GHz.

BW). This desired signal, along with potential jammers, is received by a wideband antenna, passed through a broadband matching network, and up-converted to the C-band (1550nm) optical carrier with a MZM. A 5GHz optical bandpass filter with 60GHz FSR follows to serve as both a band selection filter and to reject out-of-band interferers. After this band selection filter, the optical power is split into the main signal path and a parallel spectrum sensing path that allows for continuous jammer detection. Note that in the event of excessive optical path losses, the filtered optical spectrum could pass through an external optical amplifier before this signal splitting. Jammer suppression in the main signal path is realized with a reconfigurable notch filter bank. These jammer suppression notch filters are sequentially activated when the parallel spectrum-sensing path, consisting of swept bandpass filters, detects jammer signals. For each jammer suppression notch filter, fast tuning is achieved with an

automatic tuning loop that monitors the filter drop-port power, via a waveguide PD and low-bandwidth TIA, and employs digital control to adjust a current DAC to place the notch filter at the jammer frequency. Both O-E conversion and down-conversion to the 5GHz baseband are achieved with a balanced waveguide PD connected with a short wire-bond to an adaptive high-sensitivity/bandwidth TIA on the CMOS chip. In order to perform the baseband down-conversion, the optical carrier is modulated with an LO signal in a parallel path which includes a bandpass filter the passes only the optical LO signal and rejects harmonics generated by MZM nonlinearity. Significant power savings are realized with this photonic down-conversion, as this allows for a highly-sensitive power-efficient 5GHz CMOS TIA to process these 32.5GHz to 57.5GHz signals. In order to make the design of Hybrid-integrated silicon photonic RF front-end efficient, a photonic IC modeling in Verilog-A is necessary to allow for the co-simulation of hybrid-integrated CMOS and photonic circuitry.

7.1 Modeling Methodology

In order to accurately achieve optical signals in simulation, photonic device models should be bi-directional and wavelength dependent, and capture both amplitude and phase information. Currently, the polarization of light has not been considered, but parameters in the models can be changed to match device performances with TE or TM mode. The electric field of a light vector is described by [82]

$$\overrightarrow{E}(t) = E_F(t)\, e^{j\phi_F(t)} e^{-j\omega_0 t} + E_B(t)\, e^{j\phi_B(t)} e^{j\omega_0 t} \tag{7.1}$$

where $E(t)$ is the time varying amplitude and $\phi(t)$ is the time varying phase of the forward or backward propagating electromagnetic wave, and $e^{j\omega_0 t}$ is the carrier frequency of the light. Because of the THz frequency of light, the simulator has to use extremely small time steps to catch the oscillations. To remove THz frequency

oscillations but still be wavelength dependence, the electric field of light is given by [82]

$$\overrightarrow{E}(t) = E_F(t)\, e^{j\phi_F(t)} e^{-j\Delta\omega t} + E_B(t)\, e^{j\phi_B(t)} e^{j\Delta\omega t} \tag{7.2}$$

where $\Delta\omega$ is the frequency offset from the carrier frequency ω_0. Generally, the frequency offset $\Delta\omega$ will not be larger than one FSR of a ring resonator ($\Delta\omega << \omega_0$) for simulation of WDM systems or RF photonic receivers.

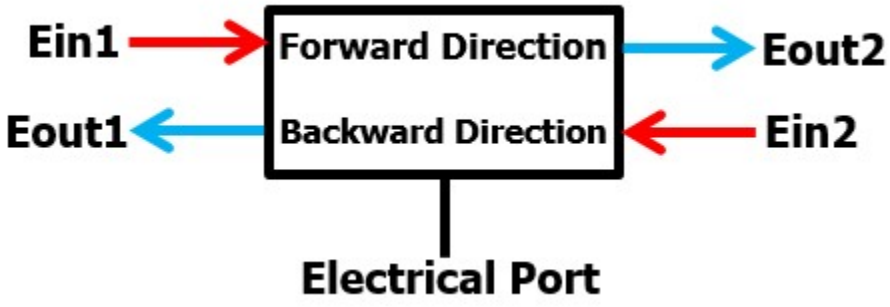


Figure 7.3: Generic photonic device block.

The silicon photonic device compact models are implemented in Verilog-A. Fig. 7.3 shows a generic photonic device block where two inputs and two outputs are related by

$$\begin{pmatrix} Eout1 \\ Eout2 \end{pmatrix} = \begin{pmatrix} P11 & P12 \\ P21 & P22 \end{pmatrix} \begin{pmatrix} Ein1 \\ Ein2 \end{pmatrix} \tag{7.3}$$

where $P_{ij} = f(\lambda, L, n, V, I, T, etc)$ are functions of one or several parameters. Unfortunately, Verilog-A does not support complex numbers. Thus, a complex number is

treated as a real part and an imaginary part where the Equation 7.3 is extended to

$$\begin{pmatrix} Eout1\_re \\ Eout1\_im \\ Eout2\_re \\ Eout2\_im \end{pmatrix} = \begin{pmatrix} P11\_re & -P11\_im & P12\_re & -P12\_im \\ P11\_im & P11\_re & P12\_im & P12\_re \\ P21\_re & -P21\_im & P22\_re & -P22\_im \\ P21\_im & P21\_re & P22\_im & P22\_re \end{pmatrix} \begin{pmatrix} Ein1\_re \\ Ein1\_im \\ Ein2\_re \\ Ein2\_im \end{pmatrix} \tag{7.4}$$

7.2 Model Description

7.2.1 Modeling Building Blocks

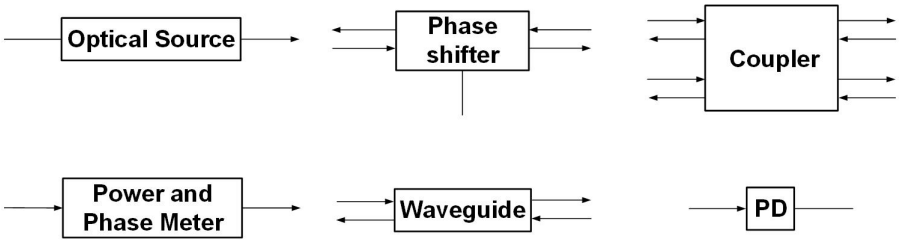


Figure 7.4: Modeling building blocks.

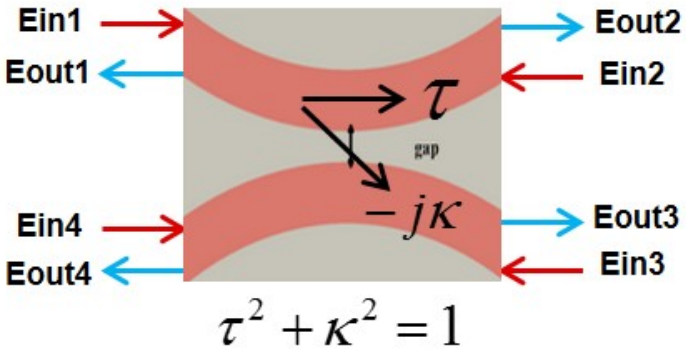


Figure 7.5: 2×2 directional couplers.

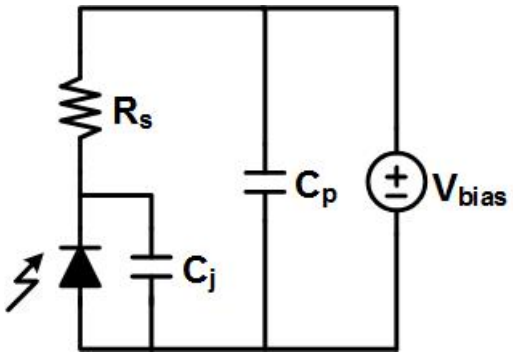


Figure 7.6: Equivalent circuit of photodiodes.

Modeling Building Blocks (Fig. 7.4) are created based on the model methodology respectively. The optical source is described by $P = \eta I$, where η is the slope efficiency. 50/50 1×2 couplers are modeled with $P_{out1} = P_{out2} = 0.5P_{in}$. 2×2 directional couplers(Fig. 7.5) are modeled with

$$\begin{pmatrix} Eout1 \\ Eout2 \\ Eout3 \\ Eout4 \end{pmatrix} = \begin{pmatrix} 0 & \tau & -j\kappa & 0 \\ \tau & 0 & 0 & -j\kappa \\ -j\kappa & 0 & 0 & \tau \\ 0 & -j\kappa & \tau & 0 \end{pmatrix} \begin{pmatrix} Ein1 \\ Ein2 \\ Ein3 \\ Ein4 \end{pmatrix} \tag{7.5}$$

where τ is transmission coefficient and κ is coupling coefficient. The equivalent circuit of photodetectors is shown in Fig. 7.6, where R_s is the series resistor, C_j is the junction capacitor, and C_p is the pad capacitor. The generated photon current is described by

$$I_{photon} = R \cdot P_{opt} - I_s \left(e^{\frac{qV}{KT}} - 1 \right) \tag{7.6}$$

where R is the responsivity of the photodiode, P_{opt} is the optical power, I_s is the saturation current of the diode, and V is the applied bias voltage on photodetectors. From the foundry report, R=0.7A/W and the bandwidth is 20GHz which is domi-

nantly determined by R_s and C_j. The power and phase meter is used to convert real part and imaginary part of the E filed of light to power and phase, which is given by

$$Power = E_{re}^2 + E_{im}^2 \tag{7.7}$$

$$Phase = arctg\,(E_{im}/E_{re}\,) \tag{7.8}$$

The phase shifter model is based on the model of waveguide which is expressed as

$$P_{out} = P_{in}e^{-\alpha L} \tag{7.9}$$

$$\Delta\phi = -\frac{2\pi}{\lambda}\Delta n_{eff}L, \tag{7.10}$$

where Δn_{eff} and α are functions of driving voltages depending on different types of phase shifters.

Carrier-depletion phase shifters modeled in Chapter 5 are implemented in MZ modulators due to the high bandwidth, while thermal phase shifters are implemented in the optical filter due to the low channel loss. Thermal phase shifter model is based on thermo-optic effect which is described by

$$\Delta n = \frac{dn}{dT}\Delta T, \tag{7.11}$$

where Δn is the refractive index change, ΔT is the temperature change, and dn/dT is the thermo-optic coefficient which is $1.86 \times 10^{-4o}C^{-1}$ for silicon. The phase change of the thermal phase shifter is given by

$$\Delta\phi = \beta P_{ele}, \tag{7.12}$$

where β is the thermal tunability coefficient and P_{ele} is the electrical power applied to the thermal phase shifter. The parameter β=0.08792rad/mW at 1550nm from the foundry report is used in the model. The propagation loss of the thermal phase shifter is assumed to be the same as the loss in waveguide due to the negligible introduced extra loss.

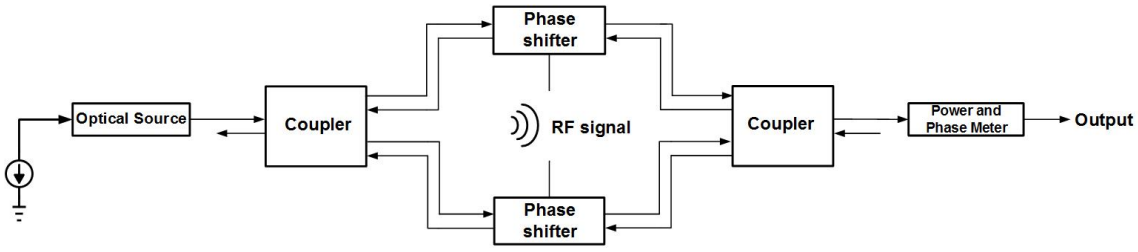


Figure 7.7: Co-simulation schematic of a MZ modulator.

7.2.2 Mach Zehnder Modulator Model

Fig. 7.7 shows co-simulation schematic of a MZ modulator. The output power is expressed as

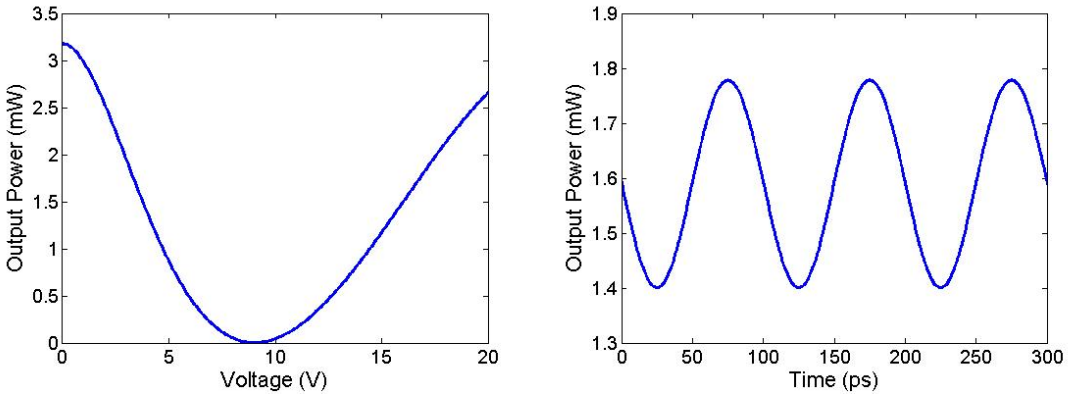
$$T = \frac{1 + \cos(\Delta\phi)}{2} \tag{7.13}$$

with

$$\Delta\phi = \frac{2\pi}{\lambda} \Delta n_{eff}(V) L, \tag{7.14}$$

where $\Delta\phi$ is the phase difference of the two arms, λ is the laser wavelength, Δn_{eff} is the effective refractive index change due to the applied voltage, and L is the length of the MZ modulator. Fig. 7.8 shows co-simulation results when input optical power is 10mW and the length of the phase modulator is 3mm. As shown in Fig. 7.8(a), the insertion loss of the MZ modulator is 5dB and the V_π is 9V. Fig. 7.8(b)

shows a transient response of a 30GHz BW MZ modulator with a $0.1V_{pp}$ 10GHz sinewave differential signal. A small voltage swing signal is essential to reduce the nonlinearity of MZ modulators. However, the voltage swing cannot be too small to achieve a required signal noise ratio (SNR) for RF systems.



(a) (b)

Figure 7.8: Simulated (a) dc and (b) transient responses of the MZ modulator.

7.2.3 4^{th} Order All-Pass-Based Filter Model

Table 7.1 shows the target specifications of the reconfigurable bandpass optical filter, with the FSR designed to allow reconfiguration of the 5GHz passband over the 32.5GHz - 57.5GHz band of interest. In order to achieve 40dB rejection, a 4th-order digital filter design is utilized with a 1550nm optical carrier. As shown in Fig. 7.9, an APF-based implementation generates a complex conjugate response on the top/bottom arms with two 3dB couplers at the beginning/end of the filter and two cascaded ring resonators. In the proposed filter, additional couplers are added to each ring as monitors for the purpose of adaptive tuning. Also, tunable couplers are implemented for the rings and at the end of the filter to compensate

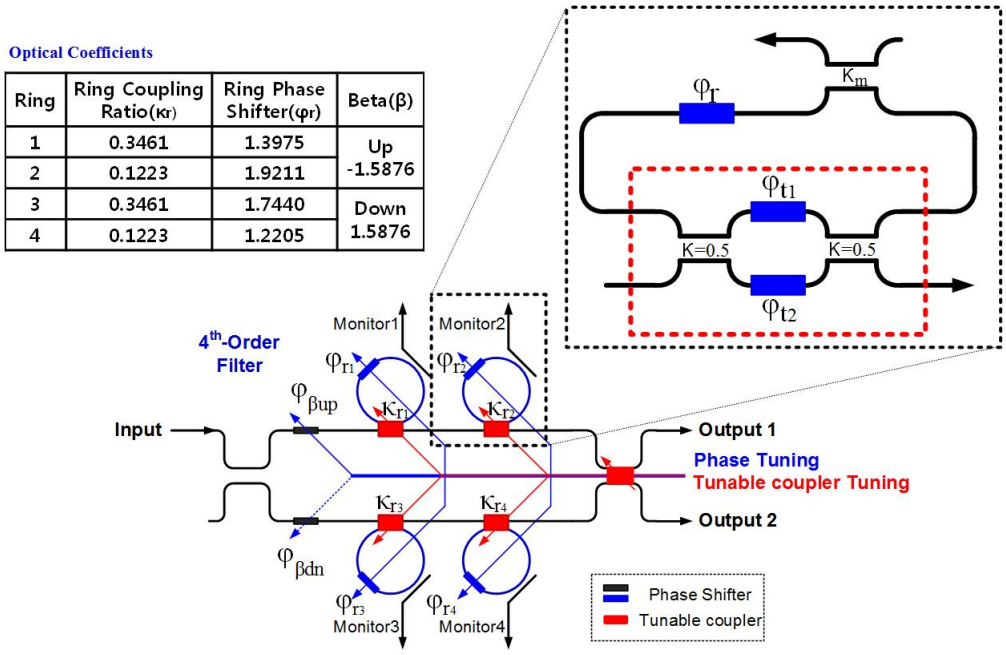


Figure 7.9: 4^{th} order APF-based optical filter schematic and optical element parameters.

for fabrication variations. The desired digital filter transfer function is mapped to the optical components of the APF-based filter based on an all-pass decomposition algorithm [83].

Table 7.1: Optical bandpass filter specifications.

Free Spectral Range (FSR)	60GHz
Pass Band Width	5GHz
Rejection	-40dB
Pass Band Ripple	0.1dB
Filter Order	4^{th} order
Filter Type	Elliptic

The co-simulation schematic of the 4^{th} order APF-based optical filter with tran-

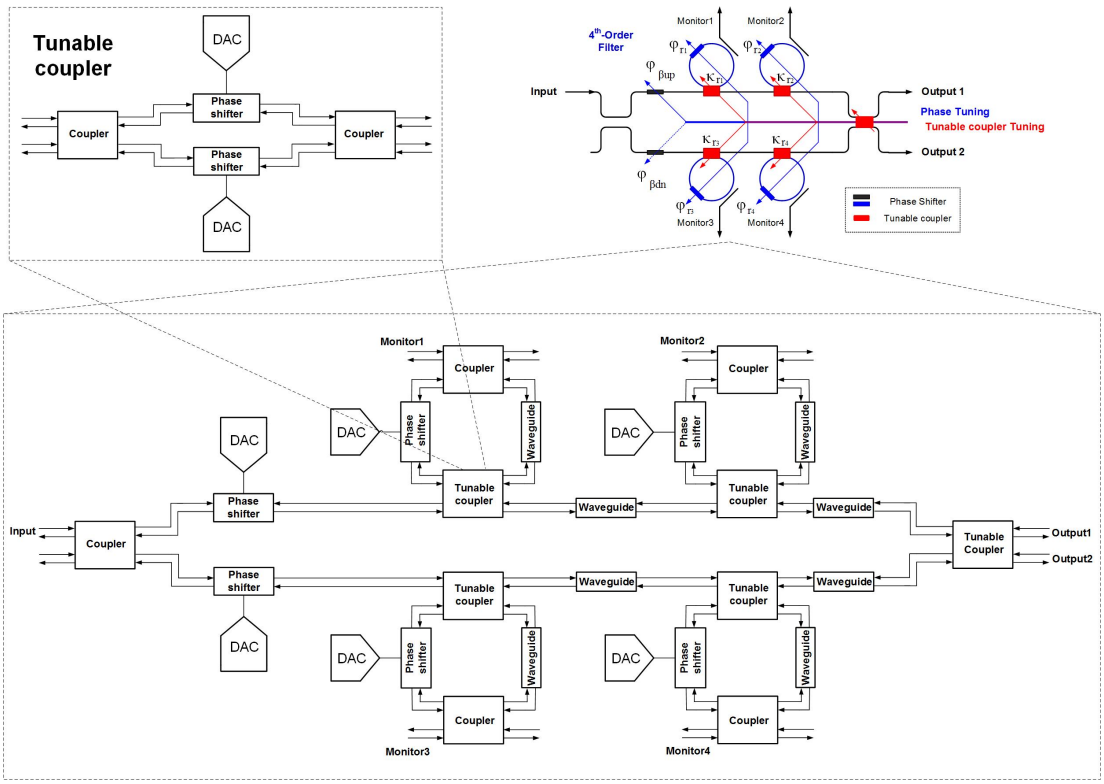
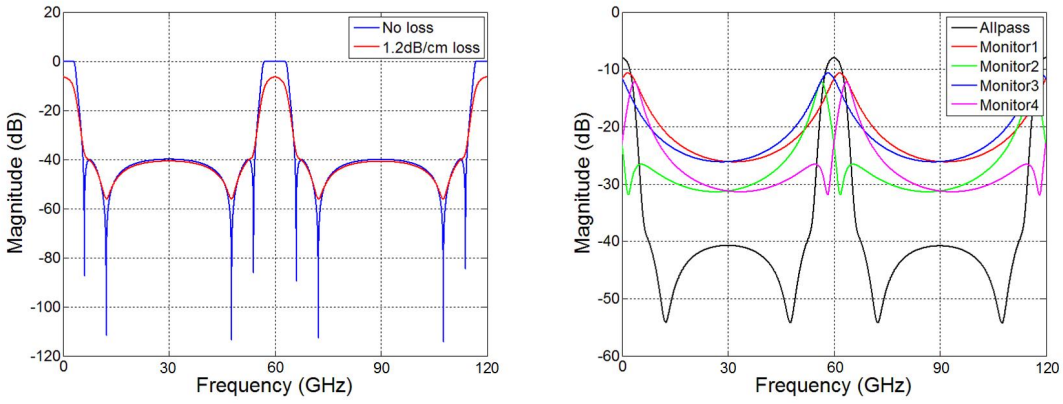


Figure 7.10: Co-simulation schematic of a fourth-order APF-based optical filter modeled in Verilog-A with transistor-level electrical tuning circuitry.

sistor level electrical tuning circuitry is shown in Fig. 7.10. By setting designed parameters in the modeling, frequency spectrums of the 4^{th} order APF-based filter shown in Fig. 7.11(a) without monitors and Fig. 7.11(b) with 5% coupling ratio monitors, respectively.

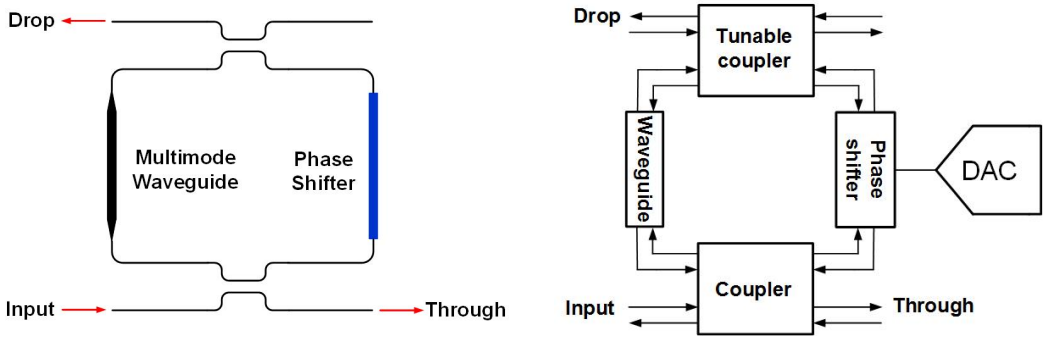
7.2.4 Jammer-Suppression Notch Filter Model

A two-bus optical ring resonator is shown in Fig. 7.12(a), which offers high-Q notch filtering in the optical domain. In order for the ring resonator to serve as a notch filter, the required -3dB bandwidth can be achieved by changing the coupling ratios of the two couplers, and the resonance frequency is changed by adjusting the optical path length of the feedback path via phase shifters. A combination of multi-



(a) (b)

Figure 7.11: Frequency spectrums of the 4$^{\text{th}}$ order APF-based optical filter (a) without monitors (b) with monitors.



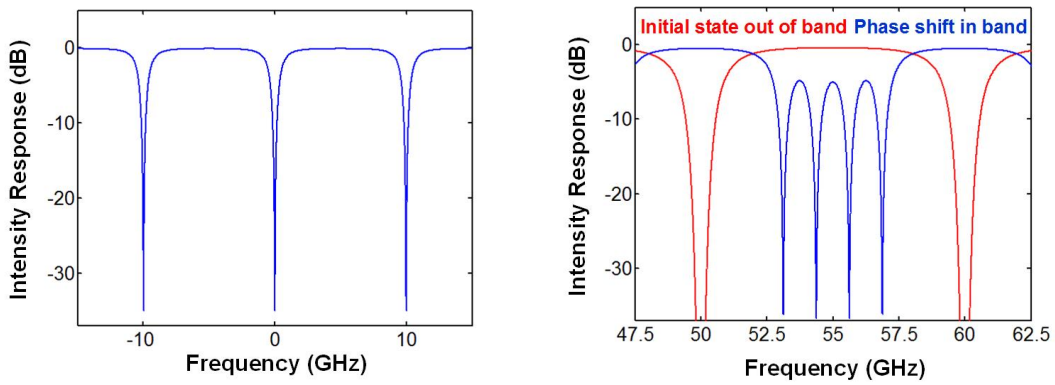
(a) (b)

Figure 7.12: (a) Ring resonator notch filter. (b) Co-simulation schematic of a notch filter modeled in Verilog-A with transistor-level electrical tuning circuitry.

and single-mode waveguides are employed to balance filter loss and area. Utilizing a wider multi-mode waveguide, with adiabatic transitions between waveguides to not excite higher order modes, allows for only 0.4dB/cm propagation loss.

Co-simulation schematic of a notch filter modeled in Verilog-A with transistor-level electrical tuning circuitry is shown in Fig. 7.12(b). As shown in Fig. 7.13(a),

the 10GHz FSR ring resonator notch filters achieve 35dB rejection ratio. If there are no jammers present, the notch filters move out of the band by tuning the ring phase shifters. The worst case signal loss occurs when all notches are in-band to reject four in-band jammers, which results in a pass-band attenuation of 5dB (Fig. 7.13(b)).



(a) (b)

Figure 7.13: (a) Single filter response. (b) Four filters initially tuned out-of-band (red) and tuned in-band (blue) to suppress jammers.

7.3 Summary

Co-simulation environments which allow for the efficient design of Hybrid integrated silicon photonic RF front-end with photonic IC model in Verilog-A are necessary. An optical element modeling framework was proposed in this Chapter for PIC modeling, and the Chapter presented the required modeling building blocks and three component models in the hybrid-integrated silicon photonic RF front-end, MZ modulators, 4^{th} order APF-based optical filters, and jammer-Suppresion Notch Filters.

8. CONCLUSION

Photonic technologies have potential in optical interconnect and RF photonic front-end applications due to the low channel loss and wide-band rapid dynamic tuning. Two commonly used PICs are based on indium phosphide material system and silicon photonics. Either optical link system or RF photonic front-end requires hybrid or monolithic integrated CMOS and PICs. Co-simulation environments for the optimization of CMOS circuitry are necessary to enable efficient design of opto-electronic systems.

Optical interconnect system efficiency is dependent on the ability to optimize the transceiver circuitry for low-power and high-bandwidth operation, motivating accurate co-simulation environments. Modeling of three photonic devices in two modulation techniques, direct modulation of lasers and external modulation of CW laser with modulators, are discussed in Chapter 3-5, respectively. The presented compact comprehensive Verilog-A VCSEL model in Chapter 3 captures thermally-dependent electrical and optical dynamics and provides dc, small signal, and large-signal simulation capabilities. Model parameters are extracted utilizing dc, small-signal electrical and optical responses, and large-signal high-speed optical pulse responses over a set of bias and temperature conditions. Excellent matching between simulated and measured 25Gb/s eye diagrams at different bias currents and substrate temperatures is achieved.

The proposed compact Verilog-A model for carrier-injection ring resonator modulators in Chapter 4 includes both non-linear electrical and optical dynamics, allowing for efficient optimization of transmitter signal levels and pre-emphasis settings. Excellent matching between simulated and measured optical eye diagrams is achieved

both at 8Gb/s with symmetric drive signals with varying amounts of pre-emphasis pulse duration, pulse depth, and dc bias, and at 9Gb/s with a 65nm CMOS driver capable of asymmetric pre-emphasis pulse duration. Modeling results also show the potential for 15Gb/s operation by both optimizing the pre-emphasis waveforms with asymmetric pulse depth and reducing device contact resistance.

The presented compact Verilog-A model for carrier-depletion ring resonator modulators in Chapter 5 includes both non-linear electrical and optical dynamics, allowing for efficient optimization of transmitter signal levels and equalization settings. Excellent matching between simulated and measured optical NRZ and PAM4 eye diagrams is achieved both at 25Gb/s with a 65nm CMOS NRZ driver capable of asymmetric equalization, and at 32Gb/s and 40Gb/s with a 65nm CMOS PAM4 driver flexible of output voltage levels, respectively.

Increased data rates have motivated the investigation of advanced modulation schemes, such as PAM4, in optical interconnect systems in order to enable longer transmission distances and operation with reduced circuit bandwidth relative to NRZ modulation. Chapter 6 analyzes how NRZ and PAM4 modulation impacts the energy efficiency of an optical link based on silicon photonic microring resonator modulators and drop filters. Two PAM4 modulator device structures were proposed, a single-segment device driven with a multi-level transmitter and a two-segment device driven by two NRZ transmitters. Modeling results show that the PAM4 architectures achieve superior energy efficiency at higher data rates due to relaxed circuit bandwidth, with the cross-over point scaling from 30Gb/s in the 65nm node to 50Gb/s in the 16nm node.

While RF photonics offers the promise of chip-scale opto-electrical systems with high levels of functionality, in order to avoid long and unsuccessful design cycles efficient models that allow for co-simulation are necessary. In order to address this,

an optical element modeling framework is proposed based on Verilog-A in Chapter 7 which allows for the co-simulation of optical elements with transistor-level circuits in a CADENCE design environment. The presented modeling building blocks and three component models in the hybrid-integrated silicon photonic RF front-end, MZ modulators, 4^{th} order APF-based optical filters, and jammer-suppression notch filters demonstrate the capability of efficient system design in co-simulation environments.

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