DESIGN OF HIGHLY EFFICIENT ANALOG-TO-DIGITAL CONVERTERS

A Dissertation

by

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ABSTRACT

The demand of higher data rates in communication systems is reflected in the constant evolution of communication standards. LTE-A and WiFi 802.11ac promote the use of carrier aggregation to increase the data rate of a wireless receiver. Recent DTV receivers promote the concept of full band capture to avoid the implementation of complex analog operations such as: filtering, equalization, modulation/demodulation, etc. All these operations can be implemented in a robust manner in the digital domain. Analog-to-Digital Converters (ADCs) are located at the heart of such architectures and require to have larger bandwidths and higher dynamic ranges. However, at higher data rates the power efficiency of ADCs tends to degrade. Moreover, while the scale of channel length in CMOS devices directly benefits the power, speed and area of digital circuits, analog circuits suffer from lower intrinsic gain and higher device mismatch. Thus, it has been difficult to design high-speed ADCs with low-power operation using traditional architectures without relying on increasingly complex digital calibration algorithms.

This research presents three ADCs that introduce novel architectures to relax the specifications of the analog circuits and reduce the complexity of the digital calibration algorithms. A low-pass sigma delta ADC with 15 MHz of bandwidth is introduced. The system uses a low-power 7-bit quantizer from which the four most significant bits are used for the operation of the sigma delta ADC. The remaining three least significant bits are used for the realization of a frequency domain algorithm for quantization noise improvement. The prototype was implemented in 130 nm CMOS technology. For this

prototype, the use of the 7-bit quantizer and algorithm improved the SNDR from 69 dB to 75 dB. The obtained FoM was 145 fJ/conversion-step.

In a second project, the problem of high power consumption demanded from closed loop operational amplifiers operating at Giga hertz frequency is addressed. Especially the dependency of the power consumption to the closed loop gain. This project presents a low-pass sigma delta ADC with 75 MHz bandwidth. The traditional summing amplifier used for excess loop compensation delay is substituted by a summing amplifier with current buffer that decouples the power consumption dependency with the closed loop gain. The prototype was designed in 40 nm CMOS technology achieving 64.9 dB peak SNDR. The operating frequency was 3.2 GHz, the total power consumption was 22 mW and FoM of 106 fJ/conversion-step.

In a third project, the same approach of decoupling the power consumption requirements from the closed loop gain is applied to a pipelined ADC. The traditional capacitive multiplying DAC used in the residual amplifier is substituted by a current mode DAC and a transimpedance amplifier. The prototype was implemented in 40 nm CMOS technology achieving 58 dB peak SNDR and 76 dB SFDR with 200 MHz sampling frequency. The ADC consumes 8.4 mW with a FoM of 64 fJ/Conversion-step.

DEDICATION

To my Parents Jesus and Victoria,

my sisters Gladys and Miriam,

and my fiancée Veronica.

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I. INTRODUCTION

1.1. Motivation

The evolution of communication systems such as cable modems, satellite DTV, cellular radios and fiber optic links motivates performance improvement in analog-to-digital converters (ADCs), wider bandwidth and resolution is required while achieving high power efficiency. Wireless system demand of higher data rates has created the need of ADCs with bandwidths in the hundreds of megahertz range and resolution of more than 10 effective number of bits (ENOB). Fig. 1.1 shows the resolution and speed requirements for different applications. Fig. 1.2 shows the resolution and speed for different types of ADCs architectures.

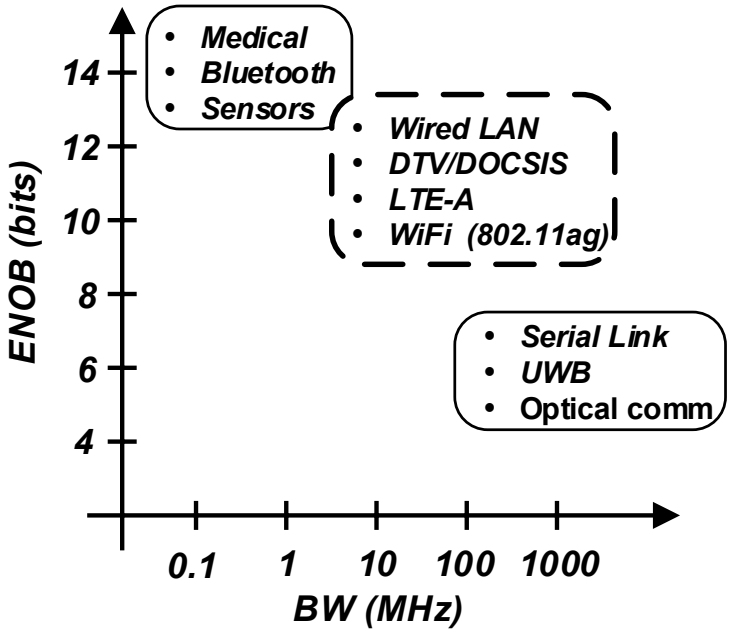


Fig. 1.1: Resolution\bandwidth requirements for different applications.

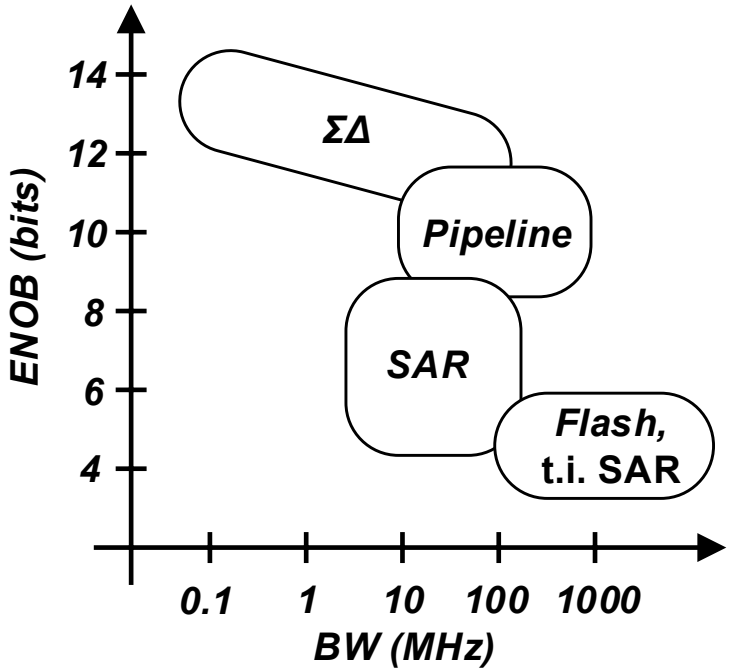


Fig. 1.2: Resolution\bandwidth for different ADCs architectures.

Consumer electronics has been taking advantage of the continuous scale of CMOS technologies, in particular by increasing the amount of digital functionalities that increase with each product's generation. This constant increase of capabilities of digital processors is been seen in the constant evolution of wireless standards, the bandwidth for ADCs and radio frequency (RF) receivers. Therefore, ADC bandwidth for a direct conversion architecture has evolved for applications such as cellphones, from 100 Khz bandwidth for GSM standard, to 10 MHz for first generation long term evolution (LTE) standard. LTE-Advance is the most recent standard for cellphones in which the concept of carrier aggregation has been introduced.

The goal of higher data rates is achieved by processing a maximum of five channels as shown in Fig. 1.3. Therefore, ADCs with bandwidths larger than 50 MHz are required. Likewise, the concept of carrier aggregation is applied in WiFi with the 802.11ac standard, in which ADCs with bandwidths higher than 80 MHz are required. Moreover, applications such as satellite and DOCSIS receivers take fully advantage of the concept of "software defined radio" and use an ADC to digitize the full band spectrum [1] as shown in Fig. 1.4. Full band capture brings the possibility to digitize the channels without the need bring down to baseband frequency. Therefore, multiple analog stages of mixing that add undesired distortion components to the wanted signal and limit the performance of a receiver, are avoided. In addition, complex analog operations such as: channel selection filtering and demodulation, are implemented in a digital signal processor (DSP). The latter has a lower cost and is more robust to process-voltage-and-temperature (PVT) variations.

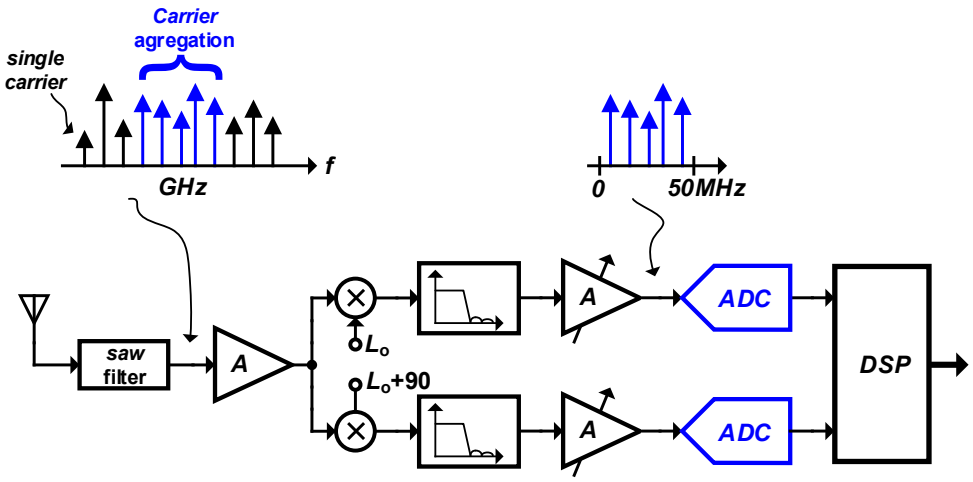


Fig. 1.3: Basic direct conversion receiver for LTE-A.

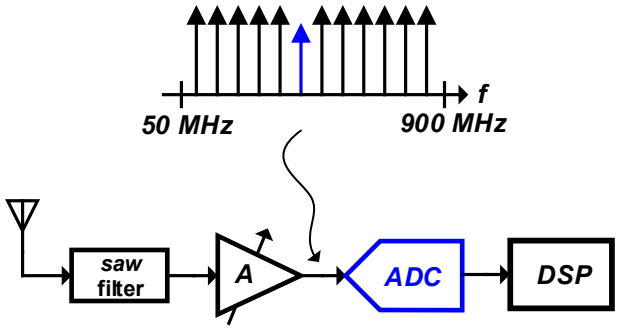


Fig. 1.4: Basic fullband capture receiver for DTV/DOCSIS.

The ADC requirements in a receiver for wireless applications is defined by the standard. The bandwidth of the ADC is defined by the channel bandwidth and the numbers of channels to be processed. The resolution is defined by the expected sensitivity and selectivity. For wireless receiver, the wanted signal normally will be accompanied by other signals commonly known as blockers, which can have larger amplitude that the wanted signal. The standard defines the selectivity of a receiver as desired-to-undesired ratio. For previous wireless standards in which only one channel was digitized, filtering before the ADC was used to reduce the amplitude of the blockers and increase the selectivity. However, for the new standards the ADC needs to process multiple channels in-band demanding high resolution from the ADC. Therefore, demanding high signal-to-noise (SNR) ratio and spurious free dynamic range (SFDR). In addition, high SNR is required by the receiver for proper sensitivity.

Sigma-delta and pipeline ADCs are the architectures that meet the specifications for the receiver of the new generation of wireless standards. Both architectures benefit from scale in process technology. Smaller channel length transistors have less parasitics and provide less delay, therefore higher sampling rate and bandwidth could be achieved. However, the reduced supply voltage in a scaled CMOS technology limits the maximum swing that an OpAmp can achieve. Also, the smaller channel reduces the intrinsic gain of the OpAmp. The lowered headroom due to power supply reduction makes it difficult to use cascode topologies, to boost the OpAmp's gain. Therefore, to design OpAmp's with high gain power consumption is increased and the silicon area increases. For sigma-delta and pipeline ADCs most of the power consumption is included by the OpAmp's.

Technology scaling also suffers from poor matching. To achieve high resolution ADCs, complicated calibration algorithms are required to compensate for the mentioned non-idealities. Although technology scaling helps digital circuitry, the increase in complexity of the algorithms, and increasing sampling frequency of the ADCs, adds significant power, silicon area and latency to the design. Therefore, it is still desired to propose new analog and mixed signal techniques to improve the efficiency of the ADCs with process scaling and minimize the complexity of the digital calibration needed.

1.2. Research contribution

This work addresses the challenges faced by today's ADCs for wireless receivers. The proposed solution focuses on achieving high power efficiency ADCs, particularly focusing in the power consumption of the OpAmp's. Also, the required complexity of digital calibration is reduced with the proposed architectures.

A continuous-time sigma delta modulator (CTΣΔM) using a 7-bit quantizer in conjunction with a fully digital quantization noise reduction algorithm (DQNRA) is presented. This architecture overcomes the signal leakage issues commonly found in cascade and multi-stage noise shaping (MASH) implementations. The DQNRA is robust to PVT variations. Also, a major feature of this approach is that digital matching filters are not required, and the high gain and power required from the OpAmp's in the modulator is relaxed. Moreover, a 7-bit quantizer with a three-step subranging architecture is implemented which minimizes power and area while fully functional at the clock rate. A fourth-order continuous-time ΣΔ with 15 MHz bandwidth was implemented in 130nm CMOS technology. The modulator's total power consumption is 20 mW, with only 6 mW used for the realization of the 7-bit quantizer operating at 500 MHz. The proposed DQNRA algorithm improved the modulator's signal-to-noise and distortion ratio (SNDR) from 69 dB to 75 dB, achieving a figure of merit (FoM) of 145 fJ/conv-step.

Furthermore, one of the main objectives of this research is to alleviate the high power consumption required at high frequencies by OpAmp's with large closed loop gain. The techniques are employed for the design of 75 MHz bandwidth CTΣΔM

fabricated in a standard 40 nm CMOS technology, and clocked at 3.2 GHz. The modulator introduces a 3rd order filter implemented with a lossless integrator and a multiple-feedback single amplifier biquadratic filter (SAB) with an embedded loop stability compensation. An active summing block is implemented employing a common-gate amplifier used as current buffer followed by a transimpedance amplifier. While the closed loop gain of the summing amplifier is still defined by a ratio of resistors, the inclusion of the current buffer avoids the reduction of the feedback gain by the input resistors. Therefore, making it functional for over GHz operation, while consuming low power. The CTΣΔM achieved an SNDR of 64.9 dB over 75 MHz bandwidth while consuming 22.8 mW of power. The obtained FoM is 106 fJ/conv-step.

This research demonstrated that the same concept applied in a ΣΔM can be used in a pipeline ADC. The traditional capacitive multiplying DAC used in the residual amplifier of pipeline, which demands high power consumption and large bandwidth, is substituted by a current mode DAC and a transimpedance amplifier. Moreover, the implemented architecture eliminates the need of complex algorithms, required to compensate the capacitor mismatch need for multi bit multiplying DAC's. The prototype was implemented in 40 nm CMOS technology achieving 58 dB peak SNDR and 76 dB SFDR with 200 MHz sampling frequency. The ADC consumes 8.4 mW with a FoM of 64 fJ/Conversion-step.

1.3. Dissertation organization

This dissertation is organized as follows: Chapter II presents a comparison between Nyquist ADCs and oversampled sigma delta ADCs.. Chapter III describes the design, analysis and results for the sigma delta modulator with 7-bit quantizer. Chapter IV presents the design, analysis and results for the low-power 75 MHz sigma delta modulator. Chapter V portrays the details of the pipeline ADC with proposed current mode stage, including a comparison with a traditional MDAC architecture. Also, the details for the most relevant building blocks are included. Finally, Chapter VI summarizes this research contribution and proposed future work.

II. ANALOG-TO-DIGITAL CONVERTER ARCHITECTURES

2.1. Introduction

There are several major types of ADC architectures that could be used for broadband communications. Each type entails different trade-offs among resolution, speed, power and area. Overall, there are two main categories to classify these ADCs according to the ratio between the sampling frequency and signal bandwidth: Nyquist ADCs and Oversampling ADCs.

2.2. Nyquist ADCs

The difference between Nyquist ADC and oversampled ADC is defined by the ratio between ADC bandwidth and the sampling frequency. In Nyquist ADCs the sampling frequency is twice the value of the maximum input frequency wanted to be digitized as shown in Fig. 2.1.

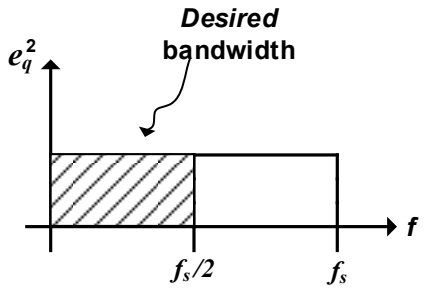


Fig. 2.1: Quantization noise ADC.

There are many different types of Nyquist ADCs that can be used in Fig. 2.2. The three most popular are Flash, successive approximation register (SAR), and pipeline ADCs [2], [3].

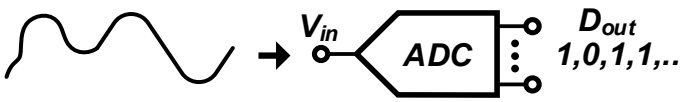


Fig. 2.2: Nyquist ADC.

2.2.1. Flash ADC

A flash ADC uses parallel comparators to compare the input signal against reference voltages, and produces a quantized version of the input signal. The output is obtained in thermometer code, which is typically converted into a binary digital output. Since the comparators operate in parallel, the latency of the output is less than one clock cycle, making this architecture suitable for speeds of several gigahertz. However, a flash ADC suffers from limited resolution, the number of comparators and references required increases exponentially with the number of bits. For an N-bit flash ADC, $2^N - 1$ comparators and reference voltages are required as shown in Fig. 2.3. Also, the offset requirement for the comparators and matching of the references increases exponentially, demanding more area and power consumption making the design of high resolution flash unreliable. The resolution for the flash ADC is 7 bits or less.

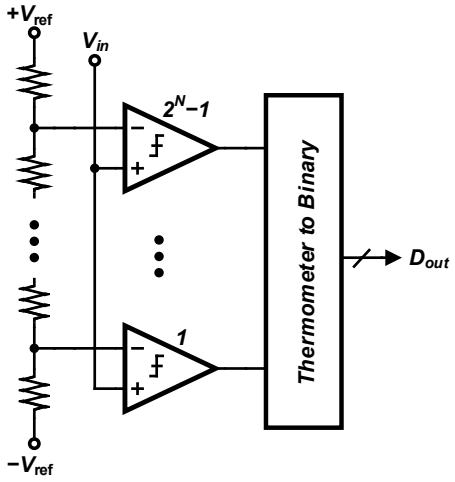


Fig. 2.3: Flash ADC architecture.

2.2.2. SAR ADC

A SAR ADC uses a single comparator to quantize the input signal using binary search. As shown in Fig. 2.4, the ADC consists of a comparator, a SAR digital decision logic, and DAC.

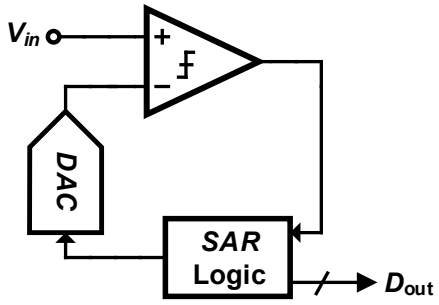


Fig. 2.4: SAR ADC architecture.

The SAR ADC requires multiple clock cycles to complete the digital output. For N-bit SAR ADC, N clock cycles are necessary. Therefore, the SAR ADC is limited to speeds in the tens of MHz. The SAR logic adjust the reference voltage provided the DAC, which defines the resolution of the ADC and is normally implemented by capacitors or resistors. Thus, for high resolution the area of the SAR is dominated by the DAC, which is sized depending on the matching requirements. SAR ADC can achieve resolutions of 14 bits.

2.2.3. Pipeline ADC

A pipeline ADC takes advantage of the speed of a flash ADC, and eliminates the exponential increase in complexity by cascading multiple stages of low resolution flash ADCs. Fig. 2.5 shows that besides the sub ADC, a DAC, a subtractor, and an OpAmp are required for each stage.

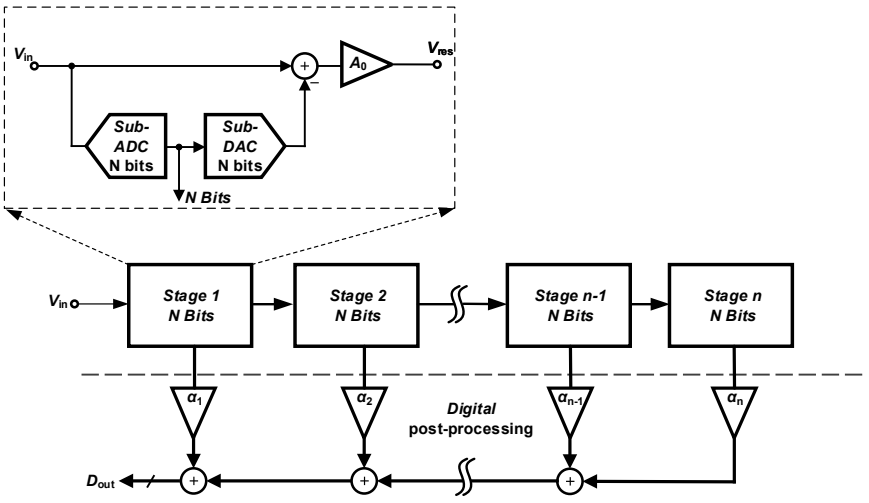


Fig. 2.5: Pipeline ADC architecture.

The operation is described as follow: First, the input signal is quantized by the sub ADC each stage includes a DAC to convert the quantized signal to analog, a residue calculator obtains the difference between the analog input signal and the quantized signal, then the residue is amplified to adjust the swing for the full-scale of the next stage, the amplified residue becomes the input of the next stage. The process is successively replicated until the last pipelined stage. The number stages depends on the number of bits solved per stage, and the total number of bits target. Since all pipelined stages work simultaneously, the conversion speed of the pipeline ADC is high. However, since the input signal is quantized successively by the stages, the output has a latency delay equal to the number of stages. The limitation of the pipeline ADC is the high power consumption required for the calculation of the residue. Pipeline ADCs can reach resolution between 8 bit to 12 bits and speeds on the hundreds of megahertz.

2.3. Oversample ADCs

Any of the previously mentioned architectures could be considered oversampled if the bandwidth of the input signal is less than half the bandwidth of the sampling frequency. However, the only architecture that uses oversampling as one the design specifications is sigma delta ADC.

2.3.1. Sigma delta ADC

A sigma delta ADC achieves high resolution by combining the techniques of: oversampling and closed loop noise shaping. Fig. 2.6 shows the basic architecture of a sigma delta ADC [4]. A sigma-delta consists of a loop filter, a sub ADC, a DAC, and a digital filter.

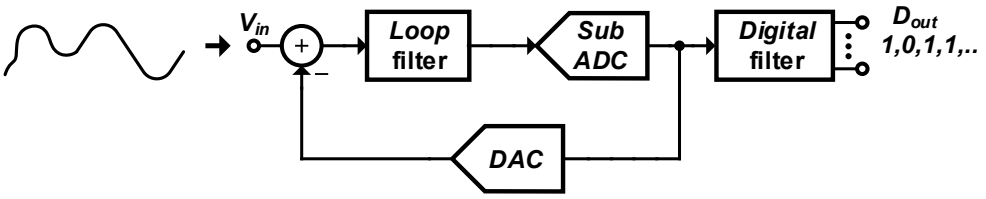


Fig. 2.6: Sigma delta ADC.

The effect of oversampling spreads the quantization from the sub ADC over a wider frequency. Therefore, if the oversampling ratio increases the quantization noise inside the desired bandwidth will reduce as shown in Fig. 2.7a. Moreover, the quantization

noise level inside the desired bandwidth is shaped by the effect of the feedback loop around the sub ADC, such that most of the noise is shifted out of the bandwidth of interest as shown in Fig. 2.7b. The former made the sigma delta ADC a perfect architecture for high resolution applications. However, the speed of the ADC was limited the need of oversample. Nonetheless, advance in process technology has allowed sigma delta ADCs a reach the hundreds of megahertz of bandwidth.

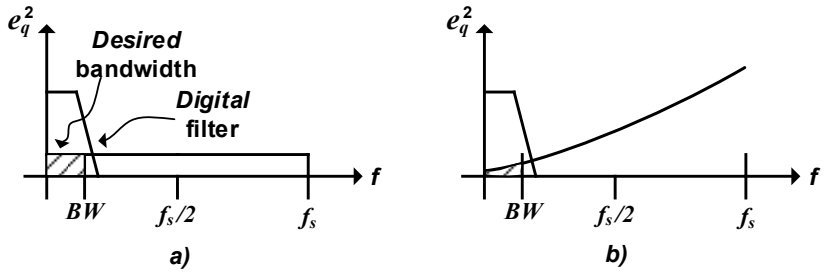


Fig. 2.7: Quantization noise a) oversample ADC, b) sigma delta ADC.

III. A 4-BIT CONTINUOUS-TIME ΣΔ MODULATOR WITH FULLY DIGITAL QUANTIZATION NOISE REDUCTION ALGORITHM EMPLOYING A 7-BIT QUANTIZER

3.1. Introduction

Continuous-time ΣΔ modulators (CTΣΔM) are used in receivers for next generation wireless standards, medical imaging and many other high performance applications. Increase in signal-to-noise ratio (SNR) is required to improve the selectivity in the presence of blockers for a wireless receiver, or to improve the sensitivity for small signal detection in medical imaging. To avoid increasing the loop filter order or sampling frequency of a single loop, cascaded and multi-stage noise shaping (MASH) architectures were implemented [5-7]. These architectures have the issue of noise leakage due to the mismatch of the loop noise transfer function (NTF) and the digitally implemented NTF needed for quantization noise cancellation. By feeding the 2^{nd} loop output to the 1^{st} loop, SMASH architecture [8, 9] avoid this problem at the cost of less aggressive NTF compared with a conventional MASH architecture. Yet, for continuous-time implementation these solutions require a precise analog delay to avoid signal leakage [9, 10].

Operations in the frequency domain are simple and available in receivers for new wireless standards. Fig. 3.1 shows the simplified block diagram of an orthogonal frequency division-multiplexing (OFDM) receiver. After the analog to digital converter (ADC), the spectrum of the signal is obtained through the fast-Fourier transform (FFT)

and then multiple digital operations are performed in the frequency domain. This chapter presents a DQNRA implemented in the frequency domain. Employing a 7-bit quantizer the algorithm is able to precisely extract the actual loop gain after which quantization noise is cancelled employing simple operations. The DQNRA overcomes the shortcomings of previously reported cascaded and MASH implementations; in addition, the methodology is precise and robust against process voltage and temperature (PVT) variations.

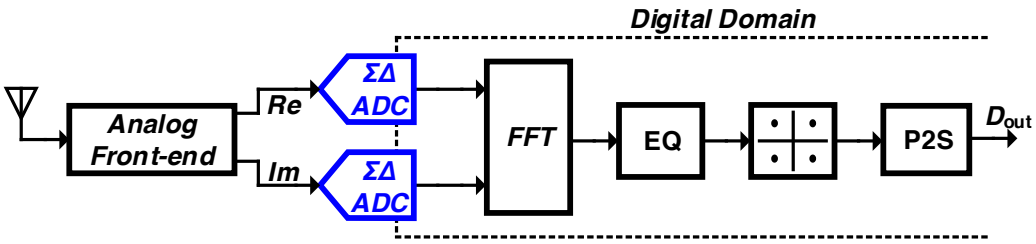


Fig. 3.1: System-on-chip diagram.

The performance of the DQNRA depends on the number of extra bits included in the quantizer. Traditionally, flash quantizer has been the architecture of choice for multi-bit sigma-delta modulators (ΣΔMs). For a good tradeoff between sampling frequency, digital to analog converter (DAC) linearity, loop filter order and complexity, a maximum of 4 bits inside the loop is preferred [11], [12]. In addition, the resources and power required by a flash quantizer grow exponentially with the number of bits; therefore, a flash quantizer with more than 4 bits is for some applications unpractical, especially in a

low-power ΣΔM. A successive approximation register (SAR) ADC can significantly reduce the power consumption of a multi-bit quantizer, but requires N-clock cycles for N-bit conversion. Therefore, the maximum frequency of operation is limited by the need of one clock cycle to resolve each quantizer bit. In recent publications, subranging [13-21] and two-step pipeline architectures [22, 23] have been proposed to address both power consumption and area requirements for flash ADCs and the SAR speed limitations. In this design, the proposed approach combines the advantages of subranging and SAR architectures by reducing the number of comparators from 128 down to 8. The proposed ΣΔ architecture is tested in a CMOS prototype achieving SNDR=75dB while dissipating 20 mW.

The chapter is organized as follows. Subsection 3.2 revisits the cascaded architectures and discusses the issues that limit the performance of cascaded continuous-time implementations. Subsection 3.3 presents the theory behind the proposed DQNRA algorithm. Subsection 3.4 presents the system level implementation of the CTΣΔM and DQNRA. Subsection 3.6 describes the circuit implementation of the CTΣΔM. Subsection 3.7 presents the design details of the 7-bit quantizer. Subsection 3.8 presents the measurement results before and after the algorithm is applied. Finally, subsection 3.9 reports the conclusions and summary of this chapter.

3.2. Background and implementation limitations of cascade CTΣΔM

The cascaded architecture achieves superior SNR without neither increasing the loop filter order nor the operating frequency; the conventional L-0 MASH architecture is shown in Fig. 3.2 [5, 6]. A single loop modulator composed by the loop filter LF_1, quantizer Q_1 and DAC_1 is displayed. For an ideal loop with no delays in the quantizer, the quantization noise E_1 is obtained by subtracting the signal Y_0 and the digital output Y_1 is converted back into an analog by DAC_0. E_1 is then quantized by the high resolution quantizer Q_2. The ideal output, assuming no delays in the quantizer, is given by

$$Y_{OUT} = X \cdot STF_1 \cdot H_1 + E_1 \cdot NTF_1 \cdot H_1 - E_1 \cdot H_2 - E_2 \cdot H_2 \tag{3.1}$$

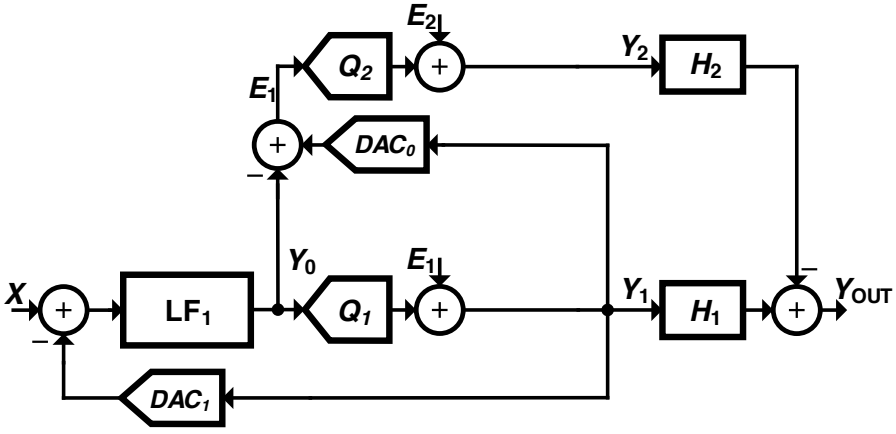


Fig. 3.2: L-0 cascaded (Leslie-Singh) architecture.

where STF_1 and NTF_1 are the signal and noise transfer function, respectively, and E_2 is the quantization noise of Q_2. Digital filters H_1 and H_2 are needed for signal

conditioning. Usually the gain of Q_2 is 1. To facilitate the discussion, let us assume that H_1 is set to 1 as well. According to (3.1), for perfect cancellation of E_1, H_2 must be set equal to NTF_1. Thus, for the ideal case the compensated ADC output is reduced to

$$Y_{OUT} = X \cdot STF_1 - E_2 \cdot NTF_1 \tag{3.2}$$

The resulting in-band Signal-to-Quantization Noise Ratio (SQNR) before and after the compensation is then given by

$$\frac{SQNR_{Yout}}{SQNR_{Y1}} \cong \frac{E_1}{E_2} \tag{3.3}$$

Therefore, $E_2 << E_1$ to get full advantage of this approach.

3.2.1. Cascaded continuous-time implementation limitations

For practical implementations, the noise cancellation is limited by the mismatch between the analog and digital transfer function as well as unavoidable analog and digital timing delays. In fact, PVT variations can make the circuit unreliable for mass production. Fig. 3.3 includes the two main sources of noise leakage in continuous-time cascade architectures.

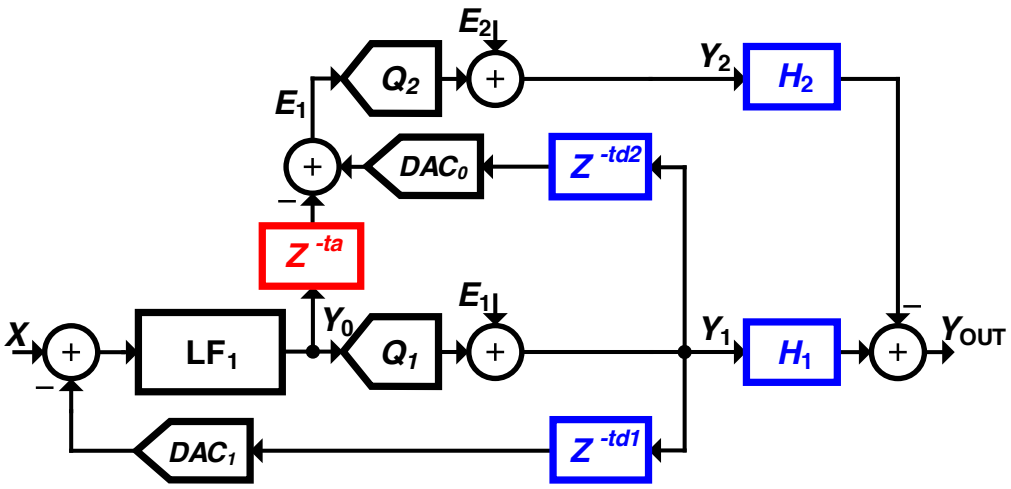


Fig. 3.3: Cascade architecture with limitations.

Because of PVT variations, the analog NTF presents unavoidable tolerances. Therefore, its digital representation H_2 does not match the required transfer function unless NTF is measured and H_2 tuned on chip. The analog NTF after fabrication can be represented as the ideal one multiplied by a factor of $1+\varepsilon_1$; ε_1, which represents the error in the analog NTF due to variations in the passive components, finite OpAmp gain, and DAC coefficient tolerances. A combination of all these variations can produce changes in the analog transfer function of up to ± 30%.

Since $H_2 \neq NTF_1$, a non-cancelled portion of E_1 will appear as leakage at the ADC output Y_{OUT} as $E_1 \cdot NTF \cdot \varepsilon_1$ will then limit the effectiveness of the noise cancelation algorithm. For a cascaded architecture with an ideal SQNR improvement of 18 dB, the effect of noise leakage due to analog *NTF* mismatch is shown in Fig. 3.4. For this plot, each RC product of a continuous-time fourth order loop filter was changed randomly from −10 % to 10 %. The SQNR improvement factor of almost 18 dB with perfect

analog and digital filter matching quickly decays with analog filter variations due to signal and noise leakage.

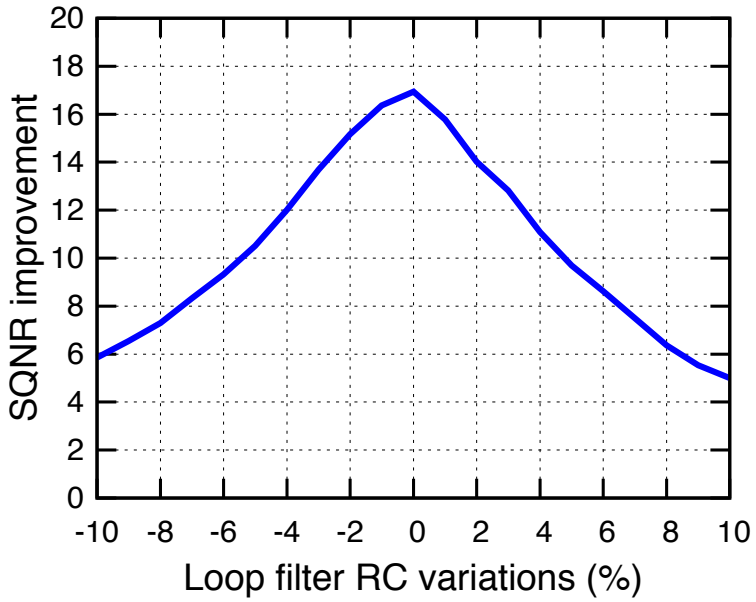


Fig. 3.4: Cascaded SNR degradation due to analog loop filter RC variations.

The second source of error is the improper computation of E_1. As shown in Fig. 3.2, ideally the sampled value of Y_0 will be combined with the digital output of Q_1 reconverted to analog format by DAC_0. As illustrated in Fig. 3.3, the output of Q_1 is not instantaneously processed due to unavoidable delay in the quantizer represented by Z^{-tdi}. The digital circuits inside the quantizer and DAC_0 introduce delay of at least T/2 secs modeled as $Z^{-1/2}$. Since Y_0 is a continuous-time analog signal, an analog delay t_a has to be added to compensate for the digital delay t_{d2} as shown in Fig. 3.3. The analog delay

needs to match with the digital delay ($t_a = t_{d2}$) for best noise cancelation. This becomes a challenge since the analog delay is sensitive to PVT variations. Any timing mismatch leads to a second source of leakage error ($\boldsymbol{\varepsilon_2}$). Although, it does not have a significant impact on the in-band noise floor since it is more relevant at high frequencies, $\boldsymbol{\varepsilon_2}$ might add significant out of band peaking [10]. Further analysis of the architecture including the effect of leakage due to non-idealities leads to

$$Y_{OUT} = X \cdot STF_1 \cdot H_1 + E_1 \cdot (\varepsilon_1 + \varepsilon_2) \cdot NTF_1 - E_2 \cdot H_2 \tag{3.4}$$

If both errors are considered, we should expect even more SQNR degradation than the one shown in Fig. 3.3. The effect of the *NTF* mismatch was already addressed in [8], while delay mismatch effects are discussed in [9] employing an analog RC delay network.

3.3. Digital quantization noise reduction algorithm

The proposed architecture's aim is to overcome all the aforementioned issues. The solution is based on the L-0 MASH architecture; the conceptual diagram is shown in Fig. 3.5. It consists of a CTΣΔM (LF_1, Q_1 and DAC_1) and an open loop quantizer (Q_2). It is assumed that the resolution of Q_2 is better than that of Q_1 and that both quantizers are perfectly matched in time. It will be shown shortly that the number of extra bits in Q_2 defines the SQNR improvement after the algorithm is enforced. The main difference with the traditional L-0 MASH implementation is that Q_2 processes the same information as Q_1 but with more resolution. The two digital output sequences, $y_{1(n)}$ and

$y_{2(n)}$, are decimated to reduce the data points and sampling frequency for further signal processing. The FFT is then used to obtain the frequency spectrums, $Y_{1(\omega)}$ and $Y_{2(\omega)}$. The DQNRA is then implemented in the frequency domain; its description follows.

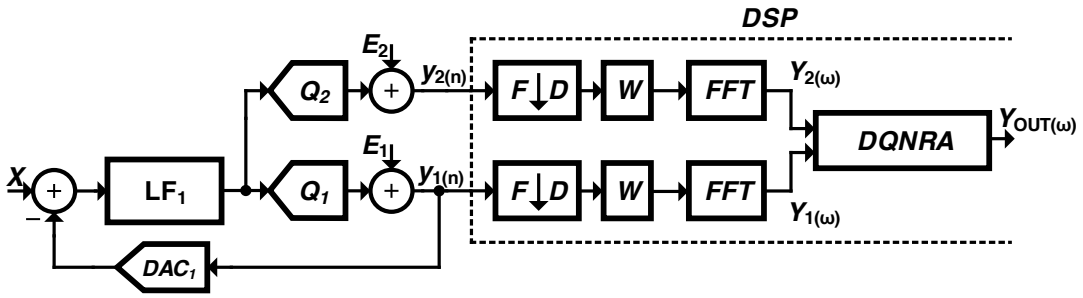


Fig. 3.5: Proposed L-0 DAMASH implementation.

3.3.1. DQNRA

The time domain sampled output of Q_1 and Q_2 are represented by the sequences $y_{1(n)}$ and $y_{2(n)}$, respectively, and can be expressed as

$$y_1(nT) = [x * stf + e_1 * ntf]_{t=nT} \tag{3.5}$$

and $$y_2(nT) = [x * stf + e_1 * (ntf - 1) + e_2]_{t=nT} \tag{3.6}$$

where the symbol (*) represents the convolution operation. Equation (3.5) shows that the output of a conventional modulator is expressed as the convolution of the input *x(t)* and the impulse response of the modulator's signal transfer function; e_1 stands for the quantization noise of Q_1 and it convolves with the impulse response of the NTF.

Assuming that the loop operates in a linear region then we can then apply superposition; that is, in-band e_1*ntf can be measured if the in-band component of $x(t)$ is made zero. Notice that subtracting (3.5) and (3.6) leads to,

$$y_e(nT) = y_2(nT) - y_1(nT) = [e_2 - e_1]_{t=nT} \tag{3.7}$$

In the frequency domain this equation is equivalent to

$$Y_e(\omega) = Y_2(\omega) - Y_1(\omega) = E_2(\omega) - E_1(\omega) \tag{3.8}$$

Equation (3.7) can be easily obtained in the time domain if both quantizers are sampled at the same time, and employ the same type of quantizer. In this case, (3.7) represents the extra LSB's of Q_2 and the subtraction operation is not needed. Merging Q_1 and Q_2 into a single quantizer ensures perfect timing matching among them, making the operations needed in (3.7) reliable and PVT insensitive.

Notice that the NTF can be estimated as follows,

$$NTF_{AD} = \left.\frac{Y_1(\omega)}{Y_e(\omega)}\right|_{X=0} = \left(\frac{E_1}{E_2 - E_1}\right) NTF = \alpha\, NTF \tag{3.9}$$

where NTF_{AD} represents the estimated adaptive noise transfer function, which is proportional to NTF. If $E_1 >> E_2$, NTF_{AD} is closer to the ideal value of the main loop NTF. Let us define the NTF estimation error in (3.9) as,

$$\alpha_{rms} = \left(\frac{{E_1}^2}{{E_1}^2 + {E_2}^2}\right)^{1/2} \tag{3.10}$$

This relationship is determined by the main quantizer noise and the number of extra bits N_{ext} added into Q_2. The quantization noise of, Q_1 and Q_2, are then related by the relationship $|E_1| = |E_2| \cdot 2^{N_{ext}}$; therefore, (3.10) reduces to

$$\alpha_{rms} = \left(\frac{2^{2N_{ext}}}{2^{2N_{ext}} + 1} \right)^{1/2} \tag{3.11}$$

For larger values of N_{ext} α approaches 1 meaning that NTF_{AD} is close to NTF within an error given by 2^{-Next}. Once NTF_{AD} bins are measured, the data is then saved in a digital memory. The new incoming error signal represented by (3.8) is multiplied by the saved NTF_{AD}, and the result will be subtracted from the new output of the modulator $Y_{1(\omega)}$.The DQNRA algorithm is then described as follows. First, $Y_{OUT(\omega)}$ is computed

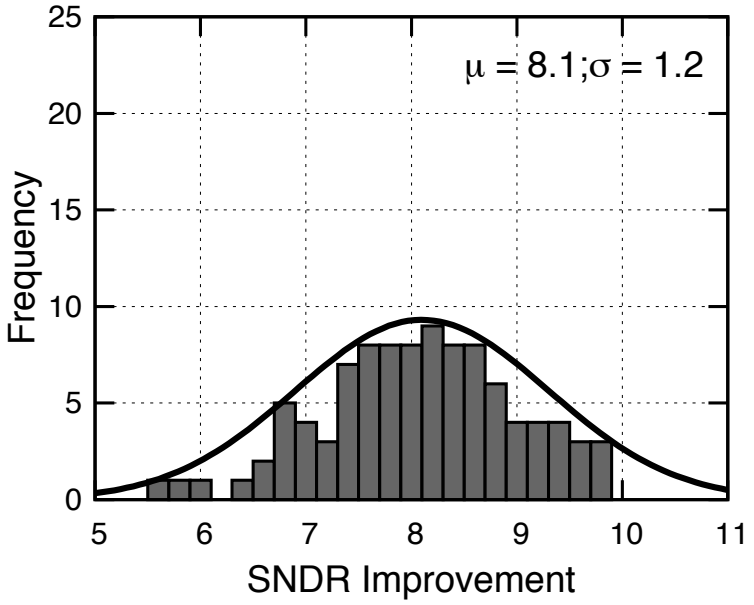
$$\begin{gathered} Y_{OUT}(\omega) = Y_1(\omega) - (Y_e(\omega) \cdot NTF_{AD}) \\ Y_{OUT}(\omega) = X \cdot STF + E_2 \cdot \alpha_{rms} \cdot NTF + E_1 \cdot (1 - \alpha_{rms}) \cdot NTF \end{gathered} \tag{3.12}$$

The DQNRA output consists of three terms. The first term is the desired input signal X, weighted by the signal transfer function. The second term contains E_2, shaped by the in memory noise transfer function NTF_{AD}. The third term contains E_1, which represents the noise leakage; this noise component is shaped by the factor $1 - \alpha_{rms}$. The E_1 attenuation factor is a strong function of the number of extra bits N_{ext}. Since $E_1 \cong E_2 2^{N_{ext}}$, the second and third terms in (3.12) have the same effect on the resulting quantization noise floor. It can be shown that (3.12) can also be expressed as follows

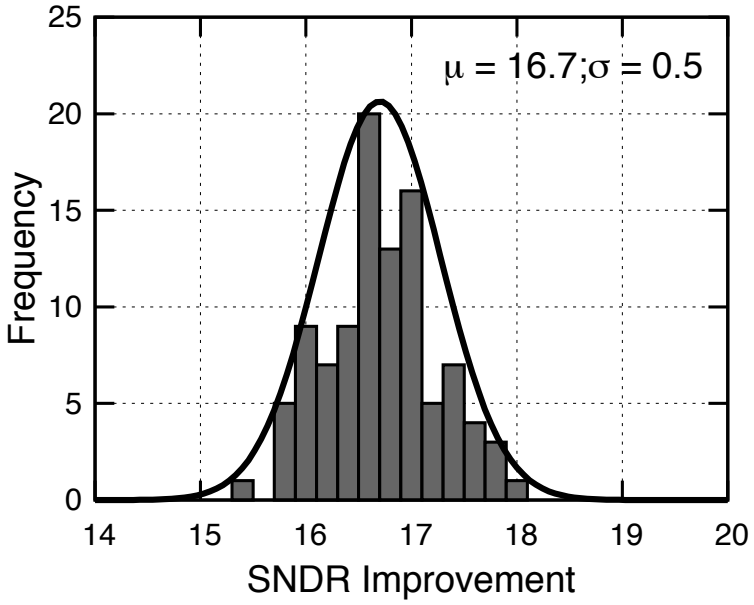
$$Y_{OUT(\omega)} = X \cdot STF + \left\{ E_2 \cdot \left(\frac{2^{2N_{ext}}}{2^{2N_{ext}} + 1} \right)^{1/2} \cdot NTF \right\} + \left\{ E_1 \cdot \left(\frac{1}{2^{2N_{ext}} + 1} \right)^{1/2} \cdot NTF \right\} \tag{3.13}$$

Although we may be tempted to combine the second and third term of these equation (E_1 is approximately equal to $2^{Next}E_2$), we should not do so because they are uncorrelated. The second term comes from Q_1 while the third term is originated in Q_2. According to this result, three extra bits in Q_2 should then result in an SQNR improvement of at least 15 dB. The algorithm is more effective if some additional design issues are considered. If NTF_{AD} is estimated from a single shot, E_1 and E_2 might not capture with enough accuracy the shape of NTF due to glitches or random artifacts. Computing NTF_{AD} and averaging the results allows to have a better estimation of the actual NTF.

Extensive simulations were performed using three extra bits in the second quantizer Q_2. First, an out-of-band tone was used and data was collected to compute NTF_{AD}. Then, a single-tone input signal was applied 100 times with random in-band frequency and amplitude, and the algorithm was applied for post-processing the data. Fig. 3.6a shows the SQNR improvement for the 100 different input signals when NTF_{AD} is computed with a single shot. The mean of SQNR improvement is 8.1 dB with a standard deviation of 1.2 dB. Fig. 3.6b displays the results when NTF_{AD} is computed averaging 20 times the modulator's output before processing the 100 different input signals. The SQNR improvement has a mean of 16.7 dB and a standard deviation of 0.5 dB, which confirms what the theory predicts a minimum benefit on SQNR of 15 dB.



(a)



(b)

Fig. 3.6: SQNR improvement due to the proposed algorithm: a) NTF_{AD} single shot calculation and b) for 20 point averaging NTF_{AD} calculation.

3.4. Realization of the proposed noise calibration algorithm

The realization of the architecture shown in Fig. 3.5 requires two quantizers. A major issue in their practical implementation is the potential magnitude and timing mismatch between them. The implemented solution merges both quantizers into a single 7-bit quantizer as shown in Fig. 3.7. The quantizer's four most significant bits (MSBs) are used in the loop, while the remaining three least significant bits (LSBs) contain the wanted error signal ($E_2 - E_1$). Fig. 3.7 also illustrates the selected system level sigma delta architecture. More details about the architecture are covered in subsection 3.6.

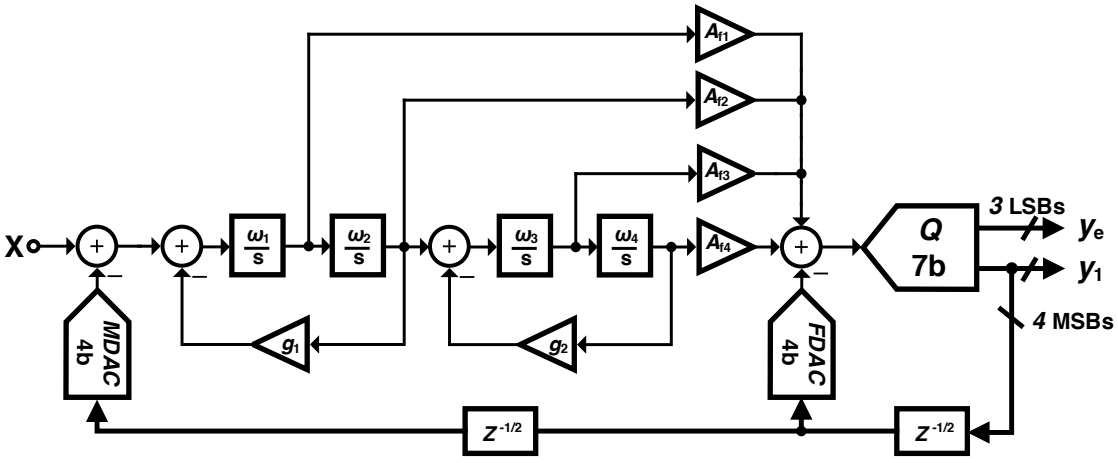


Fig. 3.7: Fourth order system level CTΣΔM with 7-bit quantizer.

During NTF_{AD} computation, an out-of-band signal is entered into the ΣΔ modulator, and data is collected and processed to estimate loop's NTF. Two FFT blocks are needed to process the four MSBs and the three LSBs independently. The block diagram of the

digital implementation to obtain NTF_{AD} is shown in Fig. 3.8. The output of the FFT blocks, Y_1 for the four MSBs and Y_e for the three LSBs, are used as inputs of a digital signal divider to obtain the estimated NTF. Since the signal is in the frequency domain the division operation is implemented bin by bin. The resulting data (NTF_{AD}) is saved in a look-up table to be used for the implementation of DQNRA with real time data.

The MATLAB® simulated outputs of the FFTs for the case of a 15 MHz bandwidth modulator, Y_1 and Y_e, are shown in Fig. 3.9. The out of band signal at 20 MHz, present in Y_1, is used to properly randomize, and stabilize the noise floor of the CTΣΔM to have a better estimation of modulator's NTF. The out of band signal is not present in Y_e, which means that Y_e only contains the information regarding the quantization noise (E_2-E_1). The signals are processed bin by bin to obtain the transfer function shown in Fig. 3.10. In a real implementation the digital decimation filter, placed before the algorithm block, removes the out of band bins making the realization easier. The test tone can also be easily removed, which reduces the complexity of the digital circuitry.

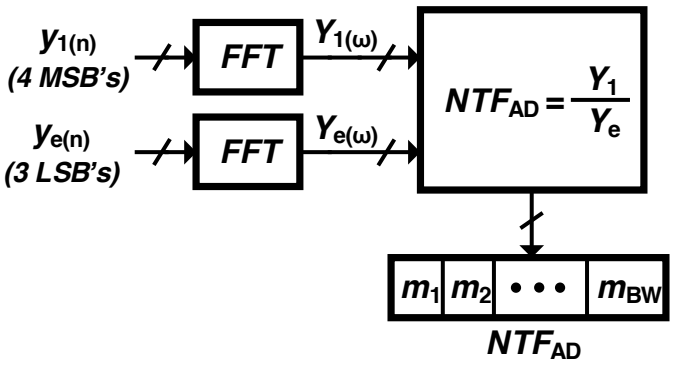


Fig. 3.8: NTF_{AD} algorithm realization.

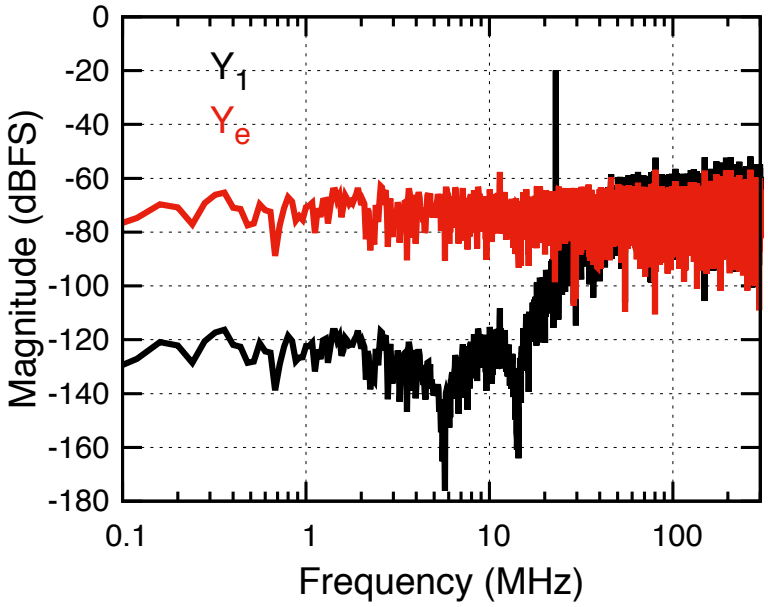


Fig. 3.9: Simulation results: CTΣΔM output data loop signal and error signal.

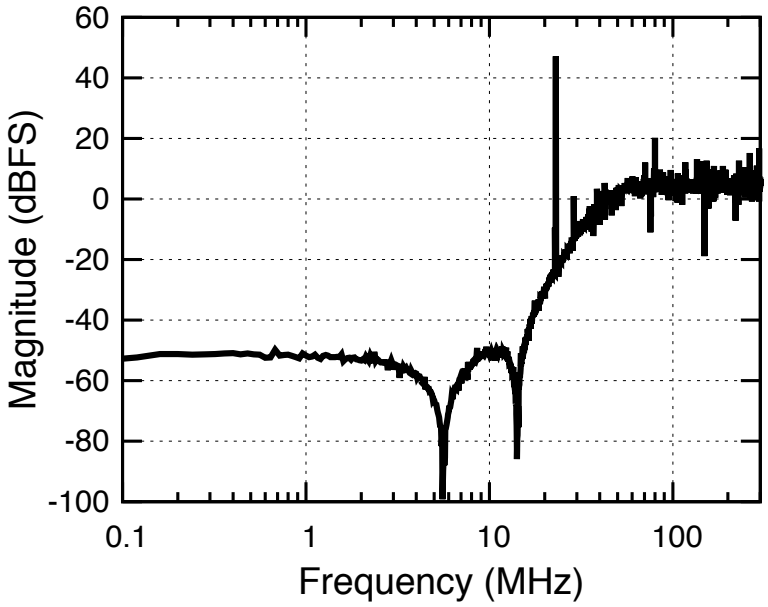


Fig. 3.10: Simulation of NTF_{AD} extraction.

Once NTF_{AD} is measured and saved, the algorithm is implemented and used for the processing of the real time data as shown in Fig. 3.11. First, the quantization error signal (Y_e) is multiplied by NTF_{AD} bin by bin. The result is then subtracted from Y_1, yielding to the output of the algorithm. The digital resources necessary to implement the algorithm are only the digital multiplier and a couple of digital adders. The needed standard digital blocks are highly scalable with process technology.

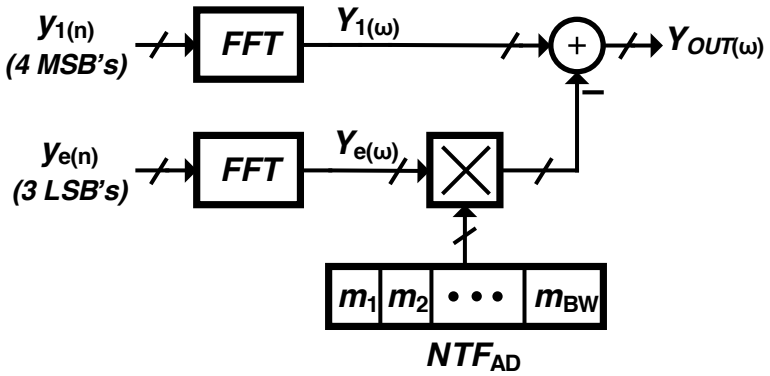


Fig. 3.11: Algorithm implementation.

3.5. Time domain filtering implementation

For a more general implementation of this technique a time-domain option is desired. The information necessary for the time-domain implementation can be obtained from the frequency domain operations. NTF_{AD} shown in Fig. 3.10 is the frequency domain representation of the impulse response of NTF_{AD}. Therefore, if the inverse-FFT (iFFT) is applied, the impulse response of the digital filter necessary for noise cancellation is

obtained; the concept of time-domain implementation is shown in Fig. 3.12. It combines the extraction of NTF_{AD} in the frequency domain and the filtering and noise cancellation implementation in the time-domain.

The number of filter taps is defined by the number points for the required FFT and iFFT; it is expected that a higher number of taps will provide a better result. However, is it desired to keep the number of points for the FFT and iFFT as low as possible to minimize the digital resources needed for the realization of the digital FIR filter. Fig. 3.13shows the effect of the number of taps on the noise improvement for the architecture proposed in Fig. 3.12. As expected, a higher number of taps results in better SQNR with less dispersion.

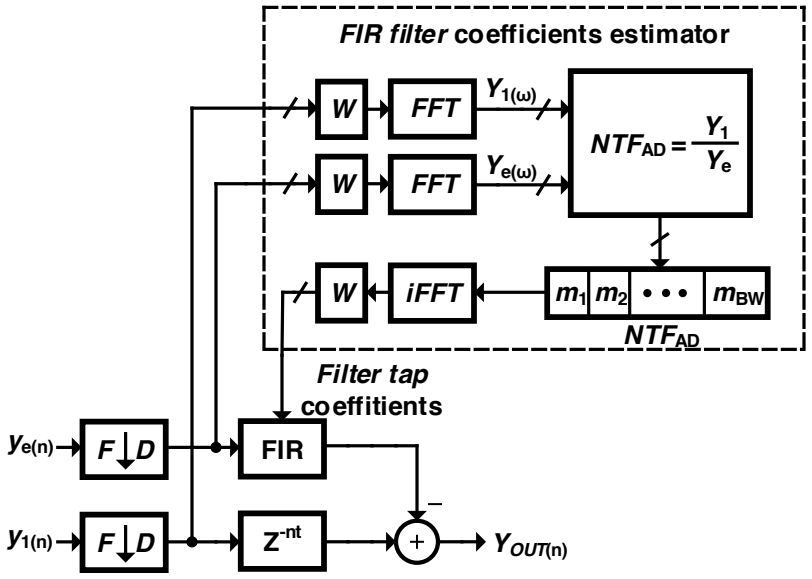


Fig. 3.12: Time domain implementation with frequency domain filter taps calculation.

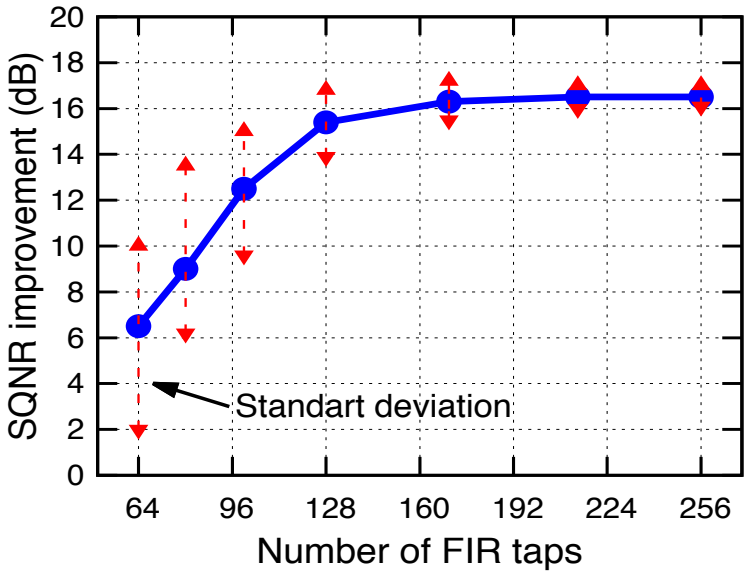


Fig. 3.13: Effect of number of FIR taps on SQNR improvement.

3.6. CTΣΔM implementation

To test the proposed algorithm, the CTΣΔM shown in Fig. 3.14 was implemented using feedforward compensation. Four transconductors (A_{Fi}) and a feedback TIA (A_5 and R_{F3}) implemented the feedforward coefficients. A_5 also served as a summing node to inject current from the excess loop delay (ELD) compensation DAC (FDAC). The main DAC (MDAC) and FDAC were implemented with conventional current steering topologies. MDAC included latches clocked at one clock delay, and on-chip mismatch calibration. An external clean clock signal was used to reduce the effect of clock jitter. FDAC was directly connected at the output of the quantizer. The 7-bit quantizer was implemented with a three step subranging architecture; details are described in the

following section. The OSR was 16.66, which will resulted in a sampling frequency (f_S) of 500 MHz. The implemented loop architecture was selected for simplicity. However, the algorithm developed in this research can be used in all other architectures. The SQNR improvement algorithm relies on the quantizer and the DQNRA.

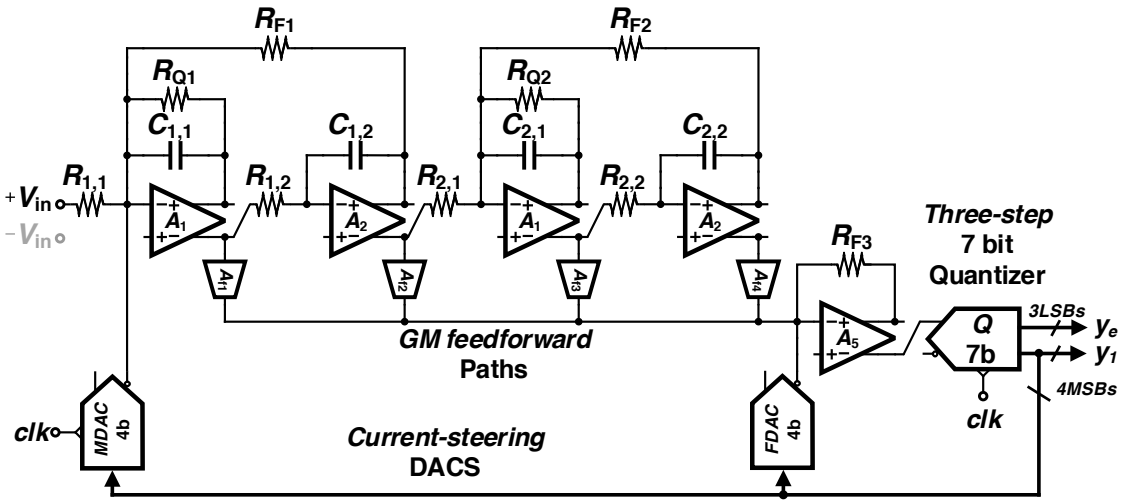


Fig. 3.14: Single-ended version of implemented modulator. (Actual implementation is fully differential).

3.7. 7-Bit quantizer implementation

Compared with a 7-bit flash ADC which requires 128 comparators, the 7-bit subranging ADC implemented with four coarse bits and three fine bits, requires 22 comparators (15 and 7 respectively). The proposed three-step architecture requires only eight comparators since different design techniques are combined. As depicted in Fig. 3.15a, during the first clock phase the MSB is solved employing a simple sign

comparator, and the result is used to select the proper (positive or negative) reference voltage needed to solve the remaining bits. The next three bits are obtained in thermometer code employing seven comparators as displayed in Fig. 3.15b. The comparator outputs are connected to coarse reference voltages generated from an accurate resistive ladder. The four MSBs are available after this stage. Finally, the remaining three bits are obtained employing the same seven comparators. A digital logic uses the four MSBs to select the proper fine reference voltages from the same resistor ladder as shown in Fig. 3.15c.

The power consumption and silicon area are cut by more than 50% compared with a two-step subranging architecture. In addition, the proposed architecture eliminates the resolution limitation introduced by the use of two sample and holds and two different channels from a subranging architecture [17].

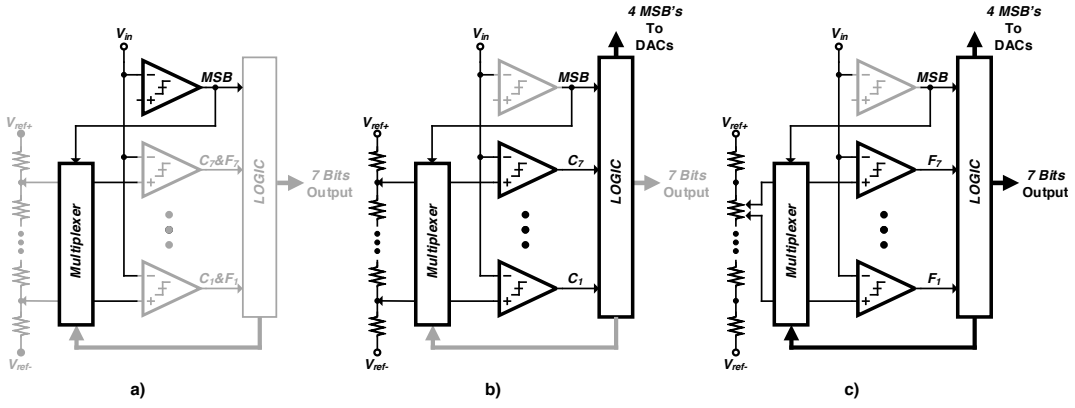


Fig. 3.15: Conceptual implementation of 7-bit quantizer. a) First step used to obtain the MSB, b) configuration used to determine the 3 MSB's and complete the 4 MSBs needed for the loop and c) the final three bits are obtained employing the subranging approach.

3.7.1. Three-step 7-bit quantizer

A detailed block diagram of the implemented 7-bit quantizer is shown in Fig. 3.16. It consists of an MSB comparator (*MSBC*), seven passive sample and hold (S/H_i) circuits, seven comparators for coarse/fine bits ($CFC_{0\text{-}6}$), digital logic for coarse and fine reference voltage selection, a MUX and a thermometer-to-binary encoder. In this quantizer, the input is connected to the MSB comparator (MSBC) and seven sample and hold (S/H_i) circuits. During the first clock phase the input signal V_i is sampled by the seven S/H_i blocks; the MSB is solved as well. In the second clock phase, the multiplexer (MUX) provides the reference voltage to solve the coarse bits. The capacitors in the S/Hs are connected such that the residue signal $V_{refi}-V_{in}$ is generated at each comparator's input. Thus, the comparison is carried out at the common-mode level rather than at the absolute value of the set of reference voltages. This technique allowed us to minimize the voltage dependent offsets and allowed us to optimize the comparator's performance. Details will be discussed shortly. After the MSBs are solved, the thermometer output of the coarse bits goes to the digital logic gates that control the MUX to select the proper fine references. In the third clock phase, the resistive segment is selected and the capacitors are properly reconnected through the control of the MUX. The LSBs are then solved. Each CFC_i is followed by two SR latches (SR-Coarse and SR-Fine); the MSB comparator is also followed by an SR latch but with no clock [24] to hold the signal for a complete clock cycle.

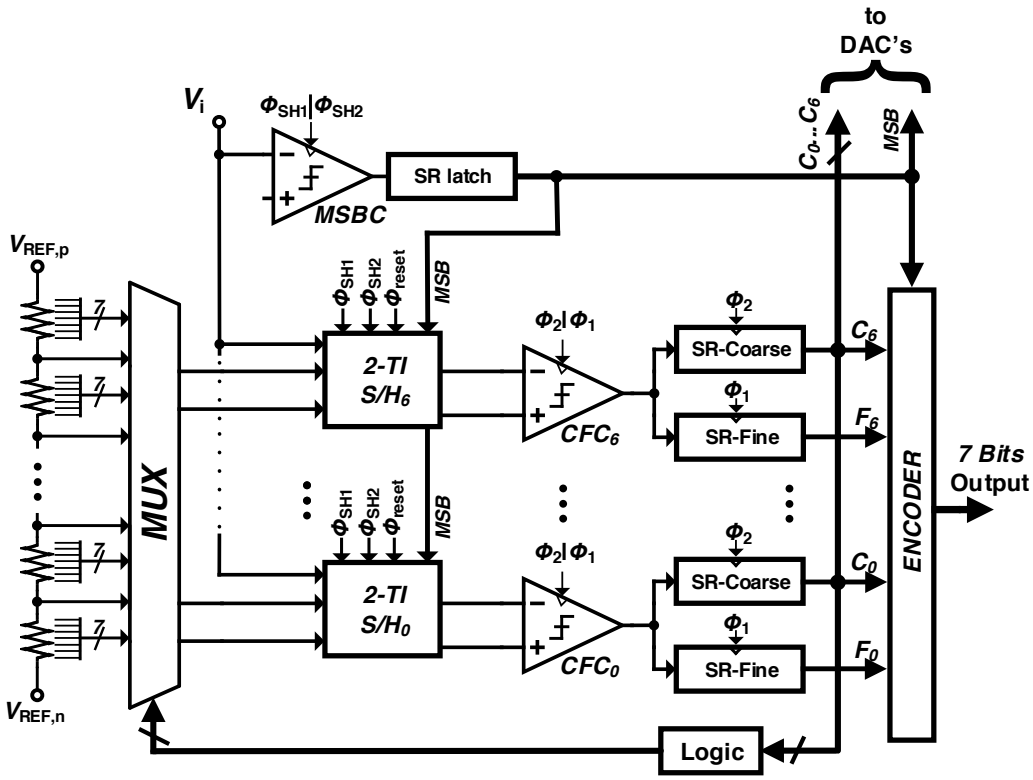


Fig. 3.16: Single-ended version of proposed 7-bit quantizer.

Fig. 3.17a shows the implementation of the S/H_i; each sample and hold is composed of four capacitors that implement a differential two-time interleaved (2 - TI) architecture. The control switches (1 and 2) are operated with two non-overlapping clock signals Φ_{SH1} and Φ_{SH2}, which operate at half of the sampling frequency (f_S). The capacitors sample the input signal and also perform two operations. Each capacitor sample and holds the input voltage ($V_{in(n)}$ and $V_{ip(n)}$) for a complete period to solve the coarse and fine bits. One of its terminals is connected to the MUX to be eventually connected ($V_{ref,n}$ and $V_{ref,p}$) to the resistive ladder while the second terminal is connected to the input of the compactor (CFC_i). This configuration allowed us to compute the residue at the comparator's input. After the residue was computed, we were able to detect the sign of the differential input signal. This sign comparison helped to simplify the design of the seven coarse/fine comparators and improved its accuracy and conversion speed. The folding switches (f_i and f_{iB}) connected the capacitors to the proper reference voltages depending on the result from the MSB comparator (*MSBC*). The circuit used to generate the folding switches control signal is shown in Fig. 3.17b. Fig. 3.17a also includes a reset switch at the input of the comparator, which is activated during the non-overlapping time to reset the parasitic capacitance at the input of the comparator to common mode voltage and reduce the effect of signal dependent errors.

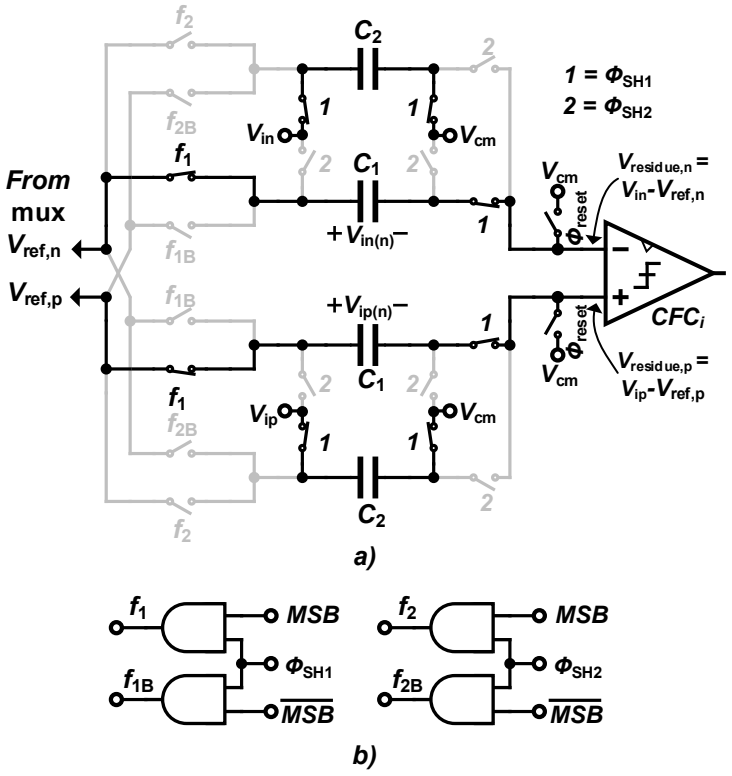


Fig. 3.17: a) Sample and hold implementation and comparator and b) folding signal generation.

3.7.2. Timing diagram for quantizer and MDAC

A detail timing diagram is shown in Fig. 3.18a; six clock signals are generated from an external 2 GHz clock reference. As previously shown in Fig. 3.16 Φ_{SH1} and Φ_{SH2} signals, besides controlling the sample and hold are used to active *MSBC* with the falling edge. The time available for SH_i to track the input signal, is the time period 2 ns minus the non-overlapping time 200 ps. For this design the available tracking time is around 1.8 ns. With almost a full clock cycle for signal tracking the design of the sampling

switches is relaxed. Φ_1 and Φ_2 have a frequency equal to f_S (500 MHz) and control the comparators (CFC_i) clock is provided with an OR gate. Φ_1 or Φ_2 activate the comparator depending if is fine or coarse bits respectively. Also, Φ_1 rising edge is 100 ps early compared with the falling edge of the sampling signals (Φ_{SHi}). This is done to solve the fine bits from the previous operation before the sampling caps are disconnected, and the input of the comparators is reset. Finally, Φ_{ref} control the time available for the MUX to select the coarse or fine reference voltage.

Fig. 3.18b shows the residual voltage ($V_{residu,\,n}$ and $V_{residu,\,p}$) change at the input of the comparator (CFC_i) for the different phases. First, both signals are equal to the common mode voltage, this is due to the reset switch, and the folding switch inside the sample and hold reacts until the MSB is solved. The signal from *MSBC* will have some delay t_{dMSB}, due to MSBC and SR-latch. After t_{dMSB}, the capacitor will be connected the coarse voltage reference and the residual voltage starts moving as shown. The residual voltage signal needs time to settle, is defined by the switch resistance and the parasitic capacitance at the input of CFC_i. The signal has 0.9 ns ($f_s/2 - 100\ ps$) to settle. Next, Φ_2 activates CFC_i to compare the differential input, and SR-Coarse to hold the bits for a complete clock period. The change between coarse and fine reference voltage has a delay t_{dCoa}, represents the delay from CFC_i, SR-Coarse and the digital logic used to determine which fine reference voltage needs to be selected from the resistive ladder. After the fine reference is selected, the residual voltages start changing again. The signal has until 1.9 ns to settle. At that moment Φ_1 activates again CFC_i to solve the remaining fine bits, SR-Fine is activated to hold the signal for a complete clock cycle. The fine

output is available after a delay t_{dFine}. Moreover, Φ_1 is used to clock MDAC, including the delay from the latches inside MDAC the main feedback signal will be injected in the input of the modulator at Z^{-1}.

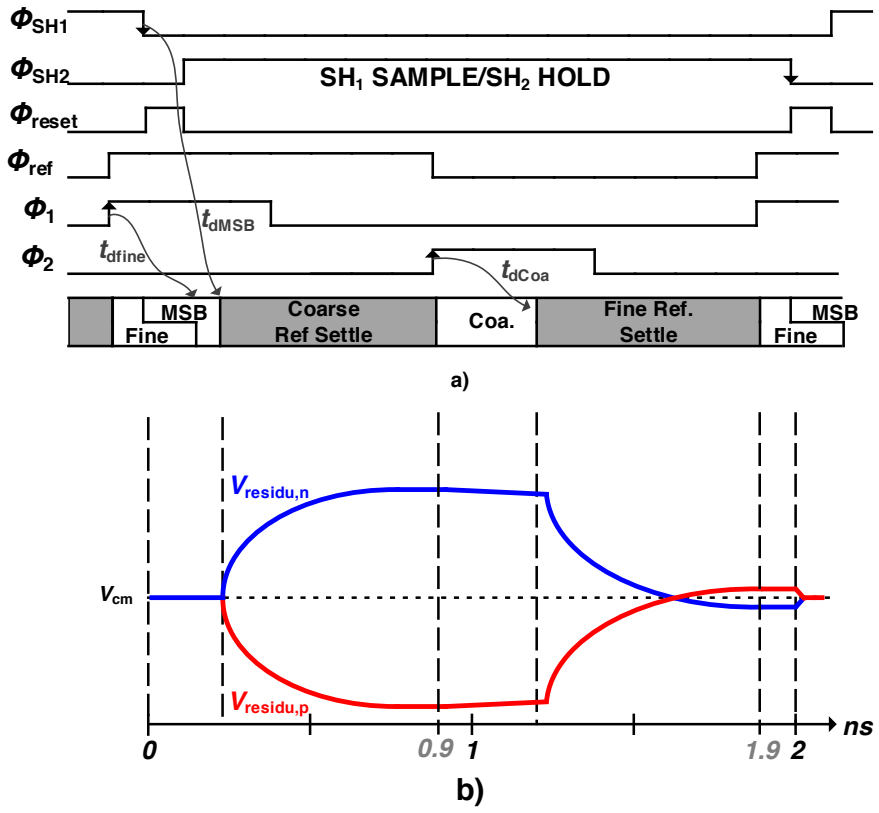


Fig. 3.18: a) Timing diagram and b) voltage change at the input of the comparator.

3.7.3. Comparator implementation and offset calibration

Fig. 3.19a shows the schematic of the comparator used in the 7-bit quantizer. Since the sampling capacitor helps to subtract the input signal from the reference voltage, a single differential amplifier is used to amplify the residue signal and also to isolate the capacitor from the latch. In contrast with the conventional differential difference amplifier (DDA) comparator topology commonly used in flash, in this design only the polarity of the input signal at the common mode level needs to be resolved, which minimizes common-mode level issues and relax the comparator's design. The 18dB preamplifier reduces kickback noise from latches. The preamplifier is followed by a modification of the double tail latch [25]. The comparator operates at 1GHz to convert the coarse and fine bits within one clock cycle. To ensure proper operation with 7-bit resolution, an offset cancelation topology is used. Fig. 3.19b shows the offset calibration circuit. The input of the preamplifier is connected to the common mode levels. Next, offset compensation current (I_{TRIM}) is injected at the output of the preamplifier. I_{TRIM} is increased in binary step with a digital logic until the output of the SR latch toggles [11].

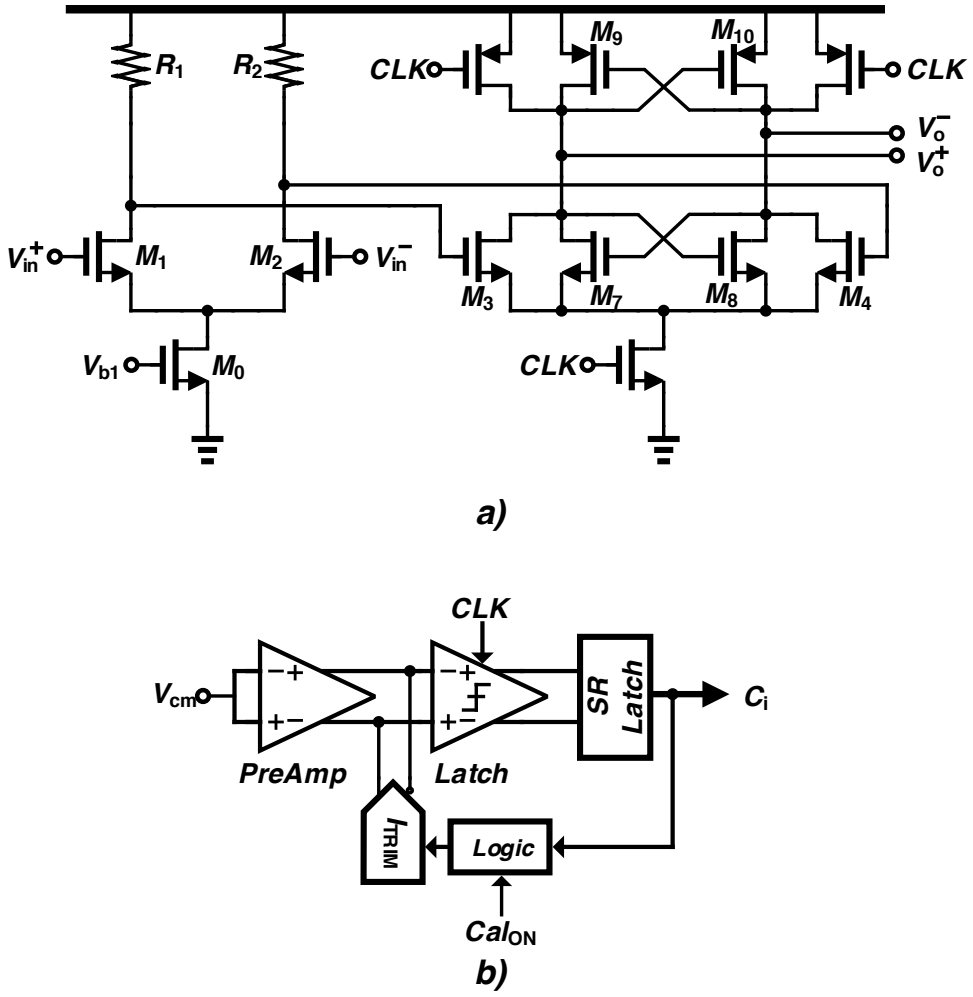


Fig. 3.19: a) Implemented comparator with pre-amp. b) comparator offset cancellation.

3.8. Measurement results

The ADC is implemented in a 130 nm CMOS process. The microphotograph of the test chip is shown in Fig. 3.20, where the active area is 1.3 mm^2. The chip operates from a 1.2 V power supply. External LDOs are used to provide the voltage for the analog and digital blocks respectively. The modulator consumes a total of 20 mW, where only 6 mW are used in the 7-bit quantizer. Fig. 3.21 shows the power consumption distribution. An internal decoder is used to convert thermometer coarse and fine bits of the quantizer to 7-bit binary and align all the signals for external post processing.

The DQNRA was implemented externally. The estimated power consumption for the digital engine needed implement a 1536-point FFT after decimation should add around 6.5 mW in 65nm, as reported in [26].

Fig. 3.22 shows the FFT output of the modulator, before and after the DQNRA was applied for a 4.15 MHz −1 dBFS single tone input. To illustrate the effect of the algorithm at high frequencies the FFT was applied to the complete data 32 K points. Before the DQNRA was applied the peak SNDR was 69 dB and SNDR increases up to 75 dB after DQNRA was used. The third harmonic distortion was also reduced indicating that this distortion could be generated in the quantizer. The algorithm is able to attenuate the harmonic distortion components coming from the quantizer. The SFDR after noise reduction was −83dBc.

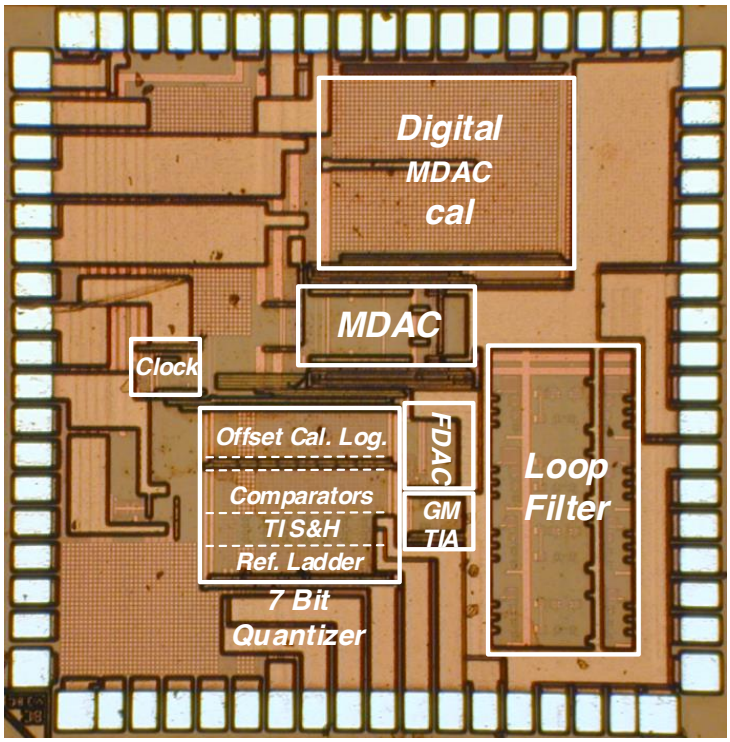


Fig. 3.20: Chip microphotograph.

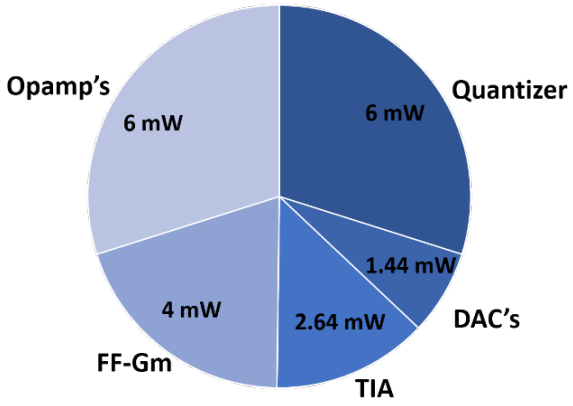


Fig. 3.21: Power consumption distribution (15.5 mW static and 4.5 mW dynamic).

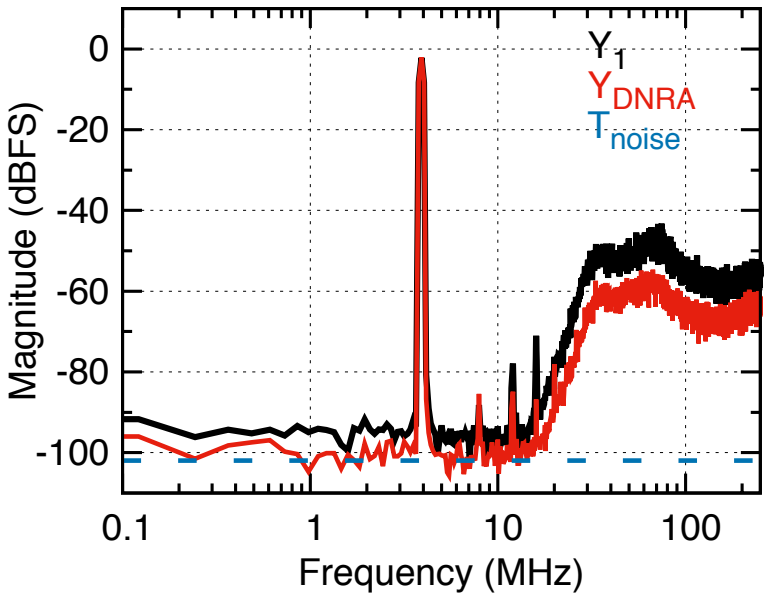


Fig. 3.22: Measured output spectrum before and after DQNRA.

Both in-band and out-of-band noise components reduced as expected. The in-band SNR improvement was around 6 dB, which was less than the expected 15 dB improvement. For this particular design, after the noise reduction algorithm was employed, the in-band noise floor was found to be limited by the thermal noise rather than quantization noise. The estimated thermal noise level is also included in Fig. 3.22. However, an SNR improvement of more than 10 dB was consistently observed for a frequency higher than 15 MHz where quantization noise dominates as shown in Fig. 3.23. This data confirms the DQNRA operation, and shows that the quantizer has an effective resolution of 6 bits.

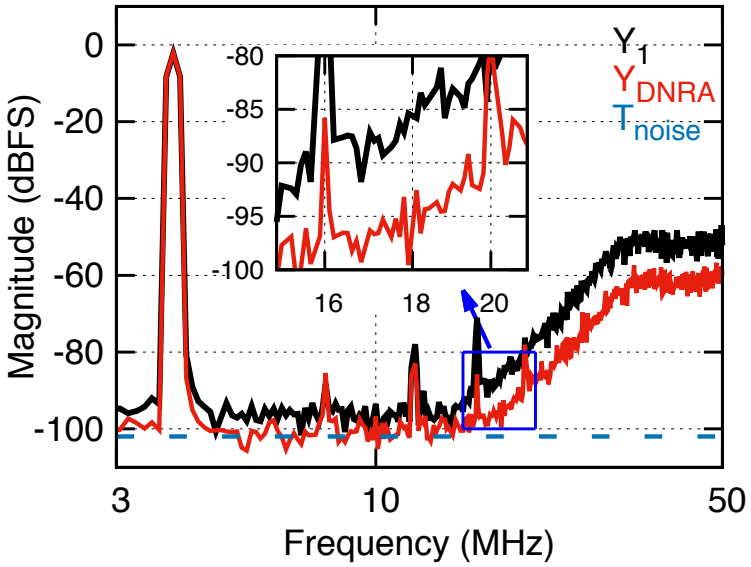


Fig. 3.23: Zoom in transition out of bandwidth noise improvement.

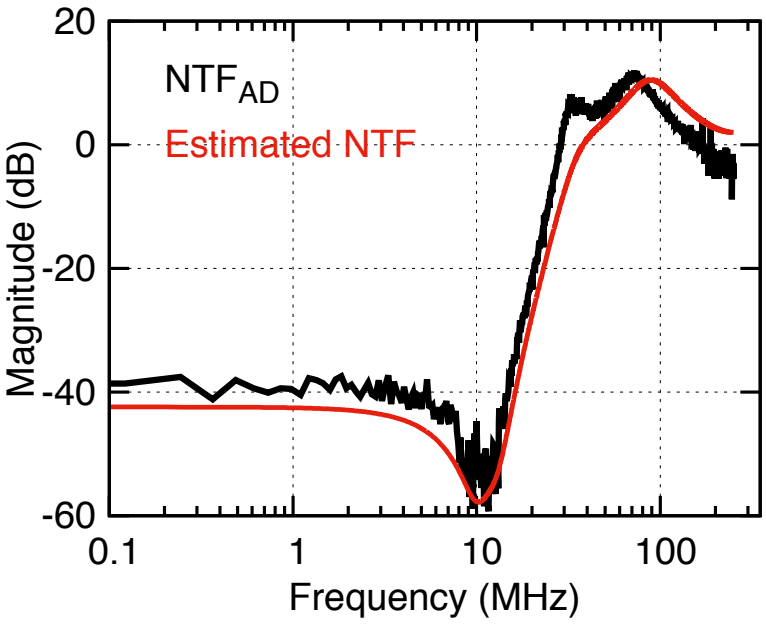


Fig. 3.24: Measured NTF with algorithm (NTF_{AD}) vs estimated NTF.

Fig. 3.24 shows a comparison of the measured NTF_{AD} through the proposed algorithm and the estimated NTF. In this case, NTF_{AD} was obtained after averaging the data 50 times. The correlation between experimental and simulation data is remarkable. It is worth mentioning that NTF_{AD} is PVT tolerant, provided that the data is updated continuously. Fig. 3.25 shows the SNDR vs input power plot, before and after the DQNRA algorithm was applied. The result shows a constant improvement of around 6 dB. Table 3.1 compares this work with recently published MASH ΣΔMs with loop bandwidths over 1MHz. Implemented in a mature process technology, this circuit achieves the best FoM for both fJ/conv and dB.

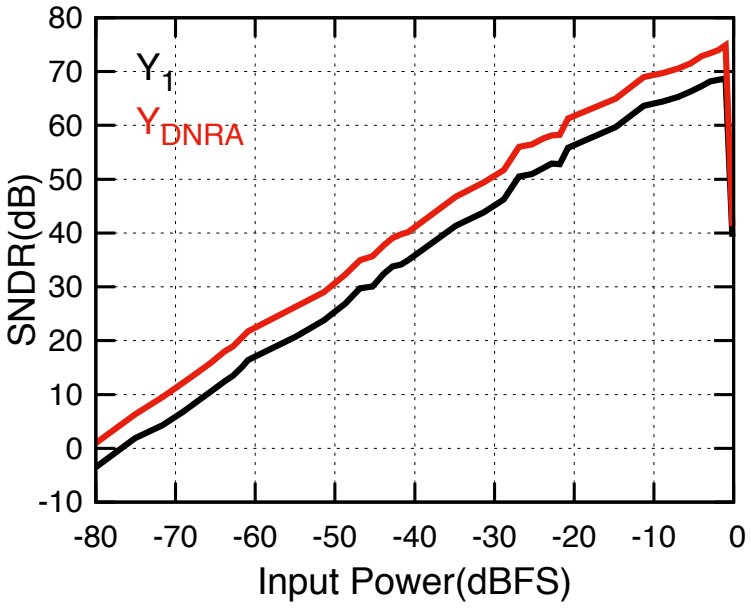


Fig. 3.25: SNDR vs input power.

Table 3.1: Results summary and comparison 15 MHz ΣΔ.

Publication	**This Work**	[7] JSSC09	[27] JSSC12	[28] JSSC14	[10] JSSC14	[9] ISSCC15
Architecture	**L-0**	0-L	L-L	L-0	0-L	L-L
Process (nm)	**130**	180	130	65	28	28
FS (MHz)	**500**	50	130	240	3200	1800
BW (MHz)	**15**	3.125	5	15	53.3	50
SNR(dB)	**78**	77.2	75.8	--	83.1	76.8
SNDR (dB)	**75**	73.9	75.7	67	71.4	74.9
DR(dB)	**79**	79*	76*	--	88	85
VDD (V)	**1.2**	1.8	1.2	1.25	1.8/-1	--
Power (mW)	**20**	24	16	46	235	80.4
FoM_1 (fJ/conv bit)	**145**	950	321	838	726	177
FoM_2 (dB)	**163.7**	155	160.6	152	155	162.8

*Extracted from DR plot because is not reported.

$FoM_1=Power/(2\cdot BW\cdot 2^{(SNDR-1.76)/6.02})$

$FoM_2=SNDR+10\cdot\log_{10}(BW/Power)$

3.9. Conclusion

This chapter presented the implementation of a CTΣΔM, with a low power and low area 7-bit quantizer and a fully digital noise reduction algorithm for SQNR improvement. The proposed algorithm is precise and robust against PVT variations and does not rely on digital filters to implement an estimated NTF. The need of precise analog delays is avoided thanks to the use of only one quantizer with higher resolution. Furthermore, the number of active components is minimized compared with the recently reported cascaded and MASH implementations. The architecture relies on the operation of a 7-bit quantizer. The implemented quantizer covers less area and is more power efficient than previously reported FLASH, subranging and two-step architectures. The obtained results in a mainstream 130nm technology achieved better performance than previously reported architectures; hence, it is expected that a better figure of merit is achievable if more advanced technologies are used.

IV. A 75 MHZ BANDWIDTH CONTINUOUS-TIME SIGMA-DELTA ADC WITH A BROADBAND LOW-POWER COMMON-GATE SUMMING TECHNIQUE

4.1. Introduction

Higher data rates required for emerging wireless standards demand continuous-time ΣΔ modulators (CTΣΔM) with bandwidth (BW) higher than 20 MHz [9, 10, 12, 29-34] that correspondingly increase its power consumption. Among other challenges, the power increase due to higher loop's filter requirements is one of the most critical ones. Filter architectures based on single amplifier biquad (SAB) realizations have already been proposed to reduce static power [35], [36]. However, for architectures that implement the excess loop delay (ELD) compensation with a fast path around the quantizer, demand more power consumption from the operational amplifiers (OpAmps).

Feedforward CTΣΔMs are the architectures of choice for low power implementations, the use of an active summing amplifiers required for the realization of the feedforward compensation coefficients and ELD compensation path [37] is not very attractive due to the excessive power required by the operational amplifier (OpAmp) [35].

To overcome these drawbacks, the use of passive networks for the implementation of feedforward zeros and ELD path has been recently proposed [38], [39]. However, loading effects in the loop filter and inherent attenuation on loop gain demand better performance in other building blocks to maintain the overall loop gain invariant. A digital compensation can also be embedded in the quantizer [40], [41] to eliminate the summing node. Unfortunately, the maximum signal swing that can be used at the input of the quantizer is reduced by the gain of the feedback ELD coefficient, thereby limiting the achievable signal to noise ratio (SNR).

In this chapter, a summing amplifier based on a common-gate current buffer that decouples the dependency of the closed loop gain and the design specifications of the summing amplifier OpAmp is proposed. This approach enables high frequency operation for closed loop OpAmps, relaxes the power consumption requirements and provides independent control of loop filter compensation coefficients. Moreover, the addition of the current buffer provides an extra degree of freedom for the design of a closed loop OpAmps with the best step response for high frequency operation. A detailed analysis on to design for the optimum phase margin for the best step response is presented, this simple approach avoids adding extra capacitors for phase margin compensation, which introduce additional delay that limits the performance at gigahertz operation.

The chapter is organized as follows. Subsection 4.2 present the implemented architecture and discusses the system level details. Subsection 4.3 presents analysis for optimum design point for the step response of a closed loop OpAmp. Subsection 4.4 present the detailed circuit implementation. Subsection 4.5 present the obtained

measurement results. Finally, subsection 4.6 presents a summary of the results and concludes the chapter.

4.2. Architecture

The selected CTΣΔM architecture is composed by a 3rd order filter, with a 4-bit quantizer. Feedforward compensation is selected due to its simplicity and robustness. Fig. 4.1a shows the selected filter architecture with a conventional summing amplifier, for which the specifications of A_3 are defined by the closed loop gain, clock frequency, and quantizer's input load, which make this implementation unpractical for the GHz range clock frequencies. Fig. 4.1b shows the selected filter architecture, including the conceptual proposed current buffer. The second-order portion of the filter is implemented employing a multiple feedback (MFB) SAB and is formed by R_2, R_3, R_4, C_y, C_2 and A_2; one of the FF compensation coefficients is embedded on the SAB and realized with a single capacitor C_x. The overall transfer function for the MFB SAB is shown in (4.1).

$$\frac{V_{ox,2}}{V_{ox,1}} = -\frac{(1+sR_2C_x)\left(\frac{1}{R_3R_2(C_x+C_y)C_2}\right)}{s^2 + s\frac{\left(\frac{R_3R_4}{R_2}C_2 + R_3C_2 + R_4C_2\right)}{R_3R_4(C_x+C_y)C_2} + \frac{1}{R_3R_4(C_x+C_y)C_2}} \tag{4.1}$$

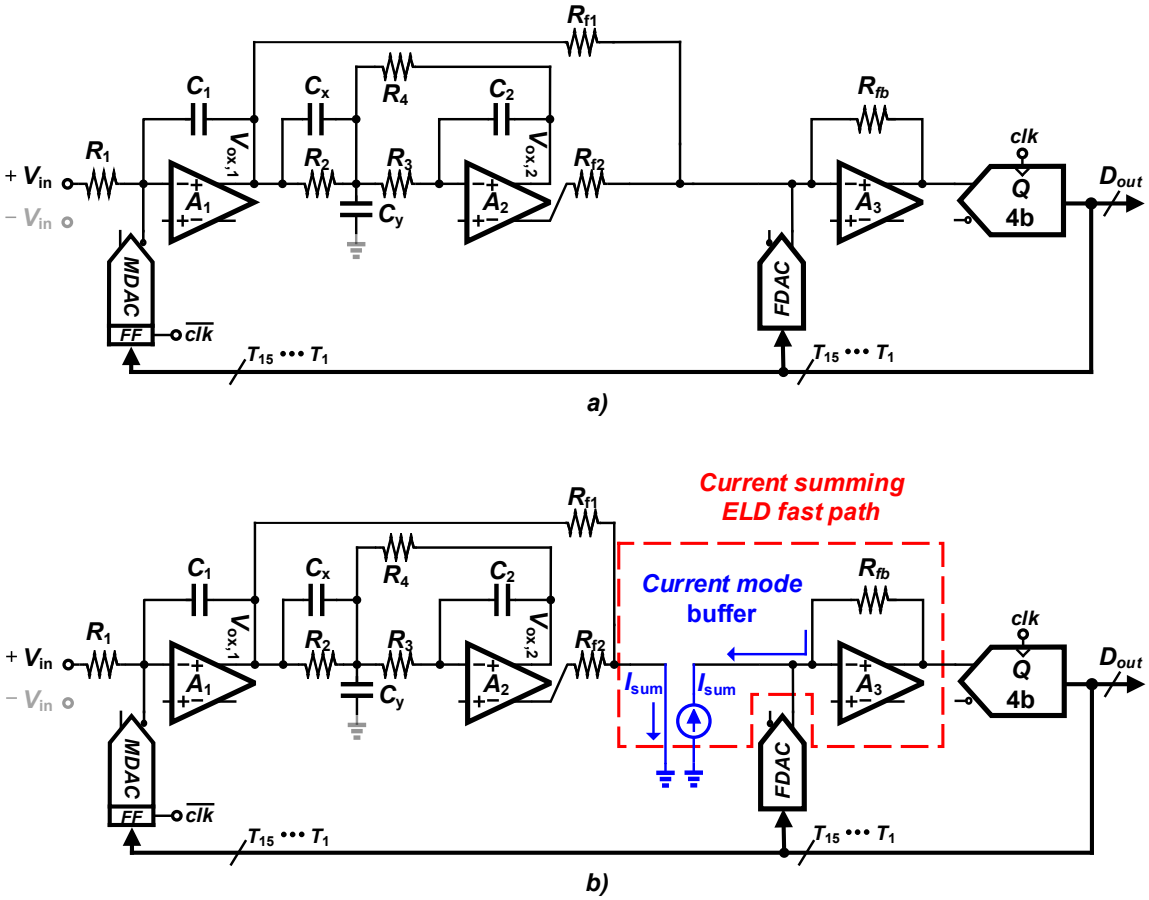


Fig. 4.1: Selected 3rd-order architecture with proposed current summing amplifier.

The remaining two FF paths implemented by R_{f1} and R_{f2}, and the ELD compensation fast-DAC (FDAC) are combined at the low impedance nodes available at the input of the current buffer block and the input of the transimpedance amplifier (TIA) formed by A_3 and R_{fb}, respectively. The quantizer uses a 4-bit flash. Also, MDAC and FDAC were implemented with current steering architectures. MDAC uses an extra set of flip-flops to avoid the voltage dependent delay errors introduced from the quantizer comparators.

The proposed current-mode adder (implementation details are shown in Section 4.4) isolates the resistors and the input of the amplifier A_3. Connecting R_{f1} and R_{f2} directly to the amplifier's input used in conventional solutions (Fig. 4.1a) reduces the feedback factor (β) and then demands more gain and BW from A_3 to maintain loop functionality. Furthermore, since A_3 processes the pulsed signal generated by FDAC, it requires a wider BW and faster response. The settling time of A_3 is proportional to the amplifier's transconductance and load impedance, but it is also inversely proportional to β. For high sampling rates (smaller time for settling) and small β the OpAmp specifications steadily increase in both circuit complexity and power consumption. In the proposed solution the current mode buffer isolates the FF resistors from the TIA input. If the current buffer provides a gain of one, the FF coefficient gain is defined by the ratio of resistors as in a conventional summing amplifier. However, the selected closed loop gain does not define the specifications for A_3, since β is defined by R_{fb} and the output impedance from the current buffer. To ensure A_3 stability, the impedance looking back at the current buffer and FDAC is adjusted to make β close to the optimum value for power consumption reduction while ensuring loop functionality.

The implementation of an active summing amplifier with gain can also help to relax the specifications from other building blocks. Fig. 4.2a shows the effect of a passive summing node that provides attenuation; hence, as the swing at the internal nodes of the loop filter and FDAC increase, more current and a larger output swing range is required from the OpAmps. However, if an active architecture with gain is used as shown in Fig. 4.2b, the larger output swing at the internal nodes of the filter are reduced demanding less output current, and the swing specifications are relaxed allowing lower voltage operation.

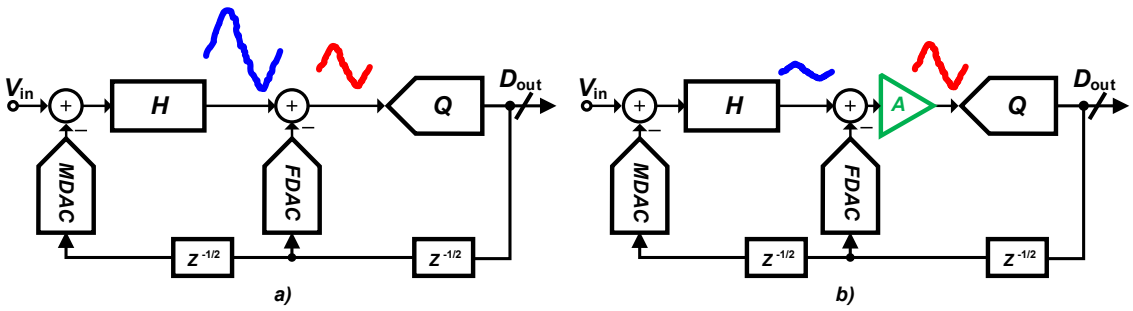


Fig. 4.2: CTΣΔM voltage swing a) passive summing node implementation with attenuation, b) active summing amplifier with gain.

4.3. High frequency ELD implementation analysis

The small signal model of the ELD circuit with current buffer for the OpAmp and FDAC is shown in Fig. 4.3. R_{buf} represents the impedance looking back at the current buffer, R_{fb} is the resistor in feedback, OpAmp A_3 from Fig. 4.1 is represented by the voltage controlled current source $g_m \cdot V_x$ and the output resistor R_o, the load capacitor C_L is mainly dominated by the input capacitance of the quantizer, I_{in} represents FDAC, and C_{in} is the parasitic capacitance at node V_x formed by the input capacitance of A_3 and the parasitics from FDAC.

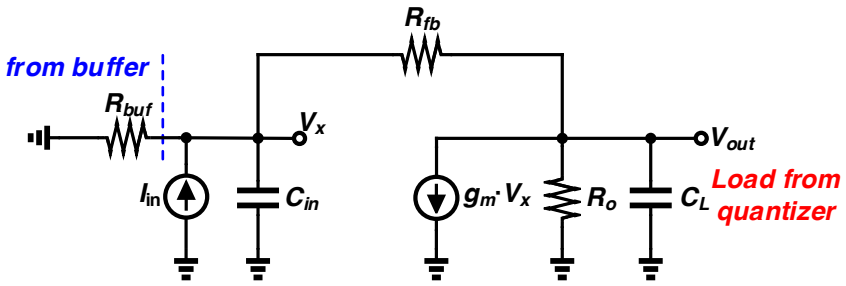


Fig. 4.3: Small signal model of summing amp with current buffer included.

Traditional analysis of OpAmp design with passive components connected in feedback normally considers a system of first order. For low frequency applications this assumption is valid considering the input parasitic capacitance very small compared with the load capacitor ($C_L >> C_{in}$). Doing small signal analysis of the circuit shown in Fig. 4.3 and ignoring C_{in} the transconductance equation can be obtained as

$$g_m = -\frac{\ln(\varepsilon) \cdot C_L \cdot f_s}{\beta} - \frac{1}{\beta \cdot R_L} + \frac{1}{R_{fb}} \tag{4.2}$$

where f_s is the sampling frequency at which the pulses from FDAC will be received, ε is the is the desired settling error, R_L is the output resistance including the loading effect from R_{fb}, $R_L = R_o \| R_{fb}$ and β is the feedback factor defined by R_{fb} and R_{buf}, $\beta = R_{buf}/(R_{buf} + R_{fb})$. Is clear from equation (4.2) that when β is closer to one, the minimum transconductance will be needed. This makes the implementation of the current buffer very attractive for power consumption reduction. But for high frequency operation a more complete analysis needs to be performed.

4.3.1. Second order design considerations

In order to have a precise analysis for high frequency operation the effect of C_{in} needs to be considered. For higher frequencies and advanced process technologies C_{in} can be within one order of magnitude with respect to C_L. Thus, including the effect of C_{in} leads to a second order transfer function as shown in equation (4.3). Therefore, precise second order large signal analysis needs to be applied to achieve a design with the best speed and power consumption tradeoff for high frequency operation.

$$\frac{V_{out}}{I_{in}}$$

$$= -\frac{\left(g_m - {}^{1}/_{R_{fb}}\right) \cdot \frac{1}{C_{in} \cdot C_L}}{s^2 + s \cdot \left(\frac{1}{R_{fb} \cdot C_{in} \cdot \beta} + \frac{C_L}{R_L}\right) + \frac{1}{\beta \cdot R_{fb} \cdot R_L \cdot C_{in} \cdot C_L} + \frac{\left(g_m - {}^{1}/_{R_{fb}}\right)}{R_{fb} \cdot C_{in} \cdot C_L}} \quad (4.3)$$

From the characteristic equation of equation (4.3) the natural frequency and damping factor can be obtained as shown in equation (4.4) and equation (4.5) respectively

$$\omega_n^2 = \frac{1 + \beta \cdot R_L \cdot \left(g_m - {}^{1}/_{R_{fb}}\right)}{\beta \cdot R_{fb} \cdot R_L \cdot C_{in} \cdot C_L} \approx \frac{g_m}{R_{fb} \cdot C_{in} \cdot C_L} \quad (4.4)$$

$$\zeta = \frac{\frac{1}{R_{fb} \cdot C_{in} \cdot \beta} + \frac{C_L}{R_L}}{2 \cdot \sqrt{\frac{1 + \beta \cdot R_L \cdot \left(g_m - {}^{1}/_{R_{fb}}\right)}{\beta \cdot R_{fb} \cdot R_L \cdot C_{in} \cdot C_L}}} \approx \frac{\frac{1}{R_{fb} \cdot C_{in} \cdot \beta} + \frac{C_L}{R_L}}{2\sqrt{\frac{g_m}{R_{fb} \cdot C_{in} \cdot C_L}}} \quad (4.5)$$

The step response of a second order system is well known, for a stable system we can have three main types of responses: underdamped ($\zeta < 1$), critically damped ($\zeta = 1$), and overdamped ($\zeta > 1$). Fig. 4.4 shows the step response of the second order system for different damping factor values with the three cases included, as shown an oversample system although it avoids peaking and ringing, it has a slow settling time. An underdamped system presents the fastest rising time, but for small values of damping

factor it presents large overshoot and ringing, which can affect the settling time. To have the best tradeoff between settling time and peaking, a damping factor between 0.7 and 1 is preferred, which is equivalent to have a loop phase margin between 65º to 76º. The selection of the proper damping factor relies on the amount of peaking that your system can tolerate. To have a peaking within 2% of the final value $\zeta = 0.9$ was selected.

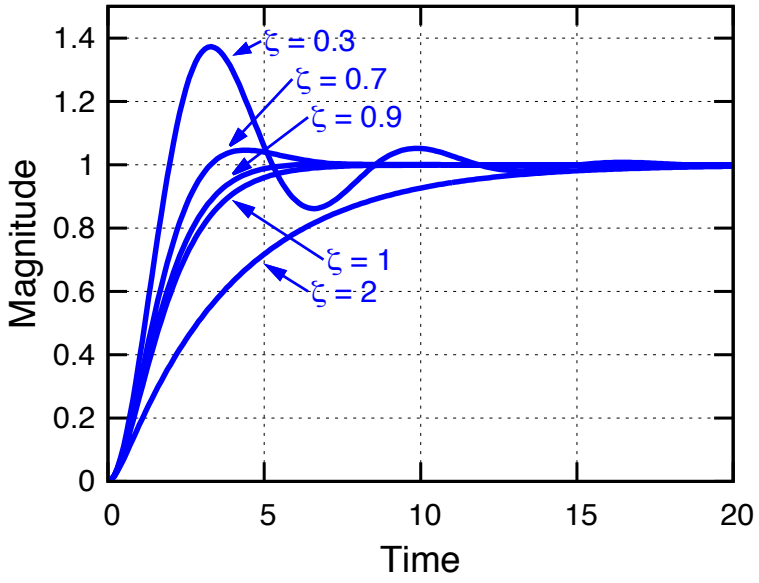


Fig. 4.4: Step response for different damping factor.

For an underdamped system the settling time is defined as follow [42],

$$t_s = \frac{-ln\left(\varepsilon \cdot \sqrt{1-\zeta^2}\right)}{\zeta \cdot \omega_n} \tag{4.6}$$

Equation (4.6) contains four variables, ε and t_s are defined by system level specifications by the allowed settling error and clock frequency respectively, ζ is also

defined as one of the design conditions to be 0.9 for the fastest settling time with minimum peaking. Therefore, the only design variable that needs to be calculated is the natural frequency ω_n, as

$$\omega_n = \frac{-f_s \cdot ln\left(\varepsilon \cdot \sqrt{1-\zeta^2}\right)}{\zeta} \tag{4.7}$$

Once ω_n is known the design component values can be calculated from equation (4.4) and equation (4.5), from this equations some variables are fixed and can be estimated from some of the components in the design, i.e., C_L is mainly dominated by the parasitic capacitance at the input of the quantizer and layout trace parasitics, C_{in} is dominated by the parasitic capacitance from FDAC. Therefore, the unknown variables are: g_m, R_{fb} and β, and since the main goal is to design for minimum g_m we need to find the optimum value for R_{fb} and β to have the minimum transconductance needed in the OpAmp. The process for this is described next.

First equation (4.4) and equation (4.5) need to be solved for g_m, then both equations can be equalized and rearranged as shown in equation (4.8), as shown β presents a quadratic behavior, more importantly it demonstrates that in a second order system β with value of one is not necessarily the optimum in terms of settling time for a step response, the optimum value of β depends on the selected R_{fb} value. In our case the selected value for R_{fb} was 4500 ohms (Ω), since is known that most of the variables (ω_n, ζ, C_L, C_{in}) in equation (4.8) are defined by design or fixed by the load of other blocks, β can be plotted with respect to R_{fb} as shown in Fig. 4.5. For any value of R_{fb} there will be only one value of β to maintain an optimum damping factor for fastest

settling time, or $\beta_{optimal}$. Fig. 4.5 also illustrates the R_{fb} value required for optimum response without the implementation of the buffer, in that case, β is fixed by the feedforward coefficients. The point for the selected R_{fb} is also included; the justification for the selected R_{fb} is shortly described.

$$\beta_{optimal} = \frac{1}{C_{in} \cdot R_{fb} \cdot \left(2 \cdot \zeta \cdot \omega_n - \frac{1}{C_L \cdot R_L}\right)} \tag{4.8}$$

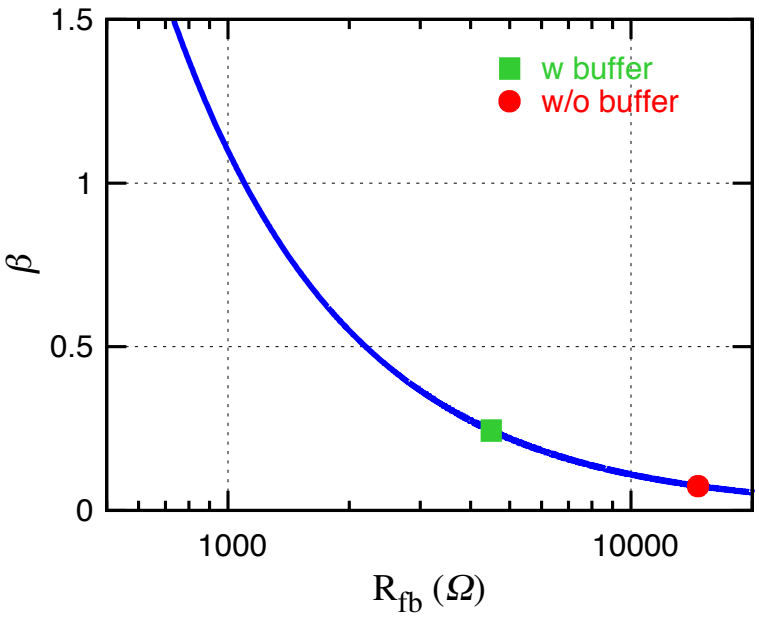


Fig. 4.5: Optimum feedback factor vs feedback resistor sweep.

Once the relationship between R_{fb} and β for the optimum step response is known, we can focus on optimize the design for minimum power consumption. From equation (4.4) the transconductance for the amplifier can found as

$$g_m = \omega_n^2 \cdot R_{fb} \cdot C_1 \cdot C_L - \frac{1}{\beta_{optimal} \cdot R_L} + \frac{1}{R_{fb}} \tag{4.9}$$

If equation (4.9) and equation (4.2) are compared, the transconductance equation for a second order system does not present the same dependency to β as the first order approximation. Instead, is more depended to R_{fb} as illustrated in Fig. 4.6. β is adjusted to the optimum value, as expected the smallest the value for R_{fb} , the smallest g_m will be. For a practical implementation there is a limit on how small R_{fb} can be as illustrated in Fig. 4.6. The reasons of this are: first, a small resistor value will produce loading, not only on the summing amplifier OpAmp, but also on the loop filter OpAmps, since the feedforward coefficients are still defined by the ratio of R_{fb} and $R_{f1,2}$. Therefore, a small value will generate smaller values for the resistors connected to the filter. Second, a small value of R_{fb} will require a large current value for FDAC to recover full-scale signal, which increase its power consumption and silicon area.

Fig. 4.6 also shows a comparison of the case with buffer included and without the buffer for optimum response in both cases. The reduction of transconductance needed from the OpAmp is significant from 58 mA/V to 16.8 mA/v. For the case without the buffer for optimum step response all the values are fixed by feedforward coefficients. In the presented design with the current buffer an extra degree of freedom is included, since β can be adjusted independently of the feedforward coefficients. Therefore, we had more

flexibility for optimization to minimize power consumption. The implementation and details on how to adjust the impedance looking back at the current buffer to control β will be shown in subsection 4.4.

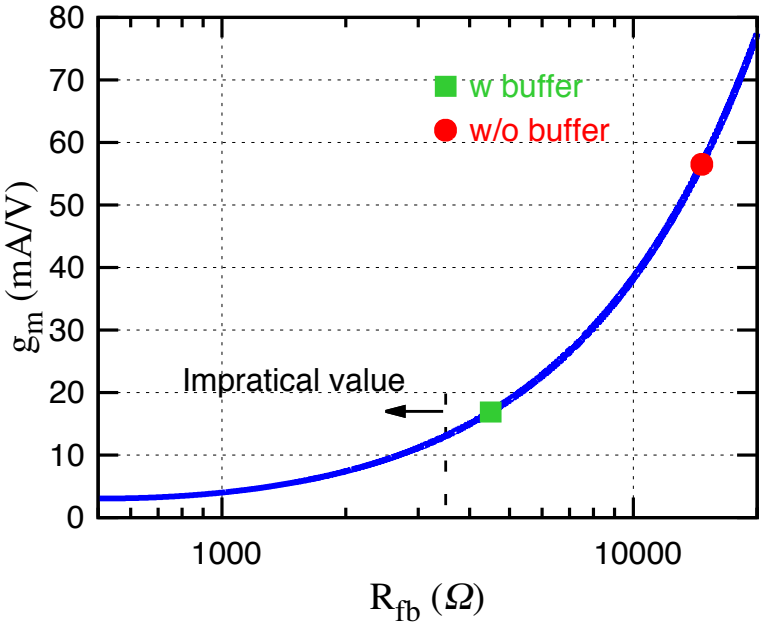


Fig. 4.6: Opamp transconductance vs feedback resistor sweep.

Fig. 4.7 shows a comparison of the effect of β for transient response for three different cases: without the current buffer, with buffer with high output impedance, and with buffer with controlled output impedance. A small β as expected reduced the loop gain, and created an overdamped second order response with slow settling time and large settling error, if the settling error is not large can be easily corrected by increasing the current from FDAC. With the buffer included and β close to one, although, it provides

the fastest slewing time it suffers from ringing the reason of this is the large loop gain and poor loop phase margin that translates to an underdamped system. The oscillations die almost after three clock cycles. With the optimization of β the signal settles properly within the required time, increasing FDAC current can compensate the small settling error.

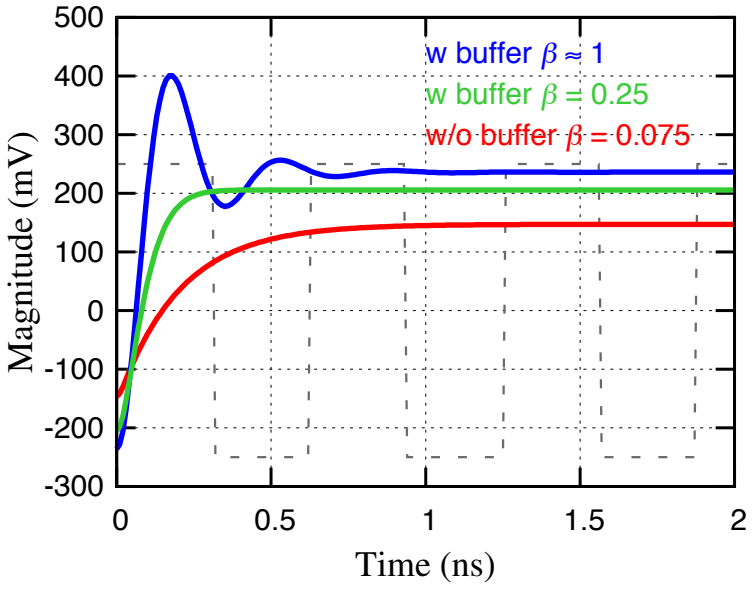


Fig. 4.7: ELD step response, no buffer (red), with buffer (blue), and with buffer with controlled impedance (green).

4.4. Circuit implementation

4.4.1. Common gate buffer with output impedance control

Fig. 4.8 shows the implementation of the current buffer ELD summing amplifier. The current buffer is implemented with a common gate (M_1) configuration. A_3 and R_{fb} implemented the TIA that converts the current difference from the current buffer and FDAC to voltage, and drives the quantizer. Transistors M_2 and M_3 provided the bias current for the current buffer M_1. M_2 also controls the impedance looking back at the output of current buffer, as shown the gate of M_2 is AC coupled to the output of the current buffer this connection created an equivalent out impedance of $\sim 1/gm_2$. Therefore, from the design considerations previously defined and the small signal model shown in Fig. 4.3, $R_{buf} = 1/gm_2$. For the selected R_{fb}= 4500 Ω and the optimum β value shown in Fig. 4.5, the optimum output impedance from the buffer was R_{buf} = 1420 Ω. Since M_2 was needed already to provide the bias current for M_1 no extra current was added for β control, M_2 was sized and biased properly for the required transconductance. Fig. 4.8 also shows the power consumption for each of the blocks, the current for the buffer was 640 μA, with 320 μA in each branch to handle an AC of ~200 μA. The current added by the buffer is minimum compared the current saved in A_3, which was reduced from 7.5 mA without the buffer to 2.05 mA with the buffer. The differential pair transistors in A_3 were designed with g_m/I_d = 16 to have the transistor with small V_{dsat} for low voltage operation, but that can operate in saturation region. The inclusion of the current buffer

will add to the total thermal noise. However, since is used after the loop filter its effect will be reduced by the gain of the OpAmps in the filter.

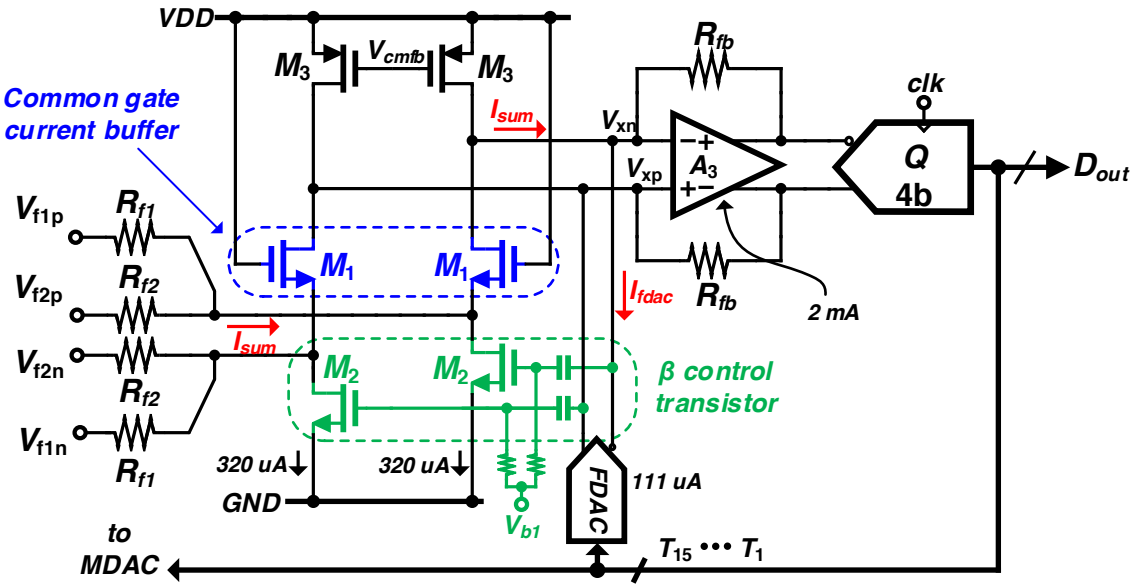


Fig. 4.8: Current buffer and ELD path implementation.

4.4.2. Current buffer input impedance

The accuracy of the feedforward coefficient values depended on the proper generation of an AC virtual ground at the source of M_1. Therefore, the main design condition for the current buffer was the value of its input impedance Z_{in}, to properly collect the AC current coming from the loop filter: $Z_{in} < R_{f1}||R_{f2}$. The small signal model for the input impedance calculation of a conventional common gate transistor is shown

in Fig. 4.9a, the input impedance is approximately the inverse of the transconductance of M_1, $Z_{in} \approx 1/g_{m1}$. Fig. 4.9b shows the small signal for the input impedance of the used current buffer, as shown the effect of the transconductance of M_2 needs to be included, the input impedance can be approximated as

$$Z_{in} = \frac{V_s}{I_{in}} \approx \frac{1}{g_{m1} \cdot \left(1 + g_{m2} \cdot \left(\frac{R_{fb}}{1 + A_3(s)}\right)\right)} \tag{4.10}$$

As shown in equation (4.10) g_{m2} is multiplied by the input impedance of the feedback TIA, this product can reduce the input impedance of the buffer. Since the input impedance of the feedback TIA was designed to be small at high frequencies the product was a small number, but even a relatively modest product of 1~2 can help since g_{m1} can be relaxed by the same factor. Thus, power and area were saved in the implementation of the current buffer.

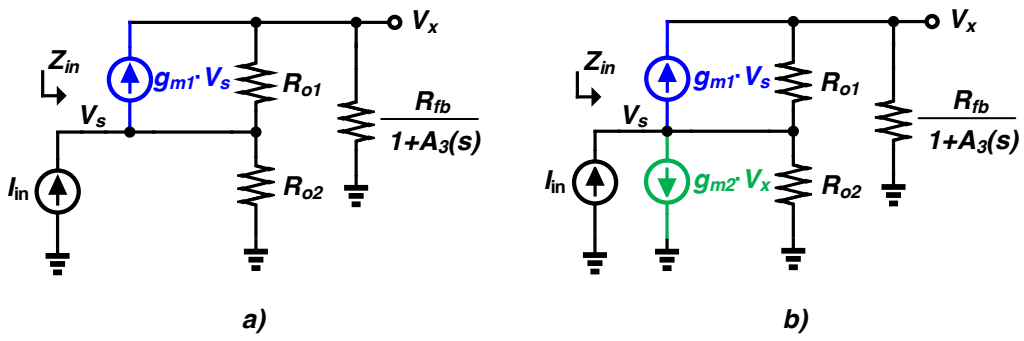


Fig. 4.9: Small signal model: a) common gate buffer and b) common gate buffer with bias transistor diode connected.

4.4.3. Filter's operational amplifier

The filter's OpAmps were implemented employing a two-stage topology with feedforward compensation for high frequency operation [43]. Fig. 4.10 shows the schematic of the OpAmp, the input stage formed by $M_{1\text{-}9}$ is a cascode architecture to provide high gain, the common mode feedback is self-biased using $R_{1,2}$ and $C_{1,2}$. Transistors $M_{12\text{-}13}$ implemented the second stage, and transistors $M_{10\text{-}11}$ implemented the feedforward coefficients with a pseudo-differential pair that reuses the current used is $M_{12\text{-}13}$. The feedforward signal is AC-coupled to optimize the bias conditions of the feedforward transistors. Active common-mode feedback is used in the second stage to have a better control on the output common mode level. The design was optimized for high bandwidth and noise performance. A_1 consumes a total of 5.9 mW including the common-mode OpAmp. The gain and phase response of A_1 are shown in Fig. 4.11, the first OpAmp provides a DC gain of 46 dB with a GBW of 7.8 GHz and a phase margin of 81 degrees; the compensating zero is visible over 2GHz. A_2 is a scaled version of A_1 and consumes a total power of 1.9 mW.

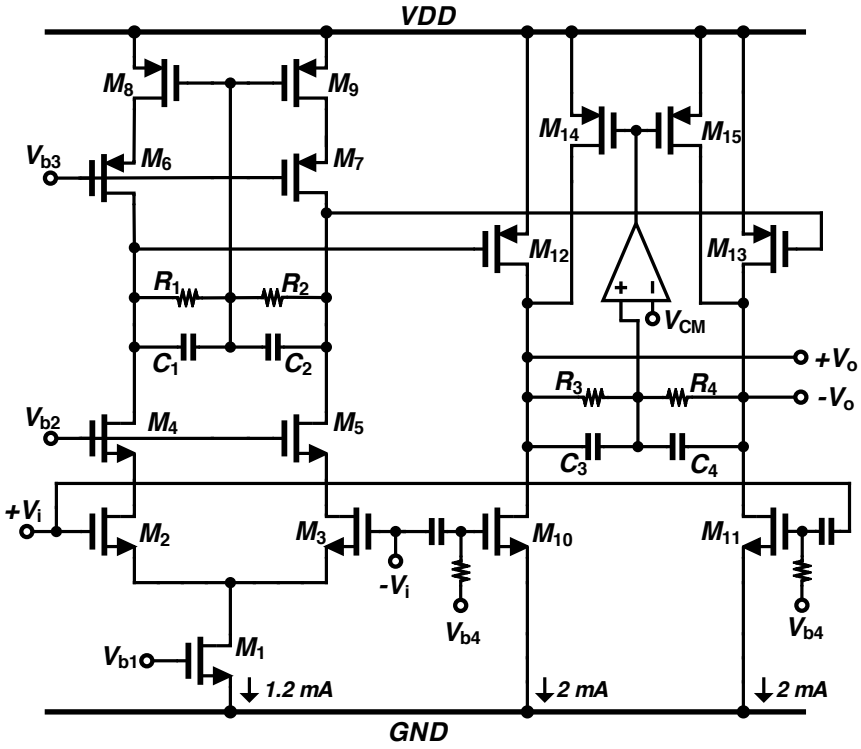


Fig. 4.10: Two stage OpAmp used in the analog loop filter.

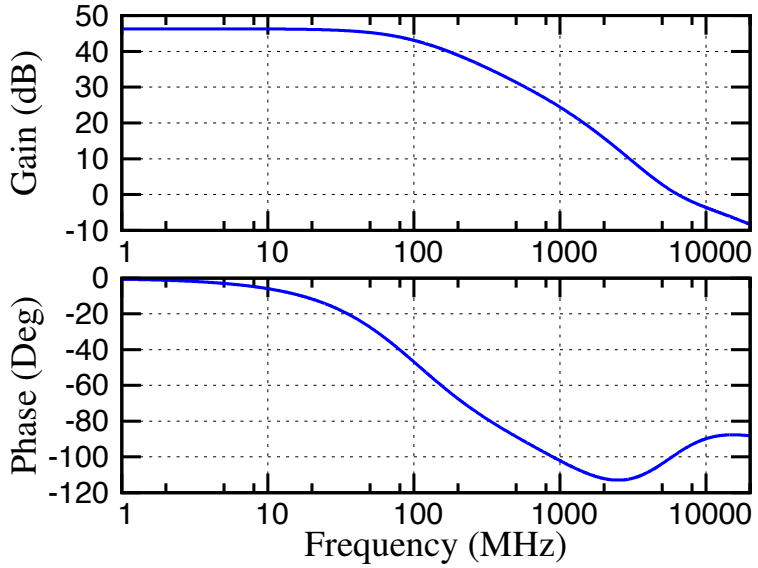


Fig. 4.11: A_1 gain and phase response.

4.4.4. Current steering DAC

The 4-bit main feedback DAC (MDAC) employs 15 cells of pMOS cascaded current source $M_{1,2}$ and a pair of current-steering switches $M_{3,4}$ as shown in Fig. 4.12. This configuration proves to be efficient due to its simplicity and ease of implementation. Each current source cell $M_{1,2}$ is designed to carry a nominal current of 67 μA (1 I_{LSB}). The current source device, M_1 was sized to achieve a device matching of 0.2% (1σ). Transistor M_2 was included to increase the output resistance of each cell and to decouple the large parasitic capacitor of M_1 from the current steering-switches $M_{3,4}$ for high speed operation. A pair of nMOS cascaded current sources $M_{5,7}$ and $M_{6,8}$, were each designed to carry a nominal current of 500 μA (7.5 I_{LSB}), which will ensure an equal common-mode level between CTΣΔM's input and DAC's output. With 500 Ω of CTΣΔM's input resistors, the equivalent CTΣΔM's full-scale differential input range is 1 V_{pp}.

The current-steering switches $M_{3,4}$ are designed to operate in saturation region to improve DAC output impedance. In addition, these transistors are driven by a low-crossing switch driver [44] to ensure that none of them turns off completely during switching. This design choice minimizes feedthrough current from parasitic gate to drain capacitances C_{gd} of $M_{3,4}$. DAC's current glitch and finite transition time also introduce input dependent dynamic error. Similar to DAC's static mismatch, DAC's dynamic mismatch generates harmonic distortion components. The main difference is that the tones generated by this non-ideality are shaped to first-order by the NRZ transfer function of $1 - z^{-1}$. Therefore, it is important to minimize this effect. FDAC is a scaled version of MDAC, the individual cells current and area were reduce by a factor of 9.

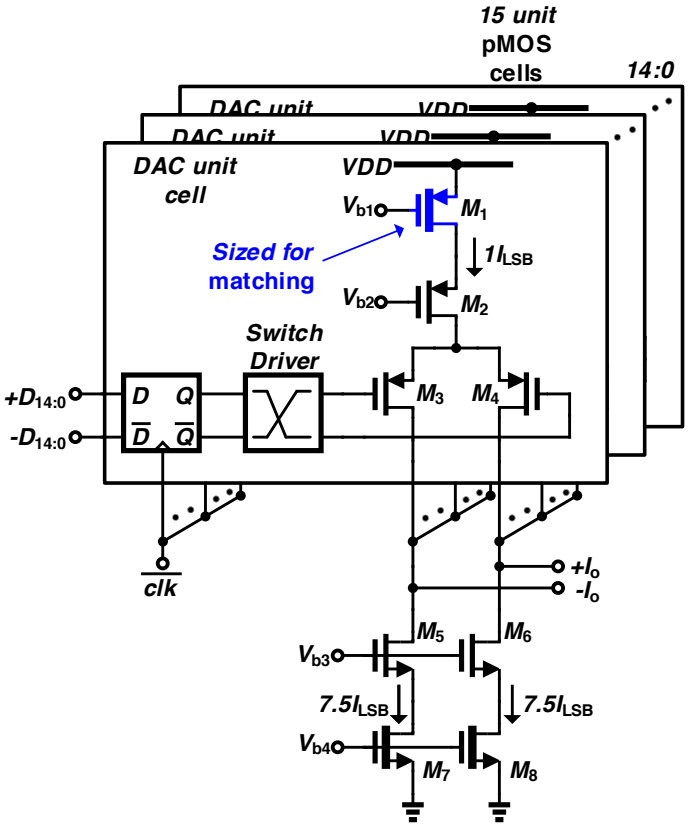


Fig. 4.12: Current steering MDAC and FDAC implementation

4.4.5. 4-bit quantizer

The 4-bit quantizer incorporates a flash-type ADC running at 3.2 GHz sampling frequency. The flash converter consists of 15 identical slices, as depicted in Fig. 4.13. Each slice is composed of a pre-Amplifier, a strong-Arm comparator and an SR-Latch. The pre-Amplifier compares the input to one of 15 differential reference levels, generated by a ladder-type resistive DAC. The value of the unit resistor is selected such that it minimizes the reference ripples to below one four of the LSB level. Kick-back

noise from the sampling clock is further attenuated by the pre-Amplifier, which provides isolation between the input and the sampling stage. The pre-Amplifier input pair sizing is selected to minimize the effect of offset, and cross-connection of differential inputs and reference inputs are used to minimize common mode variations at the comparator input.

The comparator used here is a strong-Arm latch [45], followed by a balanced SR-Latch [24]. The comparator architecture is selected to achieve optimal delay-power tradeoff, where the comparator consists of one stage that preforms both signal amplification and latch re-generation. Since the quantizer is in the modulator's high speed feedback path and to fulfill loop stability requirements, the signal delay through the quantizer needs to be less than 125 ps. Therefore, low threshold transistors are employed in the design to achieve this delay requirements.

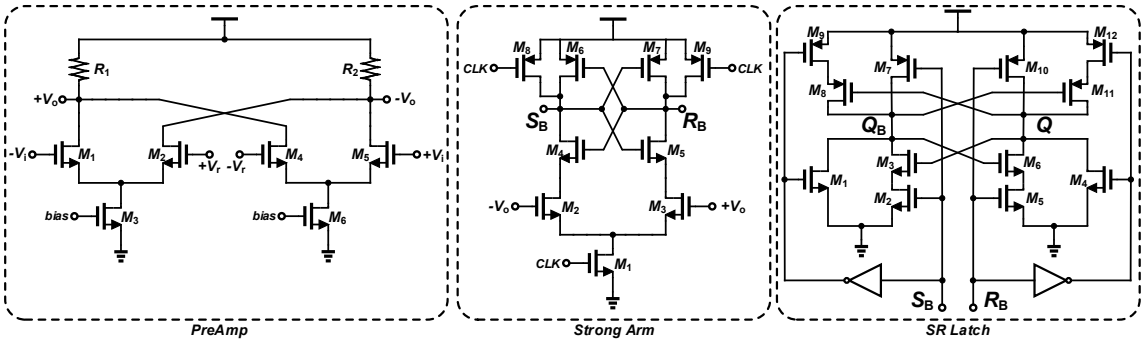


Fig. 4.13: 4-bit quantizer building blocks.

4.4.6. Noise budged considerations

In order to achieve the targeted SNR the noise level must be dominated by quantization rater that thermal noise. The ideal SNR defined by system level simulations was 68 dB. Therefore, design considerations need to be made to avoid having a noise level dominated by thermal or other non-idealities.

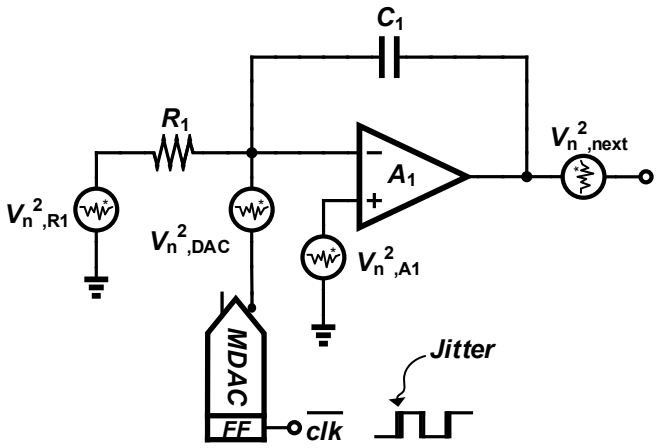


Fig. 4.14: Sigma delta main noise contributors.

In a CTΣΔM to properly predict the final performance in terms of SNR we have to consider the amount of quantization noise and also include the sources of noise from Fig. 4.14. The main sources of noise are described as follows:

1. Quantization noise: This is the amount of in-band quantization noise, is known this is defined by the properties of the loop (Loop order, OSR), is desired have this noise as the dominant.
2. *Jitter*: The effect is introduced by the clock signal at the main feedback DAC. The control of this depends on the proper design of the clocking system.
3. R_1: The noise contribution depends on the value of the input resistor, the value of the resistor needs to be properly selected to avoid increasing the complexity of other building blocks.
4. *DAC*: Depends on the amount of transconductance in the current sources.
5. 1st OpAmp: Is the input noise referred of the first OpAmp A_1.
6. Next stages: Is the contribution of the next stages, this noise is reduced by the gain of the first opamp, but is good to consider this if we want to relax the design of the next stages.

The calculation and noise budged for each of the main sources of noise shown in Fig. 4.14 is described next.

The in-band noise level normalized by the CTΣΔM's fullscale power due to loop filter's input resistors R_1 and OpAmp A_1 thermal noise contribution is given by

$$V_{n1}^2 = \frac{8 \cdot k \cdot T \cdot R_1 \cdot BW}{V_{fs}^2} \cdot \left(1 + \frac{\frac{V_{n,A1}^2}{BW}}{8 \cdot k \cdot T \cdot R_1} \right) \tag{4.11}$$

where k is the Boltzmann constant, T is temperature is Kelvin , R_1 is the input resistance of 500 Ω, BW is the signal bandwidth of 75 MHz, V_{fs}^2 is the CTΣΔM's fullscale power of 0.125 V_{rms}^2 for maximum differential sinusoidal input signal, and $V_{n,A1}^2$ is the input referred of A_1. The total noise contribution from R_1 and A_1 in this design was -84 dBFS.

The in-band noise level due to MDAC's thermal noise is given by

$$V_{n1}^2 = \frac{8 \cdot k \cdot T \cdot R_1 \cdot BW}{V_{fs}^2} \cdot \gamma \left(\frac{V_{fs}}{V_{GS1} - V_{TH}} + \frac{V_{fs}}{V_{GS7,8} - V_{TH}} \right) \tag{4.12}$$

where γ is the transistor's thermal noise constant, $V_{GS1} - V_{TH}$ and $V_{GS7,8} - V_{TH}$ are the overdrive voltages of the current source transistors for each DAC cell and the bias transistors. According to (4.12), MDAC contributes more noise power than that of the input resistor R_1 by a factor proportional to $\frac{V_{fs}}{V_{GS1}-V_{TH}}$. This factor is typically in the range 2.5 to 3. The noise contribution from MDAC was -77 dBFS.

The noise contribution from the other resistors and OpAmp in the loop filter can be ignored due to the large in-band provided by A_1.

A graphical representation of the total noise budget is shown in Fig. 4.15.

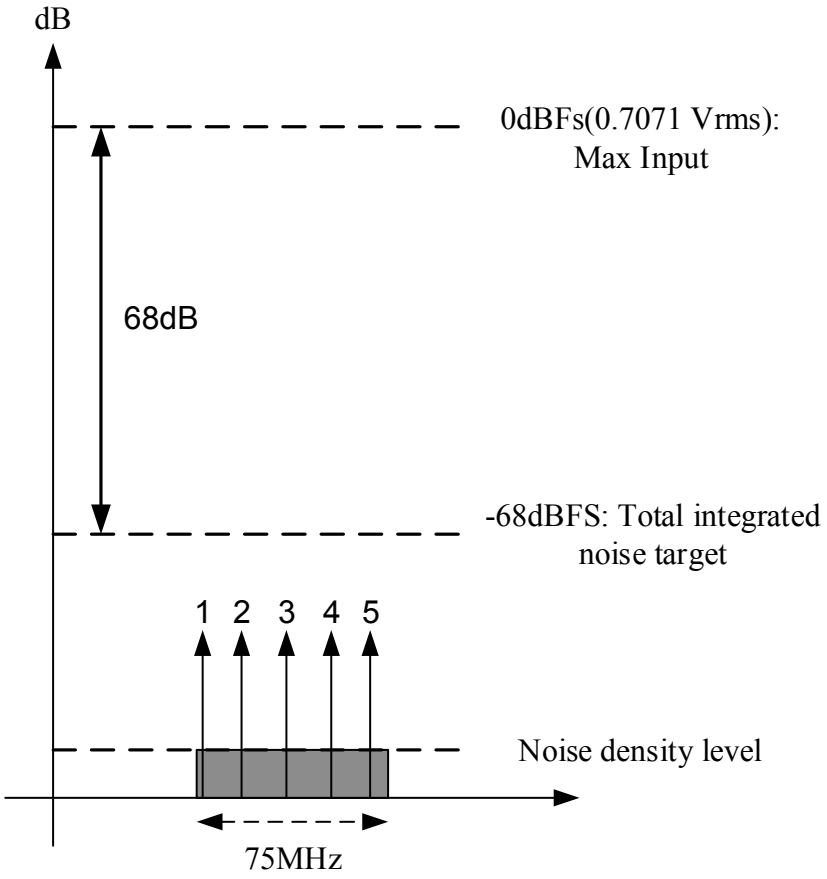


Fig. 4.15: Sigma delta total noise budget.

4.5. Measurement results

A prototype of the proposed CTΣΔM was fabricated in a 40 nm LP8M process. The chip microphotograph is shown in Fig. 4.16, the chip active area is 0.09 mm^2. Fig. 4.17 shows the measurement setup. On-board low dropout regulators were used to generate a low noise 1.1 V reference for the analog and digital blocks. The test input signal was generated form an Agilent® 33250A signal generator, passive bandpass filters were used to minimize the noise contribution from the signal generator. A low jitter 3.2 GHz differential clock signal was provided from an Agilent® N4965A, the instrument provides a low swing clock and rms jitter of around 0.8 ps, the signal is converted internally to full CMOS levels. The four bit data comes out of the chip at the 3.2 GHz clock frequency, transmission lines were carefully designed to ensure good data integrity. LVPECL output drivers were implemented on chip to drive the four channels of an Agilent® DSA91304A digital signal analyzer with 40 GS/s maximum operation rate. The data was captured and post-processed using MATLAB®.

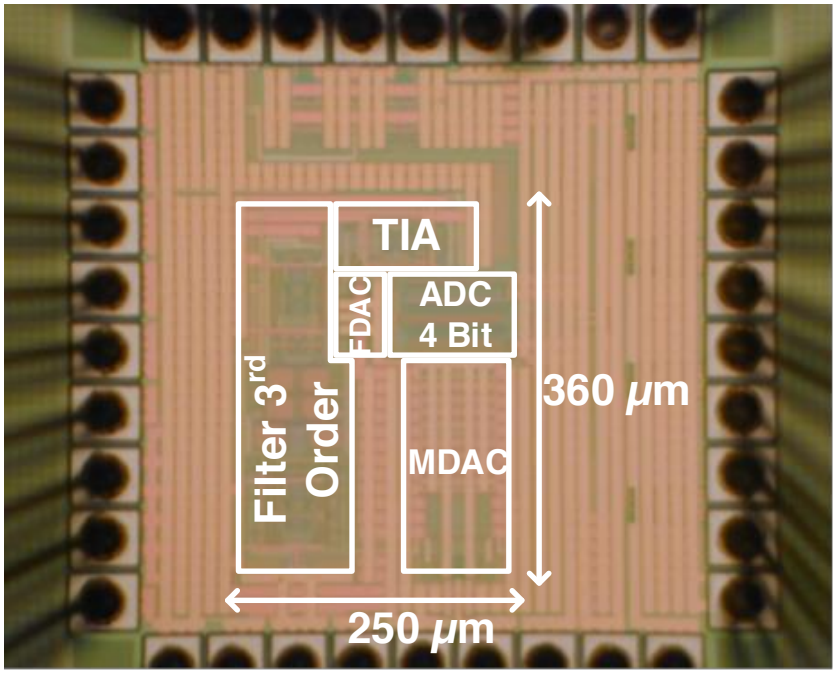


Fig. 4.16: Chip microphotograph.

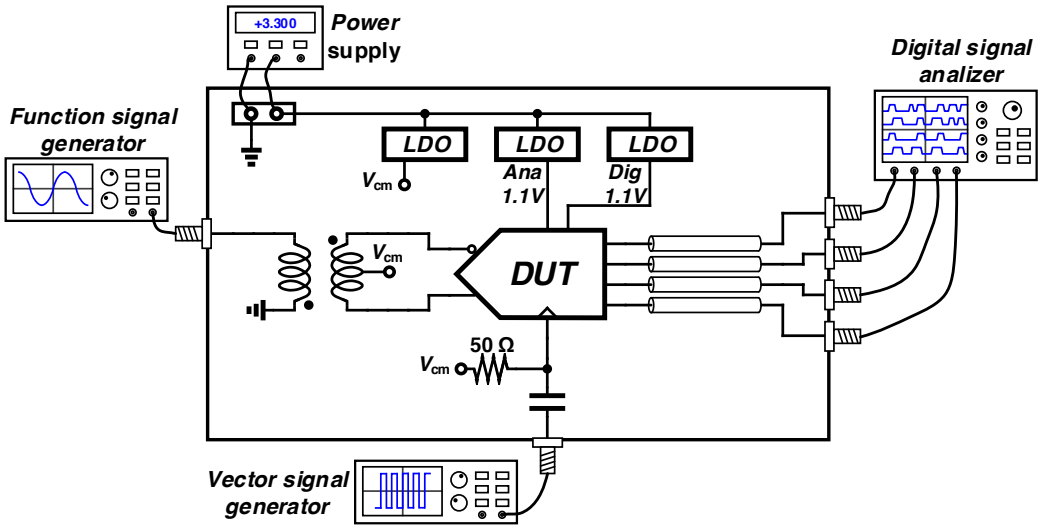


Fig. 4.17: ADC measurement setup.

The modulator consumes 22.85 mW, most of this power is consumed by the input integrator and quantizer. Fig. 4.18 shows the measured output spectrum of the modulator for a 10.5 MHz input signal with -1 dBFS input power. The measured SNDR over the 75 MHz BW was 64.9 dB, and the Total Harmonic Distortion (THD) is -74.5 dB. According to these results, the modulator's performance is limited by thermal and quantization noise with an SNR of 65.5 dB. Fig. 4.19 shows the modulator's performance for a higher frequency input, a 48.5 MHz with -1 dBFS input tone was used. The output power spectrum for out of band very small input signal is overlaid in Fig. 4.19. The noise floor level is almost the same for both cases, the only difference is around the frequency of the tone, and visible in the zoomed area. The skirt around the input signal frequency has the bandwidth of the used passive bandpass filter. Thus, we can consider that skirt noise is coming from the signal generator.

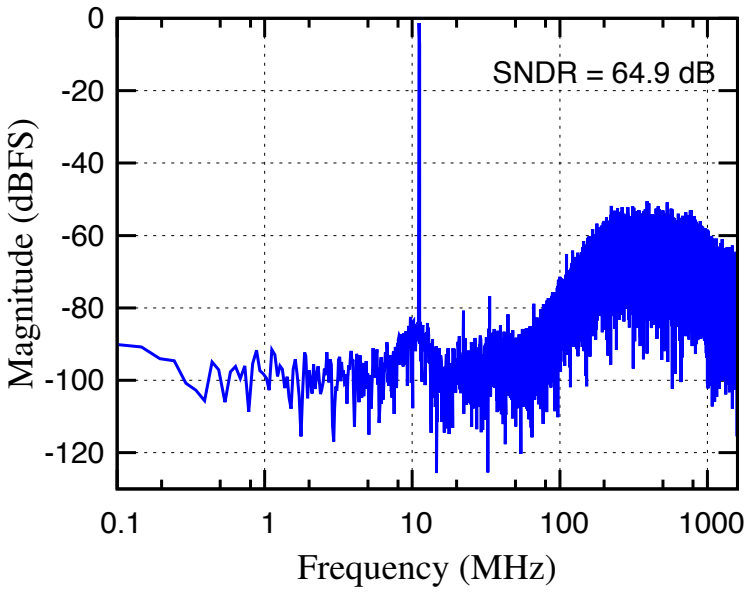


Fig. 4.18: Measured output spectrum with -1 dBFS at 10.5 MHz input signal.

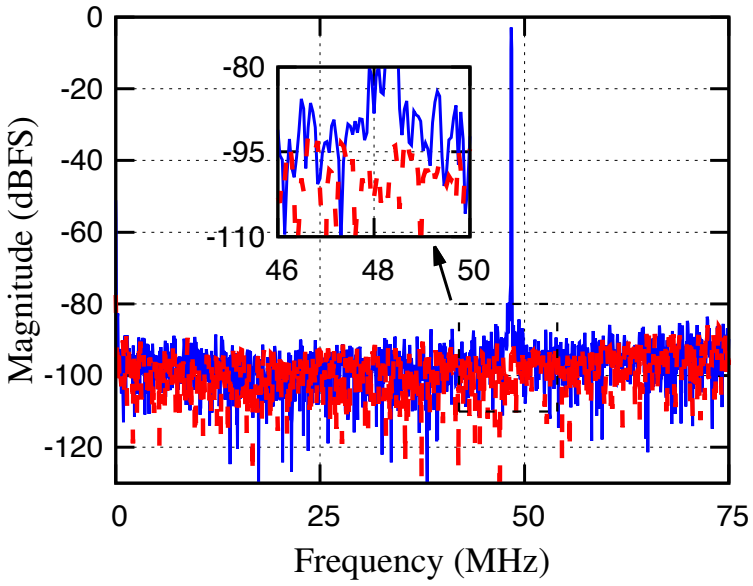


Fig. 4.19: Measured output spectrum with -1 dBFS at 48.5 MHz input signal vs no input signal.

The linearity of the loop and MDAC is tested employing the two-tone test at 10 and 11 MHz, as depicted in Fig. 4.20. Each tone magnitude was -7 dBFS, and the measured IM3 was -73 dB, if a higher resolution is required it will demand more silicon area from MDAC to suppress nonlinearity or include calibration. Fig. 4.21 shows a comparison of the SNR and SNDR performances with respect to input signal power. As expected, since the system is limited by noise, the SNDR plot has a maximum degradation of less than 1 dB. Spurious free dynamic range is around 70dB. Table 4.1 summarizes the performance of the fabricated chip and compares the results with recent state-of-the-art publications for CTΣΔM's with BW > 50 MHz. This work presents the best Walden's FoM (FoM_1) reported for uncalibrated broadband CTΣΔM implementations, and without any off-chip data post processing.

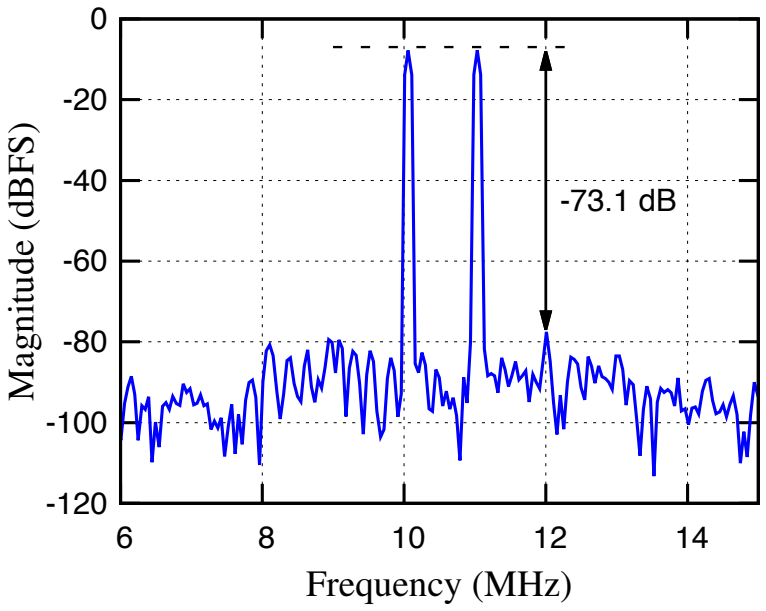


Fig. 4.20: Measured output spectrum with two tone test.

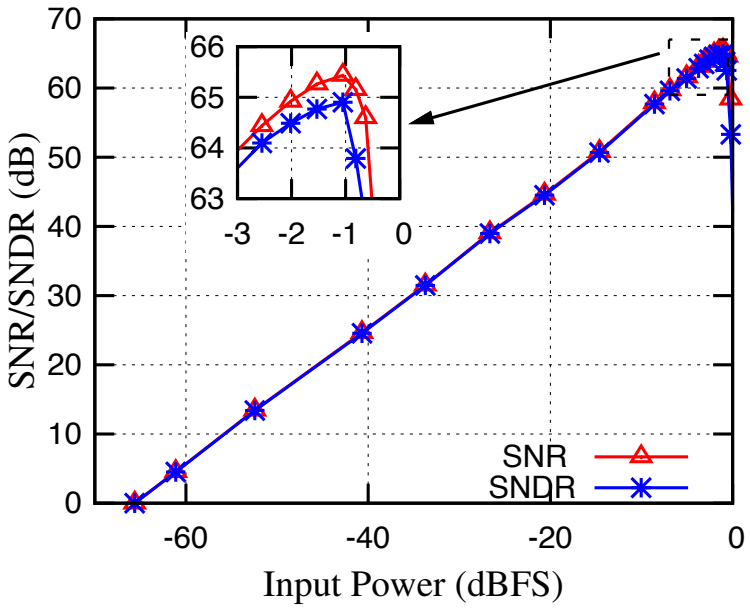


Fig. 4.21: SNR/SNDR vs input signal power.

Table 4.1: Results summary and comparison 75 MHz ΣΔ.

Publication	**This Work**	[12] JSSC11	[31] ISSCC12	[30] JSSC12	[10] JSSC14	[34] JSSC15	[9] ISSCC15
Architecture	**Single**	Single	Single	Single	MASH	Single	MASH
Process (nm)	**40**	45	45	65	28	20	28
Order	**3**	4	3	6	0-3	4	3-1
FS (GHz)	**3.2**	4	6	4	3.2	2.184	1.8
BW (MHz)	**75**	125	60	75	53.3	80	50
SNR(dB)	**65.5**	65.5	61.5	--	83.1	70	76.8
SNDR (dB)	**64.9**	65	60.6	--	71.4	67.5	74.9
VDD (V)	**1.1**	1.1/1.8	--	1.0/2.5	0.9/1.8/-1	--	--
Power (mW)	**22.8**	260	20	750	235	23	80.4
Area (mm^2)	**0.09**	0.9	0.49	5.5	0.9	0.1	0.34
FoM_1 (fJ/conv bit)	**106**	715	190	--	726	74.2*	177
FoM_2 (dB)	**161**	157	160	159	171.6	168	172.9
FoM_3 (dB)	**160**	152	155	--	155	163	171

*After off-line digital calibration

$FoM_1=Power/(2\cdot BW\cdot 2^{(SNDR-1.76)/6.02})$

$FoM_2=DR+10\cdot\log_{10}(BW/Power)$

$FoM_3=SNDR+10\cdot\log_{10}(BW/Power)$

4.6. Conclusion

In this chapter, we have demonstrated a power efficient CTΣΔM. The proposed implementation of a conventional fast-path ELD compensation allows the implementation of low power circuits that can perform at GHz sampling frequencies.

The implementation of a traditional active fast path that can provide gain, allowed the reduction of analog power consumption from the loop filter. The proposed summing amplifier with current buffer demonstrates that close loop amplifier operating at gigahertz frequencies can be implemented with low power consumption. The same approach could be used in other implementations. The modulators characterization demonstrates that the achieved results are comparable with previously reported state-of-the-art. The system level design used a conservative out of band gain of 1.8, it is expected that even better results could be achieved by using a higher out of band gain especially in terms of noise floor.

V. LOW POWER PIPELINE ADC WITH CURRENT MODE MDAC

5.1. Introduction

The increase in the demand of analog-to-digital converters (ADCs) with higher bandwidth and higher resolution has come with the motivation for RF sampling. Systems can have lower costs and substitute analog operations that are sensitive to Process-Voltage-Temperature (PVT) variations, with more robust digital operations.

Nowadays, the target is to achieve sampling rates in the range of hundreds of mega-hertz range. Pipeline ADC architectures can be considered the fastest after flash ADC architectures. Therefore, research has focus on improving the performance of the pipeline ADC by increasing the frequency of operation, then reducing the power consumption and use of non-linearity calibration algorithms to improve the resolution. Recently, it has been demonstrated that by resolving more bits in the first stage [46-48], analog power reduction can be achieved. This is possible because the resolution requirements for the back-end of the pipeline are relaxed.

This chapter presents the design and implementation of a pipeline ADC that uses a multibit front end implemented with a current mode residual amplifier, which substitutes the traditional capacitive multiplying digital-to-analog converter (MDAC). The Operational Amplifier (OpAmp) power consumption and bandwidth requirements are significantly reduced compared with a traditional MDAC implementation. Likewise, the capacitive mismatch calibration typically required for capacitive multibit MDAC is avoided with the proposed architecture.

5.2. Pipeline ADC architecture

A pipeline ADC architecture is composed of n successive stages as shown in Fig. 5.1. Since the complexity of a flash ADC increases exponentially, this architecture is often impractical for resolutions higher than 7 bits. Pipeline ADCs can achieve better resolution with less power and area requirements at the expense of latency for the output data, which depends on the number of stages. Each stage is composed by a sub-ADC, a sub-DAC, and a residual amplifier. The input signal is digitized by the sub-ADC and the output drives the sub-DAC that reconstructs the input signal. The residual voltage (V_{res}) is obtained by subtracting the input signal from the analog reconstructed version and is amplified by the gain of A_0 to increase the swing of the residual voltage and relax the design specification requirements for the back-end stages.

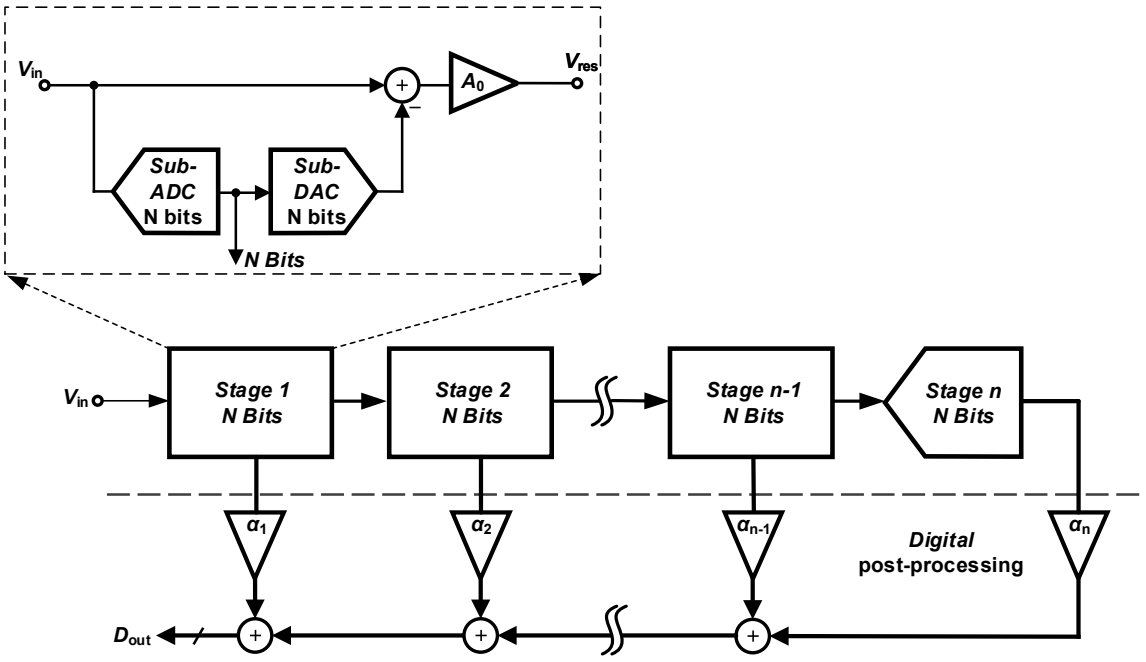


Fig. 5.1: Pipeline ADC architecture.

The specifications on the bank-end stages can be successively relaxed as the most significant bits are solved. Power consumption and area can be reduced exponentially on the back-end. Therefore, most of the precision and power consumption is depicted in the first stage, which demands an OpAmp with large gain and bandwidth, and requires high-linearity from the DAC. For proper operation, the precision from the OpAmp needs to be better than half least significant bit (LSB) from the back end resolution. Therefore, for a 1.5 bit per stage architecture with a target resolution of 10 bit or better becomes the bottleneck in terms of power consumption, which requires a precision of better than 1/1024. Likewise, the linearity from the OpAmp and the DAC will limit the final resolution of the ADC.

Foreground and background calibration techniques have been implemented to resolve some of the mentioned challenges. Most of these calibration techniques address one individual problem at a time, and need to be running constantly to warrantee robustness over PVT variations. By moving to higher sampling rates, the power consumption from the digital engines needed for calibration will increase. Therefore, it is still desired to optimize the system level design of the ADC to inherently avoid the introduction of nonlinearities and minimize the amount of digital calibration.

5.3. Multibit multiplying DAC

When trying to reduce the power consumption and required calibration, increasing the number of bits resolved per stage in a pipeline ADC could be desired. The precision from the multiplication OpAmp in the first stage is automatically relaxed according to the number of bits solved in the first stage. However, the complexity of a multibit sub-stage implemented with a flash architecture increases exponentially and complicates the design. Thus, there will be a maximum practical limit for the number of bits that can be used in the first stage. Moreover, the linearity from the MDAC becomes more critical, since the number of capacitors required also increases exponentially with the number of bits, thus increasing the digital calibration required to address this problem. Therefore, system-level design techniques can be proposed to improve the performance of each pipeline stage.

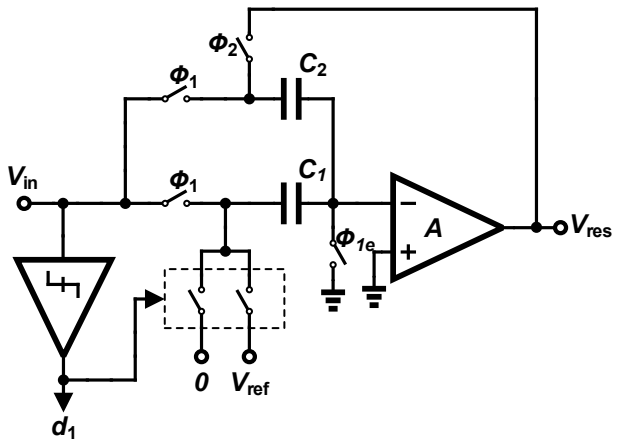


Fig. 5.2: 1-bit MDAC architecture.

Pipeline ADCs normally merged the sub-DAC and residual multiplier in to a single MDAC as shown in Fig. 5.2. A 1-bit flip around MDAC architecture shows how the circuit operates in two phases. During the first phase (ϕ_1), capacitors C_1 and C_2 sample the input signal, at the same moment that the signal is sampled and the comparator is activated to determine the polarity of the input signal. In the second phase (ϕ_2), C_2 will be flipped around and connected in feedback with the OpAmp (A), C_1 will be connected to the proper reference voltage determined by the comparator or 1-bit ADC, through charge recombination the OpAmp will amplify the residual and produce V_{res}.

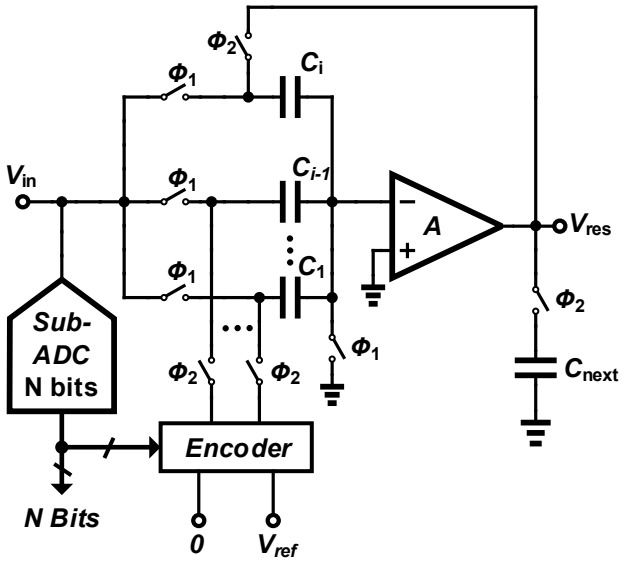


Fig. 5.3: N-bit MDAC architecture.

The implementation of a multibit MDAC is shown in Fig. 5.3. The complexity from the flash sub-ADC and capacitive DAC increase exponentially by 2^N, for the flash. Besides the increase in area and power consumption, another critical criteria to be consider is the offset from the comparators, which generate more demanding specifications if N is increased. A practical value with reasonable area and power consumption is N = 4. The offset problem from the comparators can be solved with redundancy in the back-end as it will show in the following section. On the contrary, the increase in complexity by the capacitive DAC generates errors that are not easy to solve just with the use of traditional design techniques. The multibit MDAC requires 2^N capacitors, therefore, the complexity of the layout increases and the expected matching is usually not enough for high performance ADCs. Mismatch between capacitors can

generate different levels of gain for each of the output codes from the flash ADC that can result in undesired harmonic components. Therefore, complex digital calibration algorithms are required which are usually not suitable for low power design.

The MDAC's gain selection is also critical for power consumption. As the number of bits solved in the first stage increases, the expected residual voltage is smaller, but a small output swing for V_{res} increases the complexity and power consumption of the back-end, since more precision is required. Likewise, input capacitance from the back-end needs to satisfy *KT/C* requirements, therefore, the loading in the first stage has to be considered when budgeting amplifier's power. If the output swing for V_{res} is increased to reduce the effect of the aforementioned problems, the feedback factor (β) of the OpAmp in the first stage will be reduced, leading to an increase on the specifications for the OpAmp. The tradeoffs between number of bits per stage and gain from the MDAC will be addressed latter in this section, prior to the proposed current mode architecture.

5.4. MDAC gain and feedback factor

To properly estimate the power savings, the design specifications for the OpAmp need to be defined in terms of the number of bits per stage. The output residual voltage can be defined as

$$V_{res} = \frac{V_{ref}}{2^N} \cdot A_{MDAC} \tag{5.1}$$

where V_{ref} is the reference voltage or full scale signal swing at the input of the first stage, N is the number of bits solved in the stage, and A_{MDAC} is the gain from the MDAC, that for a N-bit per stage architecture shown in Fig. 5.3 can be defined as

$$A_{MDAC} = \frac{\frac{(C_1 + C_2 + \cdots + C_{i-1})}{C_i}}{1 + \frac{1}{A} \cdot \frac{(C_1 + C_2 + \cdots + C_{i-1})}{C_i}} \tag{5.2}$$

where A is the open loop gain of the OpAmp, the total number of capacitors is defined by $i = 2^N$. The value for each unit capacitor can be obtain from the total input capacitance defined by thermal noise requirements, as shown in the next equation

$$C_T = C_1 + C_2 + \cdots + C_{i-1} + C_i \tag{5.3}$$

In this equation, C_T is the value of the total input capacitance defined by *KT/C* thermal noise level. The close loop gain can be adjusted by changing the ratio of the capacitor connected in feedback with respect to the remaining capacitors that are connected to the proper reference voltage by the sub-ADC.

The specifications for the OpAmp A depend on the maximum allowed settling error for V_{res}, which is defined by the resolution of the back-end evaluated at the end of the evaluation period, and can be defined as

$$V_{res-error} = \frac{1}{2^{N_B}} = -e^{-GBW \cdot \beta \cdot T_{CLK}/2} \tag{5.4}$$

where *GBW* denotes the gain bandwidth product from the OpAmp, β is the feedback factor ($\beta = C_i / C_T$), t is the allowed time for settling, and N_B is the resolution of the back-end. Knowing that *GBW* is equal to the transconductance of the OpAmp divided the load capacitance (C_L), the minimum transconductance need is defined by equation (5.5).

$$g_m = \frac{2 \cdot f_s \cdot ln(2) \cdot N_B \cdot C_L}{\beta} \tag{5.5}$$

$$C_L = \frac{C_T \cdot (1 - 2^{-N})}{A_{MDAC} + 1} + \frac{C_T}{A_{MDAC}^2} \tag{5.6}$$

In equation (5.5), f_s is the targeted sampling frequency, and the factor of 2 in the denominator is include assuming that we only have half clock cycle for the signal to settle. Equation (5.5) shows that as expected, if more bits are solved in the first stage, the

value for N_B will be smaller. Therefore, the transconductance needed for the OpAmp in the first stage will reduce. The effect of V_{res} swing and the closed loop gain in the transconductance is included in C_L and β. If the swing is smaller the value for C_L will increase due to thermal noise restrictions, C_L is composed by the combination of the loading effect of the capacitor in feedback and by the input capacitance of the next stage as

In equation (5.6), the first part of the equation is the loading effect with respect to the total capacitance at the input of the ADC, the number of bits solved in the first stage and the closed loop gain. The second part of the equation represents the input capacitance from the next stage defined by the thermal noise level allowed at the back-end and defined by the input capacitance and the closed loop gain of the first stage. Equation (5.6) shows that a larger closed loop gain in the first stage will reduce the loading capacitance from the OpAmp. However, equation (5.5) also shows how the effect of β can reduce in some portion the benefits of having large closed loop gain, since β is inversely proportional to A_{MDAC}.

Fig. 5.4 shows the transconductance required by the OpAmp with respect to the number of bits. The result is normalized by the transconductance of a 1.5-bit per stage. Also, for each case MDAC is adjusted to have a swing of $V_{res} = V_{ref}/2$. In practice flash ADC with more than 4-bit will increase the complexity of the sub-ADC significantly.

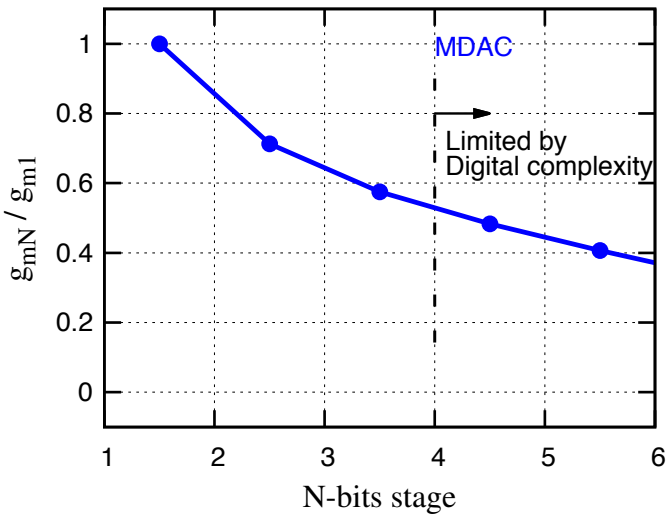


Fig. 5.4: OpAmp transconductance vs number of bits per stage (normalized to 1-bit).

5.5. Optimum MDAC gain and redundancy

It has been demonstrated that increasing the A_{MDAC} and the swing of V_{res} will help reduce power in the first stage [47]. Also, the power consumption from the back-end is reduced since the precision of the components is relaxed. The swing can be defined by how much redundancy from the next stage circuitry wants to be included to tolerate the non-idealities from the sub-ADC in the first stage. Fig. 5.5 shows an example for transfer characteristics output curve; normally having a redundancy of half V_{ref}. This is an optimum value to have enough room to compensate for any non-idealities. For a flash ADC the main source of non-ideality is the offset from the comparators. Thus, the random offset will create un-equal LSB steps at the output of the flash ADC, this makes that V_{res} surpasses the output range defined by the ideal case as shown in Fig. 5.6. If swing of half V_{ref} is wanted, the V_{res} dependency to the number of bits is $A_{MDAC} = 2^{N-1}$.

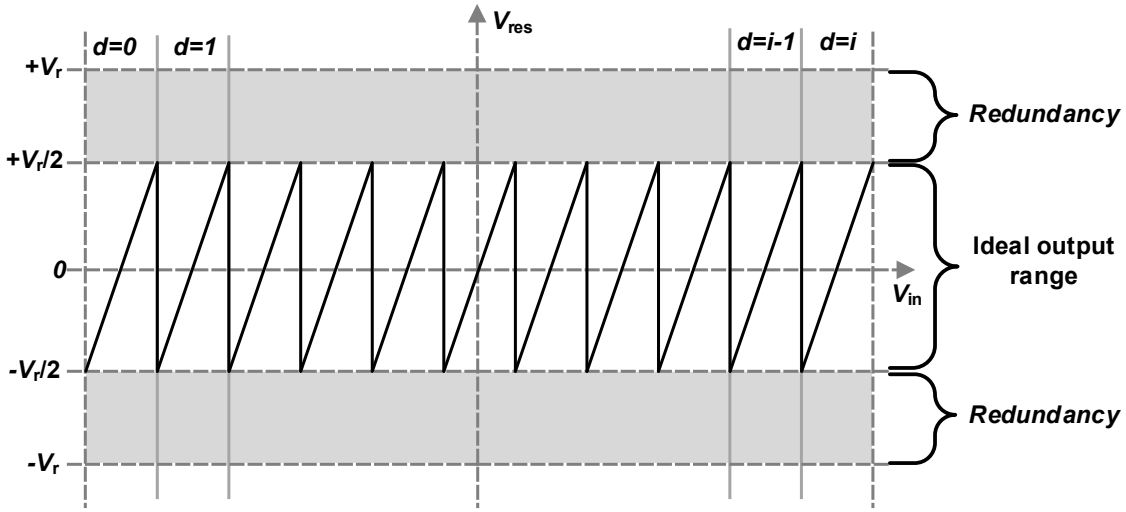


Fig. 5.5: V_{res} with redundancy ideal sub-ADC.

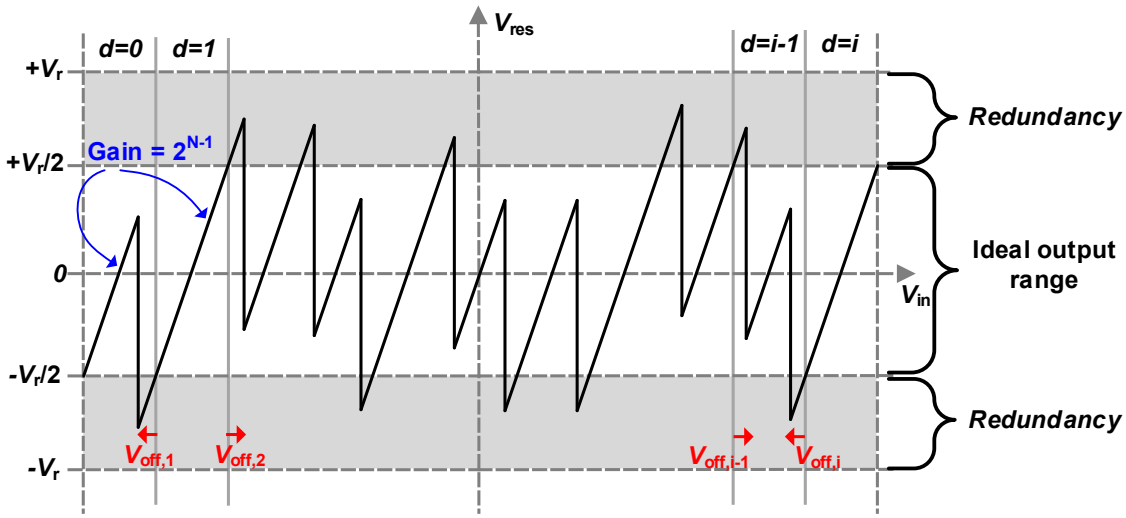


Fig. 5.6: V_{res} with redundancy, sub-ADC comparators with offset included.

It is preferred to solve offset problems with redundancy, since trying to reduce the offset from the comparator requires individual calibration and will demand a large area that can increase the power consumption and reduce the speed of the comparator.

5.6. Proposed current mode sub-ADC architecture

Multibit per stage pipeline ADCs proved to be a good option for power consumption reduction. Due to the demand of high integration on systems, new techniques need to be proposed to achieve new power consumption levels. Equation (5.5) showed that the feedback factor is a limiting factor to achieve low power consumption.

Fig. 5.7 shows the proposed current mode stage. The main goal is to decouple the dependency of the power consumption of the OpAmp feedback factor. The circuit is composed of a flash ADC, the DAC uses a current steering architecture that takes the digital version of the input signal from the flash ADC and generates the analog current version.

The input voltage signal is converted in to a current by an operational transconductance amplifier (OTA), the residual signal information is obtained by the difference of the current from the OTA and the current steering DAC. The circuit finally uses a feedback transimpedance amplifier (TIA) to convert the residual current into residual voltage V_{res} to drive the back end. The circuit uses a sample and holds in front of each stage to sample the voltage signal at the proper time. The sample and hold reduces the errors that can be introduced in the calculation of the residual voltage due to the

delay from OTA path, and the flash and current steering DAC path. The residual voltage definition is

$$V_{res} = (V_{in} \cdot G_m - I_{dac}) \cdot A_{TIA} \tag{5.7}$$

where G_m is the gain from the OTA, I_{dac} is the output current from the current steering DAC, and A_{TIA} is the transimpedance of the TIA.

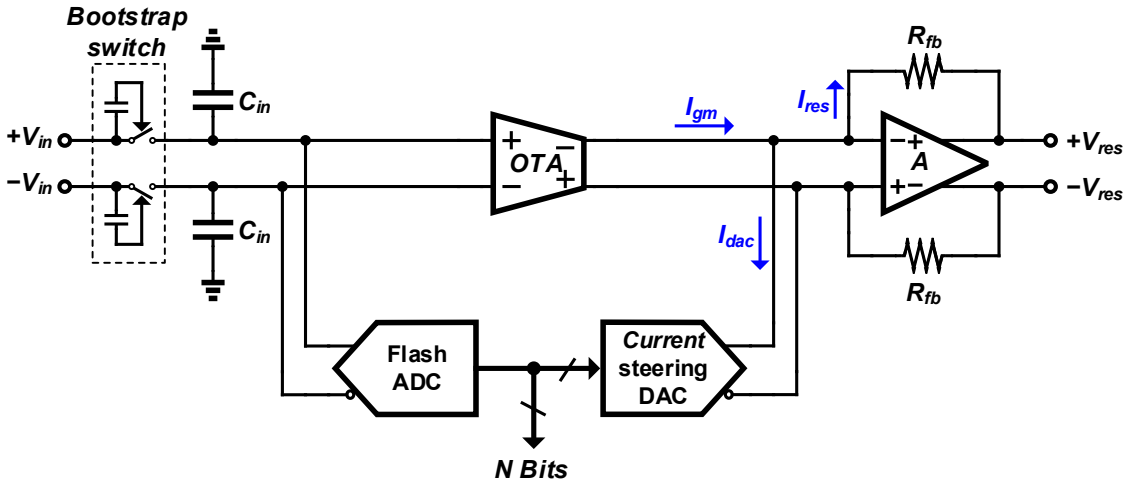


Fig. 5.7: Proposed current mode pipeline stage.

This architecture reduces the effect of the feedback factor. Since the output of the OTA and current steering DAC provide high output impedance, the effective feedback

factor for the OpAmp (A) is close to unity. Since the effect of β is close to unity equation (5.5) can be reduced to

$$g_m = 2 \cdot f_s \cdot ln(2) \cdot N_B \cdot C_L \tag{5.8}$$

Also, since the TIA is implemented with a resistor in feedback, C_L will be mainly composed only by the loading of the following stage. Thus, equation (5.6) is reduced to

$$C_L = \frac{C_T}{A_{MDAC}^2} \tag{5.9}$$

The reduction in loading capacitor is around 66% compared with the one found in the traditional MDAC architecture. The feedback can load the OpAmp if the value is small or comparable with the output resistance of the OpAmp, yet this effect will produce only gain error, which is easier to correct than settling error.

Fig. 5.8 shows a comparison of the transconductance needed in the OpAmp for the MDAC case and the presented current mode architecture. By removing the effect of β and reducing the capacitive loading at the output of the OpAmp, the reduction of the theoretical transconductance needed for the OpAmp is very significant. For the current mode architecture the transconductance reduces exponentially with respect to the number of bits solver in the stage. Even though, very significant power savings could be achieved as is shown in Fig. 5.8, there will be a minimum power consumption limit for the stage dominated at some point by the power consumption for the OTA, DAC and flash.

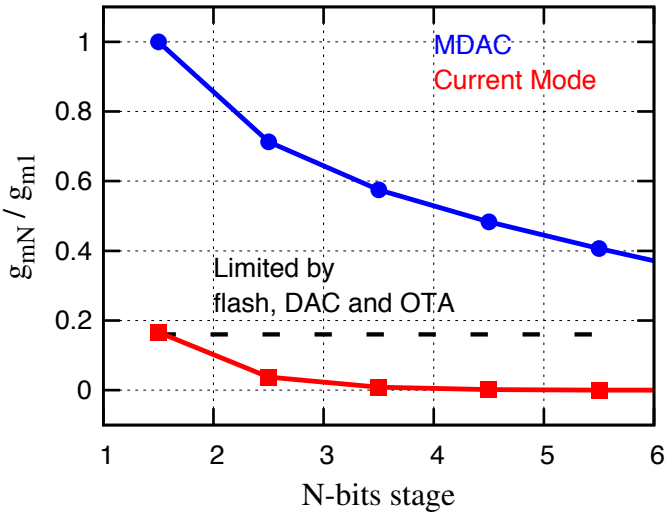


Fig. 5.8: OpAmp transconductance vs number of bits per stage (normalized to 1-bit): MDAC vs current mode.

Both OTA and DAC can be designed with low power consumption. The swing of V_{res} is defined by the current of the OTA and DAC, and the transimpedance of the TIA.

5.7. Pipeline architecture

The complete pipeline architecture is shown in Fig. 5.9. The first three stages are composed by the current mode architecture. The last stage is implemented with a flash architecture. The first stage provides 4 bits of resolution; the remaining three stages in the backend provide 3.5 bits of resolution each, with extra half bit included for redundancy as it was explained before. The power consumption and area for each stage is scaled consequently. A source follower buffer is used on chip the drive the capacitance of the sample and hold from the first stage, which is 2.8 pF.

The circuit uses only two clock signals ϕ_1 and ϕ_2. Stage one and stage three sample the signal with the falling edge of ϕ_1. After a non-overlapping time of ~200ps the sampled voltage is quantized by the internal flash sub ADC with the rising edge of ϕ_2. Stages two and four operate with the complementary edges.

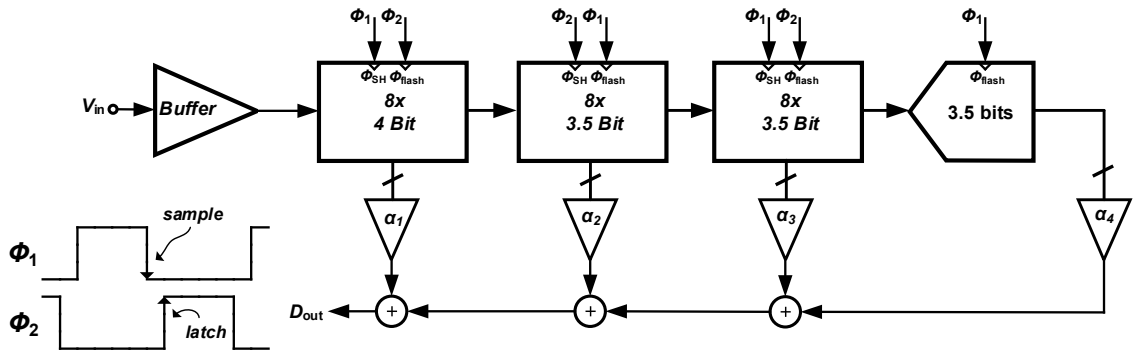


Fig. 5.9: Implemented pipeline architecture.

5.8. Circuit implementation details

Each current mode stage is composed by four main building blocks: OTA, flash sub-ADC, DAC and TIA. Following is a description for each block.

5.8.1. OTA

The linearity of the first stage is defined by two blocks: OTA and DAC. The OTA is a circuit that is widely used for high frequency operation filtering, since it operates in open loop. This block achieves higher frequencies compared with its closed loop counterparts. The simplicity of the OTA allows to achieve bandwidths in the GHz range in new process technologies. However, the OTA experience large signal swing at both the input and output transistors on contrary to the operation of a closed loop system in which the input transistors experience low swing at the gate. Therefore, the linearity performance of OTA's circuits is limited to third-intermodulation (IM_3) distortion of 40 dB or less.

Since the pipeline design demands high resolution especially in the first state, the OTA used needs to include a linearization technique to improve in linearity performance. The simplest possible solutions are shown in Fig. 5.10a. The gain is defined by the transconductance gain of the pMOS differential pair ($G_m = g_{m1,2}$). Using a simple quadratic model, it can be show that the IM3 equation can be defined as in (5.10), the distortion is proportional to the signal swing at the gate of the transistors (A_{amp}) and is inversely proportional to the saturation voltage (V_{dsat}) of each transistor. Thus, for low distortion a large V_{dsat} is desired. However, the use of large V_{dsat} requires large bias

currents. Also, large voltage headroom is required making the circuit impractical for low voltage applications.

$$IM_3 = \frac{3 \cdot A_{amp}^2}{128 \cdot V_{dsat}^2} \tag{5.10}$$

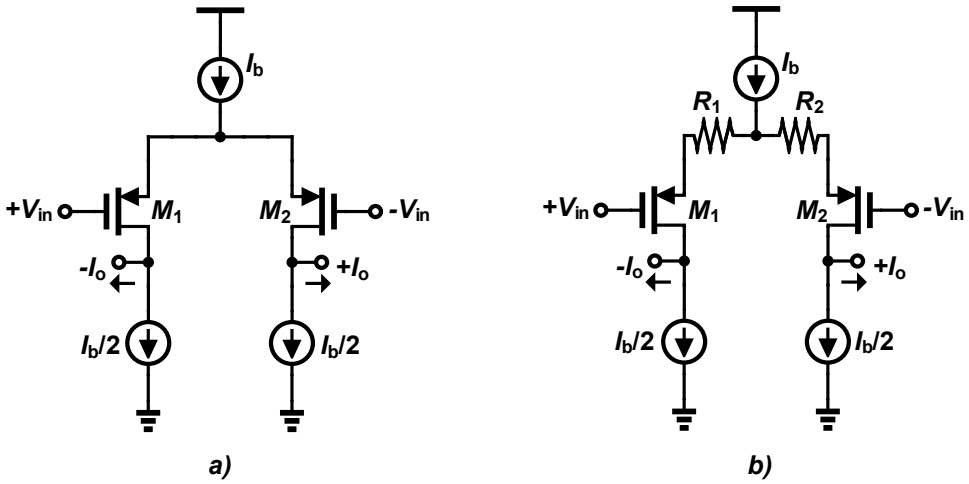


Fig. 5.10: Differential OTA a) conventional design, b) source degeneration.

The most common method to linearize an OTA is by source degeneration. Fig. 5.10b shows the simplest method to apply source degeneration on differential pairs. Resistors $R_{1,2}$ are connected between the source of transistors $M_{1,2}$ and the virtual AC ground node formed at the connection with current source. The source degeneration resistor has an

effect on the total transconductance provided by the differential pair, the effective transconductance is degraded by the gain product of $g_{m1,2}$ and $R_{1,2}$ as shown in equation (5.11).

$$G_m = \frac{g_{m1,2}}{\left(1 + g_{m1,2} \cdot R_{1,2}\right)} \tag{5.11}$$

The effect of source degeneration on distortion is shown in equation (5.12), N_r represents the source degeneration factor, Nr = $g_{m1,2}$ ·$R_{1,2}$. Considerable improvement can be achieved. An IM3 value of around 50-53 dB can be obtained in modern process technologies. However, if better performance is needed, a different solution needs to be implemented. Because the degeneration factor is increased to target higher IM_3 performance the total transconductance will be degraded demanding more power consumption.

$$IM_3 = \frac{3 \cdot A_{amp}^2}{128 \cdot (1 + N_r)^3 \cdot V_{dsat}^2} \tag{5.12}$$

Transconductance boosting by local feedback can be used to linearize the OTA as shown in Fig. 5.11a. The transconductance of transistors $M_{1,2}$ is increased by the gain provided by $A_{1,2.}$ Therefore, larger distortion improvement can be achieved without demanding more current from the differential pair or a larger degeneration resistor. The effective transconductance is shown in equation (5.13). If we consider high gain from $A_{1,2}$ it can assumed that the AC voltage at the source $M_{1,2}$ is equal to the input V_{in}, thus,

making the transconductance approximately inversely proportional to the source degeneration resistor.

$$G_m = \frac{A_{1,2} \cdot g_m}{\left(1 + A_{1,2} \cdot g_m \cdot R_s + g_m \cdot R_s\right)} \approx \frac{1}{R_s} \tag{5.13}$$

The effect of transconductance boosting in the linearity of the OTA is shown in equation (5.14). The IM_3 product is inversely proportional to the gain of the OpAmp. Therefore, for better distortion performance larger gain needs to be used.

$$IM_3 = \frac{3 \cdot A_{amp}^2}{128 \cdot A_{1,2} \cdot (1 + N_r)^3 \cdot V_{dsat}^2} \tag{5.14}$$

The inclusion of the OpAmp allows to relax the specifications for $M_{1,2}$. However, special attention needs to be included in the design of the OpAmps to avoid the power consumption to be dominated by $A_{1,2}$. Also, the DC coupling between the source of $M_{1,2}$ and the negative input of $A_{1,2}$ needs to be considered. The input signal normally has a common mode level that is different to the voltage at the source of $M_{1,2}$. In order to adjust the DC levels a battery circuit needs to be included as shown in Fig. 5.11b.

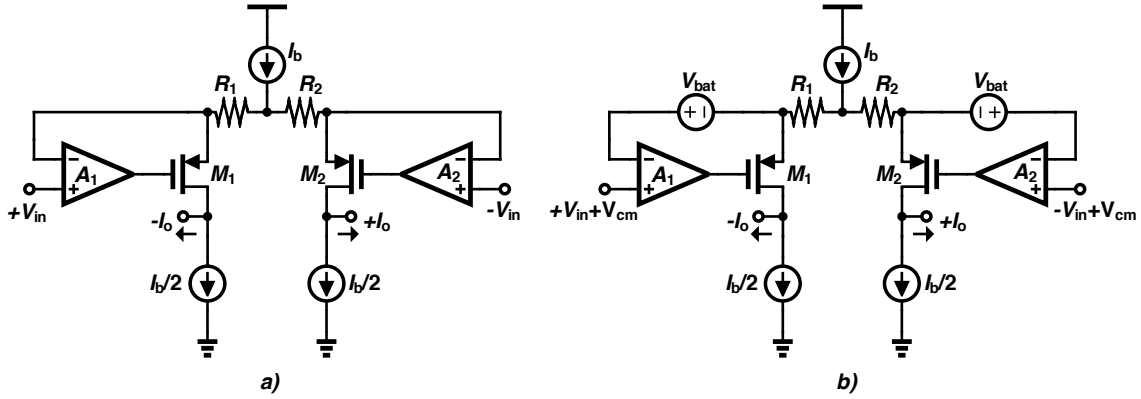


Fig. 5.11: OTA a) feedback linearization concept, b) input signal DC coupling.

The implemented OTA is shown in Fig. 5.12. The differential stage is implemented by transistors $M_{1,2}$. The bias transistor M_5 is divided in three pieces to minimize the DC current level flowing through $R_{1,2}$, the DC current for the architecture shown in Fig. 5.11 can produce a drop voltage on the resistor that can reduce the voltage for the bias transistor and put it out of saturation. Transistors $M_{5,1}$ and $M_{5,3}$ provide 25% if the bias current, this helps to increase the V_{ds} of transistor $M_{5,2}$. The current percentage provided by $M_{5,1}$ and $M_{5,3}$ needs to be a small value to minimize the noise contribution from those transistors. The noise from $M_{5,2}$ appears at the output as common mode and is not as relevant.

The transconductance boosting OpAmps are implemented with transistors $M_8 - M_{15}$. The circuit is composed by a push-pull architecture implemented by transistors M_8 and M_{10}. This implementation provides two advantages: first, the bias current is reused minimizing the current for the OpAmp. Second, the push-pull architecture inherently

provides the battery voltage illustrated in Fig. 5.11b. The voltage difference between the gate of the input transistor and the gate of the transistor in feedback is $V_{bat} = 2 \cdot V_{TH} + 2 \cdot V_{dsat}$. To adjust the DC level from the push-pull transistors with the voltage at the gate of M_1 the output is folded with transistor M_{12}. The high output impedance provided by the folding allows to minimize the length of transistors $M_8 - M_{12}$. Therefore, minimizing parasitic capacitors to achieve high frequency of operation. The length of the bias transistor M_{14} is increased to maintain adequate gain from the OpAmp.

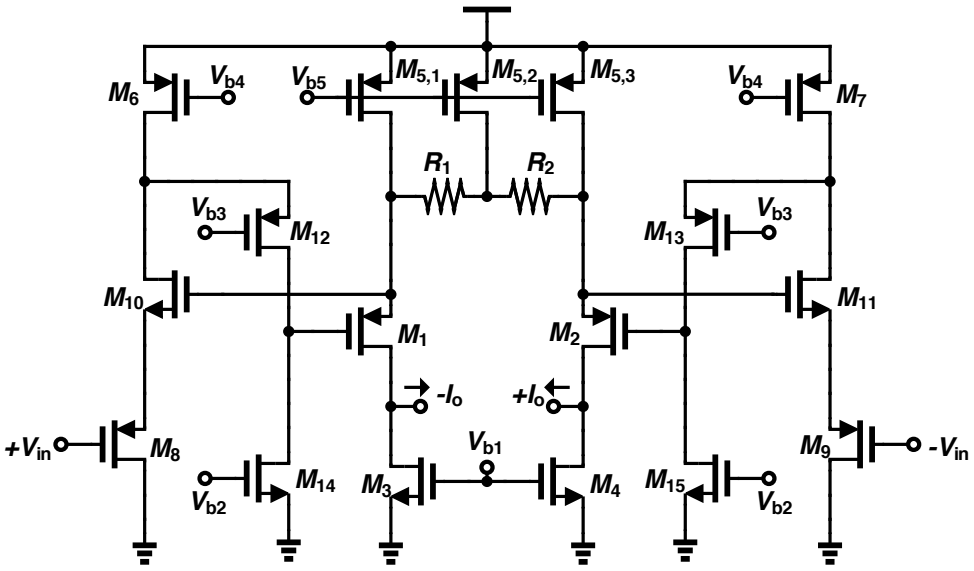


Fig. 5.12: OTA with push-pull OpAmp in feedback.

The system presents only one dominant pole at the gate of M_1. The other internal nodes provide low impedance, which push the poles to high frequencies. The low impedance provided by the TIA absorbs the pole at the output of the OTA. The power supply voltage for the OTA is 1.8 V. For the remaining blocks the power supply is 1.1 V with a common mode voltage of 0.55 V.

5.8.2. Flash sub-ADC

The flash sub-ADC uses the same architecture described in subsection 4.4.5. Since the target frequency is less for this architecture compared with the circuit presented in section IV, the specifications were relaxed but the architecture and signal swing are the same. The static current for the preamplifiers was relaxed after the first stage. Each slide of the flash sub ADC is directly connected to the DAC cells.

5.8.3. Current steering DAC

The current steering DAC architecture is shown in Fig. 5.13. The implemented architecture is similar to the DAC described in subsection 4.4.4 (for further details on the design of each DAC cell, refer to that section). The main difference is that the flip-flops at the input of the DAC are removed. This architecture is tolerant to any voltage depended delay introduced by the comparator in the flash, as long as the signal settles within less than half the clock period. Therefore, each DAC cell is directly connected to the flip-flops from the flash sub-ADC. By multiple simulations it was verified that all the signals from the DAC settle within the desired time.

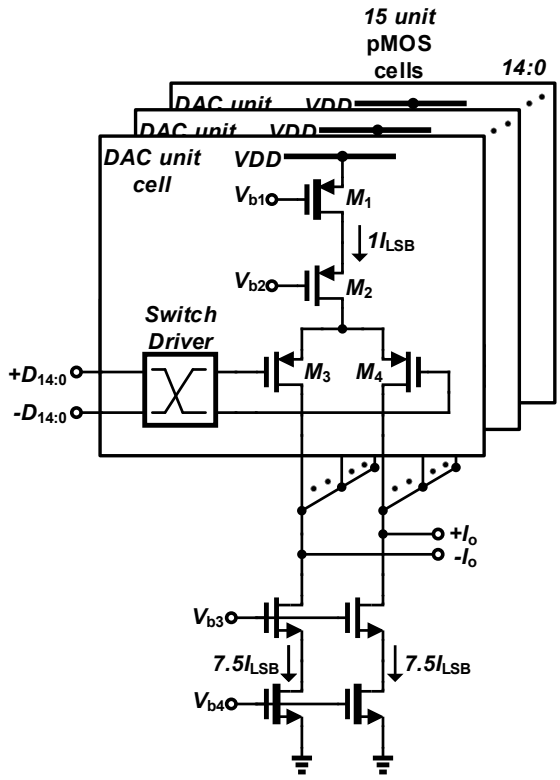


Fig. 5.13: Current steering DAC implementation.

5.8.4. Feedback transimpedance amplifier

The proposed current mode stage simplifies the design of the OpAmp required to obtain and amplify the residue voltage. Fig. 5.14 shows the implemented architecture, a single stage amplifier composed by $M_1 - M_5$ was used for the TIA. Active load was used to achieve higher gain compared to a resistive load. The feedback resistors are also included, $R_{1,2}$. The common mode feedback circuit is also shown in Fig. 5.14, the large resistors $R_{c1,2}$ measure the common mode level. The common mode signal is applied to the tail current source of the residual amplifier.

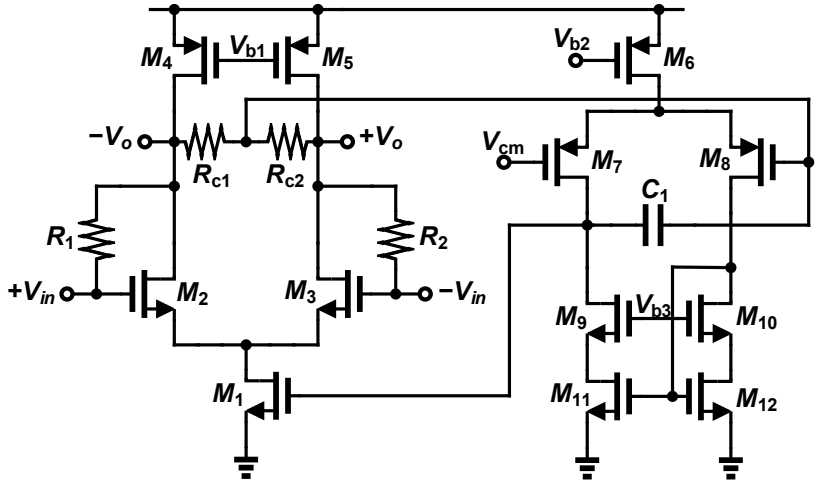


Fig. 5.14: TIA architecture with common mode feedback included.

5.9. Measurement results

A chip prototype of the proposed pipeline ADC was fabricated in a 40 nm LP8M process. The photograph of the chip is shown in Fig. 5.15. The chip active area is 0.23 mm^2, which includes the area from the buffer and the clocking circuitry. Fig. 5.16 shows the lab test setup. On-board low dropout regulators were used to generate a low noise 1.1 V and 1.8 V reference for the analog and digital blocks. The test input signal was generated form an Agilent® 33250A signal generator. Passive bandpass filters were used to minimize the noise contribution from the signal generator. The low jitter clock signals were generated from a Silicon Labs® Si5341-EVB. The data was captured with an FPGA using Texas instrument® TSW1405EVM.

The single ended input signal is converted to differential using an on board balun. The chip includes LVDS drivers to directly drive the FPGA. Differential signaling transmission lines were carefully designed to match the 100 Ω differential impedance from the FPGA board. The LVDS signal is terminated at input of the receiver in the FPGA with a 100 Ω resistor. The collected data was transferred to a computer and postprocessed using Matlab®.

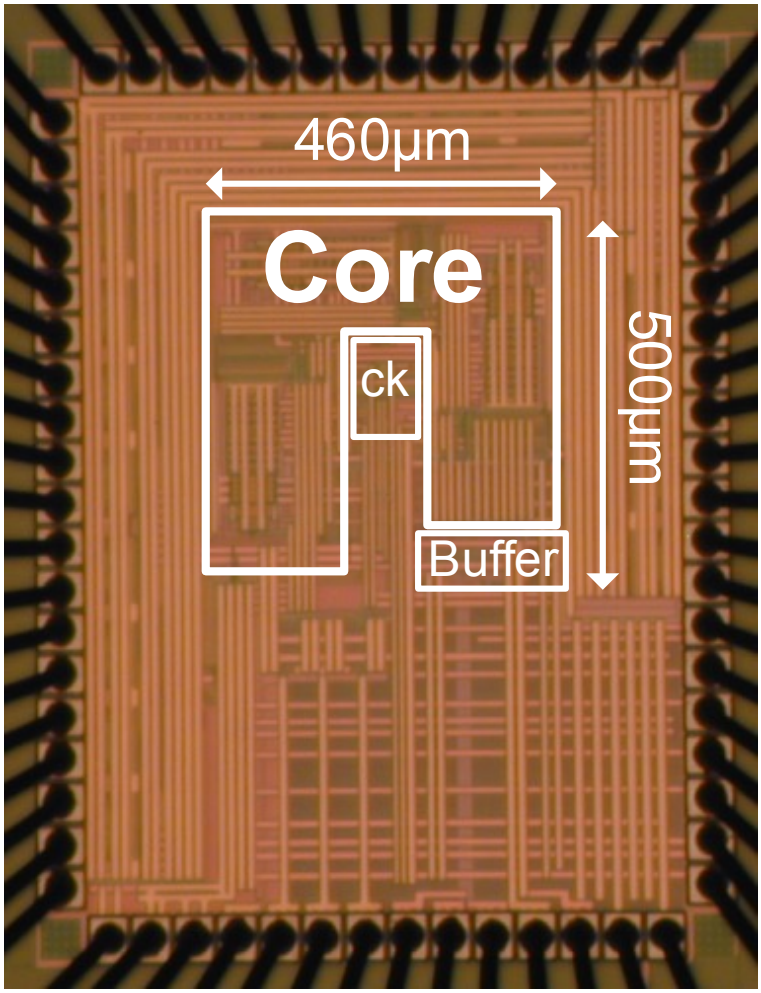


Fig. 5.15: Pipeline chip photograph, technology: tsmc40 nm.

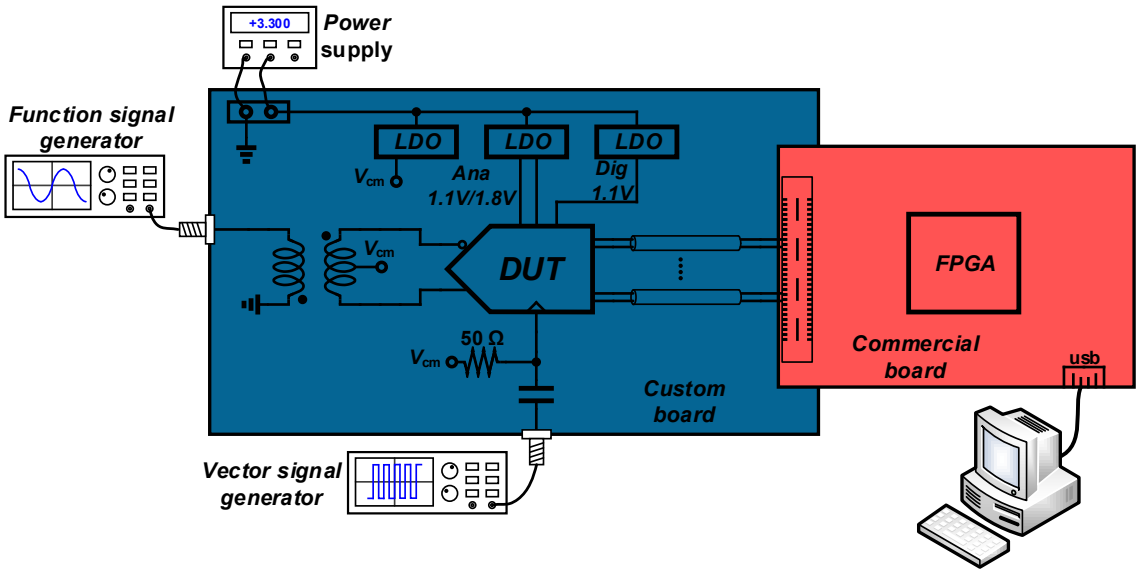


Fig. 5.16: Pipeline ADC lab testing setup.

Each pipeline stage was designed to have a gain of 8, which ideally make the architecture shown in Fig. 5.9 a 12-bit architecture. However, after fabrication the gain changed from 8 to 5.7. The best result was achieved when the digital output of each stage was multiplied by 1.4, which compensated the gain reduction. However, this digital multiplication also increased the noise by the same factor. Therefore, reducing the resolution of the architecture to 10 bits. It was concluded that the big difference on gain was produced by a significant variation on the absolute value of resistors $R_{1,2}$ shown in Fig. 5.14.

The chip consumes 8.4 mW of total power, with 3.8 mW of dynamic power and 4.6 of static power. Fig. 5.17 shows the result for a low frequency input signal, the measured SNDR is 58 dB, and 79 dB of SFDR. Even though, the result presents multiple harmonics inside the desired bandwidth, both the THD and noise floor present similar levels. When measured without input signal the ADC presents an SNR of 60 dB. Fig. 5.18 shows the output spectrum for an input signal close to Nyquist, the SNDR is 57.6 dB, and 74 dB of SFDR, the bandwidth of the circuits reduces the effect of high frequency harmonics. For a sampling frequency of 200 MHz the input frequency sweep is shown in Fig. 5.19. The ADC presents a flat response over the complete Nyquist bandwidth, confirming that for high input frequencies the result presents very low degradation. Also, the ADC performance for different sampling frequencies is shown in Fig. 5.20.

The obtained results were confirmed in simulation by intentionally reducing the gain of each stage to 5.4. The ADC is limited by noise, after multiplying the output data by the gain correction factors the noise floor is around 60 dB. It is expected that if the gain per stage is corrected on chip the result could improve by 6~7 dB. Even with the reduction in resolution the implemented prototype successfully demonstrates the concept of low power with the proposed architecture. Also, the measurement setup could be limiting the maximum frequency of operation from the ADC, capturing sixteen differential lines of data at frequencies higher than 200 MHz is a challenge. For frequencies of 100 MHz or higher is recommended to decimate the output data to reduce the data rate and have a more reliable result.

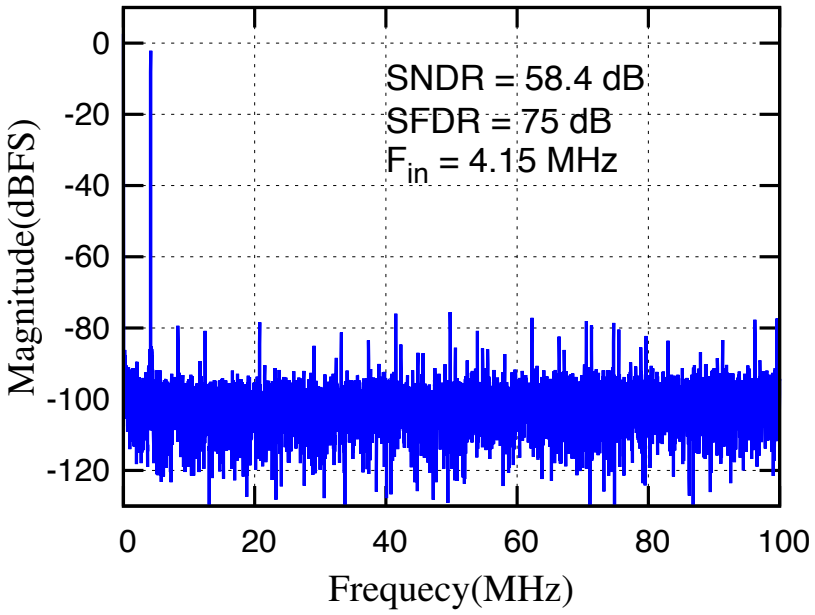


Fig. 5.17: Output spectrum for a 4.15 MHz input signal, with 200 MHz sampling frequency.

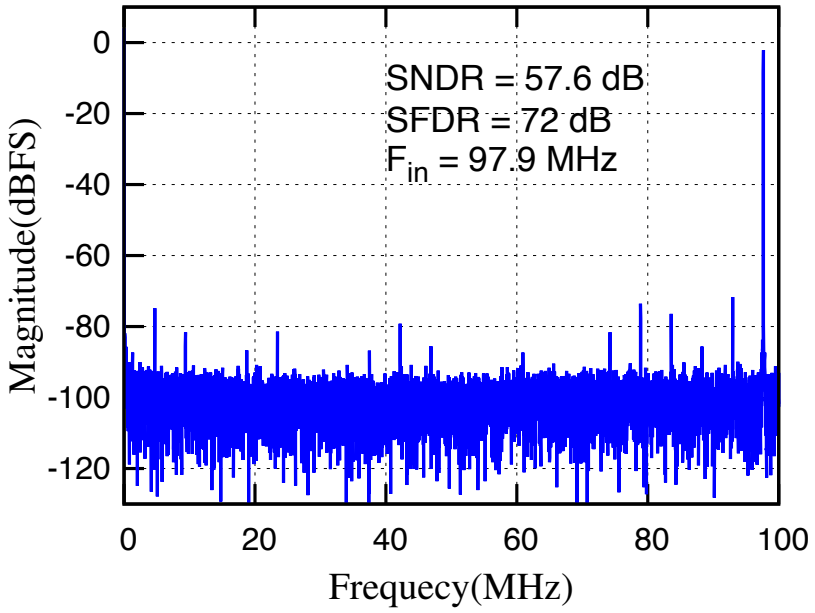


Fig. 5.18: Output spectrum for a 97.9 MHz input signal, with 200 MHz sampling frequency.

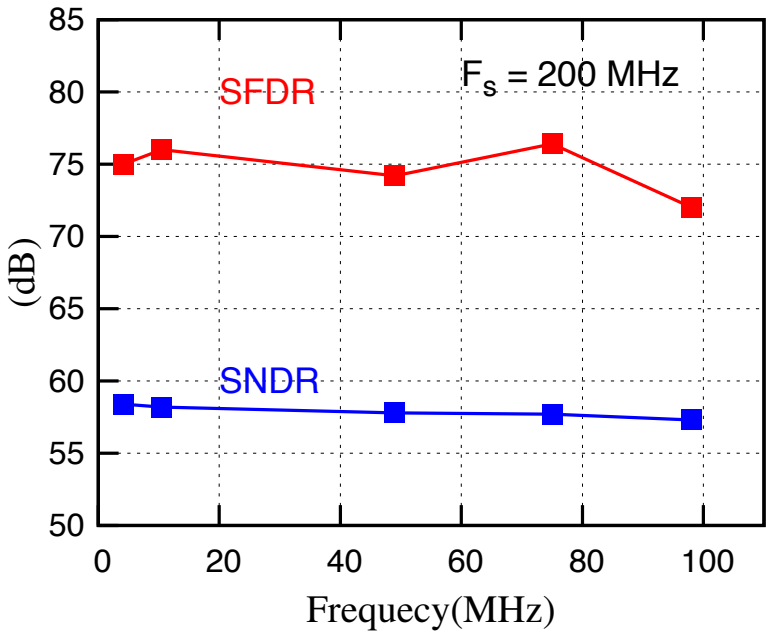


Fig. 5.19: SNDR/SFDR vs Input frequency sweep.

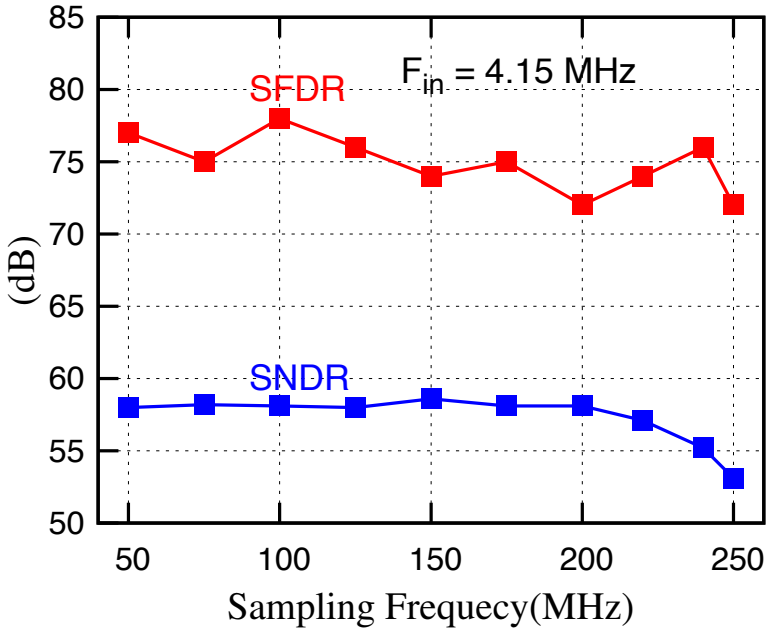


Fig. 5.20: SNDR/SFDR vs sampling frequency sweep.

The measured differential non-linearity (DNL) and integral non-linearity (INL) is shown in Fig. 5.21. The measured DNL is +1/-0.5 LSB, and INL is +2/-1 LSB. For the shown results, only the gain per stage variation has been digitally corrected by multiplying the digital output of each stage by 1.4 before the digital bits are combined. The best result is obtained when the same correction factor used in all the stage, meaning that the gain reduction is constant in all of them, no other calibration has been performed.

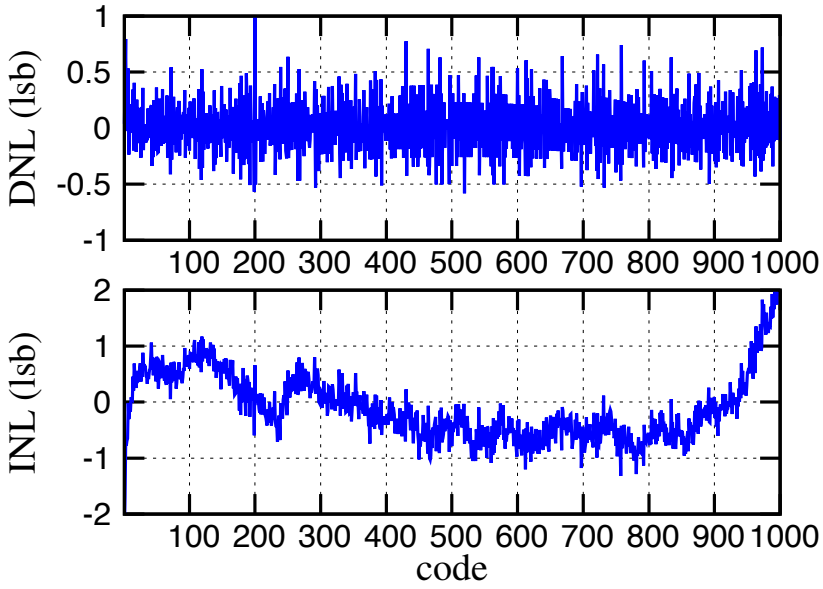


Fig. 5.21: DNL and INL for 10 bits output.

Table 5.1 shows a summary of the results and compares them with the recently reported state of the art solutions. The proposed architecture is the only one that is not implemented with switch capacitor MDAC. The achieved sampling frequency is competitive with recently reported architectures. The power consumption is the best for pipeline ADCs of 200Mhz sampling frequency or higher. However, the architecture is sensitive to variations on the absolute value of resistors, as it was confirmed by the reduction in gain per stage and consequently the reduction in resolution.

Table 5.1: Results summary and comparison pipeline.

Publication	**This Work**	[49] JSSC15	[50] ISSCC15	[51] JSSC14	[52] JSSC14	[47] JSSC13	[53] JSSC13
Architecture	**Current mode**	Split ADC	Virtual GND Ref	Zero Crossing	Charge Steering	OpAmp Cal.	OpAmp Cal.
Process (nm)	**40**	40	65	55	65	65	65
Sampling rate (MHz)	**200**	195	250	200	800	1000	200
SNDR(dB)	**58**	64	65	64	52	52	61.2
Power (mW)	**8.4**	53	49.7	30.7	19	33	19.8
Resolution	**12 b**	12 b	12 b	12 b	10 b	10 b	10 b
FoM (fJ/conv bit)	**64**	191	108.5	111	53	97	106
Supply	**1/1.8 V**	1	1.2	1.2	1	1	1

$$FoM=Power/(2\cdot BW\cdot 2^{(SNDR-1.76)/6.02})$$

5.10. Conclusion

This chapter demonstrates the functionality of a new pipeline architecture. The proposed architecture realizes the residue computation employing current mode techniques. The later allows the design of the main building blocks with low power consumption, in particular the specification for the residual OpAmp are highly relaxed. The design achieves very competitive performance up to 200MS/s. In contracts with recently reported pipeline ADCs that used complex digital calibration algorithms, the proposed architecture achieved one of the best performance and figures of merit without the use of complex calibration algorithms.

VI. CONCLUSION

The ever-increasing advance of wireless technologies creates a demand of high performance ADCs. The transistor channel scaling increases the challenges for analog design. The small intrinsic gain, low supply voltage, and large device mismatch place great limitations on the design of basic analog blocks such as OpAmps. Therefore, it becomes a challenge to design high resolution ADCs without using high power consumption or relaying on complex calibration algorithms. This dissertation presents the implementation of a CTΣΔM, with a low power and low area 7-bit quantizer and a fully digital noise reduction algorithm for SQNR improvement. The proposed algorithm is precise and robust against PVT. Furthermore, the number of active components is minimized compared with cascaded and MASH implementations, which reduces area and analog power. The architecture relies on the operation of a 7-bit quantizer. The implemented quantizer covers less area and is more power-efficient than previously reported flash, subranging and two-step architectures. The obtained results in a mainstream 130nm technology achieved an SNDR of 75 dB over a 15 MHz bandwidth, while consuming 20 mW of power.

The implementation of closed loop OpAmps at high operating frequencies is one of the main challenges in low power design. This work presents a low-pass sigma delta ADC with 75 MHz bandwidth. A summing amplifier is implemented with a current buffer that decouples the power consumption dependency with the closed loop gain. Also, the implementation of the proposed summing amplifier with current buffer helps to relax the design specification of other blocks in the sigma delta's loop filter. The

prototype was designed in 40 nm CMOS technology achieving 64.9 dB peak SNDR. The operating frequency was 3.2 GHz, the total power consumption was 22 mW.

The performance of both architectures is competitive with recently reported architectures as shown Fig. 6.1 with the Scherier's figure of merit. For the 15 MHz bandwidth sigma delta the obtained FoM is 168 dB, and for the 75 MHz bandwidth the FoM is 162 dB.

The problem of high power consumption needed for OpAmps in closed loop switching at high frequencies is also addressed in a pipeline ADC architecture. In this work, a current mode DAC and a transimpedance amplifier substituted the traditional capacitive multiplying DAC used in the residual amplifier. A highly linear OTA using a push-pull amplifier is presented, the linearity improved by 20 dB with the inclusion of the amplifier. The OTA is used to convert the sampled voltage to current for residue calculation. The prototype was implemented in 40 nm CMOS technology achieving 58 dB peak SNDR and 76 dB SFDR with 200 MHz sampling frequency. The ADC consumes 8.4 mW with a FoM of 64 fJ/Conversion-step. The competitive Walden's figure of merit is compared with recently reported Nyquist architectures in Fig. 6.2.

The obtained results fully demonstrate the effectiveness of the proposed architectures by achieving low power with high resolution and high frequency of operation.

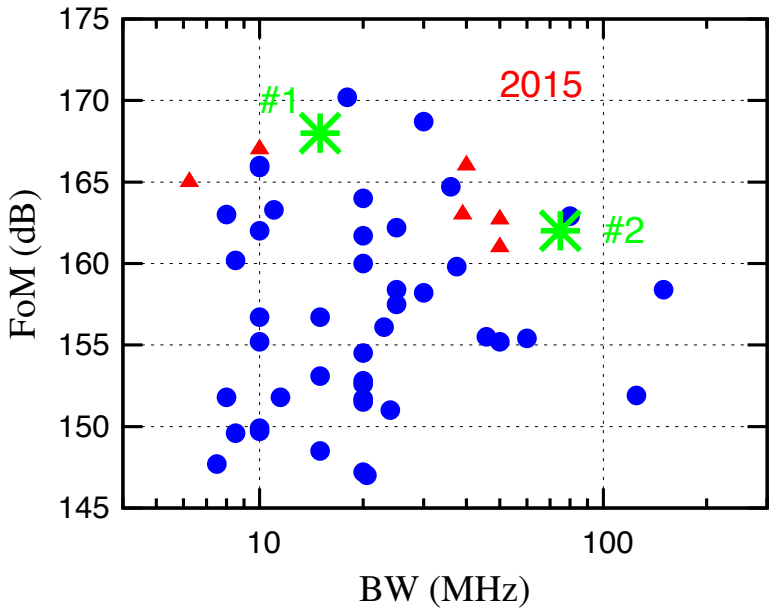


Fig. 6.1: Scherier FoM for sigma delta ADCs,BW > 5MHz.

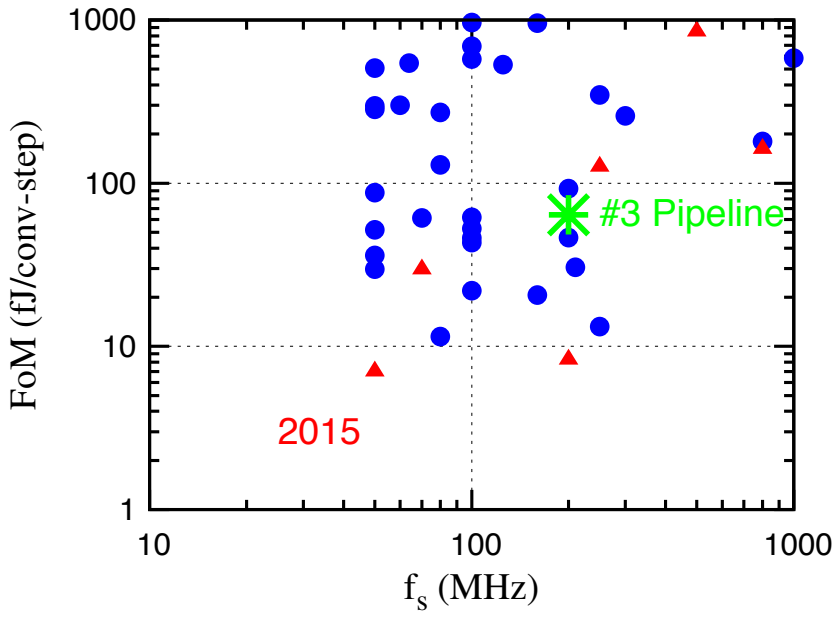


Fig. 6.2: Walden's FoM for Nyquist ADCs, SNDR>55 dB and BW>50MHz.

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