CLASS-G HEADPHONE AMPLIFIER ARCHITECTURES

A Thesis

by

BHARADVAJ BHAMIDIPATI

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

December 2010

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Edgar Sánchez-Sinencio
Committee Members,	Hamid A. Toliyat
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ABSTRACT

Class-G Headphone Amplifier Architectures. (December 2010)
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Chair of Advisory Committee: Dr. Edgar Sánchez-Sinencio

To maximize the battery life of portable audio devices like iPods, MP3 players and mobile phones, there is a need for audio power amplifiers with low quiescent power, high efficiency along with uncompromising quality (Distortion performance/THD) and low cost. Despite their high efficiency, Class-D amplifiers are undesirable as headphone drivers in mobile devices, owing to their high EMI radiation, additional costs due to filtering required at the output and also their poor linearity at small signal levels. Almost all of todays headphone drivers are Class-AB linear amplifiers, with poor efficiencies.

Here we propose a Class-G linear amplifier, which uses rail switching to improve efficiency. It can be viewed as a Class-AB amplifier operating from the lower supply and a Class-C amplifier from the higher supply. Though the classical definition of efficiency using full-scale sine wave does not show much improvement for Class-G (85.9%) over Class-AB (78%), we demonstrate that the Class-G audio amplifiers can have significant improvement of efficiencies (battery life) in the practical sense. By considering the amplitude distribution of audio signals a new realistic definition of efficiency has been proposed. This definition helps in demonstrating the advantage of using Class-G over Class-AB and also helps in optimizing the choice of supply voltages which is critical to maximizing the efficiency of Class-G amplifiers.

Two new circuit topologies have been proposed and thoroughly investigated.

The first circuit is more like a developmental stage and is designed/fabricated in AMI 0.5um. The second proposed Class-G amplifier with modified Class-AB bias, implemented in IBM 90nm, achieves -82.5dB THD+N by seamless supply switching and uses the least reported quiescent power (350μW) and area (0.08mm^2).

To

my parents Sujatha and Rama Sastry

my sister Srivani

and

my girlfriend Veena

ACKNOWLEDGMENTS

First of all, I want to thank my advisor, Dr. Sánchez-Sinencio, for all the motivation and support he has provided. I feel extremely fortunate to be the student of a great visionary. I express my deepest gratitude to him for being very demanding and also understanding the hectic class/work schedules, extracting the best out of me.

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I am grateful to MOSIS and IBM for providing fabrication support. I also want to thank John Tucker of Cirrus Logic for his very useful suggestions on the practical aspects of audio amplifier design.

Someone who needs a special mention is my teacher, Mr. Anurup Mitra at BITS, Pilani, for being an inspiration to me and many others to pursue a career in analog design. The insights he has given me have been invaluable in understanding and working with circuits.

Special thanks to Adrian Colli and Joselyn Torres for working with this project in 90nm technology while I was away. The discussions on amplifier compensation with Seenu proved very useful. It would have been impossible to finish the project in time without Reza's layout help. Without Felix's help in setting up the technologies, making the submission, testing and using the equipment, it would have been impossible to finish the work on time.

Analog design is not just about having great ideas and intuitive understanding. It also needs a lot of experience along with expertise. The elderly advice of Felix, Didem,

El-Nozahi, Mostafa, Mohsen, Raghavendra and Mandar had a significant contribution towards my learning at A&M. Not to forget the various technical discussions with peers/colleagues Jorge, Jin, Chao, Salvador, Viva, Mohan and Srikanth has been of vital importance for my success at A&M.

The company of my room mates and friends Shiva, Vivek, Raj, Vinay and Gupta has made my two year stay at A&M memorable. The motivation and moral support from my friends Vikram, Vikas and Deepthi during the tough times have helped me to remain focussed on my work.

Finally, the unconditional love that I receive from my family has been, and will be, the driving force that keeps me moving ahead in all walks of life.

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INTRODUCTION

A. Audio power amplifiers

An audio power amplifier is an electronic amplifier that amplifies low-power audio signals (signals composed primarily of frequencies between 20-20 KHz, the human range of hearing) to a level suitable for driving loudspeakers or other transducers like headphones and is the final stage in a typical audio playback chain. The preceding stages in such a chain are low power audio amplifiers, which perform tasks like pre-amplification, equalization, tone control, mixing/effects, or audio sources. Power amplifiers may have power ratings ranging from less than 100 mW to several hundreds of watts. Stereo amplifiers consist of two identical, but electrically independent, amplifier circuits housed in a single chassis, often sharing a common power supply.

The ideal amplifier delivers an output signal that, aside from its higher power level, is identical in relative spectral content to the input signal. In reality, the amplifier generates various forms of distortion: harmonic distortion (tones at multiples of the desired signal frequency), intermodulation distortion (spurious sum or difference frequencies created when multiple tones are applied to the amplifier simultaneously, as in the case of music or speech amplification), and transient intermodulation distortion (caused by rapid fluctuations of the input signal level). All forms of distortion are measured as percentages of the desired signal amplitude. Other parameters that are used to define an amplifier's characteristics include frequency response and signal-to-noise ratio in the audio band (SNR). While the above metrics define the quality of audio power amplifier, efficiency of the amplifier determines how efficiently the

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amplifier can utilize the available power from the power supply, it is defined as the ratio of total power delivered to the load to total power consumed from all the power supplies.

B. Brief history of audio amplifiers

The first audio amplifier [1] was made in 1906 by a man named Lee De Forest and came in the form of the triode vacuum tube. This particular mechanism evolved from the audion, which was developed by De Forest. Unlike the triode, which has three elements, the audion only had two and did not amplify sound. Later on during the same year, the triode, a device with capability of adjusting the movement of electrons from a filament to a plate and thus modulating sound, was invented. It was vital in the invention of the first AM radio.

After World War II, there was a surging of technology because of the advancements developed during the war. The earliest kinds of audio amplifiers were made of vacuum tubes or valves. An example of these is the Williamson amplifier [1], which was introduced in 1946. At the time, this particular device was considered cutting edge and produced higher quality sound compared to other amplifiers available at the time. The market for sound amplifiers was robust and the valve-type devices can be owned at affordable rates. By the 1960s, gramophones and televisions made valve amplifiers quite popular.

By the 1970s, valve technology was replaced by the silicon transistor [1]. Although valves were not completely wiped out as evidenced by the popularity of the cathode ray tubes, which was used for amplifier applications, silicon transistors became more and more present. Transistors amplify sound by changing the voltage of the audio input through the use of semiconductors. The reasons for the preference of

transistors over valves were that they were smaller and thus more energy-efficient. In addition to these, they're also better at reducing distortion levels and were cheaper to make.

There is a lot of controversy [2], [3] over the superiority of vacuum tube audio amplifiers over the transistor ones. The complications and controversy stem from the fact that music is played for human beings to hear, whose nonlinear ear-brain hearing systems are far from fully understood. Since no one knows exactly how to model the human auditory system, no one knows exactly what engineering measurements are appropriate to evaluating the performance of audio equipment. A smidgen of some kinds of distortion may sound worse to the ear than larger amounts of other kinds. So ultimately, the only way to judge audio equipment is by listening to it. Hence the controversy: subjective human perception–especially when flanked by questions of artistic merit–is made to order for arguments and disputation.

Briefly stated, a commercially viable number of people find that they prefer the sound produced by tubed equipment [2], [3] in three areas: musical-instrument (MI) amplifiers (mainly guitar amps), some processing devices used in recording studios, and a small but growing percentage of high-fidelity equipment at the high end of the audiophile market. These areas employ vacuum tubes of the type once known as receiving tubes, but now called simply tubes. Not only has the use of vacuum tubes in these fields defied the semiconductor tide elsewhere, but such use and demand has even surged in the course of the 1990s. Even today in the era of portable music players many audiophiles relish the warmth of vacuum tube audio amplifiers.

C. Classification of audio power amplifiers

For a long time the only amplifier classes relevant to high-quality audio were Class-A and Class- AB. This is because valves were the only active devices, and Class-B valve amplifiers generated so much distortion that they were barely acceptable even for public address purposes. All amplifiers with pretensions to high fidelity operated in pushpull Class-A. Solid-state gives much more freedom of design. We will see the meaning of Classes A, B/AB, D and G; and this certainly covers a vast majority of the solid-state amplifiers exploited commercially [4].

1. Class-A

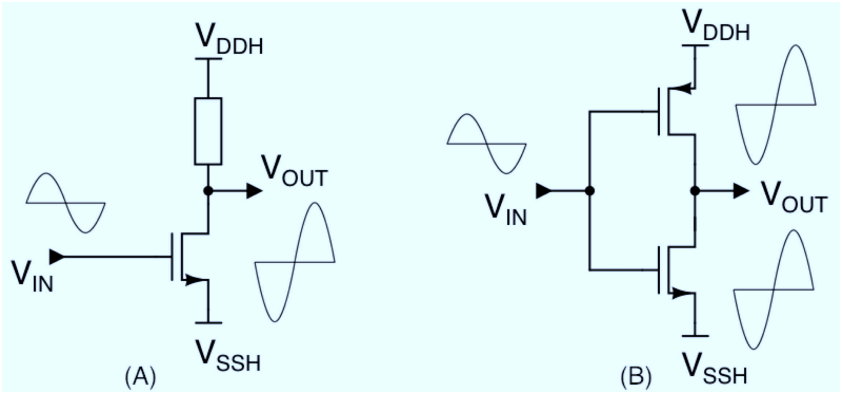

Fig. 1. Typical Class-A amplifiers

In a Class-A amplifier Fig. 1 current flows continuously in all the output devices, which enables the nonlinearities of turning them on and off to be avoided. Each of

the device conducts for the whole 360 degree phase of a sine wave. They come in two rather different kinds, although this is rarely explicitly stated, which work in very different ways.

One kind of Class-A stage Fig. 1B is simply a Class-B stage with sufficient current flowing for neither device to turn off under normal loading. The great advantage of this approach is that it cannot abruptly run out of output current; if the load impedance becomes lower than specified then the amplifier simply takes brief excursions into Class-AB, hopefully with a modest increase in distortion and no seriously audible distress.

The other kind Fig. 1A could be called the voltage controlled current source (VCCS) type, which is in essence a single common source with an active load sourcing/sinking the current. If this latter element runs out of current capability it makes the output stage clip much as if it had run out of output voltage. This kind of output stage demands a very clear idea of how low an impedance it will be asked to drive before the design begins.

2. Class-B/AB

In a Class-B amplifier shown in Fig. 2 current flows exactly for half the time in each of the output devices (for 180 degree phase of sine wave about zero). The device connected to the positive supply M_{P2} conducts during the positive half cycle of signal and the one connected to negative supply M_{N2} conducts during the negative half cycle of signal. There is a crossover at zero where both the devices are off. As the input gets closer to zero, the devices get closer to turn off and exhibit more non-linear behavior introducing lot of distortion. This makes the text book Class-B useless for real applications. Instead, letting each of the drivers M_{P2} & M_{N2} conduct for slightly more than 180 degrees of signal phase by modifying the biasing makes it a Class-AB

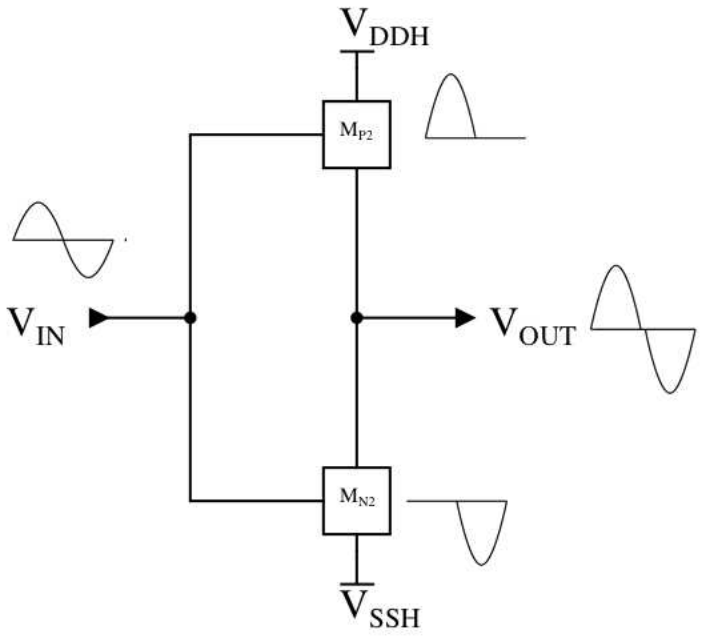

Fig. 2. Typical Class-B amplifier

stage. In real applications the terms Class-B and Class-AB are used synonymously and they usually mean Class-AB.

Class-AB is a Class-B amplifier with no or significantly reduced crossover. Each of the device conducts for just more than 180 degrees phase of the sine wave across zero. At zero, both the devices are on taking some quiescent power but significantly less than the Class-A amplifier.

3. Class-C

Class-C implies device conduction for significantly less than 50% of the time ($\ll$180 degrees phase of a sine wave about zero), and is normally only usable in radio work, where an LC circuit can smooth out the current pulses and filter harmonics. In the context of audio we can say a Class-B stage which has no conduction about zero as

working in Class-C. Though there is no meaning in using Class-C for audio, as the definition itself implies large distortion. It will be a helpful tool in understanding the Class-G.

4. Note on Class-A/AB/B/C

Essentially all these four classes are the same linear/pseudo-linear circuit. The only thing that differentiates them is how the output driver devices are biased. The transfer characteristics of these classes of amplifiers is summarized in the Fig. 3. As we keep increasing the quiescent current in the devices; we move from Class-C towards Class-A as explained in Table I.

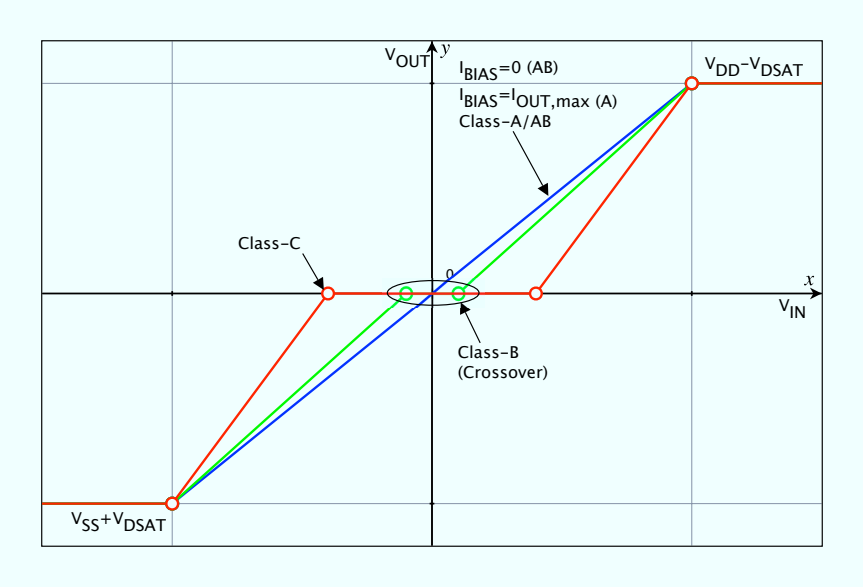

Fig. 3. Transfer characteristics of linear/pseudo-linear classes of amplifiers

Table I. Summary of Class-A, AB, B, C output stage operation

Type	Bias Current	Conduction angle
Class-A	$I_{out,max}$	360^o
Class-AB	just > 0	just $> 180^o$
Class-B	0	180^o
Class-C	0	$< 180^o$

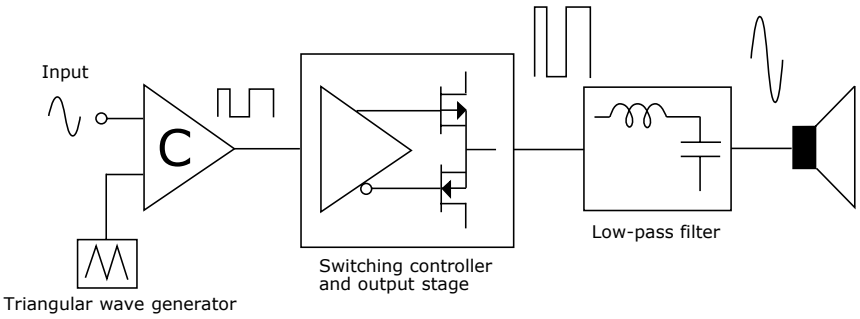

Fig. 4. Typical Class-D amplifier

5. Class-D

These amplifiers continuously switch the output from one rail to the other at a very high frequency, controlling the mark/space ratio to give an average representing the instantaneous level of the audio signal; this is alternatively called pulse width modulation (PWM). Great effort and ingenuity has been devoted to this approach, for the efficiency is in theory very high, but the practical difficulties are severe, especially so in a world of tightening EMC legislation, where it is not at all clear that a 200 kHz high-power square wave is a good place to start.

Class D audio amplifiers are typically based on pulse width-modulation (PWM) to generate the output waveform. An analog audio signal (20Hz - 20kHz) is compared with a high frequency carrier ($>$ 200 kHz) to generate a switching wave (PWM). This wave is further increased by a power stage in order to drive the output load. Once the signal is modulated, it is passed through a low-pass filter to recover the analog wave and eliminate the high frequency components [5].

The traditional class D audio amplifier architecture is depicted in Fig. 4. It is an open-loop based system whose main block is represented by the comparator (PWM generator). This topology requires having a well controlled triangular wave shape (carrier signal) which adds cost and potential degradation for non-ideal triangular waveform. The power stage block allows the system to minimize the output resistance of the amplifier in such way that most of the output power is delivered to the load, typically a speaker, through the low-pass filter whose frequency response is designed to be as flat as possible within the audible frequency band.

Another ingenious approach to Class-D amplifiers [6][7] applies sliding mode (SM) control technique and is shown in Fig. 5. Linearity of the system is enhanced by using negative feedback. Furthermore, this approach avoids the triangular wave signal

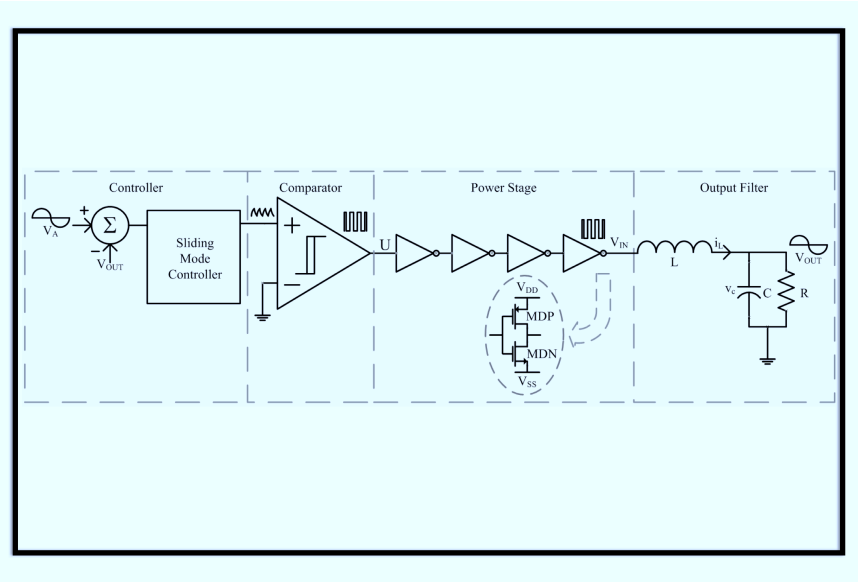

Fig. 5. Class-D amplifier using sliding mode control

used in conventional class D audio amplifiers. The stability of the proposed amplifier is not affected by process and temperature variations (PTV) or by any initial conditions. One of the best features of SM control is its robustness to external perturbations [8][9]. It consists of four basic subsystems: the controller, a hysteresis comparator, the output power stage and the output filter. Ideal SM control reproduces exactly the same waveform at the output stage of the class D amplifier using PWM; however, due to hardware implementation, SM control faces two main obstacles, the quasi-differentiation operation and the non-infinite switching frequency.

Distortion is not inherently low in either of these approaches, and the amount of global negative feedback that can be applied is severely limited by the pole due to the effective sampling frequency in the forward path. A sharp cut-off low-pass filter is needed between amplifier and speaker, to remove most of the RF; this will require

at least two or four inductors (for stereo) and will cost money, but its worst feature is that it will only give a flat frequency response into one specific load impedance.

6. Class-G

This concept was introduced by Hitachi in 1976 [10] with the aim of reducing amplifier power dissipation. Musical signals have a high peak-to-average ratio (crest factor), spending most of the time at low levels, so internal dissipation is significantly reduced by working from low-voltage rails for small outputs and switching to higher rails for larger excursions.

Class-G amplifier can be viewed as a Class-AB amplifier operating from the smaller supply and then a Class-C amplifier from the original (higher) supply rail. This is very advantageous especially in case of audio where the crest factor of the signal is typically 12-20dB. By using a smaller supply, when the input/output signal level is low we get higher efficiency, without affecting the maximum signal output (Dynamic range). The challenge is to make sure switching between the supplies introduces only a little/no non-linearity.

The above concept described can be extended to multiple supply levels, but it must be remembered that the additional supplies can not be generated for free. A more detailed discussion on the number of supply levels has been presented in a latter chapter when we discuss the efficiency in more detail.

D. Portable electronics: The place for Class-G

With the rapid growth of mobile electronics market for entertainment, there has been increased demand for devices and designs with very low standby power consumption and very high efficiencies to achieve increased battery life; all at uncompromising

performance and no increase in cost. Headphone drivers are no exception to this trend. Also there has been a trend, which is pushing all of the system functionality on to a single system on chip, to make the gadgets more and more compact and cost effective. This means, the more friendlily your design is to rest of the system, the better it is.

The Class-D switching amplifiers have very good efficiencies, but the switching causes a lot of unacceptable Electro Magnetic Interference [4] both on-chip and off-chip, making it unacceptable for integration on to any devices with RF components. Also the switching EMI prohibits the use of audio cable as an antenna for FM radio, which is present in most of the present day mobile audio devices. Apart from the EMI problems with Class-D switching amplifiers, the cost of external filter required is also a concern. Moreover, the high distortion and low efficiencies of Class-D switching amplifiers at low signal levels make them undesirable and even unacceptable as headphone drivers in mobile applications. Almost all of todays headphone drivers use Class-AB linear output stages, despite their very poor efficiencies. Class-G will be an ideal way to improve the efficiencies in portable audio devices.

Why only portable audio and why not all audio amplifiers can be of Class-G type? The Class-G amplifier will deliver much better power efficiency compared to Class-AB in any kind of application but Class-D amplifiers will be of greater benefit in big standalone audio systems, where special technologies with devices having low on resistance can be used, where the EMI interference is not a big problem and also where the use of external LC filters is acceptable. Class-D will deliver better efficiencies at competitive linearity numbers compared to the linear classes of power amplifiers (even more than Class-G). Its only when we are integrating things together they become a concern. Thats why we do not see Class-D amplifiers in portable devices and it is the right place for Class-G.

E. Scope of this work

Firstly, the concept of audio amplifier efficiency has been looked at in practical sense using the amplitude distribution characteristics of the audio signals. This enables us to choose the supply voltages optimally to maximize the efficiency of Class-G audio amplifiers. After taking a closer look at the existing Class-G works we demonstrate the concepts of class-G and various design trade-offs in detail. Finally, two circuit level Class-G implementations using the developed concepts have been proposed, implemented, fabricated in silicon and tested.

CHAPTER II

TRUE EFFICIENCY OF AN AUDIO POWER AMPLIFIER

Power Efficiency by itself is not a difficult term to understand. It defines how much of the total electrical power consumed is delivered to the load (speaker) as shown in equation (2.1). No electrical circuit is 100% efficient, always some power is dissipated in the circuit and is lost as heat. With the need for longer battery life and tighter integration in the portable devices, it is becoming increasingly important to care about the efficiency of circuits.

$$\eta = \frac{P_L}{P_{SUP}} \tag{2.1}$$

Though the term power efficiency is very old, and is constantly dwelled upon, it is very poorly understood. It is treated merely as a number to judge the quality rather than in its true sense. In this chapter we look at power efficiency in its true and useful sense rather than in the typical casual approach. From now on we refer to "power efficiency" only as "efficiency" and it is a reasonable to so because the frequency of audio operation is very low.

A. Classical efficiency

The efficiency numbers we see most of the time are derived from the classical definition. It is the ratio of average power delivered to the load to the average power taken from the supply during one cycle of a sine/cosine wave input. Why were people using that? Thanks to Fourier, sine/cosine is the classical signal used to test any system and often rail-to-rail signal is used because it gives the best number. Moreover, the calculation of efficiency is very straight forward when we use these sine/cosine input.

The efficiency of an amplifier is highly dependent on the input signal that we are using. But people have given little importance to it and they have been using efficiency in very casual sense. Before we go into a more realistic treatment of efficiency we will briefly go through the mathematics involved in reaching the classical efficiency numbers we see everywhere. This will help us as an aid to understanding the efficiency in true sense later on.

1. Class-A

The Class-A power stage is just a standard, textbook small-signal amplifier on steroids. The basic assumption in Class-A design is that bias levels are chosen so that the driving transistor operates in saturation region throughout. The primary distinction between Class-A power stage and small-signal amplifier is that, the signal currents in a power stage are substantial fraction of bias level. Class-A power stages have got very good linearity but at the expense of efficiency. There is always power dissipation due to bias current even when there is no signal. The Class-A operation is explained in Figs. 6, 7 where $\pm V_{SUP}$ are the supply voltages, V_o is the output voltage and $V_{o,pk}$ is the output voltage amplitude; and I_{SUP} is the total current drawn from the supply, I_o is the load current and $I_{o,pk}$ is the amplitude of supply current.

Assuming a close to ideal Class-A amplifier

$$\begin{aligned} V_{o,pk} &= V_{_{SUP}} \\ I_{BIAS} &= I_{o,pk} \end{aligned} \tag{2.2}$$

Total power delivered to the load:

$$P_{_L} = \frac{1}{T}\int V_o(t).I_o(t)dt = \frac{2V_{o,pk}^2}{\pi.R}\int_0^{\frac{\pi}{2}} sin^2(\phi)d\phi = \frac{V_{o,pk}^2}{2.R} \tag{2.3}$$

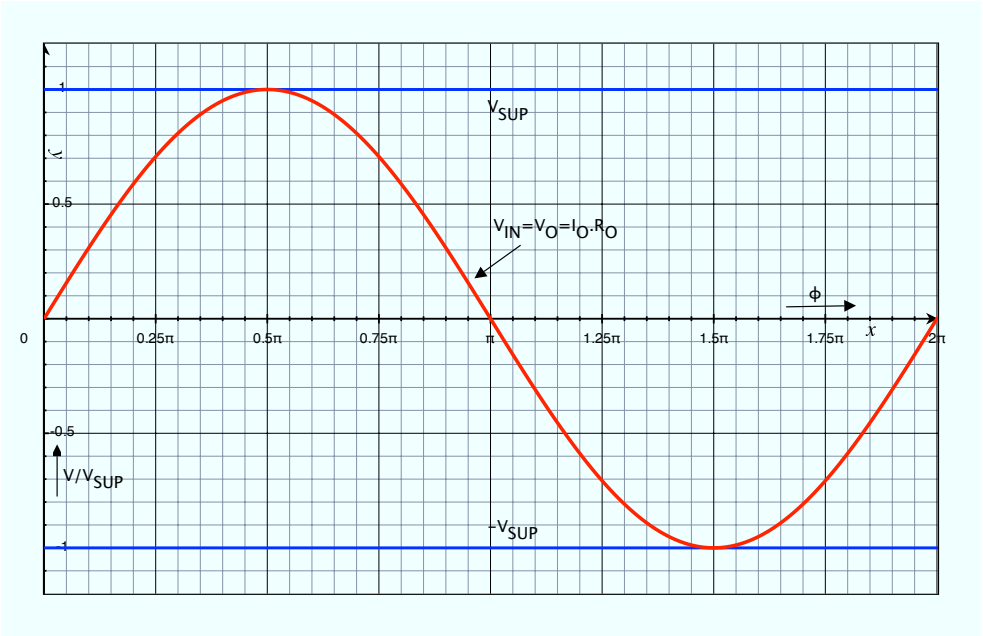

Fig. 6. Supply and output voltages in a Class-A amplifier

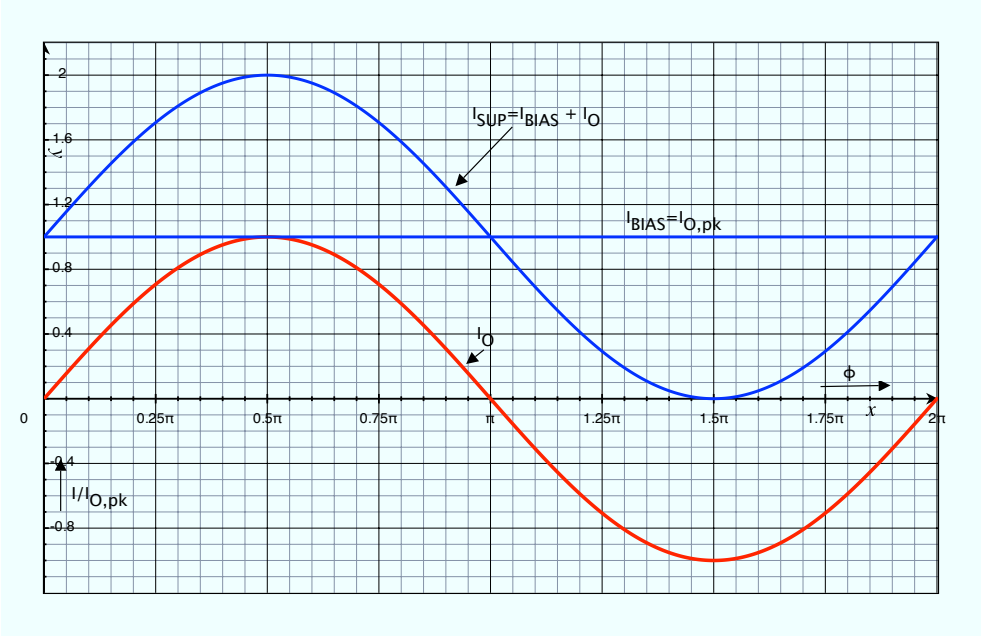

Fig. 7. Supply and load currents in a Class-A amplifier

Total current drawn from the supply:

$$I_{_{SUP}} = I_{_B} + I_o = I_{o,pk} + I_{o,pk}.sin(\phi) \tag{2.4}$$

Total power drawn from the supply:

$$P_{_{SUP}} = \frac{1}{T}\int V_{_{SUP}}(t).I_{_{SUP}}(t)dt = \frac{V_{o,pk}^2}{\pi.R}\int_0^{2\pi}(1+sin(\phi))d\phi = \frac{2V_{o,pk}^2}{R} \tag{2.5}$$

Classical Efficiency of Class-A amplifier:

$$\eta_{_A} = \frac{P_{_L}}{P_{_{SUP}}} = \frac{1}{4} = 25\% \tag{2.6}$$

This calculation assumes fairly ideal behavior, considering the V_{DSAT} of the transistors and some more bias current for both the drivers to have some current in all operating conditions pushes this 25% number down to 10-15%.

2. Class-B/AB

The first step to improving the efficiency of a power stage is taken by trying to reduce the bias current and making it ideally zero in class-B case. This comes with some undesirable effects of crossover distortion, so the bias current is chosen to be as much minimum as possible to get rid of crossover distortion in case of a Class-AB amplifier. The typical Class-B amplifier operation is described in the Figs. 8 and 9 with all the variables having the same meaning as explained in Class-A.

It can be understood from the Fig. 9, that the current drawn from the supply is exactly the amount required to drive the load, so there is no reduction of efficiency due to current. Now the instantaneous efficiency of amplifier can be defined as $\frac{V_o}{V_{SUP}}$. If the amplifier is assumed close to ideal then $V_{o,pk} \simeq V_{_{SUP}}$.

The total power delivered to the load is same as in equation (2.3) and the total

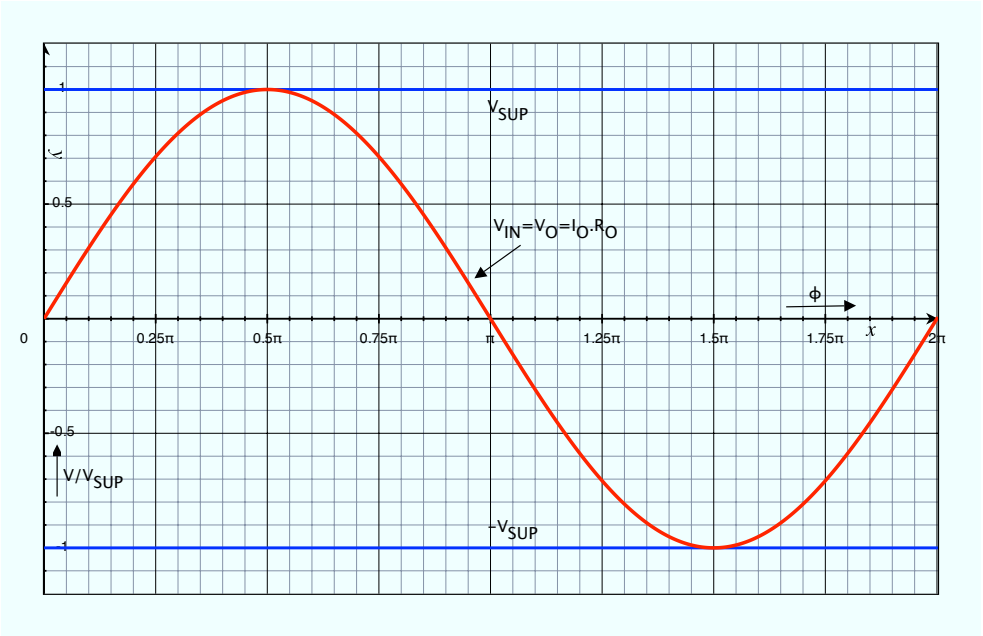

Fig. 8. Supply and output voltages in a Class-AB amplifier

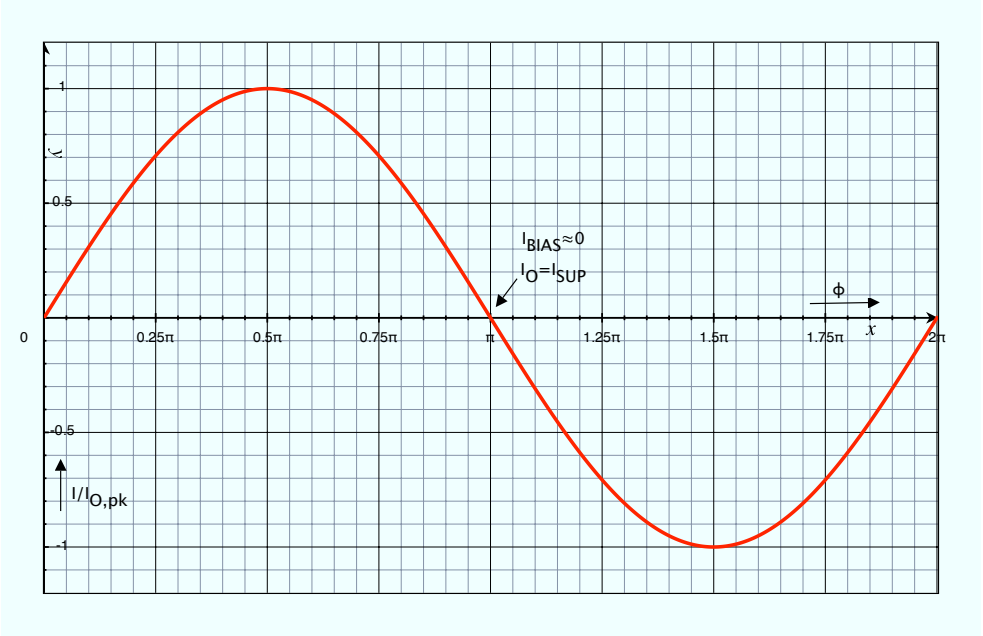

Fig. 9. Supply and load currents in a Class-AB amplifier

power drawn from the supply is:

$$P_{SUP} = \frac{1}{T}\int V_{SUP}(t).I_{SUP}(t)dt = \frac{2V_{o,pk}^2}{\pi.R}\int_0^{\frac{\pi}{2}} sin(\phi)d\phi = \frac{2V_{o,pk}^2}{\pi.R} \tag{2.7}$$

And the classical efficiency of the nearly ideal Class-AB amplifier is:

$$\eta_{AB} = \frac{P_L}{P_{SUP}} = \frac{\pi}{4} = 78.54\% \tag{2.8}$$

In practical conditions is typically about 35-50%.

3. Class-G

The obvious next step to improving efficiency is to lower the supply rail (as the instantaneous efficiency is only limited by supply voltage not by current anymore as discussed in the Class-B operation) when the input signal is small to improve the efficiency. The Class-G operation is explained with two different voltage levels in Fig. 10. The α in Fig. 10 refers to the phase of the sinusoid at which the voltage level switching takes place and thus the lower supply level $V_{SUP\_LOW} = V_{SUP}.Sin\alpha$.

The total power delivered to the load is same as in equation (2.3) and the total power drawn from the supply is:

$$\begin{aligned} P_{SUP} = \frac{1}{T}\int V_{SUP}(t).I_{SUP}(t)dt &= \frac{2V_{o,pk}^2}{\pi.R}\left[\int_0^{\alpha} sin(\alpha)sin(\phi)d\phi + \int_{\alpha}^{\frac{\pi}{2}} sin(\phi)d\phi\right] \\ &= \frac{2V_{o,pk}^2}{\pi.R}\left[sin\alpha + (1-sin\alpha)cos\alpha\right] \end{aligned} \tag{2.9}$$

And the classical efficiency of the nearly ideal Class-G amplifier with two supply levels can be shown to be maximized at $\alpha = \frac{\pi}{4}$:

$$\eta_G = \frac{\pi}{4}\left[\frac{1}{sin\alpha + (1-sin\alpha)cos\alpha}\right] = 85.9\% \tag{2.10}$$

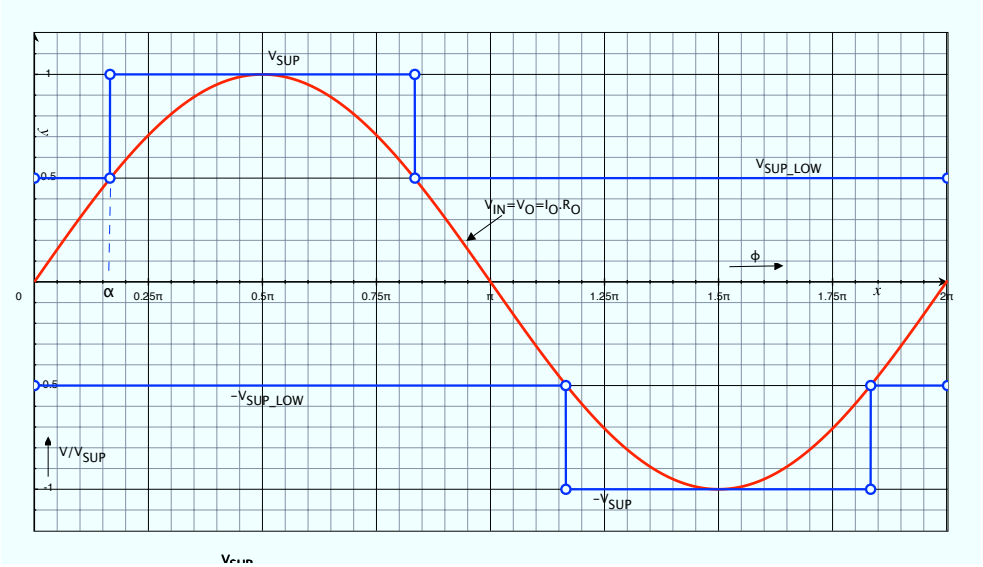

Fig. 10. Supply and output voltages in a Class-G amplifier

This gives a maximum theoretical efficiency of 85.9%. At the first look this may not seem a great improvement compared to the amount of pains that have to be taken for generating and switching between the supply levels. This is quite deceiving and is one of the reasons there is not much work on Class-G. With a clear understanding of amplitude characteristics, the benefits of Class-G can be seen easily. In the following in sections we will see more of it.

4. Multi-level Class-G

For the sake of completeness an n-level Class-G operation is presented in the Fig. 11 and its efficiency can be shown to be

$$\eta_G = \frac{\pi}{4}\left[\frac{1}{sin\alpha_1 + \ldots + (sin\alpha_{i+1} - sin\alpha_i)cos\alpha_i + \ldots + (1 - sin\alpha_{n-1})cos\alpha_{n-1}}\right] \tag{2.11}$$

where $sin(\alpha_i) = \frac{V_{DDi}}{V_{DDN}}$ and each of the V_{DDi}'s i=1,2,... n. are the n-supply levels. and α_i's are the corresponding phases of sine wave as defined.

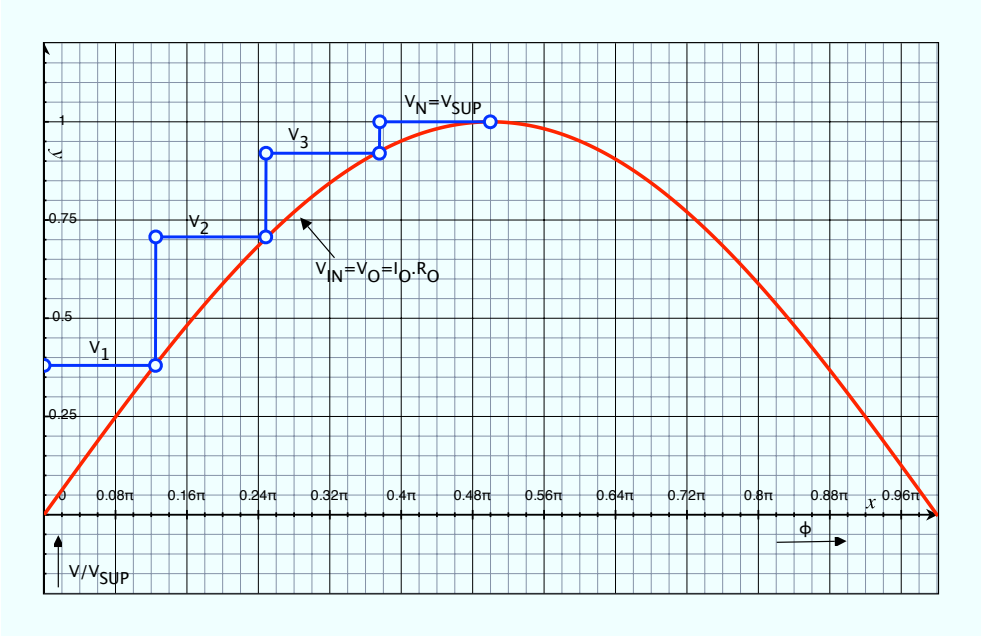

Fig. 11. Supply and output voltages in a multi-level Class-G amplifier

5. Class-D

With the nearly ideal kind of analysis of amplifiers we have been doing to achieve the classical efficiency numbers, Class-D amplifiers should have 100% efficiency as the output of the power amplifier either sits on the positive rail or the negative rail giving no scope for any power loss. The output is passively filtered to get the output voltage. But nothing is ideal, there will be losses due to dynamic consumption, leakage and finite on-resistance of power switches.

6. Class-H

As the number of supply levels(n) in the multi-level Class-G amplifier tends to infinity, it becomes a Class-H amplifier. Ideally Supply should look same as the output. But in reality supply will take some kind of modulated form depending on the input. The fundamental difference between Class-G and H is illustrated in the figures Fig. 12 and Fig. 13. Both Class-G and Class-H are similar in concept of improving efficiency in a different implementation. Class-H amplifiers are still far from practicality, to interest researchers because generating a supply modulated by input will in itself have very bad efficiency.

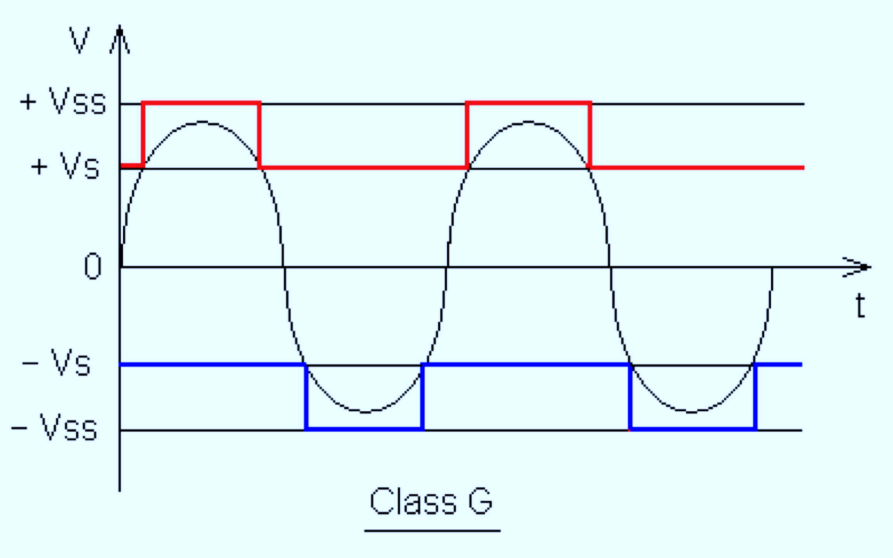

Fig. 12. Class-G operation

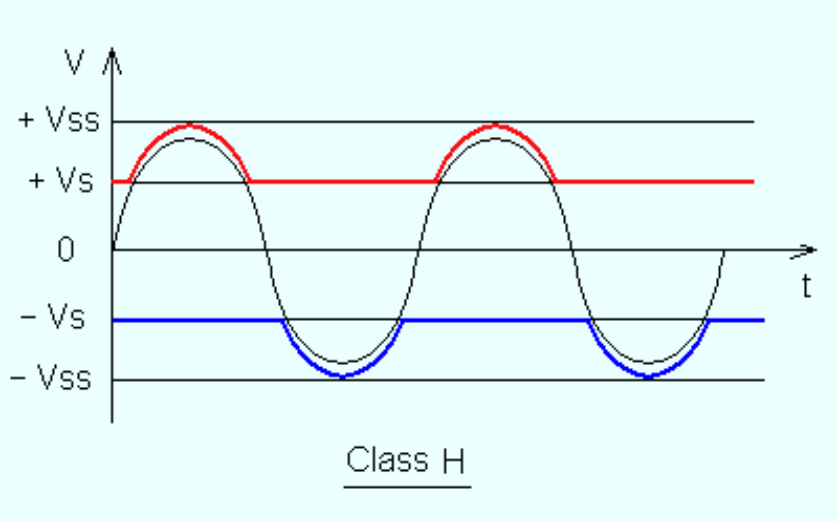

Fig. 13. Class-H operation

B. Crest factor of audio signals and its importance

The crest factor or peak-to-average ratio (PAR) or peak-to-average power ratio (PAPR) is a measurement of a waveform, calculated from the peak amplitude of the waveform divided by the RMS value of the waveform. It tells us something about the power distribution across amplitudes in a signal. The audio signals are known to have crest factors in the range of 12-20dB. Music has a widely-varying crest factor. Typical values for a processed mix are around 4-8 (which corresponds to 12-18 dB of headroom, usually involving audio level compression), and 8-10 for an unprocessed recording (18-20 dB). Which means the average amplitude of an audio signal is 4-10 times smaller than its peak value. The crest factor of our standard test signal sine/cosine wave is $20log(\frac{V_{o,pk}}{V_{o,rms}}) = 20log(\sqrt{2}) = 3dB$.

Why do we care about it? Because the efficiency of an amplifier depends sub-

stantially on the input signal. When the value of output voltage is $0.9 * V_{SUP}$ and assuming the total current taken from supply is completely delivered to the load the instantaneous efficiency is 90% and it is only 10% when the output voltage is $0.1 * V_{SUP}$. The Class-AB efficiency derived in equation (2.8) is 78.54% for a rail-to-rail sine wave, it drops by 50% to 39.27% for a sine wave with half its amplitude. The conclusion is the power distribution across different signal levels in an audio signal is very different from that of a sine wave just from the knowledge of their crest factor. In the next section we dig further into the actual amplitude distribution of audio by examining some test signals to understand how the efficiency of an amplifier can be maximized in the true sense. Soon we will realize how far the classical definition of efficiency is from reality.

C. True efficiency

True efficiency of an amplifier can be defined only with respect to a signal or set of signals with similar amplitude distribution function(*adf*) which will be defined later in this chapter. We use the instantaneous efficiency curves of various amplifiers along with amplitude distribution functions of some typical audio signals to demonstrate the range of true efficiencies for various classes of audio amplifiers.

1. Instantaneous efficiencies of Class-AB/G/D

Instantaneous efficiency is efficiency of the amplifier at a given instant. Instantaneous efficiencies of ideal Class-AB (Fig. 14) and Class-G (Fig. 15) amplifiers are shown in Fig. 16. They are pretty simple and straight forward to understand. Assuming all the supply current is being delivered to the load, the instantaneous efficiency of the class-AB amplifier is just V_{OUT}/V_{SUP} and is a straight line which goes from 0 to 1 as

the normalized input signal goes from 0 to 1.

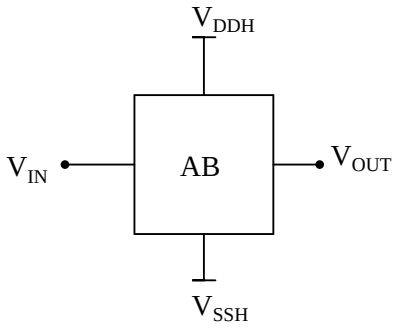

Fig. 14. Class-AB amplifier block diagram

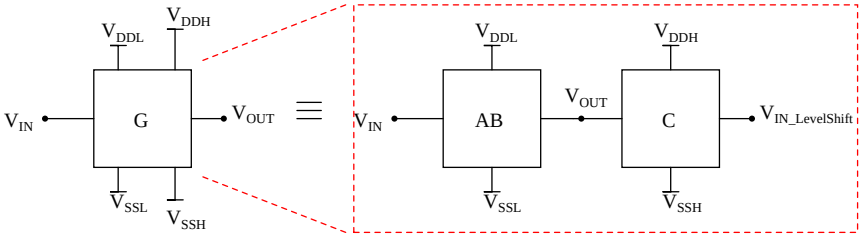

Fig. 15. Class-G amplifier block diagram

The instantaneous efficiency curve of Class-G can also understood very similarly. Now that output is driven from the smaller supply till it exceeds the smaller supply. The efficiency reaches 100% when the output equal to smaller supply then it drops to $\frac{V_{SUP\_LOW}}{V_{SUP\_HIGH}} X 100$ and follows the Class-AB curve as there is no more difference between Class-AB and Class-G. In the example curve shown the lower supply is 40% of the larger supply, hence use see the peak in Class-G efficiency at 0.4 normalized signal value.

Figure 17 gives a more realistic instantaneous plots of Class-AB/G/D amplifiers. The Class-AB and Class-G plots include a small quiescent current and the V_{DSAT}

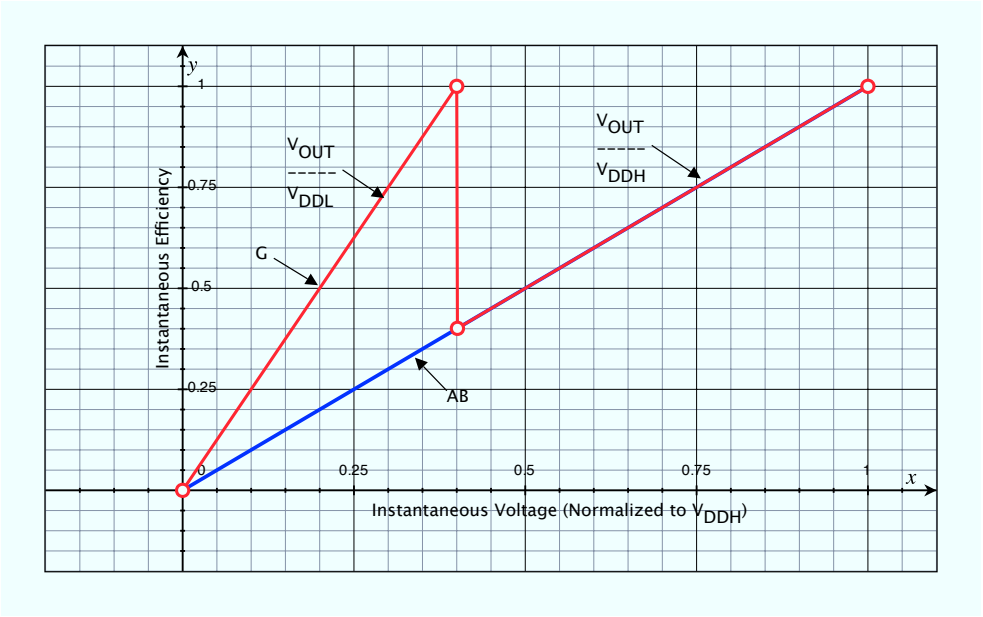

Fig. 16. Instantaneous efficiencies of ideal Class-AB/G amplifiers

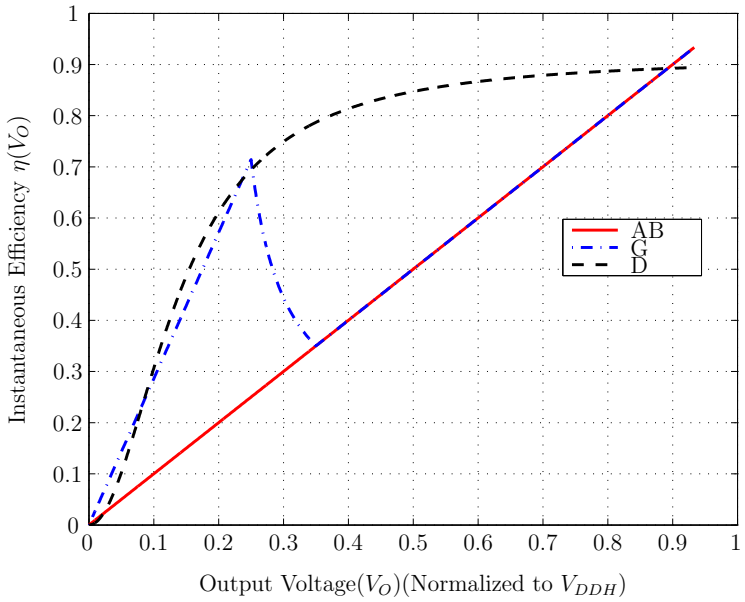

Fig. 17. Instantaneous efficiencies of real Class-AB/G/D amplifiers

influence of the drivers making the peak acceptable amplitude to about 90% of V_{SUP}. The effect of V_{DSAT} of smaller driver in Class-G also limits the intermediate efficiency peak from reaching 100% as in the ideal case. The instantaneous efficiency plot for Class-D is just an estimate from the typical efficiency vs. amplitude plots (might not be 100% accurate). These are the instantaneous efficiencies used in calculating the true efficiencies of these amplifiers in the last section of this chapter.

Figure 17 shows that Class-D amplifiers have better efficiencies at almost all signal levels. Yes, that is right and that is the reason why as discussed in chapter 1, Class-D amplifiers are a better choice when it comes to large loads and in places where there are no EMI concerns .

2. Amplitude distribution function of some typical audio signals

Amplitude distribution function $adf(V_o)$ has been defined as the probability of occurrence of signal with value V_o and has the units V^{-1}. This value will tell us the fraction of time the input/output of the amplifier will spend at that particular voltage level. If we plot the *adf* of a square wave with two levels one at 0 and the other at +ve rail and 50% duty cycle, we will have two impulses each with magnitude 0.5 at 0 and 1(since the signal is normalized to peak). A rail-to-rail triangular wave being a linear increase or decrease the *adf* is like uniform distribution. It spends equal fraction of time at all signal levels as shown in Fig. 18. The *adf* of a rail-to-rail sine wave has been shown in the Fig. 18. It can be seen, a sine wave spends greater amount of time closer to its peak (signal is normalized to this value) ($\phi = \frac{\pi}{2}$). This is intuitive as the rate of change of sine wave (derivative) is maximum at ($\phi = 0$) where the value of sine is zero and the rate of change is minimum at its peak. On the contrary audio signals spend most of the time and hence contain most of the energy in their lower signal levels. A set of typical audio signals have been analyzed and their *adf*'s

are presented in Figs. 19(melody) , 20(heavy beat), 21 (soft rock), 22 (club mix), 23 (rock), 24(classical), 25(more vocal). The genres mentioned are only for reference, depending on the actual signal the distribution may vary for any genre.

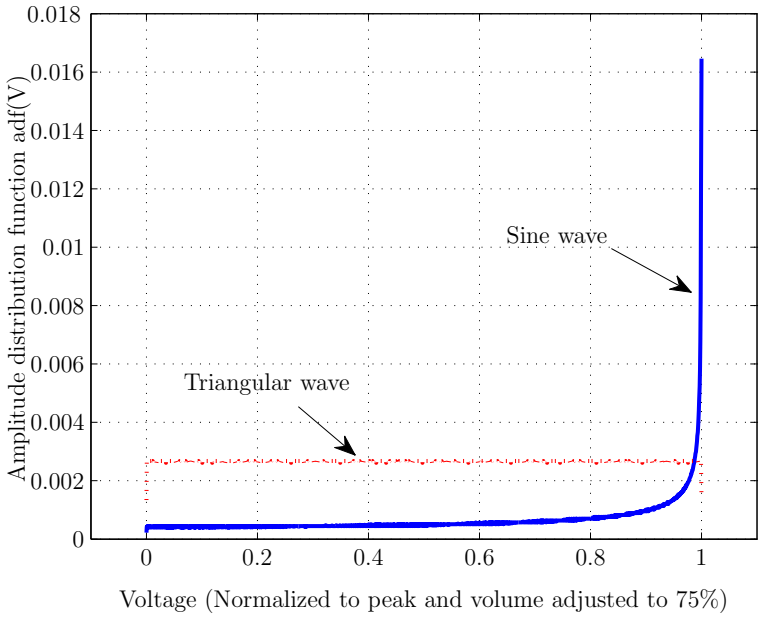

Fig. 18. Amplitude distribution function of sine wave

3. Power efficiency formula

It is not possible to calculate the efficiency of an amplifier in true sense for a very long and complex signal like audio using the classical approach presented in the first section of this chapter because the integrals become hopeless to compute. Here we derive a formula which uses the instantaneous efficiency of the amplifier and the amplitude distribution function of the signal to calculate a more meaningful number which denotes the true efficiency of that amplifier with that input signal. It gives us a realistic efficiency value for all the signals with similar amplitude distribution characteristics.

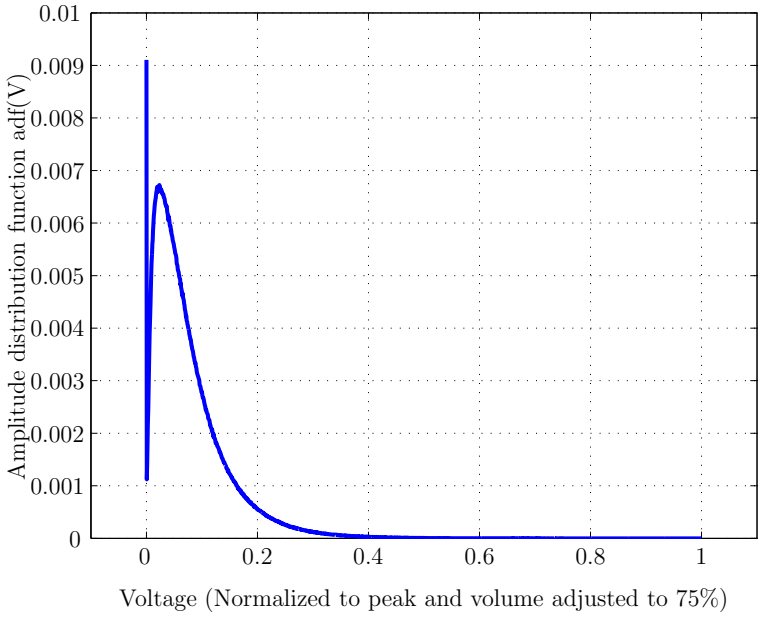

Fig. 19. Amplitude distribution function of Signal 1

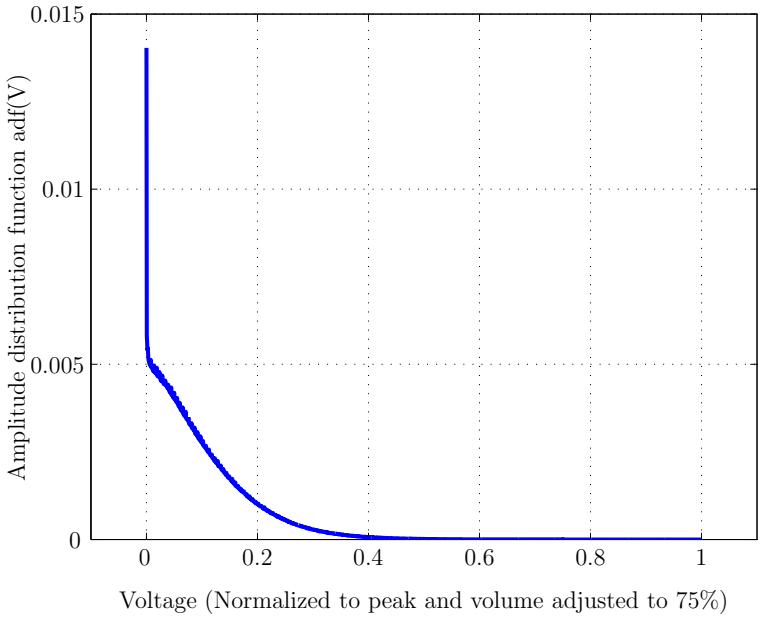

Fig. 20. Amplitude distribution function of Signal 2

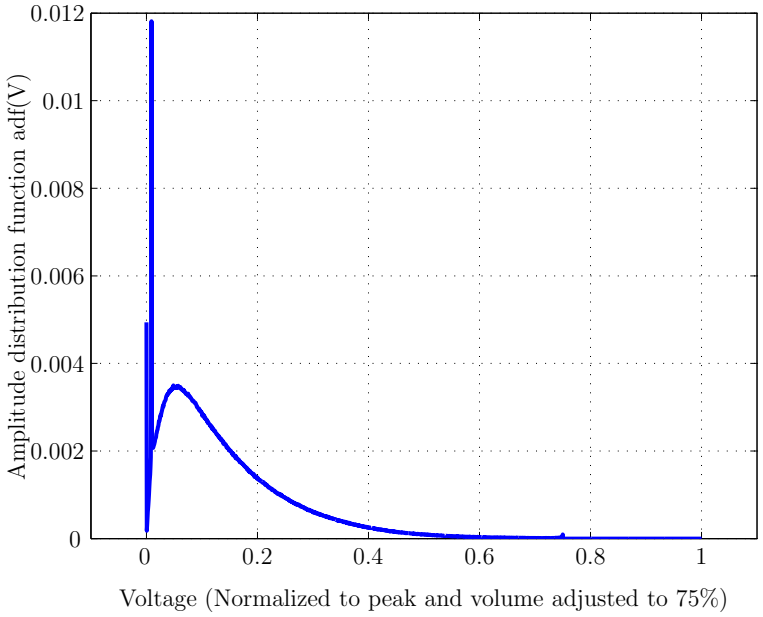

Fig. 21. Amplitude distribution function of Signal 3

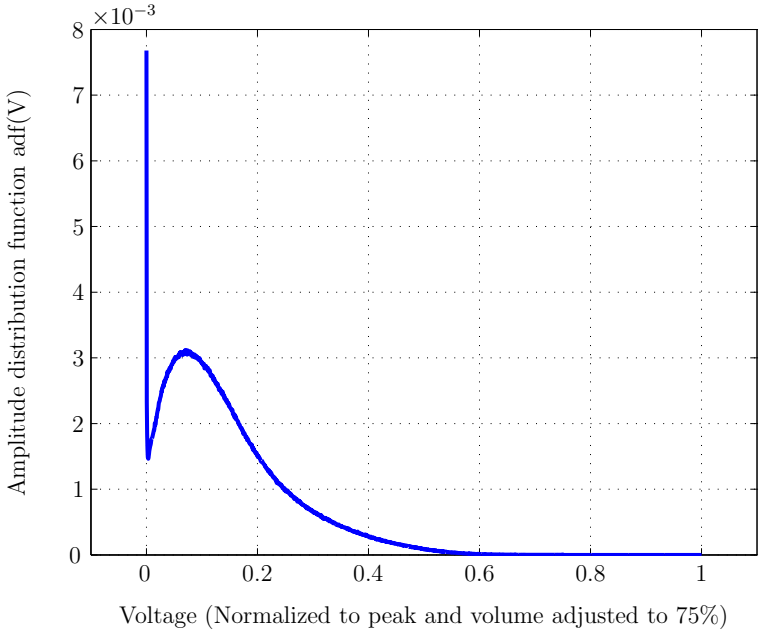

Fig. 22. Amplitude distribution function of Signal 4

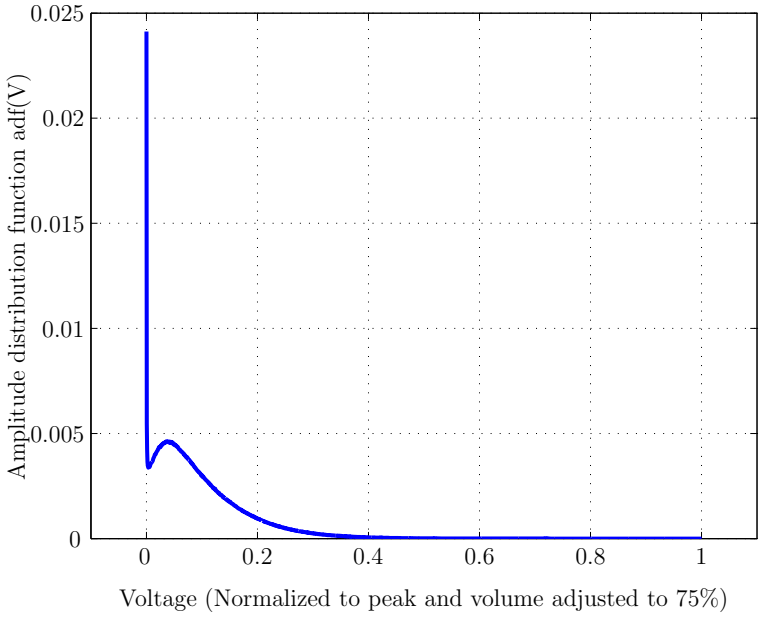

Fig. 23. Amplitude distribution function of Signal 5

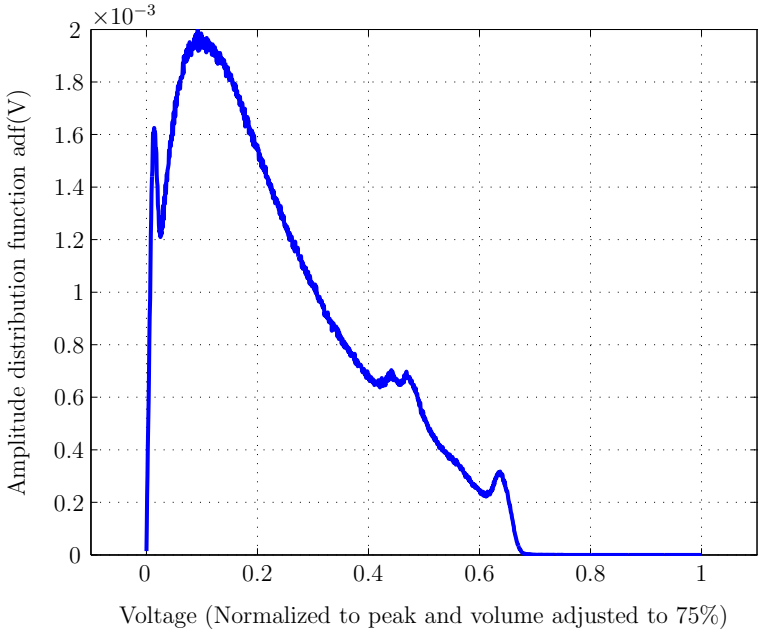

Fig. 24. Amplitude distribution function of Signal 6

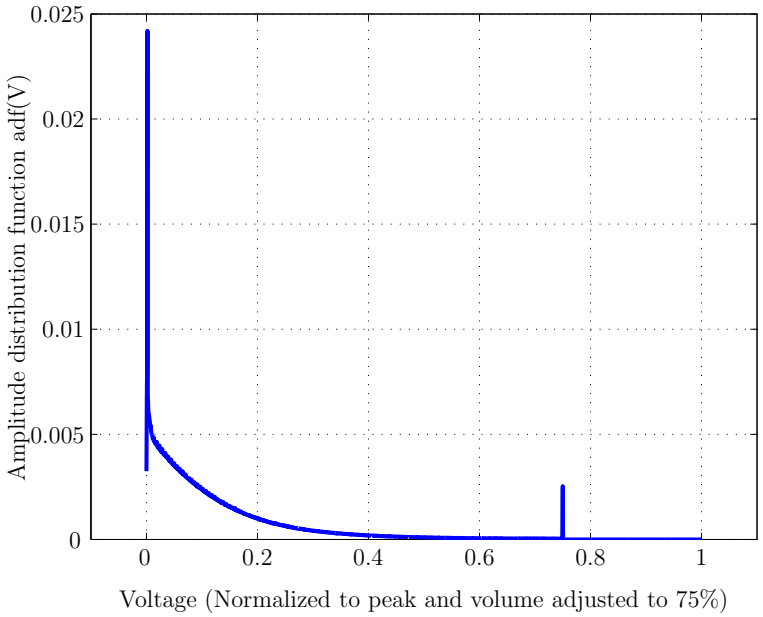

Fig. 25. Amplitude distribution function of Signal 7

If the instantaneous output voltage is V_o then the instantaneous power delivered to the load R_L is:

$$P_L(V_o) = \frac{V_o^2}{R_L} \tag{2.12}$$

and further if the instantaneous efficiency of the amplifier is $\eta(V_o)$ then the instantaneous power taken from the supply is:

$$P_{SUP}(V_o) = \frac{P_L}{\eta(V_o)} \quad for V_o \neq 0 \tag{2.13}$$

Now within the total duration of the signal if the signal spends $adf(V_o)$ fraction of time at level V_o then the total average power delivered to the load(R_L) is:

$$P_{_{L,avg}} = \frac{1}{R_L} \int_0^{V_{o,pk}} adf(V_o).V_o^2.dV_o \tag{2.14}$$

Extending the calculation to the total average power consumed from the supply is:

$$P_{_{SUP,avg}} = \left[adf(0).P_Q + \frac{1}{R_L} \int_{\substack{+\\0}}^{V_{o,pk}} \frac{adf(V_o).V_o^2}{\eta(V_o)}.dV_o \right] \tag{2.15}$$

where $adf(0)$ is the fraction of time spent at zero signal level and P_Q is the quiescent power consumption. This term has been taken out of the integral because when there is zero signal, the instantaneous efficiency is zero and the integral will be undefined.

Now using the above two equations (2.14)(2.15) we have the true average efficiency of the amplifier for the given signal as

$$\eta_{_{true}} = \frac{P_{L,avg}}{P_{SUP,avg}} = \frac{\int_{0}^{V_{o,pk}} adf(V_o).\frac{V_o^2}{R_L}.dV_o}{adf(0).P_Q + \int_{\substack{+\\0}}^{V_{o,pk}} \frac{adf(V_o).V_o^2}{\eta(V_o).R_L}.dV_o} \tag{2.16}$$

To illustrate the above efficiency formula we can use a simple example from Table II. Consider a signal with two phases of operation. The signal spends 40% of time in phase I and the system has an efficiency of 20% and consumes 100W during this phase. The signal spends 60% of time in phase II and the system has an efficiency of 80% and consumes 50W during this phase. The average power delivered to the load and taken from supply can be calculated as in equation 2.17. This gives us the effective efficiency to be 45.71%. The advantage with the above method is the complexity doesn't increase with length of the signal. Once the amplitude distribution characteristics are known we can calculate the true efficiency.

$$\begin{aligned} P_{L,avg} &= 0.4 * 0.2 * 100 + 0.6 * 0.8 * 50 = 32W \\ P_{SUP,avg} &= 0.4 * 100 + 0.6 * 50 = 70W \\ \eta &= 32/70 = 45.71\% \end{aligned} \tag{2.17}$$

Table II. Example demonstrating the power efficiency formula

Example	Fraction of time	Instantaneous efficiency	P_{SUP}(phase)
Phase I	40%	20%	100W
Phase II	60%	80%	50W

4. Comparison of practical efficiencies

The typical audio signals presented in the section C.2 of this chapter and the instantaneous efficiency plots of class-AB/G/D amplifiers presented in section C.1 are used with the efficiency formula and the following summary of comparison is obtained as shown in Table III. The user is assumed to be using the amplifier at 75% of maximum signal level. We can clearly see that Class-AB is far behind Class-G and Class-D for all kinds of signals. For the signals (1,2,5) in which the majority of power is concentrated in very small signal levels Class-G & D are very close in efficiencies. For the signals in which the power is reasonably spread out Class-D does only a little better than Class-G because of its better instantaneous efficiency for moderate to high signal levels as in Fig. 17. If the user uses the amplifier at a much lower (<50%) volume setting (input power level) then Class-G and Class-D will perform very close in terms efficiency as with signals (1,2,5) because the whole *adf*'s of the signals shrink down with reduction in volume.

5. Note on audio volume and efficiency

As we increase/decrease the playback volume, the amplitude distribution functions shown previously also expand/shrink along the signal axis. This means, it becomes

Table III. Comparison of efficiencies of Class-AB/G/D with application of typical audio signals

$\frac{Class}{Input}$	Class-AB	Class-G	Class-D
Sine	78.5%	81%	88%
Signal 1	13.4%	34.2%	31.2%
Signal 2	17%	40%	42%
Signal 3	23%	44%	57%
Signal 4	22%	43.3%	57%
Signal 5	16%	39%	40%
Signal 6	34%	48%	73%
Signal 7	25%	46%	55%

more and more important to improve the instantaneous efficiency at smaller signal levels when the devices are used at less volume. To maximally optimize the amplifier efficiency, the smaller voltage supply levels has to be dynamically scaled based on the user volume setting. This requires complex power management and is outside the scope of this work and is left for future research.

CHAPTER III

CLASS-G AMPLIFIERS

In this section, we take a look at the previous works on Class-G and then discuss the logical development of a high-performance circuit implementation of Class-G output stage from the basic Class-AB concepts and existing Class-G structures. Then we discuss various design choices and trade-offs involved in an optimum Class-G output stage design.

A. Previous work on Class-G

Though the idea of Class-G was first reported in Aug 1976, radio electronics journal. Questionable quality due to glitching commutation diodes [4] and the large amount of heat dissipation in them, kept the efficiencies very low. This kept it far from the interest of the researchers. A sample circuit from [4] is shown in Fig. 26. This figure shows a predriver and power stage in Class-G configuration. As in this example, majority of the existing solutions [11][12][10] are based on the basic class-AB source/emitter follower configuration shown in the figure on page 44 (more detail of this buffer configuration in next section) which has the fundamental drawbacks of low voltage swing due to $V_{GS(BE)}$ drop and large non-linearities. The $V_{GS(BE)}$ drop is also costly in terms of efficiency considering the small supply voltages used in present day technologies.

The following are Class-G implementations for other applications and are not very linear. Hence we only touch upon the useful ideas. The design presented in [13][14] is for a digital transmit line drivers but it proposes the concept of predictive switching which can be useful in the evolution of class-G. Using this idea by processing the digital audio data before it reaches the amplifier, we will have time to do efficient

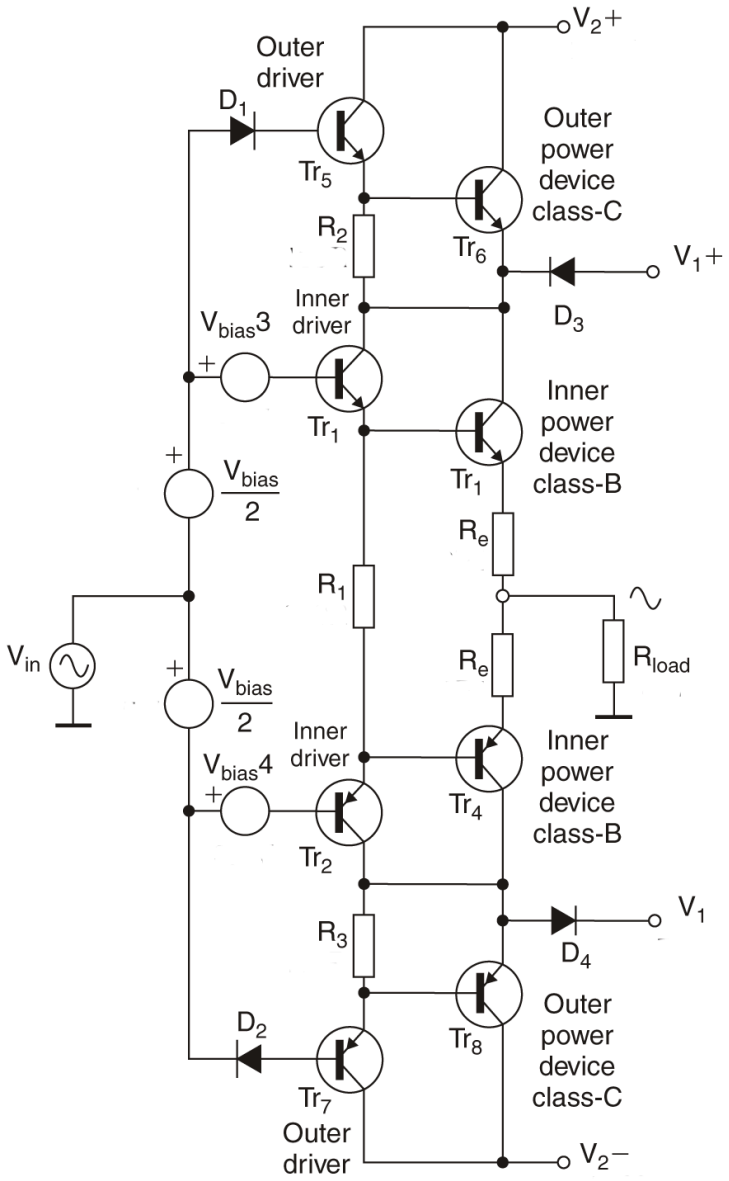

Fig. 26. Previous Class-G implementation-I

power management. The design in [15] shown in emphasizes on the idea of gradual switching, but the design as such overlooks the fundamental by using a class-A kind of structure which can't really improve the efficiency. There are other Class-G driver implementations in the literature intended for central office applications [16][17][18]. The main drawback of all these is that they are not intended to be very linear as audio amplifiers.

The latest Class-G implementation [19] fails to choose the smaller supply voltages optimally, which as we see in the chapter 2 is the most important to maximize efficiency. The block diagram of this circuit is shown in Fig. 27. It does brute-force switching between supplies, by forcefully turning on/off the parallel output stages with an external circuit. The parallel paths require separate compensation and hence double the required compensation capacitance.

There are a couple of Class-G commercial products, though not many details are known, here is a brief account of what has been done. [20] and [21] follow very similar approach to Class-G implementation. They have a single driver and the supply switching is done by the power management block. The major drawback with this approach is there is delay between the signal crossing the supply threshold and the power management circuit reacting with rail switching. This causes signal clipping and there will be distortion. The output stage linearity is marketed with not much mention about the clipping that happens when there is supply switching. [22] follows a parallel driver strategy and uses three rails (direct +ve supply and two -ve supplies generated using charge pump) for its 2.4W speaker amplifier. The main drawback is it is not ground referenced and requires DC blocking capacitors. The architecture of its output stage is not known as well.

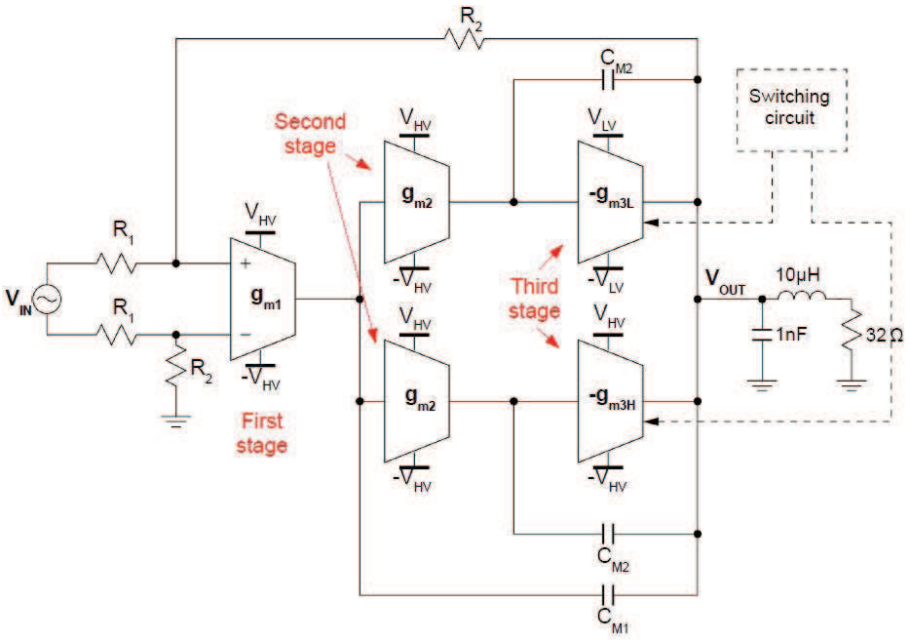

Fig. 27. Previous Class-G implementation-II

B. Series Vs Parallel Class-G structures

By the definition of Class-G, It is just an extension of Class-AB stage, where we improve on the efficiency by using a smaller supply voltage when the input/output signal level is low. There are two basic ways in which this can be realized: The 'series' implementation and the 'parallel' implementation are as shown in Figs. 28(A) and 28(B) respectively.

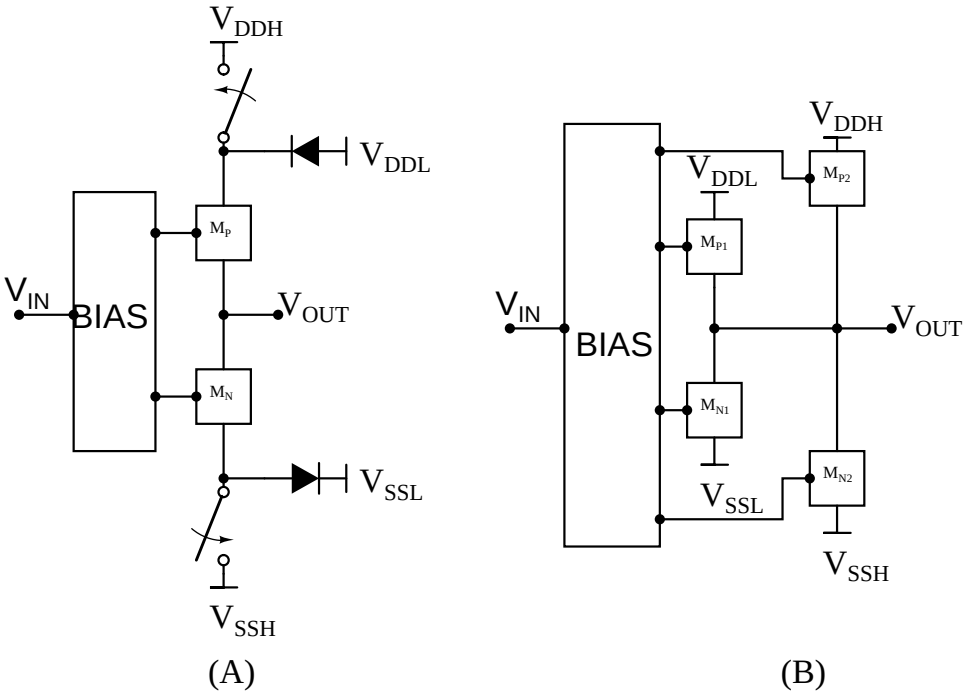

Fig. 28. Series and parallel type Class-G output stages

The most commonly used topology [11][12] is the series topology in Fig. 28A, when the output voltage is smaller than the lower supply the diode is forward biased and the switch connected to the higher supply is open, thus the output is driven by the lower supply through the forward biased diode and when the output voltage is higher than the lower supply the diode is reverse biased and the switch is closed, hence the

output is driven from the higher supply. The main drawback with this implementation is the forward biased diode drop in the smaller supply path can not be afforded in the present day low voltage portable electronics. Even if we have a specialized diode with small turn-on voltage V_{on}, the V_{on} of the diode directly affects the lower part of the instantaneous efficiency curve which we have seen is very important in the design of a Class-G stage.

The 'parallel' implementation [10] doesn't have the above drawback but takes considerably larger area compared to the series type because we now have four drivers instead of two. In today's market the efficiency of a design is more important than a fraction of silicon area. From here on in this work Class-G output stage always means 'parallel' type unless specifically stated.

In a Class-G output stage as long as the signal is smaller than the lower supply the smaller driver stage is active and when the signal is larger than the lower supply level, the bigger driver is active. To prevent powering up of the lower supply from the higher supply, the smaller driver should be turned-off and we will discuss more on ways to do it in the last section of this chapter. The switching between the supplies has to happen seamlessly, by adding no or only very little distortion, which is the most critical factor in audio amplifier design. Further in this chapter we will show how this has be achieved.

C. Class-AB: The corner stone for Class-G

With a closer look at the Class-G behavior, its not difficult to understand it is a normal Class-AB amplifier operating from the lower supply as long as the signal is smaller than the lower supply and when the signal becomes larger than the lower supply, the bigger driver stage of 'parallel' type implementation should become active. If we look

keenly, this is nothing but a Class-C behavior. In short, in a Class-G output stage, the signal is applied to both smaller driver stage(from lower supply) which is pure Class-AB type and bigger driver(from higher supply) which is of Class-C type.

As discussed in chapter 1, Class-A/AB/B/C are all the same output stage biased differently. Class-AB is biased with a little bias current and Class-C is biased such that the both the driver transistors of that stage will remain off for a significant portion of the signal about zero. Understanding this fundamental concept leads us to the obvious Class-G output stage implementation as shown in the Figs. 29 and 30. So now we can see Class-G as a Class-AB + Class-C(Level shift + driver).

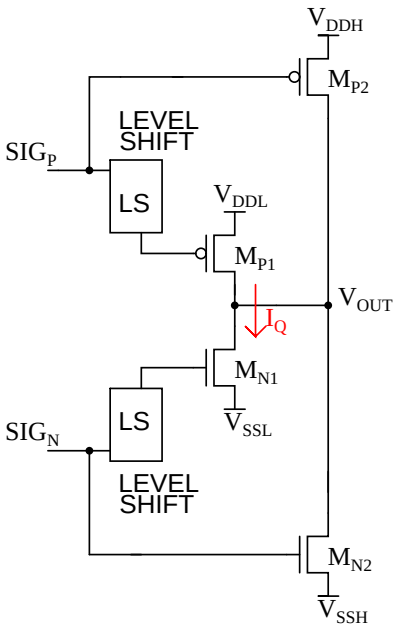

Fig. 29. Shift-in type Class-G output stage

The first of the two figures shown is 'shift-in' type as the signal is applied to the bigger driver stage and is shifted in using the level shifter to bias the smaller driver stage and similarly the second one is 'shift-out' type.

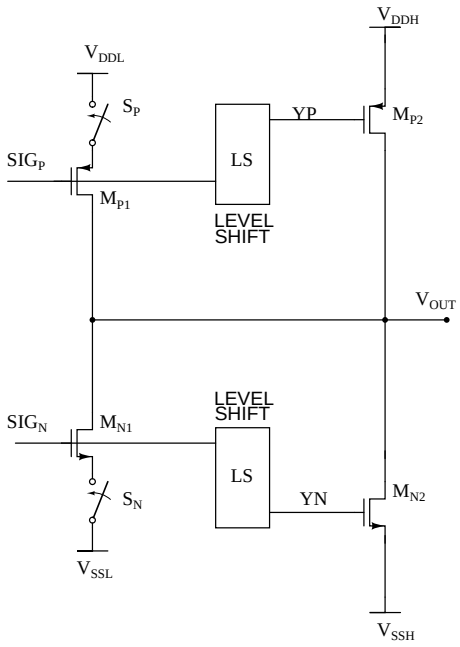

Fig. 30. Shift-out type Class-G output stage

An even closer look, reveals how much similar the design of a Class-AB output stage is to the design of Class-G. Class-G is just an extension of Class-AB: In a Class-AB output stage we have two driver transistors and one cross-over point about zero. Similarly in Class-G we have four driver transistors and three cross-over points at zero, V_{DDL} and V_{SSL}. Understanding this helps us in applying the existing linearizing techniques for Class-AB on Class-G.

1. Brief look at various Class-AB output stages

The most basic of Class-AB output stage is made up of PMOS and NMOS source followers with their sources joined at their output as shown in Fig. 31 biasing details are left out. The major drawback of this the output node can not go closer than one V_T to the rails as shown in equation 3.1, this poses a large drop in efficiency as shown

in equation 3.4 considering the small supply voltages in use. This was the most widely used topology in the past and almost all of the existing Class-G literature also uses this topology with BJTs.

$$\begin{aligned} V_{SIGP} &\leq V_{DDH} \\ V_{OUT} &= V_{SIGP} - V_{GS_{MN}} \\ => V_{OUT} &< V_{DDH} - V_{GS_{MN}} \end{aligned} \tag{3.1}$$

$$\begin{aligned} \eta_{inst_{max}} &= \frac{V_{OUT,max}.I_L}{V_{DDH}.I_L} \\ \eta_{inst_{max}} &= \frac{V_{DDH} - V_{GS_{MN}}}{V_{DDH}} \end{aligned} \tag{3.2}$$

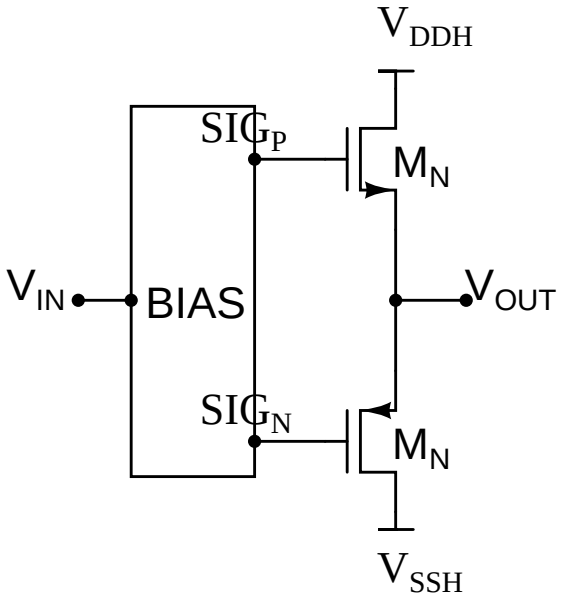

Fig. 31. Source follower Class-AB output stage

A much better Class-AB topology [23][24] formed by PMOS and NMOS common

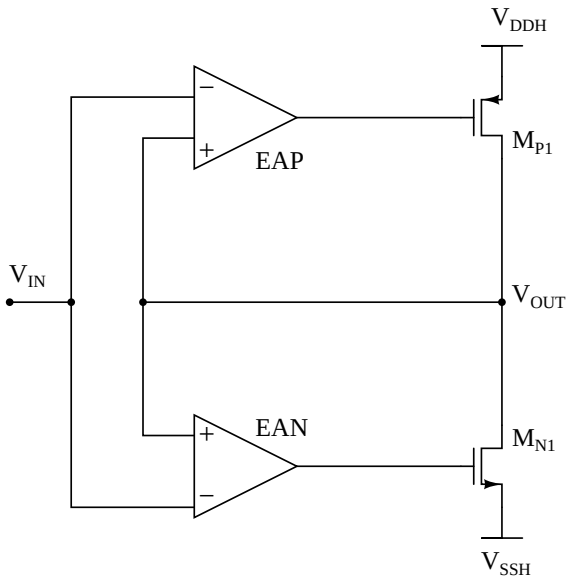

Fig. 32. Class-AB output stage with error amplifiers and common source devices

sources joined by their drains at the output as in the case of an inverter, but the biasing is such that only a little bias current flows through it. An example of such circuit can be seen in Fig. 32. The paradox is we are using the high output impedance and gain to close the loop and build an excellent buffer. In quiescent state the error amplifier outputs bias the driver transistors such that they conduct little current. When the input becomes positive the output voltage of the error amplifiers EAP and EAN drop and the PMOS M_{P1}will start driving the output such that it is equal to the input and the NMOS M_{N1} remains turned-off. When the input goes below zero, the vice-versa happens NMOS is active and PMOS is off. Unlike the buffer in Fig. 31 this one can swing as close as one V_{DSAT} to the rail as shown in equation 3.3 and this improves the maximum achievable instantaneous efficiency significantly.

For the transistor M_{N1} to be in saturation

$$\begin{aligned} V_{DS,MN1} &> V_{GS,MN1} - V_{T,MN1} \\ => V_{OUT} &> V_{G,MN1} - V_{T,MN1} \\ => V_{OUT} &> V_{DSAT,MN1} \end{aligned} \tag{3.3}$$

$$\begin{aligned} \eta_{inst_{max}} &= \frac{V_{OUT,max}.I_L}{V_{DDH}.I_L} \\ \eta_{inst_{max}} &= \frac{V_{DDH} - V_{DSAT_{MP1}}}{V_{DDH}} \end{aligned} \tag{3.4}$$

The problem with the circuit in Fig. 32 is poor control over quiescent current. To over come this there are advanced biasing schemes used in [25][26][27][28][29][30]. With any of these Class-AB design as base we can develop a class-G amplifier using parallel output stages and shift-in/shift-out level shifters to bias the bigger driver in Class-C mode making the whole setup to work in Class-G configuration as explained in previous section.

D. Important design choices

From the preceding sections, it should be clear why we choose Class-G parallel type output stage with common source type drivers. In this section, we will look at some of the quantitative design considerations of this kind of Class-G output stage.

1. V_{DSAT} of smaller drivers

The fact that instantaneous efficiency curve of Class-G as in Fig. 33 at the lower signal levels is very important in maximizing the overall efficiency because the audio signal spends a major faction of time at small signal levels. Understanding the impact of V_{DSAT} of smaller drivers is needed for optimum design.

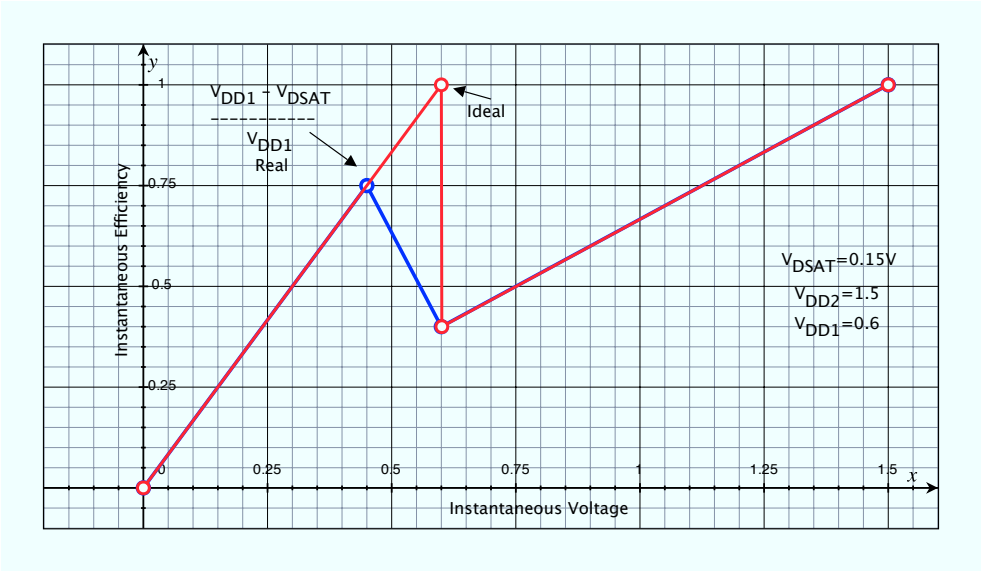

Fig. 33. Effect of V_{DSAT} of smaller drivers

Figure 33 shows the Class-G instantaneous efficiency curves ideal and $V_{DSAT} = 150mV$. In case of ideal Class-G the instantaneous efficiency reaches 100% at $V_{IN} = V_{DDL} = 0.6$ whereas in case of real Class-G the peak instantaneous efficiency is about $\frac{V_{DDL}-V_{DSAT}}{V_{DDL}}$ which is equal to 75% in this case. When the signal is greater than $V_{DDL} - V_{DSAT}$ the smaller driver goes into triode and to keep the distortion low the bigger should start driving the output, hence the efficiency drops from here on. When the output signal crosses V_{DDL} the efficiency curve starts following the original one. When the output signal level is between $V_{DDL} - V_{DSAT}$ and V_{DDL} we assumed linear handover from smaller driver to larger driver (first order approximation).

$$\frac{I_{pk}}{I_Q} = \left(\frac{V_{DSAT,max,pk}}{V_{DSAT,min,Q}}\right)^2 \tag{3.5}$$

Minimizing $V_{DSAT,max,pk}$ of driver when peak load current (I_{pk}) is flowing through smaller driver may seem to be an obvious choice but it is limited by the quiescent

current budget. The peak current taken from the smaller driver is defined by the smaller supply voltage and the minimum V_{DSAT} of driver transistors in quiescent state ($V_{DSAT,min,Q}$) is limited by the process variation of V_T. If we choose to bias the drivers in deep sub-threshold (to minimize $V_{DSAT,min,Q}$) in quiescent condition, then any smaller V_T variation will be amplified into huge variation in I_Q by the large g_m of driver (due to its size). The equation (3.5) now shows that the quiescent current I_Q and $V_{DSAT,max,pk}$ (which affects the efficeincy peak we discussed) are inversely proportional. A careful choice of $V_{DSAT,max,pk}$ has to be made for an optimal design.

For example if we have $V_{DDL} = 0.6V$ and the V_T variation with process and temperature is about 50mV. It is safer to choose 75mV or more as the $V_{DSAT,min,Q}$. Now I_{pk} is roughly defined by the smaller supply voltage value and load impedance (32Ω) and is equal to $0.6V/32\Omega = 18mA$. Now using these the possible values for I_Q & $V_{DSAT,max,pk}$ are shown in the Table IV.

Table IV. V_{DSAT} and I_Q trade-off.

I_Q	$V_{DSAT,max,pk}$
200μ A	0.7V
800μ A	0.35V
2mA	0.23V

2. Smaller supply and instantaneous efficiency

One of the most important design choices to make is the choice of smaller supply. The main reason to use a smaller supply is to improve the efficiency. So it is essential to understand the impact of smaller supply on the over all efficiency which in turn

can be understood by understanding its impact on instantaneous efficiency.

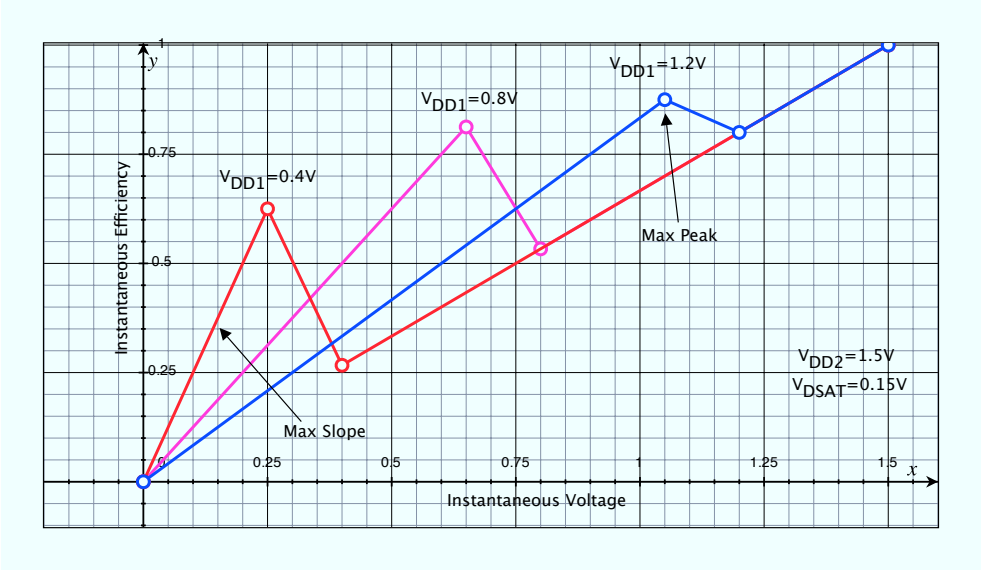

Fig. 34. Effect of smaller supply

Figure 34 shows instantaneous efficiency curve for three different smaller supply values. It can be seen that, for a given smaller driver V_{DSAT} the intermediate peak in the instantaneous efficiency curve increases with the smaller supply value, where as the slope of the lower part of the instantaneous efficiency curve decreases. It must be remembered that we have to maximize the overall efficiency and not the intermediate peak.

From our analysis of audio signals in chapter 2, we can observe that most of the audio power is concentrated in the signal levels less than 30-40% of the maximum. So the region from 0 to 30-40% of higher supply level should have the maximum possible efficiency. Hence, it is optimum to choose the smaller supply level to be about 40-45% of higher supply level. This ensures that we are driving most of the signal power with the best possible efficiency. This is way far from the classical calculation which yields

71% ($sin(\pi/4)$).

3. Number of supply levels (Multi-level Class-G)

Is it beneficial to use a multi-level class-G? What if we have three supplies instead of two. We will need to generate six supplies instead of four. They do not come for free, each will have efficiency loss from a regulator or charge pump. Further there will need for an additional driver stage, the effect of its V_{DSAT} and not to forget two additional cross-over points adding distortion. A brief comparison of two level vs. three level class-G is presented in the Table V. It is not a great idea to use any more than two levels of supply. An optimum choice of lower supply level does much more good than going for a multi-level class-G.

Table V. Two level supply vs three level supply comparison

	Two level	Three level
Supplies	4(less η loss)	6(more η loss)
Drivers	4(less area)	6(more area)
$V_{DSAT}\eta$ loss	at 1 smaller driver	at 2 smaller drivers
Complexity	average	high
Overall η	Comparable or two level is better	

E. Linearity

We know that in Class-AB amplifier the major sources of non-linearity are the cross-over distortion and the triode non-linearity when the output is driven close to the rail. To minimize the cross-over distortion some quiescent current is burnt and the triode

non-linearity is left as a trade-off for smaller die area as it shows up only occasionally when the signal is too large.

Extending this to Class-G we have cross-over distortion arising from three points and the triode non-linearity is also present. The cross-over at zero crossing is minimized by burning some quiescent current as in Class-AB. The bigger drivers should be biased such that they start delivering a portion of current to the load when the smaller drivers reach triode region. This minimizes cross-over distortion near the smaller supply levels.

It is not practical to mathematically analyze the distortion since the output MOS transistors operate in all three possible regions of operation during one cycle of a sine wave input. But some insight is required in order to design optimally, even when we are taking the help of simulator. So, let us take a look at the Closed loop amplifier.

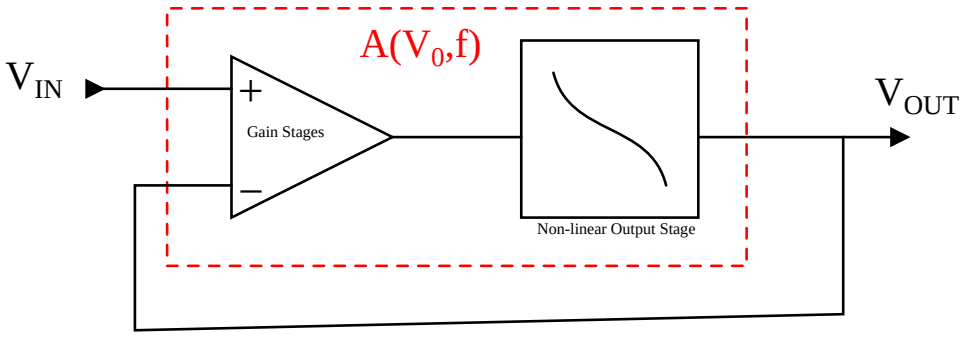

Fig. 35. Audio amplifier block diagram

The most important of all in linearizing the circuits, is the use of negative feedback. It is known to suppress the second harmonic approximately by the square of loop gain (improve HD2 by loop gain) and suppress the third harmonic by approximately cube of loop gain (improve HD3 by square of loop gain). Let us get an intuition of why this happens using first order approximation with out going into

cumbersome mathematics. Here in Fig. 35 we show the model of an audio amplifier, with a gain stage and a non-linear output stage(Can be Class-AB or G). The total gain of audio amplifier is $A(V_o, f)$, it is obviously a function of frequency (f) as is any other amplifier and in this case also a function of output voltage (V_o) as the output stage is non-linear(the g_m of output stage can vary by about 10-50X with output voltage). As long as the system is stable we know

$$\begin{aligned} (V_{in} - V_o).A &= V_o \\ Err = V_o - V_{in} &= \frac{-V_{in}}{1+A} \end{aligned} \tag{3.6}$$

Let us say we have a constant frequency sine wave input to the system and the $min[A(V_o)]$ is 60dB, then following the above equation the ratio of input to the error between input and output at that frequency will be greater than 60dB, no matter how non-linear the output stage is. So then what happens to all the non-linearity generated? It is spread in to the higher frequency harmonics just as in delta-sigma modulator noise shaping. The conclusion is the open loop gain of the audio amplifier in the band 20-10kHz is of prime importance in achieving high linearity. Why 10kHz and not 20kHz? Because all the harmonics of any frequency greater than 10kHz falls outside the audible spectrum.

The open-loop gain can be used to explain the above two mentioned sources of non-linearity. The crossover distortion occurs because, when there is no quiescent current the g_m of the output stage becomes too low reducing the open loop gain. The same thing happens when one of the driver enters the triode-region; the loop gain drops and the distortion error increases. It should be understood that increasing the gain in the preceding stages lets us reduce the crossover distortion (or the quiescent current) and also triode distortion. This is a very important trade-off between

linearity, quiescent current and power in the amplifier.

F. SR of amplifier and comparators

The maximum rate at which an audio signal changes determines the slew rate specifications. Consider the sine wave with amplitude A_m and frequency f_{in}. The maximum rate at which it can change is given by:

$$\begin{aligned} V &= A_m.sin(2.\pi.f_{in}.t) \\ \frac{\Delta V}{\Delta t} &= A_m.2.\pi.f_{in}.cos(2.\pi.f_{in}.t) \\ SR = \frac{\Delta V}{\Delta t}_{max} &= A_m.2.\pi.f_{in} = A_m.\omega_{in} \end{aligned} \tag{3.7}$$

$$SR \geq V_{DDH}.2.\pi.(20kHz) \tag{3.8}$$

For an audio signal this can be obtained by using $A_m = V_{DDH}$ and $f_{in} = 20kHz$. The slew rate at all internal nodes of the multi-stage amplifier should be better than the above obtained value in the equation (3.8).

The comparators we use to turn-off the smaller driver stage when input crosses the lower supply level should act faster than the rate at which the signal changes in order to prevent any glitches which fall in the signal band. Hence the slew rate of the comparator should be 3 to 4 times the signal SR derived in the equation (3.8).

CHAPTER IV

CLASS-G IMPLEMENTATION

In this chapter, we propose and discuss two Class-G circuit topologies. It is never like the whole concept is defined and the implementation is found. Both go together or in some cases the concept is developed from a crude form of implementation as in this case. The Class-AB amplifier with two error amplifiers explained in the previous chapter seemed most obvious choice to easily extend it into a Class-G stage. Having worked for a while on its implementation, various insights into the design have been developed. So we discuss this as the first circuit topology for easier understanding and then present the refined implementation which uses modified Class-AB biasing schemes.

A. Circuit topology 1

The Class-G circuit topology which is an extension of the Class-AB with error amplifiers in Fig. 32 is shown in the Fig. 36. Where EAP & EAN are the error amplifiers, M_{P1} & M_{N1} forms the smaller driver stage, M_{P2} & M_{N2} forms the larger driver stage and M_{PL} & M_{NL} form the shift-out level shifters.

1. Design and working

The output of the error amplifier EAP (XP) is connected to the gate of PMOS M_{P1} and the output of the error amplifier EAN (XN) is connected to the gate of NMOS M_{N1} and these are biased such that the smaller driver stage sinks the predetermined quiescent current when $V_{IN} = V_{OUT} = 0$. The level shifters in the second stage make $V_{YP} = V_{XP} + V_{SG,M_{PL}}$ and $V_{YN} = V_{XN} - V_{GS,M_{NL}}$. This amount of level shifts should be such that the PMOS M_{P2} and NMOS M_{N2} in the second stage are in cut-off region

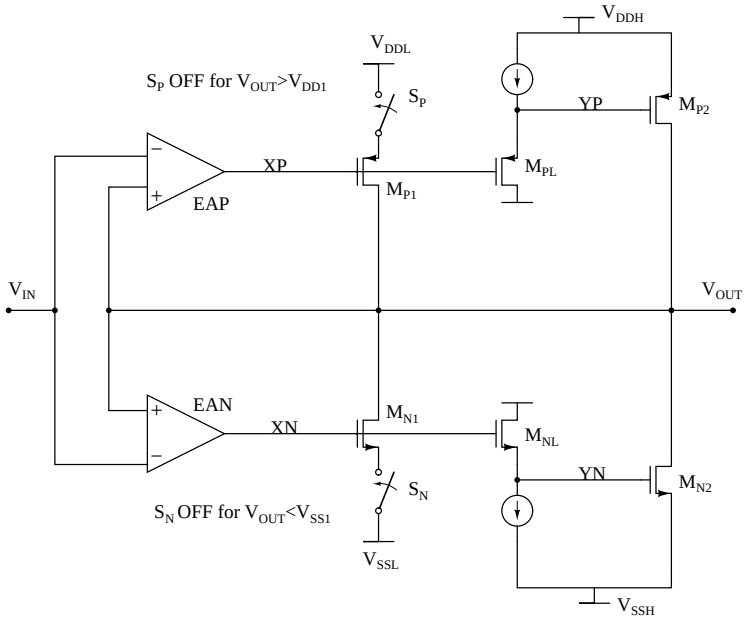

Fig. 36. Class-G circuit topology-1

for $V_{OUT} < V_{DDL}$ and $V_{OUT} > V_{SSL}$ respectively.

As the input voltage increases the PMOS M_{P1} in the first stage pulls up the output and V_{IN} remains equals to V_{OUT} during this V_{XP} changes very little as long as M_{P1} is in saturation. When V_{OUT} starts getting close to V_{DDL}, M_{P1} starts moving towards triode region reducing the gain of M_{P1} at this point V_{XP} starts dropping and this brings the PMOS M_{P2} of second stage into saturation and further the negative feedback keeps V_{IN} equal to V_{OUT}. The same process occurs when the input goes downwards from zero to V_{SSH}. Care should be taken to bias all the driver transistors and level shifters as desired. Figs. 37 & 38 explain the working of this topology when $0 < V_{OUT} < V_{DDL}$ and $V_{OUT} > V_{DDL}$. The working is similar in the negative direction as well. EAP is a folded cascode with NMOS input to efficiently handle the positive voltage levels and likewise EAN is a folded cascode with PMOS inputs.

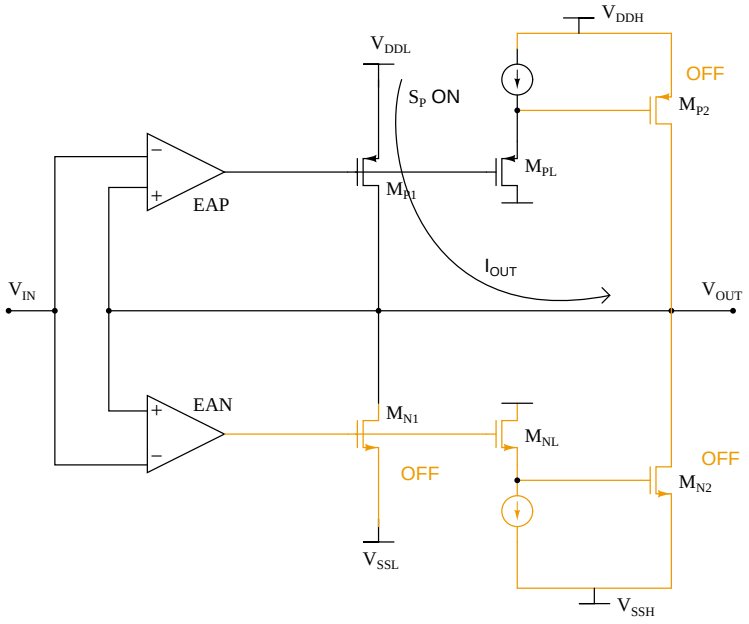

Fig. 37. Working of Class-G circuit topology-1 for $0 < V_{OUT} < V_{DDL}$

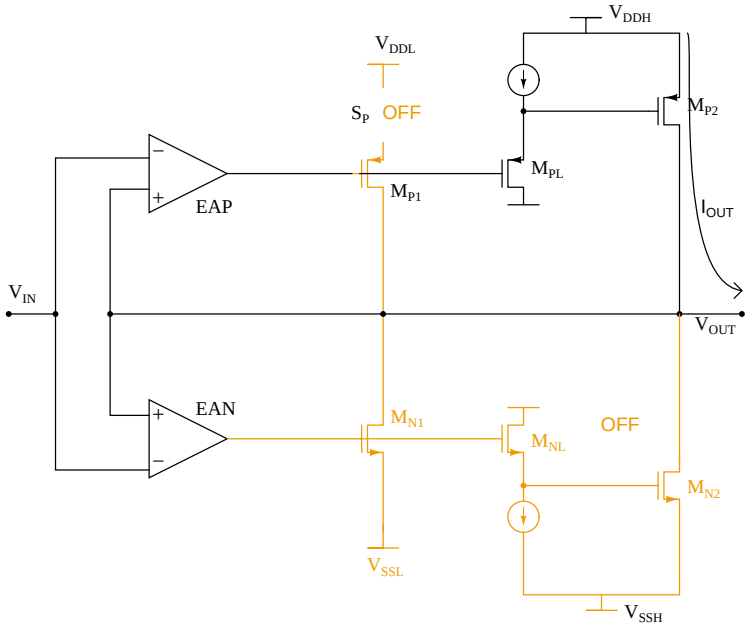

Fig. 38. Working of Class-G circuit topology-1 for $V_{OUT} > V_{DDL}$

Folded cascode topology is chosen to get wide swing at V_{XP} and V_{XN} nodes.

The circuit topology is like a two stage amplifier with only one dominant pole at the output of the error amplifiers. The output pole($f_o = 1/2.\pi.R_L.C_L = 24.86MHz$) is relatively a high frequency pole (for audio amplifier working in 20Hz-20kHz range) as the load impedance is $32\Omega \& 200pF$ only. In case if a little compensation is required to meet stability under all conditions small capacitors can be added at the outputs of error amplifiers on nodes V_{XP} & V_{XN}.

The switches S_P & S_N operate in deep triode region when ON. These are required to avoid the current flowing from V_{DDH} to V_{DDL} when $V_{OUT} > V_{DDL}$ or from VSSL to VSSH when $V_{OUT} < V_{SSL}$. These switches are large in order to reduce the ON-resistance as they are in the load current path and can hurt the efficiency. Placing the switches at the gate of the smaller driver reduces the size of these switches. But, unfortunately in the present design, it is not possible to place the switches at the gate of the drivers because the loading on the error amplifier changes from smaller driver to a level shifter causing large change in the load capacitance of error amplifier and causes instability. To avoid this the switches are place at the sources.

The major drawback with this comes for the original Class-AB itself. The drivers are biased with the output of the error amplifiers, any random offset(due to process variations) in them can cause large changes the quiescent current (because the drivers are huge and have large transconductance). For 1.5V supply and 32Ω load using a NMOS with $\mu_n.C_{ox} = 120\mu A/V^2$ assuming a overdrive of 250mV (at peak load current) the NMOS driver is as big as W=7.5mm and L=0.6μm (The PMOS will be about three times as big). It is very essential to have good control on the quiescent current when designing a high efficiency amplifier.

2. SNR and noise requirements

The SNR requirements of the audio system determines the Noise requirements of the whole amplifier. The total input referred noise of the amplifier will be dominated by the first stage of the amplifier. In the case of our circuit, EAP and EAN act as first stage for half cycle each. So we have to meet the noise requirements on both the amplifiers. Both EAP and EAN are folded cascode amplifiers, one with PMOS input pair and the other with NMOS input pair. So the analysis of one can be extended to other. First, lets derive the noise requirements of the amplifier from SNR specification=90dB. If we design the amplifier for maximum signal swing of $1.2V_pk$, the we have a total integrated noise requirement of 38uV (equation 4.1) in the audio band of 20-20kHz.

$$\begin{aligned} \frac{S}{N} &= 20log(\frac{1.2}{N}) = 90dB \\ N &= 38uV(Audio - band) \end{aligned} \tag{4.1}$$

For the folded cascode amplifier which is the first stage of circuit in page 69, the total input referred noise power density can be shown to be the one in equation 4.2. This calculation ignores the noise added due to tail transistor assuming matching and also neglects the noise added by cascode devices considering the relatively low frequency of operation.

$$\bar{v}_{i,n}^2 = 2\left[\bar{v}_{g1,n}^2 + \left(\frac{g_{m3}}{g_{m1}}\right)^2 \bar{v}_{g3,n}^2 + \left(\frac{g_{m7}}{g_{m1}}\right)^2 \bar{v}_{g7,n}^2\right] \tag{4.2}$$

where (all symbols have their usual meaning and i=1,3,7)

$$\bar{v}_{gi,n}^2 = \frac{4kT\gamma}{g_{mi}}\Delta f(thermal) + \frac{K.F_p.\Delta f}{2.\mu.C_{ox}.W.L.f}(flicker) \tag{4.3}$$

Since the audio amplifiers are low frequency amplifiers flicker noise becomes a major issue. As we design the amplifier for high gain (70dB) transconductance and size of the input pair will be maximized. This helps significantly in reducing the flicker noise contribution of input differential pair M_1 and also in suppressing the noise contribution from M_3 and M_7. One important element which contributes significant amount of noise and which is often overlooked is the flicker noise of NMOS current source M_3. Though it gets divided by the transconductance of input pair, it still remains significant. Being a NMOS sinking a small current just enough to meet the SR requirements it tends to be smaller in size contributing to large flicker noise. This problem can be overcome by using large lengths keeping the W/L ratio constant. Also degenerating these current sources will help to some extent, not to forget the thermal noise of degeneration resistors gets added.

3. Step by step sample design procedure

Since the circuit has significant non-linear behavior (open loop), the design procedure is largely iterative. The step by step procedure presented here is only for reference.

Step 1: Choose the V_{DDH} depending on the technology. In this case we choose 1.5V. The V_{DDL} should be chosen at about 40-50% of the V_{DDH} as explained in the second chapter for optimizing efficiency. For portable applications the load impedance is either 32Ω or 16Ω. For demonstrating the concept we choose 32Ω.

Step 2: With a reasonable choice of V_{DSAT} =250mV for bigger driver M_{N2} at peak load current $I_{OUT,max} = 1.5V/32\Omega = 46.8mA$ we can size the driver M_{N2} to be W=7.5mm and L=0.6μm as explained above and M_{P2} will be thrice as big as M_{N2}. Similarly the size of smaller drivers M_{N1} & M_{P1} should be calculated using reasonable assumption of $V_{DSAT,min}$, $V_{DSAT,max}$ and I_Q keeping the trade-off presented in previous chapter. All the drivers should use minimum length to minimize the area.

Step 3: Now using macro models for EAP and EAN amplifiers and just the smaller driver (we are simulating it in Class-AB mode) find out the GBW requirement on the amplifiers. Also adjust the bias and I_Q if needed.

Step 4: With the knowledge of gate voltages of smaller driver at quiescent and maximum current state, the level shifters can be designed easily such that the bigger driver is OFF in quiescent state and it just turns ON when the smaller driver is sinking maximum current.

Step 5: Now repeat the simulation of step 3 in complete Class-G mode and obtain the requirements on the amplifiers EAP and EAN. The steps 3, 4 & 5 will need a few iterations to reach an optimum design.

Step 6: Design the amplifiers with GBW obtained above. Noise requirements will be obtained from SNR target. The SR of amplifiers should be greater than that calculated in the previous chapter.

4. Results of implementation in ami 0.5um technology

Topology-1 presented in this section has been designed and fabricated in ami 0.5um technology to drive a 32Ω load. The amplifier can drive a maximum load capacitance of 1nF and the typical load capacitance used for all the measurements is 200pF. We have used the following supply levels $V_{DDH} = -V_{SSH} = 1.5$ & $V_{DDL} = -V_{SSL} = 0.6$. Since the application is for portable audio ± 1.5V has been chosen as the larger supply and from our discussion in previous chapter the smaller supply is chosen at 40% of the higher supply. The die micrograph and test setup have been shown in Fig. 39 and Fig. 40 respectively.

Fig. 41 shows the currents delivered to the load from various supplies. It shows how beautifully the supply switching occurs without any output glitches. Table VI summarizes the performance in simulation and the actual tested results. The experi-

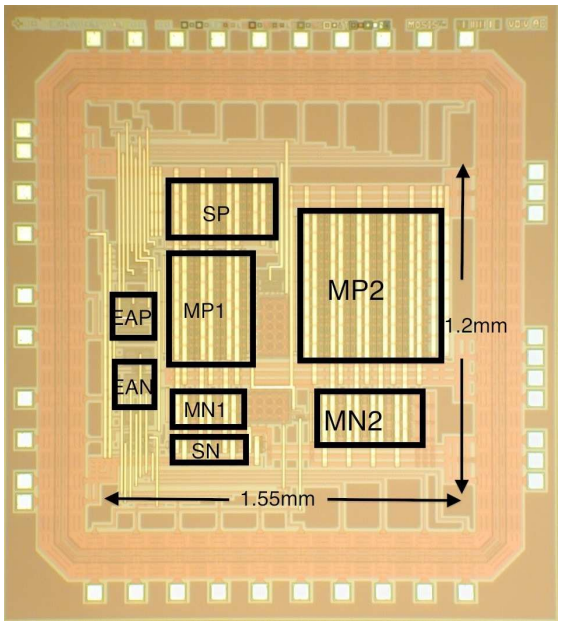

Fig. 39. Die micrograph of topology-1

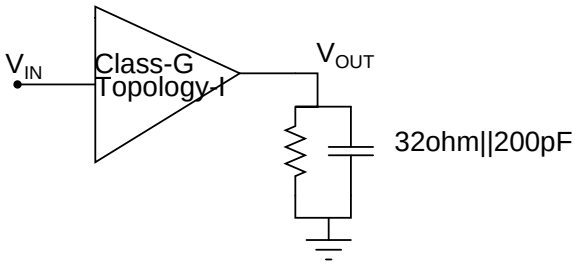

Fig. 40. Test setup for topology-1

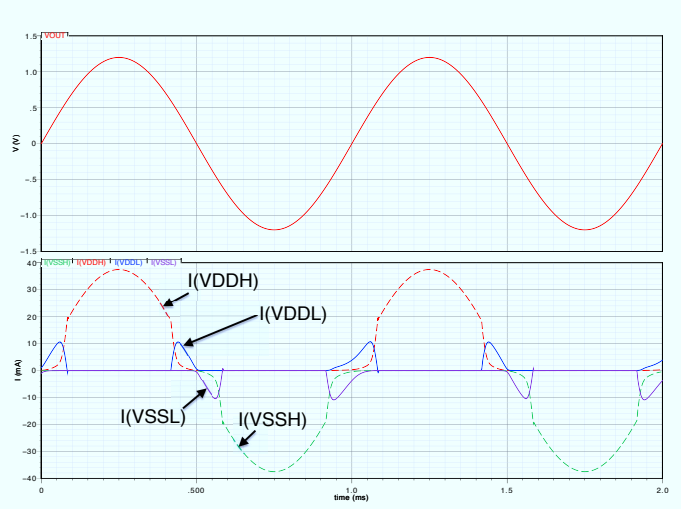

Fig. 41. Load currents from different supplies in topology-1

mental THD+N vs. frequency and amplitude plots are shown in Figs. 42 & 43. The SNR in audio band is measured to be -90dB(Both THD+N and SNR are measured with noise, un-weighted in the 20-22kHz band). The measured FFT of the output is shown in Fig. 44.

As explained this topology is sensitive to the combined offset of the amplifiers. If the offset of the amplifier EAP in Fig. 36 is positive and that of EAN is negative then the quiescent current in the output stage reduces, under this condition the efficiency looks better and the distortion is bad. A couple of mV is enough to degrade the THD by 30-40dB. This is exactly what has happened to test chip we measured and many harmonics can be seen very clearly in the spectrum in Fig. 44 due to transistors operating in sub-threshold for some portion of signal. This is an example of THD+N limited by harmonics at all amplitude levels.

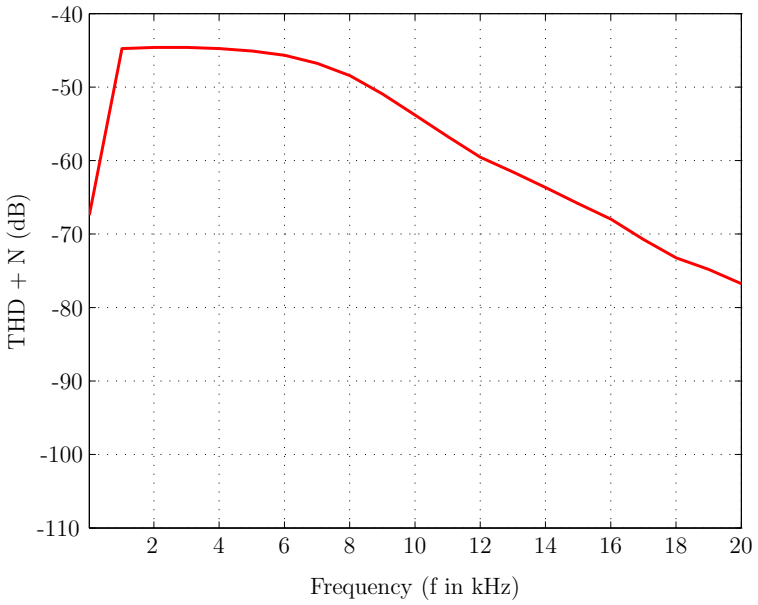

Fig. 42. THD+N vs. frequency of topology-1

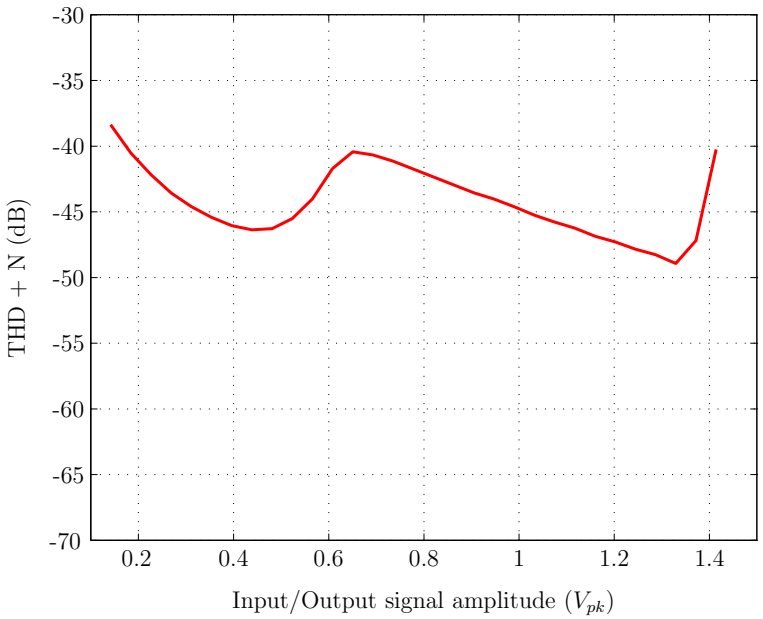

Fig. 43. THD+N vs. amplitude of topology-1

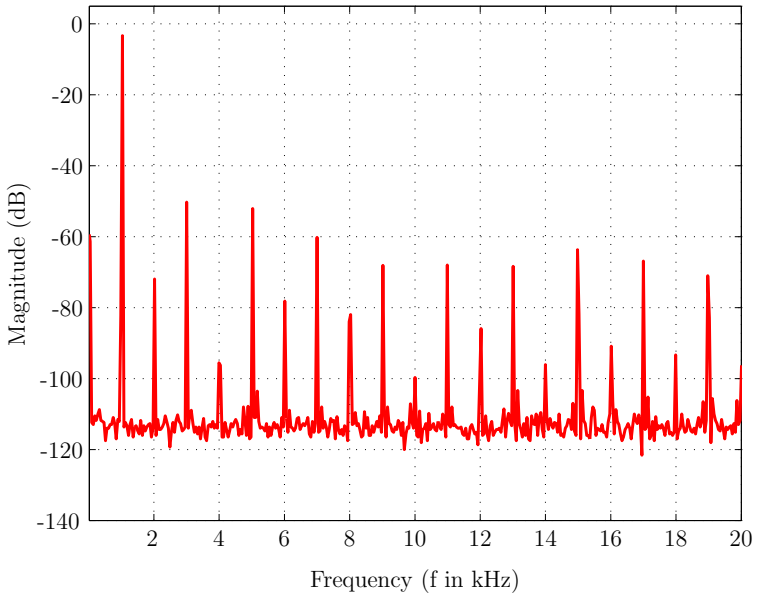

Fig. 44. FFT of topology-1 for $1.3V_{pk}$ input

Table VI. Simulation and experimental results of circuit topology-1

Design	Simulation	Experimental Results
Supply Voltages	± 1.5 & ± 0.6	± 1.5 & ± 0.6
Quiescent Power	1mW(Output Stage) + 2.1mW(Amp)	0mW(Output Stage) + 2.1mW(Amp)
THD+N	-85dB	-44dB
SNR (un-weighted)	-100dB(No flicker noise parameters in technology)	-90dB

B. Circuit topology 2

The circuit topology 1, presented above is kind of proof of the concept to demonstrate the Class-G operation. In real applications we need biasing that is robust, and doesn't degrade the performance due to process variations. For this purpose we have modified the most popular Class-AB biasing scheme proposed by Montecelli [25].

1. Modified Class-AB bias

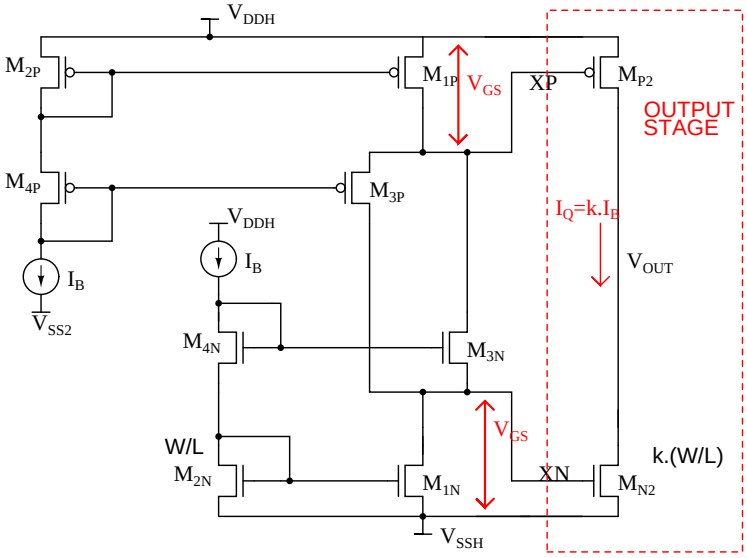

Fig. 45. Class-AB Montecelli bias

Figure 45 shows the popular feed-forward Class-AB biasing circuit proposed by Montecelli [25]. M_{P2} & M_{N2} are the Class-AB driver transistors and rest is the bias circuit. Under proper matched conditions the quiescent current is set by the biasing following the below equation (4.4). Even after considering the channel length modulation, drain induced barrier lowering (DIBL) and other process variations the above equation (4.4) gives us a reasonable estimate of the quiescent current in the

output stage.

$$
\begin{aligned}
V_{GS,M_{N2}} = V_{DS,M_{1N}} = V_{GS,M_{1N}} = V_{GS,M_{2N}} \\
V_{GS,M_{P2}} = V_{DS,M_{1P}} = V_{GS,M_{1P}} = V_{GS,M_{2P}} \\
=> I_Q = \frac{1}{2}\mu_n.C_{ox}\left(\frac{W}{L}\right)_{MN2}.(V_{GS,M_{N2}} - V_T)^2 \\
= k.\frac{1}{2}\mu_n.C_{ox}\left(\frac{W}{L}\right)_{M2N}.(V_{GS,M_{2N}} - V_T)^2 \\
= k.I_B
\end{aligned}
\tag{4.4}
$$

After the modifications shown in the Fig. 46, we should be able to use it for biasing Class-G output stage. The difference between the two circuits is instead of stacking two diode connected transistors for biasing the cascode kind of structure we now have Low voltage cascode kind of biasing. Under matched conditions this now makes the $V_{GS,M_{N2}} \simeq 1 \sim 2.V_{DSAT}$ & $V_{GS,M_{P2}} \simeq 1 \sim 2.V_{DSAT}$. This turns off the bigger driver stage of Class-G and lets its act like a Class-C. Shift-in type level shifters are used to bias the smaller driver stage in Class-AB state. The sizing of the bias transistors and level shifters needs careful attention to make sure we are at the optimum point in the trade-off between cross-over distortion and power consumption.

Another efficient way to implement the level shift is by having a diode connected transistor within the Montecelli bias branch as shown in Fig. 47. This is similar to folded mesh biasing proposed in [26]. The amount of level shift can be adjusted by changing the sizing of the diode connected transistor. The drawback with this is it will limit the amount of signal swing at nodes XP & XN in the bias branch which might be an issue depending on the design.

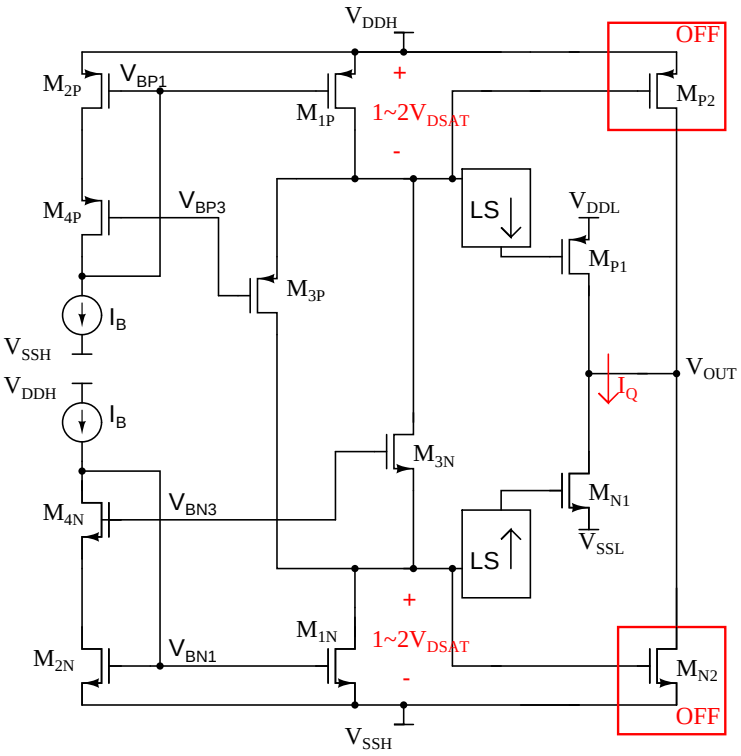

Fig. 46. Modified Class-AB bias 1 for Class-G

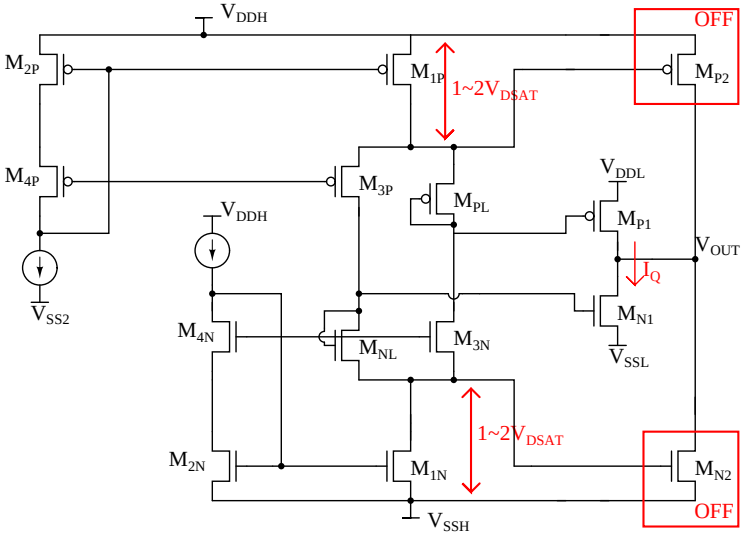

Fig. 47. Modified Class-AB bias 2 for Class-G

2. Design and working

The complete amplifier schematic with the modified Class-AB biasing is shown in the Fig. 48. In which G_{M1} the first stage is a folded cascode with PMOS pair, G_{M2} is the positive g_m second stage and the rest is the Class-G driver (G_{M3}). This three stage amplifier is compensated using nested miller compensation with split capacitor across driver (G_{M3}). Except for the modified biasing and the Class-G output stage, the circuit is very similar in operation to the typical Class-AB amplifiers [27]. The switches here are conveniently placed at the gates of smaller driver transistors killing the level shifter when required. This saves a lot of area as compared to the placement of switches at sources as in topology-1.

Even in this topology, the first stage of the amplifier is folded cascode structure, this means the noise analysis we did for topology applies to this directly. The design procedure is also exactly identical.

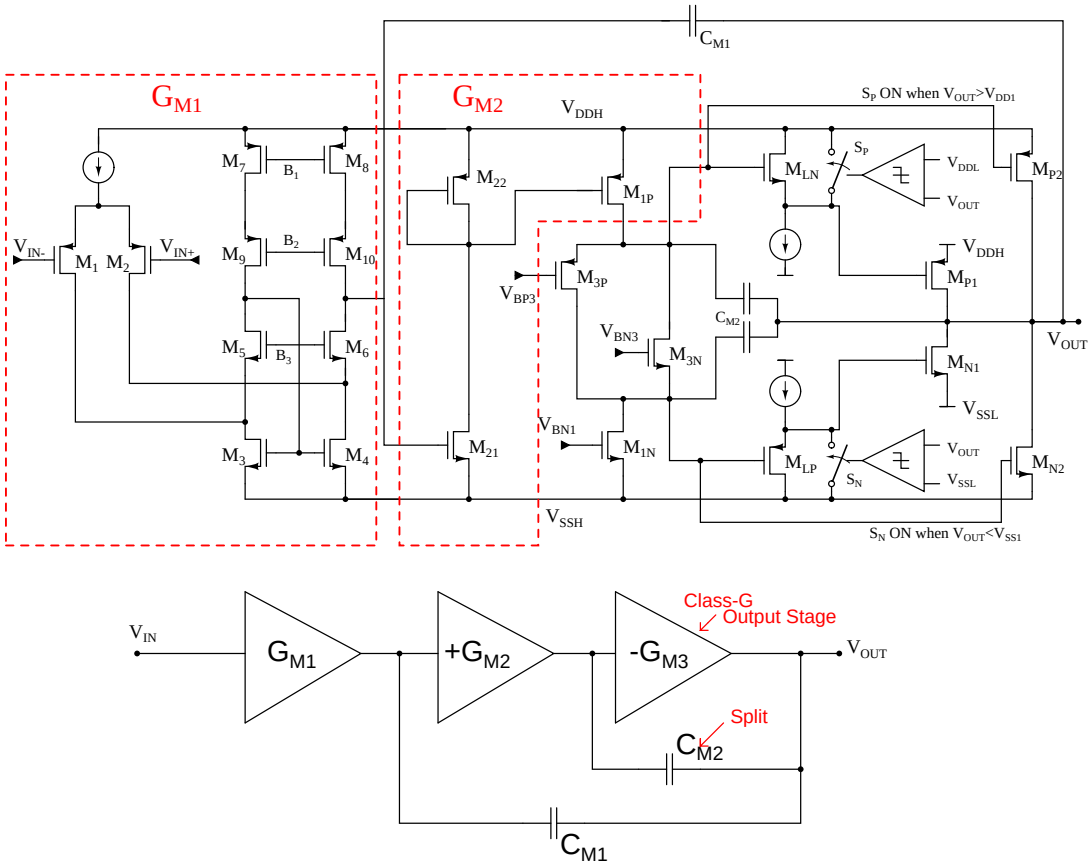

Fig. 48. Class-G circuit topology-2

3. Results of implementation in ami 0.5um technology

Topology-2 presented in this section has been designed and fabricated in ami 0.5um technology to drive a 32Ω load. The amplifier can drive a maximum load capacitance of 1nF and the typical load capacitance used for all the measurements is 200pF. We have used the following supply levels $V_{DDH} = -V_{SSH} = 1.5$ & $V_{DDL} = -V_{SSL} = 0.6$. Since the application is for portable audio ± 1.5V has been chosen as the larger supply and from our discussion in previous chapter the smaller supply is chosen at 40% of the higher supply. The die micrograph and test setup have been shown in Fig. 49 and Fig. 50 respectively.

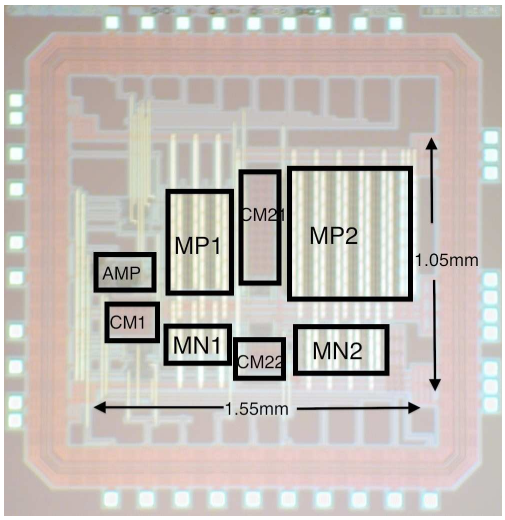

Fig. 49. Die micrograph of topology-2 in ami 0.5um technology

Figure 51 shows the currents delivered to the load from various supplies. It shows how beautifully the supply switching occurs without any output glitches. Table VII

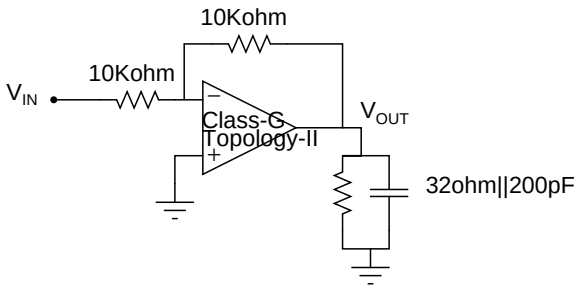

Fig. 50. Test setup for topology-2

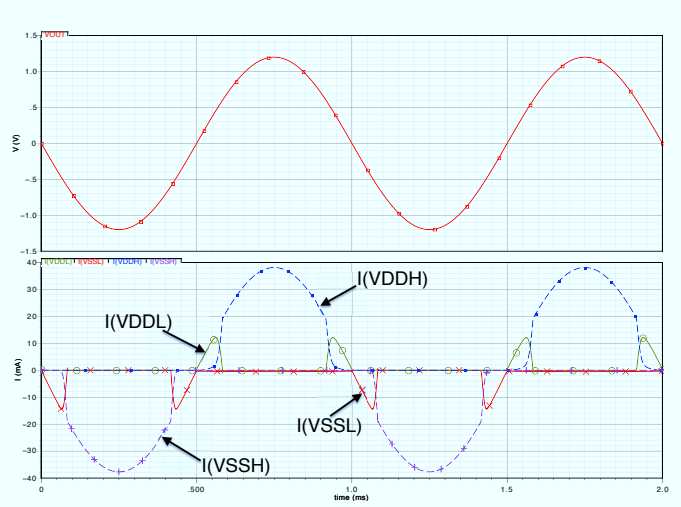

Fig. 51. Load currents from different supplies in topology-2 in ami 0.5um technology

summarizes the experimental test results. The THD+N vs. frequency and amplitude plots are shown in Figs. 52 & 53. The measured SNR in audio band is -90dB (Both THD+N and SNR are measured with noise, un-weighted in the 20-22kHz band). The instantaneous efficiency is shown in Fig. 54 and also the measured FFT of the output is shown in Fig. 55.

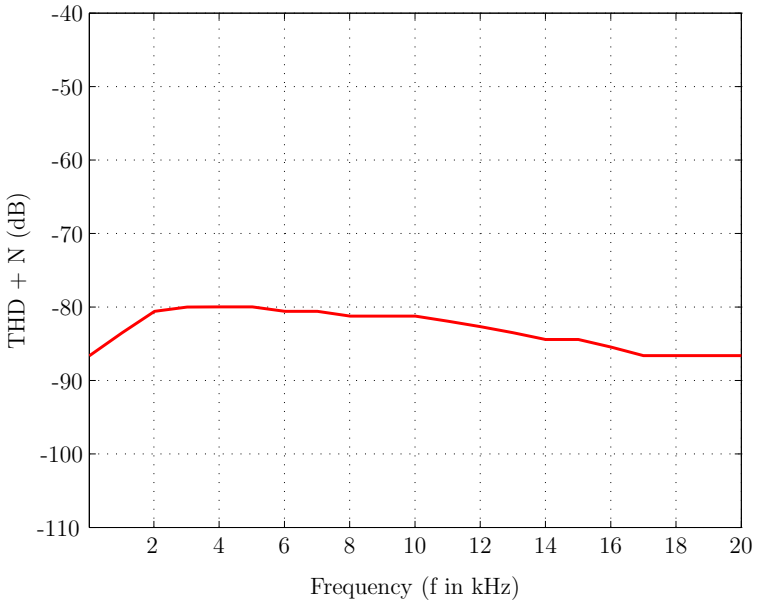

Fig. 52. THD+N vs. frequency of topology-2 in ami 0.5um technology

The Output spectrum for $V_{IN} = V_{OUT} = 1.3VV_p1kHz$ signal, in Fig. 55 shows pretty good linearity with the dominant second harmonic (due to single ended nature of output) at about -89dB and the third at about -100dB. The total THD+N is about -83.5dB. The THD+N increases a little with frequency until 6-7kHz as the open loop gain of the amplifier decreases with increasing frequency but beyond 7kHz the THD+N improves as the third harmonic is out of audio band. The THD+N values are limited by the noise in the low amplitude region. While the peak SNR is -90dB the THD+N value at one tenth the peak signal is about -70dB showing its

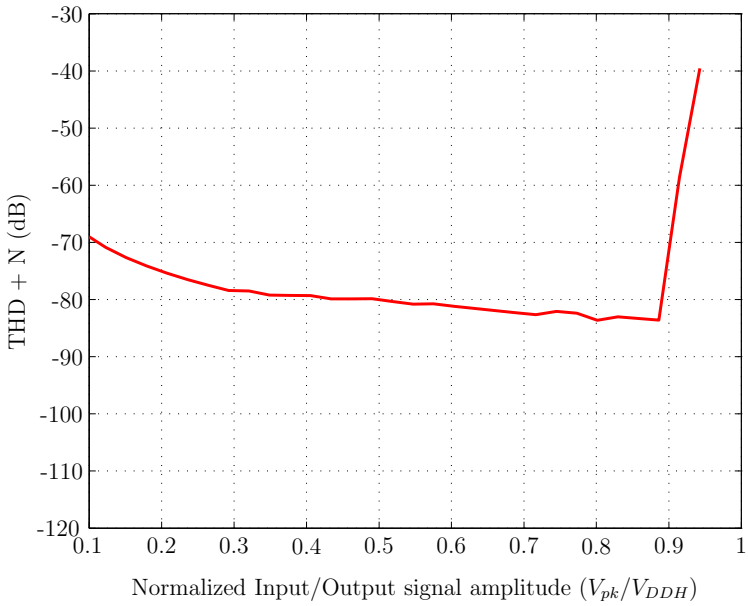

Fig. 53. THD+N vs. amplitude of topology-2 in ami 0.5um technology

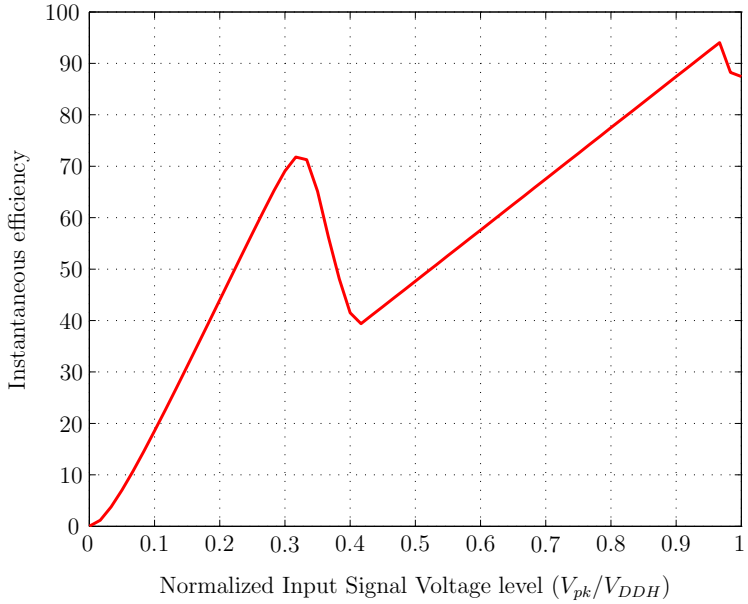

Fig. 54. Instantaneous efficiency of topology-2 in ami 0.5um technology

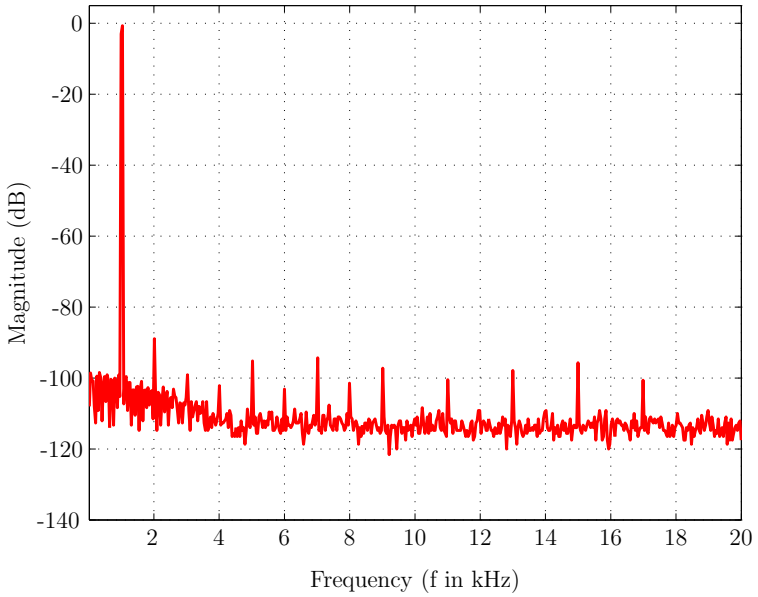

Fig. 55. FFT of topology-2 for $1.3V_{pk}$ input in ami 0.5um technology

limited by noise. The instantaneous efficiency curve is close what we have modeled.

4. Results of implementation in IBM 90nm technology

Topology-2 presented in this section has also been designed and fabricated in IBM 90nm technology. Using a smaller feature size technology helps in reducing the size of the output drivers drastically for a given load this translates to smaller compensation capacitance and as a result less power consumption. As is evident from the results we use 20X less area and 7X less power compared to the 0.5μm implementation. The amplifier implemented can drive a 32Ω resistance and a maximum of 1nF capacitance. The typical load capacitance used for all the measurements is 200pF. We have used the following supply levels $V_{DDH} = -V_{SSH} = 1$ & $V_{DDL} = -V_{SSL} = 0.5$. Since the application is for portable audio $\pm$ 1V has been chosen as the larger supply and from our discussion in previous chapter the smaller supply is chosen at 40-50% of the higher

Table VII. Experimental results of circuit topology-2 in ami 0.5um technology

Design	Experimental Results
Supply Voltages	± 1.5 & ± 0.6
Quiescent Power	600μW(Output Stage) + 1.35mW(Amp)
Peak load power	120mW
THD+N	-83.5dB
SNR(un-weighted)	-90dB

supply. The die micrograph has been shown in Fig. 56 and the test setup is same as the one used for 0.5μm technology.

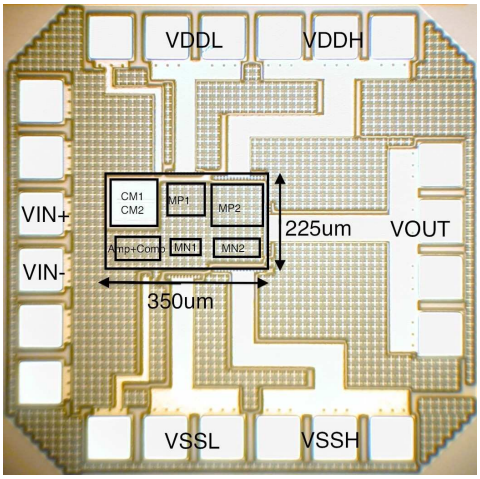

Fig. 56. Die micrograph of topology-2 in IBM 90nm technology

Table VIII summarizes the experimental test results. The THD+N vs. frequency and amplitude plots are shown in Figs. 57 & 58. The measured SNR is -89dB(Both THD+N and SNR are measured with noise, un-weighted in the 20-22kHz band). The

instantaneous efficiency is shown in Fig. 59 and also the measured FFT of the output is shown in Fig. 60.

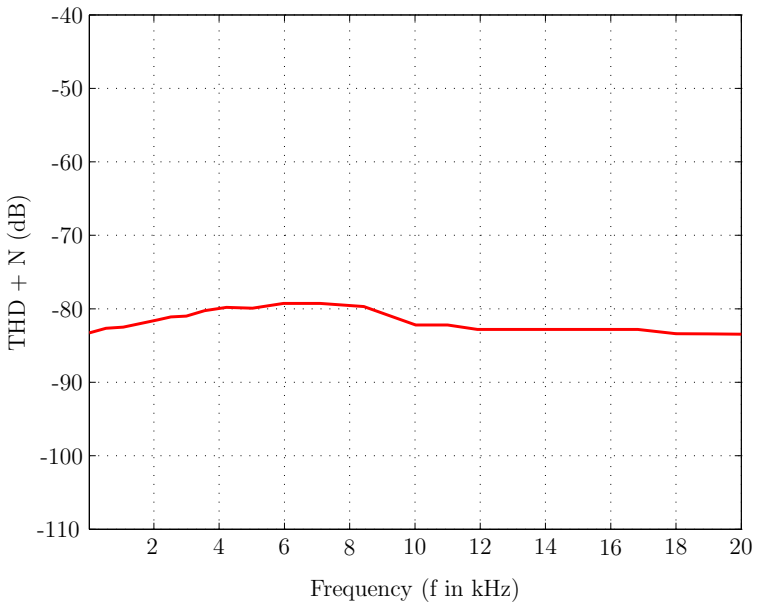

Fig. 57. THD+N vs. frequency of topology-2 in IBM 90nm technology

The SNR of topology-2 in Fig. 48 is limited by the flicker noise contribution of transistors M3 & M4 (95% of total noise contribution) and can be improved by increasing the area (channel length and width propostionally) of these current sources and also by degenerating them (it was limited by design and not by the circuit architecture).

C. Comparison of results with state-of-the-art

Figure 62 presents a comparison of the state-of-the-art headphone amplifiers reported in the literature. The proposed circuit topology achieves -82.5dB THD+N and the best efficiency (achieved by proper choice of VDDL/VSSL) by consuming the least reported quiescent power consumption and area. For true efficiency computation

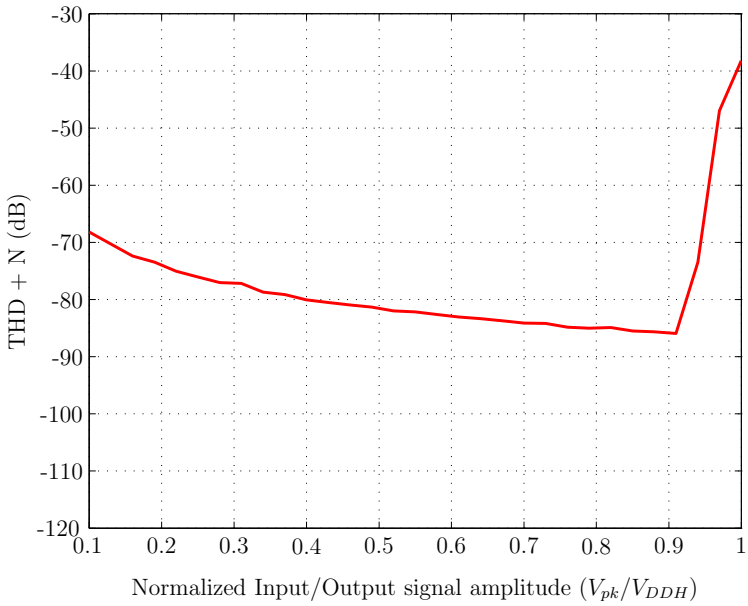

Fig. 58. THD+N vs. amplitude of topology-2 in IBM 90nm technology

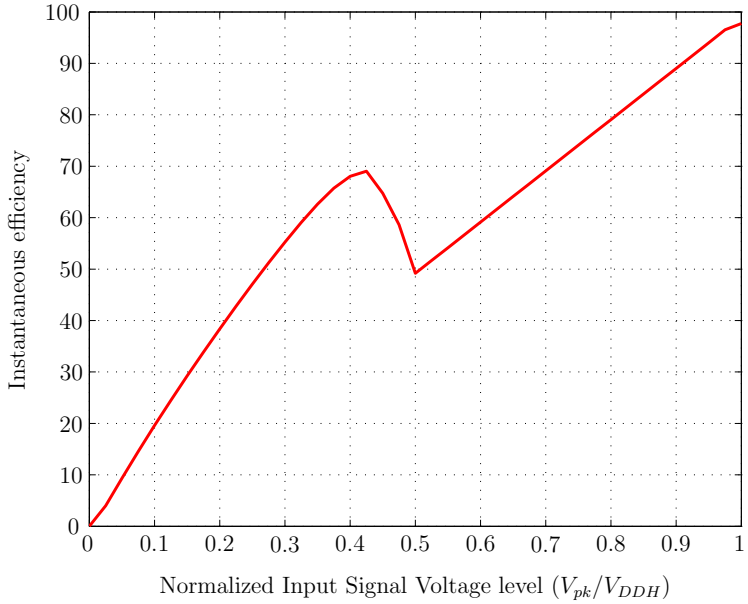

Fig. 59. Instantaneous efficiency of topology-2 in IBM 90nm technology

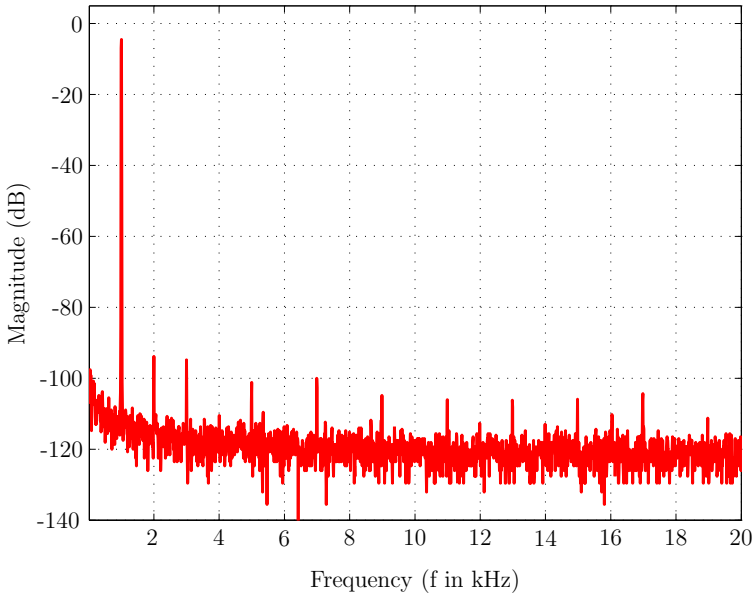

Fig. 60. FFT of topology-2 for $0.85V_{pk}$ input in IBM 90nm technology

Table VIII. Experimental results of circuit topology-2 in IBM 90nm technology

Design	Experimental Results
Supply Voltages	± 1 & ± 0.5
Quiescent Power	200u(Output Stage) + 140u(Amp)
Peak load power	50mW
THD+N	-82.5dB
SNR(un-weighted)	-89dB

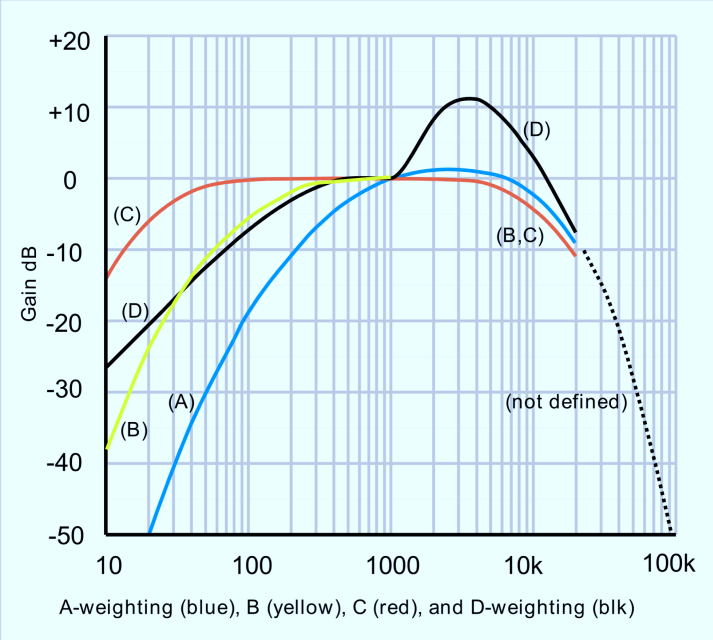

Fig. 61. A-weight filter

typical audio signal-4 has been used. Some of the works in literature report A-weighted SNR. This employs A-filter shown in Fig. 61 to the noise floor to compute the SNR. The logic behind using this filter is, human ear's response is believed to match this closely. Using this filter improves the SNR number by a few dBs.

D. Conclusion

A new realistic efficiency definition for audio amplifiers has been proposed using the amplitude distribution characteristics of the input signal. Also using the amplitude distribution characteristics of audio signals a proper choice of supply voltages is made to maximize the efficiency of Class-G amplifier. Then the concept of Class-G has been developed into a circuit level implementation and has been fabricated in ami 0.5um and IBM 90nm technologies. The prototypes fabricated, have been experimentally

Design	This Work	This Work	ISSCC '10 [19]	JSSC '09 [27]	ESSCIRC '06 [29]
Technology	0.5μm(G)	90nm(G)	65nm(G)	0.13um(AB)	65nm(AB)
Supply Voltages	$\mathbf{\pm 1.5V/\pm 0.6V}$	$\mathbf{\pm 1V/\pm 0.5V}$	$\pm 1.4V/\pm 0.35V$	$\pm 1V/\pm 0.6V$	2.5V
Quiescent Power	2mW	**0.35mW**	0.41mW	1.2mW	12.5mW
Peak Load Power*	110mW	50mW	90mW	40mW	53.5mW
($R_L = 16\Omega$)					
THD+N	-83.5dB	-82.5dB	-80dB	-84dB	-68dB@27mW
@PRMS(32Ω)	@54mW	@12.5mW	@16mW	@10mW	(16Ω)
SNR	89dB	89dB	100dB	92dB	-
	(un-weighted)	(un-weighted)	(A-weighted)	(un-weighted)	
Area	$1.65mm^2$	$\mathbf{0.08mm^2}$	$0.14mm^2$	$0.10mm^2$	-
True η^{**} @Volume	**48%/**	**50.8%/**	39.8%/	29%/	29%
(100%/75%/50%)	**45%/42%**	**48%/43.16%**	37%/35.3%	25%/22%	25%/22%

Fig. 62. Comparison of results with state-of-the-art headphone drivers

tested and the performance has been verified.

E. Future work

One of the most important un answered questions is how do we generate the supplies efficiently? Efficiently in terms of power, area and external components. An innovative switching mode circuit that generates multiple supplies efficiently using minimal external components will be the ideal next step. This directly counts into the usefulness of Class-G. Another interesting feature is to implement the dynamic supply scaling based on Volume setting. We have seen the *adf* of audio signals expand/shrink with audio volume. Doing the supply scaling based on volume setting not only helps Class-G but it is also useful to all Classes of audio amplifiers.

REFERENCES

[1] B. Duncan, *High Perfomance Audio Power Amplifiers for Music Performance and Reproduction*. Oxford, U.K.: Butterworth-Heinemann, 1996.

[2] E. Barbour, "The cool sound of tubes [vacuum tube musical applications]," *IEEE Spectrum*, vol. 35, no. 8, pp. 24–35, 1998.

[3] R. Hamm, "Tubes versus transistors: Is there an audible difference?" *Journal of the Audio Engineering Society*, vol. 21, no. 4, pp. 267–273, 1973.

[4] D. Self, *Audio Power Amplifier Design Handbook*. Oxford, U.K.: Focal Pr, 2009.

[5] B. Putzeys, "Digital audio's final frontier," *IEEE Spectrum*, vol. 40, no. 3, pp. 34 – 41, Mar. 2003.

[6] M. Rojas-Gonzalez and E. Sanchez-Sinencio, "Design of a class d audio amplifier ic using sliding mode control and negative feedback," *IEEE Transactions on Consumer Electronics*, vol. 53, no. 2, pp. 609 –617, May. 2007.

[7] ——, "Low-power high-efficiency class d audio power amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3272 –3284, Dec. 2009.

[8] J. Silva, "Pwm audio power amplifiers: sigma delta versus sliding mode control," in *Proc. IEEE International Conf. on Electronics, Circuits and Systems*, vol. 1, 1998, pp. 359 –362.

[9] J. Hung, W. Gao, and J. Hung, "Variable structure control: A survey," *IEEE Transactions on Industrial Electronics*, vol. 40, no. 1, pp. 2 –22, Feb. 1993.

[10] T. Sampei, S. Ohashi, Y. Ohta, and S. Inoue, "Highest efficiency and super quality audio amplifier using mos power fets in class g operation," *IEEE Transactions on Consumer Electronics*, vol. CE-24, no. 3, pp. 300 –307, Aug. 1978.

[11] F. Raab, "Average efficiency of class-g power amplifiers," *IEEE Transactions on Consumer Electronics*, vol. CE-32, no. 2, pp. 145 –150, May 1986.

[12] A. Downey and G. Wierzba, "A class-G/FB audio amplifier," *IEEE Transactions on Consumer Electronics*, vol. 53, no. 4, pp. 1537–1545, 2007.

[13] J. Pierdomenico, S. Wurcer, and B. Day, "A 684-mW adaptive supply full-rate ADSL CO driver," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 12, p. 1831, 2002.

[14] J. Quarfoot, M. Corsi, R. Hester, and K. Maclean, "Zero-overhead class G amplifier with threshold detection," Oct. 31 2001, uS Patent App. 10/001,330.

[15] T. Somerville and K. Wortel, "Efficient class-G amplifier with wide output voltage swing," Jul. 17 2003, uS Patent App. 10/622,051.

[16] J. Shorb, D. Allstot, and R. Roze, "Class ab-d-g line driver for central office asymmetric digital subscriber line systems," in *Proc. IEEE International Symposium on Circuits and Systems*, vol. 5, 2002, pp. V–405 – V–408.

[17] A. Bicakci, C.-S. Kim, S.-S. Lee, and C. Conroy, "A 700 mw cmos line driver for adsl central office applications," in *Proc. IEEE International Solid-State Circuits Conf., Digest of Technical Papers*, vol. 1, 2003, pp. 414 – 503.

[18] A. Bicakci, C.-S. Kim, and S.-S. Lee, "A cmos line driver for adsl central office applications," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 12, pp. 2201 – 2208, Dec. 2003.

[19] A. Lollio, G. Bollati, and R. Castello, "Class-g headphone driver in 65nm cmos technology," in *Proc. IEEE International Solid-State Circuits Conf., Digest of Technical Papers*, 2010, pp. 84 –85.

[20] Class-g directpath stereo headphone amplifier with i^2c volume control. Texas Intruments Inc., Dallas, TX., Mar. 2009, Accessed on Aug. 06, 2010. [Online]. Available: http://focus.ti.com.cn/cn/lit/ds/symlink/tpa6140a2.pdf

[21] Class g headphone amplifier with i^2c volume control. National Semiconductors Inc., Santa Clara, CA., Aug. 2009, Accessed on Aug. 06, 2010. [Online]. Available: http://www.national.com/ds/LM/LM48824.pdf

[22] 2.4w, single-supply class g power amplifier. Maxim Semiconductors Inc., Dallas, TX., Rev. 5, Mar. 2010, Accessed on Aug. 06, 2010. [Online]. Available: http://datasheets.maxim-ic.com/en/ds/MAX9730.pdf

[23] P. Gray, P. Hurst, R. Meyer, and S. Lewis, *Analysis and Design of Analog Integrated Circuits*. New Delhi, India: Wiley, 2008.

[24] B. Sekerkiran, "A compact rail-to-rail output stage for CMOS operational amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 1, pp. 107–110, 1999.

[25] D. Monticelli, "A quad cmos single-supply opamp with rail-to rail output swing," in *Proc. IEEE International Solid-State Circuits Conf., Digest of Technical Papers*, 1986, pp. 18 – 19.

[26] K. De Langen and J. Huijsing, "Compact low-voltage power-efficient operational amplifier cells for VLSI," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 10, pp. 1482–1496, 1998.

[27] V. Dhanasekaran, J. Silva-Martinez, and E. Sanchez-Sinencio, "Design of three-stage class-ab 16 headphone driver capable of handling wide range of load capacitance," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 6, pp. 1734 –1744, Jun. 2009.

[28] R. Becker and W. Groeneweg, "An audio amplifier providing up to 1 watt in standard digital 90-nm cmos," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 7, pp. 1648 –1653, Jul. 2006.

[29] P. Bogner, H. Habibovic, and T. Hartig, "A high signal swing class ab earpiece amplifier in 65nm cmos technology," in *Proc. European Solid-State Circuits Conf.*, 2006, pp. 372 –375.

[30] P. Boonyaporn and V. Kasemsuwan, "A high performance class ab cmos rail to rail voltage follower," in *Proc. IEEE Asia-Pacific Conf. on ASIC*, 2002, pp. 161 – 163.

VITA

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