MILLIMETER-WAVE CONCURRENT DUAL-BAND BICMOS RFICS FOR RADAR AND COMMUNICATION RF FRONT-END

A Dissertation

by

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ABSTRACT

The recent advancement in silicon-based technologies has offered the opportunity for the development of highly-integrated circuits and systems in the millimeter-wave frequency regime. In particular, the demand for high performance multi-band multi-mode radar and communication systems built on silicon-based technologies has been increased dramatically for both military and commercial applications.

This dissertation presents the design and implementation of advanced millimeter-wave front-end circuits in SiGe BiCMOS process including a transmit/receive switch module with integrated calibration function, low noise amplifier, and power amplifier for millimeter-wave concurrent dual-band dual-polarization radars and communication systems. The proposed circuits designed for the concurrent dual-band dual-polarization radars and communication systems were fabricated using 0.18-μm BiCMOS process resulting in novel circuit architectures for concurrent multi-band operation.

The developed concurrent dual-band circuits fabricated on 0.18-μm BiCMOS process include the T/R/Calibration switch module for digital beam forming array system at 24.5/35 GHz, concurrent dual-band low noise amplifiers at 44/60 GHz, and concurrent dual-band power amplifier at 44/60 GHz. With having all the design frequencies closely spaced to each other showing the frequency ratio below 1.43, the designed circuits provided the integrated dual-band filtering function with Q-enhanced frequency responses. Inspired by the composite right/left- handed metamaterial

transmission line approaches, the integrated Q-enhanced filtering sub-circuits provided unprecedented dual-band filtering capability.

The new concurrent dual-band dual-mode circuits and system architecture can provide enhanced radar and communication system performance with extended coverage, better image synthesis and target locating by the enhanced diversity. The circuit level hardware research conducted in this dissertation is expected to contribute to enhance the performance of multi-band multi-mode imaging, sensing, and communication array systems.

DEDICATION

To my family for all their endless love and support

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This dissertation would not have been possible without the help of many people. I would like to express my gratitude to all my committee members, Prof. Cam Nguyen, Prof. Chin B. Su, Prof. Gregory Huff, and Prof. Reza Langari for their valuable input and support throughout the course of this research. Thanks also go to my friends and colleagues who were willing to provide help and support during my time at Texas A&M University. Their encouragement and support have also become great motivation for me to accomplish this degree.

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NOMENCLATURE

BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BJT	Bipolar Junction Transistor
CMOS	Complementary Metal Oxide Semiconductor
CRLH	Composite Right/Left- Handed
GaAs	Gallium Arsenide
HBT	Heterojunction Bipolar Technology
LNA	Low Noise Amplifier
MAG	Maximum Available Gain
MTM	Metamaterial
NF	NF
PA	Power Amplifier
PDK	Process Design Kit
RF	Radio Frequency
SiGe	Silicon Germanium
SPST	Single-Pole Single-Throw

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CHAPTER I

INTRODUCTION

1.1 Technical Background of the Proposed Dual-band Circuits and Modules

There has been increasing demand in multi-band multi-mode radar and communication systems in millimeter-wave frequency bands between 30 and 300 GHz. The millimeter-wave spectrum has been mostly used for military radar application using expensive compound semiconductor process such as Gallium Arsenide (GaAs), Indium Phosphide (InP) and so on. However, cost effective silicon based technologies such as CMOS and BiCMOS enable cost-effective integrated circuits and systems with comparable performance to expensive compound processes such as GaAs and InP. Also, the demand in high-data rate wireless communication exploiting millimeter-wave spectrum led the research and development of highly-integrated multi-functional millimeter-wave circuits and systems.

In this research, the RF front-end circuits including transmit/receive switch module, low noise amplifiers, and power amplifier development was conducted for novel, compact, multi-band, and multi-polarization millimeter-wave system, which are proposed for an innovative and intelligent dual-band and dual-polarization radar and wireless communication systems. The main focus of this research is to develop some multi-band and multi-mode components in *K*/*Ka* (24.5/35 GHz) - and *Q*/*V* (44/60 GHz) - band frequency spectrum. The developed front-end circuits includes concurrent dual

K/*Ka*- band T/R/Calibration switch module to support dual-polarization operation, concurrent dual *Q*/*V*- band low noise amplifiers, and a concurrent dual *Q*/*V*- band power amplifier. All the proposed circuits and modules aims to achieve electrical integration of two modalities in *K*/*Ka*- and *Q*/*V*- band. The concurrent operation, which enables the circuits function together over multi-bands radically reduces the circuit size making a large concurrent dual-band millimeter-wave antenna array system feasible. This is not only cost effective but also innovative in that design complexity in realizing multi-band system is greatly reduced.

1.1.1 Objectives and Motivation of the Research

The objective of this research is to propose and develop integrated circuits, modules, and systems, which electrically combine multi modalities in *K*/*Ka*- and *Q*/*V*- bands. Rather than combining circuits optimized at single frequency in parallel, designing a single unit circuit operating over multi-band simultaneously can improve system performance while reducing the cost and complexity in realizing multi-band systems. Such multi-band components employed in multi-band radar and wireless communication systems can provide advantages over single-band components for better detection, identification, target tracking, locating, and high-data rate wireless communication by the frequency and polarization diversity. This enhanced detection coverage, precise target location, increased resolution, improved reliability, and high-data rate for both radar and wireless communication systems can be attractive in that all

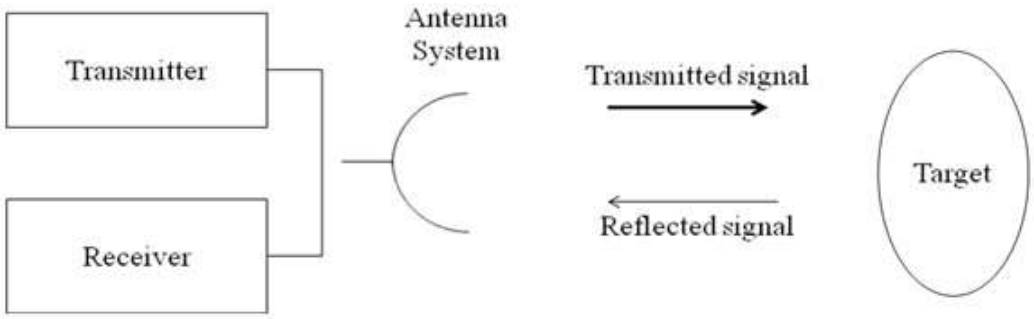


Fig. 1.1. Illustration of basic radar systems

the aforementioned improvement can be realized within a single circuit designed based on concurrent multi-band principle. The following sections will introduce some radar and commercial wireless communication applications which would benefit from the multi-band multi-modal circuits and modules proposed in this research by extended frequency and polarization diversity.

1.1.2 Radar System Overview

Radar system refers to hardware and software combined system which utilizes radio frequency for detecting and ranging targets [1]. Radar systems illuminate a target with a certain frequency signal to process the backscattered signals for, to mention a few, precise distance measurement, velocity measurement, surveillance, scatterometry, cloud radar monitoring for weather forecast, subsurface sensing, industrial applications such as

presence sensing of objects and distance control, automotive applications including safety distance measurement, blind spot detection and traffic monitoring. Other applications of radar systems include utilizing a scanning beam of a transmitter of radar for generating image of certain targets or areas.

Figure. 1.1 presents the basic principle of radar systems. The transmitter in the radar system sends out a electromagnetic signal at a certain spectrum of frequency in the form of a pulse or continuous wave to an intended target through an antenna system. Once the target is illuminated by the transmit signal, a certain amount of signal is reflected back to the radar system so the receiver can capture the backscattered signal from the target. In conjunction with the signal processing unit, the backscattered signal is processed to detect the target presence, location, image, or velocity. The target distance can be calculated by measuring the round-trip time of the radar signal from the target.

The calculation of target's location can be performed using narrow electromagnetic beam transmitted from the radar system. The precise location can be calculated by measuring the maximum received power from the echo signal. Also, if the target is a moving platform, the reflected signal will undergo the Doppler shift effect. The measured frequency shift is proportional to the velocity of the moving platform, which provides the information regarding the relative velocity to the radar system.

1.1.3 Radar System Equations

It is important to go over a number of radar system equations because they not only provide the relationship between the transmitter and receiver of a radar system but also characterize the relationship between the radar system and potential targets. The measures would also serve as a fundamental tool to radar systems since the radar system equation represents the physical relationship of the transmit power to the receiving of the reflected signals, or echo signals, from a target. With a certain sensitivity of the radar receiver, the radar equation helps to determine a maximum range for detection [2]. Supposing the radar system employs isotropic antenna to transmit radar signal, the power density at the distance R from the radar system can be expressed as

$$P_d = \frac{P_t}{4\pi R^2} \tag{1.1}$$

where P_d and P_t are the power density and the transmitted power from a radar system, respectively. The measure of power density is based on the watts per square meter. However, in many cases, radar systems employ directional antenna system to increase the gain of the radiated power. The gain of antenna is proportional to the directivity which means how much radiated energy is concentrated into a certain direction. With the antenna gain designated as G, the power density expression in (1.1) can be rewritten as

$$P_d = \frac{P_t G}{4\pi R^2} \tag{1.2}$$

where P_d and G are the power density and the antenna gain of directional antenna system, respectively. The power of the received signal from a target requires more terms to reflect the radar cross section and the effective area of the antenna system. The received power of the backscattered signal is expressed as

$$P_r = \frac{P_t G}{4\pi R^2} \times A_e \times \frac{\sigma}{4\pi R^2} \tag{1.3}$$

where *Ae* is the effective area of the antenna system and σ is the radar cross section of a target respectively.

The maximum detectable range of a radar system can be derived based on (1.3). Designating the lowest detectable signal power from a target as P_{rmin} and substituting it with the received power term in (1.3), the maximum range of a radar system can be expressed as

$$R_{\max} = \left[\frac{P_t G A_e \sigma}{(4\pi)^2 P_{r\min}} \right]^{1/4} \tag{1.4}$$

Any target beyond this maximum range shown in (1.4) cannot be detected.

1.1.4 Millimeter-wave Radar and Communication System Applications

There has been a great demand in utilizing higher frequency spectrum above 30 GHz since the microwave frequency spectrum was fully occupied with numerous commercial and military applications [3-10]. The possible benefit in utilizing the millimeter-wave spectrum is high data rate on a wide frequency spectrum. Also, a relatively shorter wavelength in millimeter-wave spectrum enables smaller circuit sizes resulting in compact electronic systems. A number of millimeter-wave radar and wireless communication applications which benefit from the characteristic of millimeter-wave spectrum are overviewed.

The millimeter-wave spectrum can be utilized for both long- and short- range radar and wireless communication systems. For long range application, the millimeter-wave frequency band such as *Ka* (26.5 to 40 GHz) - and *Q* (33 to 50 GHz) - band are utilized for satellite communications, terrestrial fixed point-to-point data link, radio astronomy radar application and high resolution radar systems [11]. The aforementioned *Ka*/*Q*- band frequency spectrum suffers relatively less atmospheric attenuation compared to other bands up to 300 GHz and hence can be utilized for long range radar and communication application.

The frequency spectrum such as *V*-band (57-64 GHz) and *E*-band (71-86 GHz) are used for high-data rate wireless communication systems, however, the applications are mostly confined to relatively shorter distance in the range of several kilometers, typically 2 or 3 kilometers or less due to atmospheric attenuation [12-14]. For the 60

GHz band, it is recently exploited for short-range wireless communication below 100 meters for applications such as 802.11ad and 802.11ac [15-16]. The increased demand in high-date rate and high-definition multimedia mobile devices are driving the need of 60 GHz wireless connectivity application. While the application is mostly confined for close proximity wireless communication for line-of-sight data transfer due to the atmospheric attenuation, this line-of-sight link enables high data-rate communication between multiple devices which present within close proximity without interference. While it has become possible to use cost effective CMOS process for millimeter-wave system design recently, the standard established for the 60 GHz ISM band for PAN and LAN is predicted to gain strong momentum later on [17].

Other noticeable application includes the active radar sensor system for car collision avoidance. The original plan to use both 24 and 77 GHz spectrum is nullified due to possible interference in 24 GHz ISM band and therefore only 77 GHz is used for the automotive radar system [18-20]. The automotive radar application will leverage the safety of drivers by the collision avoidance, enhanced automatic cruise control, and blind spot monitoring. This application is also expected to grow exponentially once the regulation for the car safety is established.

The millimeter-wave systems operating in *W* (75 - 110 GHz) -band has been also used for passive imaging radar and wireless system for remote sensing. Compared to the active radar systems, passive radar sensors are only composed of receivers which measure the weak black-body radiation, or thermal radiation, emitted from an intended

target. The actual power received by the receiver from the an intended target can be represented as follows.

$$P = k\Delta fT \tag{1.5}$$

where k and T are the Boltzmann's constant and surface temperature of the intended target, respectively. And Δf specifies the receiver bandwidth over which the black-body is integrated [21]. The received power level is used to construct the image of an intended target. Since those systems process very weak black-body radiation, it is required for the receiver in passive radar systems to have excellent sensitivity. Passive millimeter-wave imaging systems are mostly utilized for assistant landing system for aerial vehicles, concealed weapon and explosive detection, car crash avoidance in harsh weather, and etc. The application field is expanding to medical and biomedical imaging systems for breast cancer and other cancer detections. The following table summarizes the advantages and disadvantages of radar sensors in various frequency spectrums.

It can be seen from Table 1.1, the millimeter-wave radar systems offer many advantages over the infrared imager radar sensor [22]. They provide signal penetration for concealed target recognition, high spatial and frequency resolution for image generation and velocity measurement. Including other applications aforementioned, there is growing demand in the areas such as medical and biomedical imaging and detection, cosmic ray observation, next generation wireless communication systems referred to 5G.

Table 1.1

Radar sensor architectures: benefits and disadvantages

Radar Sensor	**Advantages**	**Disadvantages**
RF/millimeter-wave radar (Active)	1. Distance and image acquisitions 2. Wide scanning range 3. Independent from weather condition 4. Velocity measurement	1. Low resolution 2. Weak to interference
RF/millimeter-wave radiometer (Passive)	1. Concealed operation 2. Wide scanning range 3. Independent from weather condition 4. Velocity measurement	1. Low radiated power 2. Low resolution
Infrared imager	1. Spatial and frequency resolution 2. Concealed operation	1. Weather condition 2. No distance measure

And therefore the millimeter-wave circuits and systems are expected to contribute for both radars and wireless communication systems later on with a strong momentum boosted by commercial wireless applications [23-25]. Along with the

technical maturity in developing cost effective process and foundry for millimeter-wave application, emerging demand in new millimeter-wave radar sensors and wireless communication systems are expected to be fulfilled with highly integrated and multifunctional circuits and systems.

1.1.5 Dissertation Organization

In this dissertation, various novel multi-band circuits and circuit architectures for the use of millimeter-wave radar and wireless communication systems are proposed. The dual-band circuits presented in this thesis are fabricated on Jazz 0.18-μm BiCMOS process working at *K*/*Ka*/*Q*/*V* (24.5/35/44/60 GHz) -band frequency spectrum.

Chapter II starts with a concurrent dual-band T/R switch module with integrated filtering and calibration function (hereafter, T/R/Calibration switch module) for dual-polarization digital beam forming array architecture. In the newly proposed concurrent dual-band dual-polarization digital beam former architecture, the T/R/Calibration switch module provided dual-bandpass filtering function to avoid any blocker signals to saturate the receiver. Also the integrated calibration function enabled self-calibration both the transmit reference and receive calibration therefore enhancing accurate image synthesis of the full polarimetric digital beam former array system. Chapter III introduces novel concurrent dual-band low noise amplifiers with integrated dual-bandpass filtering function. The Q-enhanced dual-band quarter-wavelength network inspired by the composite right/left- handed metamaterial transmission line and its electrical dual

structure were utilized in realizing the dual-bandpass frequency response. The possible stability issue arose from the critical poles reside in the proposed Q-enhanced dual-band networks are resolved by employing an additional inter-stage matching network which provides pole/zero cancellation. The additional transmission zero added by the inter-stage matching network effectively suppressed the critical poles from over-compensation by the added negative resistance ensuring stable operation of the amplifiers with concurrent dual bandpass frequency response. Chapter IV proposes a new concurrent dual-band power amplifier design with dual-band impedance matching networks and harmonic termination provided by the metamaterial inspired networks. The techniques employed in this design provided filtering function to effectively suppress the inter-modulation and harmonic frequency terms. Chapter V summarizes the contribution of the proposed development.

CHAPTER II

CONCURRENT DUAL-BAND T/R/CALIBRATION SWITCH

2.1 RF CMOS Switch Architecture and Consideration

RF switches have played an important role in radar and communication systems. In the past, compound semiconductors such as GaAs were widely used for performance switching function in RF/millimeter-wave radar and communication systems. However, emerging demand for cost effective solutions in realizing RF/millimeter-wave systems lead the technical maturity of CMOS process, which has become a favorable solution even for millimeter-wave IC design. However, it is still challenging to design high-performance RF/millimeter-wave switches due to the inherent low resistivity substrate, low mobility, and various parasitic parameters of CMOS process. Hence, the fundamental T/R switch performance metrics and previous T/R switch works are overviewed.

2.1.1 T/R Switch Performance Metrics

A number of T/R switch performance metrics are introduced in this section. The basic performance parameters of the T/R switch design are: Insertion loss, Isolation, Linearity, and Impedance matching.

The insertion loss (IL) refers the power loss due to the switch which is characterized by the difference in output power and input power of the switch. Since the T/R switch is usually located at the front-end before antenna or array antenna systems, the insertion loss directly affects the noise figure (NF) of the system. Therefore, it is critical to keep the insertion loss as low as possible for any RF/millimeter-wave radar and communication systems.

The isolation (ISO) characterizes how much power is attenuated at the output compared to the input of the switch. For example, if the reception path in a Single-Pole Double-Throw (SPDT) T/R switch, the isolation is characterized over the transmission path. The difference in the input and output power level in the transmission path is designated is the isolation performance. The isolation of more than 30 dB is usually considered to be the minimum requirement.

The impedance matching condition is also an important measure of T/R switches. It is a measure of return loss at the input and the output ports of the turned-on path. The minimum return loss more than 10 dB is considered as reasonable.

The linearity performance indicates how much power the switch can handle without distortion or saturation. The 1-dB compression point (P1dB) and third-order intercept point (IP3) are the measure of linearity performances. The required P1dB and IP3 performance are in accordance with desired system performance.

Other consideration for switch design is switching speed, which is expected to be in the sub-nano second range in many millimeter-wave radar or communication system,

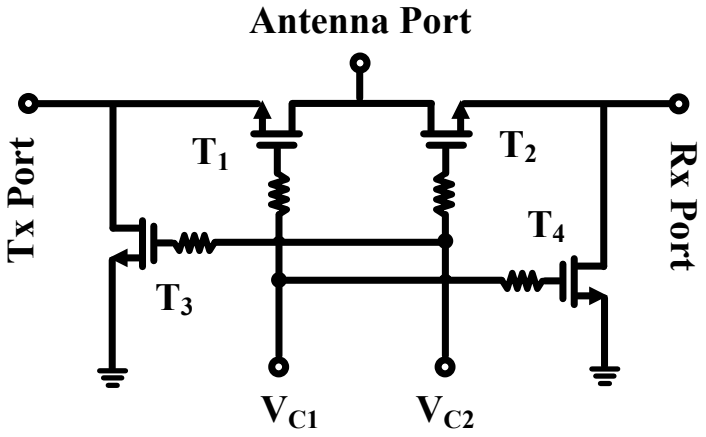


Figure 2.1. Conventional series-shunt switch architecture

low power consumption if it employs power consuming active devices, and easy integration with other circuits.

2.1.2 Conventional T/R Switch

A conventional T/R switch architecture is shown in Fig. 2.1. In the turned-on path, the series and shunt nMOS devices are turned on and off, respectively, and in the turned-off path, the series and shunt nMOS devices are turned off and on, respectively. With higher operating frequency, performance degradation in terms of insertion loss and isolation is easily observed due to parasitic capacitance between source and drain, low-resistivity bulk substrates [26-28]. As mentioned briefly, other compound semiconductors such as GaAs or GaN provides higher substrate resistance, which

minimizes leakage loss to the substrate [29-30]. There have been attempts to reduce the high-frequency leakage to the bulk substrate which resulted in bulk-floating switch architecture [31-32]. In this switch device, additional n-well layer isolates p-well of the nMOS switch device from the bulk substrate. Also, a biasing technique to keep the junction created by the n-p-n layer reverse biased to minimize the leakage is proposed as well. Other switch architecture which is commonly used for broadband operation is also proposed based on the synthetic transmission line formation and the architecture utilizes the off-state capacitance of shunt transistors to mimic that of a transmission line structure [33-34].

2.2 Concurrent Dual-band T/R/Calibration Switch Module

The proposed T/R/Calibration switch is presented in this section. The motivation of the multi-path T/R/Calibration switch work is introduced and then the new approach in realizing the concurrent dual bandpass filtering response and switch architecture will be presented. Finally, the complete four-port circuit design and the discussion on the measured performance will follow.

2.2.1 Introduction and Motivation

Multi-band systems offer a great deal of benefit in modern communication and radar systems. In particular, multi-band antenna-array radar systems with their extended

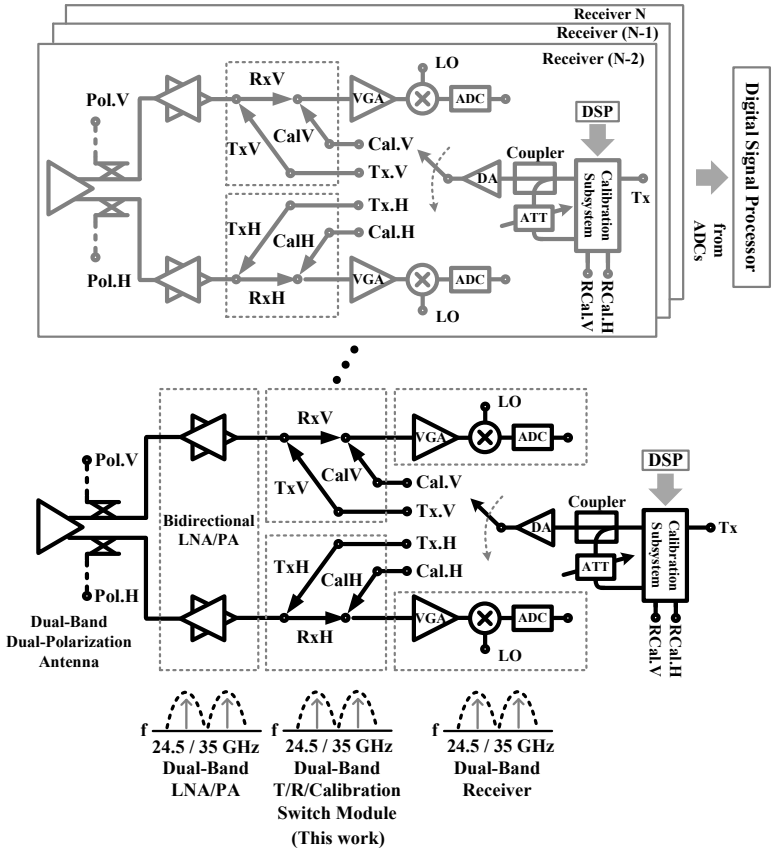
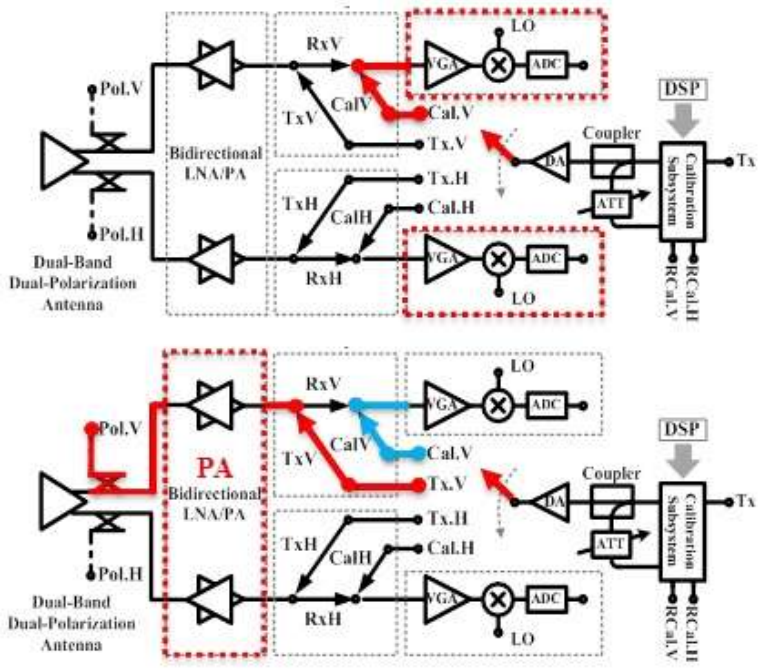


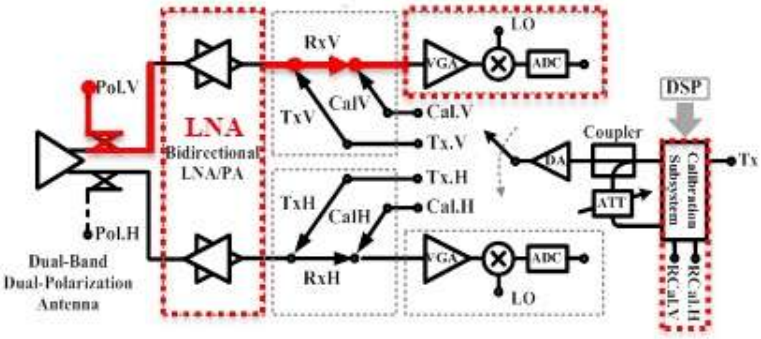
Figure 2.2.Digital beam forming array architecture

frequency diversity provide numerous advantages in detection, identification, locating and tracking a wide range of targets, including enhanced detection coverage, accurate target location, reduced survey time and cost, increased resolution, improved reliability and target information.

One of the challenging issues in an antenna-array system design is the calibration. Calibration is a critical issue, especially for millimeter-wave systems, due to various uncertainties such as imbalance and incoherence among receiver channels,



(a)



(b)

Figure 2.3.Calibration scheme (a) Transmit reference calibration and (b) Receive calibration

imbalances in amplitude and phase from components, unavoidable differences between LO signals, and power-distribution reconstruction errors in signal processing resulting from non-ideal situations. Especially for single-chip array systems, the inevitable

changes of signal parameters with process, voltage and temperature variations result in amplitude and phase errors in various constituent on-chip subsystems including the array transceiver.

In particular, an accurate calibration is a matter of significant importance for some array systems such as that proposed in Fig. 2.2 having bidirectional amplifiers for the digital beam forming (DBF) architecture in [35] or a location sensor in [36]. Moreover, in a fully polarimetric sensing system, the need of accurate calibration is critical since the ratios of amplitude and the deviations in phase between the four polarimetric (HH, VV, HV, and VH) signals contain important information for the image synthesis. A failure in accurate calibration may degrade the benefit of utilizing full polarimetry and result in misinterpretation of scattered signals. The accurate calibration can be achieved by system design in conjunction with digital signal processing. Achieving this very strict requirement of calibration is extremely difficult, particularly for systems-on-chip. A periodic calibration operation can help maintain the original performance of an array system by establishing the correction on the magnitude and phase in all the array channels.

The internal calibration for the proposed array system in Fig. 2.2 is composed of two operations, namely, transmit reference calibration and receive calibration.

In the transmit reference calibration, the dual-band receivers (VGA, Mixer and ADC chain) in Fig. 2.3(a). are calibrated first. A weak signal from the driver amplifier (DA) will be sent to Cal.H and Cal.V port and go through CalH and CalV path in the T/R/Calibration switch module and the corresponding dual-band receiver to compare the

output signals. The differences in amplitude and phase are recorded and designated as the receiver errors. Second, the weak signal from the DA will be directed to Tx.H and Tx.V port to go through TxH and TxV path in the T/R/Calibration switch module and the PA path of the bidirectional amplifier in each polarization channel. Third, the coupled signals from Pol.H and pol.V port will be sent to Cal.H and Cal.V port, respectively, and go through the corresponding H- and V- channel receiver. From the received signals, the designated receiver errors are subtracted to identify the deviations in magnitude and phase between each H- and V- channel, which are essentially the transmit errors. In the transmit mode of system, this transmit error will be adjusted by the calibration subsystem so the transmit signal for each H- and V- polarization can be maintained identical.

In the receive calibration, attenuated signals from RCal.H and RCal.V port in Fig. 2.3(b) will be distributed to Pol.H and Pol.V port, respectively. The injected signal will go through the LNA path in the bidirectional amplifier, RxH and RxV path in the T/R/Calibration switch module and the dual-band receiver. The discrepancies of the amplitude and phase in the received signal between H- and V- channels will be recorded in a digital signal processor (DSP) block and classified as the gain and phase errors of the entire receiver including the LNA in the bidirectional amplifier, T/R/Calibration switch module and dual-band receiver. In the reception mode of system, this receiver error will be subtracted from the signals reflected by intended targets.

In operation, a potential target is illuminated in the transmission mode with calibrated transmitting signals and the backscattered signal from the target is received

through the antennas of all receivers in the reception mode. The digitalized output signals in this mode are essentially the backscattered signals from the target with the inherent gain and phase errors of the receiver channels embedded. The DSP then subtracts the errors recorded in the receive calibration mode from the received signals to extract useful information. This calibration procedure can also be used as a built-in diagnosis tools to self-check the system's function [36].

Compare to the RF domain phase shifting array architectures, which possess a spatial beam steering function [37], the digital beam former performs multiple beam generation at the DSP. Such array architecture without a spatial filtering operation is vulnerable to unfiltered strong interference signals, which may saturate receiver channels and burden baseband circuits including ADC with linearity and power consumption issues [35]. Therefore, it would be of a great benefit to reject out-of-band signals to alleviate the burden of both RF and baseband blocks in the DBF array system.

This section presents a novel fully integrated concurrent dual-band 0.18-μm BiCMOS T/R/Calibration switch module in *K*- and *Ka*-band centered at 24.5 and 35 GHz, combining the transmit/receive (T/R) function with the integrated calibration and filter function, for dual-band array systems such as the DBF array shown in Fig. 2.2 using Jazz 0.18-μm BiCMOS process [38]. Possible application of the T/R/Calibration switch module is in a communication or sensing dual-band system, which works in two different bands centered at 24.5 and 35 GHz simultaneously, such as that described in Fig. 2.2.

2.2.2 Background Theories

There has been a significant interest in the use of metamaterial composite right/left-handed (CRLH) transmission lines (TLs). The artificial combination of right-handed (RH) and left-handed (LH) networks enables the phase delay control of CRLH TLs [39-43].The CRLH TL is characterized by its phase constant β_{CRLH} and characteristic impedance Z_{CRLH}, which provide conditions to determine the transmission line's dispersion, as

$$\beta_{CRLH} = \omega\sqrt{L_R C_R} - \frac{1}{\omega\sqrt{L_L C_L}} \tag{2.1}$$

$$Z_{CRLH} = \sqrt{\frac{L_R}{C_R}} = \sqrt{\frac{L_L}{C_L}} \tag{2.2}$$

where L_R, C_R and L_L,C_L are the inductance, capacitance for the right handedness and left handedness per unit cell of the CRLH TL, respectively. Equations (2.1)-(2.2) offer an extra degree of freedom to control the phase delay of a CRLH TL. This property can be utilized to realize quarter-wavelength TLs at two arbitrary design frequencies. In other words, the general dispersive phase delay relationship of a CRLH TL as shown in Eq. (2.1) enables the quarter-wavelength characteristic at two arbitrary frequencies upon enforcing the characteristic impedance condition in Eq. (2.2).

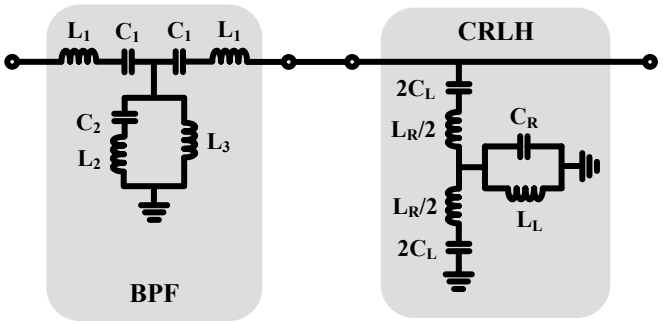
2.2.3 T/R/Calibration Switch Module Design

In this section, the proposed concurrent dual *K*/*Ka*-band T/R/Calibration switch module design is introduced in detail. First, the fundamental ideas in realizing dual bandpass filtering frequency response will be presented, which will be followed by circuit level details with complete module's performance evaluation.

2.2.3.1 Cascaded Quasi-elliptic Dual-bandpass Network

One of the major concerns in developing the T/R/Calibration switch module presented in this paper is to create a dual-band filtering function in the receiver path. As briefly explained earlier, the DBF array transceiver shown in Fig. 2.2 operates without a spatial beam steering function and therefore a rejection of out-of-band signals is essential. By employing bandpass filtering function in the proposed T/R/Calibration switch module, it was intended to achieve an out-of-band rejection of more than 30 dB below 10.5 GHz and above 59 GHz (2nd order IMDs).

Fig. 2.4 shows the cascaded quasi-elliptic dual-bandpass network, which is the main body of the complete T/R/Calibration switch module, assuming (non-resistive) ideal elements. It can be divided into two separate parts, namely, a bandpass filter (BPF) and a CRLH section, which are separately synthesized to meet certain magnitude and phase delay specifications, respectively.



Component values for cascaded dual-bandpass network with quasi-elliptic response			
C_1	81.83 fF	L_1	350 pH
C_2	133.5 fF	L_2	45 pH
C_R	428.7 fF	L_3	166.2 pH
C_L	27.56 fF	L_R	1071 pH
		L_L	68.9 pH

Figure 2.4.Cascaded quasi-elliptic dual-bandpass network

The BPF is the third-order type-I Chebyshev filter with an additional inductor (L_2) inserted in the shunt resonator tank to realize an additional rejection-zero at 65 GHz. The rejection-zero was added to make the high-frequency skirt characteristic sharper. The insertion loss (S21) and pole/zero plots associated with the BPF are presented in Figs. 2.5(a) and (b), respectively. As shown in Fig. 2.5(a), the BPF is wideband with a bandwidth of 13.5 GHz centered at 30 GHz. The associated pole/zero plot in Fig. 2.5(b) shows two zeros at the origin and a complex conjugate pair of zeros at 65 GHz. This BPF network has two poles at 23.28 GHz and 36.78 GHz which determines its bandwidth.

The S21 and pole/zero plot of the CRLH are displayed in Figs. 2.5(a) and (c), respectively. As explained in the previous section, this CRLH network creates quarter-wavelength consecutively to make open at two design frequencies, herein, 24.5 and 35 GHz. It can be seen from Fig. 2.5(a) that the insertion losses at the design frequencies are 0 dB due to this extra ordinary phase delay of this network. Also observed in the plot is a rejection occurring at the transition frequency of 29.28 GHz. In the pole/zero plot for

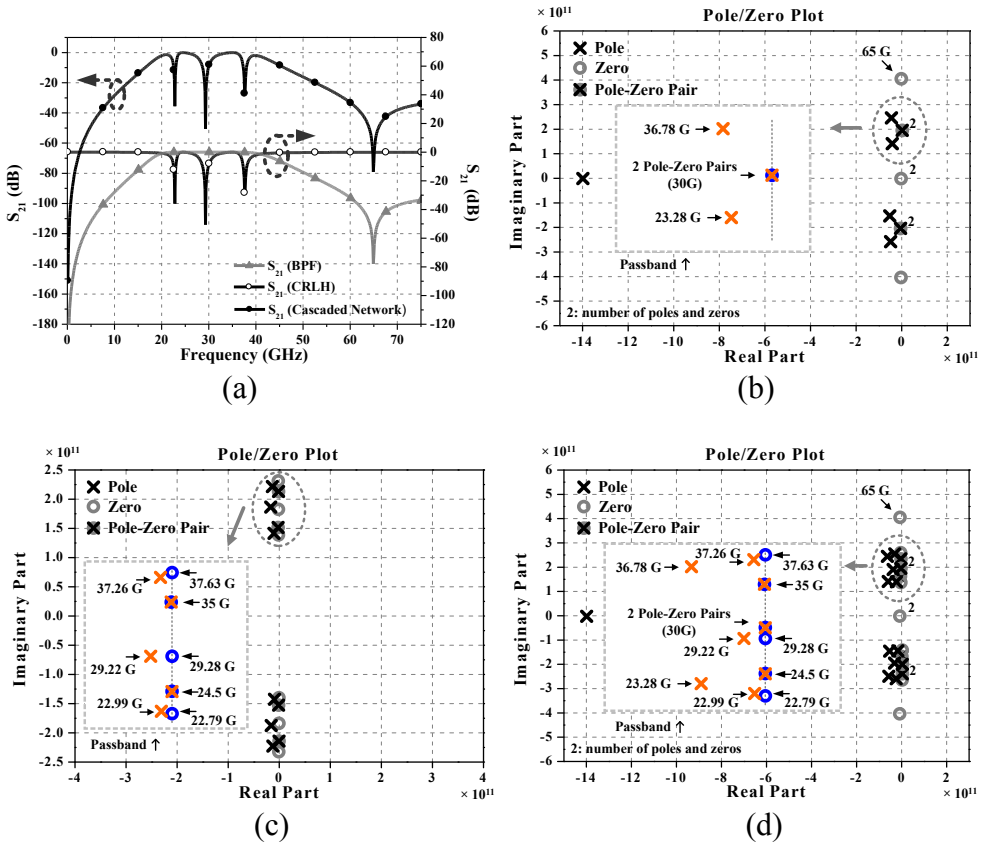


Figure 2.5.(a) S21 plot, (b) Pole/Zero plot: BPF, (c) Pole/Zero plot: CRLH TL, and (d) Pole/Zero plot: Cascaded BPF and CRLH TL

the CRLH network, the overlapped pole/zero pairs on the $j\omega$ axis at 24.5 and 35 GHz suggest that this network has no loss at those design frequencies. The transmission zeros in the S21 plot also appears in the pole/zero plot.

Along with the poles and zeros on the $j\omega$ axis, what should be examined closely are the critical poles of the CRLH network. The critical pole which appears at 29.22 GHz should be of a great concern since its frequency is very close to the zero appearing at 29.28 GHz. Thus if a certain margin of stability is not guaranteed, the critical pole at

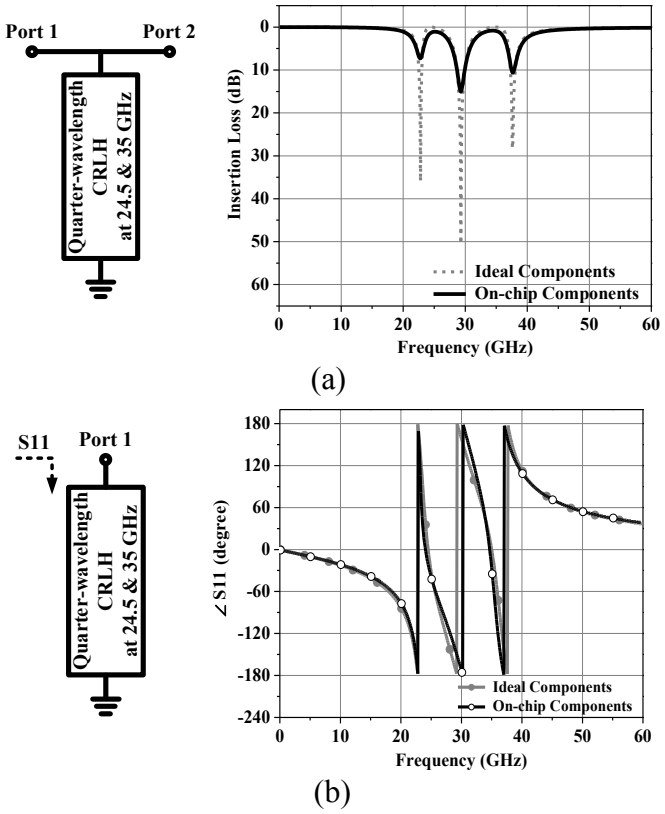


Figure 2.6.Simulated (a) S21 of two-port CRLH and (b) phase of S11 of one-port CRLH

29.22 GHz would start to move toward the $j\omega$ axis of the pole/zero plot, and eventually reaching the threshold of an oscillation. The calculated component values for +90º and -90º at the two design frequencies in the paper, 24.5 and 35 GHz, using a single unit cell of the CRLH are listed in Table I. The characteristic impedance for this network is 50 Ohm. This CRLH section will be coupled with a negative-resistance generation circuit to be presented later to improve the quality factor at 29.28 GHz.

The dual-bandpass filtering function of the entire network in Fig. 2.4 is realized by cascading the BPF and CRLH sections discussed above. As shown in Fig. 2.5(a), the

BPF section creates a wide pass-band including the design frequencies of 24.5 and 35 GHz while the CRLH section creates open only at these two design frequencies. The S21 plot of the entire cascaded network is also presented in Fig. 2.5(a), showing a dual-bandpass filtering characteristic. It can be seen from the pole/zero plot of this entire network in Fig. 2.5(d) that all the poles and zeros observed in the separate BPF and CRLH networks appear together. By examining the pole/zero locations shown in Fig. 2.5(d), it can be seen that this network provides quasi-elliptic frequency response. Although the entire network in Fig. 2.4 may be considered as a dual-bandpass filter, categorizing it as a network with a quasi-elliptic dual-bandpass response, rather than as a dual-bandpass filter, is more reasonable since the dual-band frequency response of the CRLH section is the result of a specific phase delay, not a dual-band filter synthesis based on magnitude specifications per se.

2.2.3.2 Dual-band Quarter-wavelength Network Coupled with a Negative Resistance Generation Circuit

A difficulty in utilizing the CRLH TL for a dual-bandpass filtering function presented in the previous section is the low quality factors (Q) of on-chip components, especially those of inductors. They significantly deteriorate the frequency response and limit the signal rejection at the transition frequency to around 15 dB. Figs. 2.6(a) and (b) show the simulated insertion loss and the phase of the reflection coefficient of two-port

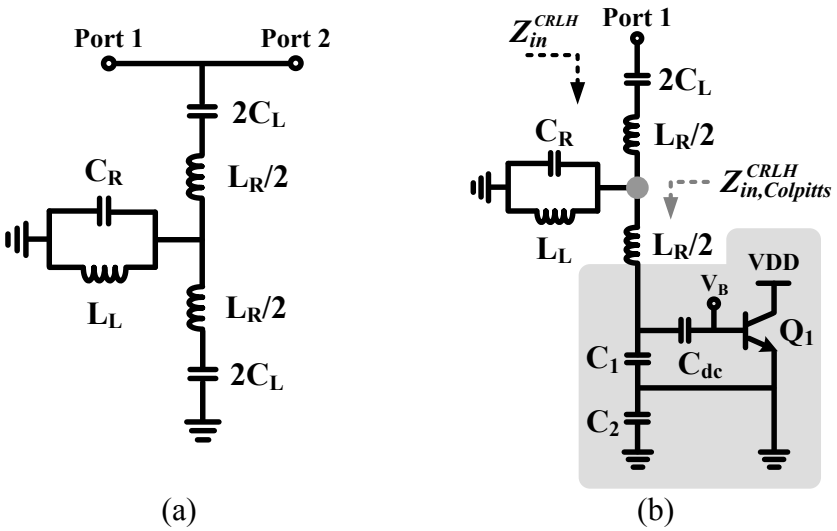


Figure 2.7.(a) Original passive CRLH network and (b) CRLH network coupled with a Colpitts style negative resistance generation circuit

and one-port single-cell CRLH networks, respectively, using the ideal and actual on-chip components.

For the simulation results with on-chip components, the real PDK (process design kit) capacitors from Jazz 0.18-µm BiCMOS process [38] and actual EM-simulated spiral inductors are used. As shown in Fig. 2.6.(a), the frequency response with the actual on-chip components loses its sharp frequency response due to the components' low Q, while still maintaining the intended phase delay at the design frequencies as seen in Fig. 2.6(b). As displayed in Fig. 2.6(b), the phase of S11 of the one-port CRLH structure crosses zero consecutively at the two design frequencies, thereby providing a sufficient condition to prove that this network creates an open in virtue of the quarter-wavelength at the design frequencies. A difficulty in utilizing the

CRLH TL for a dual-bandpass filtering function presented in the previous section is the low quality factors (Q) of on-chip components, especially those of inductors. They significantly deteriorate the frequency response and limit the signal rejection at the transition frequency to around 15 dB. Figs. 2.6(a) and (b) show the simulated insertion loss and the phase of the reflection coefficient of two-port and one-port single-cell CRLH networks, respectively, using the ideal and actual on-chip components.

To overcome the low Q issue, a Colpitts style negative-resistance generation circuit is coupled with the CRLH network as shown in Fig. 2.7. The original passive CRLH network is shown in Fig. 2.7(a) and the CRLH network with improved Q is described in Fig. 2.7(b). It should be noted that the transition frequency appears at [41]

$$\omega_O = \frac{1}{\sqrt[4]{L_R C_R L_L C_L}} \tag{2.3}$$

The resonant frequencies of series L_R and C_L and shunt L_L and C_R are

$$\omega_{SE} = \frac{1}{\sqrt{L_R C_L}}, \quad \omega_{SH} = \frac{1}{\sqrt{L_L C_R}} \tag{2.4}$$

respectively. These resonant frequencies are equal upon enforcing the condition (2.2) which leads $\omega_O = \omega_{SE} = \omega_{SH}$. A Colpitts style negative resistance generation circuit is coupled with the original CRLH network as shown in Fig. 2.7(b) at $L_R/2$ and $2C_L$ section

of which resonant frequency is ω_{SE}. The input impedances designated in Fig. 2.7(b) can be expressed as

$$Z_{IN}^{CRLH} = (j\omega L_R/2 + \frac{1}{j\omega 2C_L}) + (j\omega L_L \,\|\, \frac{1}{j\omega C_R}) \,\|\, Z_{IN,Colpitts}^{CRLH} \tag{2.5}$$

$$Z_{IN,Colpitts}^{CRLH} = R_{L_R/2} + j\omega L_R/2 + \frac{1}{j\omega}\left(\frac{1}{C_1} + \frac{1}{C_2}\right) - \frac{g_m}{\omega^2 C_1 C_2} \tag{2.6}$$

where $R_{Lg/2}$ and g_m are the resistance of the inductor $L_R/2$ and the transconductance of the BJT Q_1, respectively. The resistance is inserted only in (2.6) to facilitate manifesting a condition for Q enhancement. For the circuit in Fig. 2.7(b) to operate properly, it is necessary for it to maintain the same phase delay as in the original network shown in Fig. 2.7(a). To that end, the capacitor values of C_1 and C_2 must comply with the condition below, excluding parasitic capacitances to accommodate the desired phase delay and hence the unique dual-band characteristic offered by the CRLH TL:

$$2C_L = \frac{C_1 C_2}{C_1 + C_2} \tag{2.7}$$

Also, the current level which determines the transconductance of Q1 should be chosen carefully to prevent a possible instability which could arise from the existence of a negative resistance. As is seen in (2.6), the negative g_m can effectively cancel out the resistance in the network, thereby enhancing the Q at the transition frequency. However, an excessive negative resistance at the transition frequency (29.28 GHz) can cause the

adjacent critical pole at 29.22 GHz driven to the $j\omega$ axis on the pole/zero map, leading the network to an oscillation state or a marginally stable state. The critical pole at 29.22 GHz was already verified with the pole/zero analysis of the CRLH network.

The marginal stability condition when the oscillation could possibly occur due to the excessive negative g_m can be derived from (2.6). Besides the resistance $R_{Lg/2}$ in the Colpitts negative-resistance generation section of the CRLH network, there is also some resistance introduced by external circuits connected to this network. The quantitative expression for a marginal stability can then be written as

$$\frac{g_m^{osc}}{\omega^2 C_1 C_2} = R_{L_R/2} + R_{ext} \tag{2.8}$$

where g_m^{osc} and R_{ext} mean the transconductance for an oscillation and resistance introduced by external circuits, respectively. The optimum transconductance g_m^{opt} for Q enhancement without an oscillation can be derived as

$$g_m^{opt} = \omega^2 C_1 C_2 R_{L_R/2} \tag{2.9}$$

By taking the ratio of (2.8) for the possible oscillation and (2.9) for the optimum resistance cancellation, the safety margin can be obtained as

$$I_{osc} = I_{opt}\left(1 + \frac{R_{ext}}{R_{L_R/2}}\right) \tag{2.10}$$

where I_{osc} and I_{opt} are the current for oscillation and optimum resistance cancellation, respectively. From (2.10), it can be observed that the current for an oscillation is always larger than the current for the optimum resistance cancellation for Q enhancement. The additional resistance introduced with external circuits hence prevents oscillation from an excessive negative transconductance by adding more loss which preserves a stable operation.

2.2.4 T/R/Calibration Switch Module Architecture, Analysis, and Design

In this section, the developed concurrent dual *K*/*Ka*- band T/R/Calibration switch module with quasi-elliptic dual-bandpass frequency response is presented with its entire architecture.

Since the switch function of the proposed module is dependent on the nMOS transistors, the physical structure of deep n-well nMOS transistor will be overviewed first. A biasing technique to overcome the inherent high-frequency leakage path is presented for the use of the deep n-well nMOS transistors as switch. The entire integrated switch module architecture which supports dual bandpass filtering function in multi paths are presented in detail with the complete integrated digital control circuitry for a pair of T/R/Calibration switch module for both V- and H- polarization transceiver.

2.2.4.1 Deep n-well NMOS Transistors

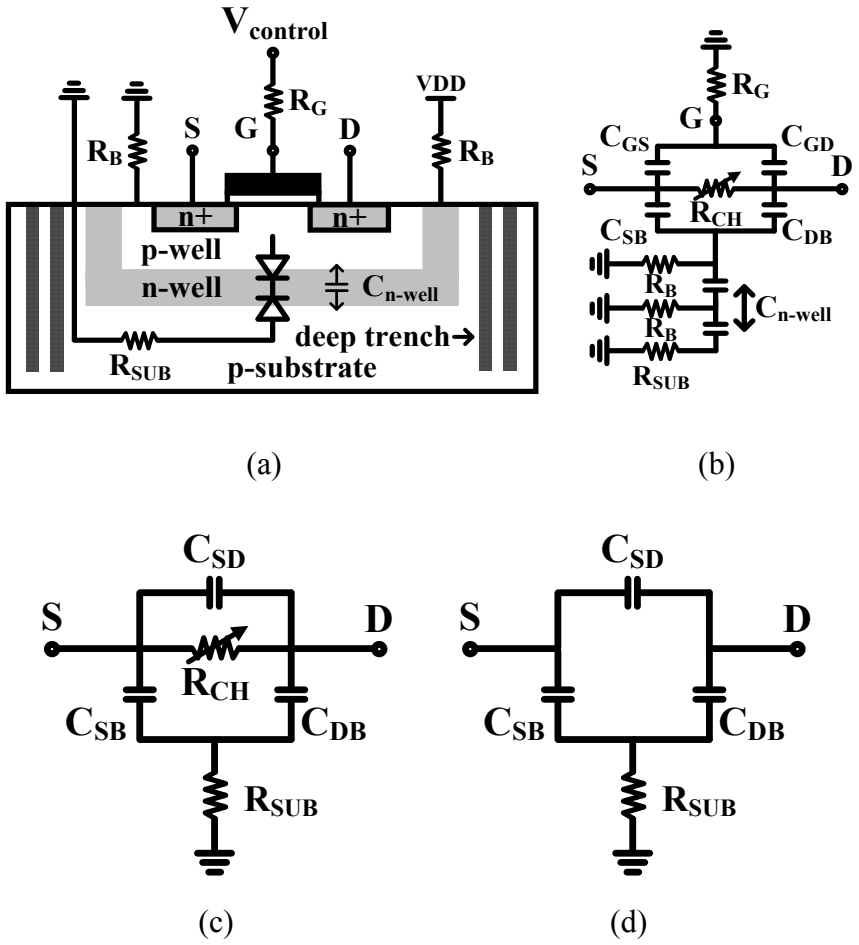


Figure 2.8.(a) Cross sectional view of nMOS transistor, (b) its equivalent circuit, and simplified (c) on-state, and (d) off-state equivalent circuits. C_{SD}, C_{SB}, C_{DB}, R_{CH}, and R_{SUB} represent the parasitic capacitance between the source and drain, source and body, drain and body, on-state resistance, and equivalent resistance of the substrate, respectively.

Fig. 2.8 presents a simplified cross-sectional geometry of a deep n-well CMOS transistor and its equivalent-circuit model. Deep n-well transistors have been used in the design of switches [45-48]. The deep n-well provides isolated p-well for nMOS devices,

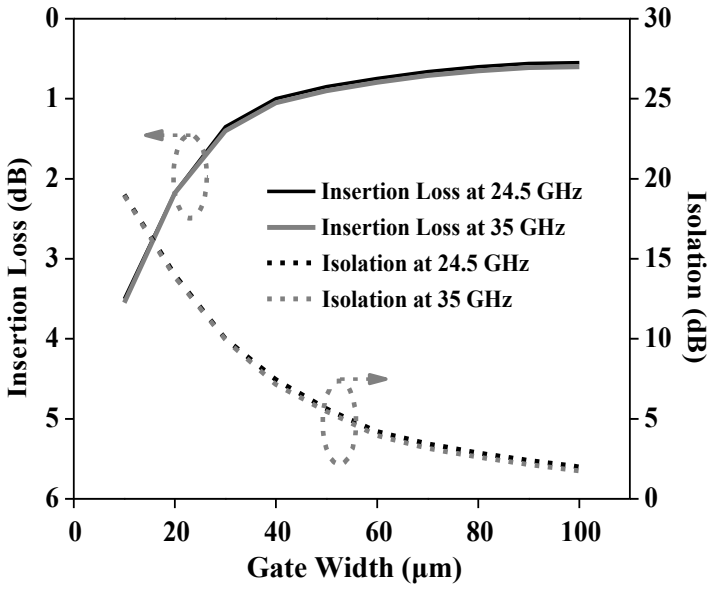


Figure 2.9.Insertion loss and isolation for different nMOS gate widths

thus floating them on a bulk substrate. To prevent the signal loss due to the junction capacitance caused by the deep n-well, it can be biased at 1.8 V while the isolated p-well/p-substrate is biased at 0 V, thus keeping the junction diodes reverse-biased all the time [44-47]. Along with the deep n-well process, a double deep trench, as seen in Fig. 2.8(a), is also used in the actual layout to prevent the coupling of noise and unwanted signals from adjacent devices.

Simplified equivalent-circuit models for the on- and off-state transistors are shown in Figs. 2.8(c) and (d), respectively. The simulated insertion loss and isolation of nMOS transistors with different widths are provided in Fig. 2.9. The total widths of nMOS transistorsT_1 and T_2 in Fig. 2.10were chosen as 76 μm (finger width: 3.8 μm, number of fingers: 20) and 58 μm (finger width: 3.8 μm, number of fingers: 15),

respectively, based on the simulation results shown in Fig. 2.9. While it is important to maintain low insertion loss and high isolation for the T/R/Calibration switch module, it becomes particularly critical to maintain high isolation in the proposed array transceiver in Fig.2.2, which utilizes the full polarimetry. First in the reception mode, the leakage signals from Tx and Calibration port to Rx port should be minimized, since unwanted leakage from the internal signal source could deteriorate the reception signal, ultimately degrading the quality of the images attained from the system. In the transmission mode, it is critical to block the high power to both of the Rx and Calibration port in all the array channels to avoid receiver breakdown and a possible leakage feedback to the transmission path, respectively. In the calibration operation, any leakages induced from undesignated paths should be strictly minimized since the undesired addition of signals to the calibration signal would cause deviation in the calibration signal in each of the array channels. In the final switch module architecture as described later, parallel inductors are connected to the source and drain nodes of nMOS transistors to provide good isolation when switches are turned off.

2.2.4.2 Proposed T/R/Calibration Switch Module

The proposed concurrent dual-band T/R/Calibration switch module architecture is presented in Fig. 2.10. The T/R/Calibration switch is a four-port circuit including Antenna, Receiver (Rx), Transmitter (Tx), and Calibration ports. In this T/R/Calibration switch module, a dual-bandpass filtering function as mentioned in Section II is

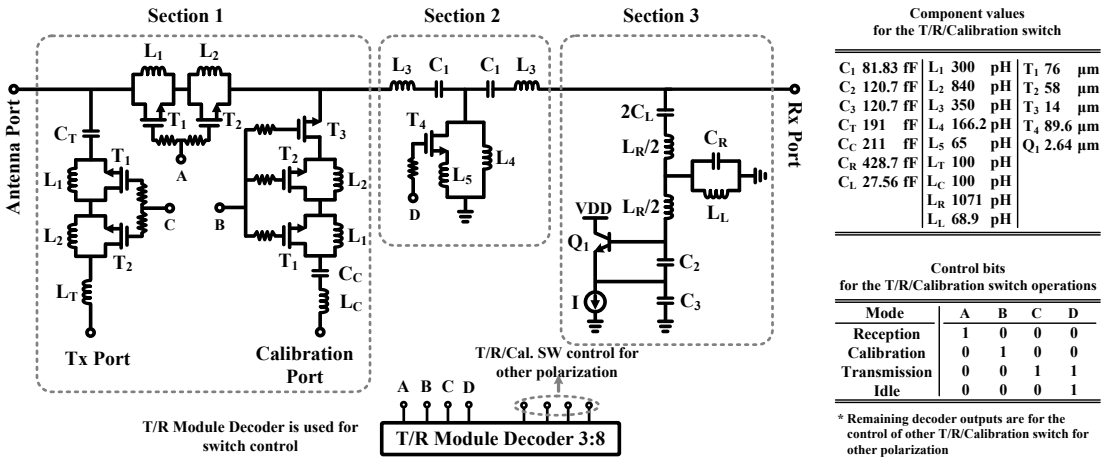


Figure 2.10. Proposed concurrent dual-bandpass T/R/Calibration switch module.

especially implemented in the reception path from the Antenna- to Rx-port to provide out-of-band rejection in all receiver channels, which are useful for many array transceivers including the DBF transceiver architecture. The T/R/Calibration switch works in four operation states to be described later: Transmission-, Reception-, Calibration-, and Idle- mode of operations.

The T/R/Calibration switch can be partitioned into three sections for the ease of a discussion. The first section is composed of identical pairs of parallel nMOS switch and inductor whose resonant frequencies are tuned at the two design frequencies of 24.5 and 35 GHz, respectively. When the nMOS switches are on, the parallel switch pairs provide a through path via on-state nMOS devices while, when they are off, the parallel inductance and equivalent capacitance of off-state nMOS devices produce high

impedance, thus blocking in-coming signals. The total capacitance of the off-state nMOS transistor can be calculated from the equivalent circuit in Fig. 2.8(d) as

$$C_{T\_OFF} = \frac{C_{SB}C_{DB}}{C_{SB} + C_{DB}} + C_{SD} \tag{2.11}$$

Given the aforementioned consideration in previous section, inductors L_1 and L_2were connected across the source and drain of T_1 and $T_2$to provide good isolation. These inductors were designed to form parallel resonances at 24.5 and 35 GHz when the switches are turned off according to

$$f_1(35GHz) = \frac{1}{2\pi\sqrt{L_1 C_{T1\_OFF}}} \tag{2.12}$$

$$f_2(24.5GHz) = \frac{1}{2\pi\sqrt{L_2 C_{T2\_OFF}}} \tag{2.13}$$

where C_{T1_OFF} and $C_{T2_OFF}$are the total capacitances of the off-state T_1 and T_2 as presented in (2.11), respectively. In the reception mode operation, the off state Tx and Calibration path work as shunt resonators, thus distorting the impedance condition in the Rx path. An additional capacitor (C_T) and nMOS (T_3) series switch are inserted in the Tx and Calibration path, respectively, to alleviate the loading effect induced by the resonators.

The second section is a Chebyshev band-pass filter integrating switching function to improve the isolation characteristic of the T/R/Calibration switch in the Transmission and Idle mode operation. The shunt capacitor in the parallel resonator is replaced with an nMOS switch. Based on the capacitance value of the Chebyshev band-pass filter design, the width of transistor T_4 is determined to be 89.6 μm for the capacitance value of 133.5 fF. The inductor L_5 is inserted in the shunt resonator tank simulated by T_4 and L_4 to form a rejection pole at 65 GHz to make a better skirt characteristic at higher rejection band.

The third section is the metamaterial CRLH dual-band quarter-wavelength network with improved Q. The unique dual-band phase delay creates an open at the two design frequencies while the enhanced Q at the transition frequency enables a high signal rejection between the two design frequencies. The incorporated negative resistance enhances the rejection between the design frequencies, hence overcoming the relatively small frequency ratio of 1.43 between these frequencies and the low Q factor of on-chip components. The cascaded network comprised of the second and third section creates dual-bandpass response as discussed earlier. The T/R/Calibration switch is operated as follows. In the Transmission mode, only the nMOS switch groups in the Tx path of the first section and T_4 in the second section are turned on while all other switches are off. In the Reception mode, only the switch group in the Rx path of the first section is turned on while all others are turned off. In the Calibration mode, only the switch group in the calibration path is turned on while having all other switches being turned off. A noteworthy feature in this mode of operation is that the frequency response

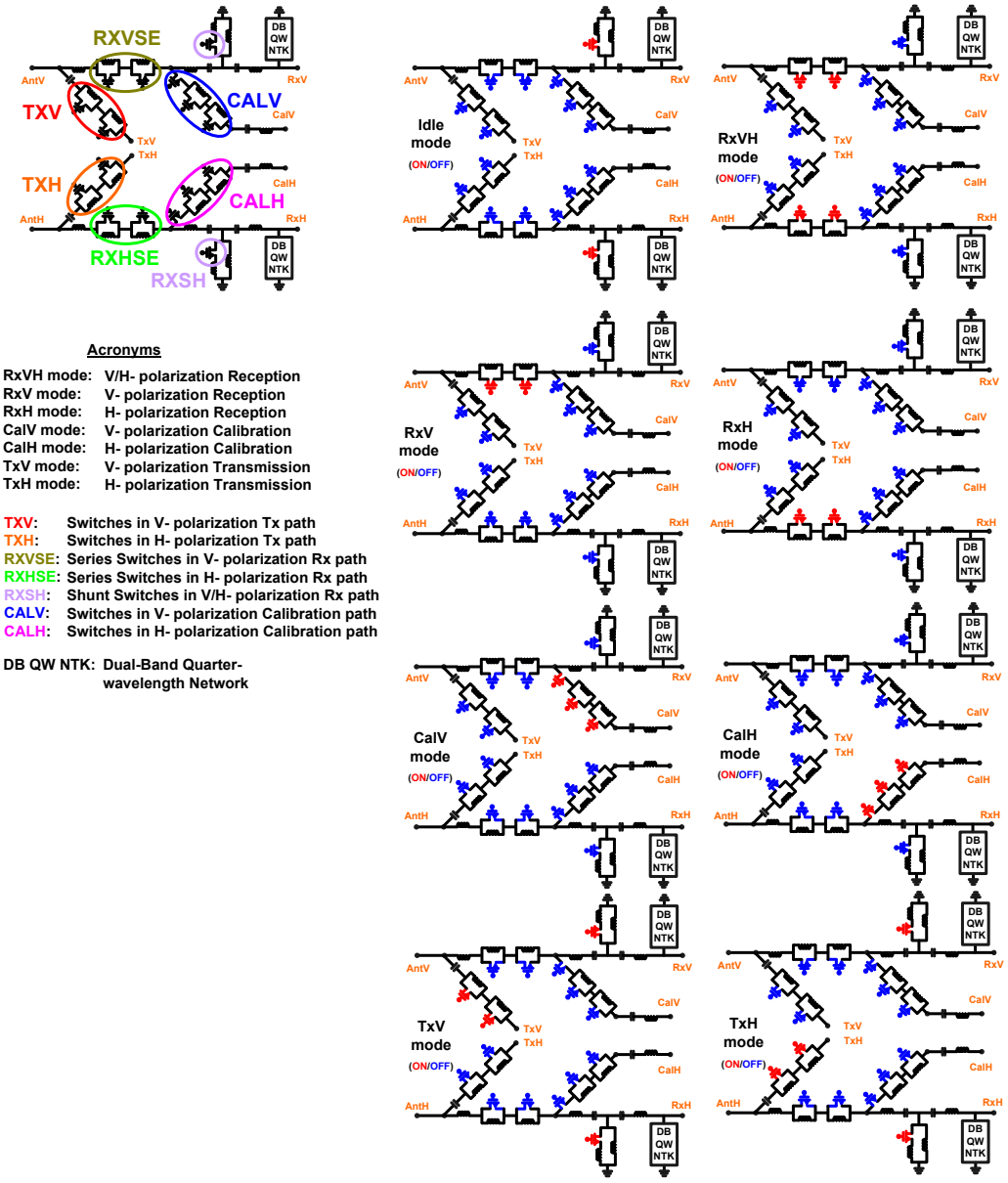


Figure 2.11.Digital control scheme for a pair of T/R/Calibration switch module for both V- and H- polarization transceiver

of the on-state calibration, which specifies the insertion loss between the Calibration and Rx port, emulates that of the reception-mode frequency response as close as possible

TXV: Switches in V- polarization Tx path
TXH: Switches in H- polarization Tx path
RXVSE: Series Switches in V- polarization Rx path
RXHSE: Series Switches in H- polarization Rx path
RXSH: Shunt Switches in V/H- polarization Rx path
CALV: Switches in V- polarization Calibration path
CALH: Switches in H- polarization Calibration path

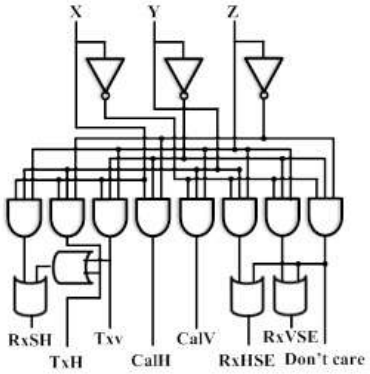
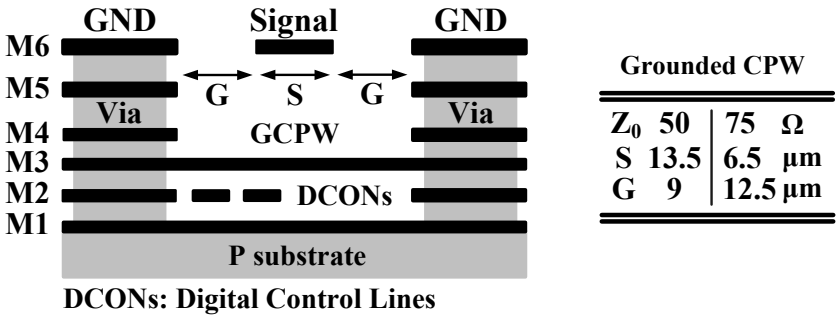


Figure 2.12.Digital control circuit for T/R/Calibration Switch Module

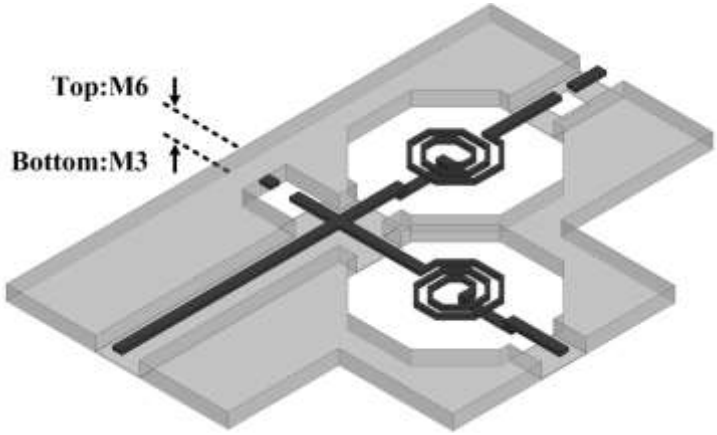
Table 2.1 Digital control scheme with modified 3:8 decoder

	X	Y	Z	Don't care	RXVSE	RXHSE	CALV	CALH	TXV	TXH	RXSH
RxVH	0	0	0	1	1	1	0	0	0	0	0
RxV	0	0	1	X	1	0	0	0	0	0	0
RxH	0	1	0	X	0	1	0	0	0	0	0
CalV	0	1	1	X	0	0	1	0	0	0	0
CalH	1	0	0	X	0	0	0	1	0	0	0
TxV	1	0	1	X	0	0	0	0	1	0	1
TxH	1	1	0	X	0	0	0	0	0	1	1
Idle	1	1	1	X	0	0	0	0	0	0	1

with a reduced magnitude, since the Calibration and Reception path share the second and third sections in common. It is attractive, given that performing a calibration from the very end of a receiver would assure the most accurate calibration results for array receivers.



(a)



(b)

Figure 2.13.(a) GCPW structure and (b) EM simulation model

The proposed T/R/Calibration architecture provides a calibration capability from the farthest end of the DBF transceiver. The component values for the switch are provided in the first table in Fig. 2.10. Table III in Fig. 2.10 summarizes the operation states and control bits of the T/R module decoder (3:8). The 10K-Ohm resistors at the gates of the nMOS switches prevent high frequency signal leakages. In the actual layout,

inverter pairs are connected before all these resistors to avoid drops of the control voltages due to lengthy connection lines.

Fig. 2.11 presents the digital control scheme for a pair of T/R/Calibration switch module for both the V- and H- polarization transceiver. This high level integration with digital control circuit enables a complex operation with the full polarimetric array transceiver. The digital control circuit schematic and truth table is presented in Fig. 2.12 and Table 2.1, respectively.

2.2.4.3 GCPW and Comprehensive Electromagnetic Simulation

The entire four-port T/R/Calibration switch is designed with Grounded Coplanar Waveguide (GCPW) structure. The metal stack-up for the GCPW employed in the proposed T/R/Calibration switch module is shown in Fig. 2.13(a). The topmost metal M6 is used as the main signal path while M3 is used as the bottom ground plane. All other metal layers used for the ground are interconnected by vias as shown. The control DC voltages for the switch operation are routed using strip lines in M2 layer with M1 and M3 ground planes. Two different GCPW with 50- and 75-Ohm characteristic impedance are used and their dimensions are provided in the table in Fig. 2.13.

The three dimensional view of an EM simulation model of a CRLH section is illustrated in Fig. 2.13(b). The illustration includes all components for a full-wave EM simulation using the GCPW structure shown in Fig. 2.13(a). The bottom ground plane in M3 metal layer underneath spiral inductors and MIM capacitors is perforated to remove

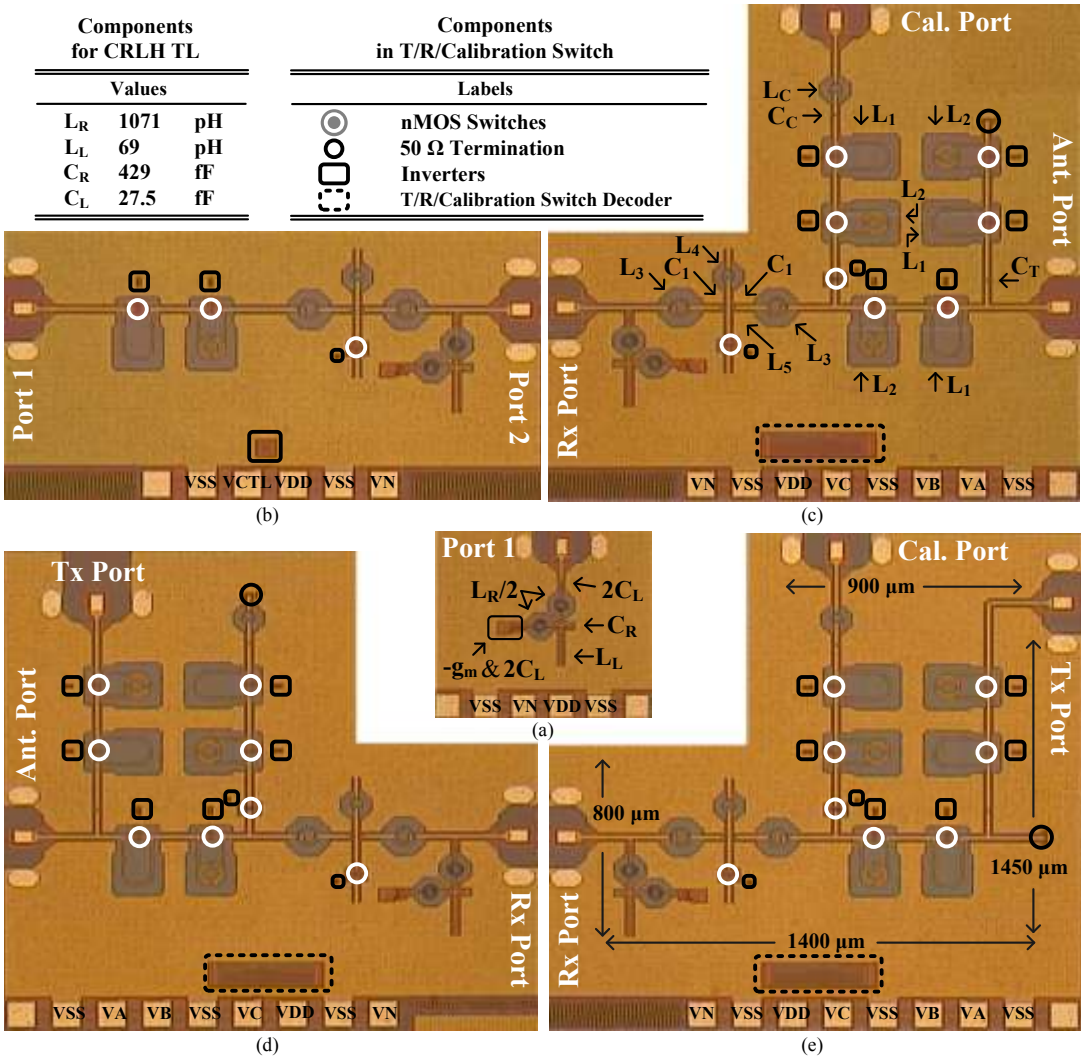


Figure 2.14.Microphotographs of T/R/Calibration switches: (a) one-port CRLH, (b) dual-bandpass SPST switch, (c) T/R/Calibration switch with Tx port termination, (d) T/R/Calibration switch with Calibration port termination, and (e) T/R/Calibration switch with Antenna port termination

parasitic capacitances to M3, which would degrade the Q of those elements. The full-wave EM simulations were performed using IE3D [48].

2.2.5 T/R/Calibration Switch Module: Performance and Discussion

In this section, the performance of the fabricated T/R/Calibration switch module is presented. Due to the four-port configuration of the switch, the proposed module is fabricated in multiple versions with different port termination. Also, the one-port active CRLH for phase measurement and two-port SPST (single-pole single-throw) switch with dual-band filtering function are presented. The S-parameter performance of all modes of operation of the switch module is presented and the linearity performance is shown as well.

2.2.5.1 Dual-band Metamaterial CRLH Network

The fabricated one-port dual-band CRLH network is shown in Fig. 2.14(a). Rather than going through a cumbersome de-embedding process to measure the phase response of the dual-band CRLH network, a simpler yet effective approach was made to make it a one-port circuit as appeared in the photograph. The phase of the reflection coefficient (S11) in this case should cross zero at 24.5 and 35 GHz consecutively because the network creates an open circuit due to the quarter-wavelength at these frequencies. As shown in Fig. 2.15, the simulated phase of S11 crosses zero degree at 24.5 and 35 GHz. The measured results show that the phase of S11 crosses zero at 24.35 and 37.1 GHz, suggesting the upper design frequency is shifted upward by 2.1 GHz. Minor changes in the inductance value by the inevitable process variation caused this

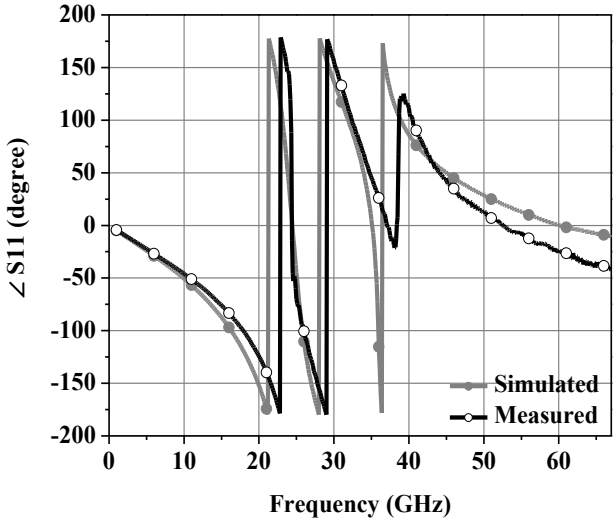


Figure 2.15.One-port CRLH ∠S11

frequency shift. The Colpitts style negative-resistance generation circuit contained in this network consumed 0.85 mA from V_{DD} of 1.8 V, which is the optimum current value to achieve a rejection ratio as high as 50 dB without any sign of an oscillation.

2.2.5.2 Dual-band Single-pole Single-throw Switch

Fig. 2.14(b) shows the fabricated dual-band SPST (Single-Pole Single-Throw) switch. It was fabricated to verify the dual-bandpass function without Tx- and Calibration- paths in the complete T/R/Calibration switch module. The dual-band SPST was designed by cascading two series switch pairs, a bandpass filter switch, and a CRLH network coupled with a negative-resistance generation circuit. The measured insertion loss (IL), isolation (ISO), and input (S11) and output (S22) return losses are shown in

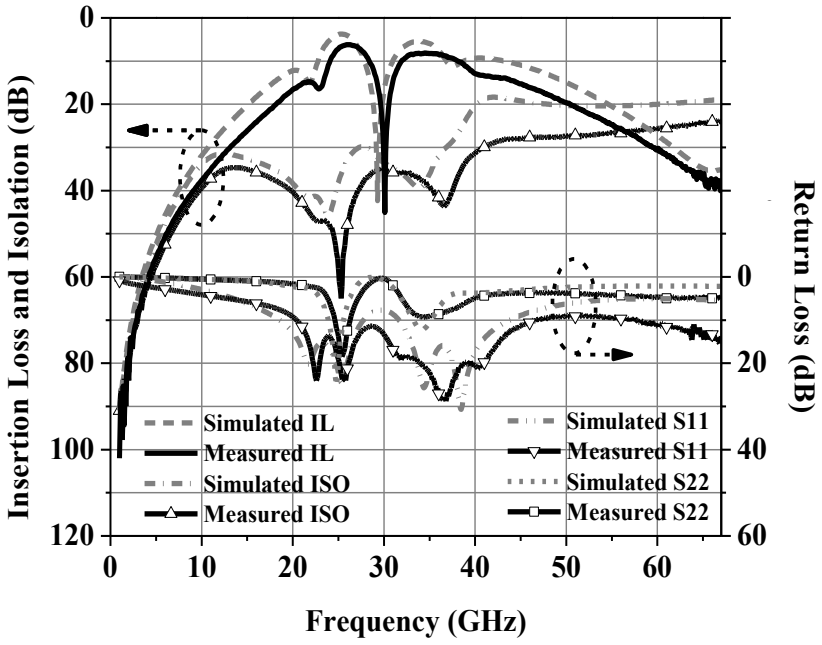


Figure 2.16.Dual-band SPST switch S parameters

Fig. 2.16. The measured (on-state) insertion loss of the SPST switch is 6.2 and 8.2 dB at the 24.5 and 35 GHz design frequencies, respectively, while the measured (off-state) isolation remains more than 30 dB up to 40 GHz and reaches 60 and 45 dB at 24.5 and 35 GHz, respectively. The input and output return losses are more than 10 dB. The measured and simulated results agree reasonably well.

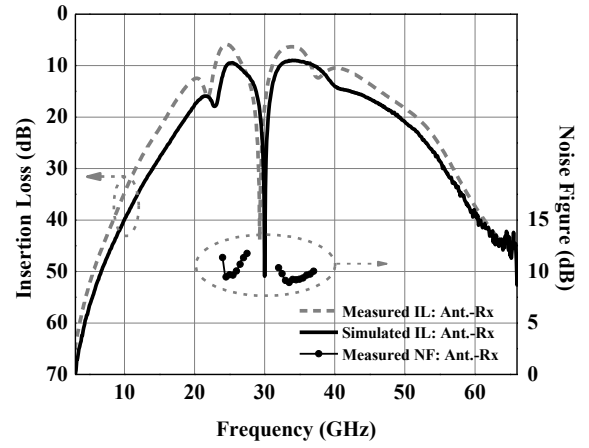
2.2.5.3 Dual-bandpass T/R/Calibration Switch Module

The complete dual-bandpass T/R/Calibration switch is a four-port circuit with the antenna, reception, transmission, and calibration ports. It is operated in four different

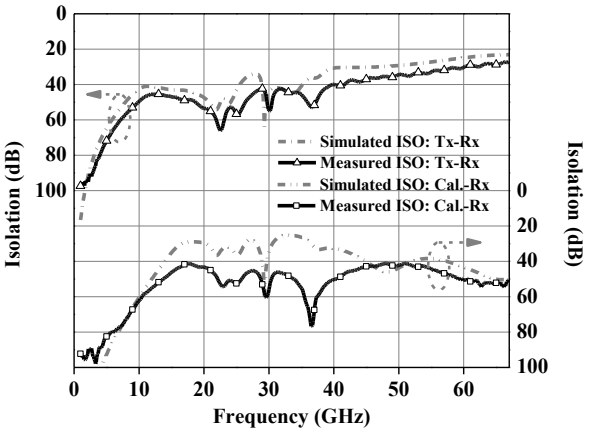
modes: reception, transmission, calibration and idle. Figs. 2.14 (c)-(e) show the dual-bandpass T/R/Calibration switches fabricated with different 50-Ohm port terminations for measurement purposes. The dual-bandpass filter function is integrated in both the receiver and calibration paths.

The concurrent dual-band frequency response of the reception path is duplicated with a reduced magnitude in the calibration path because these two paths share the same bandpass filter switch and proposed dual-band CRLH network. The second table in Fig. 2.14 shows the labels of the on-chip components.

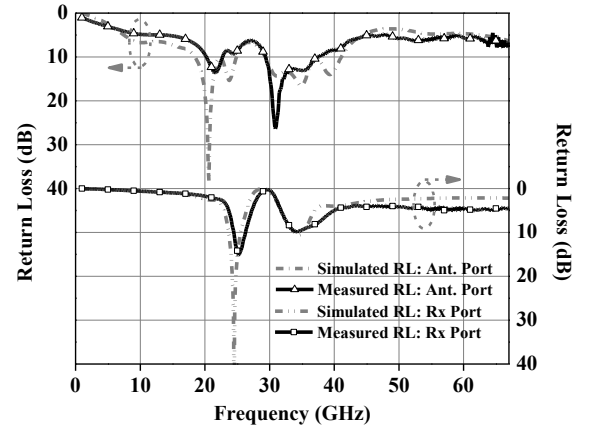
Reception Mode: The reception mode is assessed using the fabricated circuit in Fig. 2.14(c). The Tx port is terminated with a 50-Ohm resistor. Fig. 2.17(a) shows the insertion loss between the antenna and receiver ports and the isolation from the antenna to other ports. At the design frequencies of 24.5 and 35 GHz, the measured insertion losses are 9.4 and 9.1 dB, respectively. And the measured 3-dB bandwidth is from 23.7 to 28 GHz and from 31.14 to 38.9 GHz for each design frequency, respectively. The lowest measured noise figures in the aforementioned bands are 9.4 and 9.25 dB, respectively. Fig. 2.18 compares the insertion-loss responses with the negative g_m cell turned on and off, which shows the negative resistance effectively compensates the loss of the CRLH TL. When the g_m cell is turned off, the insertion losses reach 11.9 and 11.55 dB at 24.5 and 35 GHz, respectively, and the rejection at the transition frequency deteriorate only to show 11 dB difference compared to pass-band insertion losses.



(a)



(b)



(c)

Figure 2.17.Reception mode performance: (a) insertion loss, (b) isolation, and (c) return loss

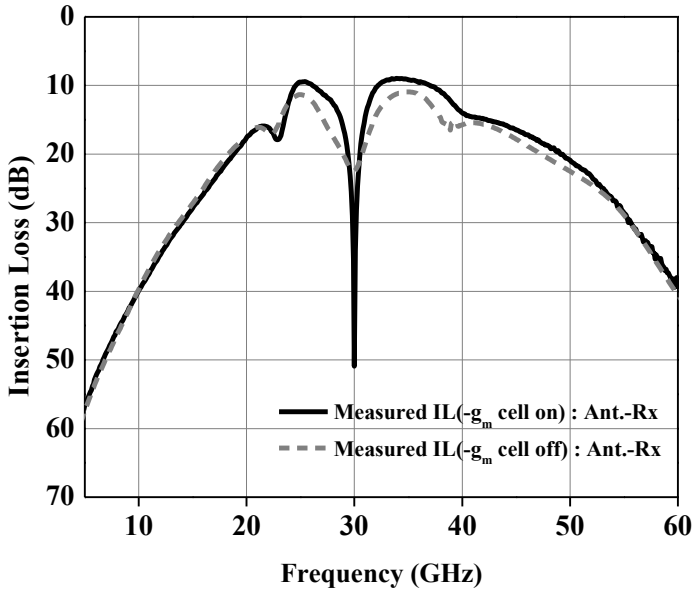


Figure 2.18.Reception-mode insertion loss with -g_m cell on and off

The rejection zero that makes a better skirt characteristic at higher frequency appears at around 65 GHz. The measured isolation between the Tx and Rx port is more than 30 dB up to 67 GHz, reaching as high as 55 dB from 24.25 to 24.75 GHz and 45 dB from 34.75 to 35.25 GHz. The highest isolation of 65 dB is achieved at 22 GHz. The measured isolation between the calibration and receiver ports is more than 45 dB from 20 to 44 GHz and reached 75 dB at about 38 GHz as presented in Fig. 2.17(b). The measured return losses are more than 9.3 dB from 24.25 to 24.75 GHz and 13 dB from 34.75 to 35.25 GHz at the antenna port, and more than 8.3 dB from 24.25 to 24.75 GHz and 9.3 dB from 34.75 to 35.25 GHz at the receiver port, as seen in Fig. 2.17(c). As can be seen, the measured and simulated insertion loss and return loss show reasonably good agreement.

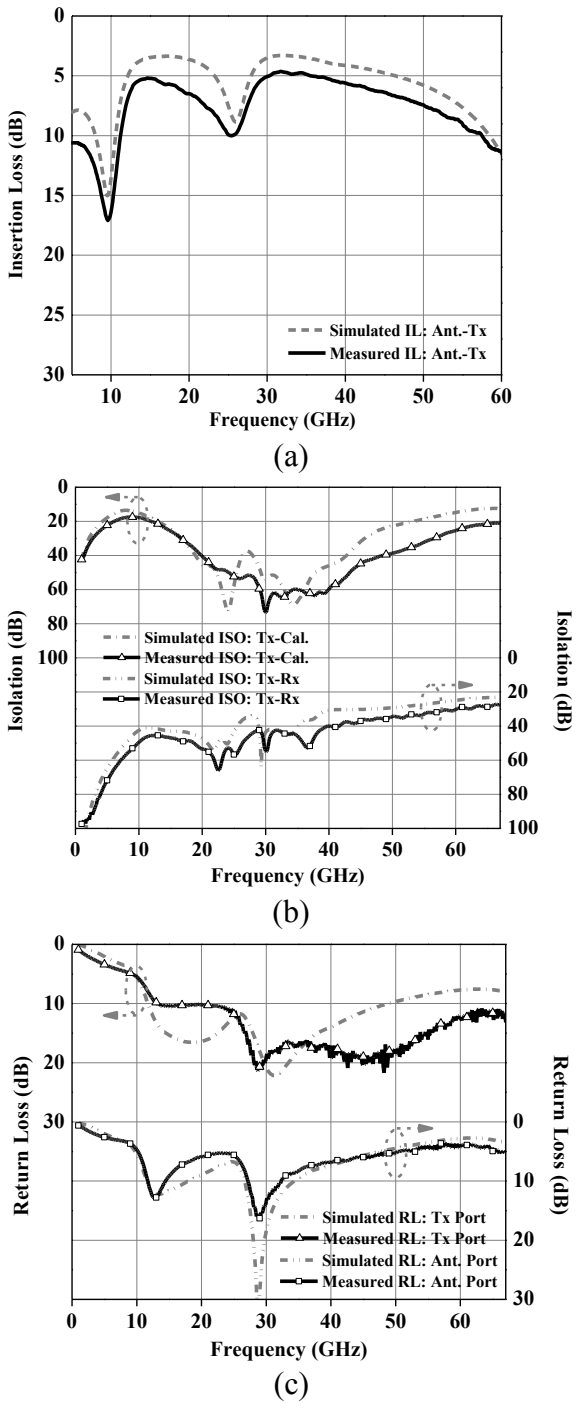


Figure 2.19.Transmission mode performance: (a) insertion loss, (b) isolation, and (c) return loss

Transmission Mode: Fig. 2.14(d) shows the T/R/Calibration switch with the calibration port terminated with a 50-Ohm resistor for the transmission-mode operation measurement. Fig. 2.19(a) shows the insertion loss and isolation. The measured insertion losses are between 9.1 to 9.6 dB from 24.25 to 24.75 GHz and between 4.8 to 5 dB from 34.75 to 35.25 GHz showing 9.2 and 4.9 dB at the design frequencies of 24.5 and 35 GHz, respectively. The measured isolation between the Tx and calibration ports is more than 55 and 60 dB at 24.5 and 35 GHz, respectively, and more than 40 dB from 20 to 50 GHz. The other measured isolation between the Tx and Rx port also remains more than 30 dB up to 67 GHz as well, achieving 50 dB from 24.25 to 24.75 GHz and 45 dB from 34.75 to 35.25 GHz. The measured isolations are presented in Fig. 2.19(b). The measured return loss, as displayed in Fig. 2.19(c), is more than 5.5 dB from 24.25 to 24.75 GHz and 8.5 dB from 34.75 to 35.25 GHz at the antenna port and more than 10 dB from 24.25 to 24.75 GHz and 17 dB from 34.75 to 35.25 GHz at the Tx port.

Calibration Mode: The T/R/Calibration switch with the antenna port terminated with a 50-Ohm resistor is shown in Fig. 2.14(e). As stated earlier, this T/R/Calibration switch architecture enables the calibration from the farthest end of the RF front-end, which would provide the best accurate calibration performance. Fig. 2.20(a) shows the insertion loss between the calibration and Rx ports and the isolation between other ports. Both of the measured insertion losses at 24.5 and 35 GHz are 12.3 dB. The measured 3-dB bandwidth was from 23.9 to 28.3 GHz and from 31.3 to 38.7 GHz for each design frequency, respectively. The measured isolation between the Tx and Rx ports is more

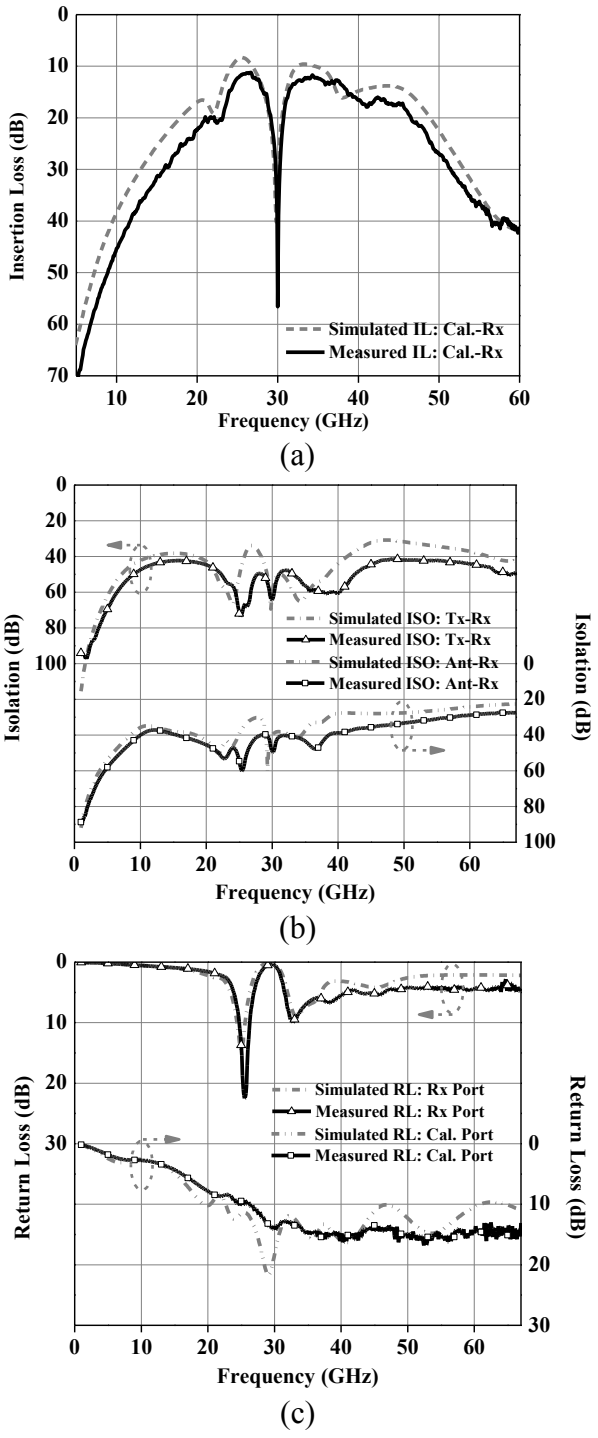
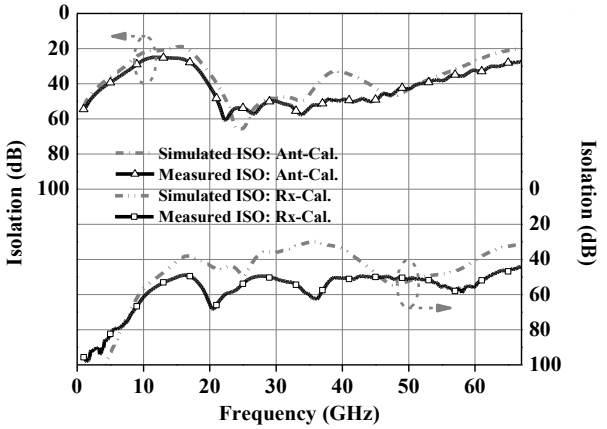
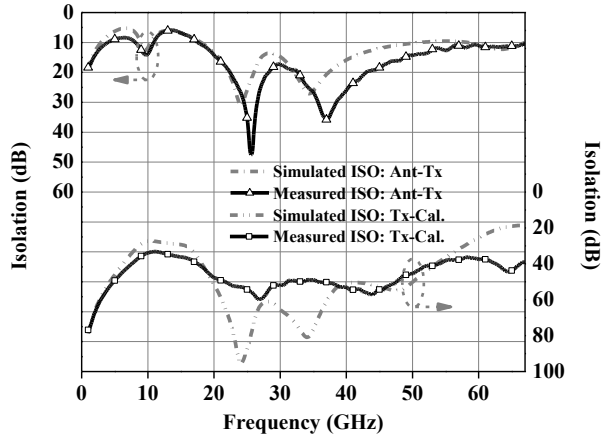


Figure 2.20.Calibration mode performance: (a) insertion loss, (b) isolation, and (c) return loss



(a)



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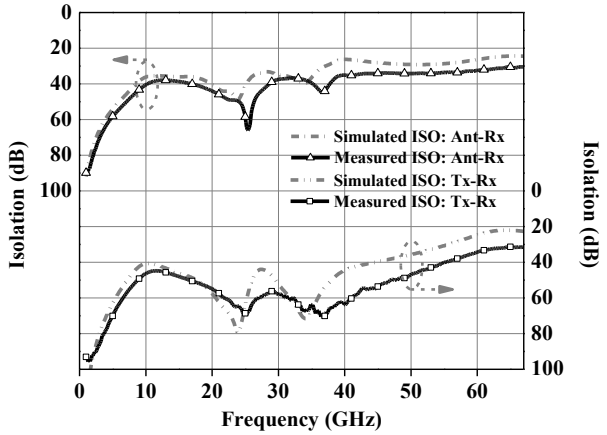


(c)

Figure 2.21.Idle mode performance: isolation between (a) Antenna-Calibration and Rx-Calibration ports, (b) Tx-Calibration and Antenna-Tx ports, and (c) Antenna-Rx and Tx-Rx ports

than 70 and 60 dB at 24.5 and 35 GHz, respectively, and more than 40 dB up to 67 GHz. And the isolation between the antenna and Rx ports remains more than 55 and 45 dB at 24.5 and 35 GHz while it is more than 30 dB from DC to 67 GHz. All the measured isolations appear in Fig. 2.20(b). The measured return loss, as seen in Fig. 2.20(c), is more than 10 dB from 24.25 to 24.75 GHz and 14.7 dB from 34.75 to 35.25 GHz at the calibration port, and more than 6.5 dB from 24.25 to 24.75 GHz and 6.5 dB from 34.75 to 35.25 GHz at the receiver port.

Idle Mode: An additional mode, namely Idle mode, is employed for non-operation state of the T/R/Calibration switch. The idle mode is executed with all the paths off when the complete transceiver does not perform any task. Good performance in this mode is essential for practical system operations in order to isolate the non-operating transceiver from undesired signals such as the leakage signals from transmitter and any incoming signals from antenna ports. Fig. 2.21 shows the six isolations between different ports. The measured isolations between the antenna and calibration, Rx and calibration, antenna and Tx, Tx and calibration, and antenna and Rx are more than 55, 50, 35, 50, and 40 dB, respectively, from 20 to 40 GHz. The measured isolation between Tx and Rx ports was more than 60 dB from 23.5 to 27.1 GHz and from 34 to 40.3 GHz.

2.2.5.4 Power Handling and Linearity

The simulated and measured linearity characteristics via insertion loss and

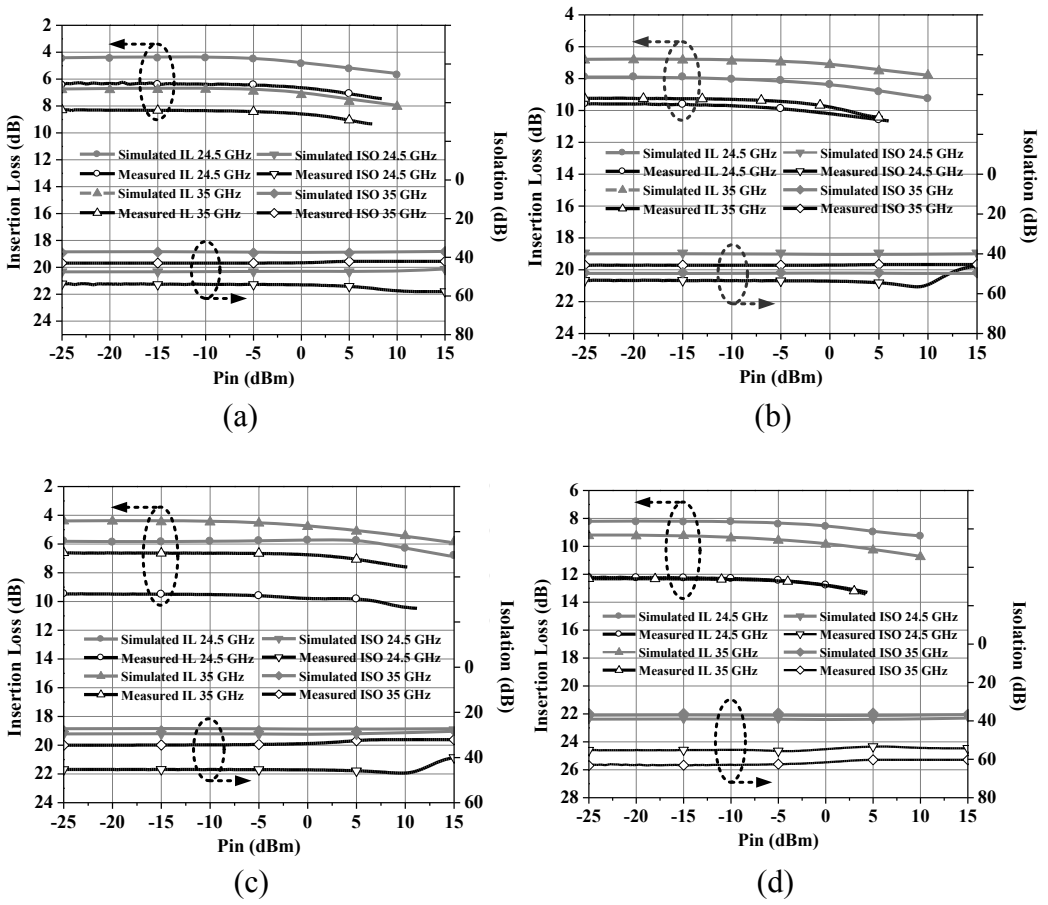


Figure 2.22.P1dB Linearity performance of the T/R/Calibration switch: (a) dual-band SPST, (b) reception path, (c) transmission path, and (d) calibration path

isolation are provided in Fig. 2.22. For dual-band SPST switch, the measured input 1-dB compression point was 8.6 and 7.5 dBm at 24.5 and 35 GHz, respectively. The measured isolation remains more than 43 dB with up to 15 dBm input power. For the reception mode of T/R/Calibration switch, both of the calculated and measured insertion loss and isolation are obtained from the antenna to Rx ports of the T/R/Calibration switch. The input 1-dB compression points are measured to be 5.6 and 5.4 dBm at 24.5 and 35 GHz, respectively. The isolation remains more than 45 dB with input power up to

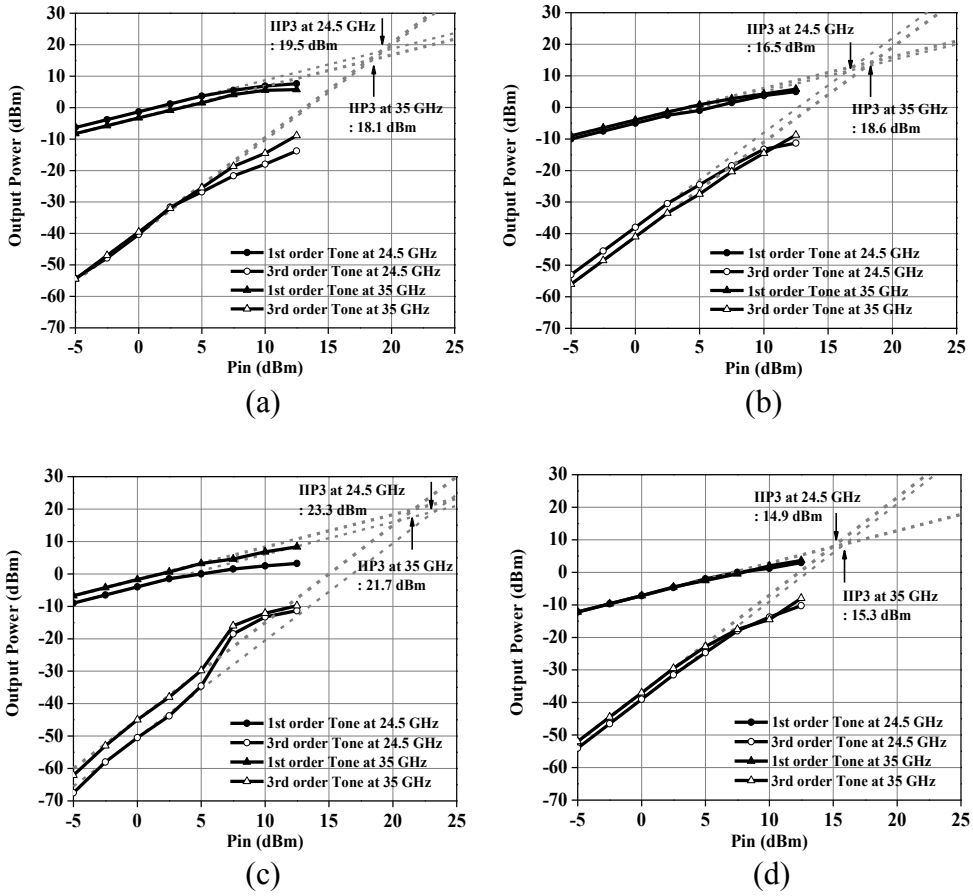


Figure 2.23.IP3 Linearity performance of the T/R/Calibration switch: (a) dual-band SPST, (b) reception path, (c) transmission path, and (d) calibration path

15 dBm at both design frequencies of 24.5 and 35 GHz. The measured linearity performance between the Tx and antenna port, in its on-state, shows the input 1-dB compression points of 11 and 10 dBm at 24.5 and 35 GHz, respectively. The isolation is more than 30 dB with an input power up to 15 dBm for both 24.5 and 35 GHz. Finally, for the calibration mode, the linearity performance is characterized between the calibration and Rx ports. The measured 1-dB power compression in the on-state occurs

at the input power of 4.2 and 3.9 dBm at 24.5 and 35 GHz, respectively. The isolation over the same path in its off-state is more than 50 dB with input power up to 15 dBm.

The results of the IIP3 measurement are shown in Fig. 2.23. The SPST switch shows the IIP3 of 16.5 and 18 dBm at 24.5 and 35 GHz, respectively. For each of the operation modes of the T/R/Calibration switch, the IIP3 were 16.5 and 18.6 dBm for the reception mode, 23.3 and 21.7 dBm for the transmission mode, and 14.9 and 15.3 dBm for the calibration mode, at 24.5 and 35 GHz, respectively.

2.2.5.5 Performance Discussion and Comparison

Table 2.2 summarizes the performance of the proposed T/R/Calibration switch module. There has been no work reported on four-port dual-band switch modules with integrated dual-band filtering function in *K/Ka*- band, which makes it ineffective in comparison of the performance of the proposed four-port dual *K/Ka*-band T/R/Calibration switch module. Nevertheless, an indirect performance comparison with other works has been attempted. To that end, the SPDT switch with the best insertion loss performance at 35 GHz [49] and the on-chip BPF [50] on similar silicon processes with similar out-of-band rejection characteristic to that of the proposed T/R/Calibration switch module are used for the insertion-loss performance comparison as follows. The SPDT switch in [49] and BPF in [50], which are optimized at 35 GHz, exhibit the insertion loss of 2.6 dB and 4.5 dB, respectively. To make the four-port configuration for comparison, a back-to-back connection of two SPDTs can be constructed, which exhibits

the insertion loss of around 5.2 dB. The cascade connection of the BPF in [50] and the back-to-back connected four-port switch would provide the insertion loss of around 9.7 dB. On the other hand, the proposed T/R/calibration switch module exhibits the insertion losses of 9.4/9.1 dB and 9.2/4.9 dB between Ant.-Rx and Tx-Ant. ports at 24.5/35 GHz in the reception and transmission modes, respectively. Excluding the Calibration path, which was intentionally designed to have more loss, the proposed T/R/Calibration switch module shows a similar or better insertion loss performance with a dual-band filtering response, not a single-band response, to a similarly configured component consisting of SPDTs [49] and BPF [50]. This is of particularly appealing considering the facts that the compared configuration is composed SPDTs [49] and BPF [50] optimized at the single design frequency of 35 GHz, while the proposed T/R/Calibration module was designed with band-pass filtering function and works concurrently in two different bands centered at 24.5 and 35 GHz. Also, considering the small frequency ratio between 24.5 and 35 GHz, which would require high Q-resonance for an agile frequency response, the proposed T/R/Calibration switch module shows a competitive loss and rejection performance. The rejection ratio between 24.5 and 35 GHz reaches as high as 50 dB and the out-of-band rejections are greater by more than 30 dB compared to pass bands in the frequency range below 10.5 GHz and above 59.5 GHz both for reception and calibration mode of operation. The measured input 1-dB compression points of 11 and 10 dBm at 24.5 and 35 GHz, respectively, would not cause problems for use in the proposed transceiver shown in Fig. 2.2 due to the use of a bidirectional LNA/PA, such as that employed in [51], in each channel. The bidirectional LNA/PA works as a PA in the

Table 2.2

Measured performance summary of the *K/Ka*-band T/R/Calibration switch

Operation	Reception		Transmission		Calibration		Unit
Frequency	24.5	35	24.5	35	24.5	35	[GHz]
Insertion Loss (Noise Figure)	Ant. - Rx ports		Tx - Ant. ports		Cal. - Rx ports		
	9.4 (9.4)	9.1 (9.25)	9.2	4.9	12.3	12.3	[dB]
Isolation	Tx-Rx ports		Tx-Cal. ports		Tx-Rx ports		
	55	45	55	60	70	60	[dB]
	Cal.-Rx ports		Tx-Rx ports		Ant.-Rx ports		
	55	75	50	45	55	45	[dB]
Return Loss	Ant. port: >12.5		Tx port: >10		Cal. port: >10		[dB]
	Rx port: >9		Ant. port: >6		Rx port: >10		
IP1dB	5.6	5.4	11	10	4.2	3.9	[dBm]
IIP3	16.5	18.6	23.3	21.7	14.9	15.3	[dBm]

* Ant.: Antenna, Cal.: Calibration
* Rejection between 24.5 and 35 GHz in Reception and Calibration mode: >50 dB
* Out-of-band rejection: > 30dB compare to pass bands below 10.5 GHz and above 59.5 GHz
* Power consumption: 1.53 [mW]

Operation	Idle		Unit
Frequency	24.5	35	[GHz]
Isolation	Ant. - Cal. ports		[dB]
	55	55	
	Rx - Cal. ports		
	55	60	
	Ant. - Tx ports		
	35	35	
	Tx - Cal. ports		
	55	50	
	Ant. - Rx ports		
	60	45	
	Tx - Rx ports		
	65	65	

transmission mode and a LNA in the reception mode, enabling high-power and low-noise signals to be obtained in these respective modes. It is recognized that concurrent multi-band and multi-function RFICs are desired for achieving low-cost, compact and versatile RF systems and, as more functions and different bands are integrated together in a single circuit, some sacrifices in circuit performance may be inevitable. This is the price to pay for achieving more functional RFICs, which is considered reasonable in view of system implementation advantages with multi-function over multiple different frequency ranges for minimum size and cost using integrated circuits, particularly silicon-based RFICs. Besides, the system architecture could be altered to overcome

potential performance degradations of employed multi-band and multi-function RFICs such as the proposed transceiver with bidirectional amplifiers shown in Fig. 2.2.

2.2.6 Conclusion

This section has presented a novel concurrent dual-band T/R/Calibration switch module fully integrated on 0.18-μm BiCMOS with band-pass filtering and integrated calibration function for dual-band *K/Ka*-band array systems. A new approach utilizing the metamaterial CRLH TL was introduced in conjunction with a negative resistance to achieve a unique quasi-elliptic dual-bandpass response. The Q-enhancement technique via negative resistance coupled with the CRLH TL expands the possibility of exploiting unique dispersion characteristics of metamaterial structures in millimeter-wave integrated-circuit design. This approach also facilitates the reduction of a bulky off-chip filter, thereby fostering single-chip integration more conveniently. Furthermore, the proposed T/R/Calibration switch topology with the integrated calibration path enables an accurate transceiver array calibration and a stand-alone operation, which is expected to enhance the performance and operation of millimeter-wave array systems.

CHAPTER III

CONCURRENT DUAL-BAND LOW NOISE AMPLIFIERS

3.1. RF/Millimeter-wave Low Noise Amplifiers

The demand in millimeter-wave wireless systems is growing rapidly. The frequency use in the millimeter-wave spectrum is for various applications such as imaging, sensing, astronomy, industrial monitoring, and radars.

To meet the high demand in the millimeter-wave applications, the silicon-based semiconductor technology has evolved to enable high performance RF/millimeter-wave transceivers on chip. One of the most important circuits in RF/millimeter-wave front end is the LNA (Low Noise Amplifier) since it affects the system noise figure significantly and limits the sensitivity of the receiver system as well.

3.1.1 RF/Millimeter-wave Low Noise Amplifier Design Considerations

In this proposed and developed work, Jazz 0.18-μm SiGe BiCMOS technology [38] is used for fabrication. As a baseline approach in designing concurrent dual-band low noise amplifiers, the size of the BJTs and bias level were determined to achieve maximum possible gain and minimum noise figure. To that end, the tradeoff between MAG (Maximum Available Gain) and NF_{min} (Minimum Noise Figure) was considered for a common-emitter and cascode topology.

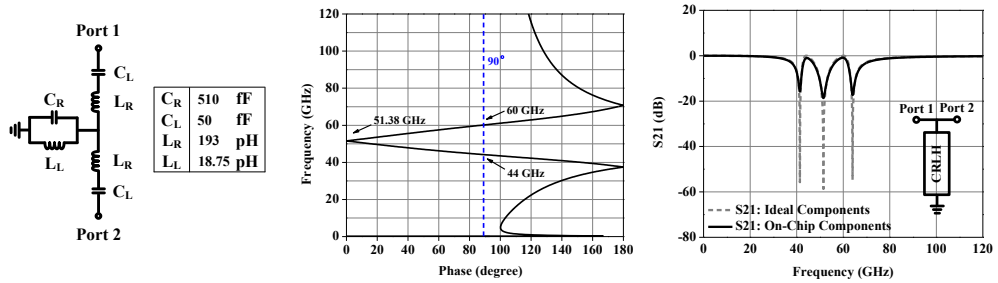
3.2. Concurrent Dual-band Low Noise Amplifiers

This section presents two concurrent dual-band low noise amplifiers (LNA) in *Q/V*- band. The developed LNAs are integrated with a Q-enhanced composite right/left-handed (CRLH) and an extended CRLH (hereafter, E-CRLH) metamaterial transmission line (TL) structures. Both the synthesized CRLH and E-CRLH are designed to exhibit quarter-wavelength transmission lines' properties at 44 and 60 GHz and are integrated with Colpitts negative resistance generation circuit to attain high Q frequency responses at their transition and stop-band frequencies, respectively, for rejection purposes. Both circuits are concurrent dual (44/60 GHz) - band amplifiers achieving maximum measured gain of 19.1 dB with minor gain imbalance of 0.2 dB or smaller between the two bands. The achieved 3-dB bandwidths are more than 6 GHz for each band of two LNAs with the lowest measured noise figure is 5.65 dB at the targeted frequency bands for all LNAs. The synthesized and Q-enhanced CRLH and E-CRLH TL proposed in this paper contributed a concurrent dual-band operation at 44/60 GHz showing a rejection of more than 30 dB between the two pass-bands. The IIP3 for each band are more than -14.1dBm at 44/60 GHz for all the LNAs. The demonstrated circuits are fabricated in 0.18-μm SiGe BiCMOS technology. The total power consumption of the proposed LNAs is 37.1mW.

3.2.1 Introduction and Motivation

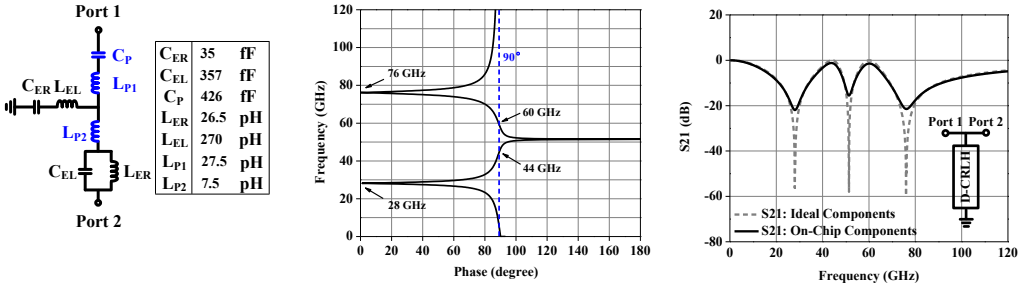
The interest in developing concurrent multi-band circuits has increased in recent days. In particular, the concurrent multi-band operation achieved electronically can contribute to enhance system diversity while reducing the system complexity for sensing and communication systems. In realizing multi-band circuits and systems, the CRLH metamaterial approach, both TL- and resonant- type, has been extensively adopted to exploit its unique dispersive characteristic for novel microwave component developments in recent years [52-54].

Furthermore, the metamaterial research has been extended to provide various fundamental forms of metamaterial structures with dual-, tri-, and quad- band characteristics [55-57]. However, many researches have been carried out in microwave regime for passive circuits, active hybrid circuits employing discrete components, and antennae design while a few are found in RF/millimeter-wave integrated circuit designs. In this section, two concurrent dual *Q/V*(44/60 GHz)- band LNAs that are integrated with the synthesized and Q-enhanced CRLH and E-CRLH are proposed and their performances are discussed. For the first dual-band LNA, the Q-enhanced CRLH is designed to exhibit quarter-wavelength at 44/60 GHz consecutively with Q-enhanced response at its transition frequency of CRLH at 51.38 GHz for an agile rejection response. The second dual-band LNA employs a synthesized and Q-enhanced E-CRLH which is designed to provide, again, quarter-wavelength at 44/60 GHz with Q-enhanced rejection at the stop band of E-CRLH at 51.31 GHz. In addition, the E-CRLH structure



(a) (b) (c)

Figure 3.1.(a) CRLH network (b) dispersion diagram of CRLH and (c) insertion loss with ideal and on-chip components



(a) (b) (c)

Figure 3.2.(a) E-CRLH network (b) dispersion diagram of E-CRLH and (c) insertion loss with ideal and on-chip components

includes parasitic components for 0° phase delay at the third order inter-modulation distortion frequencies of 28 and 76 GHz to provide additional transmission zero for better out-of-band rejection characteristic.

3.2.2 Concurrent Dual-band Low Noise Amplifier Design

The unique dispersion characteristics of the aforementioned CRLH and E-CRLH are exploited in realizing proposed concurrent dual-band LNAs at *Q*/*V*- band. The design

approaches and challenges in utilizing the proposed CRLH and modified E-CRLH are discussed which are followed by the concurrent dual-band LNA designs.

3.2.2.1 Q-enhanced Synthesized CRLH and E-CRLH

Both the synthesized CRLH and E-CRLH employed in this LNA development aims to retain quarter-wavelength at the two design frequencies of 44 and 60 GHz which are not harmonically related. The purpose in achieving quarter-wavelength consecutively at 44 and 60 GHz with the CRLH and E-CRLH network is to create open only at the design frequencies by shorting one end of the networks.

Fig. 3.1(a) shows the CRLH TL unit structure. The component values can be determined to have a quarter-wavelength at 44 and 60 GHz consecutively as appears in the dispersion diagram in Fig. 3.1(b). It can be also seen from Fig. 3.1(b) that the phase delay becomes 0° at the transition frequency of 51.38 GHz which appears between the left-handed and right-handed propagation region. The component values for the CRLH network in Fig. 3.1(a) can be obtained solving the equations provided below [52]

$$\beta^{CRLH} = \omega\sqrt{L_R C_R} - \frac{1}{\omega\sqrt{L_L C_L}} \tag{3.1}$$

$$Z^{CRLH} = \sqrt{\frac{L_R}{C_R}} = \sqrt{\frac{L_L}{C_L}} \tag{3.2}$$

where β^{CRLH} , C_L, L_R, and L_L specify the values for right-handed capacitance, left-handed capacitance, right-handed inductance, and left-handed inductance, respectively. Having

one end of the CRLH grounded the S21 response of the network exhibits open at 44 and 60 GHz and short at the transition frequency of 51.38 GHz as shown in Fig. 3.1 (c). The CRLH network returns three distinctive frequency points which are two design frequencies (f_1 and f_2) for specific phase delays and one transition frequency which is subject to the aforementioned two design frequencies determined by $\sqrt{f_1 f_2}$. However, as can be seen in the Fig. 3.1(c), the low quality factor of on-chip components (mostly that of spiral inductors) deteriorates frequency response making it difficult to utilize the CRLH for an intended filtering function.

Fig. 3.2(a) presents the modified E-CRLH network that is engineered to provide four distinctive frequency points. Based on the dual CRLH (D-CRLH) structure [55], a number of parasitic components, which are C_P, L_{P1}, and L_{P2}, are added to make it an E-CRLH structure which eventually becomes a quad-band component. The generalized extended composite right/left-handed metamaterial transmission line with a quad-band characteristic has been reported [57]. However, the proposed E-CRLH in Fig. 3.2(a) exhibits quad-band characteristic without the capacitance for right-handedness and the inductance for left-handedness in conventional CRLH portion within the phase delay range of $\pm 90°$ showing two left-handed, right-handed propagation region separated by two transition frequencies at 44 and 60 GHz. The delimited left-handed propagation at low frequency and right-handed propagation at high frequency by the absence of aforementioned capacitance for right-handedness and inductance for left-handedness in conventional CRLH portion does not impose any restrictions in designing the proposed phase delay in Fig. 3.2(b). The E-CRLH network shown in Fig. 3.2(a) is engineered to

provide quarter-wavelengths at 44 and 60 GHz consecutively and 0° phase shift at 28 and 76 GHz which are the third order intermodulation frequencies of 44 and 60 GHz. The series impedance and parallel admittance of the E-CRLH network shown in Fig. 3.2(a) can be expressed as below.

$$Z^{E-CRLH} = j\omega L_P(1-\omega_{CS}^2/\omega^2) - \frac{j}{\omega C_{EL}(1-\omega_{EP}^2/\omega^2)} \tag{3.3}$$

$$Y^{E-CRLH} = -\frac{j}{\omega L_{EL}(1-\omega_{ES}^2/\omega^2)} \tag{3.4}$$

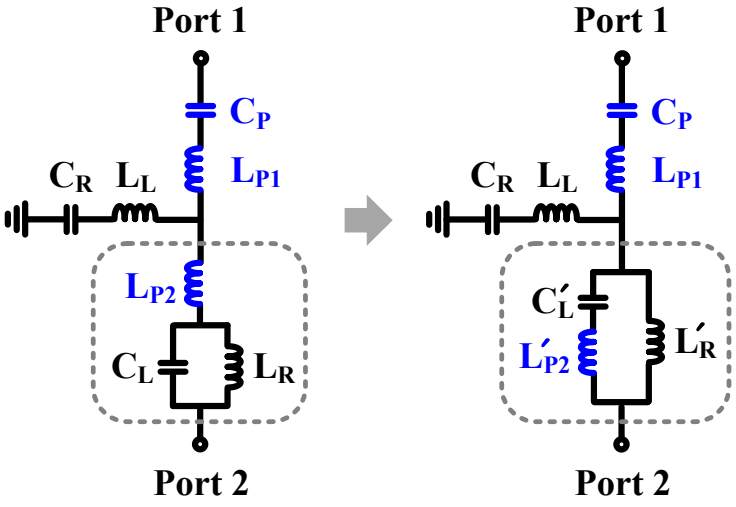
where L_P, $\omega_{CS,}$ $\omega_{EP,}$ and ω_{EP} mean (L_{P1}+L_{P2}), $1/\sqrt{L_P C_P}$, $1/\sqrt{L_{ER}C_{EL}}$, and $1/\sqrt{L_{EL}C_{ER}}$, respectively. The propagation constant can be equated with the expressions in (3.1-3.2).

$$\cos(\beta l) = 1 + Z^{E-CRLH}Y^{E-CRLH}/2 \tag{3.5}$$

where l is the physical unit length of the E-CRLH structure. Also, the characteristic impedance of the E-CRLH can be expressed as follow.

$$Z_0 = \frac{\sqrt{(ZY)^2 + ZY}}{Y} \tag{3.6}$$

where Z=$Z^{E\text{-}CRLH}$ and Y=$Y^{E\text{-}CRLH}$ shown in (3.3) and (3.4), respectively. The parameters for the intended phase delay (0°at 28/76 GHz and $\pm$ 90° at 44/60 GHz) can be found using (3.1)-(3.4) and enforcing the impedance condition of $\sqrt{L_{ER}C_{ER}} = \sqrt{L_{EL}C_{EL}}$ excluding the effect of parasitic. The dispersion diagram for this E-CRLH is shown in Fig. 3.2(b). Fig. 3.2(c) compares the frequency response of the proposed network with ideal

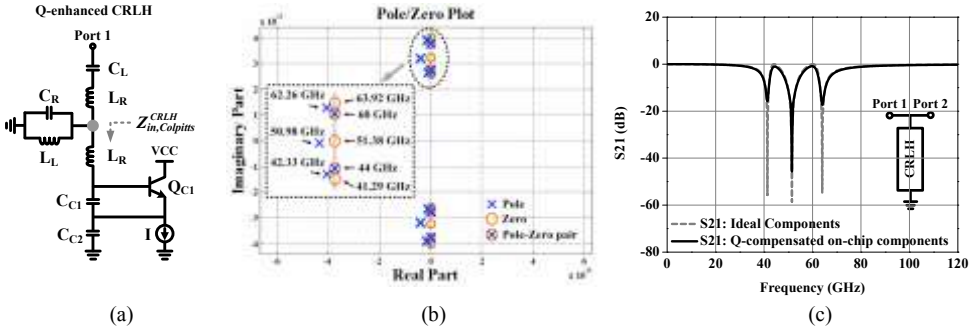


(a) (b)

Figure 3.3.Network transformation: (a) E-CRLH with parasitic components for additional transmission zeroes and (b) E-CRLH with transformed network

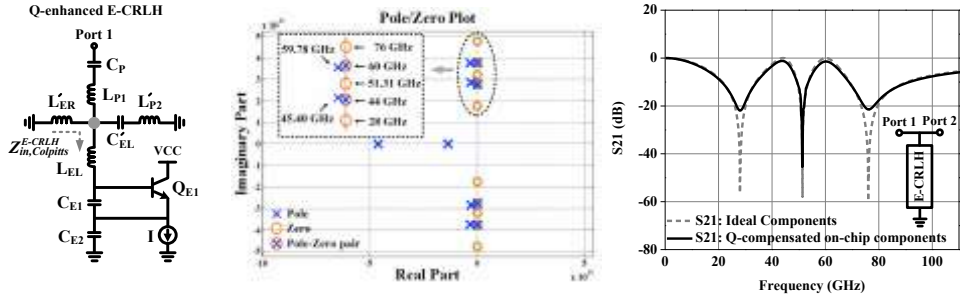
components and on-chip components having Port 2 in Fig. 3.2(a) grounded. Due to the quarter-wavelength at 44 and 60 GHz, no insertion loss is induced at those frequencies while rejection occurs at 28 and 76 GHz. The engineered E-CRLH network provides five distinctive frequency points that are four design frequencies for specific phase delays (two for $\pm$90 degree and the other two for zero degree phase shift) and one stop-band frequency which is subject to the aforementioned four design frequencies.

To facilitate a simpler layout, a part of E-CRLH shown in Fig. 3.2(a) is changed into its equivalent network. Fig. 3.3(a) shows the original E-CRLH with intended parasitic components and Fig. 3.3(b) presents the revised E-CRLH network which maintains the identical phase delay and phase response. The phase delay of this network



(a) (b) (c)

Figure 3.4.(a) active CRLH network (b) dispersion diagram of active CRLH and (c) insertion loss with ideal and on-chip components



(a) (b) (c)

Figure 3.5.(a) active E-CRLH network (b) dispersion diagram of active E-CRLH and (c) insertion loss with ideal and on-chip components

can be maintained as intended using the on-chip components, nevertheless, the frequency response cannot be retained as that of ideal components due to low-quality factor on-chip components.

To overcome the aforementioned low Q issue, the Colpitts style negative generation circuit is integrated with the CRLH and E-CRLH networks as shown in Fig. 3.1(a) and 3.2(a). The proposed active CRLH and E-CRLH structures are presented in Fig. 3.4(a) and 3.5(a), respectively. Referring to the dispersion diagram provided in Fig.

3.1(b) and Fig. 3.2(b), the negative resistance is inserted at the transition frequency of CRLH and stop-band frequency of E-CRLH which are $1/\sqrt{L_R C_L}$ and $1/\sqrt{L_{EL} C_{ER}}$, respectively.

The pole/zero analysis with the CRLH and E-CRLH networks are shown in Fig. 3.4(b) and Fig. 3.5(b) are carried out for more insights. The analysis is performed with two-port configuration as shown in Fig. 3.4(c) and 3.5(c). First with the CRLH network, it can be seen the overlapped pole/zero appears at 44 and 60 GHz on the $j\omega$ axis showing all-pass characteristic at those frequencies. The zero at the transition frequency of 51.38 GHz indicates a rejection. In the vicinity of the transmission zero at the transition frequency, the critical pole resides at 50.98 GHz near $j\omega$ axis.

With the E-CRLH network, the overlapped pole/zero can be observed at 44 and 60 GHz on the $j\omega$ axis due to the intended dispersion as presented in Fig. 3.2(b) resulting in all-pass characteristics at these frequencies. The transmission zero exists at the inherent stop-band frequency of 51.31 GHz caused by the E-CRLH structure provides a rejection between the two interest bands. The transmission zeroes at 28 and 76 GHz are achieved by the added parasitic components such as C_P, L_{P1}, and L_{P2}. These transmission zeroes create rejection at those frequencies as shown in Fig. 3.5(c). With this network as well, critical poles are observed at 45.4 and 59.78 GHz near the $j\omega$ axis also close to the transmission zero at the stop-band frequency of 51.31 GHz where a negative resistance will be added.

The critical poles at 50.98 GHz and 45.4/59.78 GHz with CRLH and E-CRLH networks, respectively, draw a particular attention since those poles can be

overcompensated by the negative resistance added at the transmission zeros at 51.38 GHz and 51.31 GHz of CRLH and E-CRLH network. The overcompensation would compel them to move closer to the $j\omega$ axis finally resulting in marginally stable or potential oscillation state. From the proposed Q-enhanced CRLH and E-CRLH structures in Fig. 3.4(a) and Fig. 3.5(a), the input impedances at the designated node in the figure can be expressed as below.

$$Z_{IN,Colpitts}^{CRLH} = (R_{L_R} + j\omega L_R) + \frac{1}{j\omega}\left(\frac{1}{C_{C1}} + \frac{1}{C_{C2}}\right) - \frac{g_m}{\omega^2 C_{C1} C_{C2}} \tag{3.7}$$

$$Z_{IN,Colpitts}^{E-CRLH} = (R_{L_{ER}} + j\omega L_{ER}) + \frac{1}{j\omega}\left(\frac{1}{C_{E1}} + \frac{1}{C_{E2}}\right) - \frac{g_m}{\omega^2 C_{E1} C_{E2}} \tag{3.8}$$

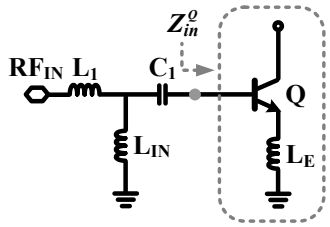
where R_{L_R} and $R_{L_{ER}}$ are the resistance in the inductor L_R and L_{ER}, respectively, and g_m is the transconductance of BJTs in the Colpitts style negative generation circuit. And C_{C1}/C_{C2} and C_{E1}/C_{E2} are the capacitance in the Colpitts negative generation circuits for Q-enhanced CRLH and E-CRLH networks, respectively. To articulate the intended Q-enhancement and associated stability condition in a straightforward manner, only the input impedance at the designated node are discussed. As can be seen from (3.7) and (3.8), the negative resistance generated by the integrated Colpitts style negative resistance generation circuit, effectively cancels out the resistance of the inductors L_R and L_{ER} (of which resistances are dominant in contributing loss) enhancing the Q at the transition and stop-band frequencies of CRLH and E-CRLH networks, respectively. From (3.7) and (3.8), it can be seen that the intended dispersion can be achieved with having the following conditions fulfilled as well.

$$C_L = \frac{C_{C1}C_{C2}}{C_{C1}+C_{C2}}, \quad C_{ER} = \frac{C_{E1}C_{E2}}{C_{E1}+C_{E2}} \tag{3.9}$$

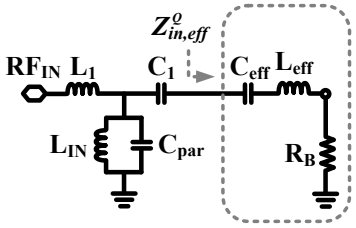
where C_L and C_{ER} are the capacitances in the original CRLH and E-CRLH networks shown in Fig. 3.1(a) and 3.2(a), respectively. The capacitances C_{C1}, C_{C2}, C_{E1}, and C_{E2} are the capacitances in the Colpitts style negative generation circuits shown in Fig. 3.4(a) and 3.5(a). As described before, the critical poles adjacent to the $j\omega$ axis on the pole/zero map may cause a marginally stable condition in case they are overcompensated. It becomes obvious the transconductance g_m determines a negative resistance to cancel out the resistance in the proposed network. The marginal stability condition can be derived by introducing the additional resistance present in the proposed Q-enhanced CRLH and E-CRLH networks and also in the amplifier which will be integrated later. Equating the negative resistance generated by the Colpitts style negative generation circuit to the total resistance introduced externally:

$$\frac{g_m^{OSC}}{\omega^2 C_1 C_2} = R_L + R_{ext} \tag{3.10}$$

where g_m^{OSC} and R_{ext} represent the marginal transconductance for oscillation and the total resistance introduced externally. The capacitance C_1 and C_2 represent C_{C1}/C_{E1} and C_{C2}/C_{E2}, respectively, and R_L represents both R_{L_R} and $R_{L_{ER}}$. The optimum negative resistance sufficient enough to create rejections at the transmission zeroes can be written as



(a)



(b)

Figure 3.6.Wideband input matching for concurrent dual-band LNAs: (a) original circuit configuration and (b) its equivalent circuit model

$$\frac{g_m^{opt}}{\omega^2 C_1 C_2} = R_L \tag{3.11}$$

where g_m^{opt} represents the optimal transconductance for creating the best rejection without oscillation. The ratio between (3.10) and (3.11) results in the stability margin as below.

$$I_{OSC} = I_{opt}(1 + \frac{R_{ext}}{R_L}) \tag{3.12}$$

where I_{osc} and I_{opt} mean the currents for oscillation and optimum Q-enhancement, respectively. The equation in (3.12) shows the current for oscillation is always larger

than the current for optimum Q-enhancement due to the external resistance, which ensures stable performance of the proposed active CRLH and E-CRLH networks.

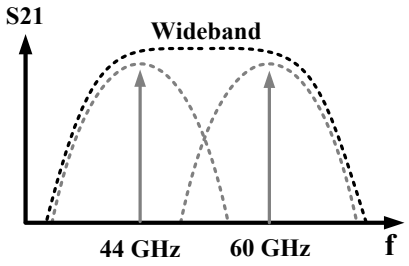
3.2.2.2 Wideband Input Matching

In developing the proposed concurrent dual-band LNAs, a wideband input matching technique is employed. While concurrent dual-band impedance matching at 44 and 60 GHz is possible, it is realized by employing more inductors and capacitors in comparison of wideband input matching, which would cause more loss thereby increasing the noise figure of the LNA.

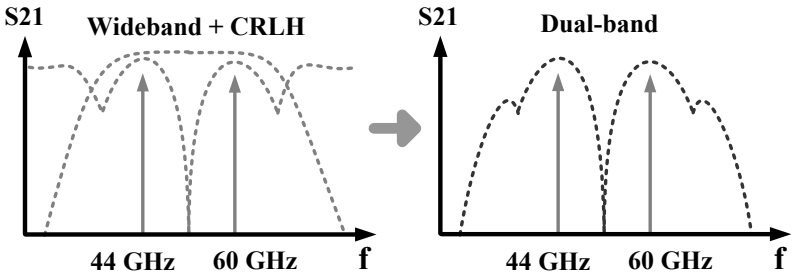
The developed LNAs utilize an emitter degenerated common emitter as a LNA driver of which equivalent circuit contributes wideband input matching with a simple input matching network. Fig. 3.6(a) shows the inductively degenerated transistor and the wideband input matching network for the proposed concurrent dual-band LNAs. The input impedance of inductor degenerated transistor can be expressed as follow:

$$Z_{in}^{Q} = r_b + \frac{g_m L_e}{C_\pi} + j\omega L_e + \frac{1}{j\omega C_\pi} \tag{3.13}$$

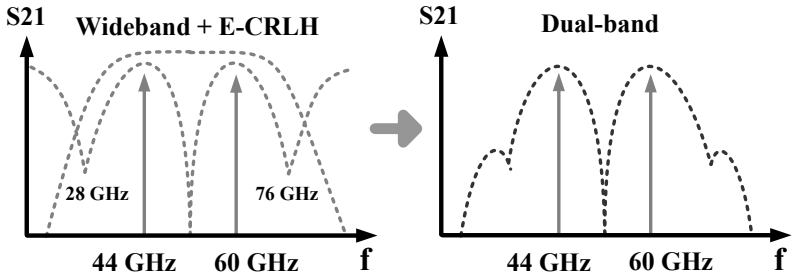
where r_b and C_π are the base resistance and base-emitter capacitance, respectively. As can be seen from (3.13), the primary purpose of the inductor degeneration is to cancel the effect of base-emitter capacitance which eventually makes the input impedance of the transistor real. In real design, the base-emitter capacitance is subject to the selection



(a)



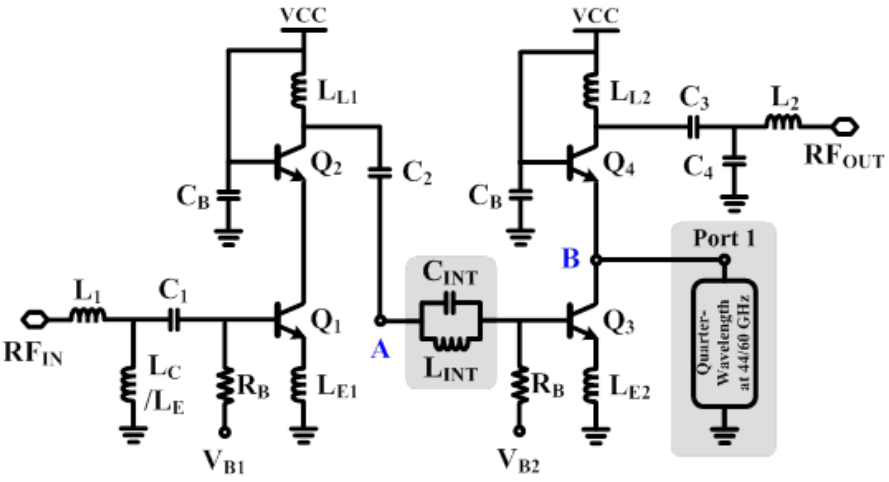
(b)



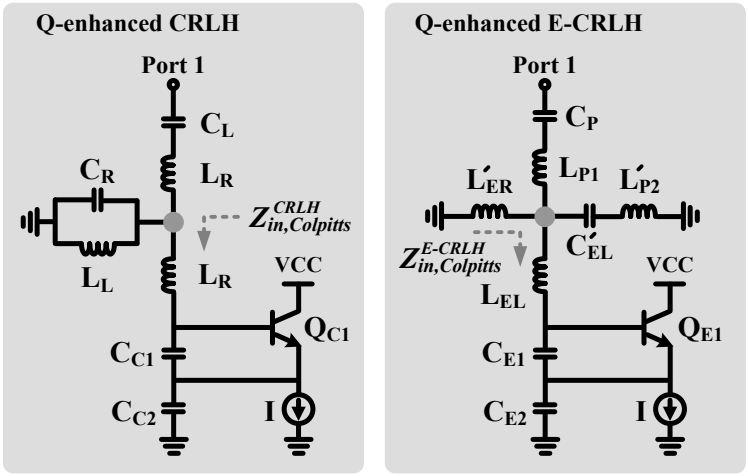
(c)

Figure 3.7.Concurrent dual-band LNAs realization: (a) Wideband S21 response with two stages, (b) Wideband and CRLH superposition, and (c) Wideband and E-CRLH superposition

of device size which is mostly chosen for low noise performance with minimum power consumption. This enforces the selection of degeneration inductor to be limited in



(a)



(b) (c)

Figure 3.8.(a) Concurrent dual-band two-stage LNA schematic, (b) Q-enhanced CRLH, and (c) Q-enhanced E-CRLH

realizing 50 Ohm input impedance. However, the degeneration inductor also affects the gain of the amplifier by lowering the g_m of the input amplifier stage, which also

improves the stability. In the proposed concurrent dual-band LNAs, the input impedance of inductor degenerated input amplifier stage is incorporated as part of bandpass filter network to accommodate wide input impedance matching. The equivalent circuit model of the aforementioned circuit in Fig. 3.6(a) appears in Fig. 3.6(b).

3.2.2.3 Two Stage Concurrent Dual-band Low Noise Amplifiers

Two-stage inductor degenerated cascode amplifiers are employed in realizing the proposed concurrent dual-band LNAs. The conceptual illustration depicting the approaches is shown in Fig. 3.7. As shown in Fig. 3.7(a), cascode stages tuned at 44 and 60 GHz are cascaded to provide a wideband S21 response. The aforementioned active Q-enhanced CRLH network is integrated with the wideband amplifier stages to finally produce a concurrent dual-band frequency response in Fig. 3.7(b). The other concurrent dual-band LNA adopts the synthesized E-CRLH with a wideband two-stage amplifier to generate the concurrent dual-band response shown in Fig. 3.7(c). It should be noted that in the latter approach, there exist two additional transmission zeros at the third order IMD frequencies of 44 and 66 GHz. The proposed concurrent dual-band LNAs are shown in Fig. 3.8(a) and the active CRLH and E-CRLH networks are present in Fig. 3.8(b) and (c).

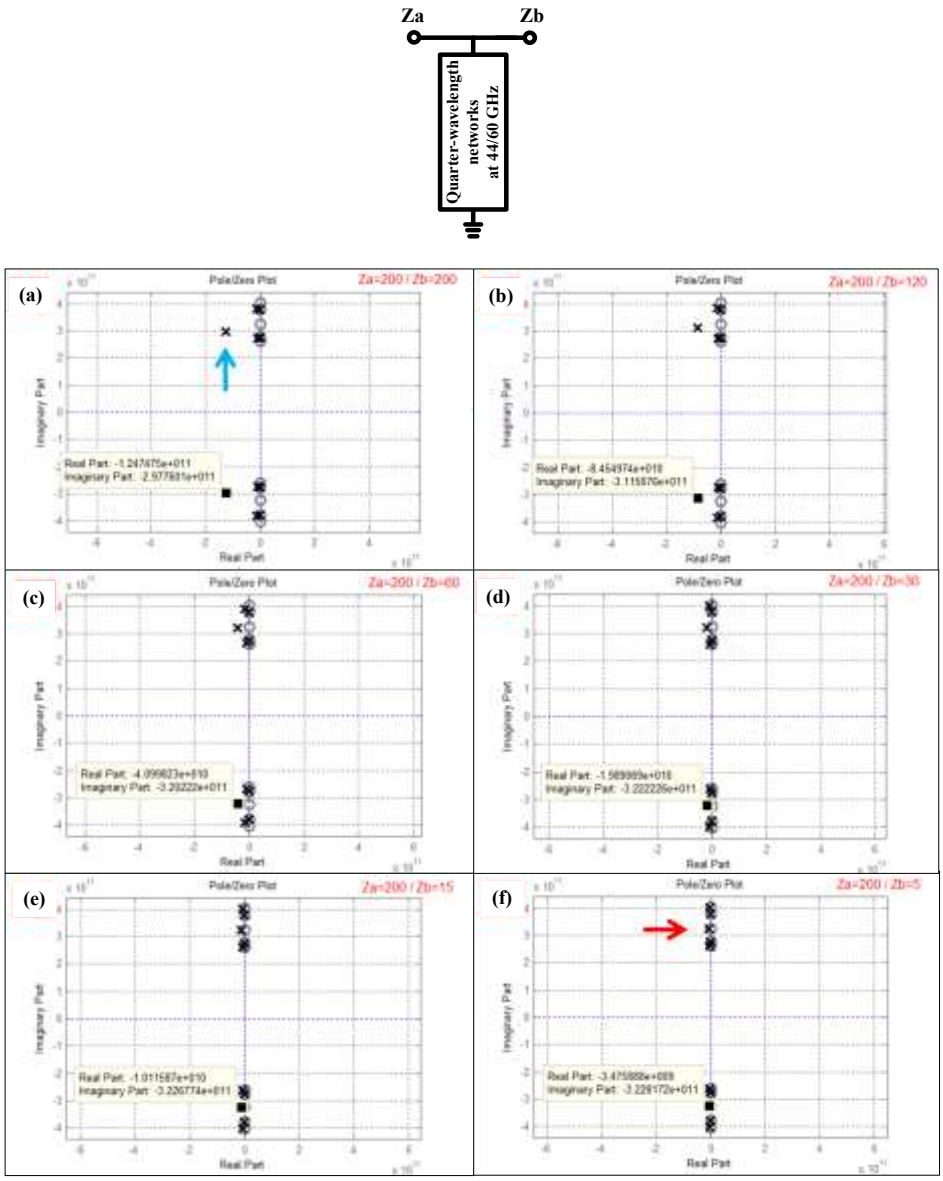
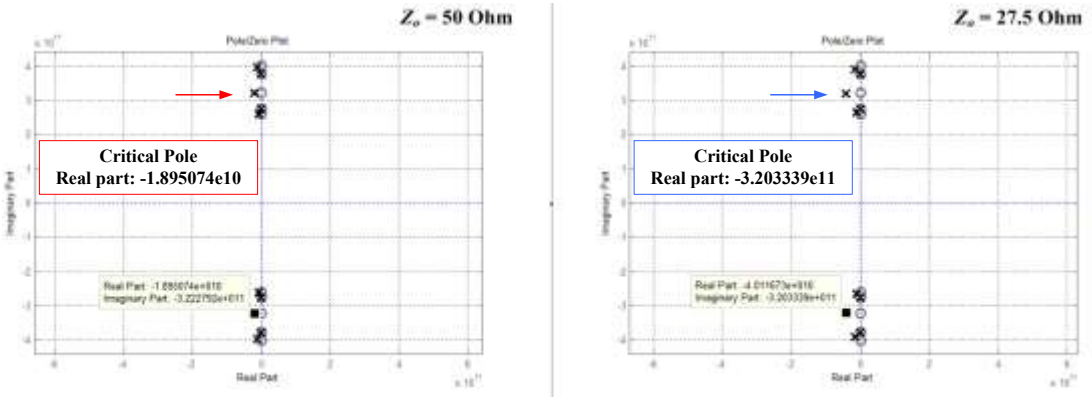


Figure 3.9.Pole migration with different impedance condition

The aforementioned active CRLH and E-CRLH networks are completely integrated with the second stage amplifiers for both designs. It was integrated with the second stage of the amplifier, rather than the first stage, to minimize the increase in the



(a) (b)

Figure 3.10.Pole migration with fixed outside impedance (a) Quarter-wavelength network with characteristic impedance of 50 Ohm and (b) Quarter-wavelength network with characteristic impedance of 27.5 Ohm

noise figure. The active CRLH and E-CRLH are connected between the main amplifying common emitter transistor and cascode transistor.

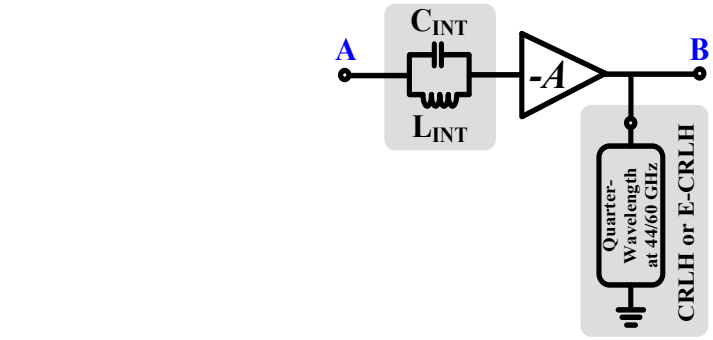
There exist critical poles adjacent to the transmission zeroes at the transition and stop-band frequency of CRLH and E-CRLH networks, respectively. The stability condition in regards of using negative resistance was also discussed to derive the stability margin. However, the impedance condition looking into the collector of the main transistor and the emitter of the cascade transistor affect the critical pole as well.

Figure 3.9 provides the migration of critical pole depending on the outside impedances which emulate impedance looking at the collector of lower transistor and the emitter of upper transistor. It can be seen from Fig. 3.9(a) to 3.9(f) that the critical pole migrates closer to the $j\omega$ axis more closer having one impedance becomes smaller

showing a possible instability. This pole/zero analysis carried out with different outside impedances provide an important insight that even before the Q compensation, due to the inherent impedance condition in cascode structure attracts the critical pole more closer the $j\omega$ axis which can be easily over-compensated. And the impedance conditions in the cascode structure are out of control in designing amplifiers using the structure.

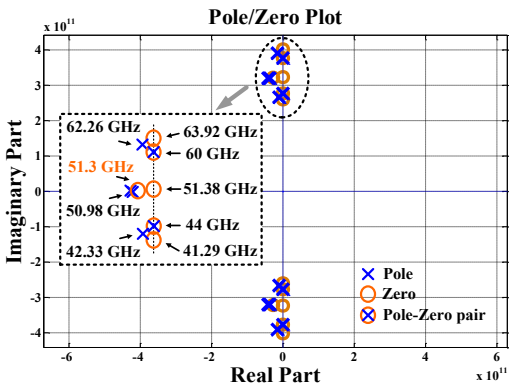
However, it can be observed from the same pole/zero analysis in Fig. 3.9, that the critical pole migrates farther into the left-half plane of the pole/zero map showing more stable condition of the system. A relative interpretation of this phenomenon provides one more important insight that the quarter-wavelengths network designed with smaller characteristic impedance would push the critical pole farther into the left-half plane of the pole/zero map for more stable condition of the system. The experiment carried out in Fig. 3.10 proves that, given the fixed outside impedances, the critical pole moves away from $j\omega$ axis with the smaller characteristic impedance quarter-wavelength network. Fig. 3.10(a) and 3.10(b) provide the pole/zero maps with 50 Ohm and 27.5 Ohm characteristic impedance quarter-wavelength network. Comparing the real part which represents the resistance portion of the poles (1.89×10^{10} and 4.01×10^{10} for the 50 and 27.5 characteristic impedance quarter-wavelength networks, respectively) suggest that there would be an attenuation of 7 dB in terms of voltage gain. In the following designs, the quarter-wavelength networks with the characteristic impedance of 27.5 Ohm are used to provide a more stable operation of the amplifier based on this experiment.

Along with the tight control of the current in generating g_m associated with the negative resistance for Q enhancement, an additional transmission zero around the

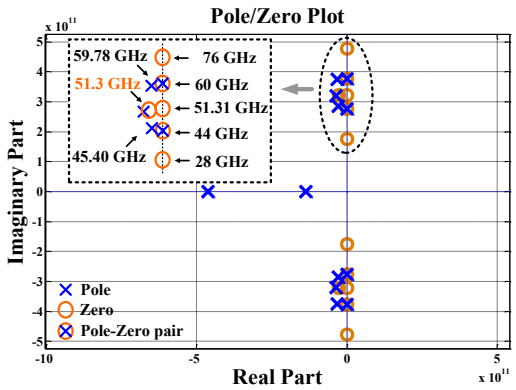


Equivalent circuit model between node A and B

(a)



(b)



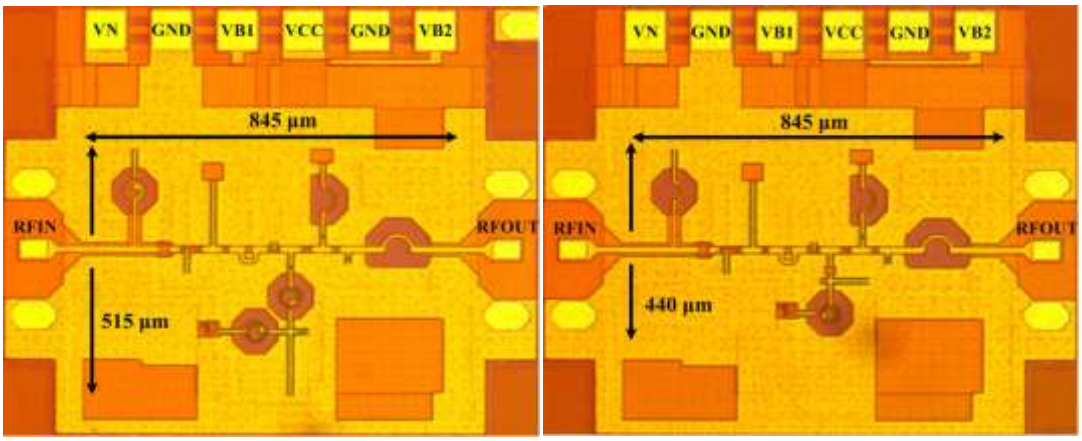
(c)

Figure 3.11.(a) Equivalent circuit model for a network from node A to B in the concurrent dual-band LNA schematic for pole/zero analysis, (b) Q-enhanced CRLH, and (c) Q-enhanced E-CRLH

critical pole can enhance the stability. To neutralize the effect of the critical poles which would possibly cause marginal stability condition, a transmission zero centered at the transition and stop-band frequency is introduced at the inter stage by parallel inductor L_{INT} and capacitor C_{INT} resonant tank as shown in Fig. 3.8(a).

Fig. 3.11(a) shows the equivalent network of the inter stage, main amplifier of the second stage and the Q enhanced CRLH network. The nodes for the pole/zero analysis are denoted by node A and B in Fig. 3.8 (a).The parallel resonant network at the inter stage provides a pair of pole and zero. The pole/zero plot of the equivalent network of the second stage of dual-band LNA including the inter-stage L_{INT}/C_{INT} network, amplifier, and the Q-enhanced CRLH in Fig. 3.11(a) is shown in Fig. 3.11(b). It can be observed from the plot that additional pole and zero caused by the inter-stage network appear along with all the poles and zeros of the CRLH network as shown in Fig. 3.4(b). The transmission zero centered at 51.3 GHz provided by the parallel L_{INT}/C_{INT} network at the inter stage is placed adjacent to the critical pole at 50.98 GHz which resides in the CRLH network. The inter-stage matching network provides a zero-pole cancellation with the additional transmission zero which would help prevent the amplifier from entering a marginally stable condition. Based on simulation, the inter-stage resonant tank with the Q factor of around 10.5 suppressed the gain at the critical pole frequency (50.98 GHz) by around 6.5 dB. Also, the negative resistance in the CRLH network will not compensate the pole provided by the inter-stage network since it is in the preceding stage of the main amplifying transistor of the second stage.

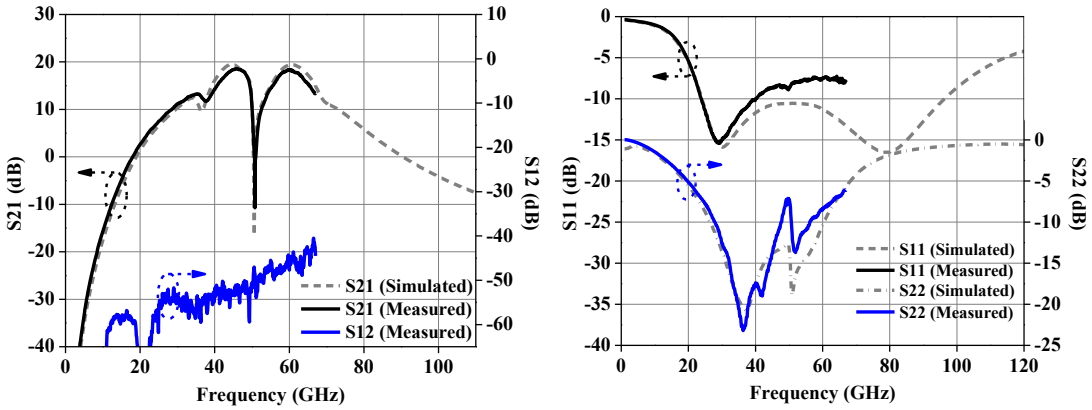
Fig. 3.11(c) presents the pole/zero plot of equivalent network of inter-stage matching, main amplifier of the second stage and the Q enhanced E-CRLH network. Along with the poles and zeros present in the E-CRLH network shown in Fig. 3.5(b), the additional pair of pole and zero provided by the inter stage parallel L_{INT}/C_{INT} appear on the pole/zero plot of the Fig. 3.11(c). The additional transmission zero is located at 51.3



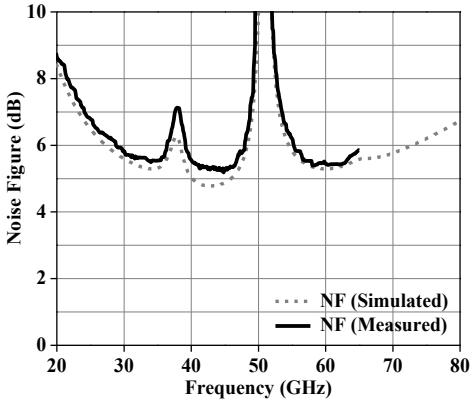
(a) (b)

Figure 3.12.Die photos (a) Concurrent dual-band LNA with Q-enhanced CRLH (b) Concurrent dual-band LNA with Q-enhanced E-CRLH

GHz, again, help neutralizing the effect of critical poles at 45.5 GHz and 59.78 GHz in case of an over compensation of critical poles by the negative resistance added at the transmission zero frequency of 51.31 GHz in the E-CRLH network. Again, the additional pole provided by this inter-stage network would not affect the stability of the amplifier since it is not compensated by the negative resistance which is present after the amplifier. For both concurrent dual-band LNAs using Q–enhanced CRLH and E-CRLH, it can be intuitively understood the amplifier gain is reduced centered around 51.38 GHz and 51.31 GHz, which are respectively at the transition and stop-band frequency, by the transmission zero in the inter-stage network. The pole/zero analysis carried out with the equivalent network provides more insight that the transmission zero in the inter-stage network neutralizes the effect of critical poles present in the CRLH and E-CRLH networks.



(a) (b)



(c)

Figure 3.13.Concurrent dual-band LNA with the Q-enhanced CRLH (a) S21 and S12, (b) S11 and S22, and (c) noise figure

3.2.3 Concurrent Dual-band Low Noise Amplifiers: Performance

The measured results for both concurrent dual-band LNAs employing Q-enhanced CRLH and E-CRLH are presented in this section. The proposed circuits are

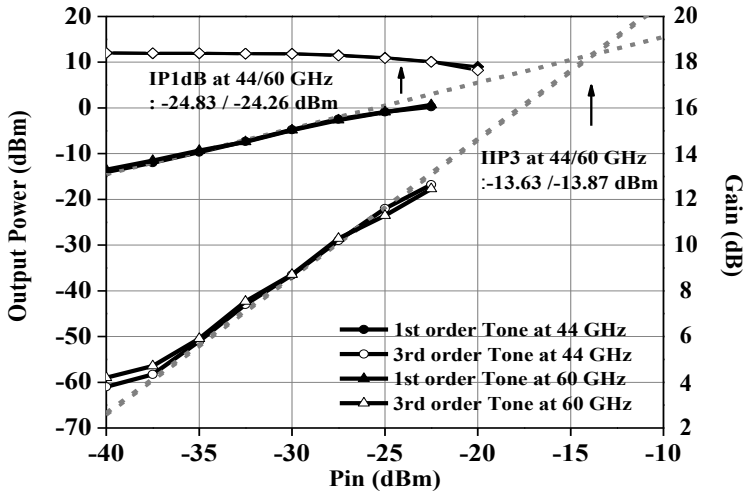


Figure 3.14.Linearity performance: Concurrent dual-band LNA with the Q-enhanced CRLH

fabricated on Jazz's 0.18-μm SiGe BiCMOS process [58]. The coplanar waveguide (CPW) and grounded coplanar waveguide (GCPW) structures were utilized in realizing the proposed LNAs. Fig. 3.12(a) and (b) shows the fabricated LNAs and their core size. The core sizes of the LNAs were 845 by 515 μm^2 and 845 by 440 μm^2, respectively, excluding DC and RF pads.

3.2.3.1 Concurrent Dual-band LNA with Q-enhanced CRLH

The measured S-parameter results and noise figure (NF) performance for the proposed dual-band LNA with Q-enhanced CRLH are shown in Fig. 3.13(a-c). Preserving the intended dual-band frequency response, the maximum gain at 24.5 and 35

GHz reached as high as 18.9 and 18.72 dB, respectively. The measured 3-dB bandwidth for each band is 8.2 GHz (from 41.1 to 49.3 GHz) and 9.3 GHz (from 55.8 to 65.1 GHz), respectively. The gain difference between the two bands remains less than 0.2 dB showing a great gain balance for a concurrent dual-band operation. The rejection between the two interested bands, which appears at the transition frequency of the CRLH structure, shows 32 dB difference compared to the pass-band maximum gain. The reverse isolation of the LNA remains more than 40 dB up to 67 GHz. The S21 and S12 performance are all presented in Fig. 3.13(a). The return loss at the input and output remains more than 10/10 and 10/8 dB at 44/60 GHz, respectively, as shown in Fig. 3.13(b). Fig. 3.13(c) presents the measured NF which exhibits the best NF of 5.65 and 5.76 dB at the first and second band, respectively.

The power handling capability of the proposed LNA appears in Fig. 3.14. The achieved IP1dB and IIP3 performance were -24.8/-24.3 dBm and -13.6/-13.9 dBm at 24.5 and 35 GHz, respectively. The LNA draws 20.6 mA current out of 1.8 V DC power supply.

3.2.3.2 Concurrent Dual-band LNA with Q-enhanced E-CRLH

The measured S-parameter and NF performance for the proposed dual-band LNA with Q-enhanced E-CRLH are presented in Fig. 3.15(a-c). The peak gain of 19.1 and 18.93 dB is achieved at 44 and 60 GHz bands, respectively, showing an identical peak gain. The measured 3-dB bandwidth for each band is 6 GHz (from 42.1 to 48.1 GHz)

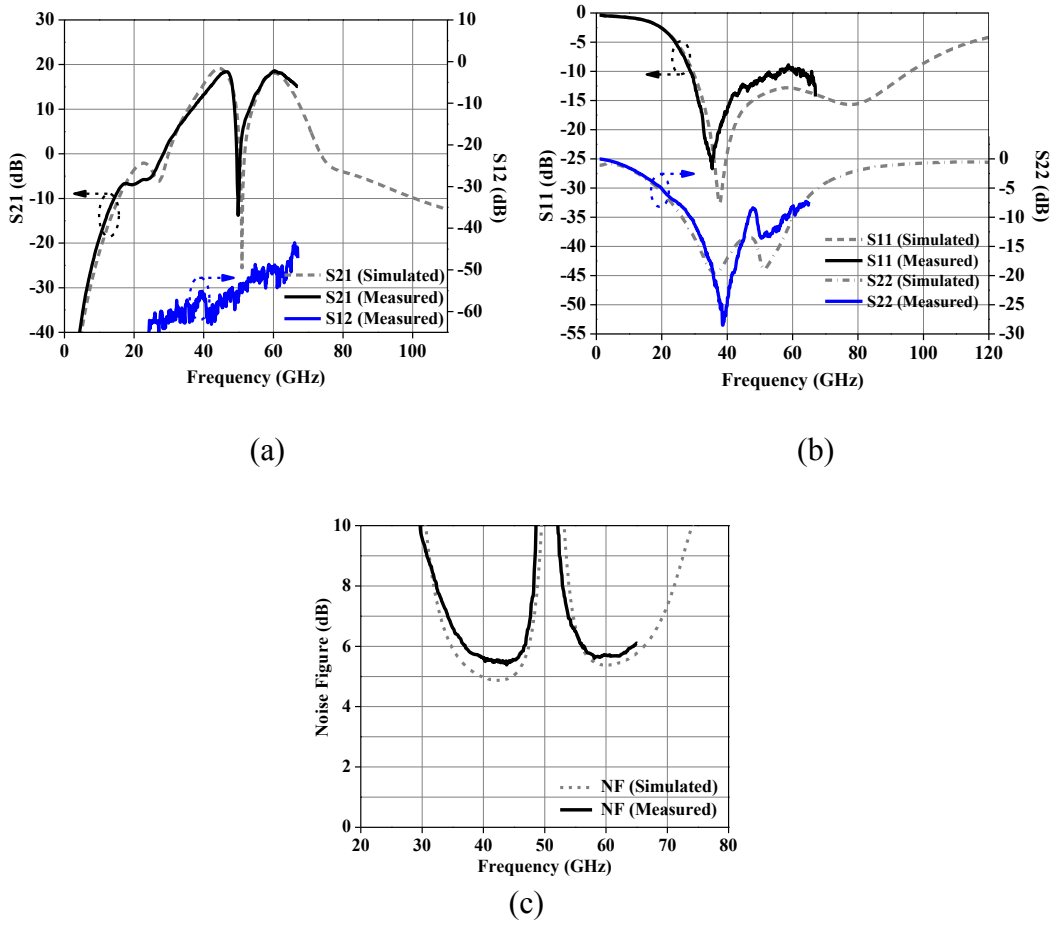


Figure 3.15.Concurrent dual-band LNA with the Q-enhanced E-CRLH (a) S21 and S12, (b) S11 and S22, and (c) noise figure

and 9.6 GHz (from 56.5 to 66.1 GHz), respectively. The rejection ratio between the two pass bands and the stop band at the bandgap frequency of 51.31 GHz is as high as 33 dB. The rejection ratio between the pass-band frequencies and IMD3 frequency of 28 GHz is more than 23 dB. The extrapolated gain shape above 67 GHs can confirm the rejection ratio between the pass-band frequencies and the other IMD3 frequency of 76 GHz can also be more than 20 dB. The intended transmission zeroes at 28 and 76 GHz directly

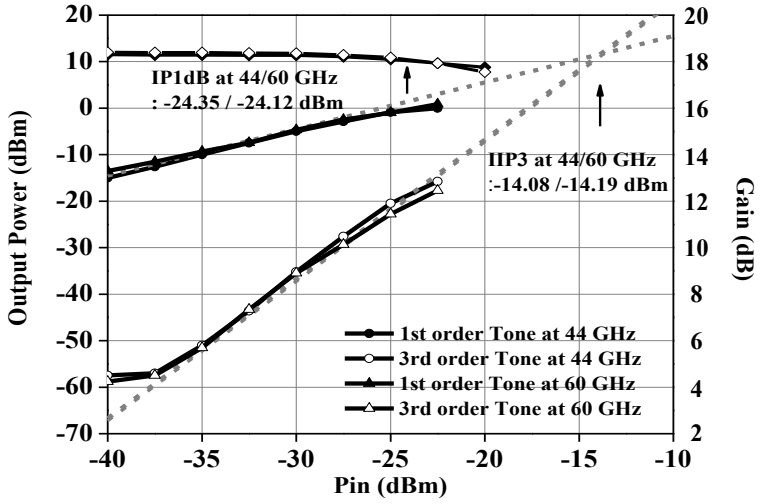


Figure 3.16.Linearity performance: Concurrent dual-band LNA with the Q-enhanced E-CRLH

suppress unwanted gains more than 20 dB below 28 and above 76 GHz. The reverse isolation remains more than 40 dB up to 67 GHz as well. The return loss at the input and output was 10/10 and 10/8 dB at 44/60 GHz, respectively, as shown in Fig. 3.15(b). The lowest measured NF at each band is 5.72 and 5.8 dB, respectively as shown in Fig. 3.15(c).

The linearity performance in terms of IP1dB and IIP3 is presented in Fig. 3.16(b). The measured IP1dB and IIP3 were -24.4/-24.1 dBm and -14/-14.2 dBm at 24.5 and 35 GHz, respectively. This LNA also consumed 20.5 mA current out of 1.8 V DC power supply.

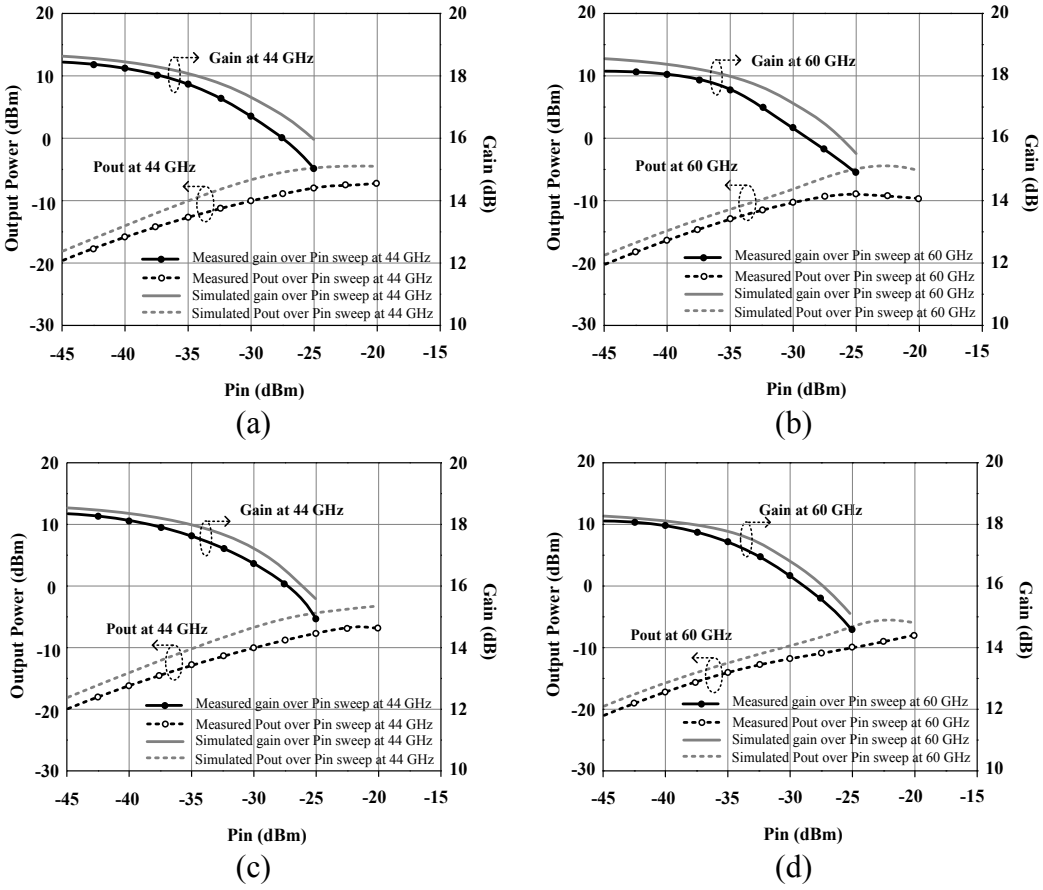


Figure 3.17. Dual-mode linearity performance: (a) linearity at 44 GHz in dual-mode LNA with Q-enhanced CRLH network, (b) linearity at 60 GHz in dual-mode LNA with Q-enhanced CRLH network, (c) linearity at 44 GHz in dual-mode LNA with Q-enhanced E-CRLH network, and (d) linearity at 60 GHz in dual-mode LNA with Q-enhanced E-CRLH network

3.2.3.3 Dual-mode Operation Linearity Performance of Proposed Low Noise Amplifiers

Fig. 3.17. presents the linearity performance when the low noise amplifiers operate in dual-mode. In this mode of operation, two tones at 44 and 60 GHz are applied

Table 3.1

Performance comparison for dual-band low noise amplifiers

Reference	Frequency (GHz)	Technology	Gain (dB)	NF (dB)	IIP3 (dBm)	Pass-band Gain Imbalance (dB)	Rejection Ratio (dB)	Power (mW)	Area (mm^2)
[59]	10/24	0.13 µm CMOS	25.3/12.1	5.3/10.4	N/A	13.2	44	12	1.14
[60]	2.3/4.5	0.35 µm SiGe BiCMOS	14.4/14.3	2.5/3.0	N/A	0.1	26	11.9	0.29
[61]	2.4/5.7	0.18 µm CMOS	7.6/8.6	5.7/6.8	-1.5/-2.4	1	30	10.8	1.15
[62]	17/24	0.18 µm CMOS	9.2/12	5.7/6.4	-2/-3	2.8	9	8	0.33
This work w/ CRLH	**44/60**	**0.18 µm SiGe BiCMOS**	**18.9/18.72**	**5.65/5.76**	**-13.6/-13.9**	**0.2**	**32**	**37.08**	**0.435**
This work w/ E-CRLH	**44/60**	**0.18 µm SiGe BiCMOS**	**19.1/18.93**	**5.72/5.8**	**-14/-14.2**	**0.17**	**30**	**36.9**	**0.372**

at the same time to investigate the linearity performance. For this dual-mode linearity experiment, input powers are applied both at 44 and 60 GHz and swept together. The linearity performance in Section 2.3.1 and 2.3.2 were measured in a single-mode of operation.

Fig. 3.17(a) and (b) shows the dual-mode gain and Pout saturation at 44 GHz and 60 GHz, respectively, when two tones at 44 and 60 GHz are applied for the dual-band LNA with Q-enhanced CRLH network. From the measured result in Fig. 3.17(a), the P1dB reached -32 dBm at 44 GHz, which is lower than that of single-band mode P1dB at 44 GHz by 7.17 dBm. The P1dB is -34.2 dBm at 60 GHz, which is lower than that of single-band mode P1dB at 60 GHz by 9.94 dBm. Fig. 3.17(c) and (d) presents the dual-mode gain and Pout at 44 GHz and 60 GHz, respectively, for the LNA with Q-enhanced E-CRLH network. As shown in Fig. 3.17(c), the dual-mode P1dB at 44 GHz is -33.5

dBm, which is lowered than the single-mode P1dB at 44 GHz by 9.15 dBm. Finally, Fig. 3.17(d) presents the dual-mode P1dB at 60 GHz for the LNA with Q-enhanced E-CRLH network. The measured P1dB reaches -31.7 dBm, which is lower than that of single-mode by 7.58 dBm.

3.2.3.4 Comparison with Other Works

Table 3.1 compares the performance of the proposed concurrent dual-band low noise amplifiers with other published works [59-62]. While there are only a few concurrent dual-band millimeter-wave LNAs, the developed LNAs provide one of the best performances among the reported dual-band LNAs in terms of noise figure, gain, gain balance between the two pass bands, and rejection ratio. The achievement is particularly attractive given the small frequency ratio of 1.36. The proposed approaches in this section are applicable to other design frequencies with small ratio which would require Q-enhanced dual bandpass frequency response.

3.2.4 Conclusion

Two novel concurrent dual-band LNAs integrated with Q-enhanced CRLH and E-CRLH are proposed. The modified CRLH and E-CRLH structures synthesized to exhibit dual-band open at 44 and 60 GHz provide Q-enhanced frequency response at their transition and band-stop frequencies. The synthesized dual-band structures are

completely integrated with two-stage LNAs showing unprecedented dual-band frequency responses making the proposed LNAs work at two closely spaced pass-bands at 44 and 60 GHz. While the conventional CRLH transmission line approach has been extensively employed in microwave regime for more than a decade, the newly proposed synthesized and Q-enhanced CRLH and E-CRLH in *Q/V*- band are expected to contribute to provide a unique yet effective solution in designing multi-band components in millimeter-wave frequency range.

CHAPTER IV

CONCURRENT DUAL-BAND POWER AMPLIFIER

4.1 Power Amplifier Principles

In this chapter, the basic principles of power amplifier design will be discussed in terms of the power capability, power amplifier efficiency, and power amplifier linearity. The discussion on different classes of power amplifier will be followed. The challenges in designing power amplifiers with high efficiency and high output power in fully integrated circuits will be overviewed. The technical motivation in designing concurrent dual-band power amplifier will be presented which will be followed by a novel concurrent dual *Q*/*V*- band power amplifier design.

4.1.1 Power Capability

The primary function of power amplifiers is to deliver a high output power to its load. In a simplest assumption, the maximum power transfer is achieved at the design frequency with a given power supply voltage and matched load. The typical setup in discussing the power capability of a power amplifier is under a matched input and output condition with a fixed power supply voltage and impedance. The harmonic frequencies generated in power amplifiers due to their nonlinearity characteristic are assumed to be

completely filtered out. Then the maximum output power delivered to a load can be expressed as follows

$$P = \frac{V_{cc}^2}{2R} \tag{4.1}$$

where V_{CC} and R is the power supply voltage and load resistance, respectively.

4.1.2 Power Amplifier Efficiency

In assessing the power amplifier performance, power amplifier efficiency is considered as one of the most important factors. It is also referred to as dc to RF efficiency since it is a measure of how much dc supply is transferred to RF output power. The power amplifier efficiency is represented by

$$\eta = \frac{P_{out}}{P_{dc}} \tag{4.2}$$

where *Pout* and *Pdc* are the output power and dc power, respectively. The output power can be expressed as

$$P_{out} = \frac{I^2 R_L}{2} \tag{4.3}$$

where I and R_L are the maximum current to the load and R_L is the load resistance, respectively. The dc power can be determined by

$$P_{dc} = \frac{1}{T}\int_0^T V_{cc} I_c dt = \frac{V_{cc}}{T}\int_0^T I_c dt \tag{4.4}$$

Where I_c is the DC current component of the supply voltage. Having the gain of the power amplifier into consideration, the power added efficiency (PAE) can also be determined.

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} = \frac{P_{out} - P_{in}/G}{P_{dc}} = \eta(1 - \frac{1}{G}) \tag{4.5}$$

where G is the power gain of the power amplifier. It can be observed that PAE becomes the efficiency discussed in (2) when the power gain of the power amplifier is high. Usually, this power added efficiency is over 90 % of the efficiency discussed in (2) once the power gain of the power amplifier is more than 10 dB. The power added efficiency will decrease as the power gain of the amplifier begins to saturate. Therefore, the best power added efficiency is determined before the gain compression point.

4.1.3 Power Amplifier Linearity

The index for the linearity measure of power amplifier is the 1-dB compression point (P1dB). The P1dB point to a power level which is reduced by 1 dB compared to a hypothetical linear power increase. The amplifiers which handle low power signals may use IP3 as the index of power handling capability, however, the nonlinear terms for power amplifiers are much greater than low power amplifiers such as low noise amplifier. Therefore, in measuring the linearity performance of power amplifiers, the 1-dB compression point is used. The measure of spectral regrowth is also considered in practical power amplifiers as the ratio between the power in main channel and adjacent channel, which is referred to as adjacent channel power ration (ACPR) [63].

As mentioned, the major concern which affects the linearity of power amplifiers are the nonlinear devices such as transistors and diodes and inter-modulation products (IMD) composed of harmonic signals. There are various ways to reduce the nonlinear terms to enhance the linearity of power amplifiers such as low pass matching, harmonic termination, degeneration, back-off, feedback, and predistortion [64].

First, the low pass matching technique indicates the output matching network is composed of low pass filtering network. With simple inductor and capacitor matching network, the inductor and capacitor are used in series and shunt, respectively, providing both the matching and low pass filtering function so that harmonic frequencies can be reduced or filtered out. Second, a harmonic termination network can be used at the output of the amplifier. It is a band-reject or stop notch filter. The tuned notch filter at

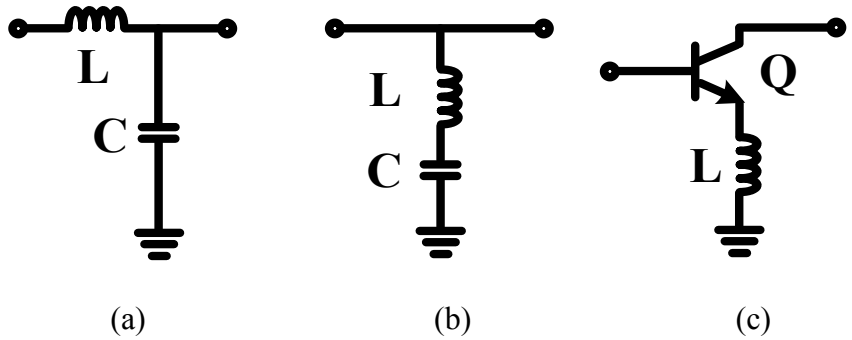


Figure 4.1.(a) Low pass matching network, (b) notch filter for harmonic termination, and (c) degeneration

harmonic signals can effectively reduce unwanted signals while not affecting the desired main signal. Third, a degeneration technique is also used for power amplifier linearity enhancement. An inductor as shown in Figure 4.1(c) is connected to the emitter (for BJT) and the source (for MOS) for degeneration. The main purpose of the inductor degeneration is to keep the amplifier stable and also improve impedance matching. It is also can be considered at negative feedback which reduces the signal level transferred in the transistor. In other words, this degeneration reduces gain of an amplifier which reduces unwanted frequency signals at the input of the amplifier, thereby keeping unwanted signal and harmonic levels after the amplifier low. The disadvantage of such a degeneration technique is the reduced gain, however, it helps to improve both the stability and linearity. Forth, the backoff technique is also widely used for a linearity enhancement. This technique have power amplifiers operate at the power level lower

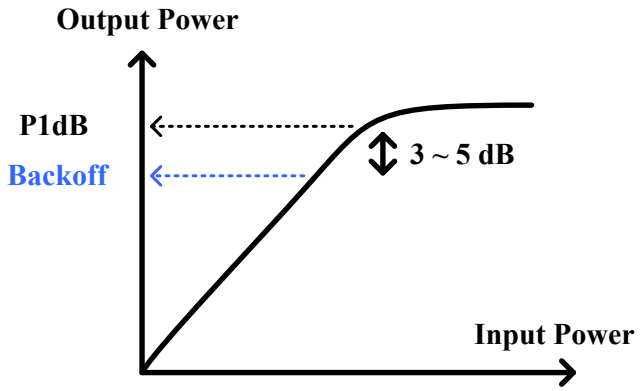
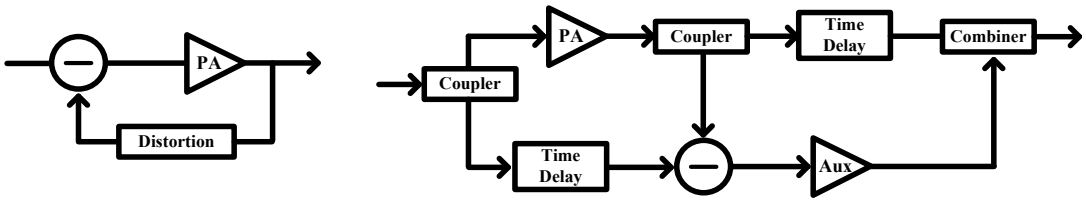


Figure 4.2.Backoff operation of power amplifier for linearity

than P1dB by 3 or 5 dB thereby guaranteeing linear operation of the amplifier as shown in Fig.4.2. Reversely, it can be taken as employing higher linearity amplifier than the required system performance, which means more power consumption and cost. Fifth, the feedback and feedforward technique are also linearity enhancement methods. The feedback technique are various in realization in amplifiers, however, the fundamental idea is to couple the nonlinear terms at the output of the amplifier and inject the distorted signal to the input of the amplifier with negative inversion so that only nonlinear terms can be reduced. Figure 4.3(a) depicts the concept of the feedback technique. The feedforward technique is presented in Figure 4.3(b). This technique also couple the nonlinear terms from the output of the amplifier. However, main tone signal is subtracted from the coupled nonlinear signal and the remaining nonlinear term is combined at the output of the amplifier. This technique effectively reduces nonlinear terms since the operation is carried out at the output. The technical difficulties in



(a) (b)

Figure 4.3.(a) Feedback and (b) feedforward technique

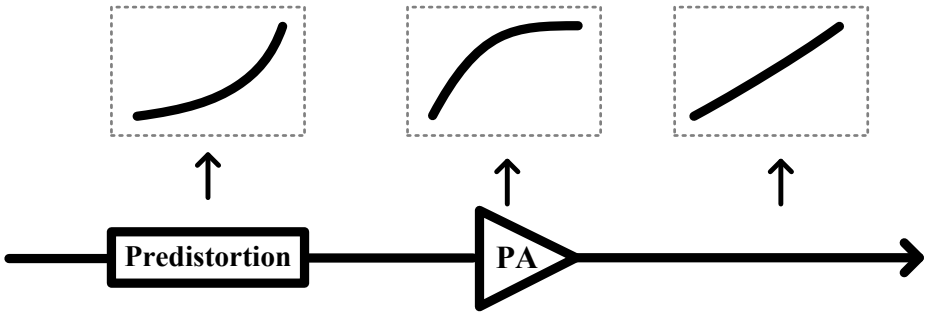


Figure 4.4. Predistortion technique

realizing feedforward are high compared to other methods so it is generally utilized for high performance base stations. Finally, the predistortion technique distorts the input signal of a power amplifier so that the output signal of the amplifier exhibits a linear output power as shown in Figure 4.4. It is conceptually simple and effectively provides linear response as well. Both the digital and analog predistortion technique are employed for integrated circuits for mobile application.

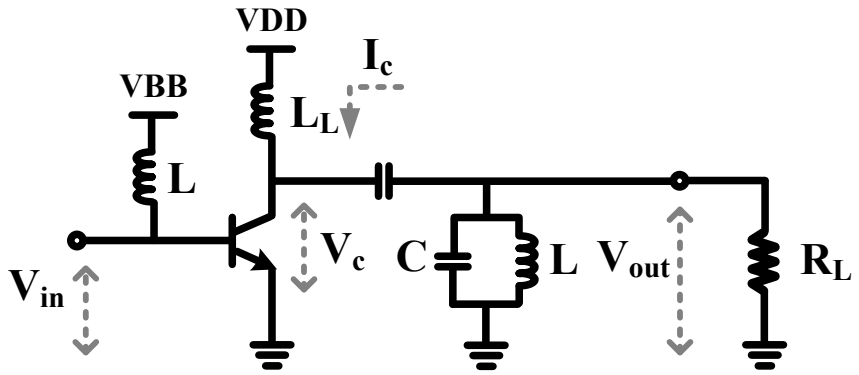


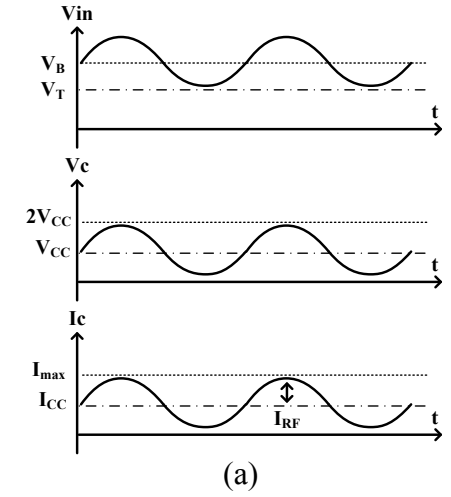
Figure 4.5. Power amplifier with tuned load

4.1.4 Class of Power Amplifiers

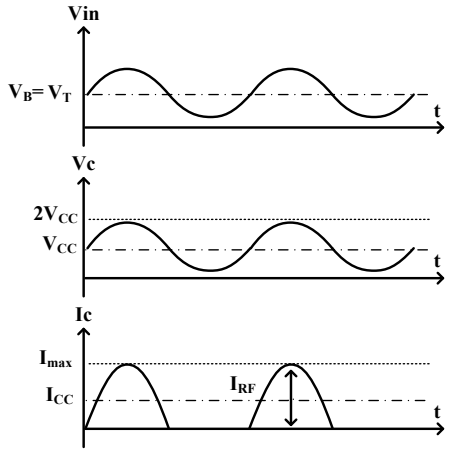
Power amplifiers are under a number of categorizes such as A, B, AB, C, D, E, F, and so on [64]. Those different power amplifiers are grouped by the difference in the voltage and current waveforms or conducting angle. Figure 4.5 presents typical power amplifier circuit with tuned load for the discussion of class A, B, AB, and C amplifier. To effectively categorize the class of different amplifiers, the base voltage is denoted as V_b, the collector voltage is denoted as V_c, and collector current is denoted as I_c. The following Figure 4.6 presents the waveforms of class A, B, and C power amplifiers.

The class A amplifier is biased to have the collector current flow all the time. Since the collector current's conduction angle is a full cycle 360 degree, this amplifier provides linear operation without any distortion ideally. The class B amplifier is biased at the threshold voltage which limits the collector current flow only during a half cycle

as shown in Figure 4.6. The conduction angle for this amplifier is 180 degree. The class C amplifier is biased at a lower voltage than the threshold at the base which makes the conduction angle of collector current to be smaller than 180 degree. The class AB amplifier is biased so that the conduction angle can be between 180 and 360 degree, which is the operation between class A and B amplifiers.

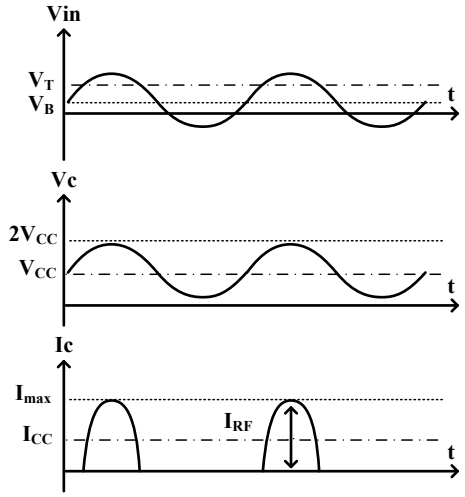


(a)



(b)

Figure 4.6.Waveforms of base voltage, collector voltage, and collector current of (a) Class A amplifier (b) Class B amplifier and (c) class C amplifer



(c)

Figure 4.6.Continued.

The following table summarizes the conduction angle and the theoretical efficiency of each power amplifier class.

Table. 4.1 Conduction angle and efficiency of power amplifiers

Class	**Conduction Angle [degree]**	**Efficiency [%]**
A	360	50
AB	180 ~ 360	50 ~ 78.5
B	180	78.5
C	0 ~ 180	78.5 ~ 100

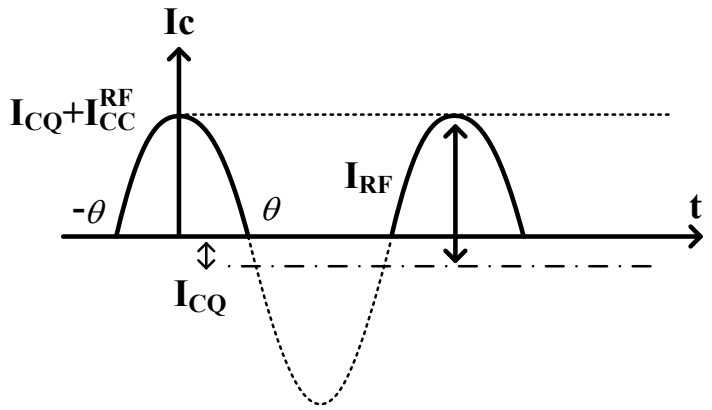


Figure 4.7. Class A, B, and C waveform analysis

The conduction angle for this amplifier is 180 degree. The class C amplifier is biased at a lower voltage than the threshold at the base which makes the conduction angle of collector current to be smaller than 180 degree. The class AB amplifier is biased so that the conduction angle can be between 180 and 360 degree, which is the operation between class A and B amplifiers.

A number of important relationships can be found by analyzing the waveform of class A, B, and C amplifiers. From Figure 4.7, the collector current is represented by

$$I_{CQ} = I_{CC}^{RF} \cos\theta \tag{4.6}$$

With the assumption that the power amplifier with tuned load as shown in Figure 4.5, the dc component with main signal tone can be derived as

$$I_{dc} = \frac{1}{2\pi}\int_{-\theta}^{\theta}(I_{CC}^{RF}\cos\omega t - I_{CQ})\,d\omega t$$

$$= \frac{I_{CC}^{RF}}{\pi}(\sin\theta - \theta\cos\theta) \tag{4.7}$$

The fundamental tone current is expressed as

$$i_f = \frac{4}{2\pi}\int_0^{\theta}(I_{CC}^{RF}\cos\omega t - I_{CQ})\cos\omega t\,d\omega t = \frac{I_{CC}^{RF}}{2\pi}(2\theta - \sin 2\theta) \tag{4.8}$$

Then the output power can be calculated by using (4.8) as

$$P_{out} = \frac{i_f^2 R_L}{2} = \frac{R_L}{2}\left[\frac{I_{CC}^{RF}}{2\pi}(2\theta - \sin 2\theta)\right]^2 \tag{4.9}$$

And the maximum output power can be expressed as following given the average peak voltage swing at the collector is *Vcc*

$$P_{out}^{\max} = \frac{V_{CC}I_{CC}^{RF}}{4\pi}(2\theta - \sin 2\theta) \tag{4.10}$$

Then the maximum efficiency can be calculated as

$$\eta_{\max} = \frac{P_{out}^{\max}}{P_{dc}} = \frac{2\theta - \sin 2\theta}{4(\sin\theta - \theta\cos\theta)} \tag{4.11}$$

The achievable efficiency for class A, B, AB, and C amplifiers based on (4.11) are already presented in Table. 4.1.

4.2 Concurrent Dual *Q/V*-band Power Amplifier

In this chapter, a concurrent dual *Q*/*V*- band power amplifier design is presented. The motivation of the proposed dual *Q*/*V*- band power amplifier will be introduced and the challenges in realizing concurrent dual-band power amplifier will be discussed.

4.2.1 Introduction and Motivation

The growing demand in millimeter-wave radar systems also provides the challenge in realizing multi-function miniaturized module on a system-on-chip. Hence the concurrency principle in designing any receiver and transmitter components can be attractive. III-V compound process such as GaAs or InGaP-GaAs has been traditionally used in high performance applications [65-67]. However, there are disadvantages in using such performance compound semiconductor: low level of integration with silicon substrate based digital circuits and high cost.

Recently, the use of SiGe (Silicon Germanium) HBT (Heterojunction Bipolar Technology) demonstrated comparable performance to III-V compound semiconductors such as GaAs [68-69]. Even though there are still issues in SiGe based process such as low avalanche breakdown voltages (B_{VCEO} and B_{VCBO}) [70-72]. Nevertheless, the cost effective silicon process is attractive because of continued process improvement for both active transistors and passive component with high quality factor. In realizing the proposed dual-band power amplifier, a number of techniques are employed to overcome the aforementioned inherent drawbacks. At the same time, to realize the concurrent dual-band design principle maintained with the T/R/Calibration switch module and low noise amplifiers in previous sections, a challenging yet effective approach was proposed in this section. A number of dual-band design techniques are proposed.

4.2.2 Concurrent Dual *Q*/*V*-band Power Amplifier Design

In this section, the design of the proposed concurrent dual *Q*/*V*- band power amplifier is introduced in detail. The power amplifier is designed using Jazz 0.18-μm SiGe BiCMOS technology with cutoff frequencies f_T/f_{max} of 230/280 GHz [38]. The process is composed of six metal layers with five copper layers and a thick aluminum top layer. The SiGe HBT breakdown voltages are B_{VCEO} of 1.9 V and B_{VCBO} of 5.8V.

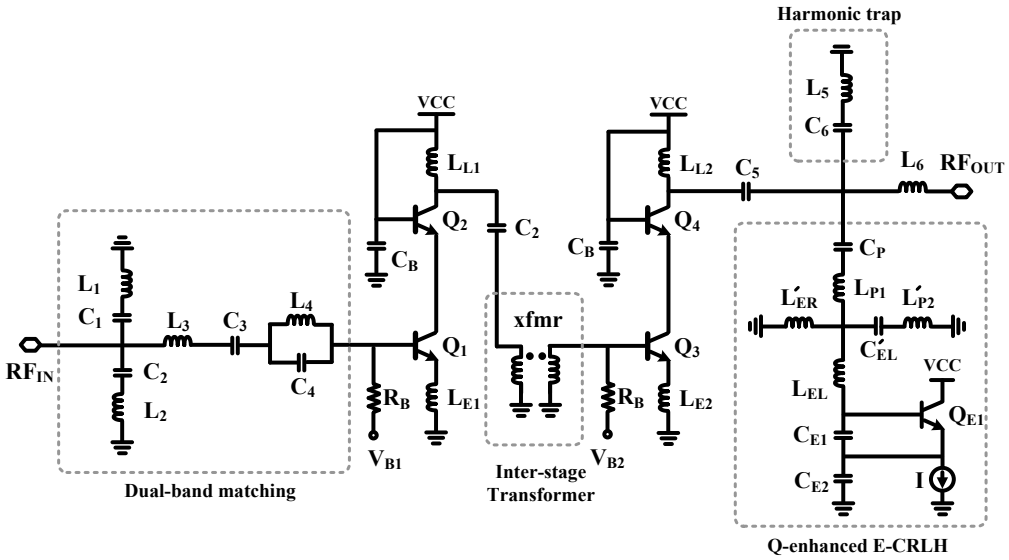


Figure 4.8.Schematic of dual-band power amplifier

Table 4.2 Component values for concurrent dual-band power amplifier

L_1	L_2	L_3	L_4	L_5	L_6	L_{L1}	L_{L2}	L_{E1}	L_{E2}
45pH	55pH	132pH	17.5pH	193pH	95pH	75pH	52.5pH	5pH	10pH
L_{P1}	$L_{ER'}$	$L_{P2'}$	L_{EL}	C_1	C_2	C_3	C_4	C_5	C_6
27.5pH	18.5pH	30pH	270pH	59.5 fF	52fF	245fF	550fF	80.75fF	513fF
C_P	$C_{EL'}$	C_{E1}	C_{E2}	Q_1	Q_2	Q_3	Q_4	Q_{E1}	$R_{B1,2}$
425fF	145fF	72fF	72fF	0.15× 20.32 μm^2	0.15× 20.32 μm^2	0.15× 20.32 μm^2	0.15× 20.32 μm^2	2.5 μm^2	350 Ohm

4.2.2.1 Two Stage Concurrent Dual-band Power Amplifier

The proposed concurrent dual-band *Q*/*V*- band power amplifier schematic is presented in Fig. 4.8. The concurrent dual 44/60- GHz power amplifier is designed to operate in class AB. To facilitate the dual-band operation of the amplifier, dual-band impedance matching is carried out and also harmonic and inter-modulation filtering is

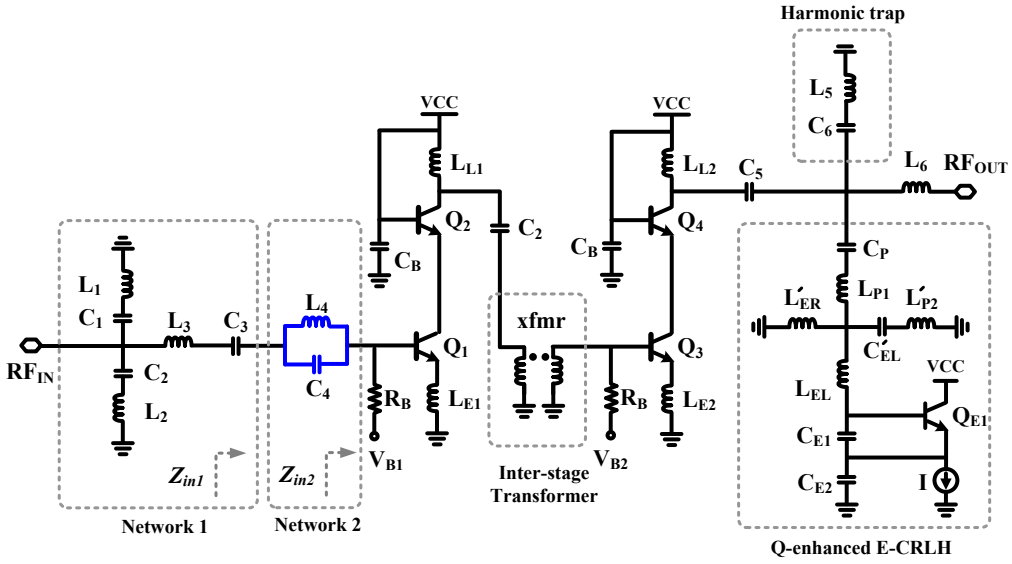


Figure 4.9.Input impedance matching for dual-band power amplifier

applied both at the input and output of the power amplifier. The inter-stage matching is performed with a transformer for a wide impedance matching over 44/60- GHz to reduce any more additional loss caused by matching networks. All the passive components such as spiral inductors, inter-connections, finger layouts of the emitter and collector of transistors are simulated with full-wave EM simulator IE3D [48].

The cascode structures are employed to overcome the breakdown voltage issue with applying higher supply voltage. The upper transistor in the cascode structure also provides better reverse isolation performance which results in a stable operation of the power amplifier. The base of the main amplifying common-emitter transistor Q1 and Q3 are biased using a 350 Ohm resistor to insure the higher voltage swing between the collector and emitter [73-74]. The transistors in both the first and second cascode stages

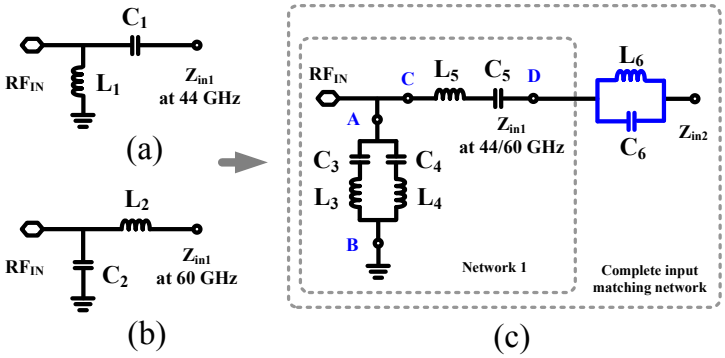


Figure 4.10. Input impedance matching

are configured to have two emitter, three base and two collector fingers and sized to have the emitter area of 0.15×20.32 μm^2, which ensures the maximum current density of 10 $mA/\mu m^2$.

To realize the concurrent operation of the power amplifier, a rigorous approach is carried out to perform dual-band matching. There has been dual-band matching schemes using a network theory [75-77]. It is shown that concurrent dual-band impedance matching with a reasonable loss performance is possible with high order inductor and capacitor network at millimeter-wave frequency range [77]. The input matching of the dual *Q*/*V*- band power amplifier carried out in this section expands the dual-band matching proposed in [77] by adding one more transmission zero which will be located at the rejection frequency between 44 and 60 GHz. The input matching network is composed of two networks as shown in Fig. 4.9. In designing the dual-band low noise amplifiers in Section III, a parallel inductor and capacitor network was inserted to suppress the unwanted signal between 44 and 60 GHz. Inspired by the idea to provide a

transmission zero between the design frequencies, a parallel inductor and capacitor network to provide a transmission zero at 51.5 GHz was inserted in Network 2 in Fig. 4.10 in the matching network. The impedance (Z_{in2} in Fig. 4.9) looking into the common emitter transistor in the first stage were 3.24-*j*3.19 and 2.91+*j0*.4 at 44 and 60 GHz, respectively, for conjugate matching. The inductor and capacitor values are tuned to provide 7 dB attenuation at 51.5 GHz. By adding Network 2, the input impedances (Z_{in1} in Fig. 4.9) have become 2.71-*j*1.7 and 2.1-*j*2.1 at 44 and 60 GHz, respectively. With a transmission zero at 51.5 GHz at the input with Network 2, a concurrent dual-band matching technique is applied to transfer these impedances to 50 Ohm. The matching networks for each single frequency at 44 and 60 GHz are derived first as shown in Fig. 4.10(a) and Fig. 4.10(b). The combined network composed of C3, C4, L3, and L4 between node A and B can provide an inductance at one frequency and a capacitance at other frequency [77], since the admittance of the network between node A and B is derived as

$$Y_{network1} = \frac{j\omega\omega_1^2 C_3}{\omega_1^2 - \omega^2} + \frac{j\omega\omega_2^2 C_4}{\omega_2^2 - \omega^2} \tag{4.12}$$

where $\omega_1 = 1/\sqrt{L_3 C_3}$ and $\omega_2 = 1/\sqrt{L_4 C_4}$. And one more resonant frequency of the network is calculated as

$$\omega_3 = \omega_1\omega_2\sqrt{\frac{C_3 + C_4}{\omega_1^2 C_3 + \omega_2^2 C_4}} \tag{4.13}$$

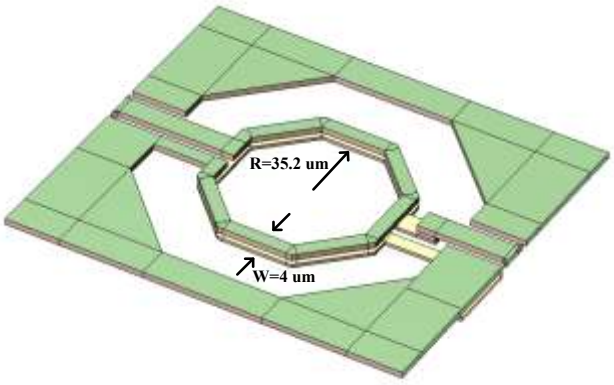
From (4.12), the admittance can provide both the inductance and capacitance at different frequency bands. The network is equivalent to inductor at $\omega_1<\omega<\omega_3$ and $\omega_2<\omega$ as follows.

$$L_{network1}^{equivalent} = 1/\left(\frac{\omega\omega_1^2 C_3}{\omega^2 - \omega_1^2} + \frac{\omega\omega_2^2 C_4}{\omega^2 - \omega_2^2}\right) \tag{4.14}$$

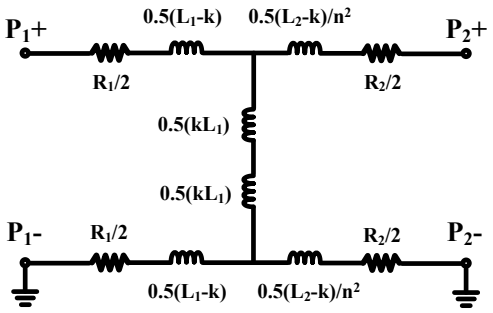
And it is equivalent to capacitor at $\omega<\omega_1$ and $\omega_3<\omega<\omega_2$ as follows.

$$C_{network1}^{equivalent} = \frac{\omega_1^2 C_3}{\omega_1^2 - \omega^2} + \frac{\omega_2^2 C_4}{\omega_2^2 - \omega^2} \tag{4.15}$$

Therefore, the combined network can function both as inductor and capacitor and the single band matching condition shown in Fig. 4.10 (a-b), $L_{network1}^{equivalent} = L_2$ and $C_{network1}^{equivalent} = C_1$, can be enforced. At the same time, the conditions to filter out the harmonic frequency of 88 GHz and intermodulation frequency of 104 GHz can be applied as $\omega_1 = 1/\sqrt{L_3 C_3} = 2\pi \times 88 \times 10^9$ and $\omega_2 = 1/\sqrt{L_4 C_4} = 2\pi \times 104 \times 10^9$. Solving the equations (4.14) and (4.15) with the harmonic and intermodulation frequency constraint provided above, the values in Network 1 can be obtained as C_3=57.34fF, C_4=51.6 fF, L_3=55.7 pH, and L_4=44.5 pH, respectively. Eventually, the combined input matching network shown in



(a)



(b)

Figure 4.11. On-chip transformer for inter-stage impedance matching (a) stacked transformer and (b) simplified equivalent circuit of the transformer

Fig. 4.10(c) provides concurrent dual-band conjugate impedance matching providing three transmission zeros at 51.5 GHz, 88GHz, and 104 GHz at the same time.

The inter-stage matching of the proposed amplifier is performed using a transformer. Due to the insertion loss arises from the dual-band input and output matching composed of multiple inductors and capacitors, a wideband on-chip transformer is designed to perform the inter-stage matching. The designed on-chip transformer is presented in Fig. 4.11(a). It is designed with two top most layers

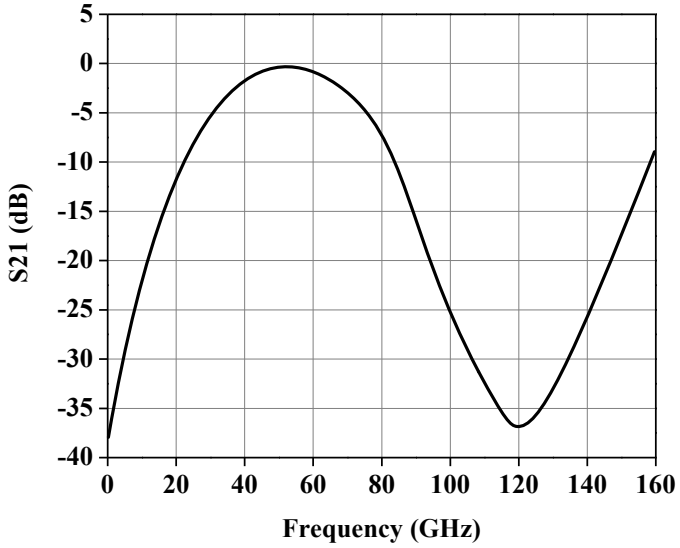


Figure 4.12. S-parameter of the designed on-chip transformer

composed of thick aluminum and copper layer. The simplified equivalent circuit of the stacked on-chip transformer is presented in Fig. 4.11(b). The quality factor of each spiral inductor L_1 and L_2 is presented as follow.

$$Q_1 = \frac{\omega L_1}{R_1}, \quad Q_2 = \frac{\omega L_2}{R_2} \tag{4.16}$$

It is also important to minimize the loss induced from the transformer along with the impedance matching. The insertion loss of the stacked transformer relies on the quality factor of each spiral arms and also the coupling factor between the two spiral inductors.

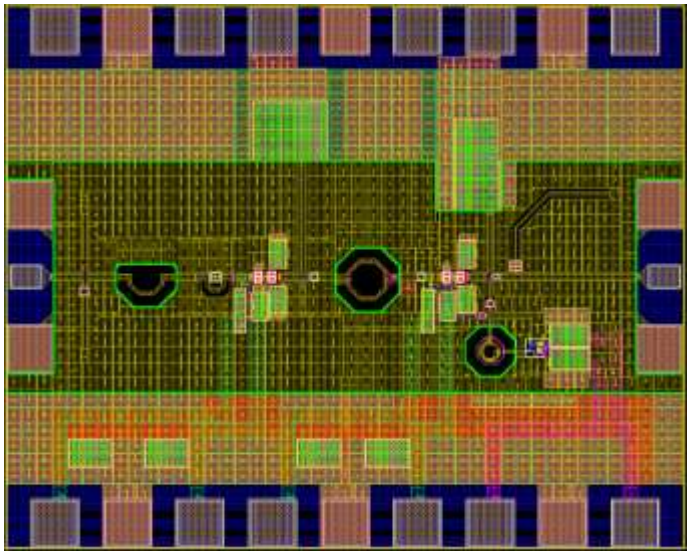


Figure 4.13.Complete concurrent dual *Q*/*V*- band power amplifier layout

The expression of the efficiency of the stacked transformer can be represented by the following equation.

$$\eta = \frac{R_L}{n^2 \left(\frac{\frac{\omega L_1}{Q_2} + \frac{R_L}{n^2}}{\omega k L_1} \right)^2 \frac{\omega L_1}{Q_1} + \frac{\omega L_2}{Q_2} + \frac{R_L}{n^2}} \tag{4.17}$$

where η and k are the efficiency of a stacked transformer and coupling factor between L_1 and L_2, respectively. From (4.17), it can be seen that high quality factor of each spiral arms and the coupling factor contributes high efficiency of the transformer. The use of

the two top most metal layers for the transformer design helps to increase its efficiency. The inter-stage transformer is designed to perform the wideband impedance matching over 44 and 60 GHz. The output impedance of the first cascode stage were 15.7-*j*8 ohm and 18.2-*j*6 Ohm at 44 and 60 GHz, respectively, and the input impedance of the second cascode stage were 2.6-*j*1.3 Ohm and 2.9+*j*3.5 Ohm, respectively. The S-parameter simulation result of the on-chip transformer is shown in Fig. 4.12. The insertion loss at 44 and 60 GHz are 0.85 and 1.15 dB, respectively. Along with the impedance matching, the geometry of the spirals is chosen to provide a transmission zero at 120 GHz which are the second harmonic of 60 GHz based on full electromagnetic simulation. The output matching of the concurrent dual *Q*/*V*- band is carried out with two intermodulation and harmonic traps. The intermodulation termination is performed with the Q-enhanced E-CRLH network presented in section III.2.2. It was already presented and analyzed in the aforementioned section. Briefly, it was designed based on the electrical dual-CRLH network to provide quarter-wavelength both at 44 and 60 GHz. To overcome the low quality factor issue with the on-chip components, the Colpitts style negative generation circuit is integrated at the stop band frequency, thereby providing signal rejection between the two design frequency of 44 and 60 GHz. Additionally, the parasitic components which are intentionally added to create transmission zeros contributed to reject the intermodulation signal at 28 and 76 GHz. The designed intermodulation and stop-band rejection network is used as a trap at the output of the dual-band amplifier as well. Furthermore, to completely reject all the harmonics and intermodulation below 120 GHz, one more harmonic trap network (L5 of 193 pH and C6 of 513 fF in Fig. 4.8)

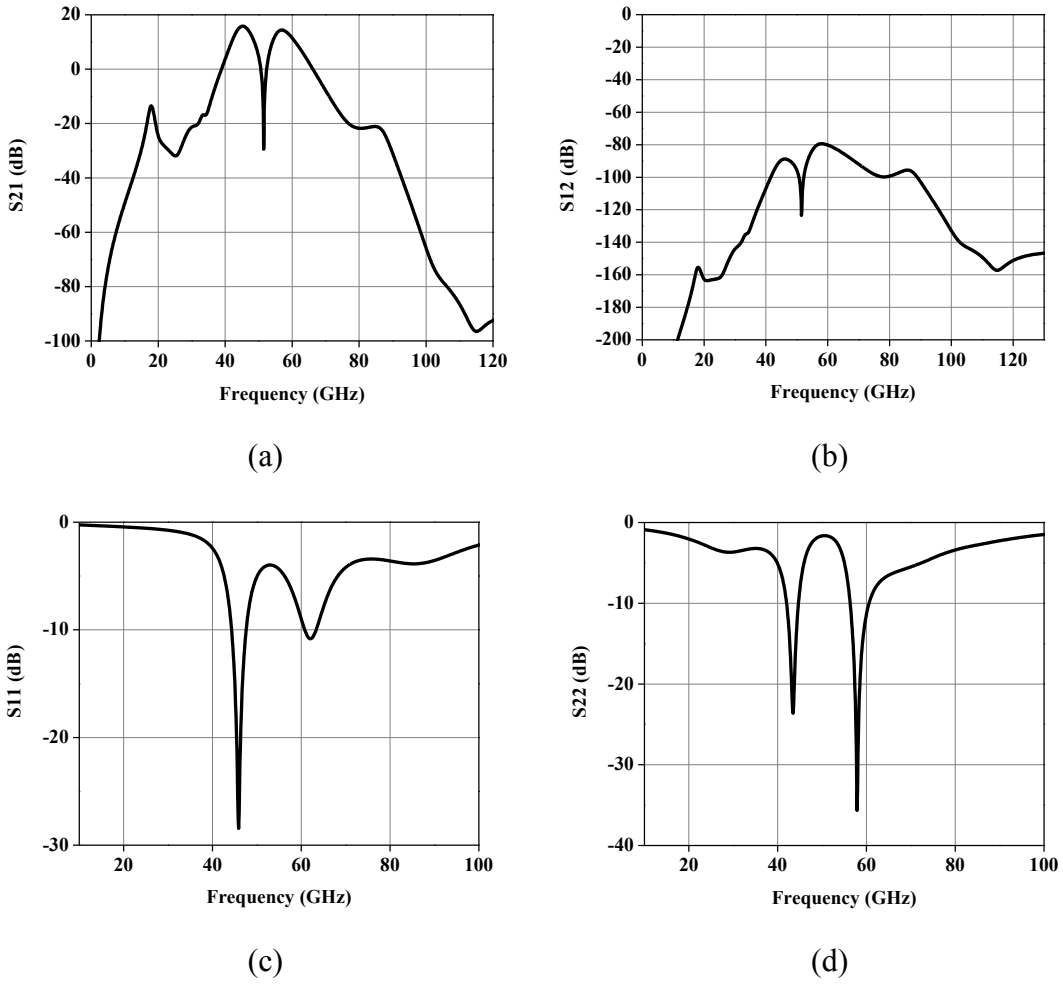


Figure 4.14. S-parameter of the designed power amplifier: (a) gain (b) reverse isolation (c) S11 and (d) S22

tuned at 16 GHz is added at the output of the power amplifier. The load pull simulation returned the optimum power matching impedances of 1.35-*j*0.3 and 1.16-*j*0.02 Ohm with both the intermodulation and harmonic trap networks and a single series inductor was used to transfer the impedances to 50 Ohm load. As will be shown in the next section, totally seven transmission zeros were created by the matching networks, harmonic, and

intermodulation trap up to 120 GHz which provided rejection at the 1st IMD terms at 16 GHz and 104 GHz, the 2nd IMD terms at 28 GHz and 76 GHz, the 2nd Harmonic terms at 88 GHz and 120 GHz, and finally at the stop-band at 51.3 GHz.

4.2.2.2 Concurrent Dual-band Power Amplifier: Performance

The performance of the proposed concurrent dual-band power amplifier is presented in this section. Fig. 4.14 presents the S-parameter simulation results. The gain response in Fig. 4.14(a) shows the gain of 17.5 and 17.35 dB at 44 and 60 GHz, respectively, with a minor gain imbalance of 0.15 dB. It is should be noticed the transmission zeros are placed at the unwanted harmonics (88 and 120 GHz), intermodulation terms (16, 28, 76, and 104 GHz), and 51.31 GHz which is the stop-band frequency between 44 and 60 GHz for dual-band response. The 3dB-bandwidth for each band was 4.8 and 4.2 GHz. The reverse isolation shown in Fig. 4.14(b) is more than 80 dB up to 120 GHz and above. The return losses both at the input and output in Fig. 4.14(c-d) presents that the impedance matching is carried out concurrently at dual-band showing more than 10 dB and 20 dB return losses at the desired frequency bands.

The linearity and power added efficiency performance in single-mode operation are shown in Fig. 4.15. In the single-mode operation, only one tone at either 44 GHz or 60 GHz is swept to measure the linearity performance. For 44 GHz single mode, the P1dB and maximum output power at 44 GHz were 10.5 dBm and 12.4 dBm, respectively, as shown in Fig. 4.15(a). The maximum power added efficiency is

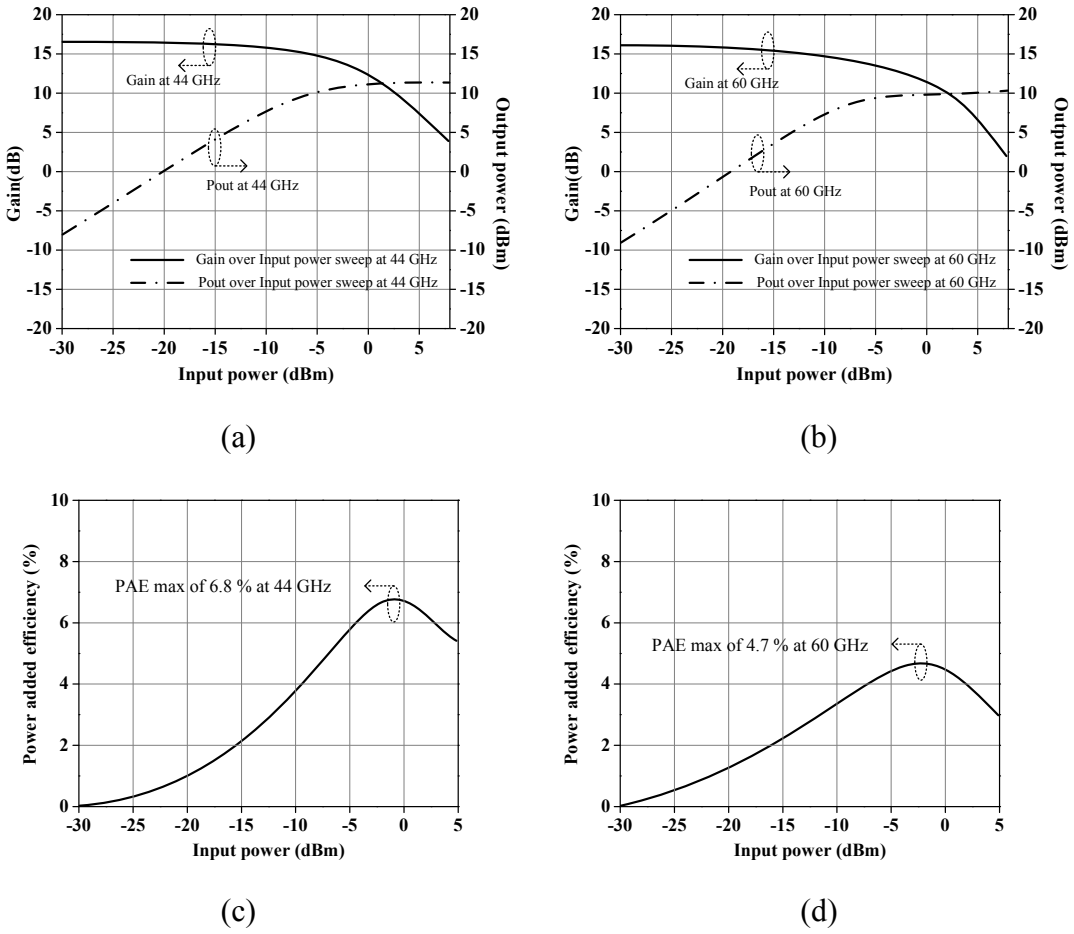


Figure 4.15.Single-band mode: gain, output power and PAE (a) gain and output power at 44 GHz, (b) gain and output power at 60 GHz, (c) power added efficiency at 44 GHz, and (d) power added efficiency at 60 GHz

calculated over input power sweep and it reached as high as 6.8 % as shown in Fig. 4.15(c).For 60 GHz single mode, the P1dB and maximum output power at 60 GHz were 10.3 and 10.6 dBm, respectively, as presented in Fig. 4.15(b). The maximum power added efficiency reached as high as 4.7 %.The linearity and power added efficiency performance in dual-mode operation are shown in Fig. 4.16. In the dual-mode operation,

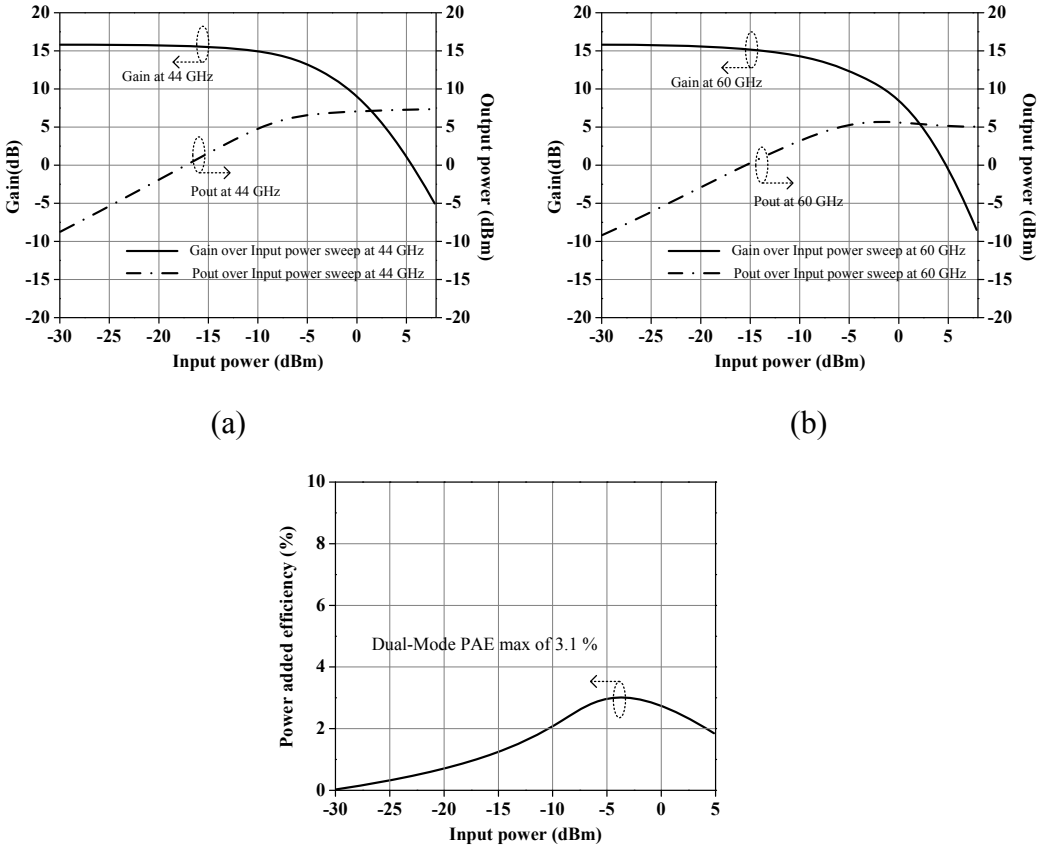


Figure 4.16. Dual-band mode: gain, output power and PAE (a) gain and output power at 44 GHz, (b) gain and output power at 60 GHz, (c) power added efficiency in dual-mode

two tones at 44 GHz and 60 GHz are swept together to measure the linearity performance. In dual-mode, the P1dB and maximum output power at 44 GHz were 6.4dBm and 8.2dBm, respectively, as shown in Fig. 4.16(a). In dual-mode operation, the P1dB and maximum output power at 60 GHz were 5.7dBm and 5.1dBm, respectively, as presented in Fig. 4.16(b). The maximum power added efficiency reached 3.1 % as displayed in Fig. 4.16(c).

Table 4.3

Concurrent dual *Q*/*V*- band power amplifier performance and comparison

Reference	Frequency (GHz)	Technology	Gain (dB)	Pass-band Gain Imbalance (dB)	Rejection Ratio (dB)	Pout_max (dBm)	P1dB (dBm)	PAE (%)	Operation Mode
[77]	25.5 / 37	0.18 µm SiGe BiCMOS	21.4 / 17	4.4	28	13 / 9.5	6.8 / 4.6	7.1	Dual
[78]	45	0.12 µm SiGe BiCMOS	11	-	-	14.8	-	25	Single
[79]	45	0.12 µm SiGe BiCMOS	6	-	-	19.4	17	14.4	Single
[80]	60	0.12 µm SiGe BiCMOS	18	-	-	20	-	12.7	Single
This work	44	0.18 µm SiGe BiCMOS	17.5	-	-	12.4	10.5	6.8	Single
This work	60	0.18 µm SiGe BiCMOS	17.35	-	-	10.6	10.3	4.7	Single
This work	44 / 60	0.18 µm SiGe BiCMOS	17.5 / 17.35	0.15	32	8.2 / 5.1	6.4 / 5.7	3.1	Dual

In dual-mode, the following power added efficiency expression is used for the calculation [77].

$$PAE = \frac{(P_{out}^{44GHz} + P_{out}^{60GHz}) - (P_{in}^{44GHz} + P_{in}^{60GHz})}{P_{DC}} \tag{4.18}$$

where $P_{out}^{44GHz} / P_{in}^{44GHz}$ and $P_{out}^{60GHz} / P_{in}^{60GHz}$ are the output/input power at 44 and 60 GHz, respectively. And P_{DC} is the dc power supplied to the power amplifier. Finally, Table 4.3 summarized the simulated performance of the proposed concurrent dual-band power amplifier with other published power amplifiers operating in *Q*- and *V*- bands. There are

only a few concurrent dual-band power amplifiers reported and the single-band power amplifiers operating at *Q*- and *V*- band are listed for references. The proposed concurrent dual 44/60- GHz power amplifier provides unique frequency response with transmission zeroes placed at all the harmonic and intermodulation product frequency terms unlike other published power amplifier works [78-80].

4.2.3 Conclusion

The design and performance of a concurrent dual *Q*/*V*- band is presented. To meet the challenging requirement for the concurrent dual 44/60- GHz band design, a novel approach was carried out for all the input matching, inter-stage matching, and output matching network in conjunction with the synthesized harmonic/intermodulation termination networks. The matching networks effectively contributed to place transmission zeros at all the harmonic and intermodulation frequency terms up to 120 GHz. The proposed dual-band power amplifier employing novel matching and harmonic termination technique provides a suitable approach in highly-integrated multi-band components design based on silicon-based technology in millimeter-wave frequency spectrum. The demonstrated design is expected to contribute high integration of low-cost multi-band millimeter-wave radar systems for sensor and communication systems.

CHAPTER V

SUMMARY AND CONCLUSION

5.1 Contribution

In this research, I proposed and developed a number of novel concurrent dual-band millimeter-wave circuits and modules. These circuits and modules are expected to meet the growing demand in multi-band multi-mode radar array transceivers or multi-functional radar sensors. To address the challenging task in developing concurrent dual-band frequency response, a novel Q-enhanced metamaterial transmission line approach was employed.

With a complex requirement for a concurrent dual-band fully polarimetric digital beam former, a novel T/R/Calibration switch module is proposed and developed. The architecture of the proposed integrated T/R/Calibration switch enables both the transmit reference and receive calibration for accurate image synthesis. The integrated module supports all the transmit, receive, calibration, and idle mode of digital beam former array operation with Q-enhanced dual bandpass filtering response at 24.5 and 35 GHz in the reception and calibration paths. A novel way in utilizing the composite right/left- handed metamaterial transmission line was proposed with Q-enhancement technique to realize the dual-bandpass filtering function. The CRLH approach has been extensively used in RF domain for more than a decade, however, the proposed technique enable the use of the artificial transmission line approach in millimeter-wave IC design. The complete

integration with digital control unit and millimeter-wave multi-path switching circuit on a single silicon die is particularly attractive since the full integration of multi-functional circuits extends higher level of integration with other RF front-end circuits as well. The following concurrent dual *Q*/*V* (44/60 GHz)- band LNAs also provide unprecedented dual bandpass filtering function employing Q-enhanced CRLH and dual-CRLH structures. The Colpitts style negative generation circuit is integrated with both the metamaterial transmission line structure. In realizing the Q-enhanced response at the transition and stop-band frequency of CRLH and dual-CRLH, an additional transmission zero is introduced at the inter-stage of the two stage cascode amplifiers to effectively neutralize the effect of critical poles reside in the dual-band quarter-wavelength networks which could be overcompensated. In other words, a pole/zero cancellation technique is applied for a stable operation of the LNAs. For the concurrent dual (44/60 GHz)-band power amplifier, synthesized dual-band matching network is employed at the input and both the harmonic trap and Q-enhanced dual-band quarter-wavelength network is utilized as part of a harmonic termination at the output of the amplifier. The inter-stage matching is carried out by a transformer to avoid additional loss caused by dual-band matching networks both at the input and output composed of multiple inductors and capacitors.

In summary, novel concurrent dual-band front-end circuits including a T/R/Calibration switch module, low noise amplifiers, and power amplifier operating at *K*/*Ka*/*Q*/*V*- bands are proposed and developed in this research. The researches carried out here in this dissertation are expected to contribute to enhance the possibility in realizing

highly integrated, yet cost effective multi-functional millimeter-wave systems for sensing, imaging, and communication systems.

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