LOW POWER HIGH EFFICIENCY INTEGRATED CLASS-D AMPLIFIER CIRCUITS FOR MOBILE DEVICES

A Dissertation

by

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ABSTRACT

The consumer's demand for state-of-the-art multimedia devices such as smart phones and tablet computers has forced manufacturers to provide more system features to compete for a larger portion of the market share. The added features increase the power consumption and heat dissipation of integrated circuits, depleting the battery charge faster. Therefore, low-power high-efficiency circuits, such as the class-D audio amplifier, are needed to reduce heat dissipation and extend battery life in mobile devices. This dissertation focuses on new design techniques to create high performance class-D audio amplifiers that have low power consumption and occupy less space.

The first part of this dissertation introduces the research motivation and fundamentals of audio amplification. The loudspeaker's operation and main audio performance metrics are examined to explain the limitations in the amplification process. Moreover, the operating principle and design procedure of the main class-D amplifier architectures are reviewed to provide the performance tradeoffs involved.

The second part of this dissertation presents two new circuit designs to improve the audio performance, power consumption, and efficiency of standard class-D audio amplifiers. The first work proposes a feed-forward power-supply noise cancellation technique for single-ended class-D amplifier architectures to improve the power-supply rejection ratio across the entire audio frequency range. The design methodology, implementation, and tradeoffs of the proposed technique are clearly delineated to demonstrate its simplicity and effectiveness. The second work introduces a new class-D output stage design for piezoelectric speakers. The proposed design uses stacked-cascode thick-oxide CMOS transistors at the output stage that makes possible to handle high voltages in a low voltage standard CMOS technology. The design tradeoffs in efficiency, linearity, and electromag-

netic interference are discussed.

Finally, the open problems in audio amplification for mobile devices are discussed to delineate the possible future work to improve the performance of class-D amplifiers. For all the presented works, proof-of-concept prototypes are fabricated, and the measured results are used to verify the correct operation of the proposed solutions.

DEDICATION

To God and to my family.

ACKNOWLEDGEMENTS

First and foremost, I would like to thank God for all the blessings that He has bestowed upon me. Without His grace, I would have been lost.

"The Lord is my rock, my fortress, and my deliverer, my God, my rock in whom I take refuge, my shield, and the horn of my salvation, my stronghold." (Psalm 18:2)

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NOMENCLATURE

BTL	Bridge Tied Load
CDA	Class-D Amplifier
CMOS	Complementary Metal Oxide Semiconductor
DMOS	Double-Diffused Metal Oxide Semiconductor
DEMOS	Drain Extended Metal Oxide Semiconductor
EM	Electromagnetic
EMI	Electromagnetic Interference
GBW	Gain Bandwidth Product
IMD	Intermodulation Distortion
LDMOS	Laterally Diffused Metal Oxide Semiconductor
NMOS	Negative Channel Metal Oxide Semiconductor
PCB	Printed Circuit Board
PFM	Pulse Frequency Modulation
PMOS	Positive Channel Metal Oxide Semiconductor
PSRR	Power Supply Rejection Ratio
PWM	Pulse Width Modulation
PZ	Piezoelectric
RMS	Root Mean Square
SNR	Signal to Noise Ratio
SMC	Sliding Mode Control
SPL	Sound Pressure Level
THD	Total Harmonic Distortion
THN+N	Total Harmonic Distortion plus Noise

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1. INTRODUCTION

1.1 Motivation

The consumer's demand for state-of-the-art multimedia devices such as smart phones and tablet computers has forced manufacturers to provide more system features to compete for a larger portion of the market share. All these extra features expand the number of applications for these devices, but at the expense of increased power consumption and less battery life. Therefore, high-efficiency integrated circuits are needed to extend the battery life of the device.

The audio reproduction feature has become a standard in mobile devices where its high demand has increased the market size for audio integrated circuits at a tremendous rate from around $2.28 billion in 2013 to an estimated $2.51 billion in 2014 [1]. Thus, audio amplifiers with low power consumption, high efficiency, and high audio quality are in high demand.

The class-D amplifier (CDA) can operate with high efficiency while providing high audio quality [2, 3, 4, 5, 6, 7]. However, conventional loudspeakers used in mobile devices require large amounts of power to operate, thereby limiting the battery life despite the amplifier's high efficiency. The piezoelectric (PZ) speaker is an alternative that provides high audio quality with low power consumption, but there are few audio amplifiers capable to drive these speakers. Available amplifiers have large power consumption and poor audio quality, lessening the impact and benefit of PZ speakers in mobile devices. Thus, a high-efficiency, low-power audio amplifier for PZ speakers that provides high audio quality is needed.

Another important requirement is that the CDA in mobile devices has to be connected directly to the battery, providing the maximum amount of available power to the load [8, 9]. To reduce the space occupied by integrated circuits, system-on-chip (SOC) applications connect the digital circuits to the same supply as the analog circuits [3, 10]. Consequently, any noise on the battery power-supply plane is mixed together with the audio signal, degrading the audio amplifier performance. Hence, a good power-supply rejection ratio (PSRR) performance is highly desirable in the CDA. Conventional amplifiers increase the power consumption and/or complexity to achieve high PSRR. Thus, a simple and low power solution to increase the PSRR is essential in portable devices.

1.2 Research impact

This dissertation focuses on the design of integrated CDA circuits for mobile devices, addressing the issues of driving a low power PZ speaker, and improving the PSRR in the CDA with minimal added power dissipation. New architectures and design techniques for high performance audio amplifiers are introduced to extend battery life and occupy less space.

Nowadays, modern society is taking advantage of the multi-functionality of portable multimedia devices for productivity, education, and entertainment. Loudspeakers and headphones have become a standard in these devices, and having a portable device that provides accessibility and convenience for long periods of time is highly desirable. Therefore, enabling low-power high-efficiency audio amplifiers would provide longer battery life for extended phone calls, remote conferencing, video streaming, games, and music.

The potential of the presented dissertation research would benefit any individual that takes advantage of the multi-functionality of mobile devices. The global leaders in CMOS integrated circuits could leverage the research developments presented in this dissertation to provide mobile devices with extended battery life.

1.3 Dissertation organization

This dissertation is organized as follows. Section 2 reviews the fundamentals of audio amplification. The principles of sound and audio, the loudspeaker's operation, and the main audio performance metrics are described to explain the limitations involved in the audio amplification process. A brief review on audio amplifier classification and operation is discussed to show the efficiency advantage of the CDA over other configurations. Typical specifications of commercial class-D amplifiers are provided to understand the performance requirements in mobile devices.

In Section 3, the operating principle and design procedure of the CDA are examined to provide a broad view of the design tradeoffs involved. The design requirements of the main building blocks in close loop architectures with different modulation techniques are discussed. The main CDA output stage configurations are examined as well as their performance tradeoffs.

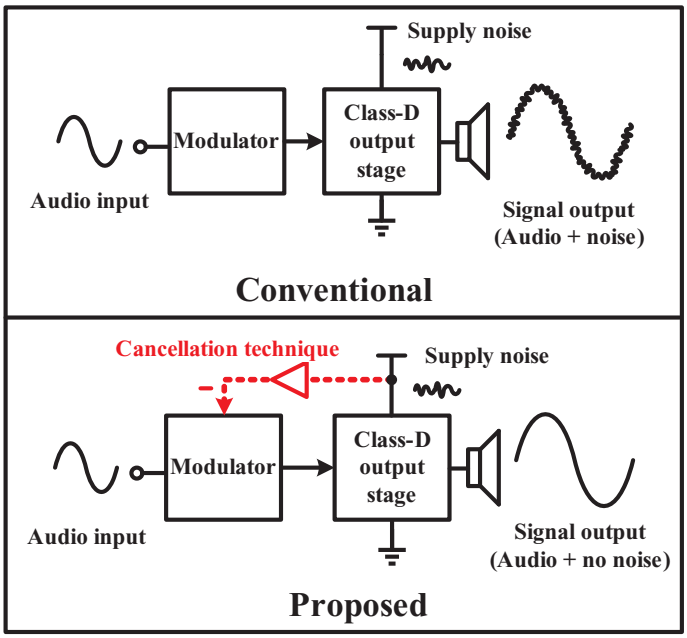

Figure 1.1: Proposed solution to cancel supply noise (Section 4).

Section 4 presents a feed-forward cancellation technique for single-ended class-D audio amplifier architectures to improve the PSRR performance with low power consumption, as illustrated in Fig. 1.1. The design methodology, implementation, and tradeoffs of the proposed technique are clearly delineated to demonstrate its simplicity and effectiveness. Simulation and experimental results are provided to verify the correct operation of the proposed technique.

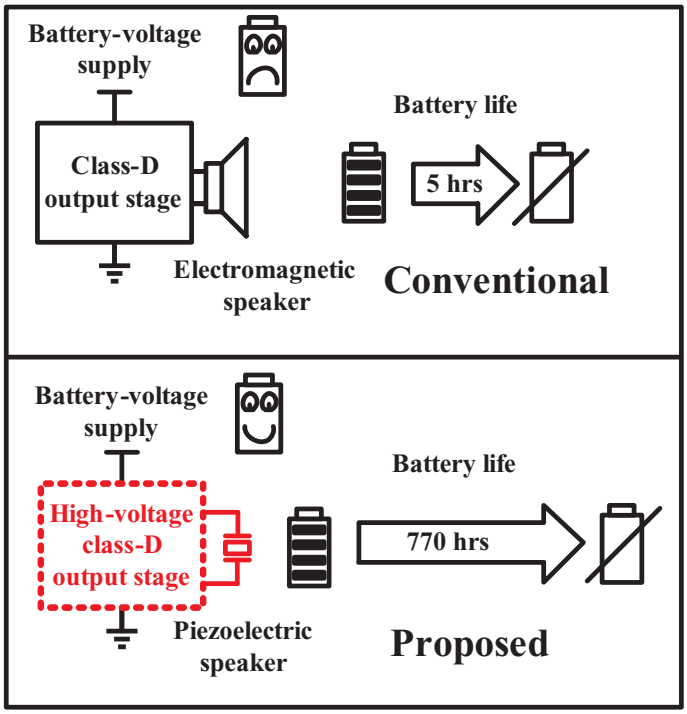

Figure 1.2: Proposed solution to drive piezoelectric speakers (Section 5).

Section 5 introduces a new CDA for driving PZ speakers to extend battery life, as depicted in Fig. 1.2. The PZ speaker's small form factor and low power consumption provide an attractive alternative for conventional loudspeakers. The design tradeoffs of the CDA for driving PZ speakers are examined. A new monolithic implementation is

proposed that uses stacked-cascode thick-oxide CMOS transistors at the class-D output stage, avoiding expensive high-voltage semiconductor devices to handle high voltages in a low voltage standard CMOS technology. The design methodology, implementation, and tradeoffs are provided as well as the experimental results.

The open problems in audio amplification for mobile devices are explained in Section 6 to describe the CDA trends to reduce the cost and EMI of the amplifier; audio CODEC processors are briefly explained to leverage the understanding of the CDA to apply it for low power low voltage analog-to-digital converters. Section 7 summarizes this dissertation. Appendix A is included to briefly detail the operation of a class-G amplifier with a proposed solution to increase the linearity of the amplifier during supply transitions with low power consumption. Appendix B presents more details for a non-linear controller in the class-D amplifier to achieve high PSRR using integral sliding mode control.

2. FUNDAMENTALS AND METRICS OF AUDIO AMPLIFICATION

2.1 Principles of sound and audio

An audio amplifier is a device that takes an input electrical signal representing the desired audio information, amplifies it, and delivers it to a transducer that converts the electrical signal back to audio as described in Fig. 2.1. The input signal can be either digital or analog, but the output signal has to be analog since the audio transducer only operates with continuous time signals.

The main objective of the audio amplifier is to accurately drive the audio transducer with the amplified output signal. To understand the tradeoffs involved in the design of audio amplifiers, it is useful to review the basics on sound and audio signals.

2.1.1 Sound and audio definition

Sound is typically defined as a mechanical pressure wave that propagates through a medium such as air or water. It originates from a vibration source that displaces the medium particles in a backward and forward motion. This pattern is characterized with some generic properties such as wavelength, period, amplitude, and direction.

The wavelength of the audio waveform (λ) is the distance that the sound travels in a single direction along a medium in a repeating pattern between consecutive points of the same phase as observed in Fig. 2.2. The typical audio signal contains many different wavelengths with distinct amplitudes, but is typically simplified as a collection of sinusoidal waves. The frequency of the signal, expressed in cycles per second, is expressed as,

$$f = \frac{c}{\lambda} \tag{2.1}$$

where c is the velocity of sound that in air takes the value of 331.45 m/s.

The fundamental frequency of the audio waveform is the greatest common divisor of the frequency of all the different frequency components of the signal. The typical audio frequency spectrum that is perceptible by humans ranges from 20 Hz to 20 kHz, or wavelengths from 16.5 mm to 16.5 m. However, most of the applications in mobile devices do not require the full range; voice communication only contain signals in the 300 Hz to 3 kHz range, and music reproduction could contain signals from 20 Hz up to 5 kHz for different music styles.

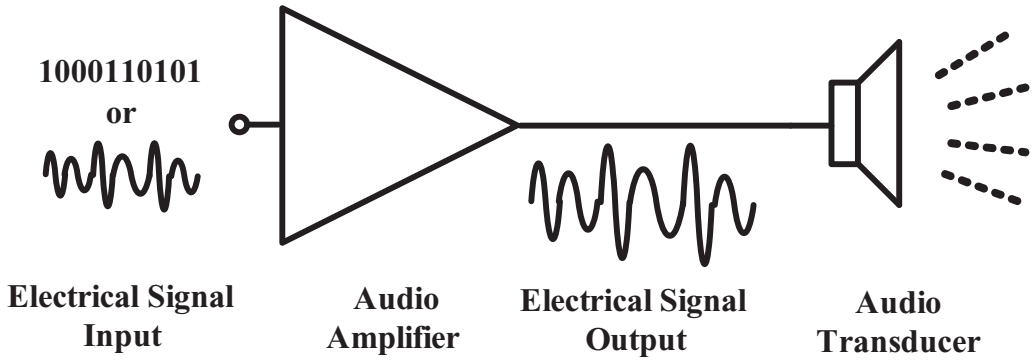

Figure 2.1: Audio amplifier operation.

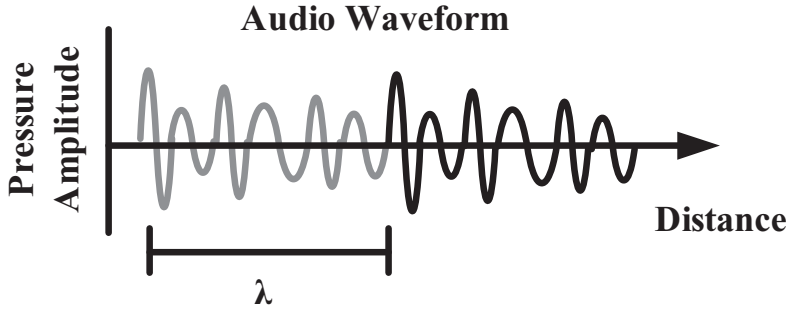

Figure 2.2: Audio waveform across distance.

The high end of the audio frequency spectrum (5 kHz up to 20 kHz) is rarely processed in mobile devices since it is only used in highly specialized professional audio applications like orchestra music reproduction.

2.1.2 Sound pressure level

The loudness of the sound wave has been difficult to characterize since each individual perceives the sound pressure differently, depending on age, lifestyle, health, among other circumstances. Therefore, a more formal metric is used to define how strong a sound wave is by measuring the difference, in a given medium, between a reference pressure (P_{ref}) and the pressure in the sound wave (P_{wave}).

The unit to measure pressure is defined as a pascal ($P_a = 1\ N/m^2$). As the human ear can detect sounds with a wide range of amplitudes, the sound pressure is often measured using a logarithmic scale such as the decibel. Therefore, the sound pressure level (SPL) can be defined as,

$$SPL = 20 \log 10 \frac{P_{wave}}{P_{ref}} \tag{2.2}$$

where $P_{ref} = 20\mu Pa$ is typically used since it is considered the threshold of human hearing for the sound propagating through air. The SPL can be measured using an instrument called a sound level meter [11] that senses the changes in pressure using a calibrated microphone and interprets the pressure difference to give a readout in the selected range. High SPL extended exposure can deteriorate a person's hearing by damaging sensitive inner-ear organs.

The typical SPL for conversational speech at 1m is 60 dB, while for a rock concert at 1m of the speaker is 100 dB; in mobile devices, the SPL performance can range from 60 dB up to 120 dB at short distances [12, 13, 14]. Other SPL examples are tabulated in table 2.1 for different scenarios.

The importance of the SPL is that it gives a metric to compare different audio transducers for different scenarios. The overall audio system loudness will depend on how much SPL the system can produce at a given distance.

Table 2.1: SPL example levels

Example	SPL (dB) at 1 m
Rustling of leaves	20
Quiet room	40
Conversation	60
Road with busy traffic	80
Noisy factory	90
Construction truck	100
Jet engine	120
Threshold of pain	140

2.2 Loudspeaker transducers in mobile devices

The audio reproduction function in mobile devices can be classified in two applications. First, small audio transducers are used in headphone applications where the sound wave only travels a few centimeters into the ear canal; these are used commonly for hands-free conversations and music listening. Second, moderate audio transducers are used as loudspeakers for video conferences, video games, and other applications where the sound wave has to travel a few meters.

The electric impedance of the speakers used in these applications greatly influences the design of the audio amplifier. Thus, an understanding of their physical construction and operation is needed to analyze their limitations and tradeoffs.

2.2.1 Electromagnetic speaker

The preferred speaker is the electromagnetic (EM) speaker, consisting of a magnet, a voice coil, and an acoustic cavity, as shown in Fig. 2.3. However, a large form factor is required in the EM speaker to deliver high SPL [15]. The typical materials used for the EM speaker construction are copper for the voice coil, plastic for the diaphragm, acrylonitrile butadiene styrene (ABS) for the frame, and Neodymium for the magnet. It operates by applying an electrical current through the voice coil to induce an electromagnetic field which in turn will generate a displacement of the acoustic diaphragm. Since the electromagnetic coupling factor is very small between the amount of electric current consumed to the amount of magnetic field produced, a large magnet and wide air cavity are needed to produce sound [11, 16].

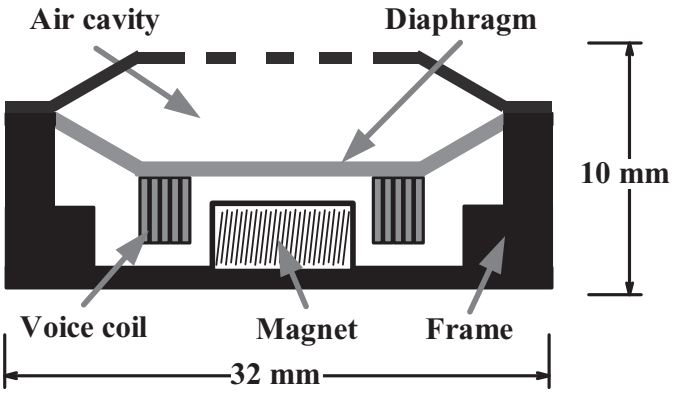

Figure 2.3: EM speaker physical structure side view.

The electrical impedance of a typical EM speaker across the audio frequency bandwidth is shown in Fig. 2.4. It can be observed that, on average, it behaves as a low value impedance between 4 to 32 Ω. A typical impedance value for most EM loudspeakers is 8 Ω while for EM headphones it is 32 Ω.

This means, that the amplifier has to output large electrical current through the voice coil to generate high SPL.

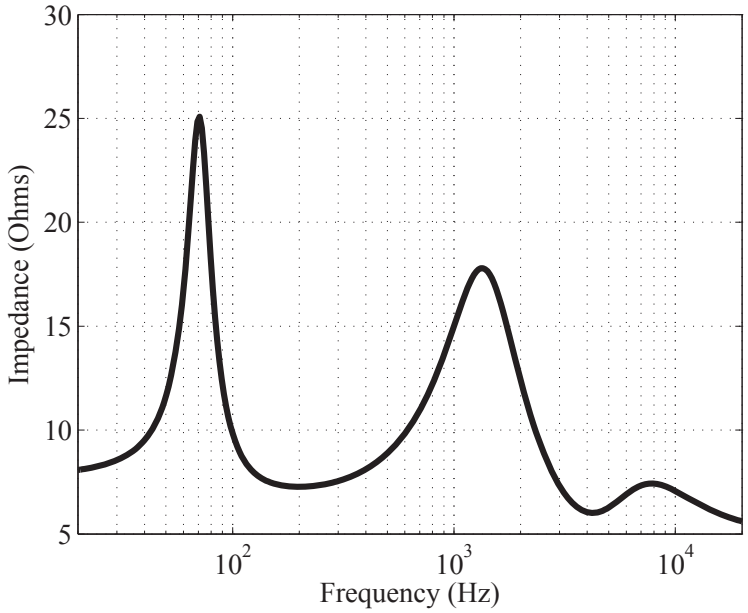

Figure 2.4: EM electrical impedance versus frequency.

An interesting point to note is that the EM speaker's low impedance requires large output power to operate, quickly consuming the battery life of mobile devices. For example, to produce 90 dB of SPL from an 8 Ω EM speaker, the battery has to provide around 1 W of average power or 353 mA of load current [15, 17, 18]. The battery life can be calculated as,

$$Battery\ life\ (hours) = \frac{Battery\ capacity\ (mAh)}{Load\ current\ (mA)}. \tag{2.3}$$

If a typical lithium-ion battery with 2000 mAh capacity is used with an ideal 100% efficient audio amplifier, the battery life only considering the EM speaker current consumption would be 5.67 hours.

In real applications, the audio amplifier current consumption would also be included in the calculation, decreasing even more the battery life; typical current consumption for audio amplifiers in mobile applications range from 1 mA to 10 mA. Thus, EM loudspeakers limit the battery life despite the audio amplifier's high efficiency and low current consumption.

2.2.2 Piezoelectric speaker

The physical structure of a typical PZ speaker is shown in Fig. 2.5 where a PZ element is attached to a film encased between a front panel and rear panel. Typical materials used for its construction are polycarbonate for the front and real panel, plastic resin or metal for the film, and lead zirconate titanate for the PZ element. The PZ element deflects with voltage applied across its terminals, causing the film to warp and bend up and down according to the voltage applied across the PZ element. The deflecting/bending action creates pressure waves pushing air through one or more openings that are arranged on the front panel that resonate and amplify the response of the speaker.

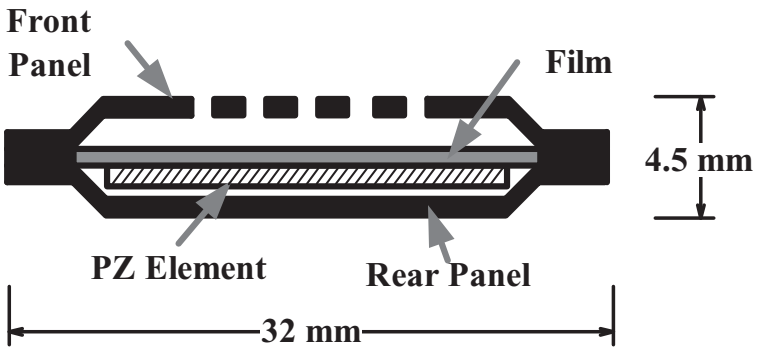

Figure 2.5: PZ speaker physical structure side view.

The PZ element in the speaker is typically a multilayer ceramic component that behaves electrically as a capacitor across the audio frequency bandwidth [19]. Fig. 2.6 shows the measured impedance versus frequency of a typical PZ speaker in comparison to the EM speaker impedance. It can be observed that for most of the audio frequency spectrum, the PZ speaker has an impedance orders of magnitude larger than the EM speaker impedance. This allows the audio amplifier to use very low power to operate the speaker, improving the battery life of mobile devices.

The capacitive behavior of the PZ speaker is highly reactive, meaning that the energy applied to the transducer is stored and most of it is returned to the supply each signal cycle. Ideally, this will allow almost no average power consumption from the battery, but the PZ speaker has some dielectric losses in the ceramic material that will dissipate some power as heat. Typical dissipation factors range from 0.4% up to 1% with quality factors > 50 for most PZ speakers available.

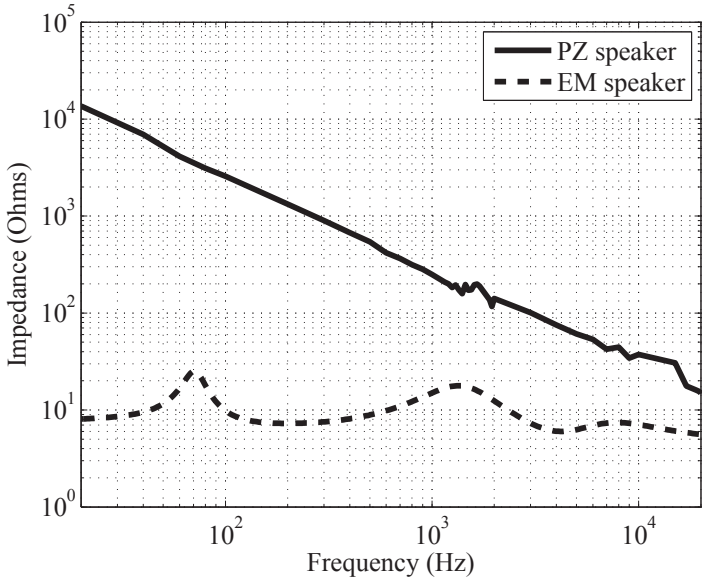

Figure 2.6: PZ and EM speakers impedance versus frequency comparison.

The following example will illustrate the PZ speaker's low power consumption. To produce the same 90 dB of SPL from the PZ speaker with a 338 Ω equivalent impedance at 1 kHz and dissipation factor of 1%, the battery only needs to provide 1.2 mW of average power or 133 μA of load current, as will be detailed in Section 5. If the same lithium-ion battery with 2000 mA/h capacity is used solely for the audio amplifier driving the PZ speaker, the battery life calculated using (2.3) would be 15,000 hours. That is a battery life extension of 2645x times compared to the EM speaker. However, in real applications, the audio amplifier current consumption would be dominant, limiting the battery life. If the amplifier has a current consumption of 2.46 mA, the real battery life would be 770 hrs. The PZ speaker provides low power consumption and high SPL, making it an attractive alternative for mobile devices, especially when used with low power high efficiency audio amplifiers.

Typical voltage levels across the PZ speaker terminals should be in the range of 10-20 V_{pp} to achieve the maximum SPL, and could be generated from the battery using high-efficiency step-up voltage circuits [20, 21, 22]. Commercial audio amplifiers for PZ speakers provide high-voltage outputs using these circuits, but their distortion and power consumption is still large [23, 24, 25, 26]. Thus, new circuits for PZ speakers that dissipate less power and produce less distortion are desirable. Section 5 introduces a new audio amplifier for PZ speakers that addresses these issues.

2.3 Performance metrics of audio amplifiers

To determine the quality of an amplifier, it is necessary to understand the main performance metrics in the audio amplification process. The metrics will be used in each proposed work throughout this dissertation to compare the obtained results with the state-of-the-art. The most used signal to measure these metrics is a sinusoidal waveform, typically at 1 kHz.

This is because a sinewave behaves as a single tone in the frequency domain, and its frequency harmonics up to the 20th harmonic are within the audio frequency band. Thus, they are easy to identify and use for various performance metrics.

2.3.1 Total harmonic distortion plus noise

The total harmonic distortion plus noise (THD+N) metric measures the amount of distortion that is generated by the amplification process compared with the fundamental input frequency, including the total noise produced by the amplifier. The THD+N is defined as the ratio of the fundamental frequency power to the sum of the harmonics power plus noise power as,

$$THD+N = \sqrt{\sum_{i=2}^{N} \frac{V_i^2}{V_1} + \frac{V_n^2}{V_1}} \tag{2.4}$$

where V_i is the RMS voltage of the nth harmonic, V_n is the integrated noise RMS voltage in the bandwidth of interest, and V_1 is the fundamental frequency RMS voltage. If the noise is not accounted and only the linearity is of interest, then a total harmonic distortion (THD) calculation can be used as,

$$THD = \sqrt{\sum_{i=2}^{N} \frac{V_i^2}{V_1}}. \tag{2.5}$$

The THD+N metric is the most accepted definition for audio quality of the system since real amplifiers will have noise that is not accounted in the THD metric. For example, for different amplifiers that have the same THD but they operate at different power levels, a large V_1 would reduce the effect of V_n in the THD+N; but for a small V_1, the contribution of V_n is larger, increasing the THD+N, as observed in (2.4). Thus, using the THD metric to compare amplifiers with different output power levels would be unfair.

The THD+N is typically measured against a sweep of output amplitudes for a single signal frequency, or for a sweep of frequencies from 20 Hz to 20 kHz for a single output amplitude. Since the THD+N varies several orders of magnitudes, the measured value can be expressed in logarithmic scale or percentage as expressed in table 2.2.

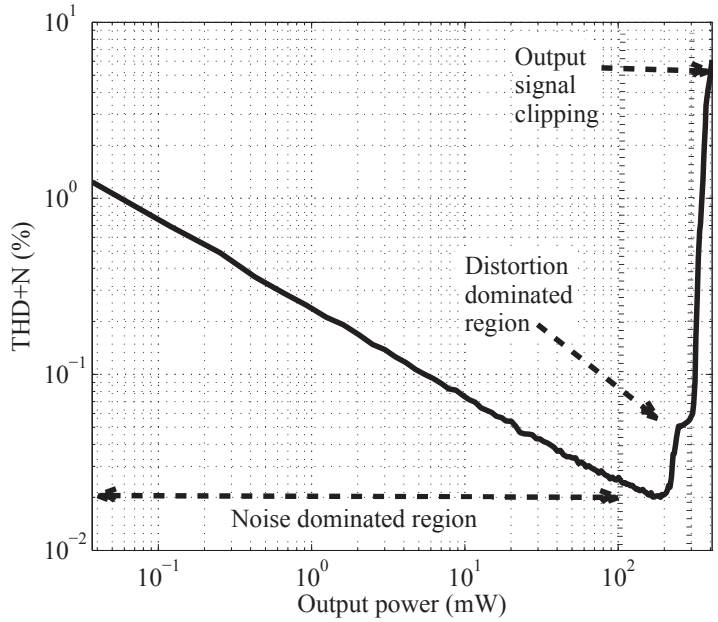

Figure 2.7: THD+N typical plot against output power for audio amplifiers.

Table 2.2: THD+N measurement units

Decibel (dB)	Percentage (%)
0	100 %
-20	10 %
-40	1 %
-60	0.1 %
-80	0.01 %
-100	0.001 %

A typical THD+N plot against the output power for a 1 kHz signal is illustrated in Fig. 2.7, where 3 regions can be identified. The first region is at low output powers where the THD+N value is dominated by the noise of the circuit. The second region is at medium to high output power where the THD+N value is dominated by the distortion of the output signal. The third region is when the output signal amplitude reaches the supply voltage value and it starts to clip, increasing the distortion drastically as observed in Fig. 2.7.

Other frequency tones can be used to compare the THD+N of an audio amplifier for a fixed output amplitude. A special case is for a 6.6 kHz input signal since the output THD+N would be dominated by the third harmonic (V_3=19.8 kHz) that is at the high limit of the audio frequency spectrum. This test signal gives the worst case scenario THD+N number of the amplifier. Typical THD+N values for commercial audio amplifiers in mobile devices range from -65 dB to -110 dB.

2.3.2 Signal to noise ratio

The signal to noise ratio (SNR) is a metric that defines the ratio of the signal power to the noise power of the amplifier. Noise sources come from the power supply hum (60 Hz), switching noise, thermal noise from the circuit components in the amplifier, and radio frequency interference. The audio amplifier noise floor integrated over the audio frequency spectrum is typically used for the measurement. The SNR can be expressed as,

$$SNR = 10\log\frac{P_o}{P_n} \cong 20\log\frac{V_o}{V_n} \tag{2.6}$$

where V_o is the output voltage amplitude of the fundamental frequency of the audio signal, and V_n is the integrated output noise of the amplifier. Fig. 2.8 shows a typical frequency spectrum for an audio amplifier where the noise floor and the signal harmonics can be observed. The noise floor is obtained by measuring the output of the audio amplifier with no audio signal.

2.3.3 Power supply rejection ratio

The power supply rejection ratio (PSRR) is a metric that defines the ratio between the output signal to the noise signal introduced by the supply of the amplifier. This metric is important since battery-powered devices share the audio amplifier's power supply plane with the same noisy power supply plane of digital circuits. The supply noise mixes with the audio and carrier signals, degrading the overall THD+N performance. Moreover, the supply noise rejection needs to be high over the whole audio frequency spectrum, to avoid a degradation of the THD+N. Since the supply noise could be orders of magnitude smaller than the output signal, the PSRR is typically expressed in decibels as,

$$PSRR = 20\log\frac{V_n}{V_o} = 20\log V_n - 20\log V_o. \tag{2.7}$$

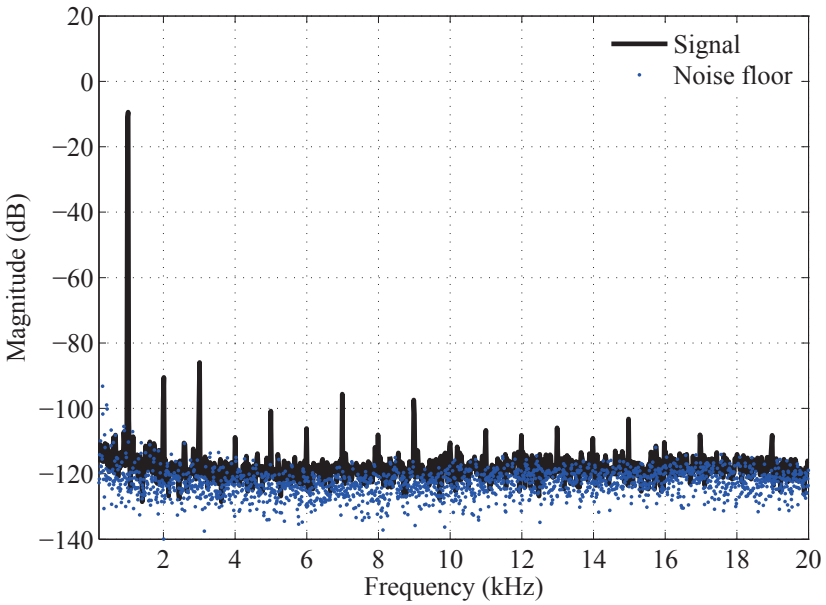

Figure 2.8: Typical output frequency spectrum for audio amplifiers.

This metric is measured when there is no audio signal present (idle condition) and the noise signal is swept across the audio frequency spectrum. A special case is for the noise signal at 217 Hz; this tone is especially important for audio amplifiers in cell phone devices since it represents the GSM burst used for the device communication. Therefore, if the audio amplifier is intended for a cell phone application, it must have a high PSRR performance also at low frequencies.

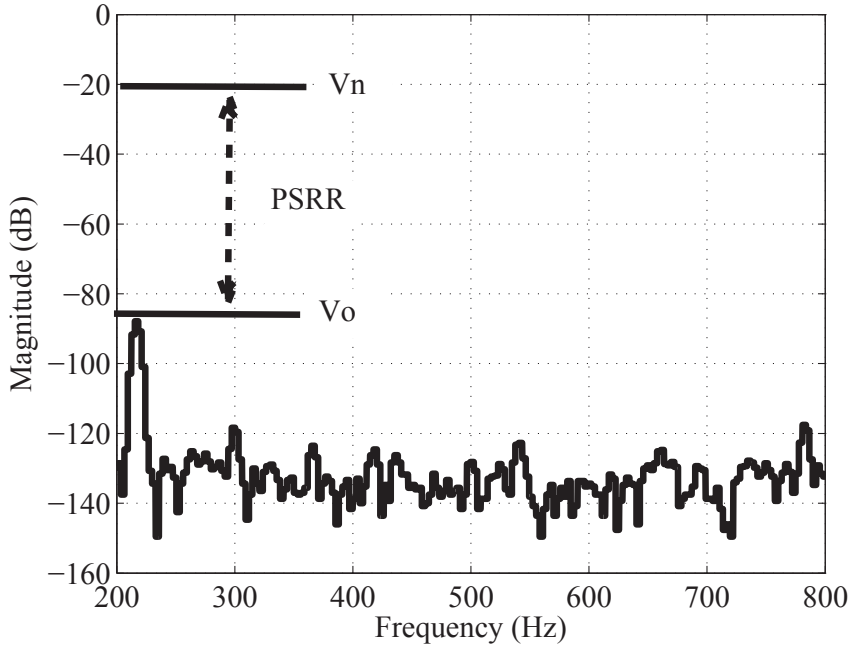

Figure 2.9: PSRR measurement example for a noise signal at 217 Hz with -20 dB amplitude.

Fig. 2.9 illustrates a sample PSRR measurement where an input -20 dB tone signal at 217 Hz is applied to the amplifier, and the output signal frequency spectrum is used to extract the signal output, supply noise, and PSRR values.

Since the plot shows the value in logarithmic scale, the PSRR is the difference between the Vo and Vn in decibels that for this example is around 65 dB. The PSRR performance of the audio amplifier is highly dependent on the topology of the amplifier and the output stage connecting the battery supply to the output.

2.3.4 Power supply intermodulation distortion

The PSRR metric characterizes the supply noise rejection at the idle condition when no audio signal is present. However, during normal operation, the supply noise and the audio signal are present in the amplifier. The power supply intermodulation distortion (PS-IMD) measures the interaction between the noise and audio signals. The PS-IMD is the amplitude modulation between noise and audio signals at different frequencies. The intermodulation products occur since all amplifiers are non-linear circuits that generate harmonics, and they are located at multiples of the sum and difference frequencies of the audio and noise signal frequencies.

The PS-IMD can be measured from the frequency spectrum of the output signal, as show in Fig. 2.10, where an audio signal at 1 kHz and a noise signal at 217 Hz generate two dominant intermodulation products at 783 Hz and 1217 Hz. The PS-IMD can be expressed as the magnitude ratio between the intermodulation products to the fundamental as,

$$PS-IMD = 20\log\frac{V_o}{V_{IMD}} = 20\log V_o - 20\log V_{IMD} \tag{2.8}$$

where V_{IMD} is the intermodulation product amplitude, and V_o is the fundamental audio signal amplitude. The PS-IMD metric is highly correlated with the linearity of the system and its PSRR performance. If the amplifier has poor PSRR and high distortion, then the PS-IMD will be poor.

2.3.5 Power efficiency

One of the most important metrics for audio amplifiers in mobile devices is the power efficiency (η). This metric represents how much of the energy provided by the battery is effectively used for the intended purpose of audio amplification. In other words, if the audio amplifier consumes/dissipates power due to its biasing or power loss, then the efficiency will be less than 100 %.

The power efficiency is typically estimated as the output power divided by the input (supply) power, using the average power definition over a sinewave signal period ($T = 2\pi/\omega$) as,

$$P_{avg} = \frac{1}{T}\int_0^T v(t)\cdot i(t)\cdot dt = V_{RMS}\cdot I_{RMS}\cdot\cos(\varphi) \tag{2.9}$$

where the phase angle between the current relative to the voltage is represented by φ.

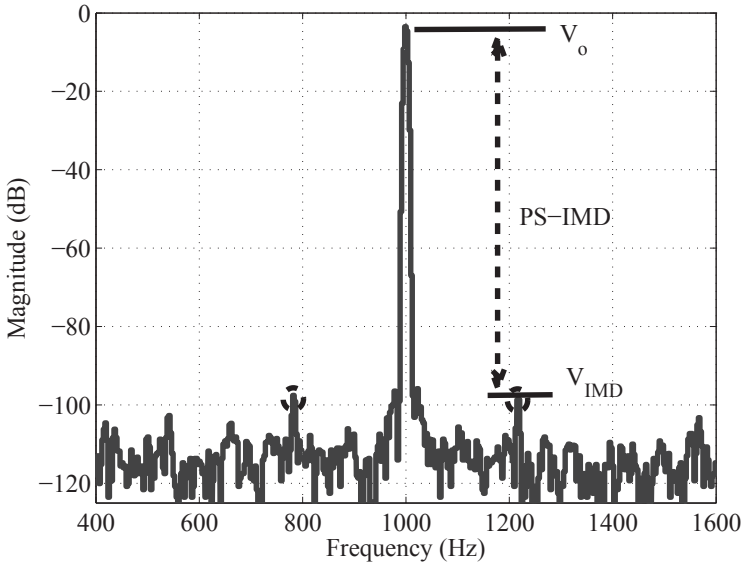

Figure 2.10: PS-IMD measurement example for a noise signal at 217 Hz and audio signal at 1 kHz.

For an EM speaker, the load appears as almost resistive, and the term $\cos(\varphi)$ in the output power is close to one, meaning that the voltage and current are in phase, and the power is being dissipated in the load, as observed in the average power in Fig. 2.11. Therefore, the power efficiency for EM speakers could be defined as [27],

$$\eta = \frac{P_{o,avg}}{P_{i,avg}} = \frac{P_{o,avg}}{P_{o,avg} + P_{loss,avg}} = 1 - \frac{P_{loss,avg}}{P_{i,avg}} \tag{2.10}$$

where the $P_{o,avg}$ is the average output power delivered to the load, $P_{i,avg}$ is the average input power consumed from the battery, and $P_{loss,avg}$ is the average power loss in the audio amplifier. In general, most of the audio amplifier applications are targeted for EM speakers; thus, this efficiency definition is typically used.

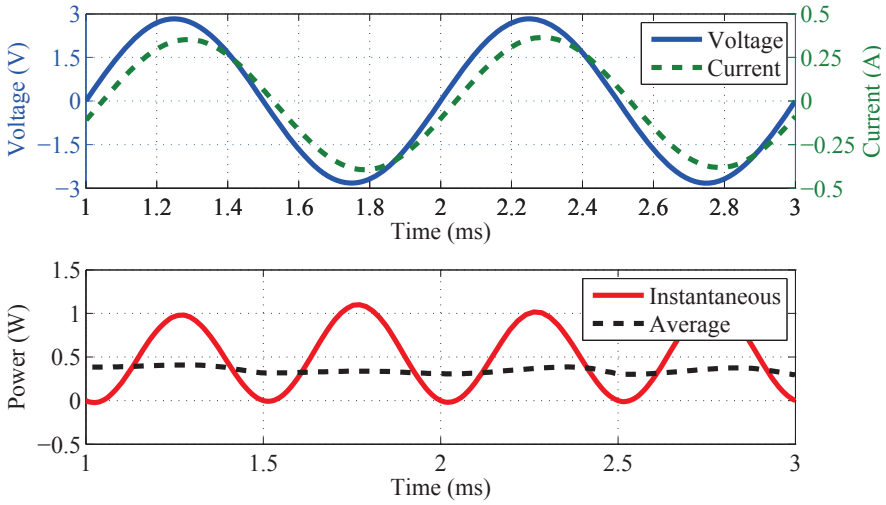

Figure 2.11: Instantaneous and average power for a EM speaker with $\varphi < 15°$.

The PZ speaker is a highly reactive speaker alternative that offers very low power consumption, as discussed in Section 2.2.2.

Its capacitive nature needs a different definition of power efficiency since the current leads the voltage by almost 90 degrees, causing the term $\cos(\varphi)$ to be close to zero, and appearing as if very little power is being dissipated by the load, as observed in the average power in Fig. 2.12. This happens because the energy supplied by the battery is stored in the reactive load and returned to the battery each cycle. If the average output power is used for the efficiency definition in (2.10), the efficiency will appear very low [28].

Another alternative is to define the efficiency in terms of energy transfer between the supply and load [29, 30]. However, the energy analysis requires an estimation of the energy for each switching cycle, making it a complex procedure. A more suitable definition of the amplifier's power efficiency for capacitive transducers has been proposed in [31, 32, 33], where the apparent power is used for the efficiency calculation.

The apparent power, measured as $P_{app} = V_{RMS} \cdot I_{RMS}$, is the magnitude of the complex power vector which contains the information of the reactive power and the average or real power, as observed in Fig. 2.13. The complex power is the general representation for the

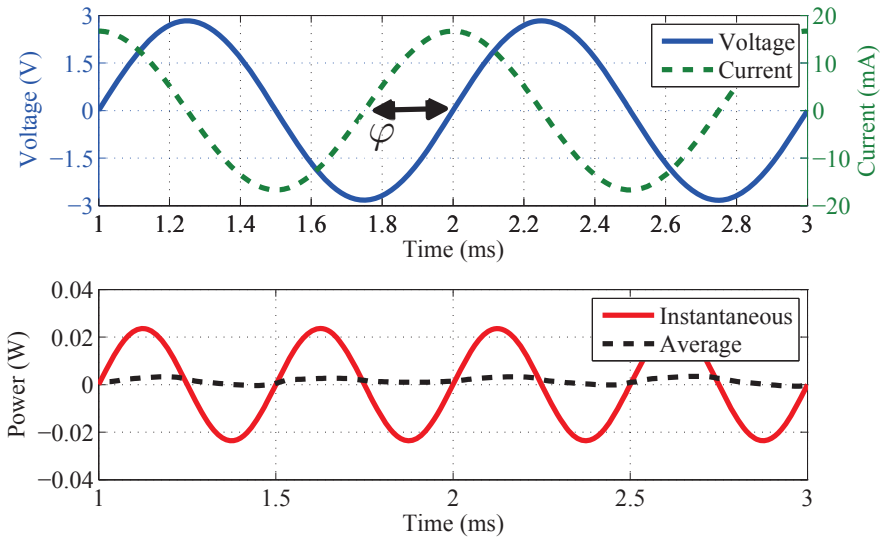

Figure 2.12: Instantaneous and average power for a PZ speaker with $\varphi \cong 90°$.

voltage and current product, and it can be expressed as,

$$\vec{P}_{comp} = \vec{P}_{av} + \vec{P}_{reac} = \vec{P}_{comp}\cos\varphi + \vec{P}_{comp}\sin\varphi. \tag{2.11}$$

Thus, the amplifier's power efficiency for capacitive loads is defined as [32, 33, 31],

$$\eta_{PZ} = \frac{P_{o,app}}{P_{i,app}} = \frac{P_{o,app}}{P_{o,app} + P_{loss,app}} = \frac{1}{1 - \dfrac{P_{loss,app}}{P_{o,app}}} \tag{2.12}$$

$$P_{o,app} = V_{o,RMS} \cdot I_{o,RMS} \cong \frac{V_{o,RMS}^2}{|Z_L(j\omega)|} \tag{2.13}$$

where $Z_L(j\omega)$ is the equivalent impedance of the PZ speaker at the operating frequency. This efficiency definition states that the amplifier has to process the apparent power required by the PZ speaker with the minimum power dissipation. In other words, the average input power reflects the power dissipation of the system. This is important since the audio amplifier has to be designed for a large capacitive load with low power dissipation. More details about the amplifier design for PZ speakers and its efficiency is addressed on Section 5.

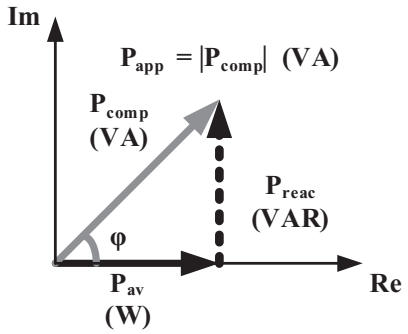

Figure 2.13: Complex power definition.

2.4 Audio amplifier classification

The audio amplifier can process the audio signal as a linear operation continuously in time and amplitude, or as a non-linear operation continuously in time but discretely in amplitude. The linear audio amplifiers process the signal with an output stage configured as a current source, while the non-linear audio amplifiers have a switching output stage that process the signal with a modulation scheme.

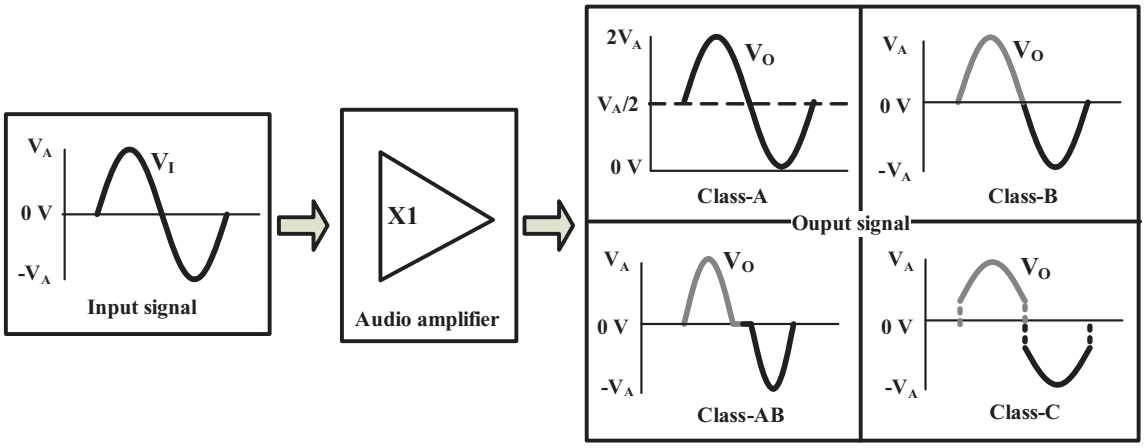

Figure 2.14: Main linear amplification classes.

The main linear amplification classes are summarized in Fig. 2.14. The audio amplifier is typically configured as a voltage follower with enough output current to drive the impedance of the speaker. The main amplifier linear classes are the class-A, class-B, class-AB, and class-C. The linear amplifiers' biasing point defines the range of the input signal that they can amplify at the output with a tradeoff between linearity and power dissipation.

The class-A amplifier outputs 100% of the signal swing, providing minimum distortion; but, its output stage biasing point is placed at half the maximum amplitude of the signal, dissipating large power.

The class-B amplifier's biasing point is chosen to output only 50% of the signal swing; the small biasing point decreases the power consumption, but at the expense of large distortion. The class-AB operation combines the reduced power dissipation and low distortion of the class-B and class-A, respectively; but, it requires a complex biasing scheme to operate [34, 35]. The class-C amplifier's biasing point is chosen to output less than 50% of the output swing to lower the power dissipation drastically; however, its high distortion prohibits its use for audio applications.

Other more advanced amplifier classes have been proposed to increase the power efficiency of linear amplifiers such as the class-G and class-H. The class-G amplifier provides better power efficiency compared with the class-AB operation [36, 37, 38]. The efficiency improvement is achieved by reducing the supply voltage for smaller output signals, and thus, reducing the power dissipation. The power-supply transition is achieved without affecting the dynamic range of the output signal, as observed in Fig. 2.15. However, the distortion during the supply transition can be detrimental in the performance of the amplifier. The detailed class-G operation and a case study to minimize the supply-transition distortion are presented in Appendix A.

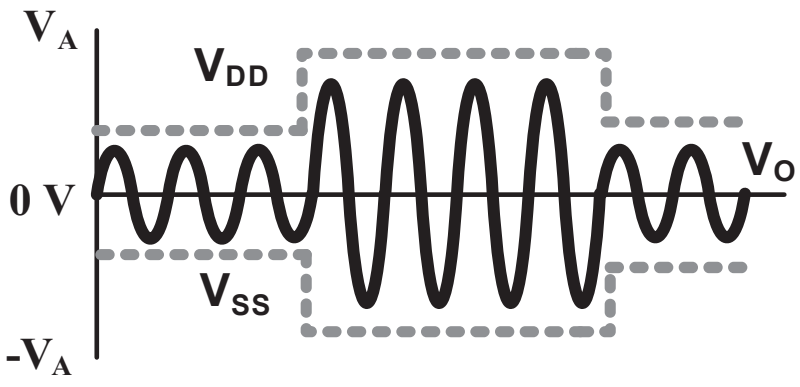

Figure 2.15: Class-G amplifier operation.

The class-H amplifier operates in a similar way as the class-G amplifier by continuously changing the supply voltages as observed in Fig. 2.16. The smooth supply transitions allow very low distortion and improved efficiency in the amplification process since the supply is high only when needed by the signal. However, a dedicated power management circuit is required to adapt the supply voltages according to the input signal, degrading the overall efficiency benefits, and increasing the cost and power consumption of the audio amplifier.

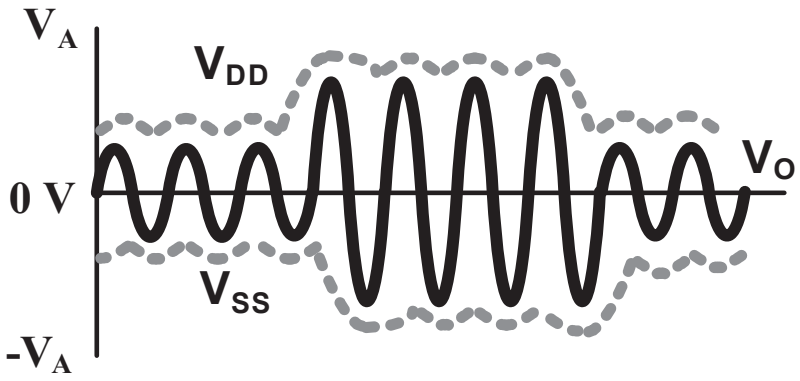

Figure 2.16: Class-H amplifier operation.

The class-G and class-H amplifiers improve the power efficiency of the amplifier by switching the supply voltage for different levels of output signal. However, the biasing's power dissipation still exist during the amplification process. Another alternative is to keep a fixed supply voltage but switch the output signal between the supply voltages to operate the output stage as a digital switch. This operation is known as a class-D operation, where the continuous input signal is modulated by a high frequency carrier that generates a stream of pulses that are applied to the load, as observed in Fig. 2.17.

The class-D operation can be better understood by looking at the output frequency spectrum of the modulated signal, as shown in Fig. 2.18; the frequency spectrum has the audio fundamental frequency (ω_o) and its harmonics ($n\omega_o$) plus the modulation carrier signal frequency (ω_{SW}) located at higher frequencies out of the audio band. The harmonics are generated since the non-ideal modulator and limited slew rate in the output stage distort the signal.

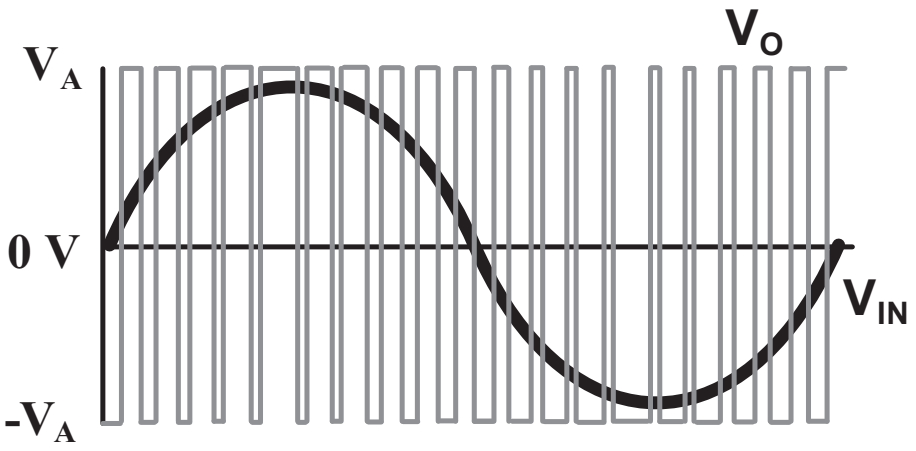

Figure 2.17: Class-D amplifier operation, time domain.

The low frequency components of the modulated output signal represents the desired audio information. Thus, a passive low pass filter is used to recover the audio signal information at the speaker. This output filter is implemented with an inductor and capacitor to avoid degrading the efficiency. The typical cut-off frequency for the output filter is 20 kHz to include the whole audio frequency band.

The advantage of this discontinuous operation of the class-D amplifier compared to the conventional amplifier classes is that ideally there is no power dissipation in the amplifier since the output stage is either on or off.

In other words, there is no quiescent power; when the output current is high, the ideal switch does not dissipate power since its resistance is zero. Therefore, the efficiency can be 100%, meaning that all the power from the supply is delivered to the speaker. In reality, maximum efficiency is limited by the finite switch resistance in the output stage, the output filter components power loss, the amplifier quiescent power, and the output stage capacitive power loss. The class-D amplifier is the focus of this dissertation due to its high power efficiency. Its operation, advantages, and disadvantages will be discussed with more detail in Section 3.

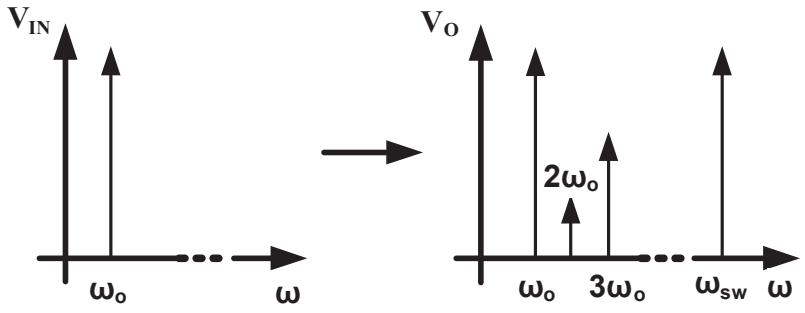

Figure 2.18: Class-D amplifier operation, frequency domain.

3. PRINCIPLES OF CLASS-D AUDIO AMPLIFIERS

3.1 Class-D amplification

The class-D amplifier (CDA), also know as digital power amplifier or switching amplifier, is an electronic device which takes an input voltage signal, either in analog or digital domain, and amplifies it using an output stage operating as a digital inverter. The main advantages of the class-D amplification are its high efficiency and its robust digital output signal.

The class-D output stage operation is as follows. If the input signal is in analog domain, the audio signal is typically modulated by a high-frequency carrier signal to obtain a pulse width modulation (PWM) and then it is amplified by the class-D output stage. Fig. 3.1 shows a single-ended open loop CDA for analog inputs, where the high-frequency carrier signal (V_C) is used to achieve the PWM of a low-frequency input signal (V_I).

If the input signal is in digital domain expressed as a bit stream of n=8 up to n=48 bits, the input digital signal vector ($D_I\ [0:(n-1)]$) is typically transformed from a pulse-code modulation (PCM) to PWM using a digital block that perform some signal processing and data rate reduction using the data clock signal (D_{CLK}), as observed in Fig. 3.2. The PCM uses a unique digital code while the PWM uses a unique pulse width to represent an output voltage level, as illustrated in Fig. 3.3. Typical PCM digital vectors are of 16 bits or ($D_I\ [0:15]$), requiring a complex and precise digital circuit to translate the information to a PWM signal.

The modulated signal (V_{PWM}) is used to switch the output power transistors between the voltage rails with high efficiency. Finally, an output low-pass filter is used to recover the low-frequency signal and apply it to the speaker.

Typical operating frequencies for the CDA in audio applications are 20 Hz - 20 kHz for the input and output signals, and 200 kHz - 400 kHz for the carrier and PWM signals.

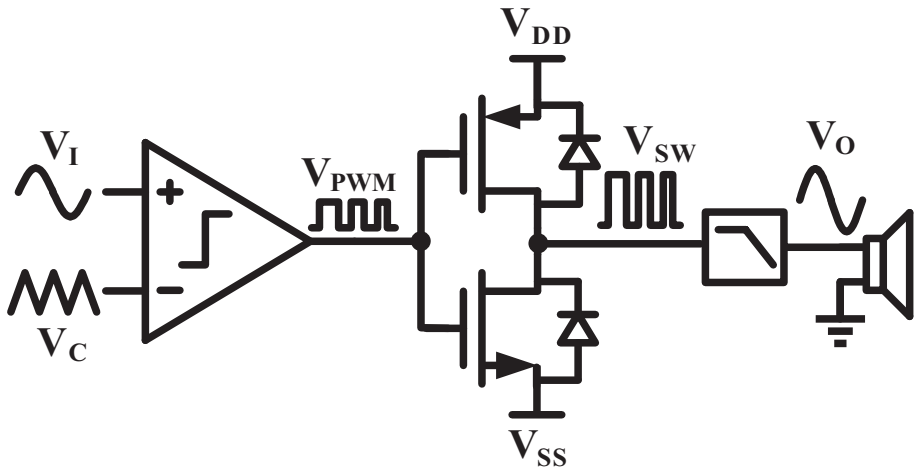

Figure 3.1: Analog class-D amplifier in single-ended open-loop architecture.

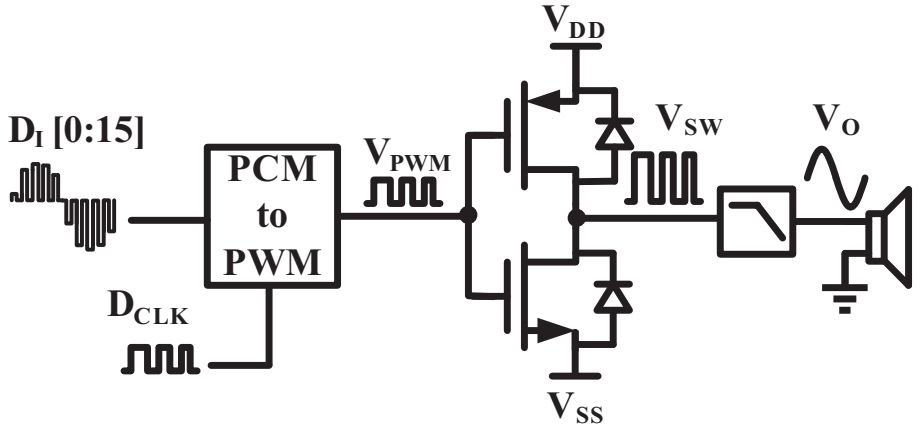

Figure 3.2: Digital class-D amplifier in single-ended open-loop architecture.

The audio information in mobile devices is processed in digital domain, making it more convenient to use the raw digital information as the input of the CDA. However, the digital input CDA is typically used in open loop architectures, requiring complex signal processing and calibration algorithms to achieve high performance. On the other hand, the analog input CDA can be used with a feedback mechanism that helps to correct distortion, noise, and enhance the audio performance in general, allowing low power operation.

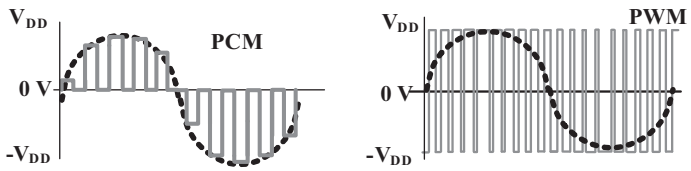

Figure 3.3: PCM and PWM comparison.

The only drawback is that it needs a digital-to-analog converter (DAC) to transform the digital input signal to analog domain in order to amplify it. The analog input CDA is the preferred choice for class-D amplification in mobile devices due to its low power operation, and is the focus of this dissertation. Thus, all the following discussion is referred to analog input class-D audio amplifiers.

It is important to notice that the output stage of the CDA, as shown in Fig. 3.1, is very similar to the output stage of a step-down DC-DC Buck converter [39, 40, 41]. The main difference is that the goal in a Buck converter is to regulate the output voltage as a constant DC voltage source under different load conditions, where the voltage V_I is a constant voltage reference, and the duty cycle of V_{PWM} is proportional to the desired output voltage. Also, the output filter is designed to reduce the voltage ripple at the output. Thus, all the modulation and design techniques discussed in this dissertation could be applied to the DC-DC Buck converter.

3.1.1 Advantages and disadvantages of class-D amplifiers

The main advantage of the class-D amplification is its high efficiency and low power dissipation that allow extended battery life in mobile devices. The output stage in CDAs is typically implemented using CMOS transistors operating as switches. When the switch is open, they appear as very high resistor ($> 1M\Omega$), having an ideal zero power dissipation since no current is flowing through them; when the switch is closed, they appear as very low resistor ($< 0.1\Omega$), having an ideal zero power dissipation since there is no voltage drop across them. This operation allows low power dissipation in the switch. Thus, the heat sink typically used in other amplifier classes can be drastically reduced or completely removed, and their low power dissipation allows very high efficiency.

One of the disadvantages of the class-D amplification is that its output signal is a squarewave at full power that needs to be removed before applying it to the speakers. This requires an output filter with external components that occupy PCB area and increase the bill-of-materials of the amplifier. However, complex techniques can be used to minimize the output filter requirements with switching strategies that provide multi-level output signals [42, 43].

Another disadvantage for the CDA is the electromagnetic interference (EMI) radiated by the inductance of the cables and/or PCB traces connecting the CDA with the speaker [44]. This is particularly important in mobile devices since most of the circuits are placed closely. Thus, sensitive analog circuits such as analog-to-digital converters, radio frequency receivers, and voltage or current references can be drastically affected by the EMI. Several techniques to improve the EMI can be used to spread the energy of the high-frequency carrier signal used in PWM modulation such as spread spectrum or edge-rate control, at the expense of additional power consumption and design complexity [45, 46].

3.1.2 Class-D amplifier power losses

The ideal CDA can reach 100 % efficiency. However, the CDA power losses due to its implementation will limit the maximum efficiency. A comprehensive analysis for the power losses in switching power stages can be found extensively in the literature [47, 27, 48, 49, 50]. The efficiency in the class-D amplifier is defined as,

$$\eta = \frac{P_o}{P_o + P_{loss}} \tag{3.1}$$

$$P_{loss} = P_Q + P_{CL} + P_{SW} + P_{BD} \tag{3.2}$$

where the power losses in the CDA (P_{loss}) is mainly dominated by the amplifier quiescent power (P_Q), the conduction losses (P_{CL}), switching losses (P_{SW}) and body-diode losses (P_{BD}) of the output stage.

Conduction losses occur due to the ohmic losses of the output switches' drain to source ON resistance (R_{dsON}) and are more prominent when the current demanded by the load is large. Switching losses occur due to the power dissipated by the charging and discharging of parasitic capacitors, especially in the output stage. Body-diode losses occur due to the body-diode conduction and its reverse recovery charge that could be considerable for large output currents. These power losses can be expressed as,

$$P_{CL} \cong I_{o,RMS}^2 \cdot R_{dsON} \tag{3.3}$$

$$P_{SW} \cong \sum_i F_{SW} \cdot V_{CP}^2 \cdot C_{P,i} \tag{3.4}$$

$$P_{BD} \cong V_{SD} \cdot F_{SW} \cdot (I_{o,PK} \cdot t_{deadtime} + I_{rrm} \cdot t_{rr}) \tag{3.5}$$

where $I_{o,RMS}$ is the output RMS current, F_{SW} is the CDA switching frequency, $C_{P,i}$ are the parasitic capacitors in the output stage, V_{CP} is the voltage across each $C_{P,i}$, V_{SD} is the body-

diode source-to-drain voltage, $I_{o,PK}$ is the peak output current, $t_{deadtime}$ is the deadtime used to avoid shoot-through current, I_{rrm} is the body-diode maximum reverse recovery current, and t_{rr} is the body-diode reverse recovery time.

The CDA efficiency can be characterized in three regions across its operating output power, as observed in Fig. 3.4 where the a sample efficiency versus output power plot is shown. It can be observed that at low power levels (region I), the P_{loss} is dominated by P_{SW} and P_Q; at medium power levels (region II), all the components of P_{loss} contribute to the total; and, at high power levels (region III), the P_{loss} is dominated by P_{BD} and P_{CL} since the output current is large.

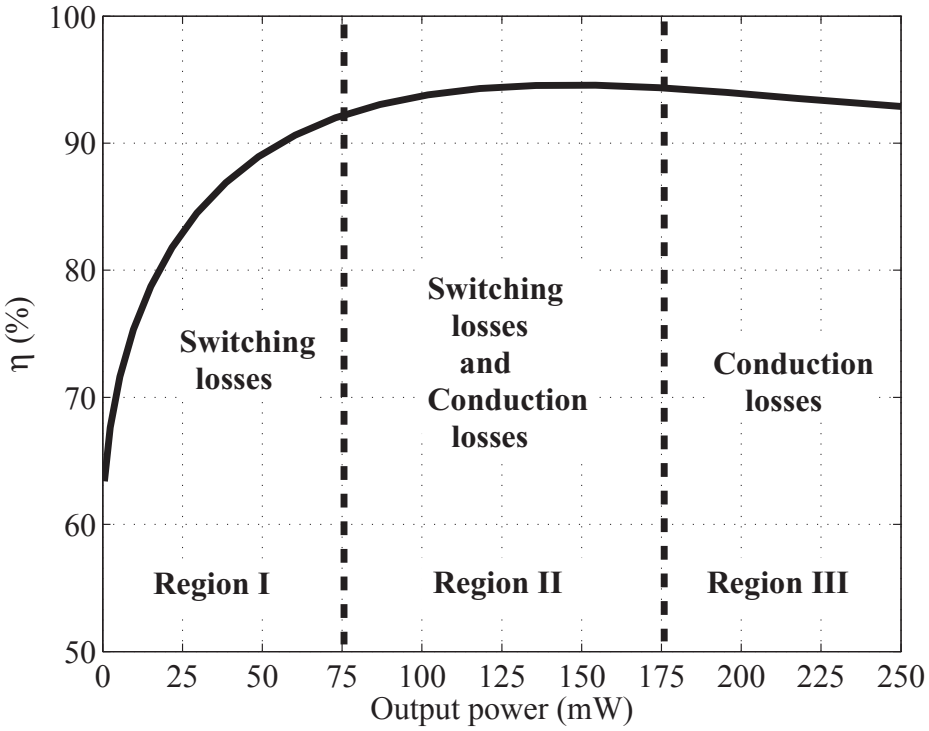

Figure 3.4: Efficiency versus output power example for a class-D amplifier, showing power losses dominated region.

The output stage is designed to minimize the power losses in a particular operating region; different optimizations will result in different efficiency curves, as depicted in Fig. 3.5. The peak in each curve is the result of the optimized output stage to minimize the power losses in the region of interest for the desired application. The main goal in high power CDA applications is to improve the efficiency in region II and III since they require low power dissipation for reduced size and weight. The main goal in low power CDA applications is to improve the efficiency in regions I and II to extend the battery life.

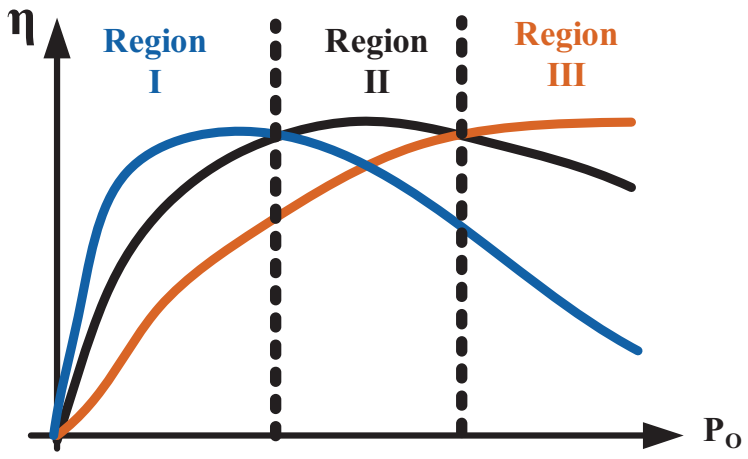

Figure 3.5: Efficiency curves for different output stage optimizations.

Different audio transducers will influence the impact of each power loss to the efficiency. Fig. 3.6 and Fig. 3.7 illustrate the output stage of the CDA when driving the electrical models of an EM speaker or a PZ speaker, respectively. The main contributors of P_{SW} are the input and output capacitances ($C_{P,i}$) of the output stage that can be large if the switches are sized to obtain small R_{dsON}. However, a large transistor switch will have a large body-diode, increasing the contribution of P_{BD} to the total power losses, and limiting the maximum efficiency.

The advantage of using the PZ speaker is that its high impedance requires small current to operate, minimizing the impact of P_{CL} in the efficiency. This would allow smaller output switches to obtain the same P_{CL} but will decrease the P_{SW}, enhancing the overall efficiency. Moreover, the small output current together with a short $t_{deadtime}$ will reduce the P_{BD} contribution to the total power losses.

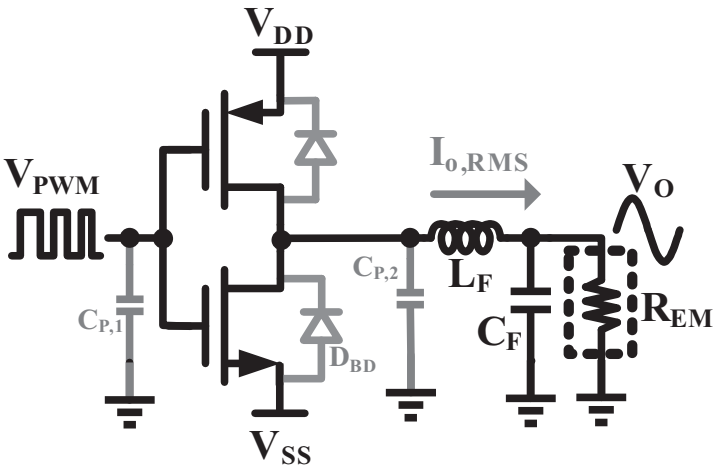

Figure 3.6: Class-D output stage driving an EM speaker load.

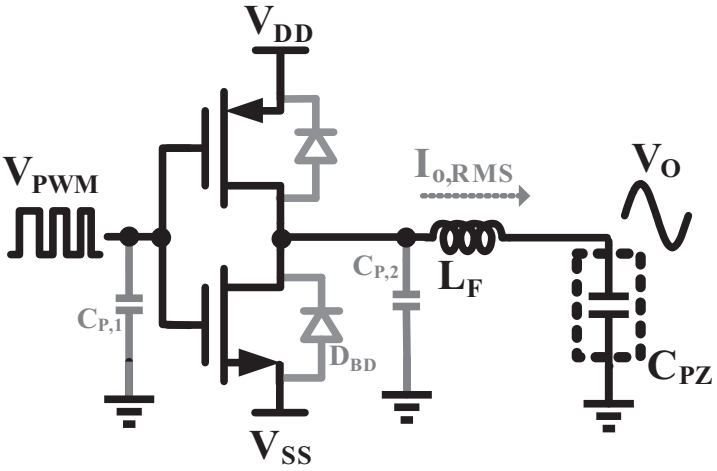

Figure 3.7: Class-D output stage driving a PZ speaker load.

3.1.3 Typical applications

The high power efficiency of class-D amplifiers makes them suitable for a wide range of applications such as boom boxes or portable stereo systems, portable video players, hearing aids, notebook computers, tablet computers, smart phones, etc. The characteristic low power dissipation in the CDA extends their applications to audio systems that are not battery powered but where reduced weight and size are important. These applications are speaker systems for amusement parks, stadiums, home theater, televisions, car audio, etc.

The CDA applications can be broadly classified in two categories: 1) low power applications targeted for battery-powered portable devices, and 2) medium to high power applications targeted for reduced heat dissipation audio systems. The low power applications require output powers less than 3 W, and their main focus is high power efficiency ($\eta > 90\%$) and high linearity ($THD+N < 0.1\%$). The medium to high power applications require output powers from 10 W up to 3600 W with small heat sinks and compact size, and their main focus is high efficiency ($\eta > 70\%$), and reduced weight and size.

For the purpose of this dissertation, the CDA low power applications will be targeted since they are more compatible to the semiconductor voltage limits in integrated circuits. However, the principles and theory that will be discussed can be applied to all class-D amplifiers in general, and the proposed solutions can be extrapolated to high power applications if needed.

3.1.4 Commercial class-D audio amplifiers typical specifications

To understand the trends in class-D audio amplifiers for mobile devices, state-of-the-art commercial CDA specifications are shown in table 3.1. It can be observed that the specification for supply voltage corresponds to the battery maximum supply voltage; for the lithium-ion batteries used in mobile devices, the standard voltage ranges from 4.8 V to 2.7 V.

Table 3.1: Typical specifications for commercial class-D audio amplifiers

Parameter	[3]	[4]	[5]	[6]	[7]
Supply (V_{DD})	5	5	5	5	3.6
I_Q (mA)	7	1.42	6.5	4.2	2.7
P_Q (mW)	35	7.1	32.5	21	9.7
Efficiency(%)	85	90	85	90	85
THD+N (%)	0.65	0.02	0.02	0.08	0.01
$P_{o,max}$ (W)	1.2	1.7	1.4	1.7	2.3
PSRR (dB)	65	88	85	93	88
SNR (dB)	83	98	96	89	97
F_{SW} (kHz)	250	192	420	300	300

Another observation in terms of audio performance is that a THD+N smaller than 0.1 %, SNR higher than 80 dB, PSRR higher than 60 dB, and efficiency higher than 80 % are required to be competitive. The power dissipation is proportional to the maximum output power provided ($P_{o,max}$), but the smaller the quiescent power (P_Q), the longer the battery will last. Typical switching frequencies (F_{SW}) are in the range of 200 to 400 kHz.

3.2 Close loop class-D architectures

Open loop CDA architectures are cost effective and simple to implement, as shown in Fig. 3.1 and Fig. 3.2. However, the absence of error correction makes them too sensitive to variations in components, timing errors, and supply noise. The main applications that leverage the low power and simplicity of the open loop CDA are toys, smoke alarms, and buzzers. To achieve outstanding audio performance in a CDA, closed-loop architectures are typically used where the negative feedback mechanism helps to correct errors in the amplification process. The close loop transfer function is typically expressed as,

$$\frac{V_o(s)}{V_i(s)} = \frac{A_{ol}(s)}{1 + A_{ol}(s) \cdot \beta(s)} \cong \frac{A_{ol}(s)}{LG(s)} \cong \frac{1}{\beta(s)} \tag{3.6}$$

where the $A_{ol}(s)$ represents the open loop gain of the system, β is the feedback factor, and assuming that the close loop gain is large (e.g. $LG(s) = A_{ol}(s) \cdot \beta(s) \gg 1$). Two important aspects can be noticed from the feedback mechanism: 1) if the β factor is chosen as a linear gain, then the close loop system will have a linear behavior; 2) any non-linearity in $A_{ol}(s)$ will be attenuated by $LG(s)$.

The general structure for a close loop CDA is shown in Fig. 3.8 where the darker blocks comprise the close loop gain of the system. The $A_{ol}(s)$ is given by the small signal models of the compensator, modulator, and output stage. It can be noticed that the output filter and speaker are outside of the feedback loop. Thus, their errors and non-linearities would not be correct by the feedback. Also, the feedback signal is the switching signal of the class-D output stage, meaning that is a high frequency square wave at full swing with a high number of harmonics. Thus, the compensator, modulator, and class-D output stage have to process all the frequency harmonics of the feedback signal, increasing the design complexity of each block.

The general close loop CDA architecture operates as follows: the compensation's function is to extract and filter the error signal coming from the difference between the audio input signal and the feedback signal. Also, this block has to provide gain in the loop to attenuate distortion and errors at the output, and ensure stability in the system. The compensator is typically implemented using an integrator chain where the order of the compensator is proportional to the number of integrators in the chain. The modulator's function is to process the output of the compensator and implement the desired modulation scheme. The modulator output signal is then passed through a chain of digital inverters that increase their output drive with each stage. Finally, the output of the inverters have to charge and discharge the large gate capacitors of the class-D output switches to be able to turn them on or off. The output switching signal is then applied to the feedback factor and returned to the input of the compensator to complete the loop.

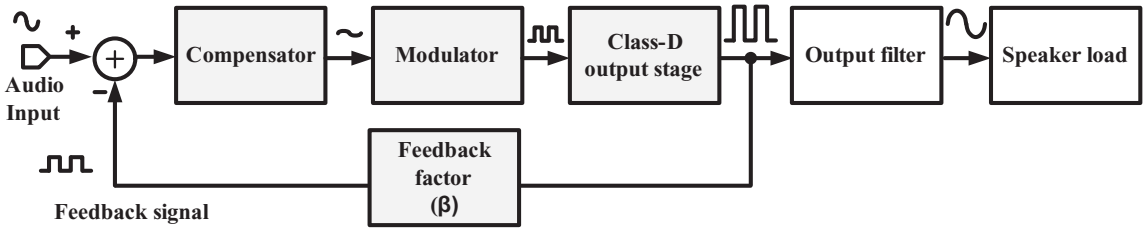

Figure 3.8: General close loop CDA architecture.

Another alternative for the feedback signal is shown in Fig. 3.9. The $A_{ol}(s)$ is given by the small signal models of the compensator, modulator, output stage, and output filter. This provides the advantage of including the output filter inside the feedback loop, correcting the non-linearities in the filter components. Also, the output filter removes the high frequency components of the feedback signal, leaving only the low frequency information of interest. This relaxes the design complexity of the compensator, modulator, and class-D

output stage. The main drawback is that the output filter typically has two poles, requiring a complex compensation scheme to make the system stable.

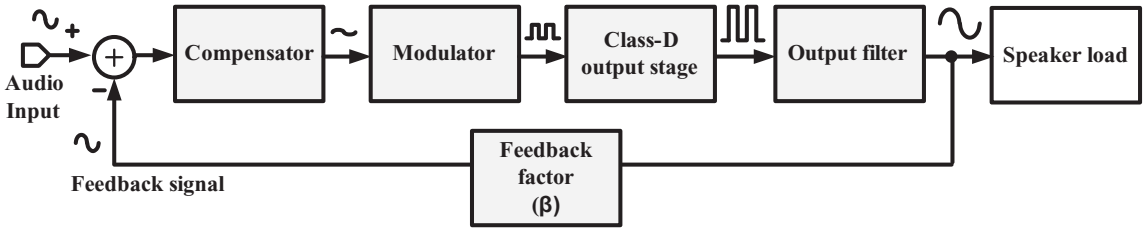

Figure 3.9: Close loop CDA architecture with alternative feedback, including output filter.

It is worth noticing that the closed-loop architecture in Fig. 3.9 is also used in the DC-DC Buck converter [41, 51]. However, the goal is to regulate the output voltage under large load transients to reduce the output voltage ripple, and using the compensator to stabilize the system with a fast transient response. Since the output signal is a constant voltage, the bandwidth of the loop is designed to react to the fastest load change, which in modern microprocessors could be in the range of tens of nanoseconds.

In some CDA for mobile devices where boosted supplies are needed to deliver more output power, the main purpose of β is to attenuate the high voltage swing of the output to make it compatible to the voltage level tolerable by the compensator. A common choice for this feedback factor is $\beta = 1$ since the compensator is also connected to the battery supply as well as the output stage. Another consideration for the feedback factor is that its errors or non-linearities will appear directly at the output, as expressed in (3.6). Thus, β is typically implemented as a linear resistive voltage divider.

One of the most important design choices for the close loop CDA architecture is the switching frequency F_{SW}, since its value affects directly the power dissipation of the system, as expressed in (3.2), and the linearity of the system. The Nyquist theorem [52]

establishes that the minimum sampling frequency needed to recover accurately a sampled input signal has to be at least 2 times the frequency bandwidth of the desired signal. For audio, the frequency bandwidth is 20 kHz. Therefore, the minimum sampling frequency to satisfy the Nyquist theorem is ideally 40 kHz. However, this condition does not take into account the non-idealities, such as finite slew-rate, of the implemented carrier signal or modulator. To avoid any intermodulation distortion caused by the aliasing of the carrier frequency and the audio signal high frequency components, a typical rule-of-thumb is to choose the F_{SW} at least 10 times larger than the desired bandwidth.

The general closed-loop CDA has been analyzed for intermodulation distortion (IMD) in time domain [53], and in frequency domain [54]. Moreover, the carrier distortion and its effect on the system has been analyzed in [55], and the effect of power-supply noise was analyzed in [56, 57, 58]. The agreement is that large loop gain and a high-frequency carrier in the system help to attenuate the distortion components and supply noise of the closed-loop system, improving the audio performance.

Different modulation schemes have been proposed for closed-loop CDA architectures to achieve high efficiency and good audio performance using modulation techniques such as PWM [8, 9, 42, 45, 46, 59, 60, 61], sigma-delta modulation (SDM) [62, 43], or self-oscillating modulation (SOM) [63, 64, 65]. Each modulation scheme has its advantages and disadvantages, depending on the implementation and application. A brief review for each of the main modulation techniques used in close loop CDA architectures is presented next.

3.2.1 Pulse width modulation

The closed loop PWM CDA architecture operates in a similar way as the open loop case shown in Fig. 3.10, where a high frequency carrier signal V_C is compared to a low frequency signal V_I to generate the modulated squarewave signal amplified by the class-D output stage V_{SW}. The difference is that a compensator block is added, as shown in Fig. 3.11, to correct the error (V_e) between the input and the feedback signal, and to provide gain and stability to the close loop system.

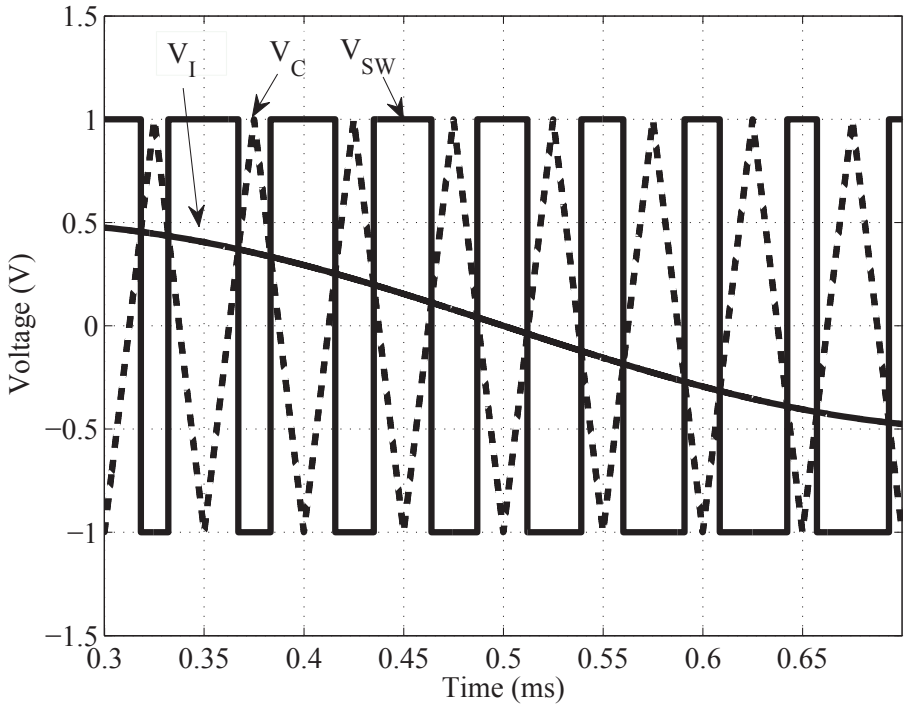

Figure 3.10: Open loop PWM waveforms.

The main design parameter for a first order compensator is the time constant τ_I, which will determine the unity gain frequency UGF=1/($2\pi \cdot \tau_I$), also know as gain-bandwidth product (GBW), of the system. Its value selection depends on several tradeoffs between the PWM carrier's frequency, CDA implementation's silicon area, amplifier's power, linearity, and noise. To understand the tradeoffs involved in the design of the close loop PWM CDA architecture, a first, second, and third order compensator design examples at the system will be discussed.

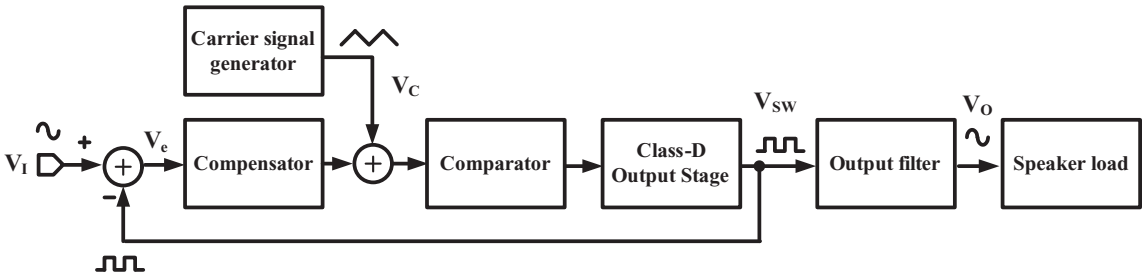

Figure 3.11: Close loop PWM CDA architecture.

The first-order compensator is typically implemented using an active integrator with an operational amplifier. The advantage of the first order compensator is that only has one pole, ensuring a stable system if the UGF $\ll F_{SW}$. The small signal transfer function for the first-order ideal compensator $G_{C,1st}(s)$, modeling the comparator and output stage as a unity linear gain, is expressed as,

$$G_{C,1st}(s) = \frac{V_{SW}(s)}{V_e(s)} = \frac{1}{s \cdot \tau_I} \tag{3.7}$$

where τ_I is the integration's time constant. For very small frequencies (e.g. s=0), the magnitude of $G_{C,1st}(s)$ is ideally infinite, while for very high frequencies (e.g. s=∞), the

magnitude is zero, and for frequencies between these two points, the magnitude has a roll off or slope of -20 dB for each decade in frequency. However, the implementation of the active integrator will be limited by the finite low frequency gain and finite GBW of the operational amplifier, as will be discussed in Section 3.3.1.

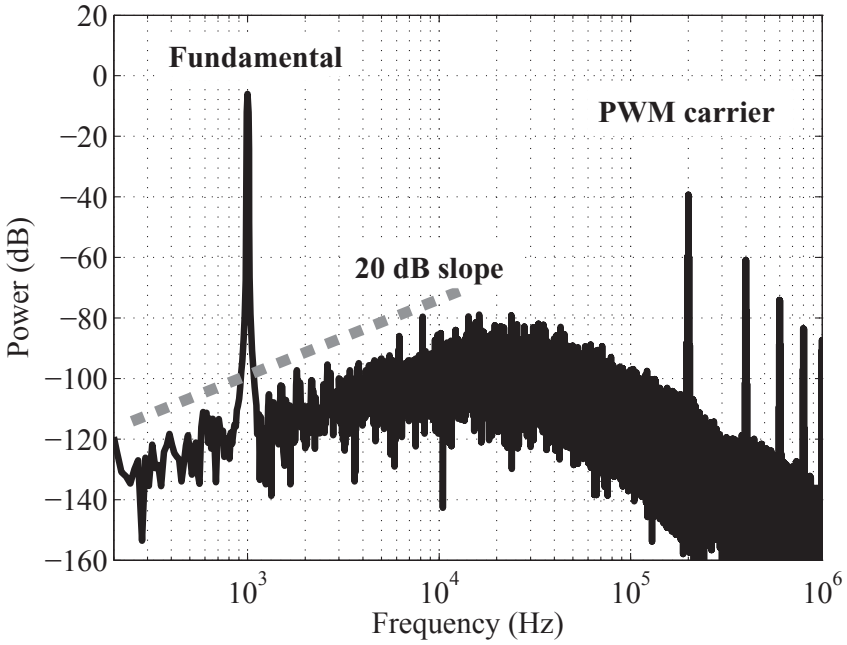

Figure 3.12: Output spectrum for 1st order PWM CDA with UGF=50 kHz.

A sample system level simulation using MATLAB© for a first-order close loop PWM CDA was performed for an input signal of 0.5 V_{RMS} at 1 kHz, $F_{SW} = 200\ kHz$, a Butterworth second order low pass filter with cut-off frequency of 20 kHz, and UGF = 50 kHz. The Simulink model used for simulation is illustrated in Fig. 3.13. The frequency spectrum for the output signal is shown in Fig. 3.12, where the input signal fundamental frequency and the carrier signal are evident.

Also, the slope from the first-order compensator is evident in the audio frequency bandwidth. It can be observed that the third harmonic for the input signal is -90 dB from the fundamental harmonic. This choice of UGF provides a DC gain of 66 dB in the loop.

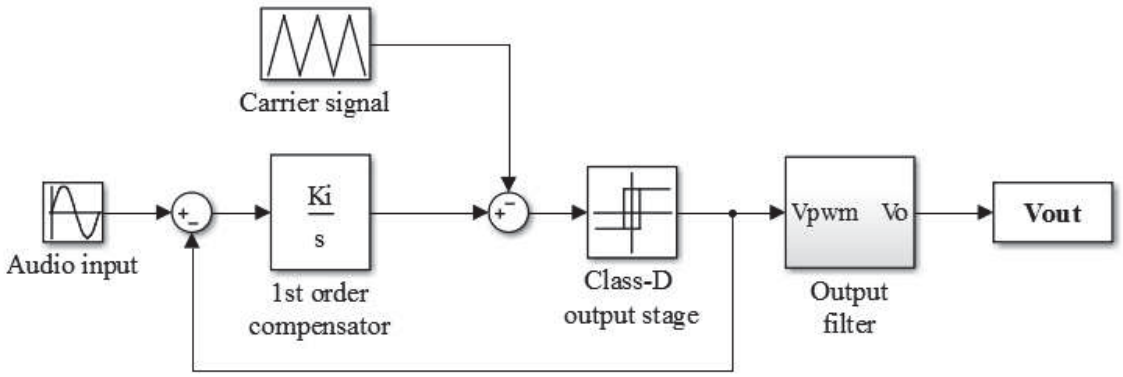

Figure 3.13: Simulink model for 1st order PWM CDA architecture.

If the UGF is chosen at lower frequencies, then the gain in the loop will be reduced; consequently, the distortion will increase. This effect can be observed in Fig. 3.14 where a UGF = 25 kHz was chosen while keeping the other parameters the same. It can be observed that the third harmonic is -84 dB from the fundamental harmonic of the signal; this -6 dB degradation is expected since the UGF was reduced in half and the gain in the loop also reduced in half. This choice of UGF provides a lower DC gain of 60 dB in the loop. Also, the high order harmonics are not attenuated due to the low UGF of the compensator and the overall THD+N is degraded.

If the UGF is chosen at higher frequencies, then the UGF of the system will start to get close the switching frequency and the stability of the system will degrade, increasing the IMD of the system and degrading the THD+N.

To verify this, the UGF was increased to 100 kHz, that is the theoretical maximum UGF according to the Nyquist criteria for this example, and the output spectrum is shown in Fig. 3.15. This choice of UGF provides a higher DC gain of 72 dB in the loop, attenuating an extra 6 dB in comparison to the original case, but the IMD at the PWM carrier frequency degrades the overall linearity.

The first order system will enhance its THD+N for larger UGF, but restricted by the F_{SW} of the system. One solution is to increase the F_{SW} to have more room to expand the UGF, but this comes at the expense of design complexity and increased power consumption in the circuits that will implement the system. Another solution is to increase the order of the compensator by adding more cascaded integrators, but the stability degrades as the compensator order increases.

The second order compensator follows the same procedure to choose the integrators time constant. The only difference is that the compensator now has two integrators in

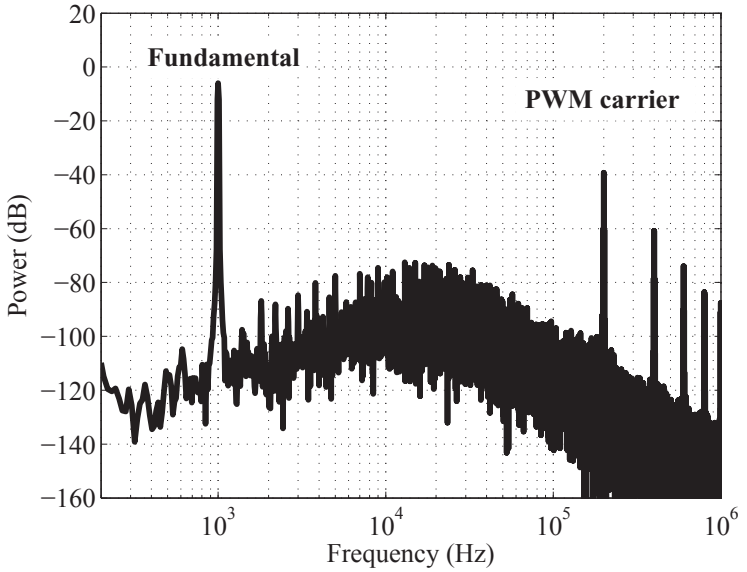

Figure 3.14: Output spectrum for 1st order PWM CDA with UGF=25 kHz.

cascade, providing a -40 dB slope in the desired bandwidth. However, the stability of the system starts to degrade since the system has two poles at the origin with a phase shift of 180°. To ensure stability, an extra zero has to be added to the compensator and its placement in frequency will affect the dynamics of the second order system. The small signal transfer function for the second-order ideal compensator $G_{C,2nd}(s)$, modeling the comparator and output stage as a unity linear gain, is expressed as,

$$G_{C,2nd}(s) = \frac{V_{SW}(s)}{V_e(s)} = \frac{1 + s \cdot \tau_Z}{(s \cdot \tau_I)^2} = \frac{1 + s \cdot K_Z \cdot \tau_I}{(s \cdot \tau_I)^2} \tag{3.8}$$

where τ_Z represents the zero time constant, and the constant $K_Z = \tau_Z/\tau_I > 1$ is typically used to determine the zero frequency location as a function of the integrator pole location to ensure stability in the system.

The UGF is now affected by the zero frequency location, especially by the choice of K_Z, and it can be estimated by finding the frequency at which the magnitude of (3.8) is

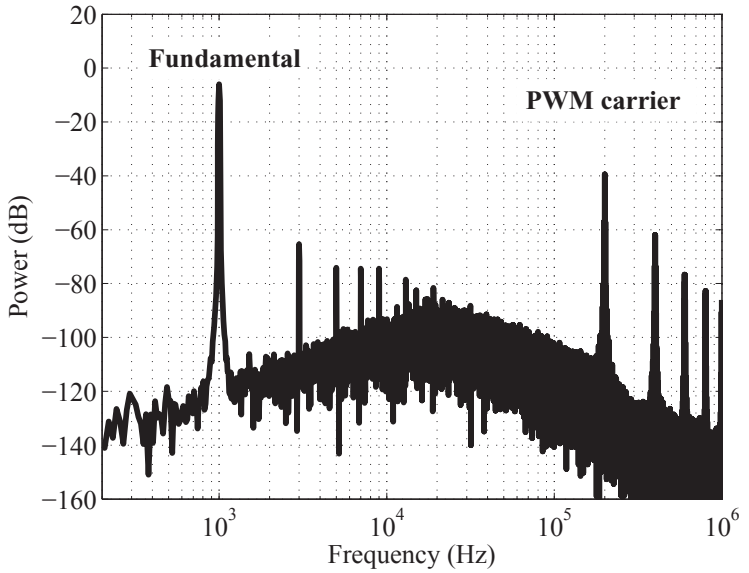

Figure 3.15: Output spectrum for 1st order PWM CDA with UGF=100 kHz.

unity as,

$$UGF_{PWM,2nd} \cong \frac{K_Z}{2\pi \cdot \tau_I}. \tag{3.9}$$

To ensure a stable close loop system, the phase margin (PM) of $G_{C,2nd}(s)$ needs to be larger than 40° to avoid ringing in the output signal. The main purpose of the extra zero is to introduce a phase boost to satisfy the PM requirement. The choice of K_Z will affect the PM of the system as,

$$PM_{PWM,2nd} = \tan^{-1}(K_Z^2). \tag{3.10}$$

Using the extra zero for compensation can extend the UGF beyond the value of the first order compensator. A large K_Z would increase the PM and UGF of the system. However, the UGF needs to keep constrained to avoid getting too close to the F_{SW} to avoid IMD and distortion. These effects are shown in the Bode plot of (3.8) for three choices of $K_Z = 0, 3, 10$, as illustrated in Fig. 3.16.

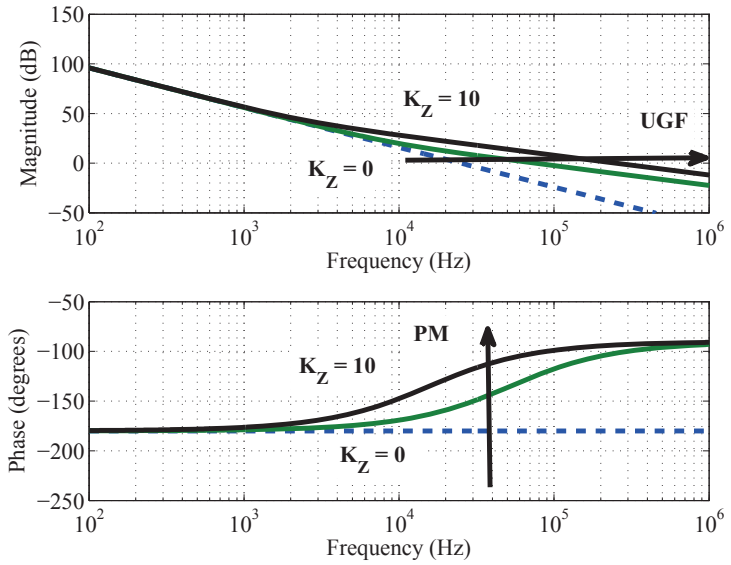

Figure 3.16: Bode plot for second order PWM CDA for different K_z values.

Small values of K_Z do not provide enough PM in the system, but for large values of K_Z, the system UGF is too large and close to the switching frequency that the close loop system would be unstable.

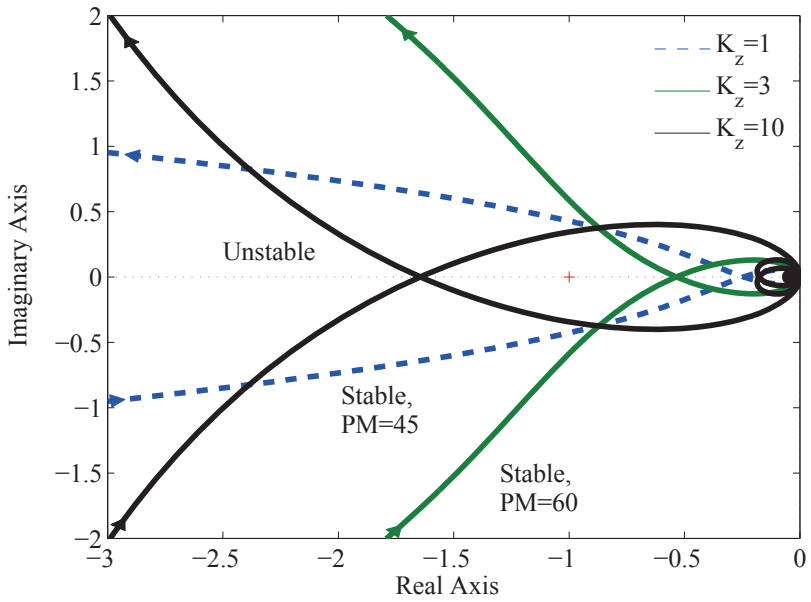

Figure 3.17: Nyquist plot for second order PWM CDA for different K_z values.

The Nyquist plot provides insight in the stability of the close loop system, as observed in Fig. 3.17 for a F_{SW}=200 kHz. A careful choice of K_Z is needed, taking into account the value of τ_I and F_{SW}. A rule-of-thumb choice for K_Z is between 1.2 and 3, since it introduces enough phase boost but keeps the UGF constrained.

The benefits of increasing the loop gain by increasing the order of the compensator, as expressed in (3.6), is a better audio performance. To demonstrate this, the same system level parameters of the first-order compensator will be used for the simulation of a second-order close loop PWM CDA with a UGF = 50 kHz and $K_Z = 2$. The simulink model used

for simulation is illustrated in Fig. 3.18. The resulting output spectrum is shown in Fig. 3.19, where the third harmonic of the input signal is -96 dB below the fundamental, and the in-band noise floor has a 40 dB slope attenuation.

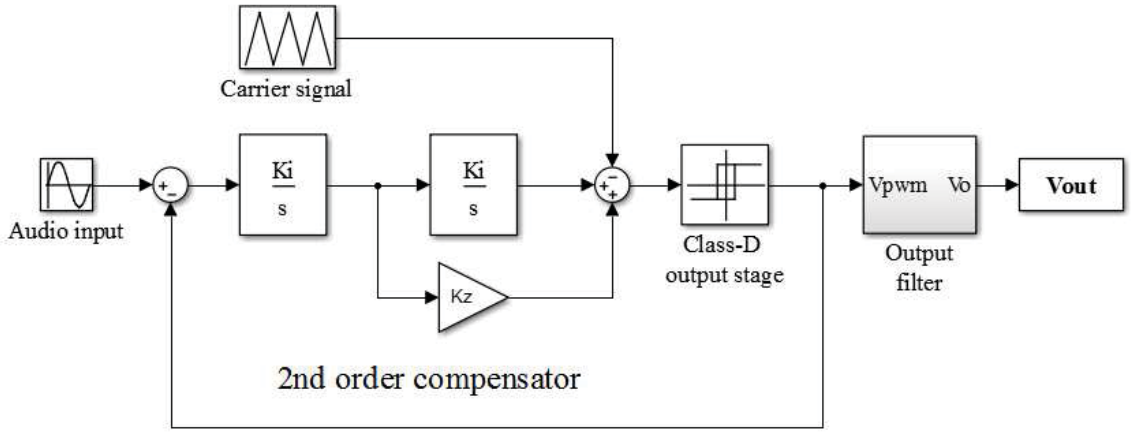

Figure 3.18: Simulink model for 2nd order PWM CDA architecture.

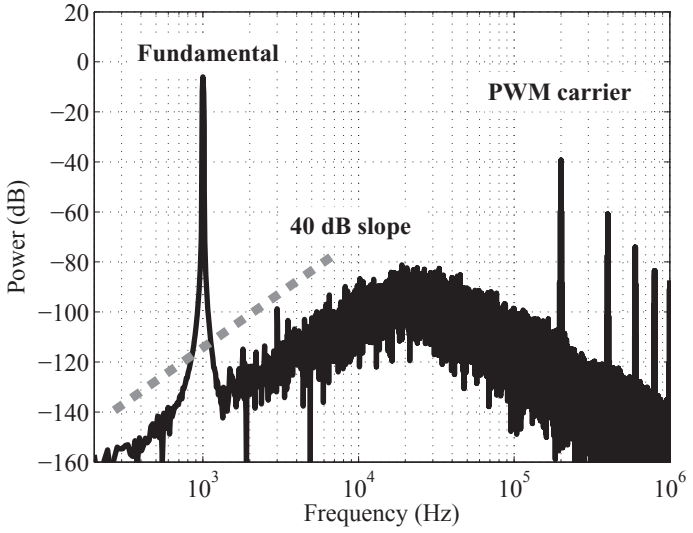

Figure 3.19: Output spectrum for 2nd order PWM CDA with UGF=50 kHz.

The distortion and noise floor have been attenuated even more, increasing the overall THD+N of the system compared to the first order system. Table 3.2 summarizes the simulation results for different compensator order, UGF, or K_z values. In conclusion, a high order compensator will help to attenuate the noise and distortion in the band of interest. However, the stability for the closed loop system degrades as the compensator order increases. Higher order modulators have been used in closed loop PWM CDA architectures to achieve high audio performance but at the expense of design complexity and power consumption [9, 42, 59, 61].

Table 3.2: Summary for the close loop PWM CDA architecture simulations

Order	UGF	DC gain	THD+N
1st	25 kHz	60 dB	-84 dB
1st	50 kHz	66 dB	-90 dB
1st	100 kHz	72 dB	-60 dB
2nd, K_z=1	50 kHz	100 dB	-92dB
2nd, K_z=2	50 kHz	120 dB	-98 dB
2nd, K_z=3	50 kHz	140 dB	-76 dB

3.2.2 Sigma-delta modulation

The sigma-delta modulation was initially developed as an oversampled system for analog-to-digital converter applications. It is also know as pulse density modulation since the input information is encoded as the number of pulses that the modulator outputs, as observed in Fig. 3.20. The main difference for the SDM compared with the PWM for CDA applications is that a higher clock frequency is typically used to exploit the oversampling effect [62].

The close loop SDM CDA architecture is shown in Fig. 3.21, where a high frequency clock signal is used to sample and hold the output of the compensator, and a quantization block is used to transform the voltage information to a pulse density encoding. The output of the quantizer is amplified in the class-D output stage and applied to the output filter. Finally, the switching output of the CDA is used as the feedback signal and returned to the input of the compensator.

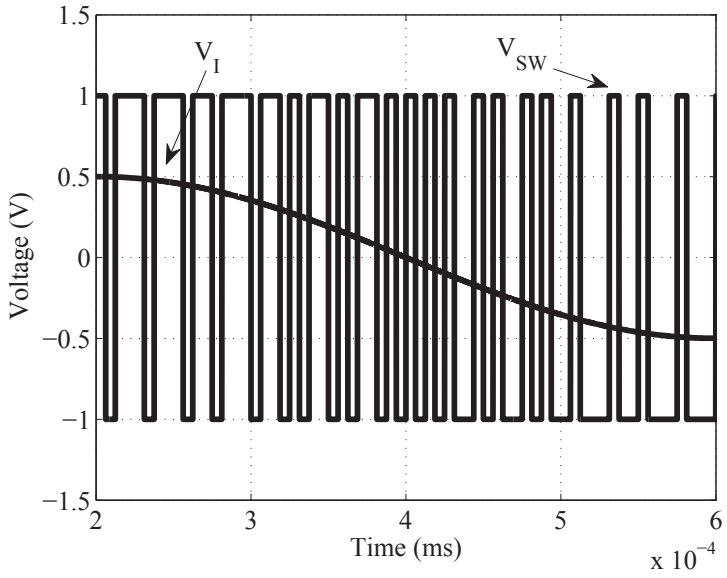

Figure 3.20: Close loop SDM waveforms.

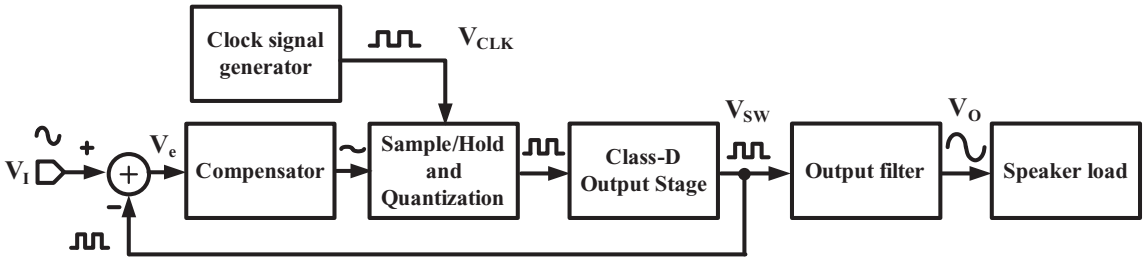

Figure 3.21: Close loop SDM CDA architecture.

To understand the benefits of using SDM, the quantization error and the oversampling effect have to be detailed. The comparator typically used as quantizer in the CDA takes its input and compares it to the a reference value (e.g. common mode voltage) to make a decision every rising edge of the clock signal. If the input signal is higher than the reference, the output changes to a high level; if the input signal is lower than the reference, the output changes to a low level. Thus, the difference between the input value and the output value of the quantizer is the quantization error. The number of quantization levels affect how big is the quantization error since each extra step is closer to the ideal value. The quantization step size (q) as a function of the number of bits in the quantizer is typically expressed as [66],

$$q = \frac{2 \cdot V_{DD}}{2^b - 1} \tag{3.11}$$

where V_{DD} is the supply voltage of the quantizer, and b represents the number of bits of the quantizer. Assuming an uniform distribution of the quantization error (e_q) across all the quantization levels, we can express the average quantization error noise power as [66],

$$\sigma_e^2 = \int_{-q/2}^{q/2} \frac{e_q^2}{q} de_q = \frac{q^2}{12} = \frac{V_{DD}^2}{3.2^{2b}}. \tag{3.12}$$

The signal to noise ratio of a n-bit quantizer for a sinusoidal signal of amplitude A with signal power $\sigma_x^2 = A^2/2$ is expressed as,

$$SNR(dB) = 20 \cdot \log_{10} \frac{\sigma_x}{\sigma_e} \cong 20 \cdot \log_{10} \frac{A}{V_{DD}} + 6.02 \cdot b + 1.76. \tag{3.13}$$

It can be observed from (3.13) that increasing the number of bits, enhances the SNR of the system. For each additional bit in the quantizer, an extra 6 dB of SNR are added. However, more bits in the quantizer increase the complexity of the quantizer design and the power consumption of the overall system.

To overcome this, oversampling can be used to decrease the quantization noise in the band of interest. The oversampling can be better understood by observing its effect on the error power density as shown in Fig. 3.22. For a desired frequency bandwidth (f_B) sampled at the Nyquist rate of $F_{SW} = 2f_B$ with a power density of $P_e(f)$, the oversampling will spread the same $P_e(f)$ across the new bandwidth, lowering the in-band error power density. Thus, if an ideal brick-wall filter is used at f_B, the error power density will be reduced by the amount of oversampling used.

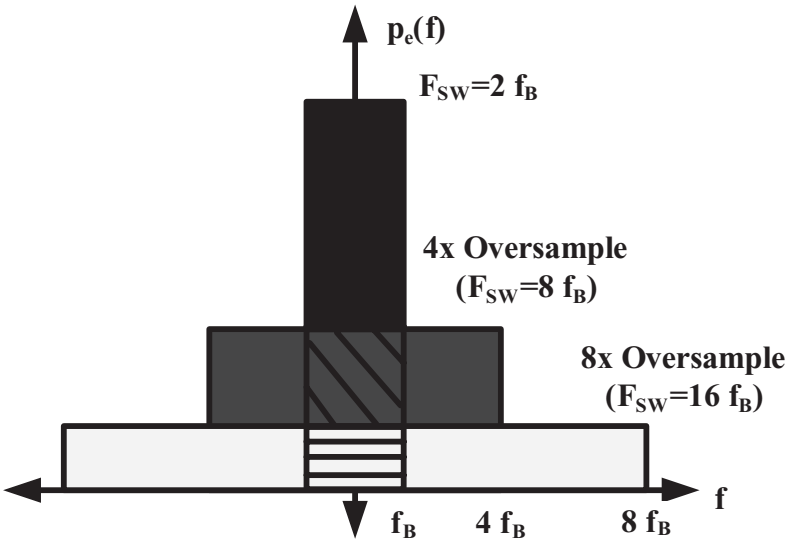

Figure 3.22: Oversampling effect on the error power density.

The amount of oversampling is typically expressed as a function of the desired bandwidth as the oversampling ratio $OSR = 2^r = F_{SW}/(2 \cdot f_B)$; The new in-band noise power after oversampling the quantization error noise power (σ_e^2) is,

$$\sigma_n^2 = \int_{-q/2}^{q/2} \frac{e_q^2}{q} \left(\frac{2 \cdot f_B}{F_{SW}} \right) de_q = \frac{q^2}{2^r \cdot 12} = \frac{\sigma_e^2}{OSR} \tag{3.14}$$

where the peak SNR for the oversampled system can be expressed as,

$$SNR(dB) = 20 \cdot \log_{10} \frac{\sigma_x}{\sigma_n} \cong 20 \cdot \log_{10} \frac{A}{V_{DD}} + 6.02b + 3.01r + 1.76. \tag{3.15}$$

It can be noticed that for every doubling in the OSR, the SNR improves by 3 dB. Thus, for low frequency applications such as audio, the OSR can be as high as 2^{10} improving the SNR by 30 dB only by using oversampling. However, this implies that a very high frequency clock signal has to be used, and that the circuitry needs to operate at the higher frequency, increasing the power consumption of the system.

Table 3.3: Ideal SNR for some SDM examples

Order (N)	OSR	SNR (dB)
1	128	60
2	128	94
3	128	128
1	256	69
2	256	109
3	256	149

The SDM architecture leverages the benefits of oversampling in a close loop system where a compensator helps to attenuate the distortion and quantization errors further, as in PWM architectures. The SDM can use a first order or higher order compensator to improve the CDA performance. However, the UGF of the loop is typically fixed to the audio bandwidth of 20 kHz.

Thus, the OSR or the compensator order (N) are increased to improve the SNR. The N^{th} order SDM peak SNR can be expressed as [66],

$$SNR(dB) \cong 6.02b + 1.76 + 10\log_{10}(2N+1) - 9.94N + 3.01(2N+1)r. \tag{3.16}$$

It can be observed that the oversampling effect is enhanced by the compensator order by a factor of (2N+1). Thus, high compensator order and high OSR can achieve outstanding performance. Table 3.3 summarizes a few examples for the calculation of the ideal SNR for an 1-bit quantizer SDM for several N and OSR. For high audio performance, the SDM CDA architecture would need a high OSR of at least 128 ($F_{SW} = 2 \cdot 128 \cdot 20\ kHz = 5.12\ MHz$), a high order compensator of at least 2nd order, or a combination of both.

A system level simulation using MATLAB© for a first-order SDM CDA was performed for an input signal of 0.5 V_{RMS} at 1 kHz, $OSR = 128$ or $F_{SW} = 5.12\ MHz$ for a f_B = 20 kHz, and a Butterworth second order low pass output filter with cut-off frequency of 20 kHz. The simulink model used for the simulation is illustrated in Fig. 3.23. The frequency spectrum for the output signal is shown in Fig. 3.24.

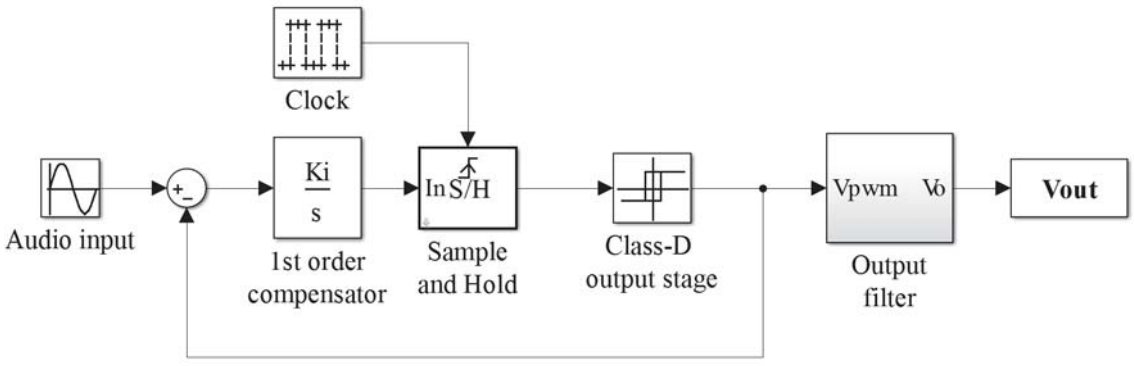

Figure 3.23: Simulink model for 1st order SDM CDA architecture.

It can be observed that the noise floor has a 20 dB/dec slope as expected. Also, the clock signal is at very high frequencies compared to the fundamental signal. Thus, the output filter attenuates it more, minimizing its effect on the speaker. The third harmonic is -80 dB from the fundamental tone, and the peak SNR is 60 dB.

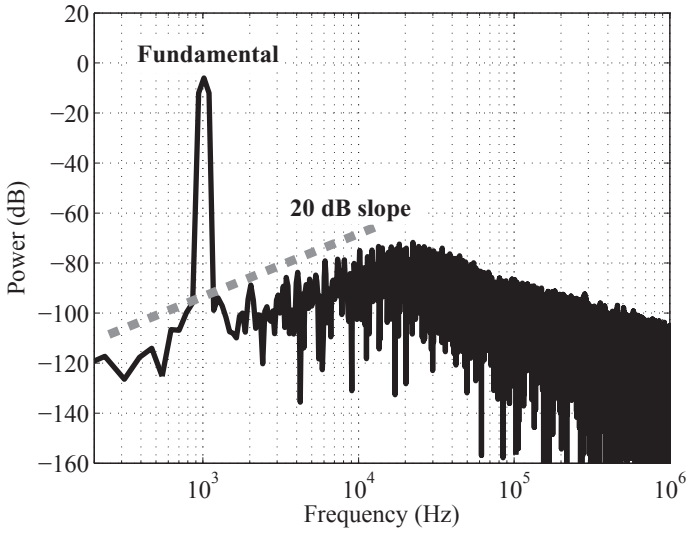

Figure 3.24: Output spectrum for 1st order SDM CDA with OSR=128.

To verify the effect of a higher compensator order as expressed in (3.16), the N was increased to 2 with the same OSR=128; the output frequency spectrum for this system is shown in Fig. 3.25. It can be observed that the noise floor is attenuated with a 40 dB slope, reducing the THD+N. By increasing the compensator order, the SNR improves as expressed in (3.16). Moreover, the higher compensator order, also helps to correct for distortion; the third harmonic is -86 dB from the fundamental tone, and the peak SNR is 72 dB. However, the SNR did not improve as predicted by (3.16) since even in an ideal simulation, the SDM is affected by timing errors in the simulator solver engine, the choice of the compensation zero frequency location, and other implementation inaccuracies.

It is evident that increasing the OSR also improves the performance of the system as expressed in (3.16). To prove this, the OSR was increased to 256 for the second order SDM CDA, and the output frequency spectrum is shown in Fig. 3.26. It can be observed that the same 40 dB slope in the noise floor remains but the noise and harmonics are attenuated even more due to the higher OSR. The third harmonic is -100 dB from the fundamental tone, and the peak SNR is 86 dB.

It is worth noticing that the SDM has also been proposed for DC-DC buck converters [67], where the main goal of using SDM is to reduce both the carrier distortion at the output and the EMI produced by the converter itself.

In conclusion, the SDM gives the advantage of using a high frequency clock signal to perform the oversampling instead of a triangle waveform as in PWM. The audio performance is highly dependent on the choice of compensator order and OSR; as the OSR increases, the circuit requirements on each block are more demanding. Also, as the compensator order increases, the stability of the loop starts to degrade, requiring careful choice of compensation.

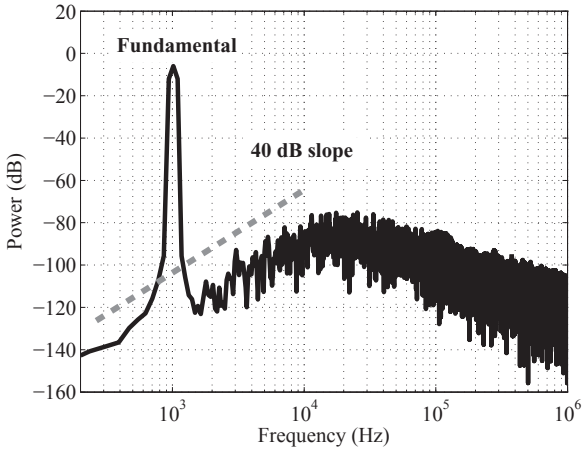

Figure 3.25: Output spectrum for 2nd order SDM CDA with OSR=128.

3.2.3 Self-oscillating modulation

The SOM is inherently a close loop architecture that leverages the fact that the compensator introduces a signal delay to implement an oscillator with an oscillating frequency at F_{SW}. This architecture meets the Barkhausen criteria (BKC) for the close loop system in (3.6) expressed as,

$$|LG(s)| = |A_{ol}(s) \cdot \beta(s)| = 1 \tag{3.17}$$

$$\angle LG(s) = \angle(A_{ol}(s) \cdot \beta(s)) = 2\pi n, n \in 0,1,2,\ldots \tag{3.18}$$

where the loop gain magnitude of the system must be 1 and the phase shift of the loop gain must be a multiple of 2π (e.g. $0^\circ, 360^\circ, \ldots$). The general SOM CDA architecture is shown in Fig. 3.27, where the $LG(s)$ is determined by the compensator transfer function, the hysteretic comparator, and the output stage transfer function. The hysteretic comparator plays an important role in the operation of the SOM since it changes its magnitude and phase shift proportionally to the input signal [55].

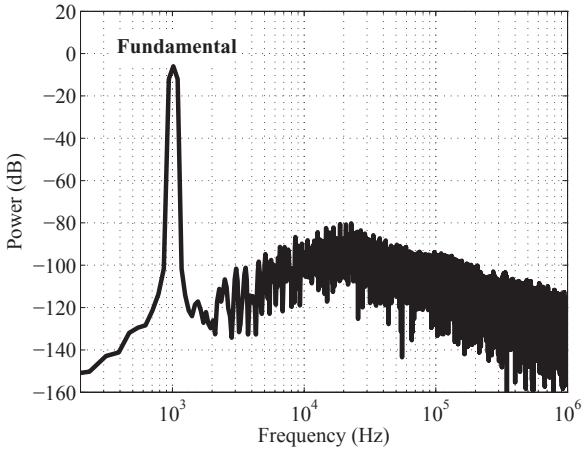

Figure 3.26: Output spectrum for 2nd order SDM CDA with OSR=256.

The input signal dependency of the hysteretic comparator can be observed from its describing function evaluation for a sinusoidal input signal with amplitude V_i that can be expressed as [68],

$$G_M(V_i) \cong \frac{V_{DD}}{V_i} e^{-j\sin^{-1}(V_h/V_i)} \tag{3.19}$$

where V_h is the hysteresis window, V_{DD} is the voltage limit or supply of the comparator, and assuming that $V_i > V_h$. The BKC for the SOM system must be accomplished by the negative feedback in the loop that adds -180° of phase shift while the compensator ideally adds less than -180° of phase shift to remain stable. Therefore, to satisfy (3.18), the loop changes the hysteretic comparator phase shift by manipulating the amplitude of its input signal (V_i). Moreover, this change in V_i also changes its magnitude gain to remain within the hysteresis window such that the overall loop gain satisfies (3.17). The main advantage of this architecture is that it obviates the need of a clock or carrier signal generator since it generates its own switching signal, saving power and reducing the complexity of the loop. The main drawback is that its switching frequency could decrease too much for large input amplitudes, degrading the THD+N.

The comparator hysteresis window, the compensator delay, and the propagation delay in the loop will determine the modulation frequency of the SOM system [55].

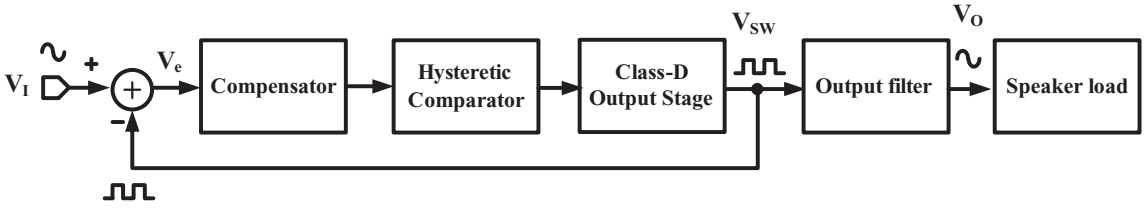

Figure 3.27: Close loop general SOM CDA architecture.

The F_{SW} as a function of duty cycle ($D = V_i/V_{supply}$) could be expressed as,

$$F_{SW}(D) = \frac{D \cdot (1-D)}{\frac{V_h \cdot \tau_{compensator}}{V_{supply}} + \tau_d} \tag{3.20}$$

where V_{supply} is the supply voltage of the comparator, V_h is the voltage hysteresis window of the comparator, $\tau_{compensator}$ is the compensator delay, and τ_d is the propagation delay from the comparator to the input of the compensator, including the comparator delay, the output stage delay, and the feedback network delay.

It can be noticed that F_{SW} is not constant since it chances as a function of the input signal. The F_{SW} variation could be reduced if needed by controlling the main parameters in (3.20) such as the propagation delay [69], the hysteresis window [70, 71], or the compensator delay [72].

The simplest architecture for a SOM is based on a relaxation oscillator using a passive low pass filter as feedback element, and a hysteretic comparator to close the loop, as observed in Fig. 3.28. This architecture is commonly know as bang-bang (BB) architecture since the output only changes when the error signal is higher/lower than the hysteresis window.

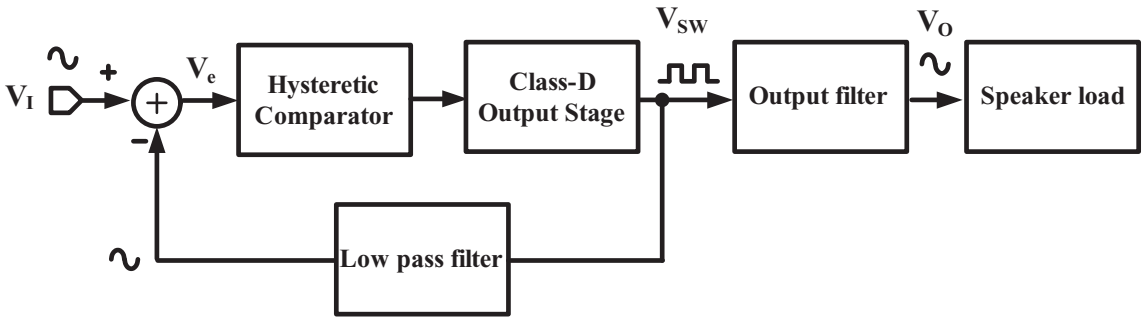

Figure 3.28: Bang-bang SOM CDA architecture.

A sample simulation using MATLAB © was performed for a bang-bang CDA to verify its functionality with a hysteresis window of 0.1 V, supply voltage of 1 V, and low pass filter pole at 20 kHz, as illustrated in the simulink model of Fig. 3.29. The output power spectrum is shown in Fig. 3.30. It can be observed that the SOM carrier frequency is not a pure tone and that its power is spread across a frequency range proportional to the amplitude of the input as expected from (3.20). Also, the loop magnitude gain is only determined by the hysteretic comparator, as expressed in (3.19), that could not be enough to achieve high performance; the third harmonic is at -64 dB from the fundamental harmonic. The simplicity and small size of the bang-bang CDA comes at the expense of limited lin-

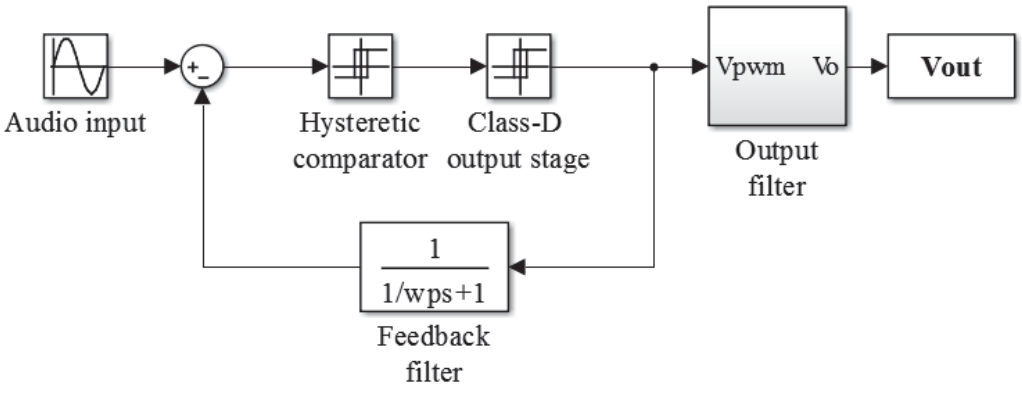

Figure 3.29: Simulink model for bang-bang CDA architecture.

earity performance due the absence of a compensator block to provide gain in the loop. Its performance can only be improved by reducing the hysteresis window or by changing the low pass filter pole location to increase F_{SW} as expressed in (3.20).

A high order compensator in the general SOM CDA architecture of Fig. 3.27 will provide better audio performance due to the increased loop gain at the expense of increased power consumption and design complexity [55, 65, 72, 73].

A system level simulation for a second order general SOM CDA architecture was performed with the same parameters as the bang-bang CDA architecture, as illustrated in the simulink model in Fig. 3.31. The output frequency spectrum is show in Fig. 3.32. It can be observed that the noise floor is highly attenuated due to the large loop gain contributed by the compensator; the third harmonic is at -110 dB from the fundamental harmonic. Also, the F_{SW} changed since the compensator delay decreased. Nonetheless, the same power spreading of the SOM carrier happens.

Different from the general architecture of Fig. 3.27, other SOM systems include the output filter in the loop and use a non-linear control technique as a compensator to remain

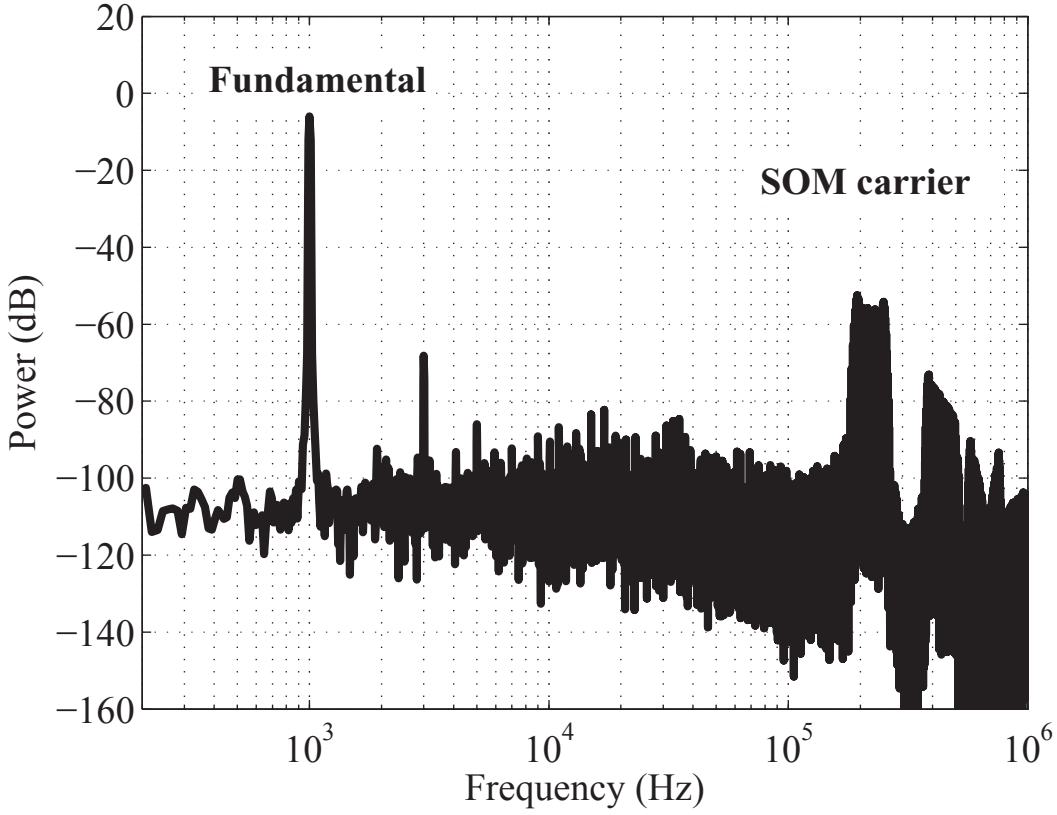

Figure 3.30: Output spectrum for bang-bang CDA architecture.

stable, as shown in Fig. 3.33. This non-linear control technique is know as sliding mode control (SMC), and it is implemented as a tracking system with robust operation under external perturbations.

The SMC architecture provides the advantage of relaxed design requirements in the compensator since the feedback signal is comprised of low frequency signal components, and the output filter errors are attenuated by the loop gain of the system. The non-linear controller ensures stability in the CDA with high audio performance and low power consumption [63, 64, 74].

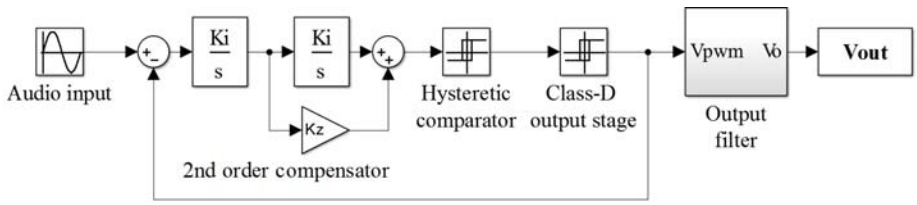

Figure 3.31: Simulink model for a 2nd order SOM CDA architecture.

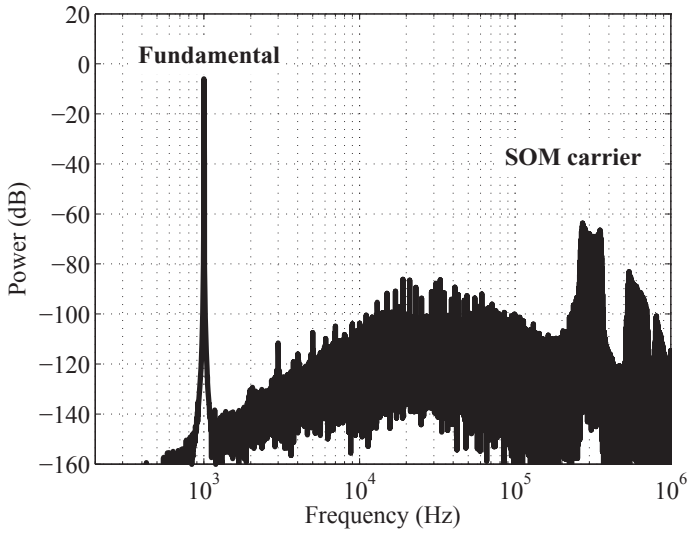

Figure 3.32: Output spectrum for 2nd order general SOM CDA architecture.

The SMC is based on the state variables of the switching structure of the system. For the CDA the state variables are the inductor current (i_L) and capacitor voltage (V_C) in the output low pass filter. The CDA has two different structures, as observed in Fig. 3.34, depending to the switching state of the output.

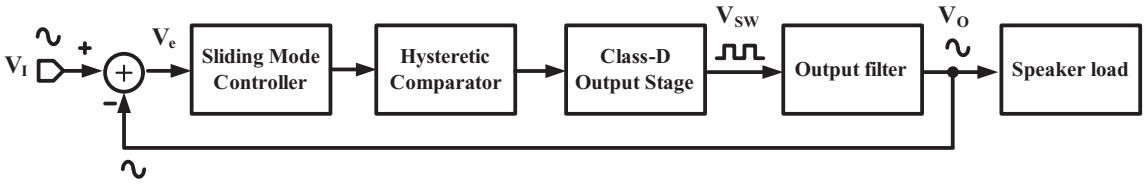

Figure 3.33: Close loop SMC CDA architecture.

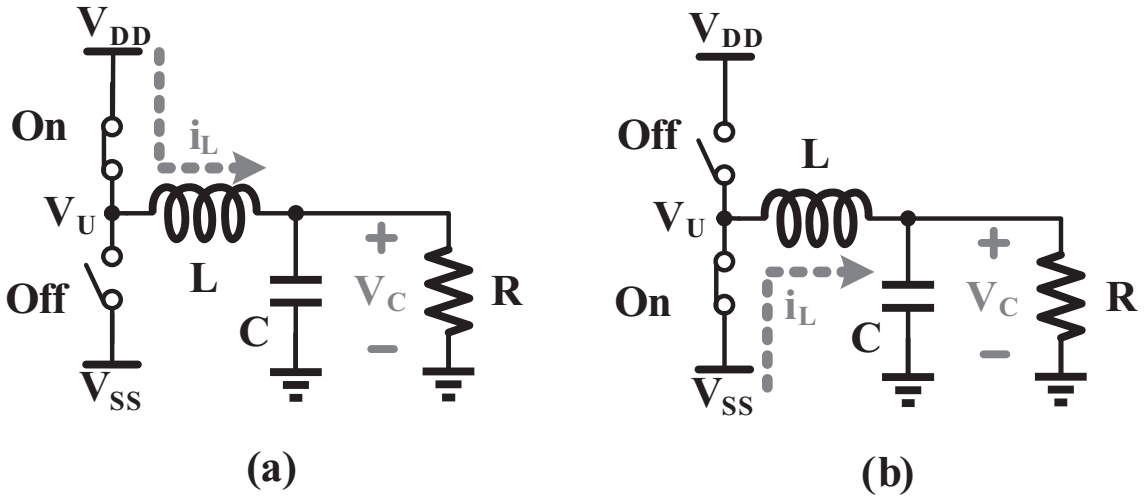

Figure 3.34: Switching structure in the CDA when connected to (a) V_{DD} or (b) V_{SS}.

The state-space model corresponding to the output filter of the CDA, as shown in Fig. 3.34, can be expressed as,

$$\frac{d}{dt}\begin{pmatrix} i_L(t) \\ V_C(t) \end{pmatrix} = \begin{pmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{pmatrix}\begin{pmatrix} i_L(t) \\ V_C(t) \end{pmatrix} + \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix} V_U(t), \tag{3.21}$$

where $V_C(t)$ is the voltage across the capacitor C, $i_L(t)$ is the current through the inductor L, R represents the speaker resistance, and $V_U(t)$ is the binary-modulated signal generated by the SMC. The goal of the SMC is to generate the control signal $V_U(t)$ using a control law defined by a switching function to force the system to follow a desired response according to the system sliding equilibrium point [75].

The switching function is typically chosen to minimize the error voltage of the system ($e(t) = V_i(t) - V_o(t)$), and it is defined in the canonical form for a second order system as,

$$s(e,t) = k_1 e(t) + k_2 \dot{e}(t) \tag{3.22}$$

where the kth coefficients need to be chosen to meet the Hurwitz stability criterion; in general the switching function for a Nth-order system will be a (N-1) order system [76]. Thus, a N=1 is needed to control a second order system which simplifies the compensator design requirements. Also, the switching function in (3.22) implies that a differentiation is needed which does not attenuate the in-band noise [63].

A system level simulation was performed for the SMC CDA architecture with $k_1 = 1$ and $k_2 = 5.83e^{-6}$, and the output power spectrum using the simulink model illustrated in Fig. 3.35. The frequency spectrum is shown in Fig. 3.36, where the third harmonic is -80 dB from the fundamental harmonic, but the in-band noise is not attenuated due to the use of differentiators in the compensator.

Another alternative is to redefine the switching function in (3.22) using integrals in-

stead of differentiations [64]. By doing this, the compensator attenuates the in-band noise, and relaxes the design requirements of the compensator. This alternative is know as integral sliding mode control (ISMC) since it uses integrators instead of differentiators, and its architecture is shown in Fig. 3.37. Note that an additional loop is added before the hysteretic comparator using the inductor current information to reduce the state-space system to a first order.

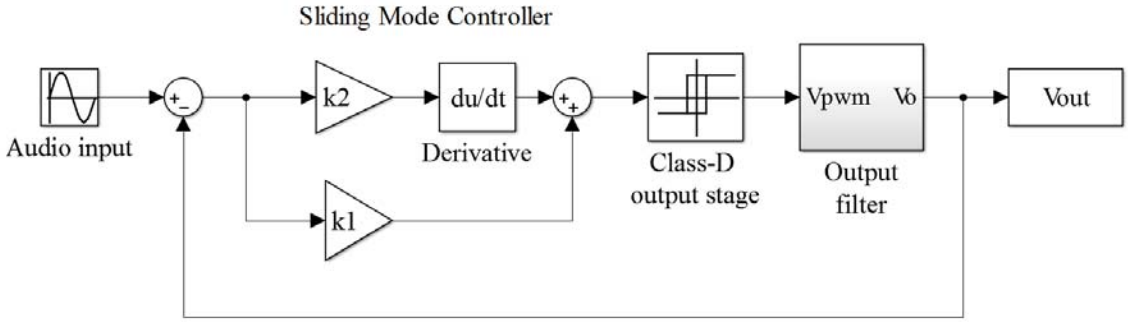

Figure 3.35: Simulink model for SMC CDA architecture.

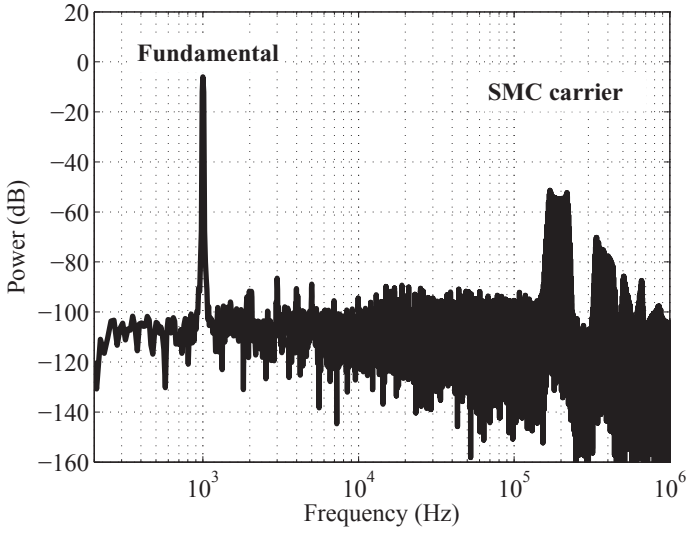

Figure 3.36: Output spectrum for SMC CDA architecture.

Thus, the new switching function for the ISMC [64] is defined as ,

$$s(e,t) = k_i \int e(t) - i_L(t). \tag{3.23}$$

The drawback of the ISMC architecture is that the inductor current information, containing high frequency components at F_{SW}, needs to be sensed; thus, the circuit that implements the adder before the hysteretic comparator has to be able to process the high frequency signals with accuracy, increasing its power consumption.

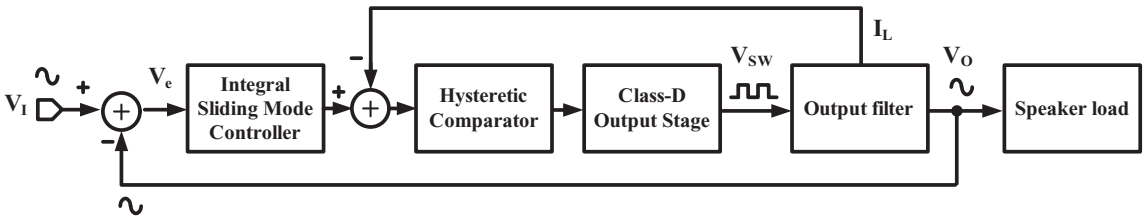

Figure 3.37: Close loop ISMC CDA architecture.

A system level simulation was performed for the ISMC CDA architecture with $k_i = 1.25e^5$ using the simulink model illustrated in Fig. 3.38, and the output power spectrum is shown in Fig. 3.39.

It can be observed that the third harmonic is -110 dB from the fundamental harmonic, and the in-band noise is greatly attenuated by the compensator. Thus, the ISMC can provide outstanding audio performance with low power consumption. More details about a sample implementation using ISMC is presented in Appendix B.

The SOM architectures have also been proposed in DC-DC buck converters where the inherent stability and fast transient response is leveraged for integrated power management modules [69, 77, 78].

In conclusion, the SOM CDA architecture obviates the need for a carrier signal generator, and it provides high audio performance, low power consumption, and high efficiency. The tradeoffs are its variable switching frequency, but this can be addressed using different schemes to keep a quasi-constant F_{SW}.

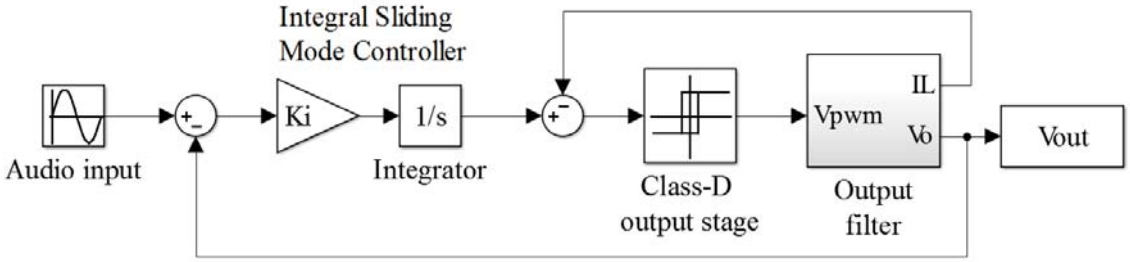

Figure 3.38: Simulink model for ISMC CDA architecture.

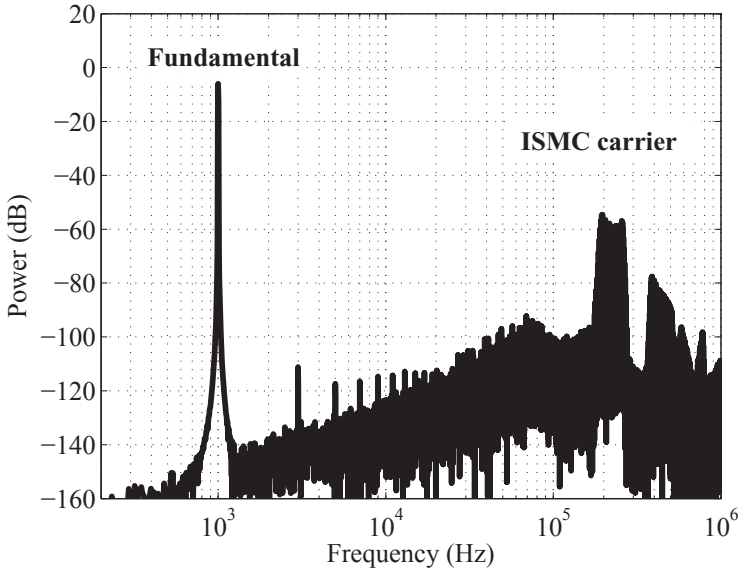

Figure 3.39: Output spectrum for ISMC CDA architecture.

3.2.4 Modulation architecture comparison

To summarize the advantages and tradeoffs in the main close loop CDA architectures in terms of audio performance, table 3.4 presents the simulation results for the main architectures and some estimations about the circuit design complexity, EMI, power, and area.

Table 3.4: Close loop CDA architecture audio performance comparison

System	Order	THD+N	SNR	Complexity	EMI	Power	Area
PWM	1	-76 dB	84 dB	L	H	L	M
PWM	2	-92 dB	90 dB	M	H	M	M
SDM	1	-81 dB	86 dB	M	L	M	M
SDM	2	-88 dB	92 dB	H	L	H	H
SOM	1	-90 dB	86 dB	M	M	L	L
SOM	2	-99 dB	100 dB	M	M	M	M
BB	1	-62 dB	86 dB	L	M	L	L
SMC	1	-80 dB	90 dB	M	M	L	M
ISMC	1	-104 dB	120 dB	L	M	L	L

L=Low, M=Medium, H=High

It can be observed that all the close loop CDA architectures could provide good audio performance, with THD+N $<$ -60 dB and SNR $>$ 80 dB. The preferred choice for a CDA architecture in commercial applications is the PWM due to its medium complexity, area, and power tradeoffs [8, 42]. The SDM architecture is typically not chosen due to its high complexity, power, and area consumption [62], but still provides a good alternative for digital input CDA due to its compatibility with sampled data. The SOM architectures provide a good alternative for high performance CDA, but their development have remained as academic research [63, 64, 65], and their commercial applications are limited.

3.3 Class-D design implementation tradeoffs

In general, the ideal system level results in Table 3.4 will be degraded by the circuit implementation of each building block in the architecture. The non-idealities in the amplifiers used in the compensator, the timing errors in the class-D output stage, the output filter non-idealities, among other perturbations will limit the maximum achievable THD+N and SNR in the system. To illustrate the circuit implementation tradeoffs, a conventional

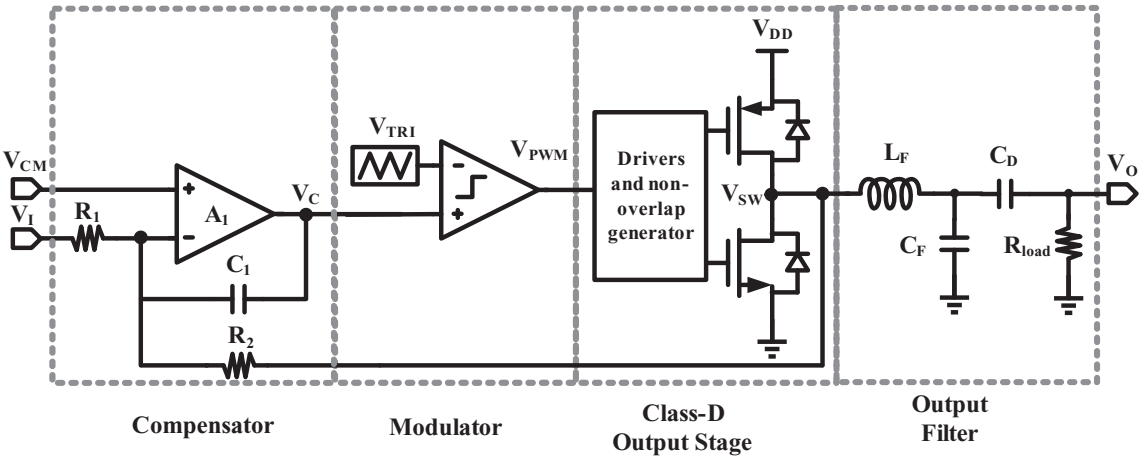

Figure 3.40: First-order single-ended PWM class-D audio amplifier circuit.

single-ended (SE) first-order PWM CDA architecture will be designed as shown in Fig. 3.40. The compensator is implemented using an amplifier (A_1) configured as an active integrator. The PWM modulator is implemented using an open-loop comparator and a triangle wave generator. The class-D output stage is implemented using a CMOS switch with drivers and non-overlap generator. The output filter is implemented as a second-order LC low-pass filter with AC coupling to remove the DC component at the speaker. The circuit design tradeoffs for each block will be detailed next, and an example implementation in a standard 0.18 μm CMOS technology will be provided.

3.3.1 Compensator amplifier

The compensator design is important since it will limit the output noise and distortion performance of the system. It is typically implemented as a chain of integrators, where each integrator is implemented using an amplifier in feedback. An ideal amplifier would provide infinite gain and GBW; but, in reality, the amplifier will have a finite gain and GBW that will degrade the implemented function. To achieve high audio performance in the CDA, it is necessary to understand the effects of the non-ideal amplifier in the implemented integrator function.

The active integrator ideal time constant is $\tau_I = R_1 \cdot C_1$, and its value selection depends on several tradeoffs in the CDA between the passive component values, amplifier A_1 power consumption, linearity, and in-band noise. Considering the finite gain of the amplifier A_1, the transfer function for the active integrator yields,

$$G_{int,actual}(s) = -\frac{G_{int,ideal}(s)}{1+\frac{1}{A_1(s)\cdot\beta_C(s)}} \cong -\frac{\left(\frac{1}{s\cdot R_1\cdot C_1}\right)}{1+\frac{s}{GBW}\cdot\left(\frac{s\cdot R_{1,2}\cdot C_1+1}{s\cdot R_{1,2}\cdot C_1}\right)} \tag{3.24}$$

where $R_{1,2} = R_1//R_2$, the amplifier's transfer function is characterized as $A_1(s) \cong GBW/s$, and $\beta_C(s)$ is the integration's amplifier feedback transfer function.

The magnitude and phase of (3.24) for $GBW \cdot R_{1,2} \cdot C_1 \gg 1$ can be expressed as,

$$\begin{aligned} G_{int,actual}(j\omega) &\cong -\frac{1}{\frac{j\omega}{\omega_{int}} - \frac{\omega^2}{GBW \cdot \omega_{int}}}, \\ |G_{int,actual}(j\omega_{int})| &\cong \frac{1}{\sqrt{1+\left(\frac{\omega_{int}}{GBW}\right)^2}}, \\ \angle G_{int,actual}(j\omega_{int}) &\cong -90^\circ - \tan^{-1}\left(\frac{\omega_{int}}{GBW}\right) \end{aligned} \tag{3.25}$$

where $\omega_{int} = 1/R_1 \cdot C_1$. The ideal integrator at ω_{int} will have a magnitude of one and a phase shift of -90°. Thus, the magnitude and phase deviations from the non-ideal integrator for $GBW \gg \omega_{int}$ can be derived from (3.25) as,

$$\begin{aligned} \Delta_M &= \frac{1-\sqrt{1+\left(\frac{\omega_{int}}{GBW}\right)^2}}{\sqrt{1+\left(\frac{\omega_{int}}{GBW}\right)^2}} \cong \frac{1}{2} \cdot \left(\frac{\omega_{int}}{GBW}\right)^2, \\ \Delta_\varphi &= -\tan^{-1}\left(\frac{\omega_{int}}{GBW}\right). \end{aligned} \tag{3.26}$$

Another way to quantify the active integrator performance is in terms of its quality factor (Q_{int}), considering it as a reactive element with a lossy resistive part. The higher the value of Q_{int}, the better the integrator. From (3.25), the Q_{int} of the active integrator implementation can be expressed as,

$$Q_{int} = \frac{X(j\omega)}{Re} \cong \frac{\omega \cdot R_1 \cdot C_1}{\frac{-\omega^2 R_1 \cdot C_1}{GBW}} = -\frac{GBW}{\omega} = -|A_1(j\omega)|. \tag{3.27}$$

The goal of the implementation is to minimize Δ_M and Δ_φ, avoiding significant deviations in the integrator performance. Thus, the amplifier's GBW has to be higher than the chosen ω_{int}.

The UGF of the close loop first-order PWM CDA is given by $UGF = \omega_{int}/(2\pi)$, as discussed in Section 3.2.1. Thus, a large value for ω_{int} would provide a higher bandwidth for the CDA loop that will result in high THD+N, high PSRR at higher frequencies, and smaller values for the passive components. However, the amplifier's power would need to be increased to avoid deviations in ω_{int} due to finite GBW. On the other hand, a small value for ω_{int} would result in low THD+N, low PSRR at higher frequencies, and bigger values for the passive components. However, the amplifier's design requirements are relaxed, requiring low power consumption.

From section 3.2.1, we observed that a good tradeoff between performance and power consumption for the UGF of the first order PWM CDA architecture is 1/10 of F_{SW}; thus, for this example implementation, a UGF= 50 kHz is selected for the system with F_{SW}= 500 kHz. The passive component selection to implement τ_I need to consider the input resistors (R_1, R_2 in Fig. 3.40) noise contribution and the amplifier's driving capability. The resistor thermal noise for 1 Hz bandwidth can be expressed as,

$$V_R^2(f) = 4kTR \cong 4kTR_s\frac{L_R}{W_R} + R_C \tag{3.28}$$

where $k = 1.38\text{x}10^{-23}$ is the Boltzmann constant, T is the temperature in Kelvin degrees, R_s is the resistance per square for the chosen resistor type, L_R is the length of the resistor layout, W_R is the width of the resistor layout, and R_C is the total resistance from all the contacts in the resistor layout. Thus, a large resistor value will introduce large thermal noise that can limit the THD+N and SNR performance of the whole system; but, a large capacitor will load the amplifier, requiring large power consumption to drive it.

Note that a capacitor implementation occupies more silicon area than a resistor; thus, the resistor design has a tradeoff between area, noise, and power consumption.

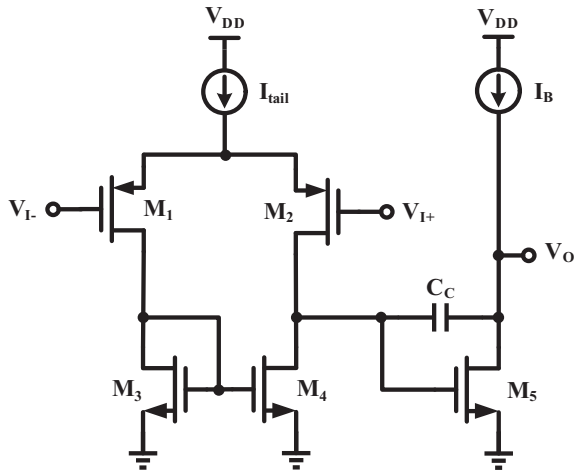

Figure 3.41: Miller compensated two-stage amplifier.

The amplifier A_1 is typically implemented as a two-stage Miller-compensated amplifier as shown in Fig. 3.41, where the Miller compensation capacitor (C_C) implements a pole-splitting technique to ensure an stable system [79, 80, 81, 82]. The main design parameters for the amplifier are its input referred noise, slew rate (SR), DC gain (A_{DC}), and GBW. Each design parameter has its own tradeoffs and are interrelated.

From a design perspective, the only variables in the amplifier design are the tail current (I_{tail}), the dimensions of each transistor, the bias current of the second stage (I_B), and any other passive that is used for compensation. In general, most amplifier topologies are greatly dependent of the transconductance (g_m) of the input transistors. A large g_m in the input pair will reduce the thermal noise, provide large DC gain, and increase the GBW, but at the expense of increased power consumption as will be detailed next.

The design equations for g_m as a function of the transistor dimensions and biasing

operating point can be expressed as,

$$g_m = \frac{I_{tail}}{V_{dsat}} = \frac{W}{L}\mu_p C_{ox} V_{dsat} = \sqrt{\frac{W}{L}\mu_p C_{ox} I_{tail}} \tag{3.29}$$

where μ_p is the mobility parameter for PMOS, W is the transistor width, L is the transistor length, C_{ox} is the oxide capacitance, and V_{dsat} is the voltage difference between the gate to source voltage (V_{gs}) and the threshold voltage (V_{th}) of the transistor defined as,

$$V_{dsat} = V_{gs} - V_{th} = \sqrt{\frac{I_{tail}}{\frac{W}{L}\mu_p C_{ox}}}. \tag{3.30}$$

It can be observed, that the g_m can be increased by having a large I_{tail}, a large W/L ratio, or by increasing both parameters. However, increasing I_{tail} will also increase the power consumption of the amplifier, and increasing the W/L ratio will reduce V_{dsat} too much, making the amplifier sensitive to process variations [79, 83].

The equivalent input referred noise for low and moderate frequencies in a MOS transistor is typically expressed as,

$$V_n^2(f) = V_{thermal}^2 + V_{flicker}^2 = 4kT\left(\frac{2}{3}\right)\frac{1}{g_m} + \frac{K_f}{WLC_{ox}f} \tag{3.31}$$

where K_f is a device-dependent parameter, and assuming two uncorrelated noise sources. It can be observed that to reduce the thermal noise contribution from the amplifier, a large g_m is needed, but this will require a large I_{tail} and/or large W in the transistors. It is important to notice that the noise of transistors $M_3 - M_5$ is attenuated by the g_m of the input transistor, minimizing their contribution to the equivalent input noise. Thus, the input transistor's noise contribution is critical and must be minimized. To reduce their flicker noise contribution, a large W and L are needed but at the expense of increased

active area. The input transistors (M_1, M_2 in Fig. 3.41) in A_1 are frequently chosen as PMOS transistors since the K_f is smaller than in the NMOS. Also, wide L are typically used to minimize their flicker noise contribution in the audio bandwidth.

The GBW and A_{DC} for the amplifier topology shown in Fig. 3.41 are,

$$GBW = \frac{g_{m1,2}}{2\pi \cdot C_C} \tag{3.32}$$

$$A_{DC} = \frac{g_{m2}}{g_{ds4}} \left(\frac{g_{m5}}{g_{ds5}} \right) \tag{3.33}$$

where g_{ds} is the drain to source conductance of the transistor, and assuming that $M_1 = M_2$ and $M_3 = M_4$. Typically, the g_m is chosen as a function of the desired GBW as expressed in (3.32). Then, the g_{ds} of the transistors are designed to satisfy the required DC gain. To choose the amplifier's GBW, several tradeoffs need to be considered such as the SR, power consumption, and its effect on (3.24).

The amplifier's SR imposes a limitation in the large signal operation of the compensator. In the two-stage miller-compensated amplifier topology, the worst case SR for a unity gain configuration can be expressed as [79, 83, 84],

$$SR \cong \frac{I_{tail}}{C_C} = \frac{I_{tail} \cdot 2\pi \cdot GBW}{gm_{1,2}} = 2\pi \cdot GBW \cdot V_{dsat_{1,2}}. \tag{3.34}$$

The full-power bandwidth is defined as the maximum frequency (f_{max}) at which the amplifier will yield an undistorted AC output with the largest possible amplitude (V_{max}) [83]. The minimum SR requirement for amplifier A_1 using this definition is,

$$SR_{min} \geq 2\pi \cdot f_{max} \cdot V_{max}. \tag{3.35}$$

The compensation's amplifier A_1 has to process the input audio signal and the high frequency feedback signal. Therefore, the f_{max} would correspond to the feedback's switching frequency, and V_{max} to the peak voltage of the error signal in the system. To specify a minimum GBW requirement, the small signal behavior in (3.34) could be related to the large signal by using (3.35), and solving for GBW [84]. The minimum GBW needed in A_1 amplifier can be expressed as,

$$GBW_{min} \geq \frac{f_{max} \cdot V_{max}}{V_{dsat_{1,2}}}. \tag{3.36}$$

Several design alternatives are possible taking into account the tradeoffs present in (3.36). Also, the $V_{dsat_{1,2}}$ design choice presents tradeoffs in the amplifier A_1 between its DC gain, offset voltage, noise, bandwidth, and stability [79, 83].

Table 3.5: Design procedure for active integrator

1.	Choose R_1, R_2 values based on the desired output noise.
2.	Determine $C_1 = 1/(\omega_{int} \cdot R_1)$.
3.	Find minimum GBW to satisfy (3.36).
4.	Select C_C to ensure stability for the obtained GBW_{min}.
5.	Calculate minimum I_{tail} to satisfy (3.34).
6.	Find required $g_{m1,2}$ using (3.32).
7.	Select input transistor's width to meet (3.29), using a wide length value to lower noise contribution.
8.	Design remaining transistors $M_3 - M_5$ to ensure high DC gain.

Table 3.5 summarizes the design procedure for the active integrator used in the compensator to determine the component values of the amplifier given the output noise, V_{max}, f_{max}, $V_{dsat1,2}$, and ω_{int}. For this example implementation, the input resistors R_1, R_2 were chosen as 400 kΩ and the integrating capacitor C_1 as 8 pF. This will result in an integrated noise in the 20 kHz bandwidth of 11.37μV at 300° K. The A_1 amplifier's uses

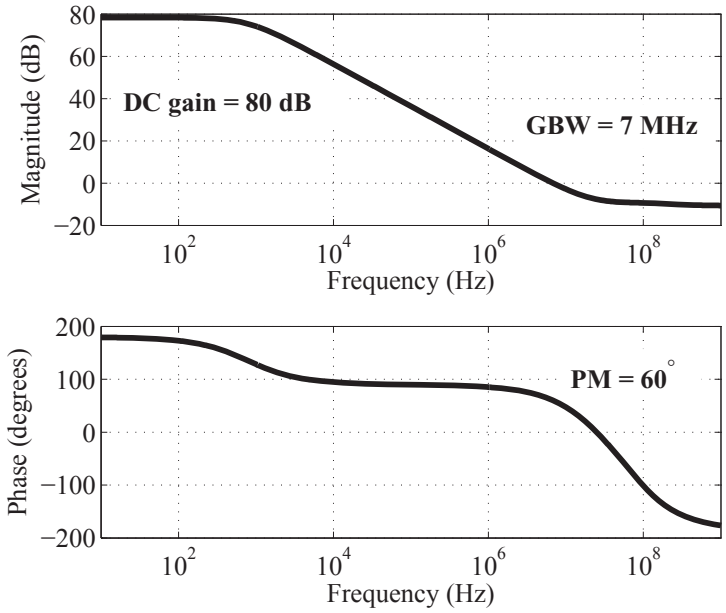

Figure 3.42: Bode plot of two-stage example amplifier.

$V_{dsat_{1,2}} = 100\ mV$ for a $f_{max} = 500\ kHz$ with $V_{max} = 0.9\ V$, which would require a minimum GBW of 4.5 MHz. Since the GBW parameter is chosen to satisfy (3.36), the A_1 amplifier's DC gain is selected taking into the account the tradeoffs between the integrator performance and the amplifier's power and area consumption, as detailed in (3.29) to (3.33). For an integrating capacitor (C_1 in Fig. 3.40) of 8 pF, a C_C for phase margin of 60° is typically chosen as $C_C > 0.22C_1$ [79]. Thus, a C_C= 2pF is chosen.

The required g_m for the C_C and GBW selection is 60 μS, consuming an $I_{tail} = 6\ \mu A$ for a $V_{dsat} = 0.1\ V$, as expressed in (3.29).

The remaining transistors $M_3 - M_5$ in A_1 are designed to maximize their conductance to obtain high DC gain, as expressed in (3.33). The simulated frequency response of the designed amplifier is shown in Fig. 3.42, where the DC gain and GBW requirements are satisfied, and showing a stable system with PM of 60°. This design selection yields a magnitude and phase deviation in the integrator function of 0.0025% and 0.4° as expressed in (3.26), respectively.

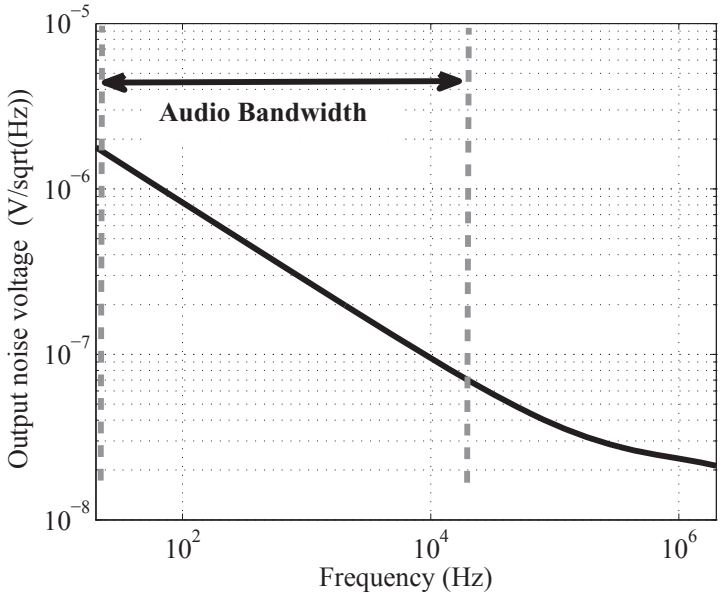

Figure 3.43: Equivalent output noise voltage for the example amplifier.

The equivalent output noise voltage for the designed amplifier example is shown in Fig. 3.43. The integrated noise in the audio bandwidth is 13 μV at 300° K, that is comparable to the input resistor noise.

This is important since these two noise sources will dominate the output noise of the CDA. If the resistor noise is higher than the amplifier noise, then the amplifier can lower its power consumption to have less or equal noise than the input resistors. On the other hand, if the resistor noise is lower than the amplifier noise, then the amplifier has to increase its power consumption to have less or equal noise than the input resistors, or to drive a larger capacitance since the resistor value decreased to lower its noise.

The total amplifier power consumption from a 1.8 V supply is 56 μW, where the first stage consumed 18 μW and the second stage consumed 38 μW. The second stage often consumes more power than the first stage to push the output pole to high frequencies, ensuring a single pole frequency response in the amplifier [79, 83].

3.3.2 Pulse-width modulator

The PWM circuit is typically implemented using a comparator with large DC gain [79]. The comparator can be designed as a push-pull open loop amplifier, , as shown in Fig. 3.44, to achieve high slew rate to minimize propagation delay and with high PSRR to suppress the supply noise contribution at its output.

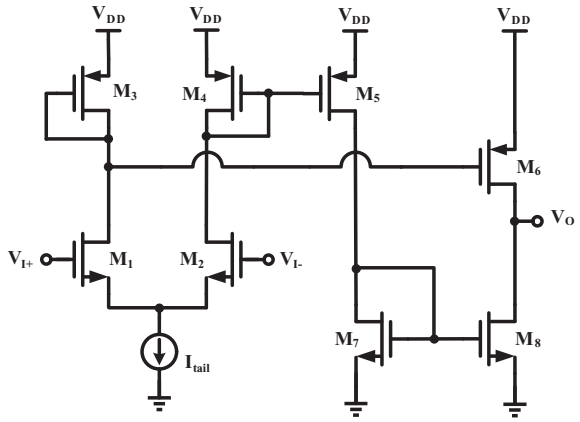

Figure 3.44: Comparator schematic diagram with push-pull output stage.

The comparator takes the input voltage difference and amplifies it such that the output is pushed up to the supply voltage or pulled down to ground. The DC gain of the comparator is given by,

$$A_{DC,comp} = \frac{g_{m1}}{g_{m3}} \left[\frac{(W/L)_6}{(W/L)_3} \right] \cong \frac{(W/L)_1}{(W/L)_3} \left[\frac{(W/L)_6}{(W/L)_3} \right] \tag{3.37}$$

where transistors are assumed as $M_1 = M_2$, $M_3 = M_4$, $M_5 = M_6$, and $M_7 = M_8$. The main advantage of this implementation is that all the internal nodes appear as high impedance, minimizing the signal propagation delay from input to output. Thus, all the transistors are sized with small widths and lengths. The output transistors M_6 and M_8 can provide almost rail-to-rail output voltage, and are sized such that they can charge and discharge the output node very fast.

The power consumption in the comparator implementation of Fig. 3.44 depends on the operating frequency of the PWM carrier signal and the load capacitance of the comparator. The load capacitance (C_{load}) is typically the gate capacitor of a digital inverter in the range of 10-30 fF. Thus, the comparator power dissipation (P_{comp}) due to charging and discharging of the load capacitor and its quiescent current can be expressed as,

$$P_{comp} = P_Q + P_{SW} \cong V_{DD} \cdot I_{tail} + C_{load} \cdot V_{DD}^2 \cdot F_{SW}. \tag{3.38}$$

The goal of the comparator is to minimize its propagation delay by reducing the rise/fall time of its output. A rule-of-thumb is to target a rise/fall time of 0.5% of the switching period. For example, for a $F_{SW} = 500\ kHz$ with switching period of 2μs, the desired maximum rise/fall time is 10 ns. To avoid being slew rate limited, the minimum I_{tail} needs to be higher than 5 μA, as expressed in (3.34).

If the F_{SW} is increased to 2 MHz, then the minimum I_{tail} will increase to 20 μA or 4X times more power. Thus, increasing the F_{SW} will directly increase the power consumption of the comparator.

Table 3.6: Design procedure for PWM comparator

1. Choose minimum I_{tail} to satisfy (3.34) and (3.35) for a given F_{SW} and $C_C = C_{load}$.
2. Determine $(W/L)_1/(W/L)_3$ using (3.37) to maximize DC gain.
3. Select M_1 transistor's width, using minimum lengths to maximize (3.37)
4. Select M_3 transistor's width, using large lengths to maximize (3.37)
5. If more DC gain is needed, $(W/L)_6/(W/L)_3$ can be increased.

Table 3.6 provides a concise design procedure for the comparator in Fig. 3.44. For example, a $F_{SW} = 500\ kHz$ with switching period of 2μs will require a minimum I_{tail} = 5 μA for a desired maximum rise/fall time of 10 ns in a $C_{load} = 10fF$. For a DC gain of 60 dB or 1000 V/V, a $(W/L)_1 = 1000 \cdot (W/L)_3$ is needed. Thus, the transistor sizes are selected as $(W/L)_1 = 18\mu m/0.18\mu m$ and $(W/L)_3 = 0.36\mu m/4\mu m$, having a DC gain of 60.91 dB or 1111 V/V.

The triangle wave signal is typically generated from a relaxation oscillator as shown in Fig. 3.45, where the output triangle wave signal (V_{TRI}) is used as the input for two comparators that will set the voltage limits of V_{TRI}. The output of the comparators are used to control a set-reset (SR) latch that generates the gate voltages for switches M_1 and M_2. The comparators used to set the voltage limits have to be fast and glitch free to avoid errors or peaking during the transitions. The SR-latch should have small metastability and small delay to avoid deviation from the desired F_{SW}.

The current sources should have high output conductance to avoid distortion of the carrier signal. The switches' on-resistance have to be small enough to avoid voltage drops during each switching cycle.

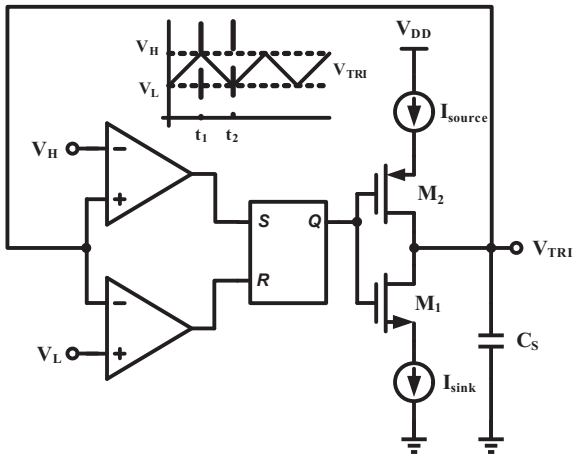

Figure 3.45: Triangle wave generator circuit.

The operation is as follows: During the period t_1, M_2 is on and M_1 is off; thus, the capacitor C_S is charged with a constant current given by I_{source} to ramp up V_{TRI} until it exceeds the high voltage threshold V_H. Then, during the period t_2, M_1 is on and M_2 is off; thus, C_S is discharged with a constant current given by I_{sink} to ramp down V_{TRI} until it falls below the low voltage threshold V_L. This process is repeated each cycle and the period of the carrier wave signal is $T_{SW} = t_1 + t_2$. Thus, the F_{SW} can be expressed as,

$$F_{SW,tri} = \frac{I_{sink}}{2C_S(V_H - V_L)} \tag{3.39}$$

where $I_{sink} = I_{source}$ is assumed. If the current sources are not equal, then the output triangle waveform will be distorted. The main design tradeoffs are between the area occupied by the capacitor and the current sources power consumption. A large C_S value will allow

low power consumption but will occupy considerable area to implement it. A small C_S value will occupy small area but will consume large power. Also, if the I_{sink} is large, the drop across the on-resistor of the switches is more prominent, requiring large transistors to minimize the voltage drop.

The distortion of the output waveform results from the cropping of the peaks and valleys of V_{TRI}. If the output swing is rail-to-rail, then when the output signal is near a rail, the voltage drop across the current sources and the switches will limit the maximum output swing, distorting the output waveform.

The resulting $F_{SW,tri}$ is highly dependent on the variations of C_S. Thus, the capacitor choice needs to consider the sensitivity of the material used to implement it under different voltage conditions. The circuit is sensitive to variations in the supply and in its limit voltages. For this example implementation, a V_H=1.35 V, V_L=0.45 V, and C_S=1 pF, will require an $I_{sink} \cong 1\ \mu A$. The V_{TRI} will have an amplitude of 0.9 V_{PP} centered around 0.9 V that is the common mode voltage of the system.

3.3.3 Class-D output stage

The class-D output stage is typically designed to minimize its dynamic power dissipation and its conduction power dissipation without degrading the propagation delay [60]. This is to achieve high power efficiency as discussed in Section 3.1.2. A typical implementation is shown in Fig. 3.46, where a non-overlapping signal generator is used to avoid excessive short-circuit current through the class-D output stage. The non-overlap delay (t_{ov}) is chosen as a tradeoff between efficiency and distortion [85]. Nevertheless, due to the large gate capacitance of the output stage transistors, a driver stage implemented as a tapered buffer is used to charge and discharge these large gate capacitances with minimum power-delay product [86].

For this design example, nominal 1.8 V devices are used to implement the output power stage. Nonetheless, higher output power capabilities could be expanded using high voltage devices such as thick oxide,LDMOS, or DMOS transistors depending on the desired application [8, 62].

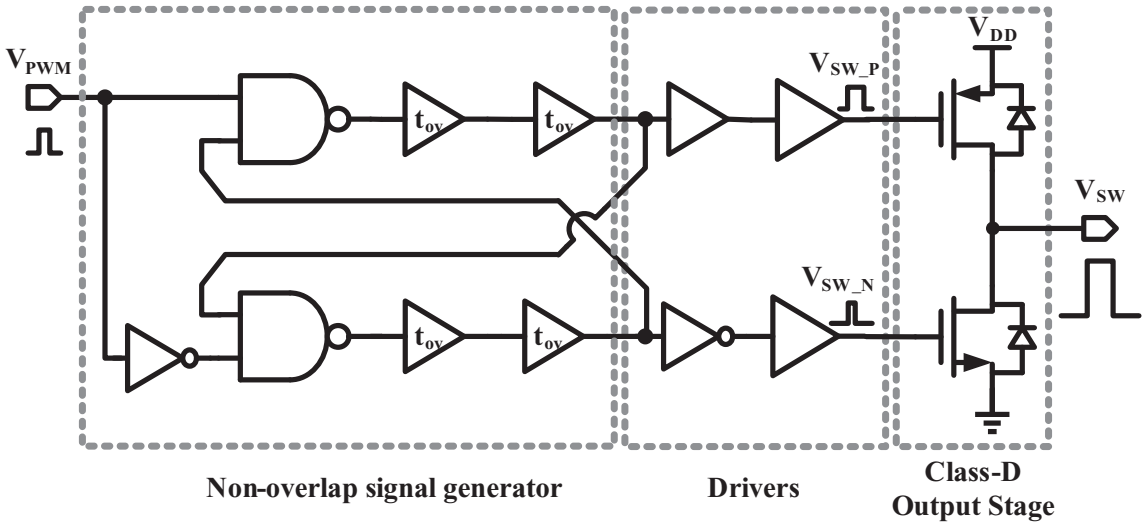

Figure 3.46: Class-D output stage with auxiliary circuits.

The class-D output stage as shown in Fig. 3.46 is commonly known as a single-ended or half-bridge output stage. Its output transistors need to be carefully sized to avoid the dynamic or conduction losses to dominate the overall efficiency performance. Fig. 3.47 illustrates the design tradeoffs when choosing the width for the NMOS and PMOS transistors for a minimum length of 180 nm.

For example, for a typical EM speaker with an 8 Ω impedance, a $R_{dsON} = 0.2$ Ω will limit the efficiency to 97 % at high output power, as expressed in (2.10) and (3.2). Thus, from Fig. 3.47, the PMOS need to have a width of 12 mm, and the NMOS need a width of 3 mm. This will result in gate capacitance for the PMOS of 16 pF, and 4 pF for the NMOS.

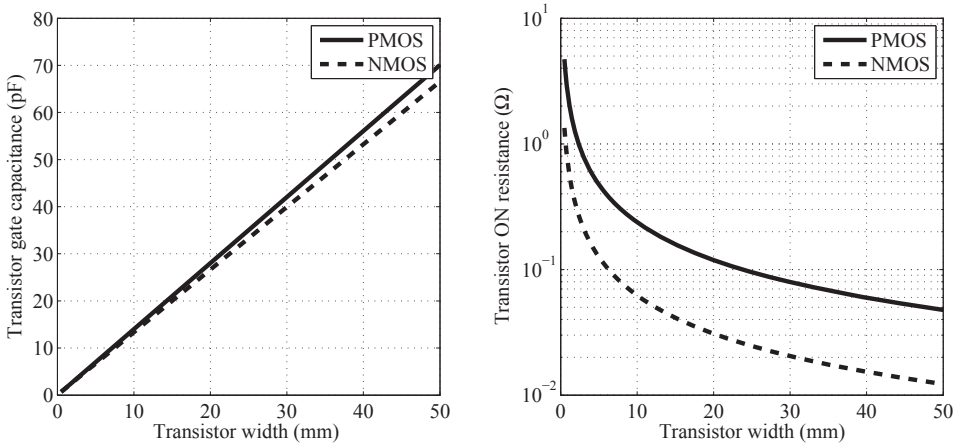

Figure 3.47: Transistor gate capacitance and R_{dsON} versus transistor width.

It can be noticed that further reducing the R_{dsON} will dramatically increase the gate capacitance, increasing the switching losses, and decreasing the power efficiency in the CDA at low output power. Since the transistors have large widths, their substrate area is large, resulting in a parasitic body-diode that plays a role in the power losses of the output stage, as expressed in (3.5). A sample design procedure for the half-bridge output stage is illustrated in Table 3.7.

The maximum output power that the half-bridge output stage in Fig. 3.46 can provide to an EM speaker is a function of its supply voltage and the load impedance. The power rating can be expressed as,

$$P_{O,max} = V_{O,max} \cdot I_O = \frac{V_{O,max}^2}{R_{load}} \tag{3.40}$$

where $V_{O,max}$ is the maximum RMS voltage of the audio signal. For this implementation example, the common mode level is 0.9 V for a supply voltage of 1.8 V; thus, the audio signal amplitude swings from 1.8 V to 0 V, resulting in a maximum peak voltage of 0.9 V. Then, the $V_{O,max}$ is 0.636 Vrms, resulting in a $P_{O,max}$ of 50.6 mW for an 8 Ω EM speaker, or 101.12 mW for a 4 Ω EM speaker. .

To increase the power rating of the CDA without increasing the supply voltage, a full-bridge configuration as shown in Fig. 3.48 can be used as the class-D output stage, where the output audio signal is taken differentially as the voltage across the speaker load.

Table 3.7: Design procedure for half-bridge output stage

1.	Determine maximum $I_{load} = V_{out}/\lvert Z_{load}\rvert$ for a given loudspeaker impedance and supply voltage.
2.	Choose desired efficiency region to optimize from Fig. 3.4
3.	Plot the NMOS and PMOS transistor's width versus $R_{ds,on}$ and gate capacitance, as in Fig. 3.47
4a.	For region I, choose the NMOS and PMOS transistor's width for the desired gate capacitance to minimize P_{SW}.
4b.	For region II, determine the NMOS and PMOS transistor's width based on where the $R_{ds,on}$ and gate capacitance plot intersect each other.
4c.	For region III, choose NMOS and PMOS transistor's width for the minimum $R_{ds,on} = R_{load}(1-\eta)/\eta$.

This configuration is also known as a Bridge-tied Load (BTL) or H-bridge output stage.

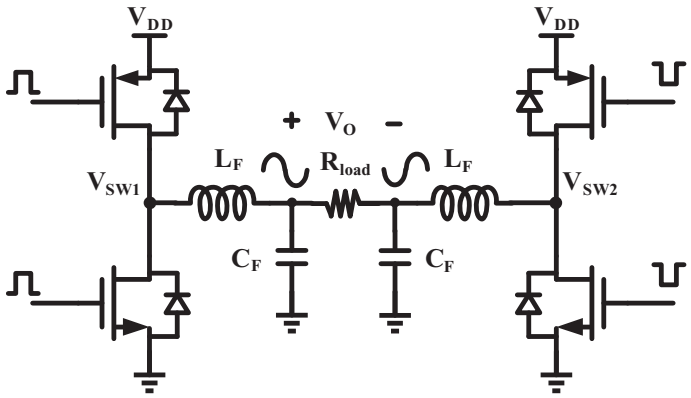

Figure 3.48: Full-bridge class-D output stage.

Since each side or leg of the H-bridge process the full audio signal amplitude but with 180° phase difference between each leg, the output voltage swing compared to the half-bridge output stage is doubled, increasing 4 times the output power.

Also, the output signal even harmonics get ideally canceled by the subtraction operation, including the DC voltage. For the same example as in the half bridge, the $V_{O,max}$ is 1.272 Vrms, resulting in a $P_{O,max}$ of 202 mW for an 8 Ω EM speaker or 404.5 mW for a 4 Ω EM speaker.

To implement the H-bridge output stage, the active area used for the output switches and the cost of components in the output filter are doubled, since you need a complete half-bridge for each side, as observed in Fig. 3.48. Also, the CDA power consumption is doubled since the output signal is differential and needs to be translated to a single-ended configuration using an additional block in the feedback.

A design procedure for the full-bridge output stage is presented in Table 3.8.

Table 3.8: Design procedure for full-bridge output stage

1.	Determine maximum $I_{load} = 2V_{out}/\lvert Z_{load}\rvert$ for a given loudspeaker impedance and supply voltage.
2.	Choose desired efficiency region to optimize from Fig. 3.4
3.	Plot the NMOS and PMOS transistor's width versus $R_{ds,on}$ and gate capacitance, as in Fig. 3.47, for half-bridge of the output stage.
4a.	For region I, choose the NMOS and PMOS transistor's width for the desired gate capacitance to minimize P_{SW}.
4b.	For region II, determine the NMOS and PMOS transistor's width based on where the $R_{ds,on}$ and gate capacitance plot intersect each other.
4c.	For region III, choose NMOS and PMOS transistor's width for the minimum $R_{ds,on} = R_{load}(1-\eta)/\eta$.
5.	Duplicate the designed transistors to create the full-bridge output stage.

Another alternative is to use a differential CDA architecture, as observed in Fig. 3.49. Compared with the SE CDA architecture shown in Fig. 3.40, the differential CDA architecture doubles the amount of components needed to implement the system, increasing the area and power consumption of each block in the loop. Pseudo-differential or fully-differential amplifier configurations could be used in the compensator to process the two feedback paths [57, 87]. The main advantage is that the differential output voltage is processed differentially by the loop, enhancing greatly the audio performance.

One drawback in the H-bridge output stage is when the audio signal is not present, the switching signals ($V_{SW1,2}$) are still existing, and the differential switching signal ($V_{SW1} - V_{SW2}$) is changing from V_{DD} to -V_{DD}.

Thus, some output current ripple is still present across the output filter, dissipating power. One alternative to decrease considerably this ripple is to switch the outputs $V_{SW1,2}$ in phase such that when no signal is present both cancel each other, reducing the signal across the load, as shown in Fig. 3.50. This switching strategy is commonly know as filter-less modulation or three level modulation [42, 63], and its typical waveform is illustrated in Fig. 3.51 to contrast it with the conventional H-bridge switching.

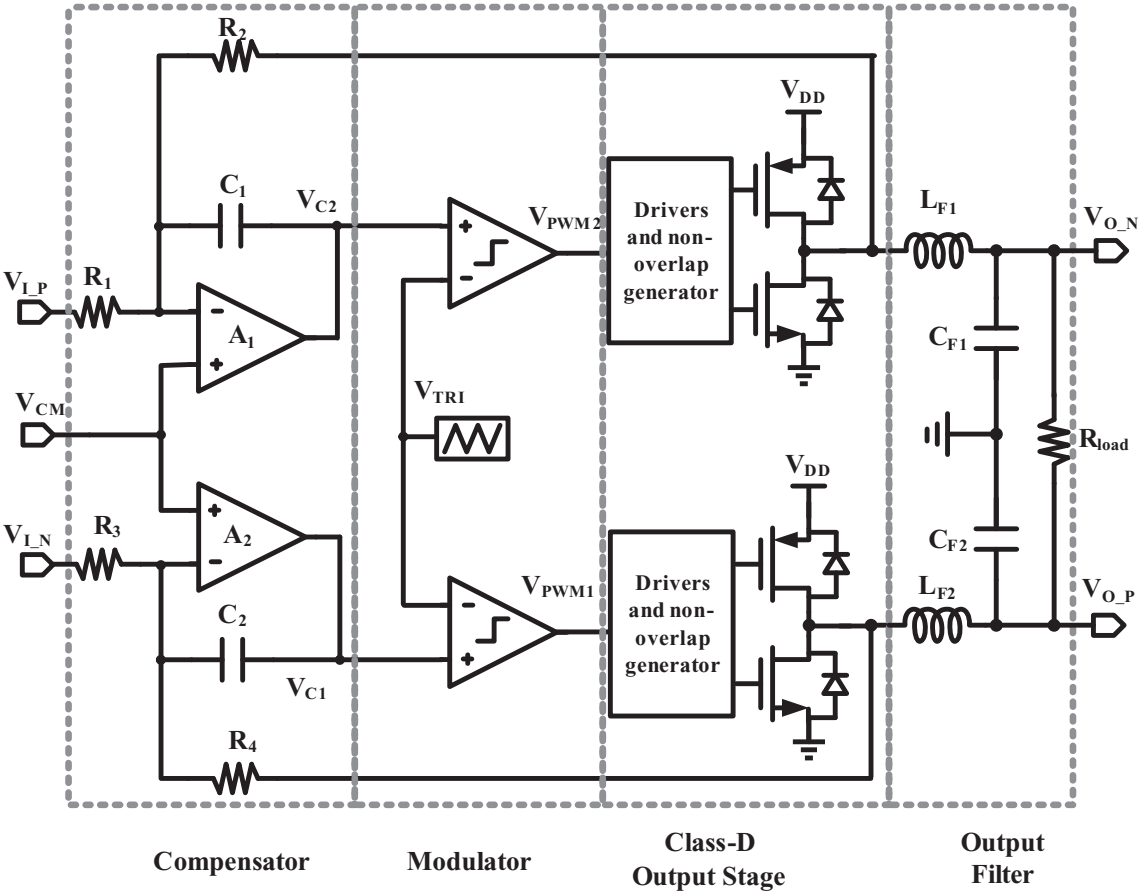

Figure 3.49: First-order differential PWM CDA architecture.

The main advantage of the three level switching is that the frequency components of the carrier signal are doubled, allowing smaller filter components, or, if the EM speaker has high inductance, to completely remove the output filter at the expense of THD+N degradation and large EMI.

A more complex approach to cancel more harmonics in the switching output signal requires multiple power transistors at the output stage operating from two different supply voltages, as shown in Fig. 3.52 [43].

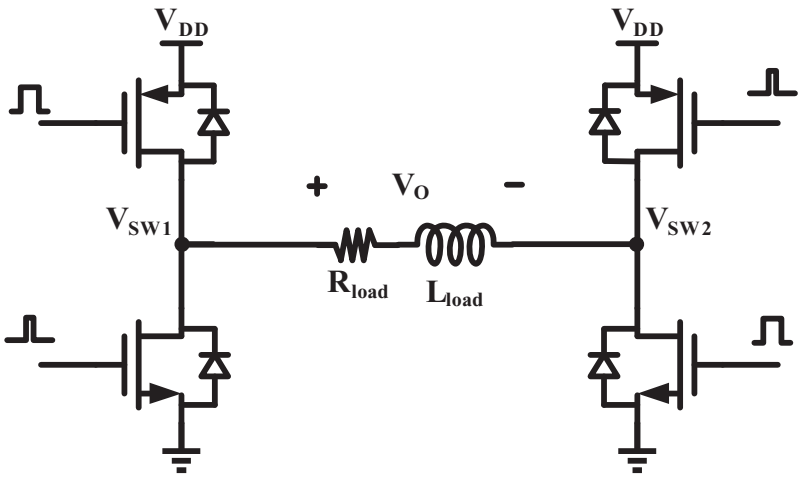

Figure 3.50: Filterless class-D output stage.

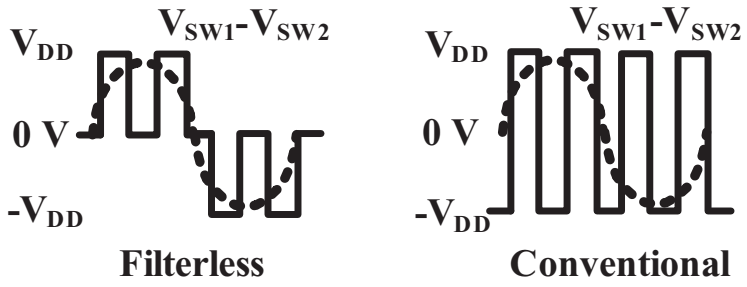

Figure 3.51: Filterless and conventional H-bridge switching comparison.

This approach will achieve a multilevel switching signal which in turn will increase the linearity of the quantization process by increasing the number of effective bits, as expressed in (3.13). Its switching output waveform is shown in Fig. 3.53 where 5 quantization levels can be observed.

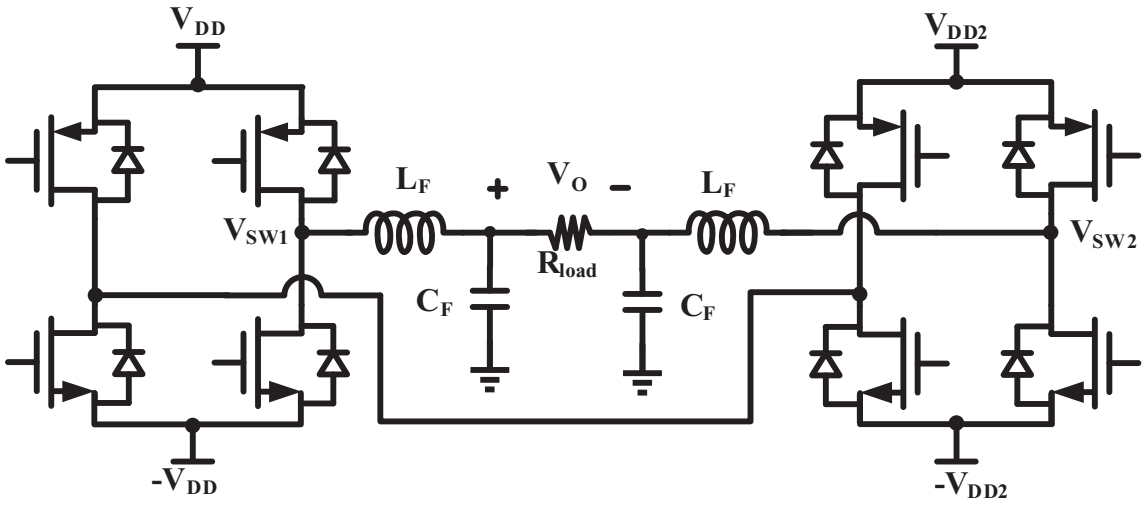

Figure 3.52: Multilevel class-D output stage.

The main drawbacks is the need for 8 switches, two floating supplies, and a complex switching strategy. The power consumption of this technique dramatically limits the efficiency, making it not practical for mobile devices applications. Also, any timing error in the switching signals of any transistor will reduce the effectiveness of the linearity enhancement.

The effect of increasing the effective F_{SW} can also be achieved by using a single voltage supply but multiple phases in an interleaved output stage as shown in Fig. 3.54 where 3 different phases separated 60° apart from each other are used to process the output signal.

The main drawback of this output stage is that an extra inductor is needed for each additional clock phase [88, 89, 90].

The multilevel and multiphase approach have also been used in DC-DC buck converters to reduce the output voltage and current ripple, and to lower the RMS current flowing into each inductor. However, since each additional clock phase or output level requires an extra inductor, the multiphase approach in Buck converters is practically limited to 3 levels [91].

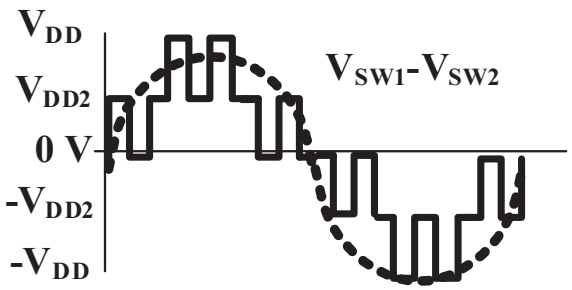

Figure 3.53: Switching output waveform with 5 quantization levels.

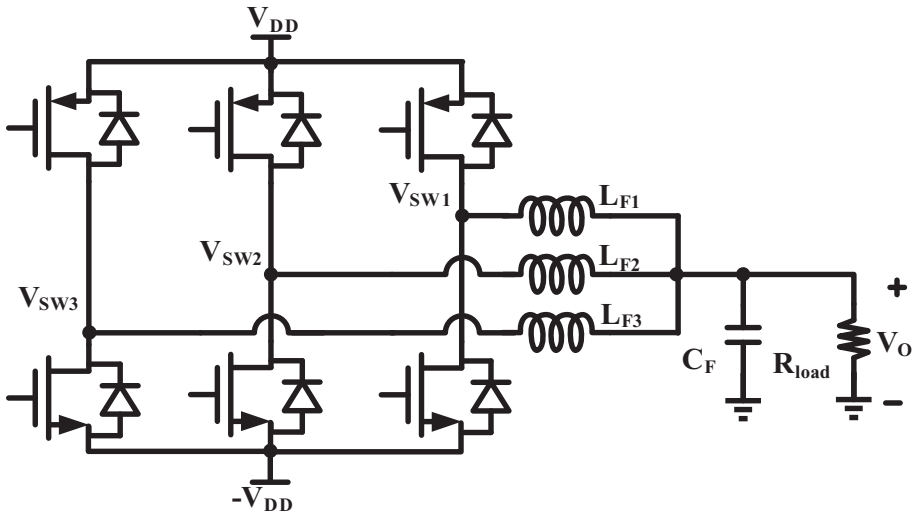

Figure 3.54: Multiphase interleaved class-D output stage.

3.3.4 Output filter

The main function for the output filter is to recover the low frequency audio signal from the modulated output. An off-chip second-order low-pass filter is typically used. Since the output current flows through the output filter components, an inductor and capacitor are typically used to avoid extra power dissipation. Fig. 3.55 show two typical configurations for the half-bridge output stage when a dual supply or single supply are used.

The EM speaker must not have a DC component to avoid damaging the transducer. Thus, the single supply configuration must have a large decoupling capacitor to remove the DC component. The transfer function for the LC filter with single supply and decoupling capacitor shown in Fig. 3.55 can be expressed as,

$$\begin{aligned} \frac{V_O(s)}{V_{SW}(s)}_{Single} &= \frac{\omega_{LC}^2}{s^2+\omega_{LC}^2}\left(\frac{s}{s+\omega_z}\right) \\ &= \frac{1/(L_F C_F)}{s^2+1/(L_F C_F)}\left(\frac{s}{s+1/(C_D R_{load})}\right) \end{aligned} \tag{3.41}$$

where the cutoff frequency of the filter is given by $L_F C_F$ and the decoupling capacitor C_D creates a high pass filter characteristic with the load.

The transfer function for the LC filter with dual supply shown in Fig. 3.55 is expressed as,

$$\begin{aligned} \frac{V_O(s)}{V_{SW}(s)}_{Dual} &= \frac{\omega_{LC}^2}{s^2+s\cdot 2\cdot\zeta\cdot\omega_{LC}+\omega_{LC}^2} \\ &= \frac{1/(L_F\cdot C_F)}{s^2+s\cdot(R_{load}/L_F)+1/(L_F\cdot C_F)} \end{aligned} \tag{3.42}$$

where it can be observed that the EM speaker equivalent resistance will determine the damping factor (ζ) of the LC filter.

The filter design presents several tradeoffs between the cut-off frequency, the F_{SW} of the system, the linearity of the components, and its power dissipation. The selection of the damping factor can affect the linearity of the audio signal if peaking is present in (3.42). Also, the inductor value selection will affect the amount of current high frequency ripple that will create power losses in the non-idealities of the components.

For this example implementation, the dual supply filter was designed with a cutoff frequency of 22.5 kHz, and the filter components were chosen as $L_F = 50\ \mu H$, $C_F = 1\ \mu F$, and $R_{load} = 8\ \Omega$. This selection will result in a Butterworth filter approximation which gives a flat magnitude response and a linear phase response. A blocking capacitor $C_D = 10\ \mu F$ is included to remove the DC component applied to the speaker.

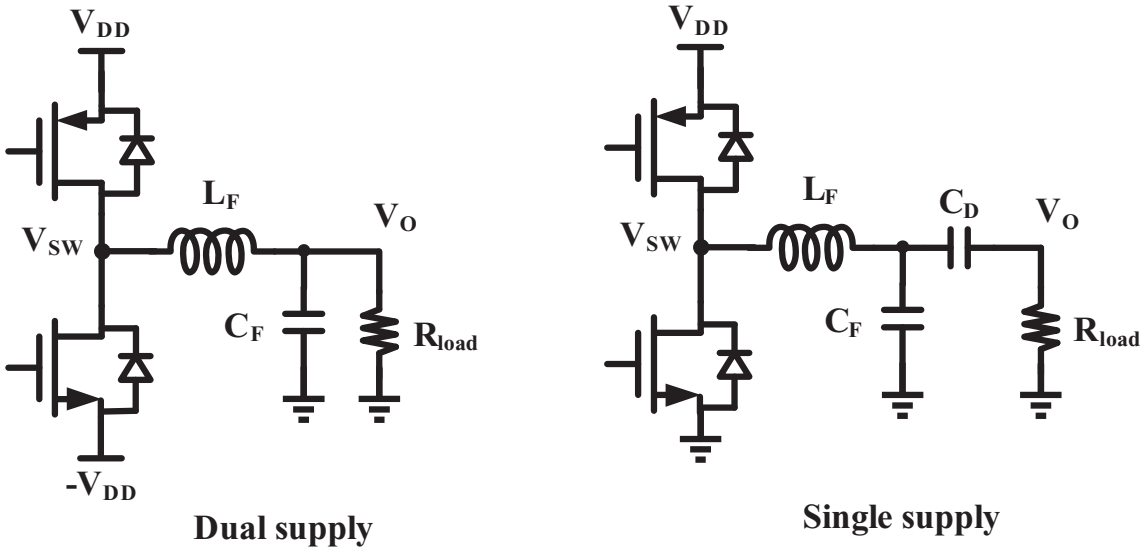

Figure 3.55: Single-ended output filter configurations.

3.3.5 Current and voltage sensor techniques

Some close loop CDA architectures need to monitor the output voltage and output current to determine the correct operation of the system [64]. Also, when the current and voltage information is available, intelligent signal processing can be achieved to extract the real time impedance of the speaker, and calibrate the system to maximize the output power and efficiency [92]. Another useful function is the over-current protection of the output stage. The output voltage is easily monitored with the feedback loop since most CDA operate in voltage domain. Thus, a simple wire line connection is enough to sense the output voltage. The main challenge is to accurately monitor the output current. Several current sensing techniques have been explored in DC-DC power converters [93, 94]. Most of the techniques imply adding extra components in series or parallel to the output stage or output filter to extract the output current information. A brief overview of the most used techniques will be discussed next.

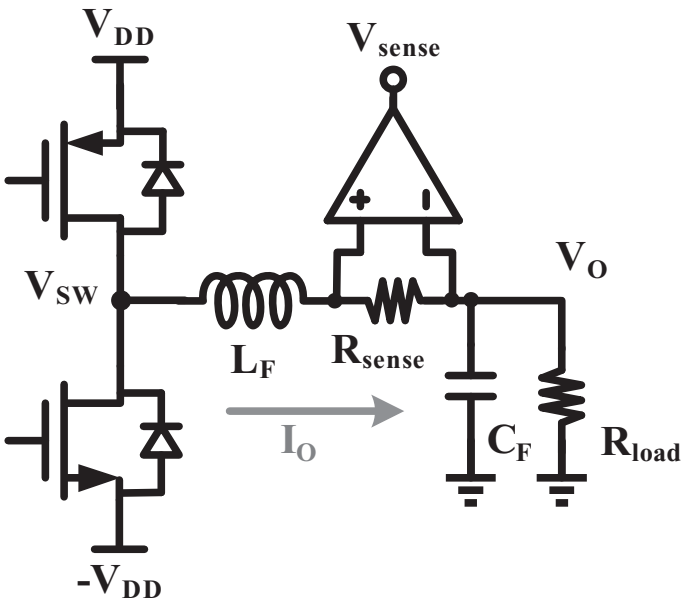

Figure 3.56: Current sensing method using inductor series resistor.

The simplest method to measure the output current is to extract it from the inductor current using a sensing resistor (R_{sense}) in series with the inductor as shown Fig. 3.56, where the sensing voltage ($V_{sense} = I_O \cdot R_{sense}$) is frequency independent and proportional to I_O.

The drawback of this technique is that R_{sense} is in the high current path, dissipating power. Also, its dynamic range is very limited since to sense small I_O, a large R_{sense} would be needed, but when I_O increases, the large R_{sense} would saturate the sensing amplifier output.

Another simple method is to use a current transformer or coupled inductor as the inductor in the output filter, as illustrated in Fig. 3.57. This sensing technique dissipate very little power since the transformer is magnetically coupled to the inductor filter and attenuates the sensing current by its transformer gain determined by the N turns around the magnetic core; the sensing voltage is given by $V_{sense} = I_O/N \cdot R_{sense}$. R_{sense} is also used to convert the output current of the transformer to voltage.

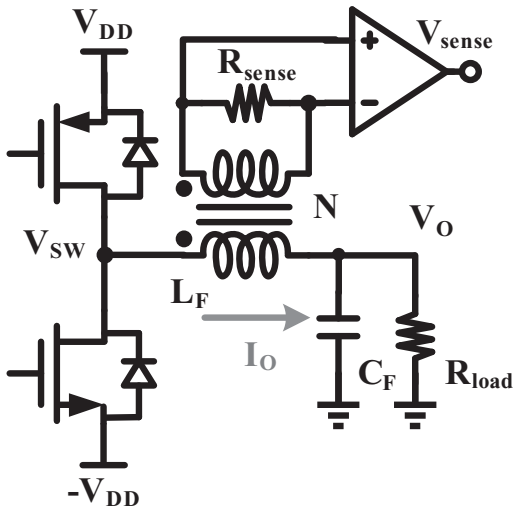

Figure 3.57: Current sensing method using current transformer.

The main drawback of this technique is that the current transformer is a bulky and expensive component that requires large PCB area to avoid EMI with other components. Also, its frequency response has to be high enough to process the carrier signal. The

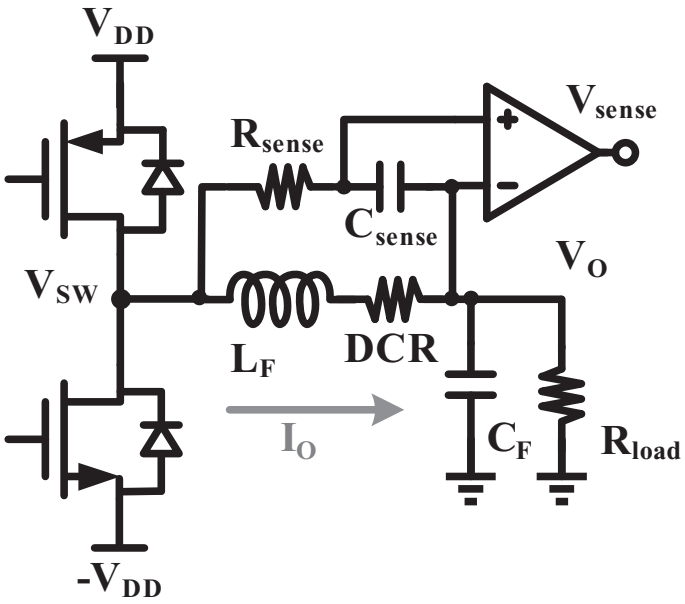

Figure 3.58: Current sensing method using DCR sensing.

sensing technique in Fig. 3.58 uses the parasitic inductor resistance (DCR) to sense the current across it. The DCR is not an explicit component and must be extracted from the inductor frequency response. In other words, the inductor and DCR have a high pass frequency response. Thus, a low pass frequency response is needed to cancel flatten the frequency response, and extract the DCR magnitude which is proportional to the output current.

The sensing voltage for the DCR sensing technique can be expressed as,

$$V_{sense} = \left(\frac{1 + sL_F/DCR}{1 + sR_{sense}C_{sense}} \right) \cdot DCR \cdot I_O. \tag{3.43}$$

The main drawback of this technique is that the inductor and DCR exact values are needed, and they depend on the manufacturer that provides accuracies up to 20%. Thus, the technique is not accurate and highly sensitive to component variations.

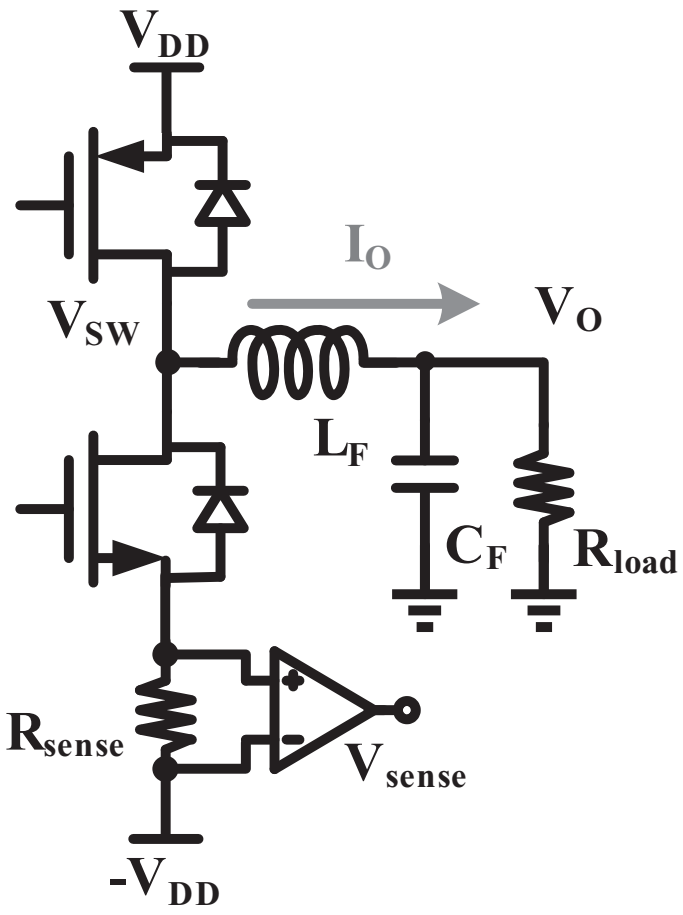

Figure 3.59: Current sensing method using source sensing resistor.

All the previous current sensing technique have the drawback that require external components. Thus, the terminal capacitance, the lead inductance and resistance of each external component will affect the accuracy of the measurement. Thus, a current sensing technique that can be fully integrated on the same die as the output stage is desired to have high accuracy in the measurement.

A fully integrated current sensor can be implemented using an on-chip sensing resistor in series with the NMOS transistor, as illustrated in Fig. 3.59. This resistor is typically implemented as a low value metal resistor. However, it only monitors the output current when the NMOS transistor is active, and the sensing resistor dissipates power. This is a simple current sensing scheme that is typically preferred for over-current applications.

A more practical fully integrated sensing technique with good accuracy is shown in Fig. 3.60, where a sensing transistor K times smaller than the output transistor is used to extract the output current. The amplifier is used to force the same V_{DS} drop across both transistors. Since both transistor have the same V_{GS} and V_{DS}, the current flowing through the R_{sense} is an attenuated copy of the current in the output transistor.

The main drawback of this technique is that the output current is only measured when the PMOS is active. The other half of the cycle the current is not monitored. A similar sensing scheme would be needed for the NMOS transistor to monitor the complete cycle, at the expense of extra power consumption. The sensing voltage for the current mirror MOSFET sensor can be expressed as,

$$V_{sense} = \frac{I_O}{K} \cdot R_{sense} \tag{3.44}$$

where K is the width ratio between the output and sensing transistor.

Another drawback for this sensing technique is the matching between transistors. The output transistor is typically implemented as hundreds of small transistors in parallel, while the sensing transistor is implemented as a single transistor. Thus, the process variations across the chip affect each transistor differently, degrading the accuracy of the measurement. Also, the high frequency switching noise is passed to V_{sense} by the amplifier, requiring filtering to accurately sense small currents.

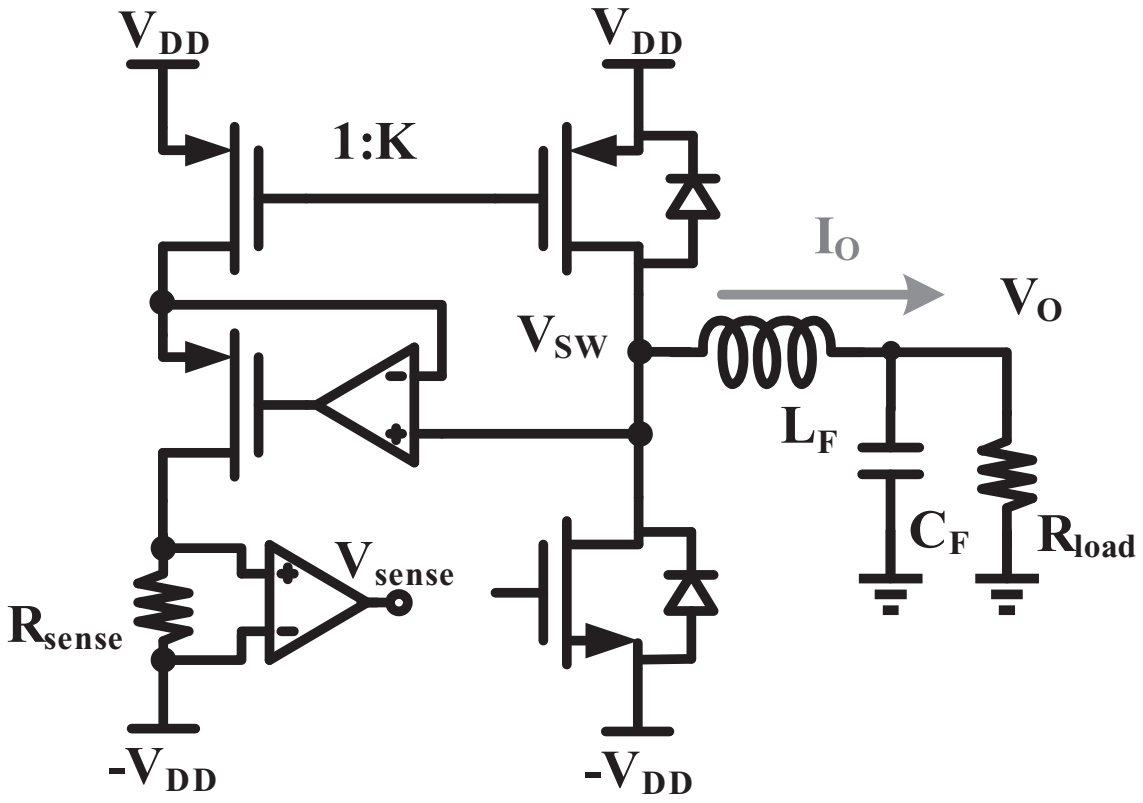

Figure 3.60: Current sensing method using a current mirror MOSFET.

Table 3.9 summarizes the tradeoffs for each of the discussed current sensing techniques [93, 94]. Each technique is useful and has its applications. However, for CDA applications in mobile devices, the inductor series resistor, the transistor source resistor, and the transistor current mirror sensing techniques are the most suitable.

Table 3.9: Current sensing techniques comparison for CDA applications

Sensing Technique	On-chip Integration	Accuracy	Power Dissipation	Complexity	Operational Bandwidth
Inductor series resistor [64]	No	H	H	L	H
Current Transformer [95]	No	H	L	L	L
Inductor DCR sensing [96]	No	M	L	H	L
Transistor source resistor [92]	Yes	M	H	L	M
Transistor current mirror [47]	Yes	H	M	M	L

L=Low, M=Medium, H=High

4. A FEED FORWARD POWER SUPPLY NOISE CANCELLATION TECHNIQUE FOR CLASS-D AMPLIFIERS*

4.1 Power-supply noise problem in class-D audio amplifiers

Mobile devices often require the CDA output stage to be connected directly to the battery, providing the maximum amount of available power to the load [8, 9], as expressed in (3.40) of Section 3.3.3. In system-on-chip applications, the digital and radio frequency (RF) circuits often share the same battery as the analog circuits [3, 10]. Consequently, any noise on the battery power-supply plane is mixed together with the audio signal, degrading the amplifier's performance, as depicted in Fig. 4.1.

Open-loop CDA architectures are very sensitive to the power-supply noise since they directly couple the noise to the load each time the output stage switches. Hence, a good power supply rejection ratio (PSRR) is highly desirable for the CDA in battery-powered applications. One proposed solution to improve PSRR is to introduce a voltage regulator between the battery and the class-D amplifier to provide isolation from the power-supply noise [2]. However, this solution might reduce the available voltage delivered to the load, thereby limiting the audio amplifier's maximum output power, which generally degrades the efficiency of the overall audio system due to the additional power dissipation in the voltage regulator.

Closed-loop CDA architectures conventionally enhance the PSRR by means of negative feedback. This feedback mechanism limits the noise coupled from the power-supply rail to the output. The resulting noise attenuation is proportional to the loop gain of the system.

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Thus, a common method to improve the PSRR is to attenuate the supply noise with a high-order compensator's large loop gain [57], as explained in section 3.2 and depicted in Fig. 4.2.

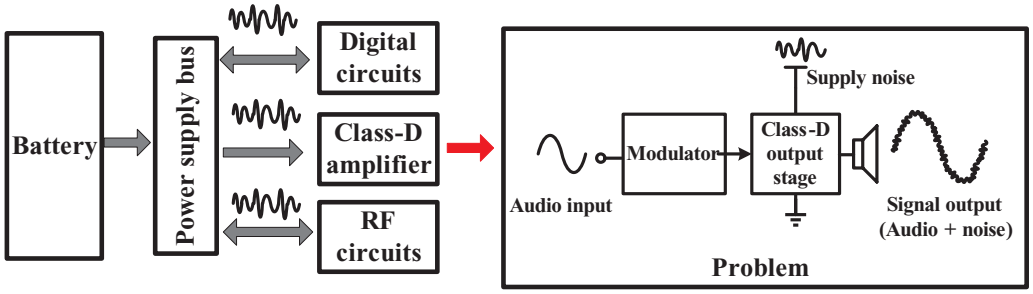


Figure 4.1: Power supply noise problem in class-D amplifiers.

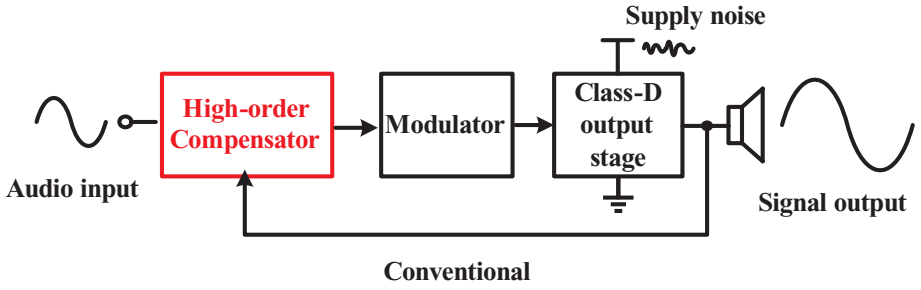


Figure 4.2: Conceptual diagram of conventional solution to reduce power supply noise in class-D amplifiers.

High-order filters have been implemented in the compensator to improve audio performance [9, 42, 61, 62, 65, 97]. However, frequency compensation techniques are required to ensure a stable system, increasing the quiescent power consumption and silicon area.

Similarly, self-oscillating techniques in [63, 64, 65] have been suggested to accomplish higher audio quality, using non-linear compensation techniques. However, the PSRR is still limited by the amount of loop gain and/or mismatch achieved in differential architectures.

Differential architectures with H-bridge output stages could provide good PSRR performance at the expense of larger silicon area and power consumption [9, 42, 61, 62, 65, 97]. In these architectures, matching between the differential paths limits the PSRR [57, 98]. Mismatch values as low as 0.01 % for passive components can be achieved with good layout, trimming, or calibration techniques [99]. However, this comes at the expense of increasing the silicon area and complexity. In [98] a self-adjusting voltage reference scheme was proposed to alleviate the matching requirements in bridge-tied load (BTL) differential architectures to achieve high PSRR. Nevertheless, the PSRR improvement is not constant across the audio bandwidth, limiting its benefits.

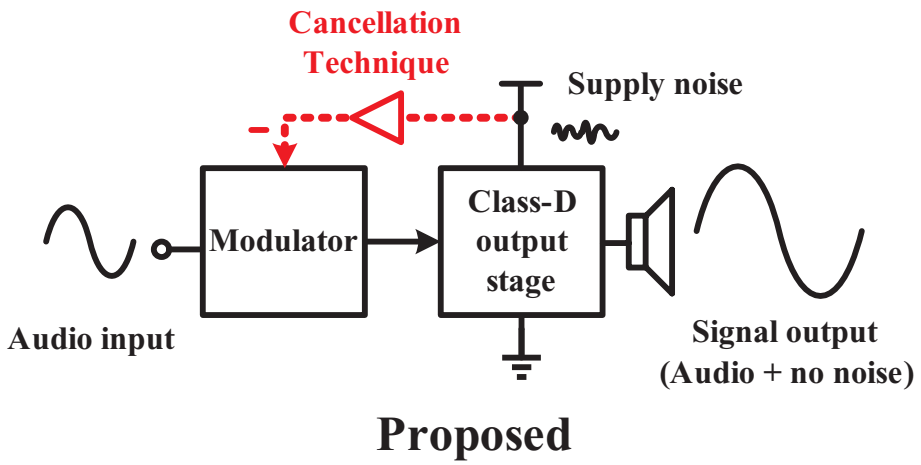


Figure 4.3: Conceptual diagram of proposed solution to reduce power supply noise in class-D amplifiers.

This section presents a design methodology to improve the PSRR in single-ended CDA architectures without increasing the compensation's filter-order. This is accomplished by using a feed-forward power-supply noise cancellation (FFPSNC) technique to suppress the supply-noise present in the system, as observed in Fig. 4.3. The technique improves the PSRR across the entire audio bandwidth independent of the compensation's frequency characteristics. Also, the technique provides single-ended (SE) CDA architectures a PSRR performance comparable to differential architectures. The FFPSNC technique's small quiescent power and silicon area overhead, makes it an attractive alternative to enable high PSRR in the single-ended CDA architecture.

4.2 Power-supply noise modeling in class-D audio amplifiers

A review of the small signal linear model for the CDA is discussed to understand the system limitations. From these models, the power-supply noise transfer function for the CDA system is evaluated. The inputs of the system are assumed AC ground, and the only source of noise comes from the CDA output stage's power-supply. The SE CDA architecture and the differential BTL CDA architecture models are discussed to emphasize their tradeoffs.

4.2.1 Single-ended load

The linear model of the SE CDA architecture is shown in Fig. 4.4; where V_N represents the supply noise in the output power stage, G_C(s) symbolizes the transfer function (TF) of the compensator, G_M(s) denotes the modulator TF, β(s) is the feedback TF, D represents the CDA duty cycle (which in this analysis is considered constant [51]); and F(s) is the output filter TF. The output filter is typically designed with $|F(s)| \cong 1$ across the audio bandwidth.

Therefore, the TF from V_N(s) to V_O(s) for single-ended CDAs can be expressed as,

$$\left.\frac{V_O(s)}{V_N(s)}\right|_{SE} = \frac{D \cdot F(s)}{1 + G_C(s) \cdot G_M(s) \cdot \beta(s)} \cong \frac{D}{LG(s)} \tag{4.1}$$

where $LG(s) = G_C(s) \cdot G_M(s) \cdot \beta(s)$ is the loop gain TF. The ratio in decibels between the power-supply noise and the output signal can be expressed as,

$$PSRR_{SE,dB} = 20 \cdot \log\left(\left|\frac{V_N}{V_O}\right|\right)\Bigg|_{SE} \cong -20 \cdot log(D) + 20 \cdot \log(|LG(s)|). \tag{4.2}$$

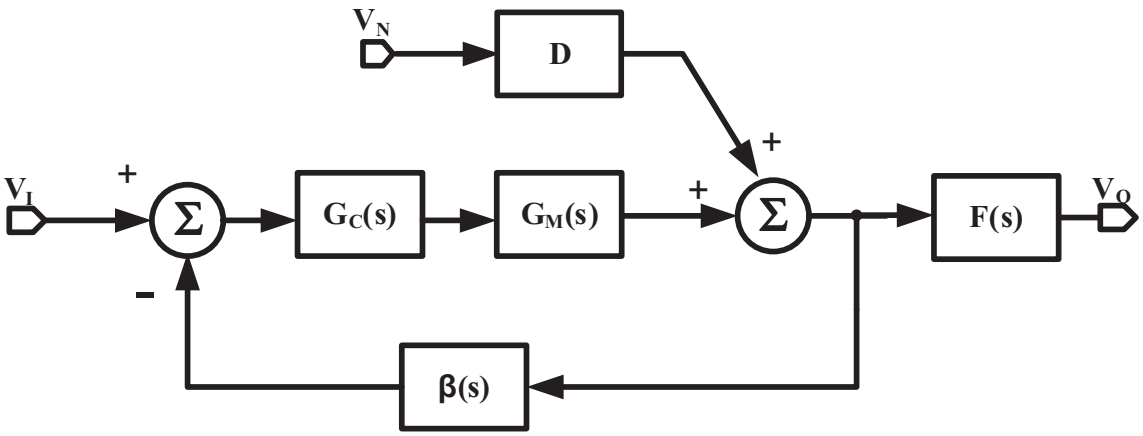


Figure 4.4: Single-ended class-D audio amplifier linear model.

As can be seen in (4.2), large loop gain magnitude is required to have a high PSRR. As discussed in Section 3.2, the loop gain magnitude is typically increased by two methods. First, $G_C(s)$ could be enhanced by increasing the compensation's filter-order. Nonetheless, stability for all the input signal magnitude range is more difficult to achieve in high-order filters, and would require large silicon area and extra quiescent power consumption [9, 42, 61, 62, 65].

Second, $G_M(s)$ could be increased to enhance PSRR. For example, a constant frequency PWM modulator is modeled as a linear constant magnitude, depending only on its input [51]; as expressed by,

$$G_M = \frac{V_{supply}}{V_{TRI}} \tag{4.3}$$

where V_{supply} denotes the modulator's output square wave voltage amplitude and V_{TRI} is the triangular-wave carrier's peak-to-peak voltage amplitude. To increase G_M in a battery-powered device with fixed V_{supply}, V_{TRI} needs to be reduced. This requires a more stringent design on the comparator to detect smaller voltages, and as a result, the PSRR improvement is limited. Other modulation schemes like SO or SDM will have different $G_M(s)$, providing a different gain in the loop.

4.2.2 Bridge-tied load

The linear model for the BTL differential CDA architecture is illustrated in Fig. 4.5. It can be observed that each differential path receives the same noise contribution from the power-supply, assuming ideal matched conditions between the two paths. Therefore, we can express the transfer function for the power-supply noise of the BTL CDA to its differential output $V_O(s) = V_{O,P}(s) - V_{O,N}(s)$ as,

$$\begin{aligned} \left.\frac{V_O(s)}{V_N(s)}\right|_{BTL} &= \frac{D\cdot(LG_2(s)-LG_1(s))\cdot F(s)}{1+LG_1(s)+LG_2(s)+(LG_2(s)\cdot LG_1(s))} \\ &\cong D\left(\frac{LG_2(s)-LG_1(s)}{LG_2(s)\cdot LG_1(s)}\right) \end{aligned} \tag{4.4}$$

where $LG_i(s) = G_{Ci}(s)\cdot G_{Mi}(s)\cdot \beta_i(s)$, for $i = 1,2$.

It can be observed in the numerator of (4.4) that the power-supply noise contribution depends on the difference between $LG_1(s)$ and $LG_2(s)$.

Hence, assuming $LG(s) = LG_2(s) = (1 \pm \delta) \cdot LG_1(s)$ and $0 < \delta < 1$, to take into account the deviation δ between the two differential paths, the transfer function in (4.4) becomes,

$$\begin{aligned} \left.\frac{V_O(s)}{V_N(s)}\right|_{BTL} &\cong D\left(\frac{(1 \pm \delta)LG_1(s) - LG_1(s)}{LG(s) \cdot LG_1(s)}\right) \cong D\left(\frac{|\delta| \cdot LG_1(s)}{LG(s) \cdot LG_1(s)}\right) \\ &\cong D\left(\frac{|\delta|}{LG(s)}\right). \end{aligned} \tag{4.5}$$

The PSRR transfer function in decibels for the BTL CDA yields,

$$PSRR_{BTL,dB} = 20 \cdot \log\left(\left|\frac{V_N}{V_O}\right|\right)\Bigg|_{BTL} \cong -20 \cdot \log(D) + 20 \cdot \log(|LG|) - 20 \cdot \log(|\delta|) \tag{4.6}$$

In the ideal scenario where both paths are perfectly matched, this architecture provides infinite PSRR since the deviation (δ) would be zero.

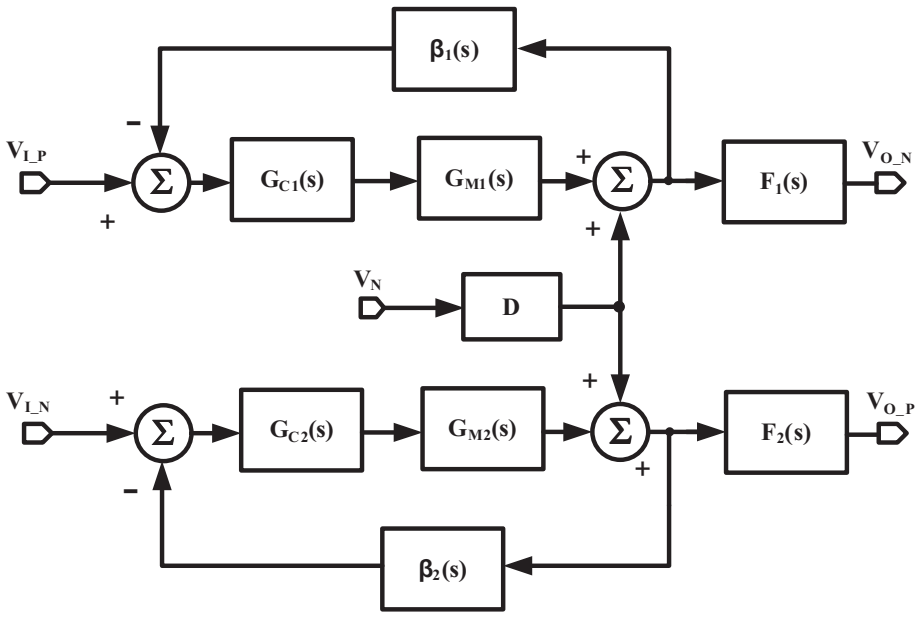


Figure 4.5: Bridge-Tied Load differential CDA linear model.

Nonetheless, mismatch geometries on passive components and active devices, together with amplifier errors (due to amplifier finite loop-gain and bandwidth), will limit the PSRR performance. In other words, the deviation δ is a frequency dependent variable since it needs to match the frequency responses of both differential paths.

For example, a second-order BTL CDA design with a deviation $\delta = 10\%$ between both loops, $|LG(s)| = 70\ dB$ at 217 Hz, and D=0.5 would have a PSRR of 96 dB at low frequencies according to (4.6). The deviation δ is typically the limiting factor for the PSRR in differential CDA architectures, and it typically depends on the matching of two passive feedback networks (e.g. for a first-order compensator shown in Fig. 3.49, the error δ would be limited by the mismatch between two resistors and two capacitors [57]). Also, if the modulator is implemented with a pseudo-differential arrangement of comparators, then the delay, offset, and gain mismatch between comparators will increase the deviation δ in the loop.

4.3 Proposed feed-forward power-supply noise cancellation technique

The proposed FFPSNC technique linear model is illustrated in Fig. 4.6 for the CDA architecture. As can be observed, an additional feed-forward path $G_{FF}(s)$ is introduced in the system to inject the power-supply noise at the input of the modulator block. The feed-forward path's purpose is to replicate the power-supply noise with the correct gain and polarity and inject it into the system to cancel out the supply noise going through the feedback loop before it reaches the modulator block. This is because the modulator block performs a non-linear operation that results in intermodulation and harmonic distortion.

The transfer function from $V_N(s)$ to $V_O(s)$ for the CDA (including the proposed FFPSNC technique) is given by,

$$\left.\frac{V_O(s)}{V_N(s)}\right|_{FFPSNC} = \frac{D\cdot\left(1-G_{FF}(s)\cdot\left(\frac{G_M(s)}{D}\right)\right)\cdot F(s)}{1+G_C(s)\cdot G_M(s)\cdot\beta(s)}. \tag{4.7}$$

It is worth noting that if we remove the $G_{FF}(s)$ path, the transfer function in (4.7) reduces to (4.1). By observing the numerator of (4.7), we can conclude that the power-supply noise present at the output would be completely canceled by selecting $G_{FF}(s) = D/G_M(s)$. This cancellation can be achieved independently of $G_C(s)$. Another alternative to implement the feed-forward path $G_{FF}(s)$ is to apply it before the compensator block $G_C(s)$. However, the required $G_{FF}(s)$ would contain the reciprocal of $G_C(s)$, which is a frequency dependent block, and would require matching more components, making this choice less feasible. The proposed path shown in Fig. 4.6 is the best tradeoff choice between additional hardware overhead and design complexity.

Note that the proposed FFPSNC technique could be applied to BTL architectures but it would require two feedforward paths applied to each differential path, introducing another mismatch element. The PSRR would be limited by the differential path mismatch, the mismatch between the feed-forward cancellation paths, and the $G_{FF}(s)$ implementation mismatch, making the technique not very feasible for BTL implementations.

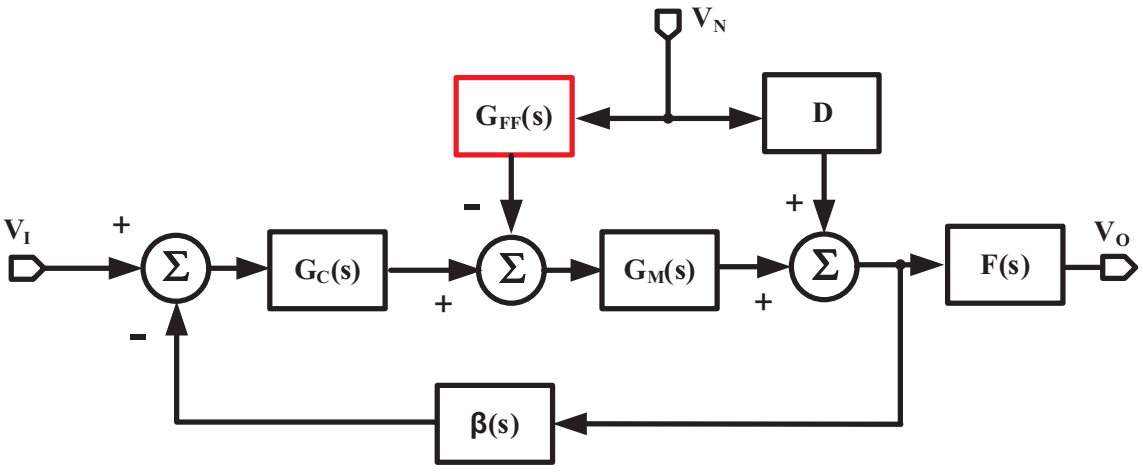


Figure 4.6: Class-D amplifier linear model with proposed FFPSNC technique.

4.3.1 Proposed FFPSNC technique description

The amount of noise cancellation depends on the ability of $G_{FF}(s)$ to precisely replicate $D/G_M(s)$. Thus, any deviation from it will limit the amount of noise cancellation achieved by the technique. Considering the deviation α from the ideal value, which includes variations in D or $G_M(s)$, the actual $G_{FF}(s)$ in (4.7), expressed as $G_{FF}(s) = (1 \pm \alpha) \cdot D/G_M(s)$ with $0 < \alpha < 1$, becomes,

$$\left.\frac{V_O(s)}{V_N(s)}\right|_{FFPSNC} = D \cdot \frac{\left(1 - (1 \pm \alpha) \cdot \left(\frac{D}{G_M(s)}\right) \cdot \left(\frac{G_M(s)}{D}\right)\right)}{1 + LG(s)} \cong D \cdot \frac{|\alpha|}{LG(s)}. \tag{4.8}$$

The PSRR in decibels for the single-ended CDA with the proposed FFPSNC technique can be expressed as,

$$\begin{aligned} PSRR_{FFPSNC,dB} &= 20 \cdot \log\left(\left|\frac{LG(s)}{D \cdot \alpha}\right|\right) \\ &\cong -20 \cdot \log(D) + 20 \cdot \log(|LG|) - 20 \cdot \log(|\alpha|). \end{aligned} \tag{4.9}$$

The PSRR improvement for the proposed technique is $-20 \cdot \log(|\alpha|)$ compared with (4.2). The FFPSNC technique provides the benefit of additional PSRR limited by the amount of mismatch between two paths, as in BTL architectures. However, to minimize the error δ in (4.6), a precise match of two feedback networks must be obtained to achieve high PSRR, and this matching would consume a large silicon area [57, 87]. In the proposed FFPSNC technique, the deviation α will depend on the implementation of $G_{FF}(s)$.

The key parameter for the implementation of $G_{FF}(s)$ is a good extraction of the linear gain $G_M(s)$ since it varies across different modulations schemes. However, the modulation process is a non-linear operation that depends on its input amplitude, and it requires a quasi-linearization to be able to extract the equivalent gain $G_M(s)$. To accomplish this, the describing function (DF) methodology is used since it provides an approximate proce-

dure for analyzing certain non-linear blocks in control systems such as the modulation of switching circuits [68, 100]. A general representation for the DF as a complex gain for a sinusoidal input of amplitude V_i and frequency ω can be expressed as,

$$\begin{aligned} G_M(V_i,\omega) &= G_p(V_i,\omega) + jG_q(V_i,\omega) \\ &= M_G(V_i,\omega)e^{j\phi_G(V_i,\omega)} \end{aligned} \tag{4.10}$$

where the terms $G_p(V_i,\omega)$ and $G_q(V_i,\omega)$ are the in-phase and quadrature gains of the non-linearity. The magnitude and phase representation can be expressed as,

$$\begin{aligned} M_G(V_i,\omega) &= \sqrt{G_p^2(V_i,\omega) + G_q^2(V_i,\omega)}, \\ \phi_G(V_i,\omega) &= \tan^{-1}\left(\frac{G_q(V_i,\omega)}{G_p(V_i,\omega)}\right). \end{aligned} \tag{4.11}$$

The modulation schemes used in the CDA are typically implemented with a relay, relay with hysteresis, or odd quantizer non-linearities. For the PWM, the modulation is implemented with a comparator with sharp transition that can be approximated to a relay non-linearity [68] with a DF given by,

$$G_M(V_i,\omega)_{PWM} = \frac{V_{DD}}{V_i} \cong \frac{V_{DD}}{V_{TRI}} \tag{4.12}$$

where V_{DD} is the supply of the comparator and V_{TRI} is the peak amplitude of the triangular carrier waveform. For the close loop PWM CDA architecture, the loop forces the input of the comparator to be within the carrier peak amplitude. Thus, the quasi-linearized gain in (4.12) using V_{TRI} as the peak amplitude at the input of PWM modulator corresponds to the expression in (4.3), verifying the analysis.

Also, it is worth noticing that (4.12) is frequency independent, which allows a simpler $G_{FF}(s)$ implementation expressed as,

$$G_{FF}(s)_{PWM} = \frac{D}{G_{M,PWM}} \cong \frac{D \cdot V_{TRI}}{V_{DD}}. \tag{4.13}$$

For the SDM, the modulation is implemented with a quantizer that can be approximated to an uniform quantizer non-linearity with a DF given by,

$$G_M(V_i, \omega)_{SDM} = \frac{V_{DD}}{V_i} \sum_{m=1}^{n} \sqrt{1 - \left(\frac{2m-1}{2}\frac{q}{V_i}\right)^2} \tag{4.14}$$

where q is the quantization step as expressed in (3.11), and n is the number of quantization output levels in the quantizer. It can be observed that as n increases, the G_M approaches a linear gain. This is expected since a multilevel quantizer provide less quantization error and a more linear operation as expressed in (3.12), at the expense of increased power consumption as discussed in Section 3.2.2.

The gain in (4.14) is frequency independent and will approach unity for $V_i \gg q$, assuming $V_i = V_{DD}$ for full dynamic range. However, since the quantizer in a SDM architecture is typically preceded by a sample and hold circuit, the modulator gain $G_{M,SDM}(s)$ contains the delay introduced by this block.

The sample and hold operation can be approximated to a zero-order hold (ZOH) model with transfer function expressed as,

$$G_{ZOH}(s) = \frac{1 - e^{-sT_{SW}}}{sT_{SW}} \tag{4.15}$$

where $T_{SW} = 1/F_{SW}$.

The implementation of $G_{FF}(s)$ for SDM needs to consider both gains and it would be given by,

$$G_{FF}(s)_{SDM} = \frac{D}{G_{M,SDM}} \left(\frac{1}{G_{ZOH}(s)} \right). \tag{4.16}$$

To evaluate the effect of the ZOH, a bode plot for the ZOH with two different sampling frequencies is shown in Fig. 4.7. It can be observed that if the sampling frequency F_{SW} is much higher than the desired signal bandwidth, the magnitude of (4.15) is almost unity. However, the phase shift is dramatically different for a $F_{SW} = 200\ kHz$ with a phase shift of -20° at 20 kHz bandwidth, while for a $F_{SW} = 2\ MHz$, the phase shift is -1.8°. Thus, for $F_{SW} > 2\ MHz$ the ZOH transfer function can be obviated.

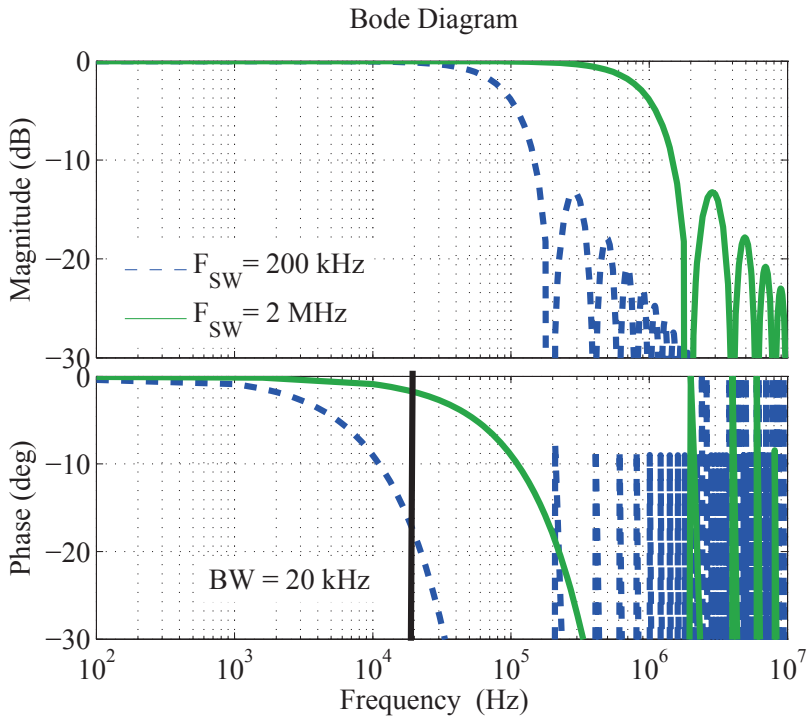


Figure 4.7: Magnitude and phase frequency response of zero-order hold.

For the SOM, the modulation is implemented with a hysteretic comparator that can be approximated to a relay with hysteresis non-linearity with a DF defined in (3.19). Its modulator gain, magnitude, and phase can be expressed as [68],

$$\begin{aligned} G_M(V_i,\omega)_{SOM} &= \frac{V_{DD}}{V_h} e^{j\tan^{-1}\left(\frac{V_h/V_i}{\sqrt{1-(V_h/V_i)}}\right)}, \\ M_G(V_i,\omega)_{SOM} &= \frac{V_{DD}}{V_h}, \\ \phi_G(V_i,\omega)_{SOM} &= \tan^{-1}\left(\frac{V_h/V_i}{\sqrt{1-(V_h/V_i)}}\right) \cong \sin^{-1}\left(\frac{V_h}{V_i}\right) \end{aligned} \tag{4.17}$$

where V_h is the hysteresis window. As in the PWM case, the close loop will force the input signal of the hysteretic comparator to be within the hysteresis window. Thus, the $M_G(V_i,\omega)_{SOM}$ is constant and frequency independent, but its phase response is a function of the input amplitude and the hysteresis window, as discussed in Section 3.2.3.

Contrary to the PWM or SDM, the SOM is highly dependent on the modulator input voltage and would present a input-dependent delay. Thus, the $G_{FF}(s)$ implementation has to replicate the reciprocal of this phase variation, and it can be expressed as,

$$G_{FF,SOM}(s) = \frac{D}{G_{M.SOM}(s)} \cong \frac{D \cdot V_h}{V_{DD} \cdot \left(\sqrt{1-\left(\frac{V_h}{V_i}\right)^2} + \frac{V_h}{V_i}s\right)}. \tag{4.18}$$

4.3.2 Class-D with FFPSNC technique circuit implementation

From all the discussed modulation schemes, the PWM provides the simpler implementation for $G_{FF}(s)$. Thus, to demonstrate the effectiveness of the proposed scheme, a first-order SE PWM CDA with the FFPSNC technique is implemented.

Fig. 4.8 shows the schematic circuit of the implemented CDA with the proposed technique. The design for each block is addressed next.

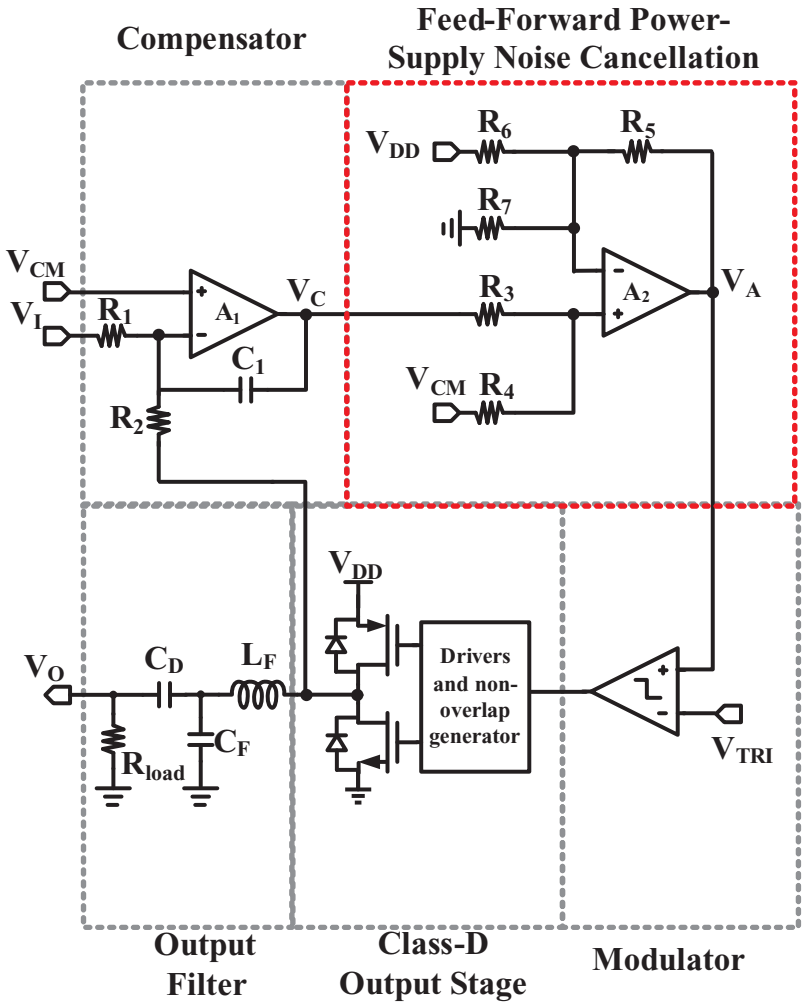


Figure 4.8: Proposed CDA implementation with FFPSNC technique.

The compensator was implemented as a first-order continuous-time integrator with crossover frequency $f_{int} = 1/(2\pi \cdot R_1 \cdot C_1)$. Its value selection depends on several tradeoffs between the passive's area, amplifier's power, linearity, and noise, as discussed in Section

3.3.1. To avoid significant deviations in the compensator's performance, the amplifier's gain-bandwidth product (GBW) has to be higher than f_{int}, as expressed by,

$$G_{int,actual}(s) = -\frac{G_{int,ideal}(s)}{1+\frac{1}{A_1(s)\cdot\beta_C(s)}} \cong -\frac{\left(\frac{1}{s\cdot R_1\cdot C_1}\right)}{1+\frac{s}{GBW}\cdot\left(\frac{s\cdot R_{1,2}\cdot C_1+1}{s\cdot R_{1,2}\cdot C_1}\right)} \tag{4.19}$$

where $R_{1,2} = R_1//R_2$, the amplifier's transfer function is characterized as $A_1(s) \cong GBW/s$, and $\beta_C(s)$ is the integration's amplifier feedback transfer function.

As discussed in Section 3.2, a large value for f_{int} would provide a higher bandwidth for the CDA loop. A large bandwidth would result in high linearity, high PSRR at higher frequencies, and smaller passive component values. However, the high frequency amplifier's noise would also be amplified, and the amplifier's power would need to be increased to avoid deviations in f_{int} due the finite GBW [84]. The $f_{int} = 15.5\ kHz$ was chosen as a compromise between these tradeoffs.

The integrator component values are $C_1 = 32\ pF$ and $R_1 = R_2 = 320\ k\Omega$. The input resistor values were chosen considering the tradeoff between the resistor's thermal noise contribution and its matching requirements. The amplifier A_1 is implemented as a two-stage Miller-compensated amplifier where the input transistors were designed with lengths of 2 μm to minimize their flicker noise contribution in the audio bandwidth.

The amplifier's slew rate (SR) imposes a limitation in the large signal operation of the compensator. A two-stage miller-compensated amplifier topology was chosen with $GBW = \frac{gm_{1,2}}{2\pi\cdot C_c}$ [79, 84, 83], where the SR in unity gain configuration is expressed as,

$$SR \cong \frac{I_{tail}}{C_C} = \frac{I_{tail}\cdot 2\pi\cdot GBW}{gm_{1,2}} = 2\pi\cdot GBW\cdot V_{dsat_{1,2}}. \tag{4.20}$$

The full-power bandwidth is defined as the maximum frequency (f_{max}) at which the

amplifier will yield an undistorted AC output with the largest possible amplitude (V_{max}) [83]. The minimum SR requirement for amplifier A_1 using this definition is,

$$SR_{min} \geq 2\pi \cdot f_{max} \cdot V_{max}. \tag{4.21}$$

The compensation's A_1 amplifier has to process the input audio signal and the high frequency feedback signal. Therefore, the f_{max} would correspond to the feedback's switching frequency, and V_{max} to the peak voltage of the feedback signal in the system. To specify a minimum GBW requirement, the small signal behavior in (4.20) could be related to the large signal by using (4.21) and solving for GBW [84]. The minimum GBW needed in the A_1 amplifier to avoid being GBW limited can be expressed as,

$$GBW_{min} \geq \frac{f_{max} \cdot V_{max}}{V_{dsat_{1,2}}}. \tag{4.22}$$

Several design alternatives are possible taking into account the tradeoffs present in (4.22). Also, the $V_{dsat_{1,2}}$ design choice presents tradeoffs in the amplifier A_1 between its DC gain, offset voltage, noise, bandwidth, and stability [79, 83]. The implemented design uses the A_1 amplifier's $V_{dsat_{1,2}} = 100\ mV$ for a $f_{max} = 500\ kHz$ with $V_{max} = 1.8\ V$, which would require a minimum GBW of 9 MHz. Since the GBW parameter is chosen to satisfy (4.22), the A_1 amplifier's DC open-loop gain parameter is selected taking into the account the tradeoffs between the integrator performance and the amplifier's power and area consumption. The implemented amplifier A_1 achieves a DC open-loop gain of 76 dB with a phase margin of 61°, and GBW of 10 MHz. The amplifier consumes a quiescent current of 28 μA from a 1.8 V supply.

Pulse width modulation (PWM) was chosen for this implementation since its quasi-linear modulation gain, $G_M(s)$, can be approximated as a constant in the audio bandwidth if the modulation frequency is constant and at least two times higher than the audio bandwidth [51]. The G_M magnitude represents the linear gain of the combination of the modulator and output power stage. Note that the modulator's noise contribution from the supply is already represented as the noise signal at the output of the linear model.

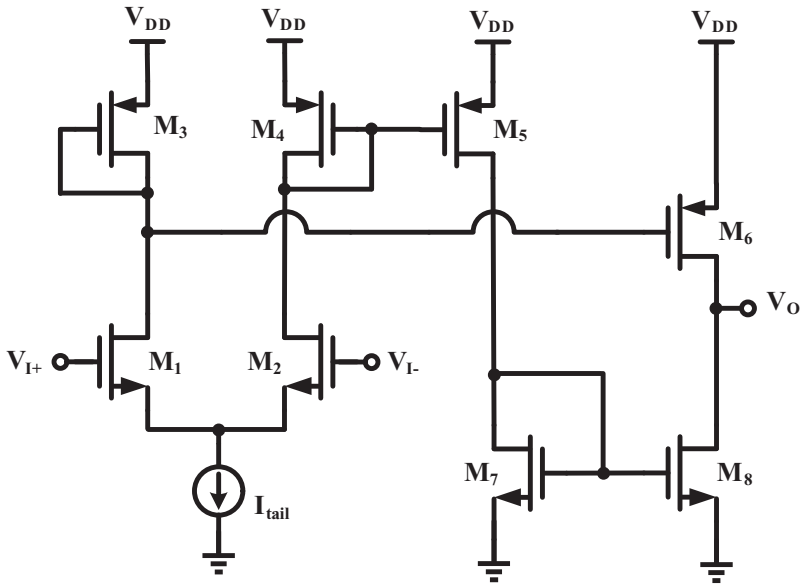


Figure 4.9: PWM comparator schematic diagram.

The PWM modulator was implemented using an open-loop comparator with large open-loop gain as show in Fig. 4.9 [79]. The comparator was designed as a push-pull amplifier, as discussed in Section 3.3.2, to achieve high slew rate to minimize propagation delay, and its high PSRR suppress the supply noise contribution at its output.

The main advantage of this implementation is that all the internal nodes appear as high impedance, minimizing the signal propagation delay from input to output.

Thus, all the transistors are sized with small widths and lengths. The output transistors M_6 and M_8 can provide almost rail-to-rail output voltage, and are sized such that they can charge and discharge the output node very fast. The comparator consumes 20 μA of quiescent current from a 1.8 V supply. An external 500 kHz triangle-wave carrier signal with peak-to-peak amplitude of 0.9 V was used to have a modulator gain $G_M \approx 2$. This is to have external control on the amplitude of the triangular waveform for manual calibration of G_M.

The output power stage was designed to minimize dynamic power dissipation without degrading the propagation delay [60], as discussed in Section 3.3.3. A typical implementation is shown in Fig. 4.10, where a non-overlapping signal generator is used to avoid excessive short-circuit current through the class-D output stage. The non-overlap delay (t_{ov}) is chosen as a tradeoff between efficiency and distortion [85]. Nevertheless, due to the large gate capacitance of the output stage transistors, a driver stage implemented as a tapered buffer is used to charge and discharge these large gate capacitances with minimum power-delay product [86].

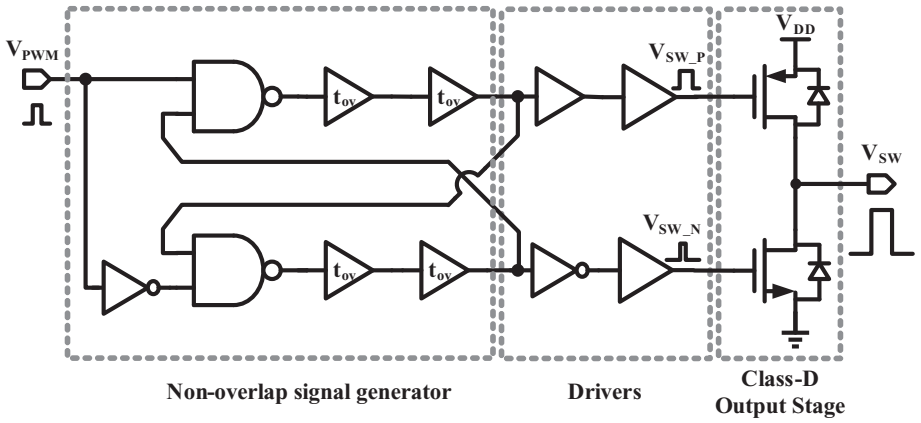


Figure 4.10: Single-ended class-D output stage.

For demonstration of the FFPSNC technique, nominal 1.8 V devices were used to implement the output stage. Nonetheless, higher output power capabilities could be expanded using high voltage devices such as thick oxide,LDMOS, or DMOS transistors depending on the desired application [8, 62].

The class-D output stage as shown in Fig. 4.10 is commonly known as a single-ended or half-bridge output stage. Its output transistors need to be carefully sized to avoid the dynamic or conduction losses to dominate the overall efficiency performance. Fig. 4.11 illustrates the design tradeoffs when choosing the width for the NMOS and PMOS transistors for a minimum length of 180 nm. For example, for a typical EM speaker with an 8 Ω impedance, a $R_{dsON} = 0.2\ \Omega$ will limit the efficiency to 97 % at high output power. Thus, from Fig. 4.11, the PMOS need to have a width of 12 mm, and the NMOS need a width of 3 mm. This will result in gate capacitance for the PMOS of 16 pF, and 4 pF for the NMOS.

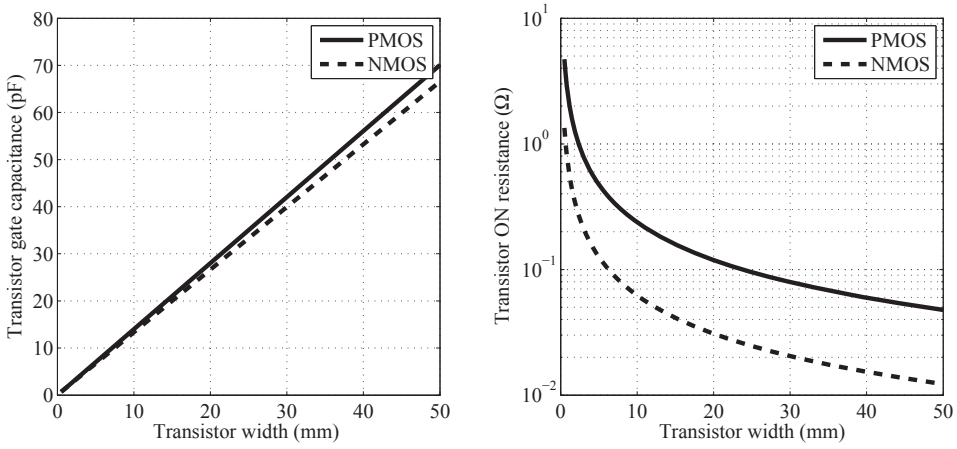


Figure 4.11: Transistor total gate capacitance and R_{dsON} versus transistor width for output stage sizing.

The main function for the output filter is to recover the low frequency audio signal from the modulated output. An off-chip second-order low-pass filter is typically used. Since the output current flows through the output filter components, an inductor and capacitor are typically used to avoid extra power dissipation. Also, the EM speaker must not have a DC component to avoid damaging the transducer. Thus, the single supply configuration must have a large decoupling capacitor to remove the DC component. The transfer function for the LC filter with single supply and decoupling capacitor shown in Fig. 4.8 can be expressed as,

$$\begin{aligned} \frac{V_O(s)}{V_{SW}(s)}_{Single} &= \frac{\omega_{LC}^2}{s^2+\omega_{LC}^2}\left(\frac{s}{s+\omega_z}\right) \\ &= \frac{1/(L_F C_F)}{s^2+1/(L_F C_F)}\left(\frac{s}{s+1/(C_D R_{load})}\right) \end{aligned} \tag{4.23}$$

where the cutoff frequency of the filter is given by $L_F C_F$ and the decoupling capacitor C_D creates a high pass filter characteristic with the load. The filter was designed with a low-pass cutoff frequency of 22.5 kHz. The filter components were implemented as $L_F = 50\ \mu H$, $C_F = 1\ \mu F$, and $R_{load} = 8\ \Omega$. A blocking capacitor $C_D = 10\ \mu F$ was selected to remove the DC component applied to the speaker.

For the implemented PWM scheme, $G_{FF}(s)$ is assumed constant since the average magnitude of D and G_M, with no input signal, is assumed constant [51]. Then, G_{FF} is implemented based on a resistor's ratio. To minimize silicon area and quiescent power consumption, the FFPSNC technique was implemented using an additional amplifier A_2 in a balanced adder configuration as shown in Fig. 4.8. Assuming A_2 is an ideal amplifier and that the supply noise voltage V_N comes from V_{DD}, the output of the amplifier can be expressed as,

$$
\begin{aligned}
V_A &= V_C \cdot \left[\left(\frac{R_4}{R_4 + R_3} \right) \cdot \left(1 + \frac{R_5}{R_6 // R_7} \right) \right] - V_N \cdot \left(\frac{R_5}{R_6} \right). \\
&= \frac{V_C}{1 + \dfrac{R_3}{R_4}} \left(1 + \frac{R_5}{R_7} + \frac{R_5}{R_6} \right) - V_N \cdot \left(\frac{R_5}{R_6} \right).
\end{aligned}
\tag{4.24}
$$

This arrangement allows the use of only one amplifier to provide two functions: 1) provide a feed-forward path to add V_N to the system, and 2) scale V_N with the proper gain and polarity. Resistor ratio R_5/R_6 implements G_{FF}, and their values were chosen for an average $D = 0.5$ such that $G_{FF} = D/G_M = 0.5/2 = 0.25$. The values of resistors $R_3 - R_4$ were chosen to provide a unity gain path from V_C to V_A, to avoid altering the feedback loop characteristics. Resistor R_7 value was chosen equal to R_6 to set the DC value of the negative input of A_2, at the system's common-mode voltage of 0.9 V.

As will be detailed in the Section 4.4, for the proposed implementation, the deviation α in (4.9) can be minimized without a large silicon area requirement. Also, since the PWM has a $G_M(s)$ constant across the audio bandwidth, then the FFPSNC technique would be effective across the entire audio bandwidth.

4.4 Proposed technique tradeoffs and methodology

The proposed FFPSNC implementation for $G_{FF,i} = -(R_5/R_6)$ in (4.24) presents important design choices and tradeoffs. To evaluate the effects of mismatch in the implementation of R_5/R_6 resistors and the gain error due to finite loop gain in the amplifier A_2, the deviation α in (4.9) can be broken down in two error components.

First, the resistor mismatch in R_5/R_6 is expressed as $(R_5/R_6) \cdot (1 \pm \alpha_1)$, for $0 < \alpha_1 < 1$. Second, the amplifier's A_2 DC gain error due to finite loop gain is expressed as $\varepsilon = 1/(A_2(s) \cdot \beta_{FF})$, for $(A_2(s) \cdot \beta_{FF}) \gg 1$, where $A_2(s)$ is the amplifier's open-loop gain and β_{FF} is the feedback gain [84].

The gain error ε in A_2 is further divided since the feedback gain is expressed as,

$$\beta_{FF} = \frac{R_6//R_7}{R_5 + (R_6//R_7)}, \tag{4.25}$$

that also contains the mismatch component α_1 between R_5/R_6. Considering both error components, the implemented feed-forward gain $G_{FF,a}$ is,

$$G_{FF,a}(s) = \frac{G_{FF,i}(s)}{1 + \frac{1}{A_2(s)\cdot\beta_{FF}}} \cong \frac{-\left(\frac{R_5}{R_6}\right)\left(1 \pm \alpha_1\right)}{1 + \frac{1}{A_2(s)}\left[1 + \left(\frac{R_5}{R_6}\right)\left(1 \pm \alpha_1\right)\left(1 + \frac{R_6}{R_7}\right)\right]}. \tag{4.26}$$

Assuming $|A_2(s)\cdot\beta_{FF}| \gg 1$ and $A_2(s) \cong A_{o,2}$ over the audio bandwidth, the expression in (4.26) can be approximated as,

$$G_{FF,a}(s) \cong G_{FF,i}\left(1 - \frac{1}{A_2(s)\cdot\beta_{FF}}\right)$$

$$\cong -\left(\frac{R_5}{R_6}\right)\left(1 \pm \alpha_1\right)\left(1 - \frac{1}{A_{o,2}}\left[1 + \left(\frac{R_5}{R_6}\right)\left(1 \pm \alpha_1\right)\left(1 + \frac{R_6}{R_7}\right)\right]\right) \tag{4.27}$$

$$\cong G_{FF,i}(1 \pm \alpha_1) - G_{FF,i}\left(\frac{1 \pm \alpha_1}{A_{o,2}}\right) + (G_{FF,i})^2\frac{(1 \pm \alpha_1)^2}{A_{o,2}}\left(1 + \frac{R_6}{R_7}\right).$$

From (4.27), it can be observed that there are multiple solutions for the two variable equation which is in the generic form $G_{FF,a} = k_1 + k_2\ x + k_3\ y + k_4\ xy + k_5\ x^2y$, where $x = \alpha_1$ and $y = 1/A_{o,2}$. Therefore, the amount of PSRR improvement achieved by the proposed FFPSNC implementation is,

$$PSRR_{dB,imp} = -20\cdot\log(|\alpha|) = -20\cdot\log\left(\left|\frac{G_{FF,a} - G_{FF,i}}{G_{FF,i}}\right|\right). \tag{4.28}$$

4.4.1 FFPSNC technique implementation tradeoffs

To illustrate the design tradeoffs for the proposed implementation on the PSRR improvement, multiple solutions of (4.28) were drawn in a 3D plot shown in Fig. 4.12, where the two variables ($x = \alpha_1, y = 1/A_{o,2}$) were swept over a wide range of values. The contour plot is shown in Fig. 4.13, which illustrates clearly the design tradeoffs in the proposed FFPSNC implementation.

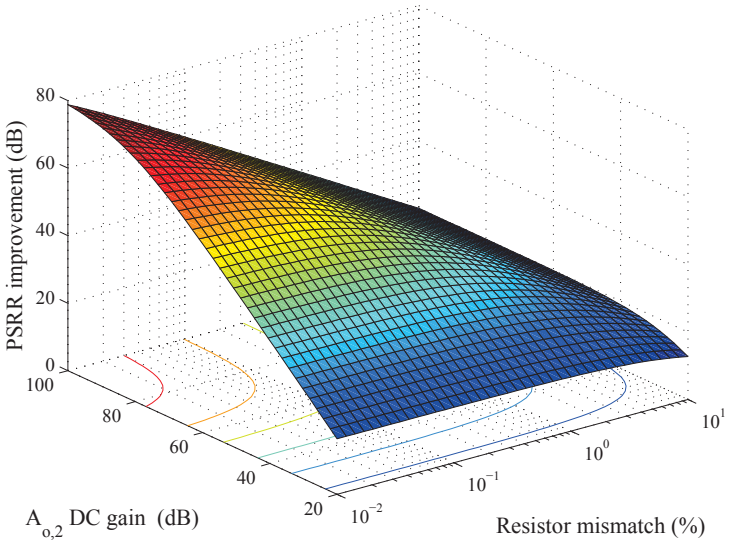


Figure 4.12: 3D-surface plot of design tradeoffs for G_{FF} implementation.

It can be observed from Fig. 4.13, that the resistor mismatch (α_1) is the dominant error parameter in (4.27) when the DC open-loop gain $A_{o,2}$ is higher than 60 dB. On the other hand, if the resistor mismatch is less than 0.02%, then $A_{o,2}$ needs to be higher than 80 dB or it will become the limiting factor in the PSRR improvement. It can be noted that the α_1 error in (4.27) depends only on the mismatch between resistors R_5/R_6.

This mismatch can be minimized using less silicon area overhead compared to the area needed to minimize the error δ in the BTL CDA architecture as discussed in Section 4.2.2.

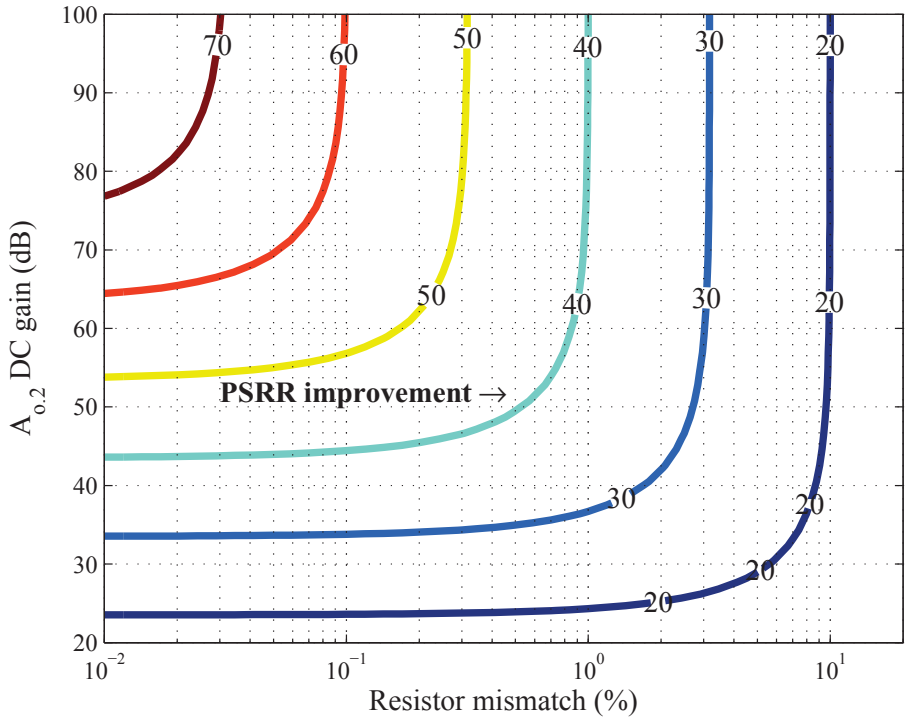


Figure 4.13: Contour plot of design tradeoffs for G_{FF} implementation.

Another possibility to reduce the mismatch in the implementation of G_{FF} is to use dynamic element matching techniques in the resistors by choosing different but almost equal-valued resistors to represent a more accurate value as a function of time [79, 101]. The goal is to transform the accuracy error due to the resistor's mismatch from a DC offset into an AC signal of equivalent power that can be removed by the noise shaping action of the compensator in the close loop system. However, this increases the complexity, area, and power consumption [101].

To illustrate the proposed design methodology, the FFPSNC technique was implemented with $A_{o,2} = 54\ dB$, and the resistors were implemented with a expected mismatch of less than 2% to obtain a PSRR improvement around 34 dB, according to (4.28) and Fig. 4.13. Amplifier A_2 is implemented as a two-stage miller-compensated amplifier with DC gain of 54 dB, phase margin of 72°, and GBW of 10 MHz. It consumes a quiescent current of 27.5 μA.

4.4.2 FFPSNC technique design procedure

Using the contours in Fig. 4.13, we can determine both, the minimum amount of resistor mismatch α_1 and the minimum $A_{o,2}$ gain needed for a desired value of PSRR improvement for different applications. The proposed FFPSNC technique implementation is illustrated in Fig. 4.14.

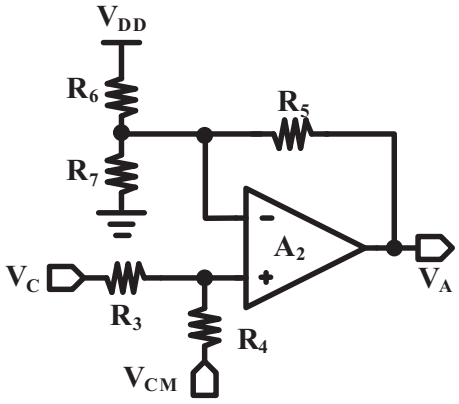


Figure 4.14: Proposed FFPSNC technique implementation.

A comprehensive design procedure for the implementation of G_{FF} for PWM is summarized in Table 4.1. For this example, for a $G_M = 2$ and D=0.5, a $G_{FF} = 1/4$ will be needed. If we desire a 40 dB PSRR improvement, we can tolerate a minimum resistor mismatch of 1% with the $A_{o,2}$ gain of 70 dB. On the other hand, if the design application

only needs an extra 20 dB of PSRR improvement, then we could tolerate up to 10% of resistor mismatch with an A_2 open-loop gain of 50 dB. For this example, a 30 dB PSRR improvement will be target, requiring $A_{o,2} = 50dB$ and $\alpha_1 = 2\%$. Then, after designing the amplifier, we can look that the CMOS 0.18 μm technology requires a minimum resistor width of 1 μm for an $\alpha_1 \cong 2\%$.

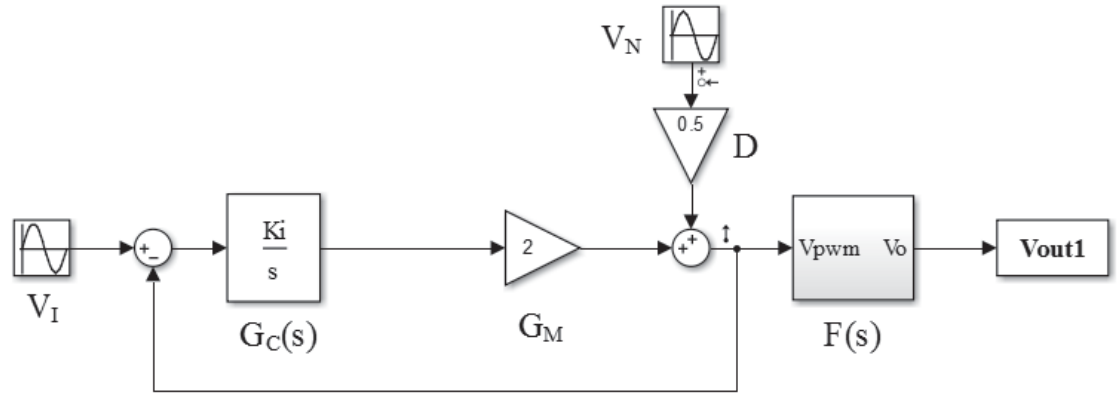
The next step is to choose the resistor values. R_5 is chosen as 50 kΩ to avoid loading the amplifier output. R_6 is chosen as 200 kΩ to implement the desired $G_{FF} = 1/4$. Then, for a $V_{CM} = V_{DD}/2$, $R_7 = R_6 = 200k\Omega$. The final steps are choosing $R_3 = R_5 = 50k\Omega$ and $R_4 = R_7//R_6 = 100k\Omega$ to achieve a unity gain for the controller output containing the audio signal, and to have a fully balanced amplifier less sensitive to common mode noise. All resistors were implemented using P+ poly material over N-well with a width of 2 μm.

Table 4.1: Proposed FFPSNC technique design procedure for SE PWM architectures.

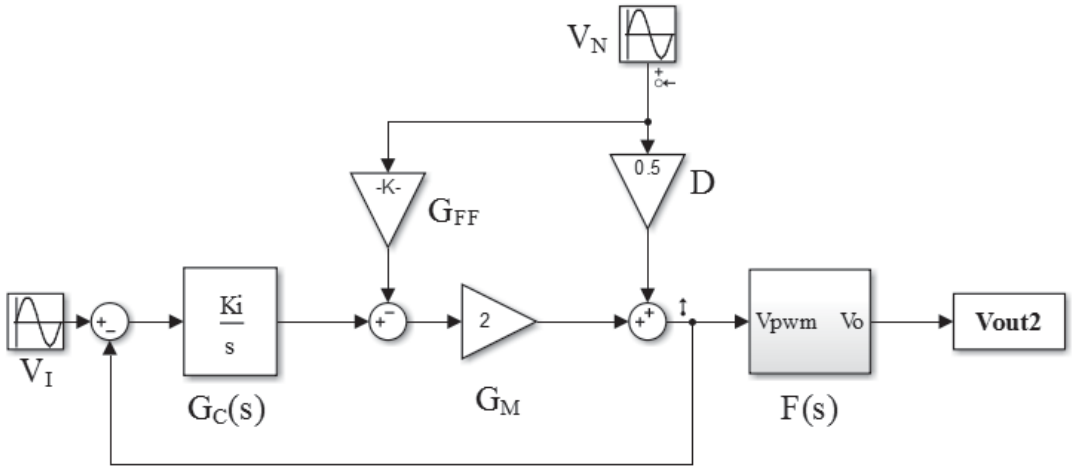
Design procedure based on Fig. 4.13 and Fig. 4.14
1. Determine $G_{FF} = D/G_M$.
2. Select desired PSRR improvement contour line.
3. Find minimum $A_{o,2}$ and resistor mismatch α_1.
4. Design amplifier A_2 for desired DC gain $A_{o,2}$.
5. Choose resistor width from technology data for minimum α_1.
6. Choose R_5 much larger than R_{out} of amplifier A_2 to avoid limiting the DC gain.
7. Choose $R_6 = R_5/G_{FF}$ to implement desired FF gain.
8. Choose $R_7 = R_6 \cdot (V_{DD} - V_{CM})/V_{CM}$ for desired V_{CM}.
9. Choose $R_3 = R_5$ for unity gain for audio signal
10. Choose $R_4 = R_6//R_7$ for fully balanced amplifier.

4.5 Simulation results of proposed FFPSNC technique

To verify the versatility of the proposed technique in single-ended architectures, a first-order and a second-order PWM CDA systems were designed with and without the proposed FFPSNC technique for comparison; the MATLAB © Simulink simulation models are illustrated in Fig. 4.15 for the first order compensator and in Fig. 4.16 for the second order compensator.



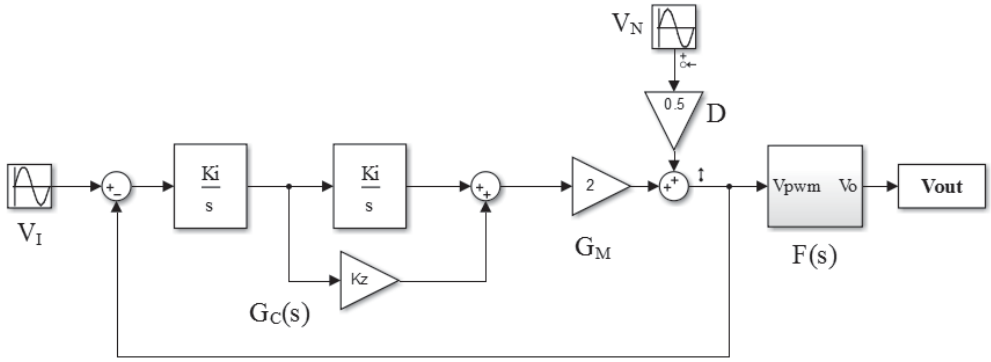
1st Order PWM CDA without FFPSNC technique



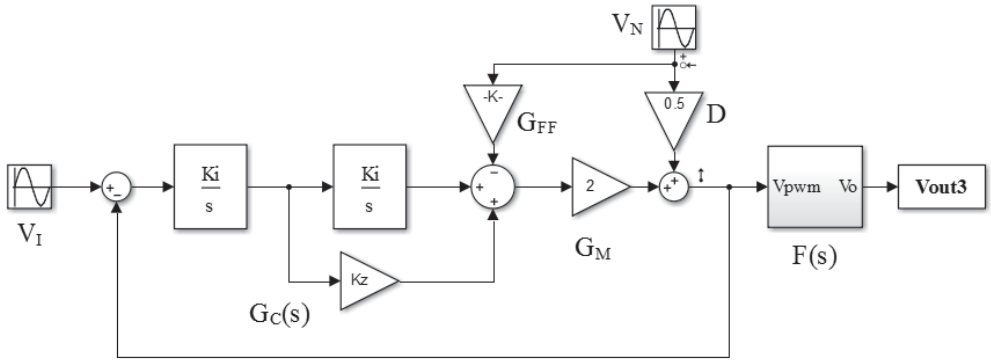
1st Order PWM CDA with FFPSNC technique

Figure 4.15: Simulink models for 1st order PWM CDA for supply noise.

It can be observed that the PWM modulator plus the class-D output stage are linearized and represented by a single gain element. Also, the G_{FF} gain is implemented by a gain element with a value equal to the desired gain plus some error.



2nd Order PWM CDA without FFPSNC technique



2nd Order PWM CDA with FFPSNC technique

Figure 4.16: Simulink models for 2nd order PWM CDA for supply noise.

The ideal models demonstrate the basic principle behind the FFPSNC technique and can be used to simulate the supply-noise rejection using a linear analysis. However, in the real implementation the system could present some inaccuracies in the cancellation path since is always switching.

To verify that the proposed FFPSNC technique is still valid on the transistor level design, the first order and second order PWM loops were implemented with and without the FFPSNC technique. Both circuit designs were simulated using the periodic-state analysis together with the periodic stability analysis; the simulation results are shown in Fig. 4.17. A 2% mismatch was introduced in the FFPSNC implementation, and both first and second order systems achieved around 34 dB of PSRR enhancement. The FFPSNC technique could be applied to a high-order loop to increase its PSRR if it is required by the application. The additional PSRR is independent of the order of the compensator since it only depends on the accuracy of the implementation of G_{FF}.

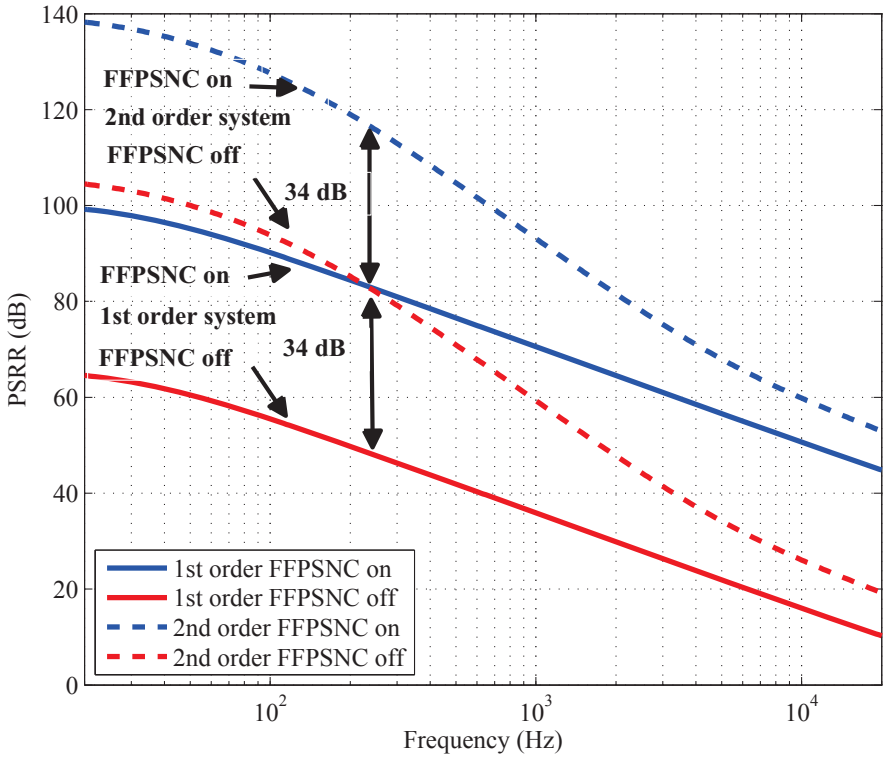


Figure 4.17: PSRR simulation results comparison for transistor level designs.

The added cost of the second order loop is an extra integrator and the required compensation for stability of the loop. The only cost of the FFPSNC is an extra amplifier and the G_{FF} implementation, but no extra compensation is required. Moreover, the first order system with FFPSNC technique provides a better PSRR at high frequencies compared with the second order system without the proposed technique.

To verify the robustness of the proposed FFPSNC technique implementation, a Montecarlo simulation with 200 runs for the PSRR improvement is shown in Fig. 4.18. It can be observed that the mean value for the PSRR improvement is 33.21 dB, while the standard deviation is only 2.29 dB. This is mainly limited by the resistor mismatch in the proposed implementation which is around 2%. This mismatch can be reduced by occupying more silicon area; for example, for this particular 180nm technology using P+ polysilicon resistors, to obtain a PSRR improvement of 50 dB a mismatch of 0.1 % would be needed, increasing the silicon area occupied by 220%.

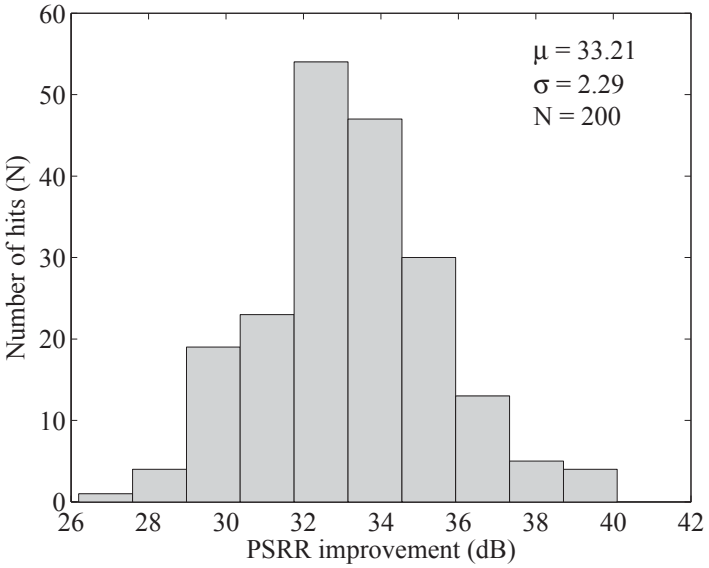


Figure 4.18: PSRR improvement Montecarlo simulation results.

4.6 Experimental results of CDA with FFPSNC technique

A first-order PWM CDA with the proposed FFPSNC technique was fabricated in 0.18 μm CMOS standard technology, as discussed in Section 4.3.3, and tested with a System One Dual-Domain Audio Precision instrument using a 1.8 V supply voltage. The chip was encapsulated in a QFN-24 package. Fig. 4.19 shows the die micrograph of the fabricated CDA, where blocks I, II, III and IV correspond to the compensator, FFPSNC technique, comparator, and output power stage, respectively. The total active area occupied by the class-D amplifier with the proposed FFPSNC technique is 0.121 mm^2.

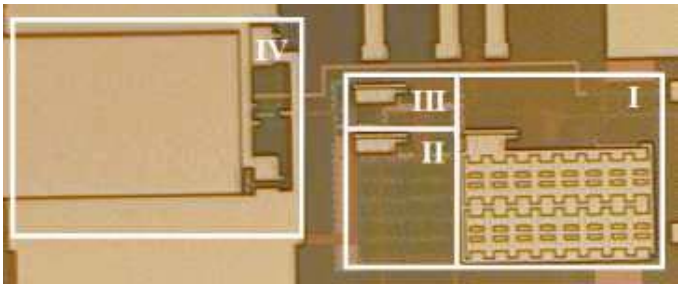


Figure 4.19: Class-D audio amplifier die micrograph, I compensator (0.044 mm^2), II FF-PSNC technique (0.019 mm^2), III comparator (0.003 mm^2), and IV output power-stage (0.055 mm^2).

To be able to quantify the PSRR improvement, a similar CDA was fabricated without the proposed technique; its PSRR was measured for comparison, as depicted in Fig. 4.20. Fig. 4.21 shows the measured PSRR of the CDA with the proposed FFPSNC technique and the conventional CDA without the FFPSNC technique.

A peak PSRR value of 83 dB was obtained in the CDA with the proposed technique, when a 217 Hz sine-wave ripple of 250 mV was superimposed on the power-supply voltage, and no input signal was present.

From Fig. 4.21, it can be observed that the proposed technique achieves a PSRR improvement of 33 dB when compared with the similar CDA without it. This is expected from the implementation simulation shown in Fig. 4.18. Also, the FFPSNC technique is effective across the entire audio bandwidth.

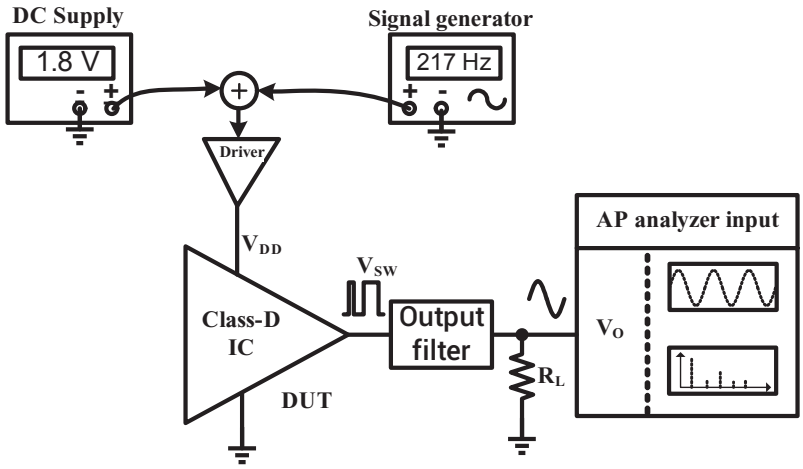


Figure 4.20: Test setup for PSRR measurement of single-ended CDA.

It is worth noting that the proposed FFPSNC technique can be applied to any single-ended CDA architecture to improve the PSRR performance, and that larger PSRR improvements can be achieved at the cost of additional silicon area and/or extra power consumption to improve the matching between R_5/R_6 or to achieve higher $A_{o,2}$ gain, as discussed in Section 4.4.

Table 4.2 summarizes the measured PSRR performance between the CDA with the proposed FFPSNC technique and the conventional CDA without it. As can be seen, the proposed technique is effective across the entire audio bandwidth while adding minimum area and quiescent power to the conventional design.

The additional silicon area and quiescent power consumption are 0.019 mm^2 (16%) and 49.5 μW (14%), respectively. The additional power and area is mainly due to the implementation of G_{FF}. Also, the measured PSRR improvement is similar to the expected results from the first-order CDA simulation, as shown in Fig. 4.17 and 4.18.

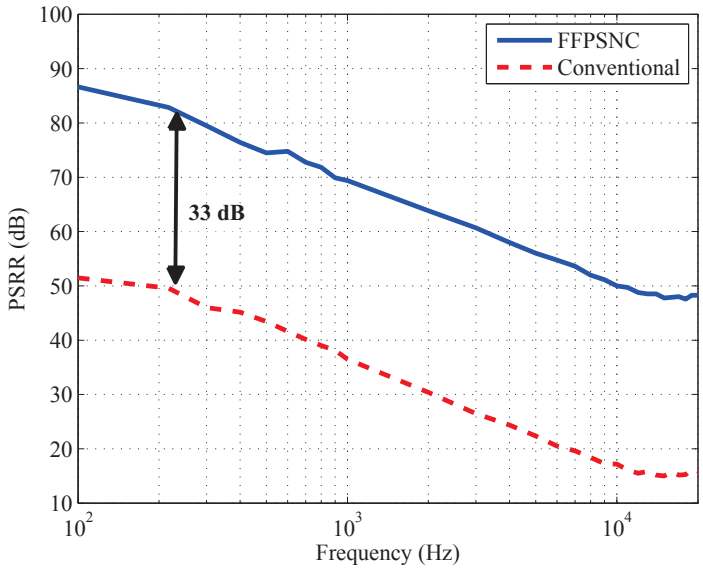


Figure 4.21: Class-D audio amplifier PSRR measurement results with FFPSNC technique.

Table 4.2: Comparison between conventional and FFPSNC technique

Parameter	FFPSNC	Conventional	Difference
PSRR @ 217Hz	83dB	50dB	33dB
PSRR @ 1kHz	69dB	36dB	33dB
PSRR @ 10kHz	50dB	17dB	33dB
Active area	0.121mm^2	0.102mm^2	0.019mm^2
Quiescent power	356μW	306.5μW	49.5μW

The proposed FFPSNC technique does not affect the CDA's loop parameters, as discussed in Section 4.3.1; thus, the following measurements achieved the same results with and without the proposed technique. The output spectrum of the system with an input $V_I = 0.5\ V_{RMS}$ at 1 kHz is illustrated in Fig. 4.22. The difference between the fundamental tone and the largest harmonic is -76.5 dB.

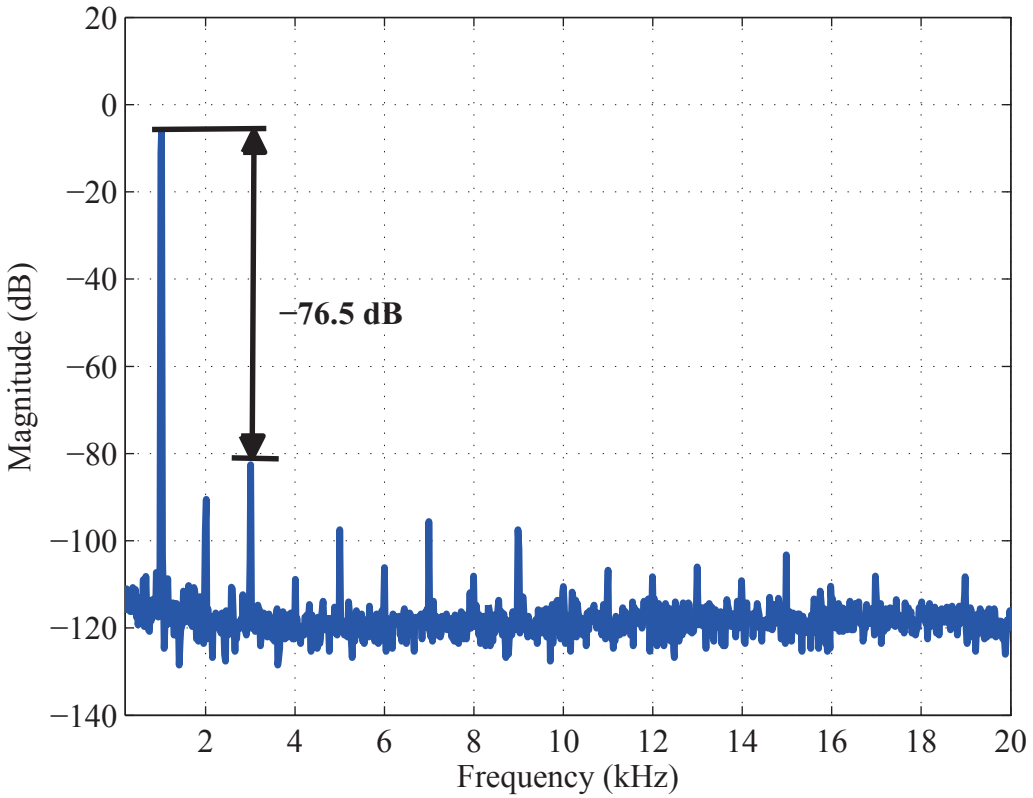


Figure 4.22: Measured output spectrum for CDA with FFPSNC technique with Vin= 0.5 Vrms at 1 KHz.

The measured THD+N versus output power is shown in Fig. 4.23. A minimum THD+N of 0.0149% was measured in the CDA prototype, and a minimum SNR of 84 dB was measured across all the audio bandwidth, as observed in Fig. 4.24.

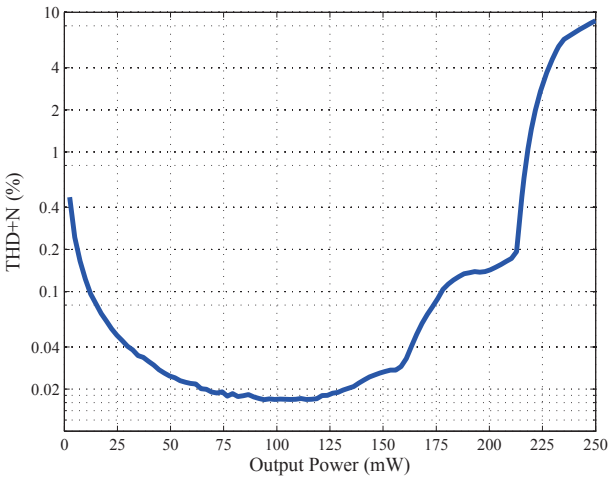


Figure 4.23: Measured THD+N versus output power for CDA with FFPSNC technique.

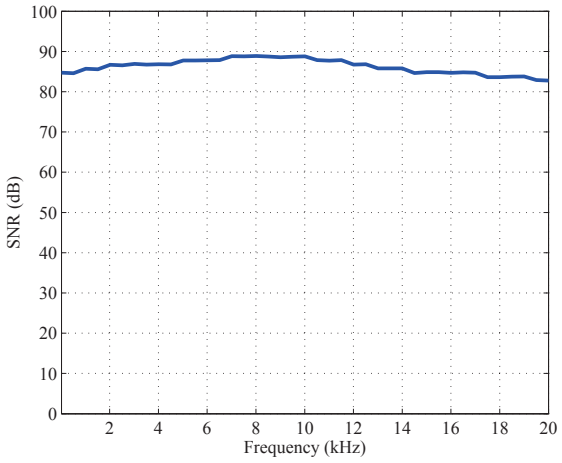


Figure 4.24: Measured SNR for proposed CDA with FFPSNC technique.

Fig. 4.25 shows the efficiency measurement setup where an 8 Ω resistor is used as the load, and low-value sensing resistors are used in series with the supply voltage and the load to measure the input and output current, respectively. Fig. 4.26 shows the measured amplifier efficiency versus the output power range from 2 mW to 250 mW.

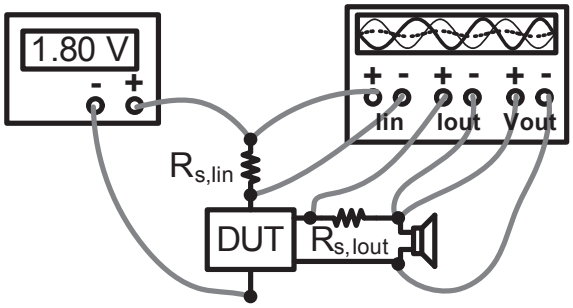


Figure 4.25: Test setup for efficiency measurement in single-ended CDA.

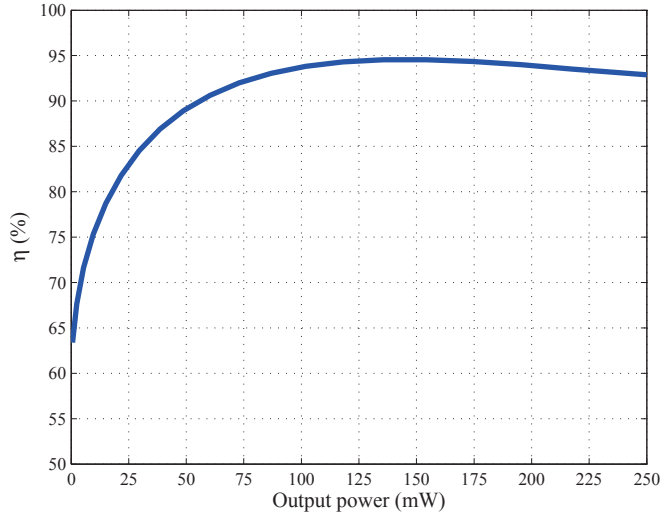


Figure 4.26: Measured efficiency versus output power for CDA with FFPSNC technique.

A maximum efficiency of 94.6% was measured when delivering 150 mW of output power. Since the output stage was optimized for operation in the low to medium output power range, the efficiency curve has its peak in the Region II of the efficiency curve, as discussed in Section 3.1.2 and Fig. 3.4.

The power-supply intermodulation distortion (PS-IMD) provides a linearity metric to quantify the intermodulation distortion between the amplifier's power-supply noise and the input audio signal, when both signals are present in the system as explained in [8, 64, 61, 42]. It was measured as show in Fig. 4.27 where a 1 kHz sine wave with 1 V_{pp} was used as the input of the audio amplifier together with 0.1 V_{pp} at 217 Hz signal at the amplifier supply source. The measured frequency spectrum of the output signal is shown in Fig. 4.28. As can be seen, both intermodulation tones are at least 81 dB below the fundamental tone.

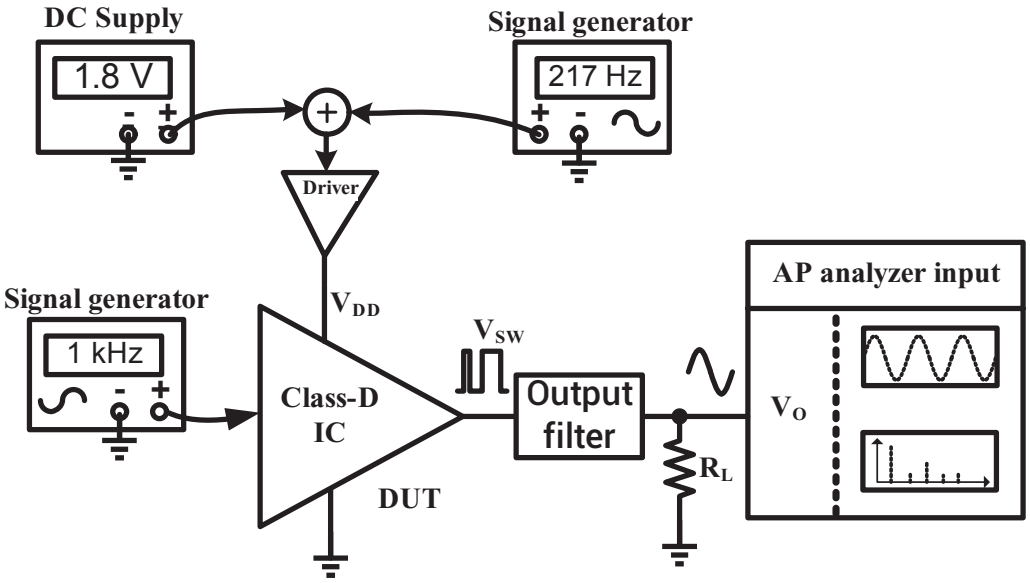


Figure 4.27: Test setup for PS-IMD measurement for single-ended CDA.

Fig. 4.29 illustrates the total area and quiescent power consumption breakdown for the proposed CDA. The proposed FFPSNC technique occupies only 16% of the total active area and consumes 14% of the total quiescent power. The output power stage occupies 45% of the active area and consumes 62% of the total quiescent power when no audio signal is applied.

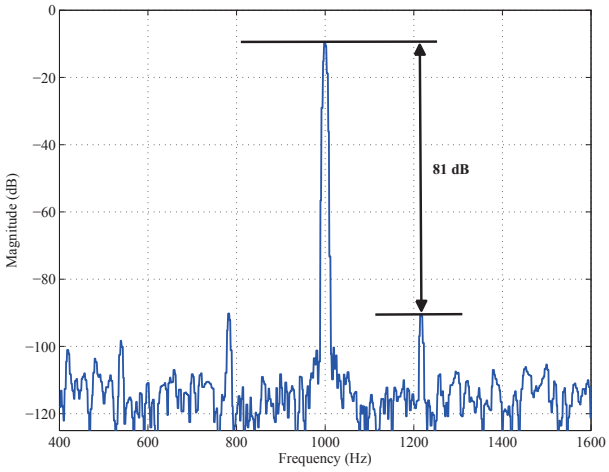


Figure 4.28: Power-supply intermodulation distortion measurement for CDA with FFP-SNC technique.

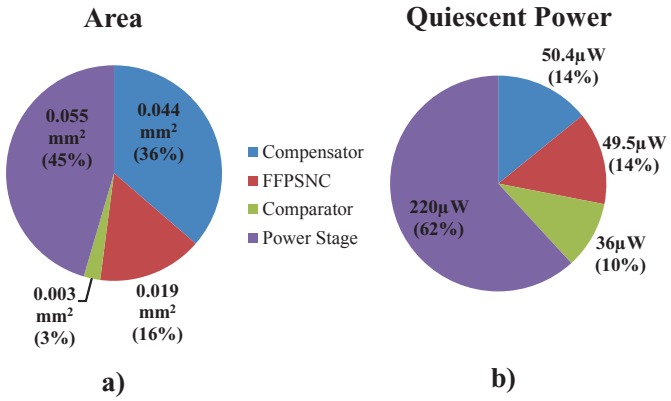


Figure 4.29: CDA with FFPSNC, a) area and b) quiescent power with $V_{in} = 0V$.

Table 4.3 compares the performance of the presented CDA with the FFPSNC technique to that of the state-of-the-art. As can be seen, the fabricated CDA achieves a PSRR comparable to CDAs with BTL architectures or high-order compensator filters, but with a low complexity implementation and low power consumption.

As discussed in Section 4.4.1, the PSRR can be improved further by decreasing the resistor mismatch in the G_{FF} implementation. This can be accomplished by occupying more silicon area using large widths in the resistor's layout; for this particular technology, a 0.1% can be achieved without special trimming by using a 30μ width in the resistor. Also,

Table 4.3: Comparison of FFPSNC technique with state-of-the-art

Parameter	This Work[a]	[8]	[9]	[62][b]	[97][c]	[42]	[64]
Compensator order	1	1	3	7	4	2	1
PSRR(dB) @ 217Hz	83	70	88	65	82	96	82
I_Q(mA)	**0.20**	4.70	3.02	22.00	1.40	4.00	0.55
P_Q(mW)	**0.36**	14.98	11.17	194.00	3.50	10.00	1.49
η(%)	**94.6**	75.5	85.5	88	80	93	84
Area (mm^2)	**0.121**	0.44	1.01	10.15	0.30	1.44	1.65
Process (μm)	0.18 CMOS	0.09 DMOS	0.18 CMOS	0.6 BCD MOS	0.065 CMOS	0.25 CMOS	0.5 CMOS
THD+N(%) @ 1 kHz	0.0149	0.0300	0.0180	0.0012	0.0132	0.0012	0.0200
Supply(V)	1.8	4.2	3.7	5.0	2.5	2.5	2.7
F_{SW}(kHz)	500	410	320	450	667	1000	380
Max P_{out}(W) @ 8Ω load	0.25	0.70	1.15	10 (6Ω)	0.05 (32Ω)	3.60	0.41
Load configuration	SE	BTL	BTL	BTL	SE	BTL	BTL

SE: Single-Ended, BTL: Bridge-Tied Load

[a] Do not include triangle-wave generator

dynamic element matching techniques could be implemented to achieve high accuracy in the resistor ratio but this would increase drastically the complexity as well as the silicon area occupied.

The PSRR performance of the single-ended can be enhanced further if the FFPSNC technique is applied to a high-order loop. For example, the second order compensator would use double the area and power of the first order compensator but the PSRR can achieve more than 100 dB at 217 Hz if the FFPSNC technique is applied, as observed in Fig. 4.17. The added cost to the actual design would be an additional 0.044 mm^2 (36%) area occupied and 51 μW (14%) power consumption.

4.7 Conclusion

The design methodology, implementation, and tradeoffs of a feed-forward power-supply noise cancellation technique were clearly delineated in this section; the proposed technique is capable of achieving high PSRR in single-ended class-D audio amplifiers. The attractive features of this approach are its simplicity and effectiveness. The tradeoffs for its utilization in several applications were discussed. A first-order single-ended PWM class-D audio amplifier was fabricated to demonstrate the effectiveness of the proposed technique. The class-D amplifier prototype achieves a PSRR of 83 dB at 217 Hz, a THD+N of 0.0149%, and a maximum efficiency of 94.6%. The proposed technique enhances the fabricated CDA's PSRR by 33 dB across the entire audio bandwidth compared with a conventional CDA without it. The class-D audio amplifier prototype was implemented using 0.18 μm CMOS standard technology and occupies a total area of 0.121 mm^2. It consumes a total of 356 μW of quiescent power.

5. A HIGH-EFFICIENCY SELF-OSCILLATING CLASS-D AMPLIFIER FOR PIEZOELECTRIC SPEAKERS*

5.1 Background in audio amplifiers for PZ speakers

The consumer's demand for smartphones and tablet computers with longer battery life has required manufacturers to implement the standard multimedia tasks, such as audio reproduction, using high-efficiency circuits. Switching DC-DC converters have been used in power management modules to achieve high-efficiency power conversion in battery-powered devices [20, 69, 102, 40]. The CDA uses a similar switching output stage as DC-DC converters to provide outstanding audio performance with high efficiency; but, to truly extend battery life, low power consumption is also required when the system is active. Conventional electromagnetic (EM) loudspeakers used in mobile devices require large amounts of power to operate, thereby limiting the battery life despite the amplifier's high efficiency.

The preferred loudspeaker for portable applications is the EM speaker. However, as discussed in Section 2.2.1, its electrical impedance across the audio frequency bandwidth behave as a low value resistor between 4 to 32 Ω, needing large electrical power to generate high SPL. On the other hand, the piezoelectric (PZ) speaker is an electromechanical transducer that consumes little electrical power while providing high SPL in small-form factors [19], as discussed in Section 2.2.2; these properties make the PZ speaker an attractive alternative to extend battery life in portable devices, especially when a high-efficiency switching amplifier such as the CDA is used [28, 103].

Open loop CDA architectures are cost effective and simple to implement. However, the

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absence of error correction limits their audio performance. To achieve outstanding audio performance in a CDA, closed-loop architectures are typically used where the negative feedback mechanism helps to correct errors in the amplification process. The closed-loop CDA has been analyzed for intermodulation distortion (IMD) in time domain [53] and in frequency domain [54]. Moreover, the carrier distortion and its effect on the system has been analyzed in [55], and the effect of power-supply noise was analyzed in [58]. The conclusion is that large loop gain and a high-frequency carrier in the system help to attenuate the distortion components and supply noise of the closed-loop system, improving the audio performance.

Closed-loop CDA architectures have been proposed to achieve high efficiency and good audio performance using different modulation techniques such as pulse-width modulation (PWM) [45, 46, 59], pulse-frequency modulation (PFM) [62, 43], or sliding-mode control (SMC) [63, 64], as discussed in Section 3.2. However, these architectures have an output stage that is typically optimized to drive low impedance loads such as the EM speaker and might not be suited to provide the high-voltage output swing needed for the PZ speaker. Typical voltage levels across the PZ speaker terminals should be in the range of 10-20 V_{pp} to achieve the maximum sound pressure level (SPL), and could be generated from the battery using high-efficiency step-up voltage circuits [20, 21, 22].

High-voltage semiconductor devices such as DMOS, LDMOS, or drain-extended MOS transistors are typically used to withstand the large voltage potential needed at the output stage. Unfortunately, these devices are typically optimized to minimize conduction losses, and their parasitic capacitors can be large, increasing the power consumption due to their large switching losses, especially when a high-frequency carrier signal is used [47, 27, 48, 49, 50]. Furthermore, using these devices in monolithic implementations would require additional fabrication steps and/or a larger silicon area; thus, increasing the cost of the amplifier. Commercial CDA architectures for PZ speakers provide high-

voltage outputs using these devices, but their distortion and power consumption is still large [23, 24, 25, 26].

Other switching output stages have been proposed to drive high-voltage capacitive actuators for different applications [29, 104]. Nonetheless, the primary objective of these applications is to deliver the maximum amount of energy at the actuator's resonant point, making them not suitable for audio applications.

This section discusses the design tradeoffs of the CDA architecture for driving PZ speakers, especially when low power consumption and high efficiency are desired. An example implementation is proposed to achieve high-efficiency and high-linearity in the CDA architecture for PZ speakers to extend battery life in mobile devices. The self-oscillating closed-loop architecture is used to obviate the need of a carrier signal generator to achieve high linearity with low power consumption. Moreover, the CDA monolithic implementation is able to provide an 18 V_{pp} output voltage swing in an 1.8 V core-voltage twin-well 11-16 Ω-cm p-type substrate CMOS technology without requiring expensive special high-voltage semiconductor devices. The use of stacked-cascode CMOS transistors at the H-bridge output stage provides low input capacitance to allow high switching frequency to improve linearity without sacrificing the high efficiency.

5.2 Class-D amplifier design considerations for piezoelectric speakers

The PZ speaker capacitive nature needs a different definition of power efficiency since ideally it does not dissipate average power. Thus, the typical definition of efficiency can't be used. As discussed in Section 2.3.4, the amplifier's power efficiency for capacitive loads could be defined as [31, 32, 33],

$$\eta \cong \frac{P_{o,APP}}{P_{o,APP} + P_{loss}} \tag{5.1}$$

$$P_{o,APP} = V_{o,RMS} \cdot I_{o,RMS} \cong \frac{V_{o,RMS}^2}{|Z_L|} \tag{5.2}$$

$$P_{LOSS} = P_Q + P_{CL} + P_{SW} + P_{BD} + P_{FILT} \tag{5.3}$$

where the power dissipation in the CDA (P_{LOSS}) is mainly dominated by the amplifier quiescent power (P_Q), the conduction losses (P_{CL}), switching losses (P_{SW}) and body-diode losses (P_{BD}) of the output stage, and the losses due to the current ripple in the output filter together with the dielectric losses of the PZ speaker (P_{FILT}). The real power losses in the output filter can be expressed as,

$$P_{FILT} = I_{OUT,RMS}^2 \cdot |Z_F| \cos(\varphi) + C_{PZ} \cdot V_{OUT,RMS}^2 \cdot 2\pi \cdot F_{audio} \cdot DF \tag{5.4}$$

where $|Z_F| \cos(\varphi)$ is the resistive part of the output filter impedance at F_{SW}, C_{PZ} is the equivalent capacitance of the PZ speaker, F_{audio} is the output audio frequency applied to the PZ speaker, and DF is the dissipation factor of the PZ speaker. Typical dissipation factors range from 0.4% up to 1%.

It can be noticed that the output filter component selection affects the real power dissipation, and the DF of the PZ speaker could dominate the P_{FILT} for large operating frequencies and amplitudes. To achieve high efficiency, the CDA has to process the power of the highly reactive load with minimum power dissipation dominated by the power losses in the amplifier and output filter.

The main contributors of P_{SW} are the input and output capacitance of the output stage that can be large if the switches are sized to obtain small R_{dsON}. As discussed in Section 3.1.4, the advantage of using a PZ speaker is that its high impedance requires small current to operate, minimizing the impact of P_{CL} in the efficiency. This would allow smaller output switches to obtain the same P_{CL} but will decrease the P_{SW}, enhancing the overall efficiency. Moreover, the small output current together with a short $t_{deadtime}$ will reduce

the P_{BD} contribution to the total power losses. To reduce the impact of the supply voltage variation due to the body-diode di/dt, a low inductance package can be used with several bonding wires in parallel for the supply, ground, and outputs.

Another consideration is that the high-voltage special semiconductor devices needed at the output stage to safely operate with the high-voltage swing required by the PZ speakers possess large input and output capacitances which would restrict the carrier signal frequency due to their large switching losses. Thus, the output stage design needs to consider the tradeoffs between high voltage operation, power efficiency, and linearity.

The high-voltage switching output in the CDA for PZ speakers could impact the EMI radiated by the inductance of the cables and/or PCB traces connecting the CDA with the speaker. This is particularly important in mobile devices since most of the circuits are placed closely. Thus, the sensitive analog circuits could be drastically affected by the EMI. Several techniques to improve the EMI can be used to spread the energy of the high-frequency carrier signal used in PWM modulation, at the expense of additional power consumption and design complexity [45, 46]. The advantage of using the PZ speaker is its inherent filtering, as observed in Fig 3.7, that can be leveraged to minimize the high-frequency energy at the output.

5.3 Proposed class-D architecture for piezoelectric speakers

A new class-D output stage is devised using cascode devices to be able to operate at supply voltages higher than the technology nominal voltage with high efficiency. The advantage of using cascode devices at the output stage is that the input and output capacitances are reduced considerably since smaller thick oxide transistors could be used as switches to withstand the high-voltage output signal. Thus, the carrier signal frequency can be increased to enhance linearity with low power consumption.

5.3.1 Architecture description

The proposed CDA architecture for driving PZ speakers with low power consumption and high linearity is shown in Fig. 5.1. A self-oscillating first-order loop was employed to avoid the extra power consumption of the modulation carrier generator, as discussed in Section 3.2.3. Unlike PWM or PFM modulations, the self-oscillating modulation provides inherent frequency spreading of the carrier signal to decrease the EMI without any extra power consumption.

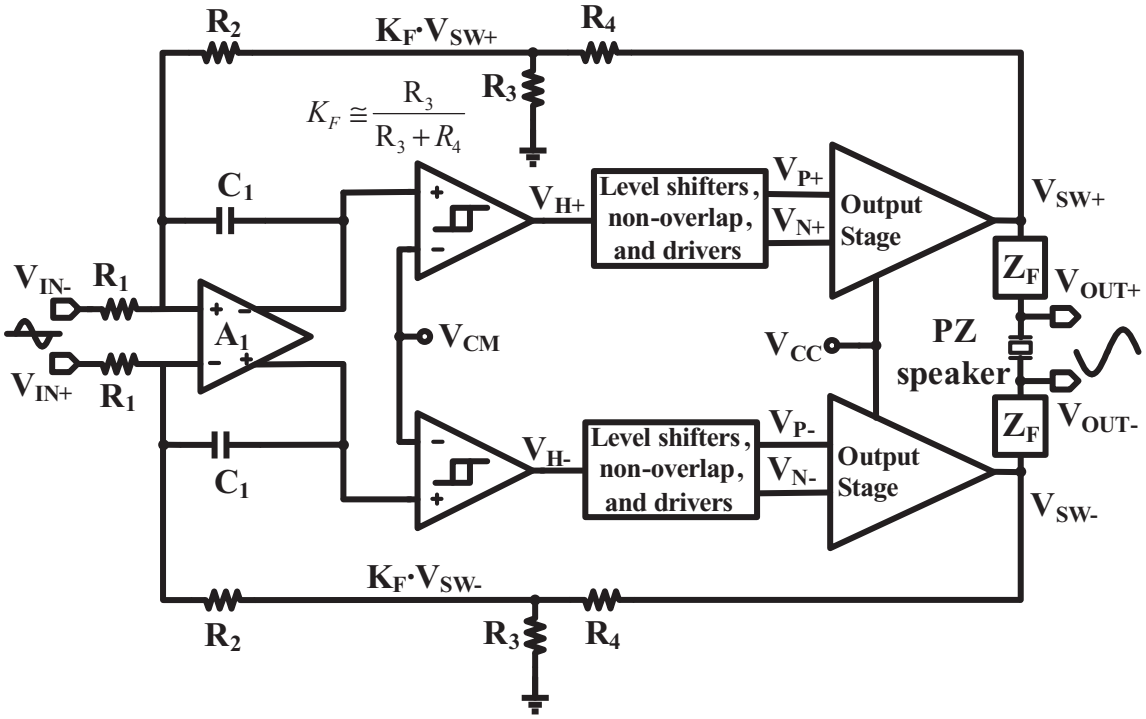

Figure 5.1: Proposed CDA architecture for PZ speakers.

A fully-differential architecture was implemented to provide more dynamic range, low distortion, and higher PSRR in the CDA. The amplifier A_1 implements a first-order integrator as compensator to obtain the error signal from the difference between the input and

feedback signals. The integrator's output signals are modulated by a pseudo-differential arrangement of hysteretic comparators to generate low voltage switching signals (V_{H+}, V_{H-}). These signals pass through non-overlapping, level shift, and pre-driver circuits, generating the gate signals for the stacked-cascode output stage. For this implementation, to achieve the desired 18 V_{PP} output signal from the H-bridge, the high-voltage supply $V_{CC} = 9\ V$ was chosen.

The proposed stacked-cascode H-bridge output stage applies the high-voltage output switching signals (V_{SW+}, V_{SW-}) to the PZ speaker through an impedance (Z_F). The impedance Z_F is used in series with the PZ speaker to limit the current consumption at high frequencies and implement a low-pass filter to reduce the energy of the carrier's frequency components at the output.

Finally, the output high-voltage switching signals are fed back to the integrator using a resistive divider with factor $K_F = 1/5$ to adjust the high-voltage signal back to the nominal voltage of the technology. This selection would fix the differential closed-loop gain of the CDA to 10 V/V or 20 dB. Resistors $R_3 = 10\ k\Omega$ and $R_4 = 40\ k\Omega$ were chosen taking into account the tradeoff between their effect on the integrator's time constant and the power consumption [62].

5.3.2 Compensator design

A fully-differential first-order integrator was employed to provide high loop gain to correct for errors in the feedback loop. A higher order compensator could be used to achieve better performance but at the cost of more power consumption and design complexity to maintain stability for all modulation indexes [62, 59]. The compensator was designed taking into account the tradeoffs discussed in Section 3.2 and Section 3.3.1.

The integrator's ideal time constant is implemented by $\tau_I = R_1 \cdot C_1$, and its value selection depends on several tradeoffs between the passive component values, amplifier A_1

power consumption, linearity, and in-band noise. The transfer function for the implemented integrator yields,

$$G_{int,actual}(s) \cong -\frac{\left(\frac{1}{s \cdot R_1 \cdot C_1}\right)}{1 + \frac{s}{GBW} \cdot \left(\frac{s \cdot R_{1,2} \cdot C_1 + 1}{s \cdot R_{1,2} \cdot C_1}\right)} \tag{5.5}$$

where $R_{1,2} = R_1 // R_2$. To avoid significant deviations in the integrator's performance, the amplifier's gain-bandwidth product (GBW) has to be higher than $f_{int} = 1/(2\pi\tau_I)$. A large value for f_{int} would provide a higher bandwidth for the CDA loop that will result in high linearity, high PSRR at higher frequencies, and smaller values for the passive components. However, the amplifier's power would need to be increased to avoid deviations in f_{int} due to finite GBW. The $f_{int} = 50\ kHz$ was chosen as a compromise between these tradeoffs to provide high loop gain across the audio frequency bandwidth with low power consumption.

The input resistor values have to be chosen considering the tradeoff between the resistor's thermal noise contribution and its matching requirements for loop performance [58]. For this implementation, the integrator's component values are $C_1 = 8\ pF$ and $R_1 = R_2 = 400\ k\Omega$. The amplifier A_1 provides a DC gain of 45 dB with a GBW of 70 MHz. This design selection yields a magnitude error and phase error in the integrator function of 0.5% and 0.07% [84], respectively.

5.3.3 Self-oscillating modulator design

The hysteresis window of the comparators in the modulator, the integrator's time constant, and the propagation delay in the loop will determine the modulation frequency of

the self-oscillating system as expressed in,

$$F_{SW}(D) = \frac{D \cdot (1-D)}{\frac{V_{hyst} \cdot \tau_{int}}{V_{supply}} + \tau_d} \tag{5.6}$$

where V_{supply} is the supply voltage of the comparator, V_{hyst} is the voltage hysteresis window of the comparator, τ_{int} is the integrator's time constant, and τ_d is the propagation delay from the comparator to the input of the integrator, including the comparator delay. As discussed in Section 3.2, the average value of F_{SW} could be chosen taking into account the tradeoffs between power consumption, distortion, output filter components, and the excitation of undesired mechanical resonant modes in the PZ speaker [19].

A higher value of F_{SW} would result in less distortion and smaller output filter components but at the expense of extra power consumption due to higher switching losses [62], and wider GBW of A_1. On the other hand, a low value of F_{SW} would reduce the power consumption but at the expense of more distortion and bigger output filter component values [55].

Leveraging the low input capacitance of the stacked-cascode output stage in the proposed class-D output stage, a high-frequency carrier is used to achieve high linearity with high efficiency. The average value of $F_{SW} = 800\ kHz$ was chosen as a compromise between these tradeoffs for this implementation. Therefore, from (5.6), V_{hyst} can be found for a D = 0.5 as,

$$V_{hyst} = \frac{V_{supply}}{\tau_{int}} \cdot \left(\frac{1}{4 \cdot F_{SW}} - \tau_d \right). \tag{5.7}$$

For a $V_{supply} = 1.8\ V$, $F_{SW} = 800\ kHz$, $\tau_{int} = 3.2\ \mu s$, and $\tau_d = 100\ ns$, a $V_{hyst} \cong 120\ mV$ was obtained. Fig. 5.2 shows the variation of the calculated F_{SW} versus the duty cycle (D) for several τ_d cases as expressed in (3.20). It can be seen that F_{SW} is a parabolic function of D, and the delay τ_d would impose a limit in the maximum achievable F_{SW}.

For the assumed $\tau_d = 100\ ns$, the average switching frequency decreases from 800 kHz to 300 kHz as the peak input amplitude increases.

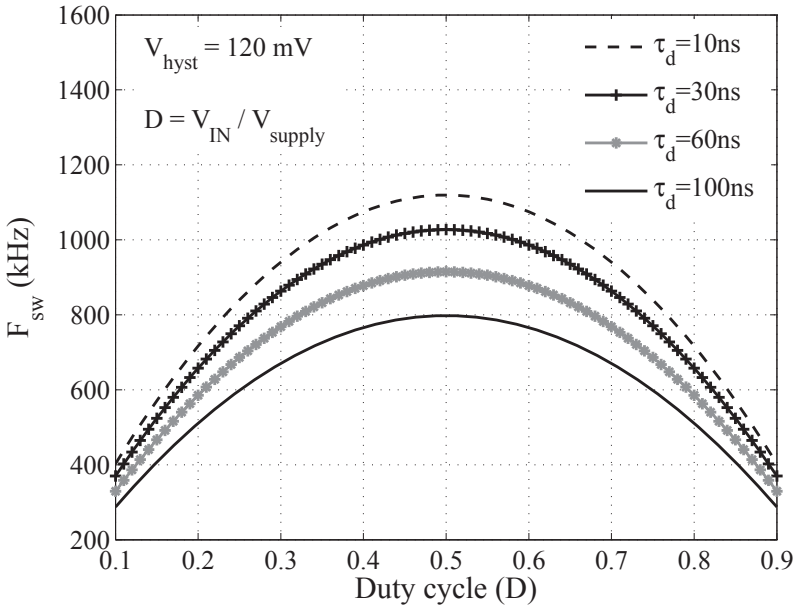

Figure 5.2: Calculated switching frequency (F_{SW}) versus duty cycle (D) of the CDA for several propagation delay (τ_d) cases with a fix hysteresis window.

One of the drawbacks of the variable-frequency modulation is that the output current ripple will be increasing for large audio signals due to the decreasing F_{SW}, as expressed in (5.4). Thus, the output RMS current will increase, and the real power dissipation in the non-ideal components of the output filter will increase as expressed in (5.4). The F_{SW} variation could be reduced if needed by controlling the main parameters in (3.20) such as the propagation delay [69], the hysteresis window [70, 71], or the integration time constant [72]. For this implementation, the variable F_{SW} will be exploited to help spread the energy of the high-voltage high-frequency switching signal at the output of the audio amplifier to decrease the radiated EMI components.

5.3.4 Output filter design for PZ speakers

Another consideration about the capacitive behavior of the PZ speaker is that it presents a low impedance value at high frequencies, especially close to F_{SW}, that will increase the current consumption of the speaker if it is driven directly by the switching output signal. To minimize this effect, an impedance Z_F can be placed in series with the PZ speaker to limit the current delivered to it at high frequencies, that makes it possible to use smaller transistors in the stacked-cascode output stage. An additional benefit of using Z_F in series with the PZ speaker is the inherent filtering function since the PZ speaker behaves as a capacitor. This inherent output filter will mitigate the high frequency components of the high voltage switching output that could negatively impact the EMI.

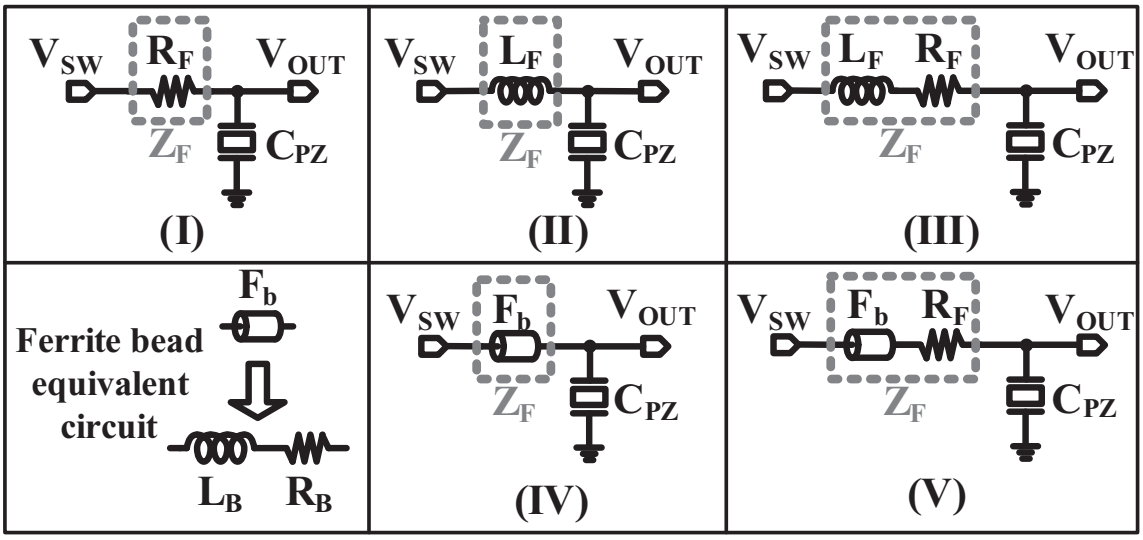

Figure 5.3: Different output filter configurations for impedance Z_F together with PZ speaker equivalent impedance C_{PZ}.

Several options for implementing Z_F can be selected as shown in Fig. 5.3; single-ended configurations are shown for simplicity. A current limit resistor (R_F) can be used

as in Fig. 5.3 (I) since its impedance is constant and independent of frequency. However, using a resistor could impact the efficiency of the overall audio system since it would dissipate power. Its value selection needs to take into account the cut-off frequency of the low pass filter, current limit, and power dissipation. The transfer function of the resulting first order RC low pass filter with cut-off frequency ω_{RC}, given by R_F and the PZ speaker impedance (C_{PZ}), is expressed as

$$\frac{V_{OUT}(s)}{V_{SW}(s)}_{I} = \frac{1}{1+s/\omega_{RC}} = \frac{1}{1+s\cdot C_{PZ}\cdot R_F}. \tag{5.8}$$

A more power-efficient alternative is to use a reactive element to implement Z_F. An inductor can be used as in Fig. 5.3 (II). The inductor high impedance at high frequencies compensates for the low impedance of the PZ speaker to have a more constant output impedance, thereby limiting the current. Moreover, the resulting low pass filter is second order, minimizing the EMI and the carrier signal energy at the PZ speaker. R_F is used as in Fig. 5.3 (III) to introduce damping in the second order filter to avoid unwanted peaking that can increase the output signal distortion.

However, the R_F value needs to be chosen taking into account its power dissipation since the inductor ripple would dissipate real power across the resistor. The transfer function of the second order low pass filter, with cut-off frequency ω_{LC} given by the L_F and C_{PZ}, is expressed as,

$$\begin{aligned}\frac{V_{OUT}(s)}{V_{SW}(s)}_{III,V} &= \frac{\omega_{LC}^2}{s^2+s\cdot 2\cdot\zeta\cdot\omega_{LC}+\omega_{LC}^2} \\ &= \frac{1/(L_F\cdot C_{PZ})}{s^2+s\cdot(R_F/L_F)+1/(L_F\cdot C_{PZ})}.\end{aligned} \tag{5.9}$$

Fig. 5.4 shows the frequency magnitude response for different output filter configurations.

It can be observed, that filter III provide the best attenuation at the EMI region, but at the expense of more external components; on the other hand, the filter I uses less external components, but at the expense of less attenuation at the EMI region and increased power dissipation.

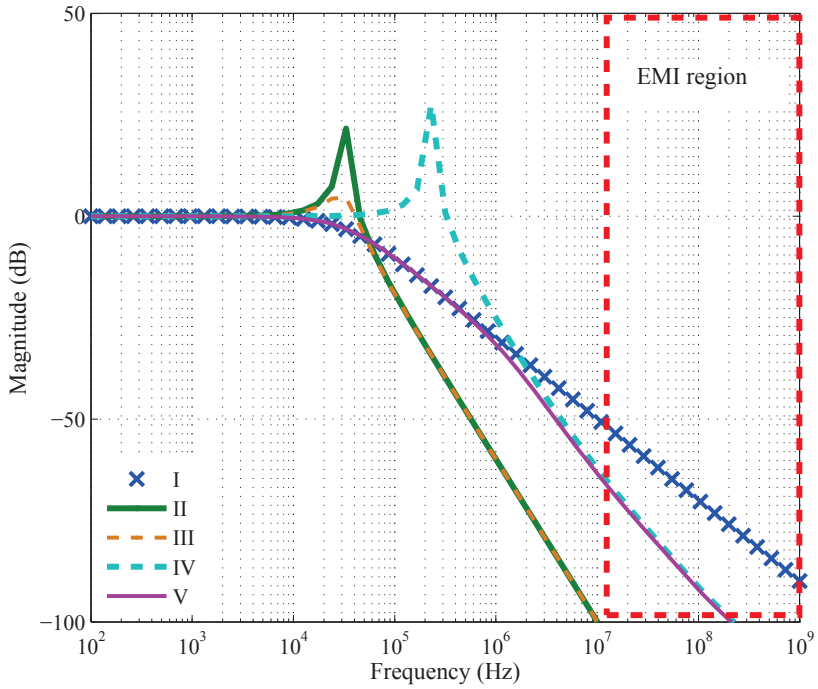

Figure 5.4: Bode plot for output filter configurations with PZ speaker.

The main drawbacks of choosing Z_F as an inductor are the component cost and PCB area occupied. On the other hand, if an application does not require a low cut-off frequency in the low-pass filter but requires low EMI, a ferrite bead (Fb) can be used as the reactive element to filter out the high frequency components as in circuit Fig. 5.3 (IV) and (V). The ferrite bead behaves as an inductance (L_B) at high frequencies and as a low value resistor (R_B) at low frequencies as shown in Fig. 5.3.

Ferrite beads cost less than an inductor and use less PCB area. However, the ferrite bead selection needs to take into consideration the peak current capability of the core material to avoid current saturation and variations in the equivalent inductance that could increase signal distortion. Also, the equivalent series resistor R_B value needs to be considered to avoid extra power dissipation.

5.4 Proposed stacked-cascode H-bridge output stage

The main motivation for using stacked-cascode switches in the H-bridge output stage is to reduce the switching losses due to the small input and output capacitors. Moreover, it allows to handle high voltages in monolithic implementations while ensuring sufficient lifetime in a CMOS technology with a significantly lower supply voltage. This over-voltage protection is conceptually illustrated in Fig. 5.5, where the stacked-cascode transistors absorb enough voltage across them to allow safe operation in the main switch.

The use of cascodes in the output stage of the CDA presents two main challenges. First, the switching output signal (V_{SW}) is changing between V_{CC} and GND. Therefore, two different gate voltages for the cascode transistor connected to the output terminal are required [39]. This is to avoid exceeding the maximum allowed voltage potential across any of its terminals during the output high or low state. Therefore, a simple adaptive biasing structure is proposed for this implementation to safely operate the stacked-cascode H-bridge. Second, the R_{dsON} and V_{SD} increase by adding cascodes. The impact of the conduction losses will depend on the average output current flowing through the stacked-cascode switches. Each additional stacked-cascode switch will increase the total V_{SD} that will increase the P_{BD}. However, since the PZ speakers appear as a high impedance to the amplifier, the RMS current flowing through the H-bridge is small, lessening the impact of large R_{dsON} and V_{SD} on the efficiency.

5.4.1 Stacked-cascode output stage description

The proposed stacked-cascode output stage for driving PZ speakers is illustrated in Fig. 5.6. Thick-oxide 3.3 V transistors were used in the output stage; however to achieve safe operation the top PMOS transistor has to ensure that its N-well to substrate potential does not exceed the reverse bias breakdown voltage of 10.8 V for the CMOS technology used, limiting the V_{CC} to 9 V.

The thick-oxide devices can tolerate sustained operation within 10% of their voltage rating but they can suffer from irreversible damage if the voltage across its terminals exceed the gate oxide breakdown voltage of 5.2 V. All the transistors have their sources tied to their bulk to avoid larger R_{dsON} due to the body effect; where the NMOS cascode devices use triple-well transistors with N-well voltage (V_{NW}) of 7.5 V to reverse bias the P-well to N-well diode.

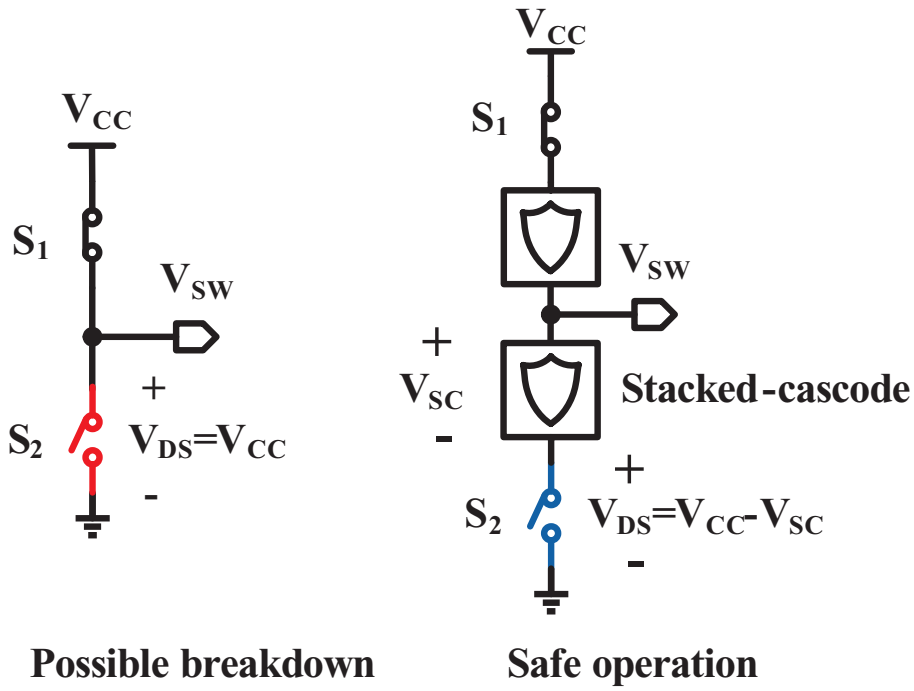

Figure 5.5: Stacked-cascode over-voltage protection conceptual operation.

The transistors M_1, M_6, M_7, and M_{12} are the input switches of the H-bridge. Two cascode transistors are stacked vertically on top of each input switch to avoid exceeding the maximum allowed voltage potential across any of their terminals. The biasing at the gates of the cascode devices ensure that when the signal switch $M_1, 12$ or $M_6, 6$ are off, the source voltages of the cascode devices will follow,

$$V_S > V_G - V_{TH} \tag{5.10}$$

where V_S is the source voltage, V_G is the gate voltage, and V_{TH} is the threshold voltage of the transistor.

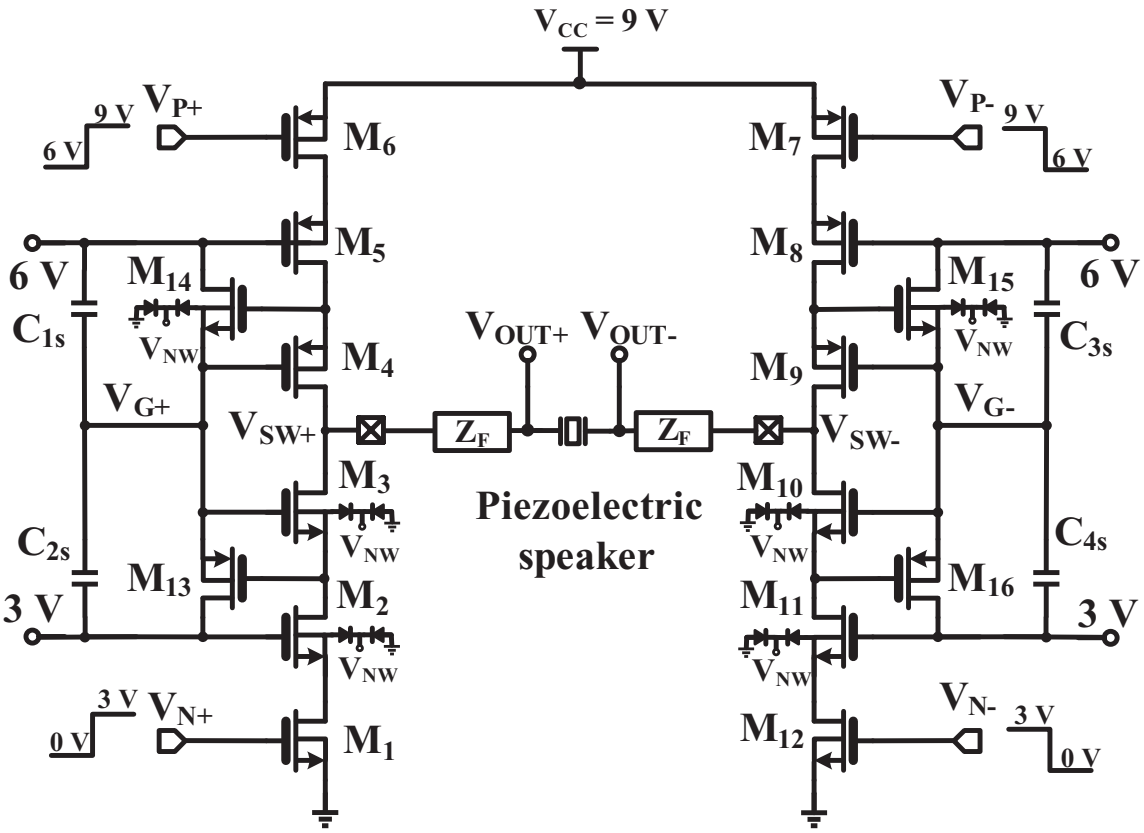

Figure 5.6: Proposed output stage schematic for driving PZ speakers.

The gate voltage of M_2 and M_{11} is fixed to 3 V, while the gate voltage of M_5 and M_8 is fixed to 6 V. This is to ensure that the voltage drop across any terminal of the transistors is below 3.3 V. Table 5.1 details the design procedure for the biasing of the proposed stacked-cascode output stage for PZ speakers.

The output switching node V_{SW} will be switching between 0 V and 9 V; therefore, the gate of transistors M_3, M_4, M_9, M_{10} needs to change is voltage to ensure the safe operation of these transistors. Transistors $M_{13} - M_{16}$ are used as switches to alternate the gate voltage (V_G) of the cascode transistors M_3, M_4, M_9, and M_{10}, between 3 V and 6 V, depending on the switching state. These gate voltages allow safe operation during the switching transient for the transistors. Capacitors $C_{1s} = C_{3s} = 9\ pF$ and $C_{2s} = C_{4s} = 2\ pF$ are used to stabilize the node V_G by absorbing the charge injected at this node during the switching transients.

5.4.2 Stacked-cascode output stage operation

The steady-state operation of the proposed stacked-cascode output stage of the two switching states for half of the H-bridge is depicted in Fig. 5.7 for the switching high state, and low state; for simplicity, transistors M_{14} and M_{13} were replaced for switches S_1

Table 5.1: Stacked-cascode biasing design procedure

1. Determine $V_{CC} = V_{O,RMS}/2$ for maximum SPL of the chosen PZ speaker.
2. Verify the maximum allowed rated voltage (V_{BRK}) across any terminal for the chosen devices of the CMOS technology.
3. Determine the number of devices $N = V_{CC}/V_{BRK}$ needed in series.
4. Select $V_{G,PMOS} < V_{CC} - V_{BRK} + V_{TH}$.
5. Select $V_{G,NMOS} < V_{BRK} + V_{TH}$.
6. Capacitors C_{1s} and C_{2s} are sized such that node V_G does not change during the high to low transition and low to high transition, respectively.

and S_2, respectively.

For the switching high state, transistors $M_4 - M_6$ and switch S_1 are ON, and transistors $M_1 - M_3$ and switch S_2 are OFF. On this operating condition, the voltage at V_G is 6 V, allowing a maximum voltage drop of 3 V across any of the terminals of transistors $M_2 - M_5$. The capacitor C_{2s} was chosen to provide a low impedance path for the current injected during the low to high transition by the parasitic capacitance $C_{p,ON}$, that is mainly composed of $C_{gd,M4}$, $C_{gs,M4}$, and $C_{gs,M14}$.

Similarly, for the switching low state, transistors $M_4 - M_6$ and switch S_1 are OFF, and transistors $M_1 - M_3$ and switch S_2 are ON.

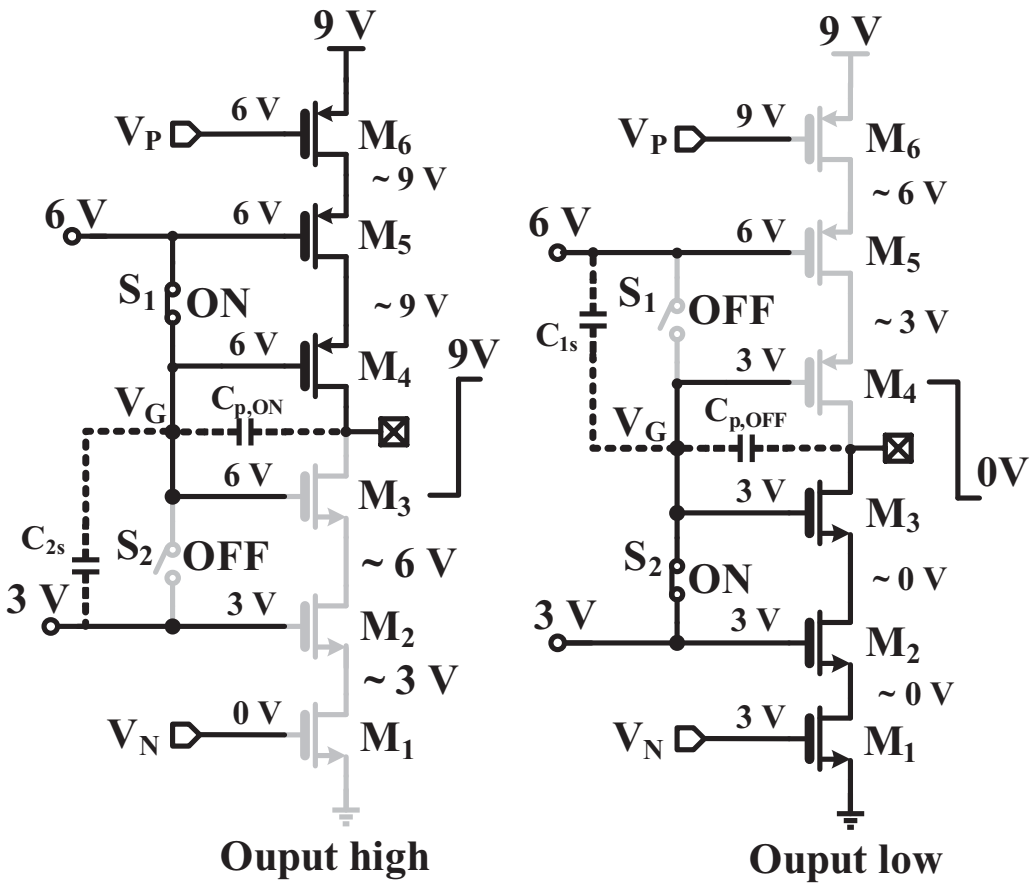

Figure 5.7: Proposed stacked-cascode output stage simplified operation.

For this operating condition, the voltage at V_G is 3 V, allowing a maximum voltage drop of 3 V across any of the terminals of transistors $M_2 - M_5$. The capacitor C_{1s} absorbs the current injected during the high to low transition by the parasitic capacitance $C_{p,OFF}$ mainly comprised of $C_{gd,M3}$, $C_{gs,M3}$, and $C_{gs,M13}$.

The automatic adjustment of V_G allows a safe operation for the cascode transistors connected to the output terminal. To verify this, the circuit was simulated across process and temperature variations (PVT) for the slow PMOS and slow NMOS (ss) case, the slow PMOS and fast NMOS (sf) case, the fast PMOS and fast NMOS (ff) case, and the fast PMOS and slow NMOS (fs) case. The node V_G was saved on each simulation case, and the results are plotted in Fig. 5.8.

It can be observed that V_G never exceeds the 6.5 V or 2.5 V limits, avoiding stress in the transistors that could deteriorate their performance. The timing variations observed are expected since the blocks used in the implementation of the CDA will vary the loop delay τ_d by small amounts, changing the F_{SW} as shown in Fig. 5.2.

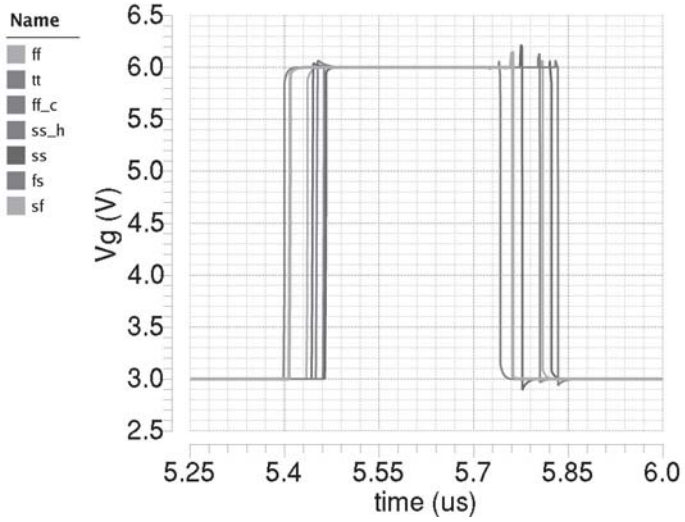

Figure 5.8: Transient simulation of V_G across PVT.

5.4.3 Gate driver design

Fig. 5.9 shows the block diagram for the proposed gate driver of the stacked-cascode output transistors for half-bridge of the output stage. The goal of the gate drivers is to drive the large gate capacitance of the output MOS devices.

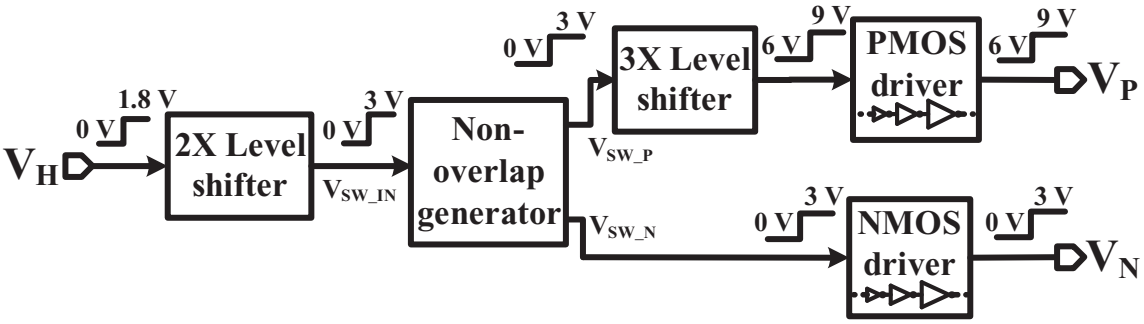

Figure 5.9: Gate driver block diagram stacked-cascode output stage.

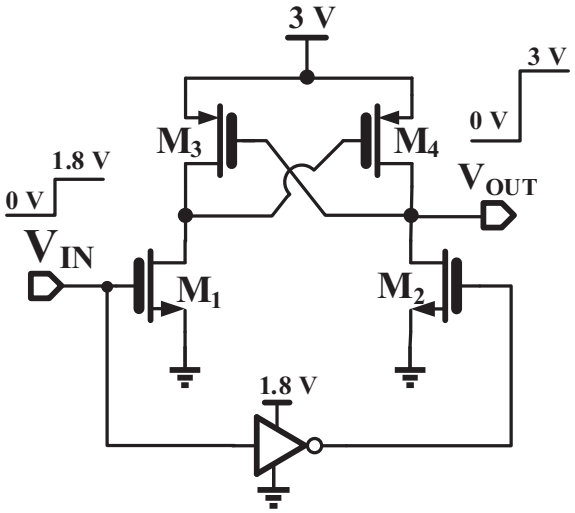

Figure 5.10: Level shifter from 1.8 V to 3 V schematic.

The switching output of the comparators (V_H) is level shifted from 1.8 V to 3 V using a cross coupled level shifter circuit as shown in Fig. 5.10. The level shifter uses positive feedback implemented by thick-oxide transistors $M_3 - M_4$ to decrease the propagation delay of the block. The output of the level shifter switch between 3 V and ground

A non-overlap signal generator is used to avoid excessive short circuit current at the output stage. The non-overlap time of 2 ns or dead-time of 0.16% of the period is chosen as a tradeoff between the propagation delay τ_d in the loop, efficiency, and distortion [85].

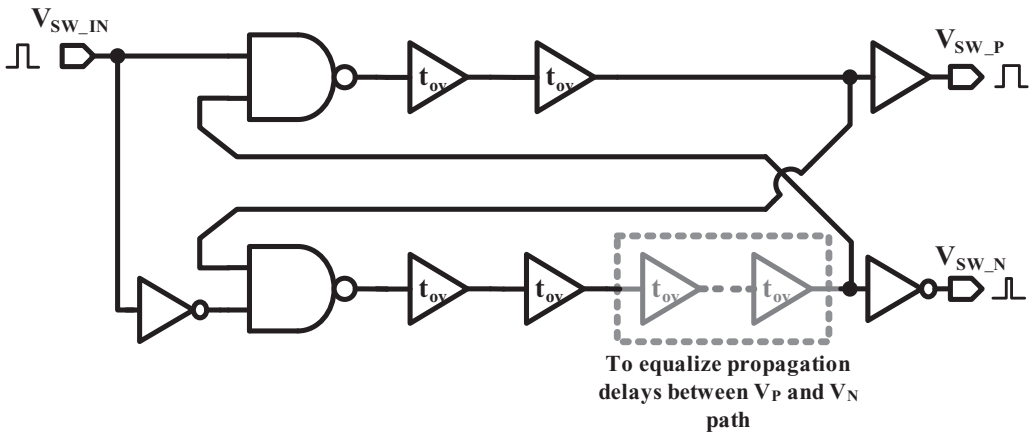

Figure 5.11: Implemented non-overlap generator for gate drivers.

The non-overlapped signals, as illustrated in Fig. 5.12, are applied to the pre-driver circuits that will drive the gates of the stacked-cascode output transistors.

The PMOS signal path has an extra level-shift block that introduces some delay and makes the non-overlap delay at the output signals (V_P/V_N) asymmetrical. This asymmetry would cause the switching node to introduce distortion to the audio signal. To correct this, the non-overlap delay for the NMOS path was adjusted to the PMOS path by introducing extra delay elements, as observed in Fig. 5.11.

The gate signal (V_P) of the output PMOS switch connected to V_{CC} needs to switch between 6 V and 9 V to avoid excessive high voltage potential across its terminals. This is achieved by level-shifting the switching signal from 0-3 V to 6-9 V using a high-speed 3X level-shifter [105] with triple-well NMOS transistors in the inverters to shift the ground level to 6 V, as shown in Fig. 5.14. Stacked-cascode transistors are also used to protect from exceeding voltage stress limit in the main switches of the level shifter. A bootstrap capacitor C_{3X} is used to reduce the propagation delay of the block by injecting current in the positive feedback latch implemented by $M_6 - M_7$.

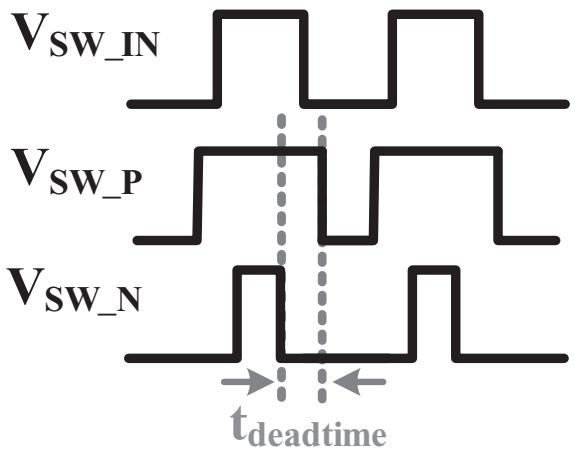

Figure 5.12: Non-overlapping gate drive typical waveforms.

The PMOS drivers use floating inverters with triple well thick-oxide transistors to keep the signal switching between 6 V and 9 V, as shown in Fig. 5.13. The NMOS drivers are implemented using 1.8 V transistors. The main goal of these gate drivers is to minimize the delay with minimum switching loss.

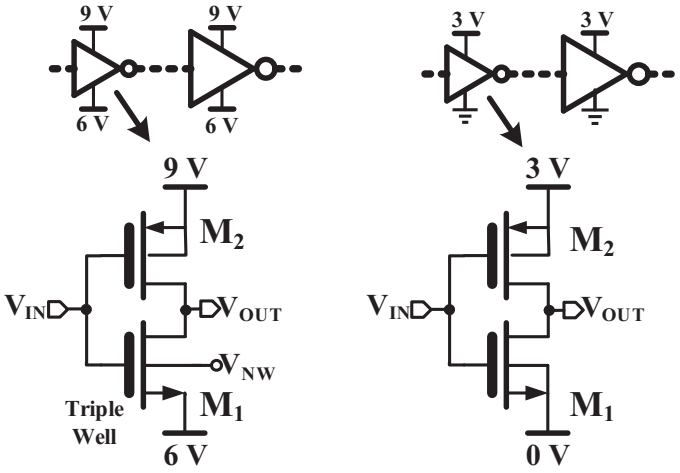

Figure 5.13: Gate drivers implementation for PMOS and NMOS path.

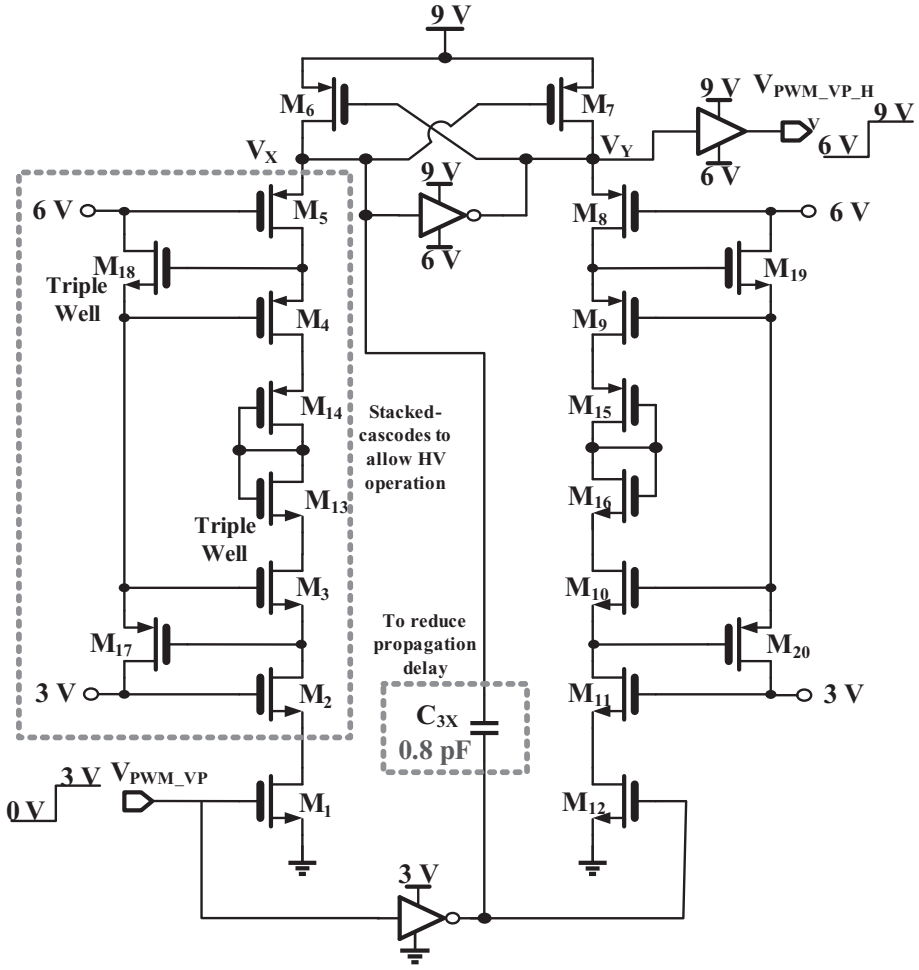

Figure 5.14: Level shifter from 3 V to 9 V schematic with floating ground.

5.5 Experimental results of CDA for PZ speakers

The proposed CDA for PZ speakers was fabricated in 0.18 μm CMOS standard technology. Fig. 5.15 shows the die micrograph of the fabricated CDA, where blocks I, II, III, and IV correspond to the integrator, hysteretic comparators, pre-driver circuits, and stacked-cascode output stage, respectively. The total active area occupied by the proposed CDA for PZ speakers is 0.4165 mm^2, where the stacked-cascode H-bridge uses 0.2571 mm^2 (61.72%) of the active silicon area.

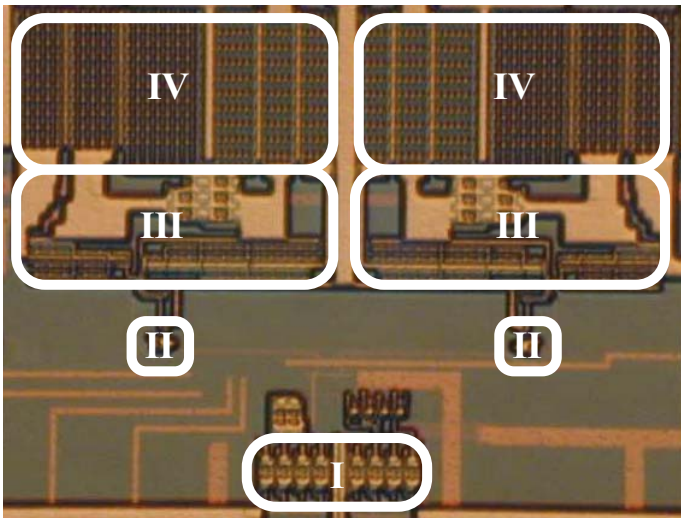

Figure 5.15: Die micrograph of CDA for PZ speakers, I integrator (0.0715 mm^2), II comparator (0.0026 mm^2), III Pre-drivers (0.0852 mm^2), and IV stacked-cascode output stage (0.2571 mm^2).

The prototype was tested with a System One Dual-Domain Audio Precision (AP) instrument as shown in Fig. 5.16. The AP instruments provide a complete solution for characterizing audio performance.

The instrument is capable to generate high audio quality output signals to apply to the device under test (DUT), and it has a signal acquisition port to capture the audio signal for processing. The setup in Fig. 5.16 allows to measure the THD+N, SNR, and output power.

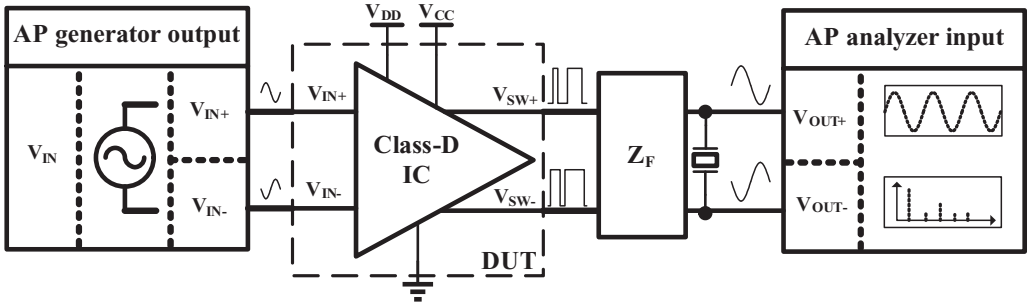

Figure 5.16: Measurement test configuration of CDA for PZ speakers.

To measure the supply current and efficiency of the amplifier, the input current, the output current, and the output voltage waveforms were monitored with an oscilloscope as shown in Fig. 5.17. The current waveforms were measured using series sensing resistors $R_s = 0.1\ \Omega$, where the voltage across them is proportional to the current, as explained in Section 3.3.5.

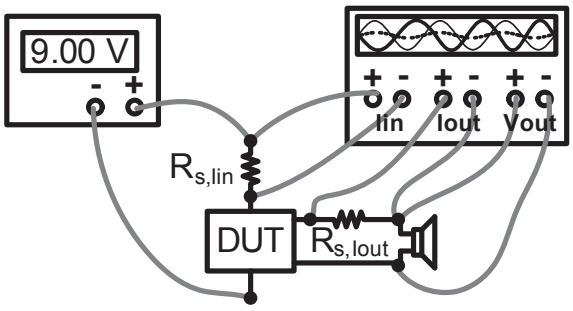

Figure 5.17: Measurement test configuration for supply and output currents.

The measured CDA supply current versus the output RMS voltage for a 1 kHz signal is shown in Fig. 5.18. The RMS value (i) represents the capacity of the CDA to process the demanded current by the PZ speaker; the RMS current is dominated by the switching frequency ripple at lower output voltages and by the PZ speaker at higher voltages.

The average current value (ii) represents the power dissipation of the system and is expected to be very low since the load is highly reactive; it was obtained by averaging the supply current waveform for several audio signal periods. The measured quiescent supply current of the proposed CDA driving the PZ speaker at idle condition (e.g. when no audio signal is present) is 0.7 mA.

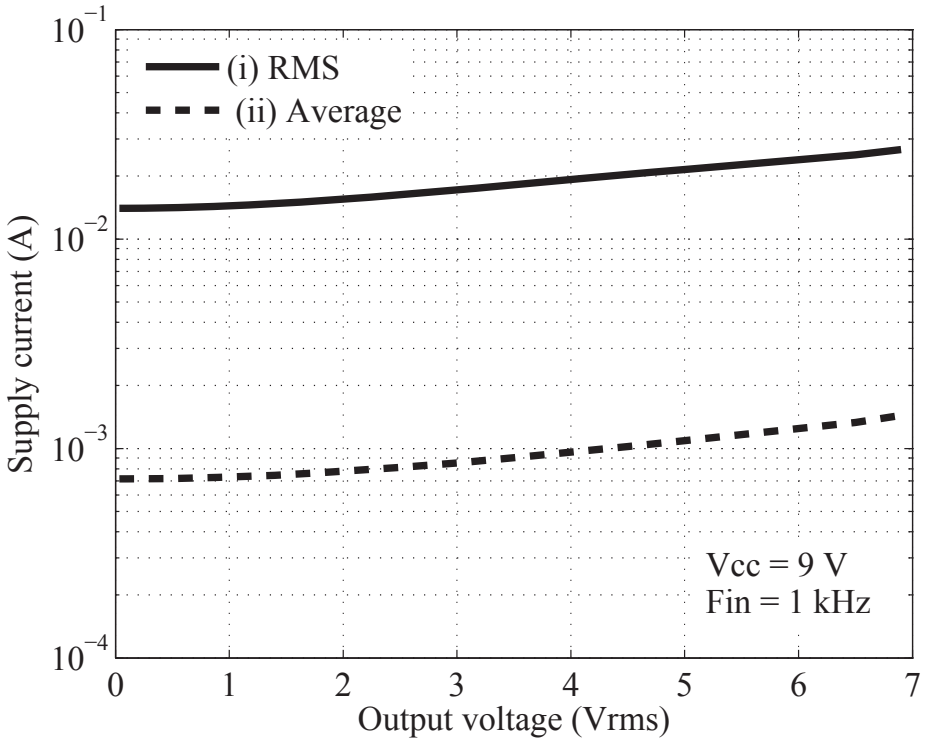

Figure 5.18: Measured supply current for CDA driving a PZ speaker.

The power-efficiency of the CDA with the PZ speaker was measured using the apparent power as described in Section II-B.1. Fig. 5.19 shows the measured efficiency versus the output RMS voltage for a 1 kHz signal, achieving a maximum efficiency of 96%.

The measured frequency spectrum of the system for an output $V_{OUT} = 18\ V_{PP}$ at 1 kHz is illustrated in Fig. 5.20, where the difference between the fundamental tone and the highest harmonic is -67 dB. High linearity is achieved with high-voltage output swing as desired for audio applications using PZ speakers. The integrated output noise from 20 Hz - 20 kHz (un-weighted) for the idle condition was obtained as 167μV.

To evaluate the impact of different reactive elements at the output filter, two Z_F implementations, (III) and (V) with $C_{PZ} = 470\ nF$, $R_F = 5.6\ \Omega$, $L_F = 47\ \mu H$, $R_B = 100\ m\Omega$, and $L_B = 1\ \mu H$ as shown in Fig. 5.3, were used for the THD+N measurement. The measured THD+N of the proposed CDA for both Z_F configurations with a 1 kHz signal is shown in Fig. 5.21.

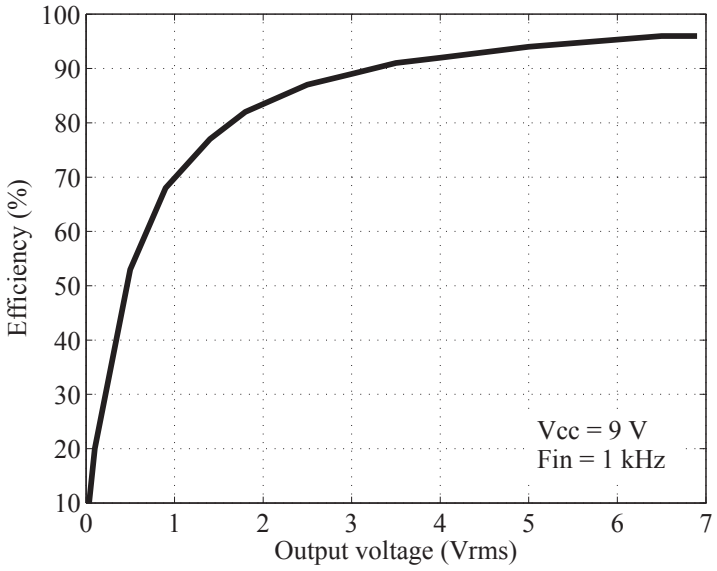

Figure 5.19: Measured power-efficiency for CDA driving a PZ speaker.

The system with the output filter (III) achieves better THD+N performance than the system with the output filter (V). The minimum measured THD+N is 0.025% and 0.1% for the CDA with Z_F configurations (III) and (V), respectively. The degradation in THD+N in filter (V) appears to be caused by the ferrite bead material due to its magnetic history curve (B-H curve) non-linear behavior, and a non-constant permeability (μ_m) that changes with the magnitude of the magnetic field and operating frequency [16]. The THD+N for the output filter (III) with a signal at 6.67 kHz is also included in Fig. 5.21 where a degradation in the THD+N can be observed due to the third harmonic distortion being dominant.

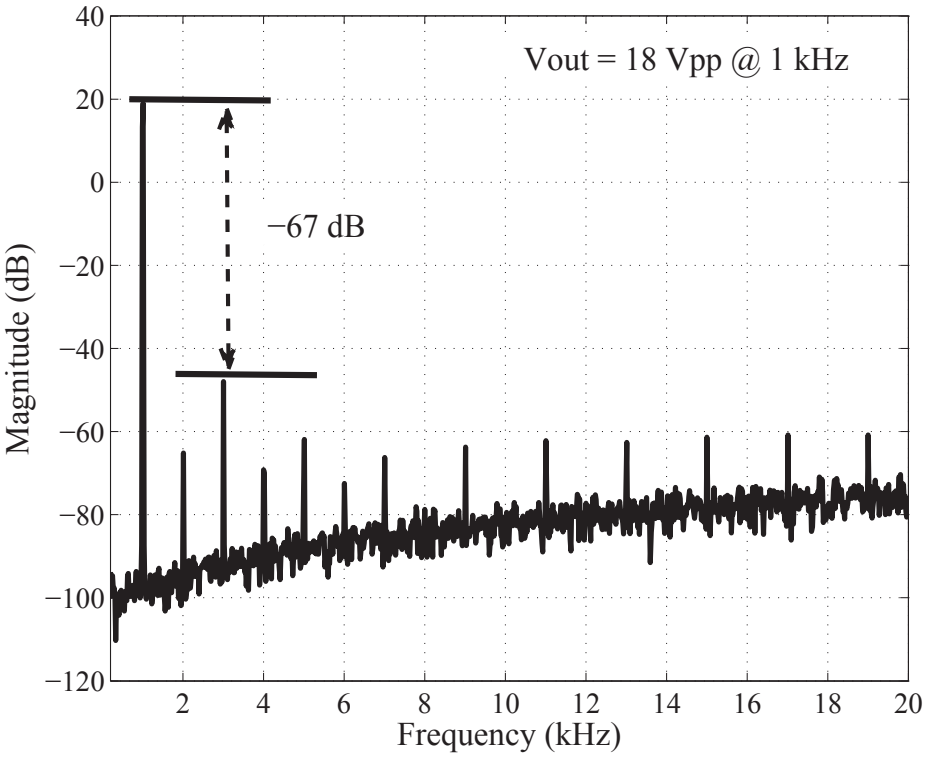

Figure 5.20: Measured frequency spectrum for 18 V_{PP} output signal at 1 kHz.

Power-supply intermodulation distortion (PS-IMD) provides a metric to evaluate the effect of the amplifier's power-supply noise when the audio signal is also present [53, 54, 58].

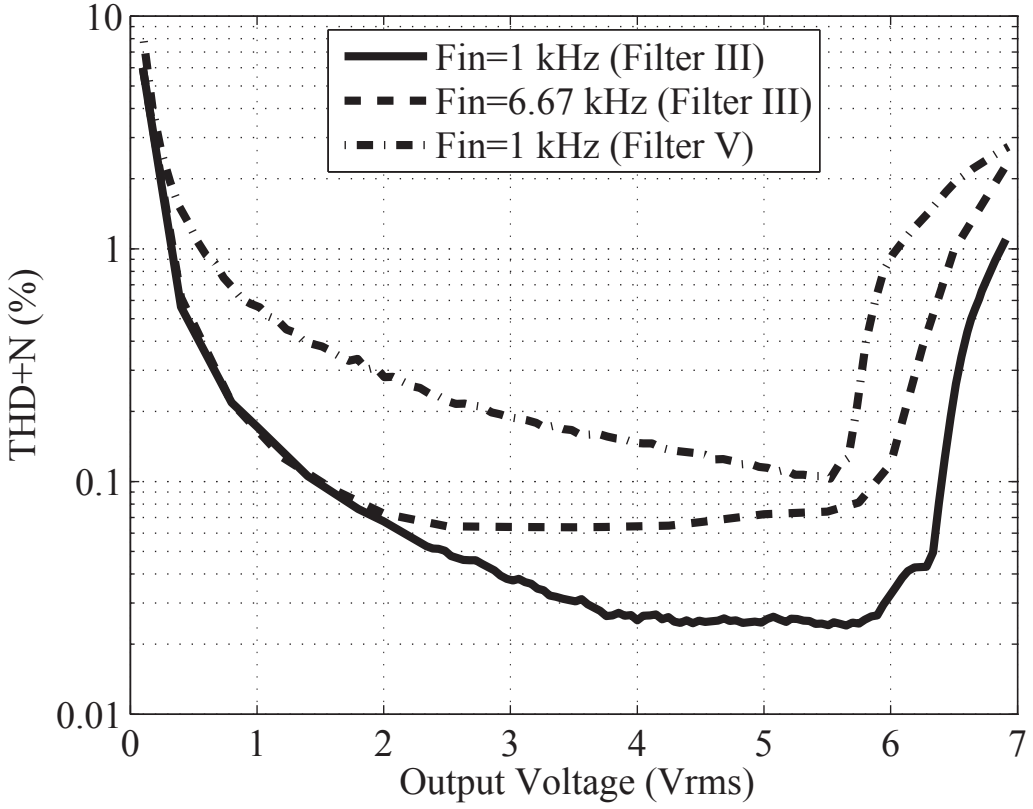

Figure 5.21: Comparison of the measured THD+N versus output voltage.

A 1 kHz sine wave with 0.5 V_{PP} was used as the input of the audio amplifier together with 0.2 V_{PP} at 217 Hz signal at the amplifier's high-voltage supply V_{CC}, as shown in Fig.5.22.

The measured frequency spectrum of the output signal is shown in Fig. 5.23. As can be seen, both intermodulation tones are at least 96 dB below the fundamental tone, showing that the high-frequency carrier helps to attenuate the IMD components as expected [53].

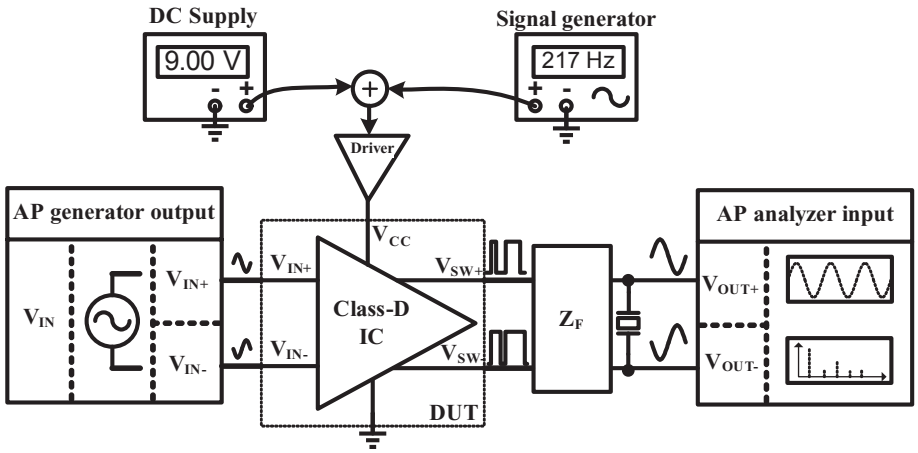

Figure 5.22: PS-IMD test bench of CDA for PZ speakers.

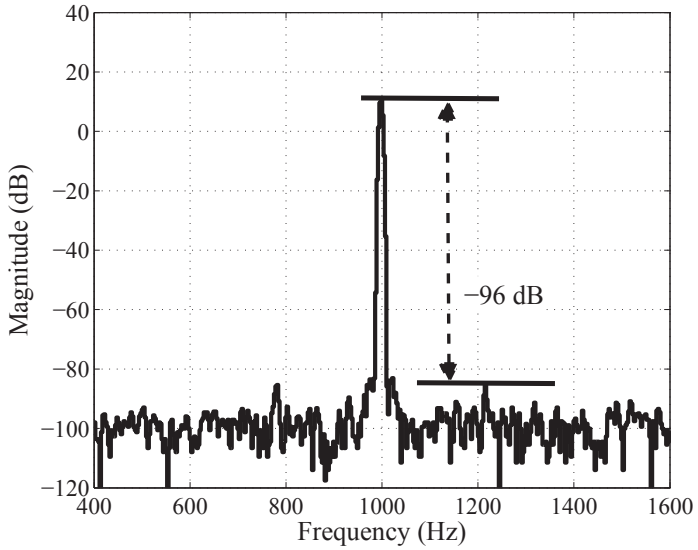

Figure 5.23: Measured PS-IMD frequency spectrum of CDA for PZ speakers.

To quantify the maximum SPL of a typical PZ speaker driven by the proposed amplifier, an 18 V_{PP} output signal at 2 kHz was used to measure the SPL. The obtained SPL was 96 dB at 10 cm, producing a comparable SPL to EM speakers but with less power consumption.

To the author's best knowledge, other CDAs for PZ speakers could not be found in the technical literature. Therefore, commercial products were used to compare the performance of the proposed CDA architecture. Table 5.2 summarizes the performance of the proposed CDA and compares it with commercial amplifiers for PZ speakers. It is evident that the proposed architecture is able to drive PZ speakers with 18 V_{PP} with higher linearity, high efficiency, and low power consumption.

5.6 Conclusion

The design tradeoffs of the CDA for driving PZ speakers were introduced, including efficiency, linearity, and EMI. A simple implementation was proposed to demonstrate the advantage of using a CDA to drive PZ speakers. The monolithic implementation used

Table 5.2: Performance comparison with audio amplifiers for PZ speakers

Parameter	This work[a]	[23]	[24]	[25]	[26]
Vout (V_{PP})	18	19	14	20	14
THD+N (%)	**0.025**	0.070	0.100	0.100	0.080
I_Q (mA)	**0.7**	4	17	13	8
P_Q (mW)	**6.3**	22	61	48	29
Efficiency(%)[b]	**96**	92	72	90	84
PSRR (dB)	90	100	65	-	77
SNR (dB)	95	94	80	80	108
F_s (kHz)	750	300	250	250	-
Amplifier class	D	D	D	D	G

[a] High-voltage supply generation not included
[b] Estimated for 1kHz signal using apparent power

stacked-cascode thick-oxide CMOS transistors at the H-bridge output stage, avoiding expensive special high-voltage semiconductor devices and making it possible to handle high voltages in a low voltage standard CMOS technology. The output stage's low input capacitance allowed high switching frequency to improve linearity with high efficiency. A self-oscillating modulation was used to obviate the need for a carrier signal generator and provide good audio performance using low quiescent power. The CDA prototype driving the PZ speaker consumed 0.7 mA of quiescent current and was capable of delivering 18 V_{PP} output amplitude with a maximum efficiency of 96%. The minimum measured THD+N was 0.025% at 5 V_{RMS}. The prototype occupies an active silicon area of 0.4165 mm^2 in standard CMOS 0.18 μm technology. Compared to other CDAs for PZ speakers, the proposed CDA achieved higher linearity, lower power consumption, and higher efficiency.

6. OPEN PROBLEMS IN CLASS-D AMPLIFIERS

The class-D amplifier in closed-loop architectures provides outstanding audio performance with high power efficiency, as discussed in Section 3. The distortion and noise can be reduced effectively using high-order compensator circuits in the close loop architecture. High power efficiency is achieved with proper design of the class-D output stage. However, there are other unwanted characteristics proper to the class-D output stage such as EMI, output filter distortion, speaker variations with temperature, the distortion of the input audio information, among others. This section evaluates the current trends and open problems in the class-D audio amplification for mobile devices.

6.1 Class-D amplifier current trends

The state-of-the-art mobile devices typically store the audio data in a digital compression format to be able to transport hours of music in a tiny device. Moreover, the complete audio processing has been implemented in the digital domain, and the output audio information of the main processor is typically a binary number with high data rate that needs to be converted to an analog signal to be applied as the input of the CDA. Thus, a high performance DAC is needed to avoid distortion of the audio analog signal.

One trend is to process the digital data and convert that to a signal compatible to the output stage. This is typically achieved using a digital PWM block, and apply this PWM signal to a close loop class-D output stage [106, 107, 108, 109, 110, 111, 112, 113, 114]. The advantage is that the high performance DAC is avoided, and the class-D output stage is in a close loop architecture, increasing its performance. Also, calibration and self-correction schemes can be implemented in the digital domain. The main drawback is that a more complex and power hungry digital signal processor (DSP) is needed.

Another trend is to decrease the number of external parts required for the CDA, especially of the output filter. This is mainly important since the footprint of the inductor limits the amount of PCB reduction, and its cost increase the bill of materials. The main goal is to reduce the power of the carrier signal such that the inherent filtering of the speaker could recover the audio signal since the human ear is not capable of perceiving the carrier signal. A fully-differential CDA architecture implementing the filterless switching strategy at the output stage, as discussed in Section 3.3.3, is typically used to reduce the size of the output filter or completely remove it, at the expense of decreased audio performance [3, 5, 42, 109].

The filterless output stage lessens the impact of the carrier signal at the speaker, allowing a reduction of the output filter size. However, the EMI at the switching output is still present in the cables and PCB traces. Careful layout in the PCB board could help to decrease the EMI in the surrounding circuits, but still is dominant. Thus, a current trend is to include modulation techniques to improve the EMI that can be used to spread the energy of the high-frequency carrier signal, at the expense of additional power consumption and design complexity [45, 46, 92, 114, 115], and affect the linearity of the output stage. The THD+N and EMI tradeoff is still limiting the use of the CDA as a headphone amplifier where a long cable is used from the amplifier to the speaker. Also, most headphone amplifiers are single-ended, and a differential filterless output stage is too complex and expensive for an application that does not require high output power.

The consumer's demand for louder mobile devices is driving the CDA designers to provide more output power to the loudspeaker. To accomplish this from a battery-powered device, a voltage step-up circuit is needed to boost the voltage.

The main drawback is that the efficiency of the step-up circuit directly affects the efficiency of the overall audio system since its power consumption would reduce the battery life. Also, most of the conventional step-up circuits require external components, increasing the cost of the device [20, 21, 22, 92]. Thus, high efficiency step-up circuits that can be integrated on the same die as the CDA are highly desirable.

6.2 Audio CODEC integration

The audio recording and reproduction in a typical mobile device is usually managed by the main processor. However, as more multimedia functions and interface devices are integrated in state-of-the-art mobile devices, the main processor is heavily loaded with functions that would require a high amount of power to handle along the audio processing.

The audio CODEC, which stands for compressor-decompressor, is typically used as a separate audio processor that is dedicated to handle all the functions related to audio. It includes all the necessary interfaces to record audio using a microphone, and to reproduce sound for headphones and loudspeaker.

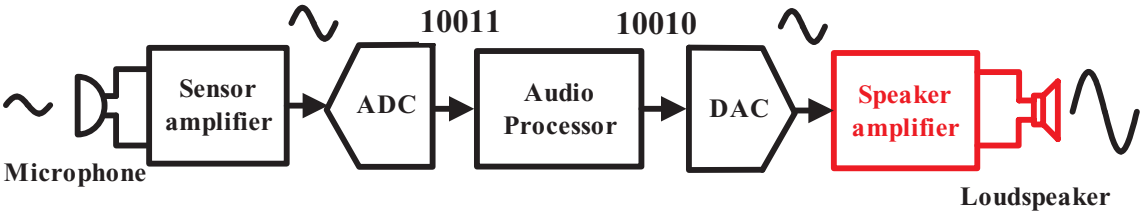

Figure 6.1: Typical audio CODEC block diagram.

The key design blocks in an audio CODEC are the ADC and DAC blocks which interface the audio DSP with the microphone or speakers, as shown in Fig. 6.1.

The main goal is to integrate as many functions as possible with high performance and low power [116, 117, 118]. The typical input resolution for the microphone ADC is 16-bit with a sampling rate of 48 kHz. The desired SNR for the microphone amplifier circuit is 90 dB to be able to perceive very small sounds.

The preferred ADC and DAC architecture in integrated audio CODEC circuits is the sigma delta ($\Sigma\Delta$). The low frequency bandwidth of the audio signals (20 kHz) allows a high OSR which combined with a high order compensator would provide high SNR, as discussed in Section 3.2.2. The main drawback is that CMOS technology scaling is continuously degrading the performance of analog circuits, and lowering the voltage supply to less than 1 V. Thus, to achieve high resolution in the analog-digital conversion when the full dynamic range is less than 1 V, complex compensation techniques are needed as well as high power consumption in the circuits.

One alternative that benefits from the improved timing resolution of small CMOS technology nodes is to perform the analog to digital conversion in time domain. The comparison with traditional voltage/current domain ADC is illustrated in Fig. 6.2. The time domain ADC involves mapping the voltage domain audio signal to a pulse encoded signal where the duty cycle is proportional to the voltage input signal level, as in PWM. Then, the pulse signal is converter to a digital output using a time-to-digital converter (TDC).

The main advantage of using a time domain ADC is that it can achieve high resolution limited only by the smallest delay of the technology. In other words, its resolution would be limited by the accuracy of the voltage-to-time conversion, and the smallest time step that the technology can provide which is typically a couple of inverters. For example, for an 1 kHz audio signal modulated by a carrier at 10 MHz or 100 ns period, and a TDC with time resolution of 100 ps, the output would have 1000 digital levels or the equivalent to a 9.5 bits ADC; if the TDC has a finer time resolution, then the number of bits would increase as well.

It is important to notice that this example is considering an open loop ideal quantization which will be affected by timing errors and supply variations. However, if the whole time-domain converter (PWM+TDC) is included in a close loop architecture, the negative feedback would correct for any error or distortion that would result in an effective resolution of more than 20 bits.

Most of the techniques developed for the CDA to correct for timing variations and to reduce noise or distortion, can be applied to a time-domain ADC. This is important since audio CODEC with the same strategies in the audio input path as the output path would simplify drastically the design and time to market of this important block for mobile devices.

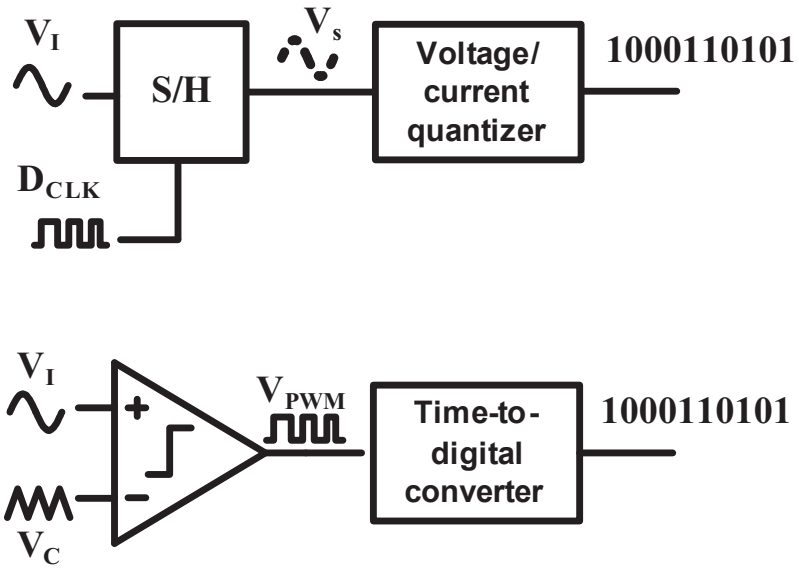

Figure 6.2: Comparison between voltage/current ADC and time-domain TDC.

7. SUMMARY

This dissertation presented new architectures and design techniques focused on the design of high efficiency class-D amplifiers to achieve high performance audio amplifiers while consuming low power and silicon area. The first part of the dissertation discussed the research motivation, and presented a concise explanation of the fundamentals of audio amplification, including the loudspeaker's operation and tradeoffs as well as the main audio performance metrics. Moreover, the operating principle and design procedure of class-D audio amplifiers were discussed to provide a broad view of the tradeoffs involved in the design. The main close loop architectures with different modulation techniques were considered as well as the involved circuits.

The second part of the dissertation presented two solutions to achieve low power high efficiency class-D audio amplifiers for battery-powered mobile devices. The first work introduced a feed-forward cancellation technique for single-ended class-D audio amplifier architectures to improve the power-supply rejection ratio across the entire audio frequency range. The design methodology, implementation, and tradeoffs of the proposed technique were clearly delineated to demonstrate its simplicity and effectiveness. A first-order single-ended PWM class-D audio amplifier was fabricated to demonstrate the effectiveness of the proposed technique. The class-D amplifier prototype achieves a PSRR of 83 dB at 217 Hz, a THD+N of 0.0149%, and a maximum efficiency of 94.6%. The proposed technique enhances the prototype's PSRR by 33 dB across the entire audio bandwidth compared with a conventional class-D amplifier without it. The class-D audio amplifier prototype was implemented using 0.18 μm CMOS standard technology and occupies a total area of 0.121 mm^2. It consumes a total of 356 μW of quiescent power.

The second work focused on the design of a class-D audio amplifier for piezoelec-

tric speakers. The design tradeoffs of the class-D audio amplifier for driving piezo-electric speakers were introduced, including efficiency, linearity, and electromagnetic interference. A monolithic implementation was proposed using stacked-cascode thick-oxide CMOS transistors at the H-bridge output stage, avoiding expensive special high-voltage semiconductor devices, and making it possible to handle high voltages in a low voltage standard CMOS technology. The amplifier prototype driving the piezoelectric speaker consumed 0.7 mA of quiescent current and was capable of delivering 18 V_{PP} output amplitude with a maximum efficiency of 96%. The minimum measured THD+N was 0.025% at 5 V_{RMS}. The prototype occupies an active silicon area of 0.4165 mm^2 in standard CMOS 0.18 μm technology. Compared to other solutions for piezoelectric speakers, the proposed class-D architecture achieved higher linearity, lower power consumption, and higher efficiency.

Finally, the open problems in audio amplification for mobile devices were discussed to delineate the possible future work to improve the performance of class-D amplifiers. For all the presented works, proof-of-concept prototypes were fabricated, and the measured results were used to verify the correct operation of the proposed solutions. Appendix A was included to briefly detail the operation of a class-G amplifier with a proposed solution to increase the linearity of the amplifier during supply transitions with low power consumption. Appendix B presented more details for a non-linear controller used in the class-D amplifier to achieve high PSRR using integral sliding mode control.

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APPENDIX A

CLASS-G AMPLIFIER CASE STUDY

Despite their good power-efficiency, class-D amplifiers are not often preferred as headphone drivers due to their EMI concerns in single-ended architectures [44, 58]. Moreover, the radiated EMI prohibits the use of the audio cable as an antenna for FM radio. This makes the linear amplifier classes (A/AB) preferable for headphone drivers despite their high quiescent power consumption [34, 35].

As discussed in Section 2, the class-G amplifier provides better power efficiency compared with class-AB amplifiers. The efficiency improvement is achieved by reducing the supply voltage for smaller output signals, and thus, reducing the quiescent power consumption. Moreover, the power-supply transition is achieved without affecting the dynamic range of the output signal. The main challenge is to ensure minimal or no additional distortion when the switching between the power-supply levels occurs.

In this appendix, a class-G headphone amplifier comprised by the parallel connection of a class-AB amplifier operating from lower supplies (V_{DDL}/V_{SSL}), and a class-C amplifier operating from higher supplies (V_{DDH}/V_{SSH}), with a crossover region between V_{DDL} and V_{SSL} is presented. Moreover, the proposed parallel class-G output stage has a gradual power-supply transition to achieve low distortion during the supply switching.

A.1 Class-G amplification background

The class-G implementation can be classified broadly into three approaches: (1) series output stages, (2) single output stage with power management block to switch the supply, and (3) parallel output stages.

The mainstream existing solution is the series approach which is based on the basic

class-AB source (emitter) follower configuration, and has the drawbacks of low voltage swing and very poor efficiency [36]; both due to the substantial $V_{GS(BE)}$ drop in comparison to the small supply voltages used in multimedia portable devices.

The second approach to class-G implementation uses a power management block for supply switching [38]. A single output driver is used and whenever the signal crosses the threshold of the smaller supply a power management block switches its rail to a higher level and makes it stay there for a minimum amount of time. A drawback for this implementation is the delay between the output signal crossing the supply threshold and the power management circuit reacting with rail switching. One way to overcome the delay in this supply transition is to delay the input signal in digital domain and switch the supply predicting the next signal level. However, the slow response time and the transient glitches in the power management block can create distortion during the supply switching. Thus, degrading the efficiency since the supply rail has to be held high for a minimum amount of time, which is always longer than needed.

The third approach uses two different parallel output stages that are active one at a time for certain amount of the output signal level. The class-G implementation in [37] realizes the supply switching by forcefully turning on/off the parallel output stages with an external circuit. The impact of this hard switching is added distortion during the supply transition. Also, the parallel paths to the output stages require separate compensation and hence doubles the total compensation capacitance compared to the equivalent class-AB, increasing the cost for the solution.

Recent CMOS class-G audio amplifiers reported in the literature [37, 38] exhibit linearity degradation during the power-supply switching. Thus, a parallel implementation for a class-G output stage with gradual switching between the power-supplies is proposed to achieve very low distortion during the supply transition.

A.2 Proposed class-G implementation

Leveraging the understanding between the output stage operating mode and the bias condition, as discussed in Section 2, the proposed class-G amplifier is composed by the parallel connection of a class-AB amplifier operating from lower supplies (V_{DDL}/V_{SSL}), and a class-C amplifier operating from higher supplies (V_{DDH}/V_{SSH}), with a crossover region between V_{DDL} and V_{SSL}. This is illustrated in the block diagram of the proposed class-G amplifier in Fig. A.1, where a gain stage is used to amplify the signal, a biasing block ensures that each output stage in the parallel configuration is active during the correct output signal levels to achieve a class-G operation, and the two parallel output stages are used to drive the load.

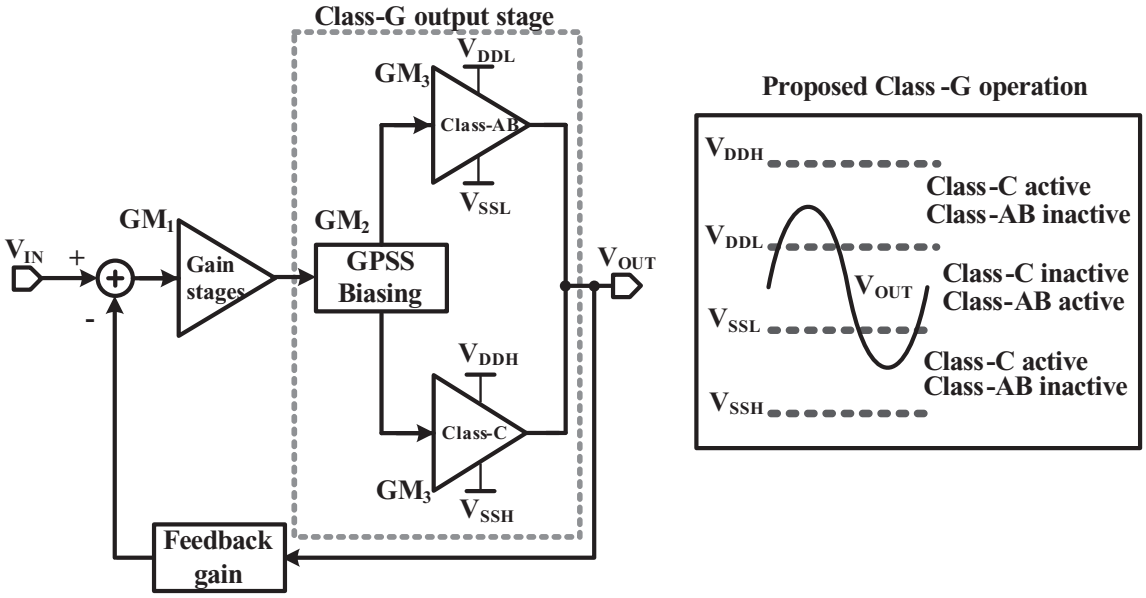

Figure A.1: Proposed class-G amplifier diagram and operation.

To ensure low distortion during the power-supply transition and suitable class-G operation in the parallel output stage, a gradual power-supply switching (GPSS) biasing circuit is proposed as shown in Fig. A.2. M_{P1} and M_{N1} are the class-AB driver transistors operating from the lower supply, and M_{P2} and M_{N2} are the class-C driver transistors operating from the higher supply.

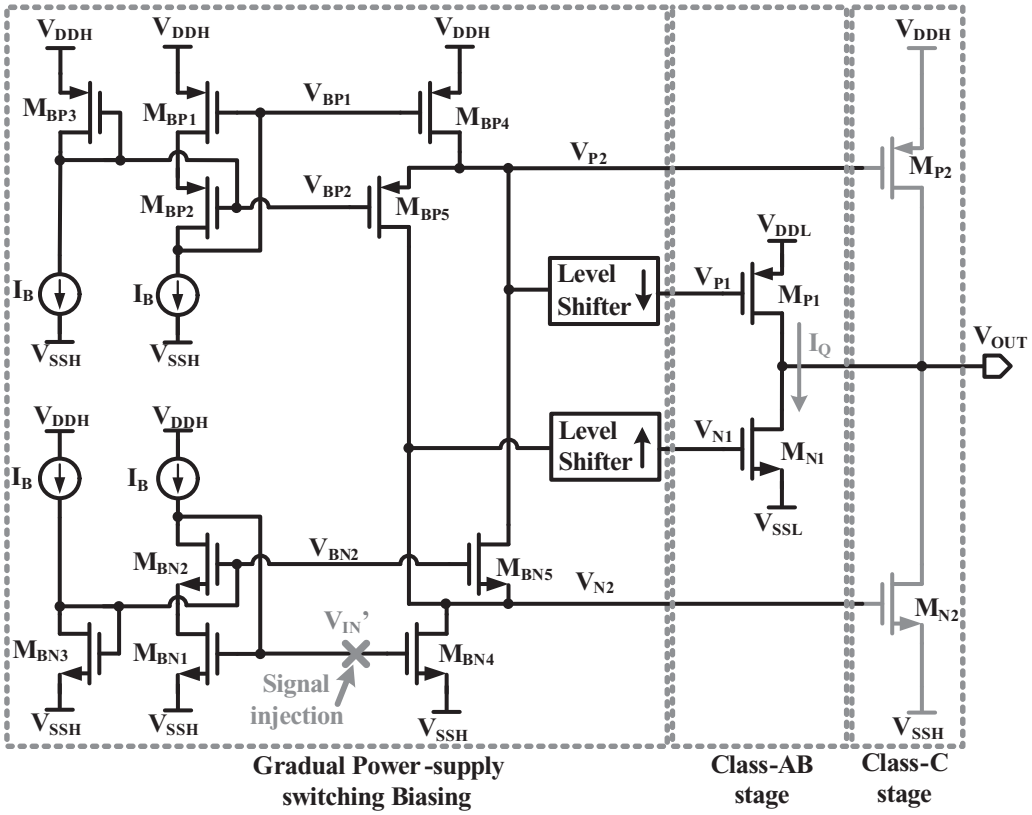

Figure A.2: GPSS biasing circuit at quiescent condition.

The GPSS circuit at quiescent conditions is under proper matched conditions when $V_{GS,M_{N2}} \cong (1 \sim 2)V_{DSAT,M_{BN4}}$ and $V_{GS,M_{P2}} \cong (1 \sim 2)V_{DSAT,M_{BP4}}$. This selection will place the class-C stage in the crossover region during the quiescent condition $V_{OUT} \cong V_{IN} \cong 0\,V$.

Even after accounting for the channel length modulation, drain induced barrier lowering (DIBL) and other process variations, the quiescent current (I_Q) in the output stage is set to a reasonable accuracy. The I_Q variations will be influenced by the smaller supply variation and threshold voltage (V_{TH}) variation of the level shifter circuit. This effect can be minimized by increasing the V_{DSAT} of M_{P1} and M_{N1}.

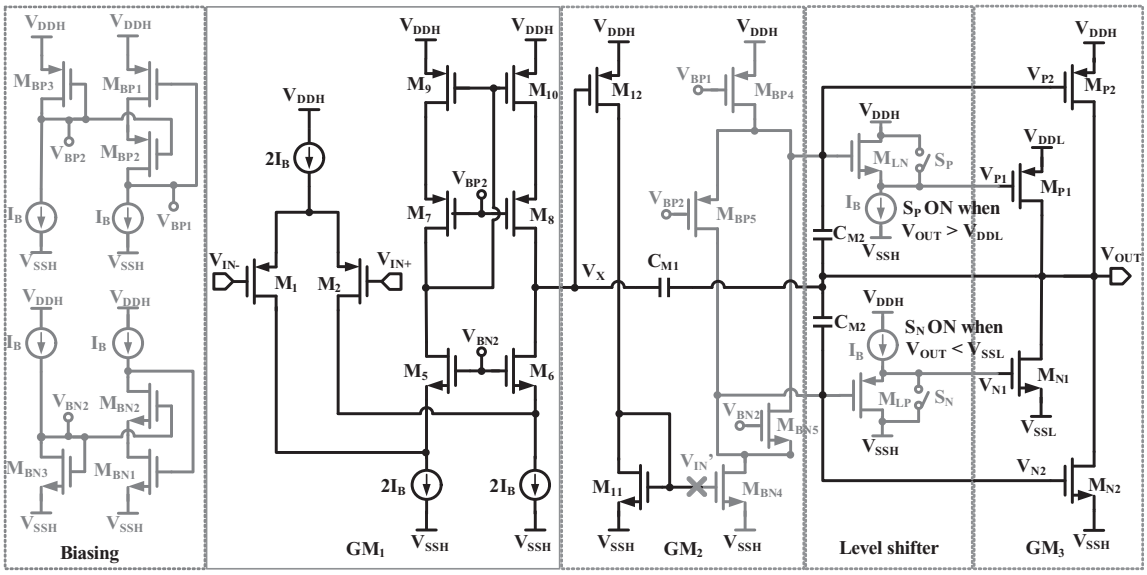

Figure A.3: Proposed class-G audio amplifier schematic with GPSS biasing.

The schematic diagram of the proposed class-G amplifier is shown in Fig. A.3, where the first stage (GM_1) is a folded cascode architecture with PMOS input pair, GM_2 is the second stage comprised by the GPSS bias branch which is made a positive g_m stage for compensation purposes, and the third stage (GM_3) is the class-G output driver where M_{P1} and M_{N1} comprise the class-AB output stage, and M_{P2} and M_{N2} operate as the class-C output stage.

Transistors M_{LN} and M_{LP} comprise the level shifters; their V_{GS} values are selected such that M_{P2} and M_{N2} operate as a class-C output stage in the crossover region for the quiescent state. The switches S_P and S_N are required only to avoid reverse conduction in M_{P1} and M_{N1} from V_{OUT} to V_{DDL} when $V_{OUT} > V_{DDL}$, and from V_{SSL} to V_{OUT} when $V_{OUT} < V_{SSL}$.

V_{OUT} Condition	Active Device	GM_3
$0 < V_{OUT} < V_{DDL}-V_{DSAT}$	M_{P1}	gm_{P1}
$V_{DDL}-V_{DSAT} < V_{OUT} < V_{DDL}$	M_{P1} and M_{P2}	$gm_{P1}+gm_{P2}$
$V_{OUT} > V_{DDL}$	M_{P2}	gm_{P2}
$V_{OUT} = 0$	M_{P1} and M_{N1}	$gm_{P1}+gm_{N1}$
$0 > V_{OUT} > V_{SSL}+V_{DSAT}$	M_{N1}	gm_{N1}
$V_{SSL}+V_{DSAT} > V_{OUT} > V_{SSL}$	M_{N1} and M_{N2}	$gm_{N1}+ gm_{N2}$
$V_{OUT} < V_{SSL}$	M_{N2}	gm_{N2}

Figure A.4: Class-G output stage operation across the output voltage swing.

As the input voltage increases, M_{P1} pulls up the output and the negative feedback ensures V_{OUT} equals to V_{IN}. During this phase, M_{P2} is off and V_{P2} changes very little as long as M_{P1} is in saturation. When V_{OUT} starts getting close to V_{DDL}, M_{P1} starts to enter the triode region reducing the loop gain. At this instant, the node voltages V_{P2} and its level shifted version V_{P1} start dropping. If the level shift voltage is chosen adequately, the change in V_{P2} should slowly make M_{P2} start conducting. Both M_{P1} and M_{P2} will conduct when $V_{DDL} - V_{DSAT} < V_{OUT} < V_{DDL}$, and eventually, M_{P2} will be in the saturation region and M_{P1} will be forced to turn off when $V_{OUT} > V_{DDL}$. The same gradual switching occurs when the input goes downwards from zero to V_{SSH}. The proposed class-G operation and its equivalent transconductance (GM_3) is summarized in Fig. A.4 for different V_{OUT} conditions.

Throughout the output signal level, the proposed GPSS circuit allows a gradual transition between the parallel class-AB and class-C output stages. In addition, as long as the loop has large gain and remains stable, the negative feedback helps to attenuate the supply transition distortion.

A.3 Class-G design tradeoffs

The level shifter circuits in Fig. A.3 should satisfy two conditions: (1) At the quiescent state, V_{P2} and V_{N2} should bias the class-C stage (M_{P2} and M_{N2}) in the cut-off region, and V_{P1} and V_{N1} should ensure that M_{P1} and M_{N1} conduct the desired quiescent current; (2) When M_{P1} and M_{N1} enter the triode region, the level shift voltage should be enough to put M_{P2} and M_{N2} in the saturation region.

A level shift voltage (V_{LS}) that is too large will put the class-C stage (M_{P2} and M_{N2}) deeply into cut-off such that it will need a large change in V_{P2} and V_{N2} to bring transistors M_{P2} and M_{N2} into the conduction state; thus, it will force M_{P1} and M_{N1} into deep triode degrading the loop gain severely, and increasing distortion during the supply transition. A V_{LS} that is too small will not completely turn off transistors M_{P2} and M_{N2}, increasing the quiescent power consumption and degrading the instantaneous efficiency. A $V_{LS} = 650\,mV$ was chosen as a compromise of these tradeoffs.

The V_{DSAT} of the class-AB stage, M_{P1} and M_{N1}, impacts the instantaneous efficiency at small to moderate output signal levels. Fig. A.5 shows the class-G instantaneous efficiency curves assuming $V_{DDL} = 0.5\ V$ and $V_{DDH} = 1\ V$ for two cases: (1) an ideal $V_{DSAT} = 0\ V$ and (2) a non-ideal $V_{DSAT} = 150\,mV$.

The class-G peak instantaneous efficiency, considering only the effect of V_{DSAT}, can be expressed as

$$\eta_{pk,V_{DSAT}} \cong \frac{V_{DDL} - V_{DSAT}}{V_{DDL}}. \tag{A.1}$$

It can be observed, that in the ideal case ($V_{DSAT} = 0\ V$), the class-G peak instantaneous efficiency could reach 100% at $V_{IN} = V_{DDL}$, whereas in the non-ideal case ($V_{DSAT} = 150\ mV$), the peak efficiency only could reach 70%.

For a class-AB stage with output transistors having a $V_{DSAT} \neq 0$, the intermediate peak in instantaneous efficiency curve increases with the smaller supply value, whereas the instantaneous efficiencies (slope) at smaller signal levels decrease at the same time, as expressed in (A.1). This can be observed in Fig. A.6 for several smaller supply values with a $V_{DSAT} = 150\ mV$.

If the value of the smaller supply V_{DDL}/V_{SSL} is too low, V_{DSAT} impacts heavily since the output signal switches to the higher supply more frequently which impacts the overall efficiency. On the other hand, if V_{DDL}/V_{SSL} value is too high, its value impacts the instantaneous efficiency at smaller output signal levels.

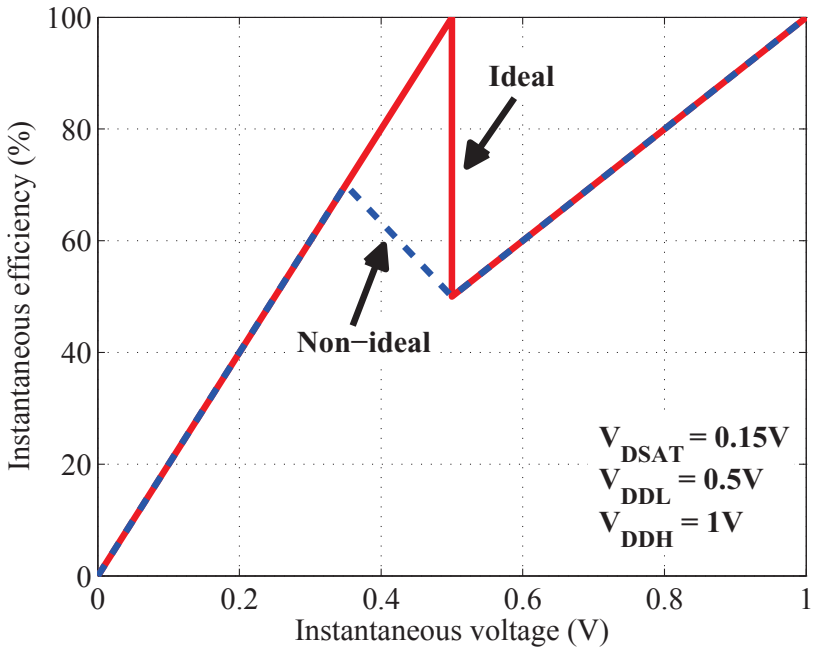

Figure A.5: Effect of V_{DSAT} of class-AB transistors on the class-G efficiency.

For audio signals with crest factors in the range of 12-20 dB, the smaller supply choice should be 25-45% of the higher supply to maximize efficiency [36]. However, this approximation does not include the impact of V_{DSAT}. Assuming a $V_{DSAT} = 150\ mV$, the smaller supplies should be about 35-60% of the higher supply. Other parameters that affect the maximum efficiency achieved for certain value of smaller supplies are the V_{TH} of the devices, quiescent power, V_{DSAT}, and V_{DDH}. In this work, the value for the smaller supplies was chosen to be 50% of the higher supplies as a compromise between these tradeoffs.

In the class-G amplifier, the major sources of non-linearity are: (1) the crossover distortion arising from three points of V_{OUT} ($V_{OUT} = -V_{SSL}$, $V_{OUT} \cong 0$, and $V_{OUT} = V_{DDL}$), and (2) the triode non-linearity when the output signal is close to the large supply rails (V_{DDH}/V_{SSH}). The distortion at zero crossing is minimized by increasing the quiescent current in the class-AB drivers.

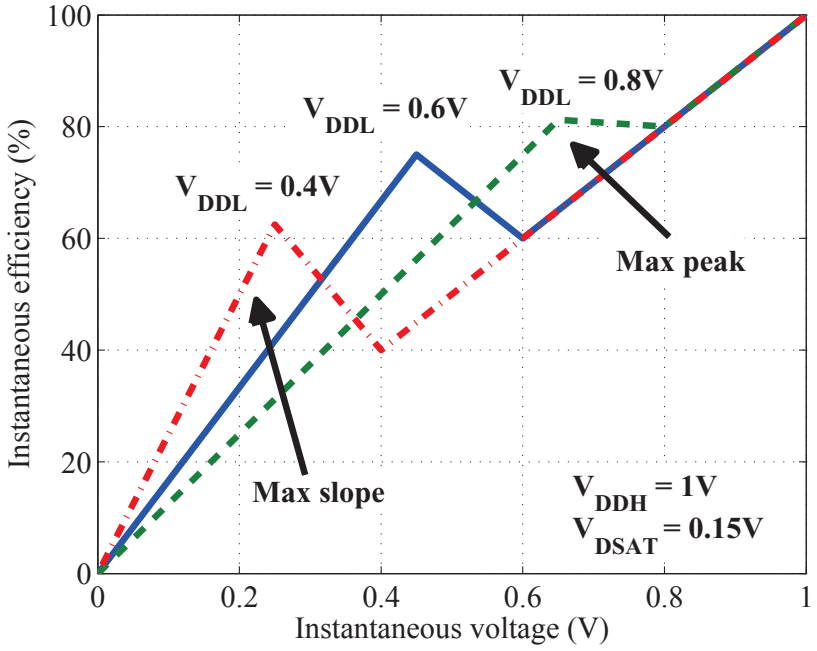

Figure A.6: Effect of smaller supply (V_{DDL}) choice on the class-G efficiency.

The distortion at V_{DDL}/V_{SSL} crossing is minimized by biasing the class-C drivers such that they start delivering a portion of the load current when the class-AB drivers reach triode region. The triode non-linearity is left as a trade-off for smaller die area as it only occurs when the output signal is too large.

To minimize errors in the output signal, negative feedback is used as shown in Fig. A.1. As long as the loop is stable and the open loop gain across the audio frequency bandwidth is large enough, then all the non-linearity of the output stage is suppressed by the loop gain. It can be noted that increasing the loop gain allows reducing the crossover and the triode non-linearities.

The amplifier was designed to drive a wide load range of $R_L = 16$ to 32 Ω and $C_L =$ 10 pF to 1 nF. The amplifier is stabilized using nested Miller compensation (NMC) due to its simplicity [80]. However, if the amplifier needs to drive larger capacitive loads for a different application, a more advanced compensation can be used as detailed in [82, 81]. The main difference between the proposed class-G amplifier and any three stage amplifier in terms of compensation, is that the output stage GM_3 (as shown in Fig. A.3) changes its value depending on the output voltage as defined in Fig. A.4.

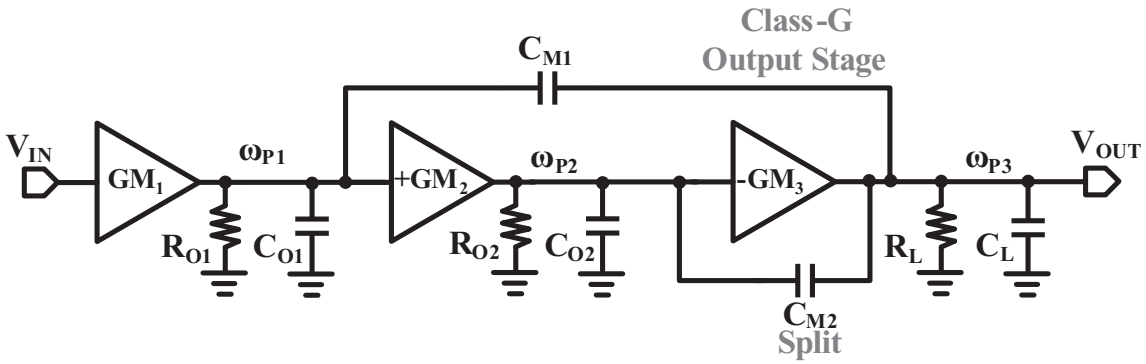

Figure A.7: Proposed class-G audio amplifier small-signal block diagram.

The small signal diagram for the proposed class-G amplifier is depicted in Fig. A.7. Parameters GM and R_O are the stage transconductance and output resistance, respectively. Capacitors C_O represent the equivalent capacitance at the output of each amplification stage, and R_L and C_L are the load resistance and capacitance, respectively.

The open-loop transfer function of the class-G amplifier with NMC can be expressed as,

$$\frac{V_{OUT}}{V_{IN}} \cong \frac{-A_{DC}}{1+\dfrac{s}{\omega_{p1}}} \left(\frac{1 - s\dfrac{C_{M2}}{GM_3} - s^2 \dfrac{C_{M1}C_{M2}}{GM_2GM_3}}{1 + s\dfrac{C_{M2}}{GM_2} + s^2 \dfrac{C_L C_{M2}}{GM_2GM_3}} \right) \tag{A.2}$$

provided that $GM_1 \gg 1/R_{O1}, 1/R_{O2}$, $GM_3 \gg GM_2$, and $C_{M1}, C_{M2}, C_L \gg C_{O1}, C_{O2}$; where $A_{DC} = GM_1GM_2GM_3R_{O1}R_{O2}R_L$ is the low frequency gain, and the dominant pole of the system is $\omega_{p1} \cong GM_1/(A_{DC}C_{M1})$.

It can be noted from the numerator in (A.2) that the system has a right-half plane (RHP) zero that needs to be considered to avoid degradation in the stability of the system. If the RHP zero, given by the terms G_{M2}/C_{M1} and G_{M3}/C_{M2}, is placed well above the GBW of the system, its impact on the stability will be minimized. Also, to avoid the poles in the denominator of (A.2) to be complex conjugate and degrade the phase response, GM_3 needs to satisfy the minimum value of

$$GM_3 > 4C_L \frac{GM_2}{C_{M2}}. \tag{A.3}$$

Then, the GBW and high frequency poles of the system can be approximated as,

$$GBW \approx G_{M1}/C_{M1}; \quad \omega_{p2} \approx G_{M2}/C_{M2}; \quad \omega_{p3} \approx G_{M3}/C_L. \tag{A.4}$$

where for the stability condition of a phase margin of 60^o [81] can be expressed as,

$$2GBW \leq \omega_{p2} \leq \frac{1}{2}\omega_{p3}. \tag{A.5}$$

From a typical corner simulation, the composite GM_3 as defined in Fig. A.4 took values approximately in the range of 60 mS to 200 mS. The implemented class-G amplifier used $C_{M1} = 8\ pF$, $C_{M2} = 16\ pF$, $GM_1 = g_{m1} = 50\ \mu S$, and $GM_2 = g_{m12}(g_{m16}/g_{m11}) = 200\ \mu S$. The Miller capacitor C_{M2} across GM_3 stage has to be split into two parts to compensate when the P-side (M_{P1} or M_{P2}) is active or the N-side (M_{N1} or M_{N2}) is active.

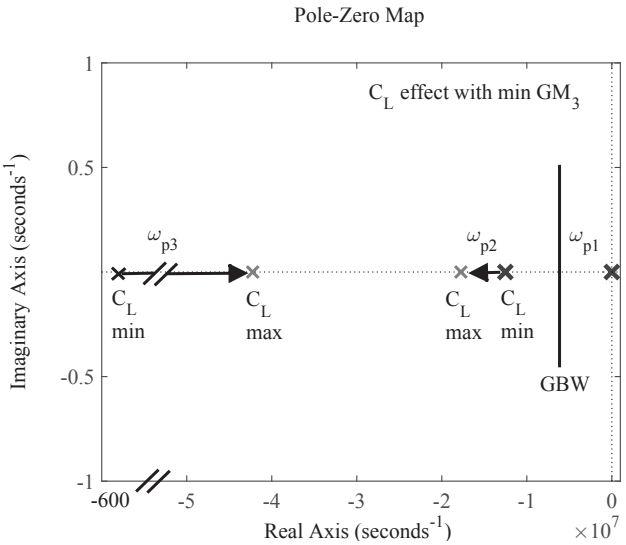

Figure A.8: Pole-zero map when load capacitance changes from 10 pF (C_L min) to 1 nF (C_L max).

Fig. A.8 show the pole-zero map of the system for $C_L = 10\ pF,\ 1\ nF$ with the minimum GM_3 condition and its effect on the non-dominant poles. It can be observed that the high frequency poles were placed such that the poles ω_{p2} and ω_{p3} won't become complex and are located at frequencies higher than the GBW of the system. Fig. A.9 shows the pole-zero map of the system to show the effect of the GM_3 variation of the proposed class-G amplifier with the maximum $C_L = 1\ nF$ condition. It can be noticed that the GM_3 variation only affects the RHP zero (ω_z) and ω_{p3} that are located at high frequencies well above the GBW to avoid their effect on the stability.

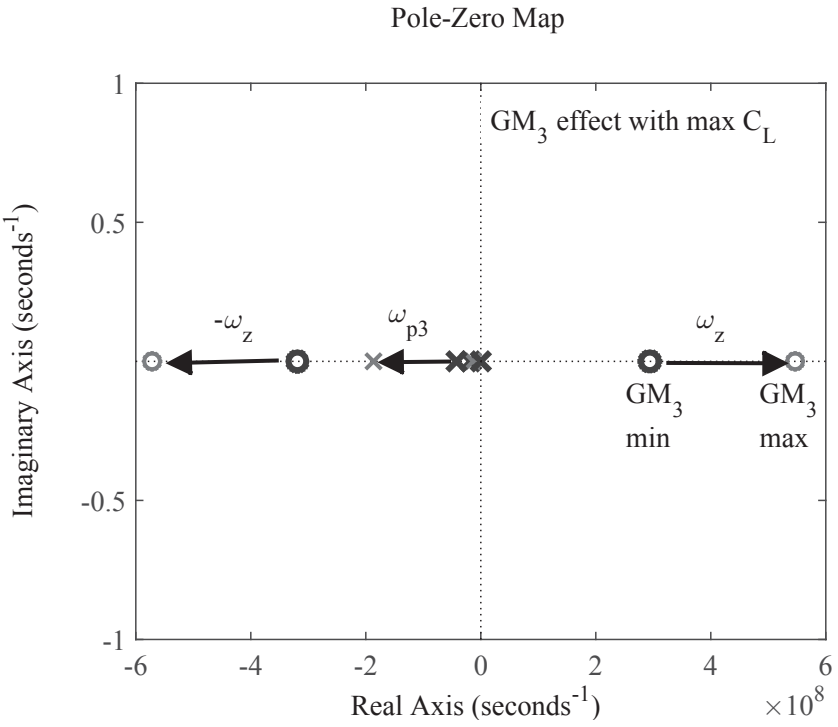

Figure A.9: Pole-zero map when output transconductance changes from class-AB (GM_3 min) to class-C (GM_3 max) operation.

The simulation results are summarized in Fig. A.10 for different loading conditions where the phase margin under these parameter variations is acceptable.

Parameter	Condition	GBW	f_{p2}	f_{p3}	$f_{z,RHP}$	Phase Margin
$C_{L,MAX}$ = 1nF	$G_{M3,MIN}$ = 60mS	1 MHz	2 MHz	9.5 MHz	48.7 MHz	60°
$C_{L,MIN}$ = 10pF				954 MHz	48.7 MHz	65°
$G_{M3,MAX}$ = 200mS	$C_{L,MAX}$ = 1nF			31.8 MHz	88.9 MHz	63°

Figure A.10: Stability and pole location for different output load conditions.

A.4 Experimental results of proposed class-G amplifier

The proposed class-G topology has been designed and fabricated in 90 nm standard CMOS technology to drive an equivalent load $R_L = 16 - 32\ \Omega$ and $C_L = 10 - 1000\ pF$. Nonetheless, the experimental test setup was performed with 32 Ω and 200 pF loading to emulate a typical headphone speaker. Testing was done using Audio Precision's (AP) System One Dual-domain equipment. The power supply selection is $V_{DDH}/V_{SSH} = \pm 1\ V$, and $V_{DDL}/V_{SSL} = \pm 0.5\ V$. The prototype die micrograph and the quiescent power consumption distribution are shown in Fig. A.11 and Fig. A.12, respectively.

Considering reliability in 90nm technology, the complete design is made using thick oxide 2.5 V I/O transistors. The gain stages and GPSS biasing circuit consume 70 μA from $\pm 1\ V$ supply, and the class-AB stage sinks an I_Q of 200 μA from the $\pm 0.5\ V$ supply. An un-weighted SNR of 89 dB was measured and a minimum THD+N of -82.5 dB was measured for a 1.8 V_{pp}, 1 kHz sine wave input with 32 Ω load. Fig. A.13 shows the measured FFT and THD+N vs. frequency for a 1.8 V_{pp} signal.

Fig. A.14 shows the instantaneous efficiency and THD+N vs. amplitude for a 1 kHz signal vs. the normalized output signal amplitude. Note that the output stage behaves as a class-AB for $V_{pk}/V_{DDH} > 0.4\,V$, as a class-C for $V_{pk}/V_{DDH} < 0.5\,V$, and as a combination of both during the supply transition ($0.4\,V < V_{pk}/V_{DDH} < 0.5\,V$).

From Figs. A.13 and A.14, it is evident that the GPSS allows a supply transition with

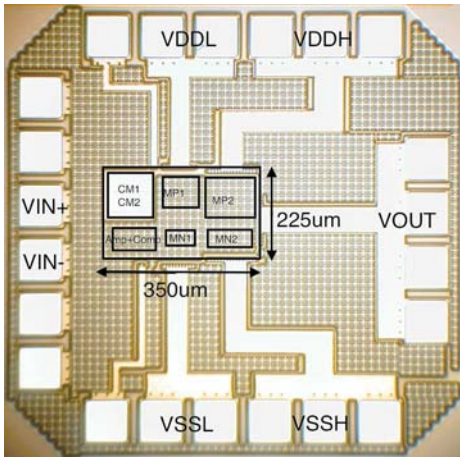

Figure A.11: Proposed class-G amplifier die micrograph.

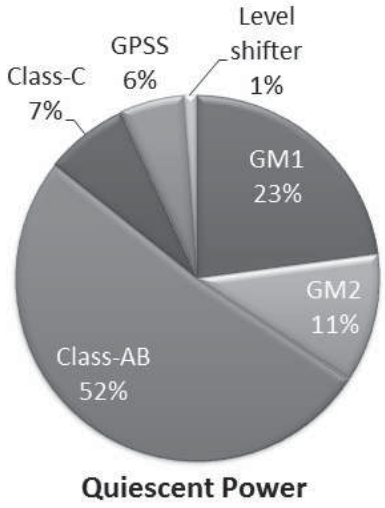

Figure A.12: Proposed class-G amplifier quiescent power distribution.

very low distortion. Also. it can be noticed in Fig. A.14 that the THD+N performance is limited by noise. It can be improved by decreasing the noise contribution from GM_1 at the expense of additional silicon area and increased quiescent power. The proposed implementation was chosen considering this tradeoff to achieve low quiescent power and low active area. If desired, the proposed GPSS biasing and class-G output stage can be designed to operate from higher supply voltages to provide more output power while keeping the ultra-low distortion during the supply transitions.

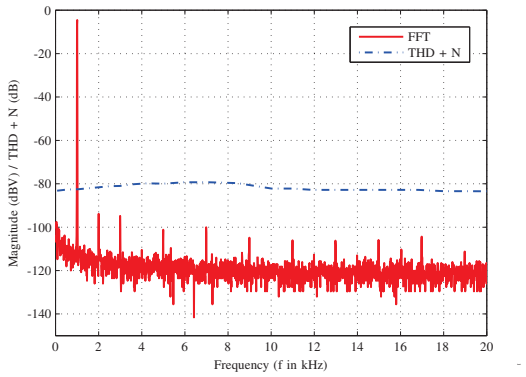

Figure A.13: Measured THD+N and output FFT versus frequency.

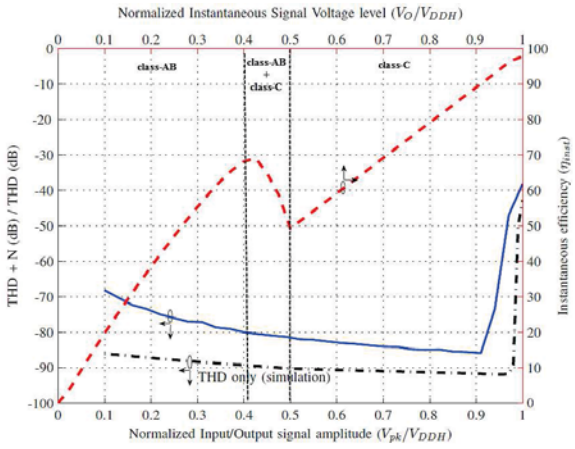

Figure A.14: Measured THD+N and efficiency versus amplitude.

Table A.1 presents a comparison of the state-of-the-art linear headphone amplifiers reported in the literature. It is evident that the proposed class-G output stage and GPSS biasing allows ultra-low distortion during the supply switching compared with the state-of-the-art class-G amplifiers while consuming low quiescent power and active area. The key problem in reported class-G amplifiers is the increased distortion due to the power supply transition. The proposed amplifier solved this problem by using the GPSS biasing. Unlike previously reported class-G amplifiers, the proposed work does not add substantial distortion after the supply transition.

Table A.1: Comparison with state-of-the-art headphone amplifiers

Design (class)	**This work (G)**	**[8] (G)**	**[9] (G)**	**[10] (G)**	**[5] (AB)**	**[6] (AB)**
Supply voltages	± 1.00 V ± 0.50 V	± 1.40 V ± 0.35 V	2.95 V - 4.50 V	2.65 V - 4.50 V	3.00 V	3.3 V
Quiescent power	**0.35mW**	0.41mW	1.77mW	2.91mW	1.43mW	0.84mW
Peak Power [a] (R_L=16Ω)	50mW	90mW	62mW	120mW	94mW	82mW
THD+N @1 kHz @P_{RMS} (32Ω)	-82.5dB @12.5mW	-80dB @16mW	-88dB @10mW	-95dB @10mW (16Ω)	-78dB @94mW (16Ω)	-84dB @10mW (16Ω)
SNR	89dB (un-weighted)	100dB (A-weighted)	108 dB (A-weighted)	111dB (A-weighted)	80dB (un-weighted)	-
Area	**0.08mm²**	0.14 mm²	0.31mm²	0.62mm²	0.34 mm²	0.67 mm²
Technology	90 nm	65 nm	180 nm	180 nm	500 nm	40 nm
Added distortion (after supply switching) [b]	**~0dB**	6dB	1~2dB	1~4dB	N/A	N/A

[a] 1 kHz signal, THD+N ≤ 1%

[b] Approximated estimation from reported THD+N vs. amplitude plots

A.5 Conclusion

A CMOS class-G headphone amplifier with low distortion during the power-supply transition was presented. The proposed class-G output stage achieves a gradual power-supply switching which is enabled by proper biasing and negative feedback applied to the amplifier. The design tradeoffs such as supply variation, load variation, stability, and linearity were discussed for the implemented prototype. The proposed class-G headphone amplifier was fabricated in CMOS 90 nm standard technology, and achieves a THD+N of -82.5dB, using low power consumption (350μW), and small silicon area (0.08mm^2).

APPENDIX B

CLASS-D AMPLIFIER WITH SLIDING MODE*

Architectures using variable structure control (VSC) based on sliding mode control (SMC) can decrease the power consumption, achieve low distortion, and reduce the complexity of the system [63]. Still, this approach is prone to high-frequency noise, as it requires a differentiator in the feedback loop, as discussed in Section 3. Also, this topology has a limited power supply rejection ratio (PSRR) in the audio band because the differentiation's low-frequency attenuation reduces the loop gain. To overcome this limitation, we propose a CDA with integral sliding mode control (ISMC) [76] to increase the low-frequency loop gain above that in [63] and to keep the controller power consumption low.

This appendix presents a clock-free current-controlled CDA using integral sliding mode control [64]. The proposed CDA provides the low distortion and high efficiency benefits of state-of-the-art CDAs, but consumes at least 30 % less controller power. Additionally, the proposed design improves the PSRR mainly due to good matching. Also, improvement of PSRR is obtained by higher loop gain within the audio band when compared with [63].

B.1 Design of the proposed class-D architecture with ISMC

Fig. B.1 shows the block diagram of the proposed architecture. This topology consists of two feedback loops and four main building blocks. The outer voltage loop minimizes the voltage error between the input and output audio signals, and the inner current loop

*

contains information proportional to the inductor current which is necessary to implement the controller, as will be explained later in the paper. The building blocks are the integral sliding mode controller, a hysteretic comparator, an output stage, and an off-chip low-pass filter (LPF). The ISMC processes the necessary information to generate the binary modulated signal. The hysteretic comparator obviates the carrier signal generator that would have been required in conventional architectures based on PWM [8]. The output stage provides the required current-drive capability for an 8-Ω loudspeaker, and the output filter recovers the audio signal.

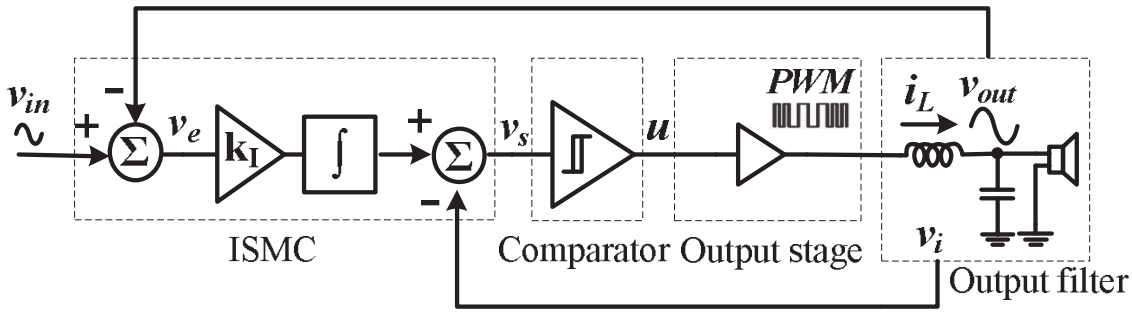

Figure B.1: Block diagram of the proposed class-D amplifier.

The audio amplifier implements a tracking system governed by a control law, defined with the switching function given by,

$$s(v_e, v_i) = k_I \int v_e(t)dt - v_i(t) \tag{B.1}$$

where k_I is an integration constant whose value ensures stability and fast transient re-

sponse, v_e(t) is the voltage error function defined as,

$$v_e(t) \;=\; v_{in}(t) \;-\; v_{out}(t) \tag{B.2}$$

and $v_i(t)$ is a sensed voltage proportional to the inductor current $i_L(t)$.

The ISMC retains all the properties of variable structure control (VSC) with sliding-mode operation such as simple design, stability, robustness, and good transient response. Moreover, the ISMC forces the system to operate with sliding mode under any initial condition [76]. This property guarantees robust system operation from any starting point. The ISMC's integrator nulls the steady-state voltage error, and the closed-loop dynamics reduce high-frequency noise. Furthermore, sensing the current across the output inductor improves the dynamic response of the amplifier [74].

The system can be proven to be asymptotically stable with the equivalent control method analysis [76]. This method consists of determining the dynamics of the system on the switching surface, i.e. $s(v_e, v_i) = 0$. The sliding-equilibrium point of the proposed architecture is a stable focus because the eigenvalues of the system are complex with negative real part. Moreover, the final value theorem (FVT) shows that the steady-state response of the equivalent control model tracks the input signal [63].

B.2 Integral sliding mode controller

Fig. B.2 shows the schematic of the implemented CDA. The blocks marked as I, II, III and IV are the ISMC, comparator, output power stage, and LPF, respectively.

Examining the node $v_{s\pm}(t)$ one obtains the switching function implemented as

$$s(v_e, v_i) = k_I \int \left[v_{in\pm}(t) - v_{out\mp}(t)\right] dt - v_i(t), \tag{B.3}$$

where

$$\begin{aligned} v_i(t) &= k_s \cdot R_s \cdot i_L(t) \\ &= k_s \left[v_{c\pm}(t) - v_{out\pm}(t) \right] \\ &= k_s \left[v_{c\pm}(t) + v_{out\mp}(t) \right] \end{aligned} \tag{B.4}$$

represents the voltage proportional to the current i_L(t) across the inductor and $k_s = R_D/R_C$. Equations (B.3) and (B.4) describe the implemented controller circuit.

The proposed CDA uses two external precision resistors (R_s) in series with the filter inductor to sense the inductor current and to feed it back to the controller. The value of these resistors was chosen high enough to sense the voltage across the resistor but sufficiently small to minimize its impact on the power efficiency of the system.

Fig. B.3 shows the tradeoff between the R_s value and the efficiency of the CDA when

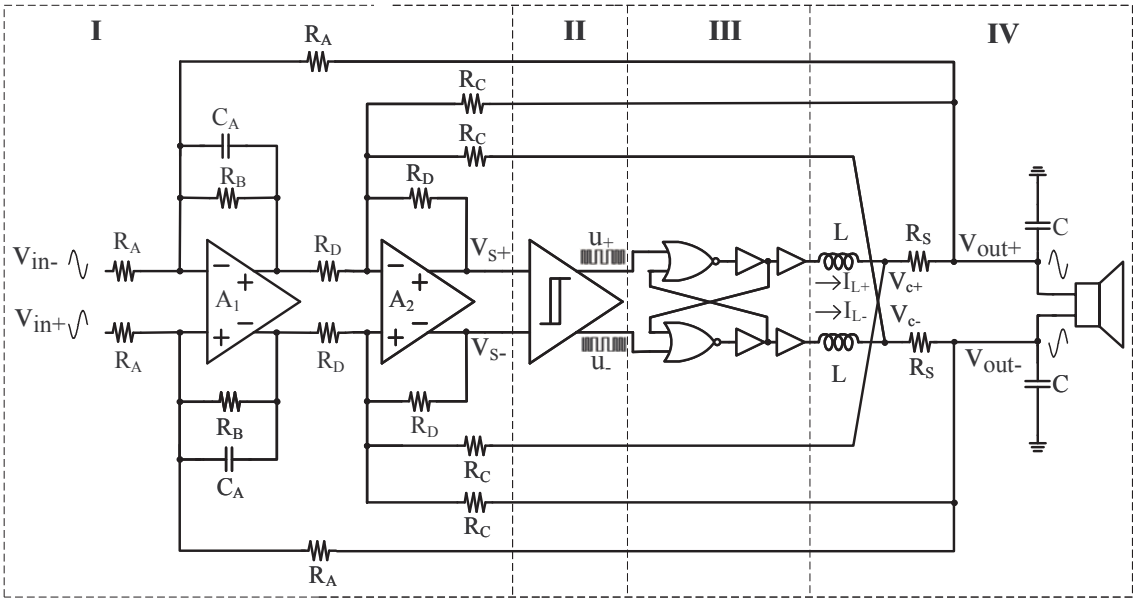

Figure B.2: Proposed ISMC implementation, I ISMC implementation, II comparator, III output power stage, IV LPF.

V_{in} = 2 V_{pp}; the smaller R_s, the higher the efficiency. However, an excessively small value of R_s could be comparable to parasitic board/package resistances, reducing measurement accuracy. We choose R_s = 100 mΩ to achieve both good accuracy and high efficiency, we choose k_s= 10 to have a voltage $v_i(t)$ directly proportional to i_L(t). Note that other current sensing techniques, as discussed in Section 3, could be employed in the ISMC architecture to improve efficiency and/or to reduce the external component count.

A fully differential amplifier (A_2) senses the inductor current using cross connected $v_{c\pm}$(t) nodes. Both the lossy integrator (A_1) and current sense (A_2) amplifiers are two-stage-Miller compensated and consume 35 μA and 90 μA of static current, respectively. Amplifier (A_1) has a DC open-loop gain of 68 dB and a phase margin of 59° and amplifier (A_2) has a DC open-loop gain of 62 dB and a phase margin of 45°.

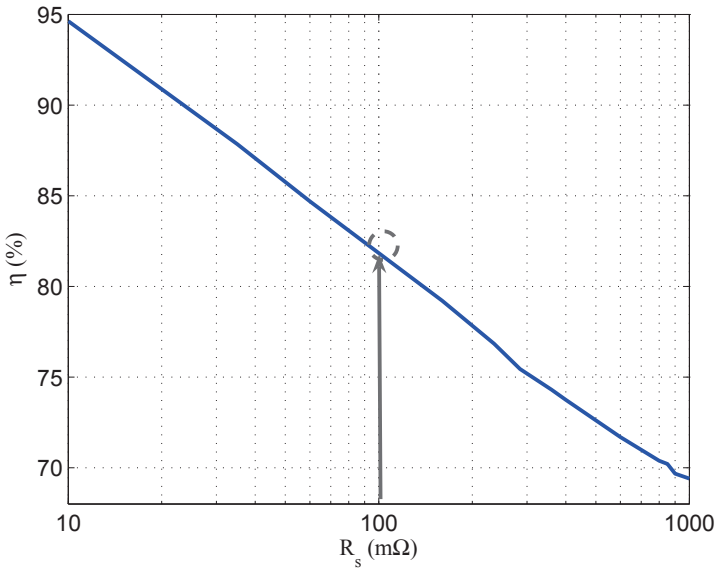

Figure B.3: Efficiency versus R_s for V_{in}= 2 V_{pp}.

The lossy-integrator has $k_I = 1/R_A C_A = 1.78 \cdot 10^5$ for fast transient response[63], where R_A = 280 kΩ , and C_A = 20 pF. Resistor R_B was implemented with a T-network structure to save die area.

The comparator consumes only 50 μA and has internal positive feedback [119] to generate a $\pm$10 mV hysteresis window such that the CDA runs at approximately 380 kHz. The schematic of the comparator is shown in Fig. B.4.

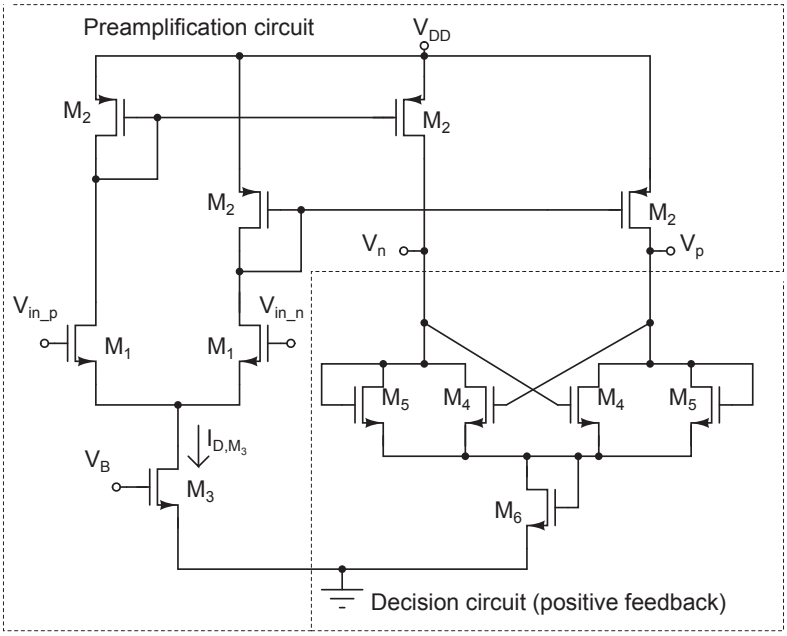

Figure B.4: Hysteretic comparator implementation.

The comparator consists of two stages: the input preamplifier to improve the comparator sensitivity and a positive feedback or decision stage. An output buffer (not shown) converts the output into a rail-to-rail signal. The transconductance g_m of M_1 determines the 1st stage gain, and the size W, L of M_1 determines the input capacitance C_{in}. To ensure high speed, the circuit has no high-impedance nodes other than the input and output nodes.

The decision circuit uses positive feedback from the cross-gate connection of transistors M_4 to increase the gain of the decision element. The hysteresis window [119] is given by,

$$V_{hys} = \frac{2I_{D,M3}}{g_{m,M1}} \frac{\frac{\beta_{M4}}{\beta_{M5}} - 1}{\frac{\beta_{M4}}{\beta_{M5}} + 1} \; for \; \beta_{M4} \geq \beta_{M5} \tag{B.5}$$

where

$$\beta_{M4,5} = K_n \frac{W_{M4,5}}{L_{M4,5}}. \tag{B.6}$$

Transistor M_6 increases the switching point to the desired DC common mode level. The output buffer is a NAND SR latch to convert the output of the decision circuit to a full swing signal.

We designed the output buffer to minimize the dynamic power dissipation without degrading the propagation delay, and we reduced the short-circuit current with a non-overlap configuration. In addition, we minimize conduction losses by reducing the CMOS on-resistance R_{on}. The calculations yielded a tapering factor between stages T = 11, a number of inverters N = 4 with and R_{on} = 220 mΩ. The dimensions of the PMOS power switch are W = 27000 μm and L = 0.6 μm and the dimensions of the NMOS power switch are W = 9000 μm and L = 0.6 μm.

The off-chip 2^{nd}-order LPF was designed with a cutoff frequency of 20 kHz, with L = 45 μH, C = 1.5 μF, and an 8 Ω speaker. We chose a Butterworth filter approximation to achieve flat magnitude response within the audio band. The design of the integral sliding mode controller relies on the value of the elements in the low-pass filter as mentioned in the appendix. Therefore, the proposed topology could be if necessary converted into a filterless architecture by calculating the coefficients of the integral sliding mode controller according to the speaker model to obtain the highest performance possible.

B.3 Experimental results of CDA with ISMC

The class D audio power amplifier was fabricated in 0.5 μm CMOS standard technology (V_{THN} = 0.7 V, V_{THP} = -0.9 V) and tested with a System One Dual Domain Audio Precision instrument using a 2.7-V single voltage supply. The chip was encapsulated in a DIP 40 package. Fig. B.5 shows the die micrograph of the fabricated CDA where blocks I, II, and III correspond to the ISMC, comparator, and output power stage, respectively. The total active area occupied by the class-D audio amplifier is approximately 1.65 mm^2.

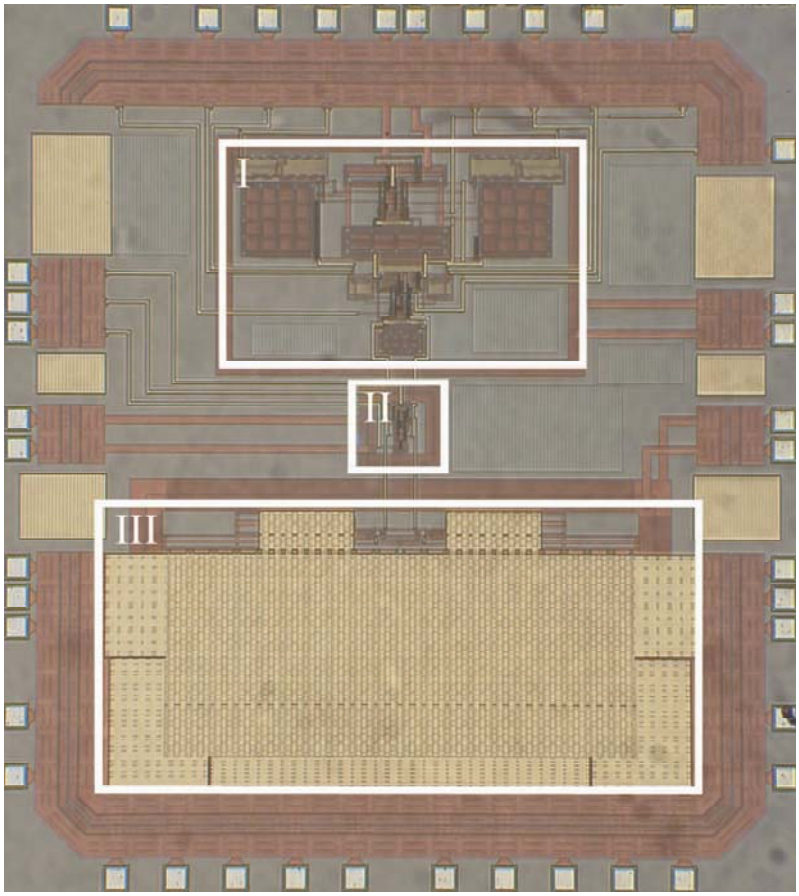

Figure B.5: Class-D with ISMC die micrograph, I controller (0.430mm^2), II comparator (0.033mm^2), and III output stage (1.190mm^2).

The class-D amplifier quiescent power distribution is shown in Fig. B.6(a). The output stage consumes 68 % of the total quiescent power and the current-sense amplifier (A_2) consumes approximately half of the controller's power.

The area distribution of the class-D audio amplifier is presented in Fig. B.6(b). The power stage occupies around two thirds of the total area. On the other hand, the comparator represents only 2% of the total area.

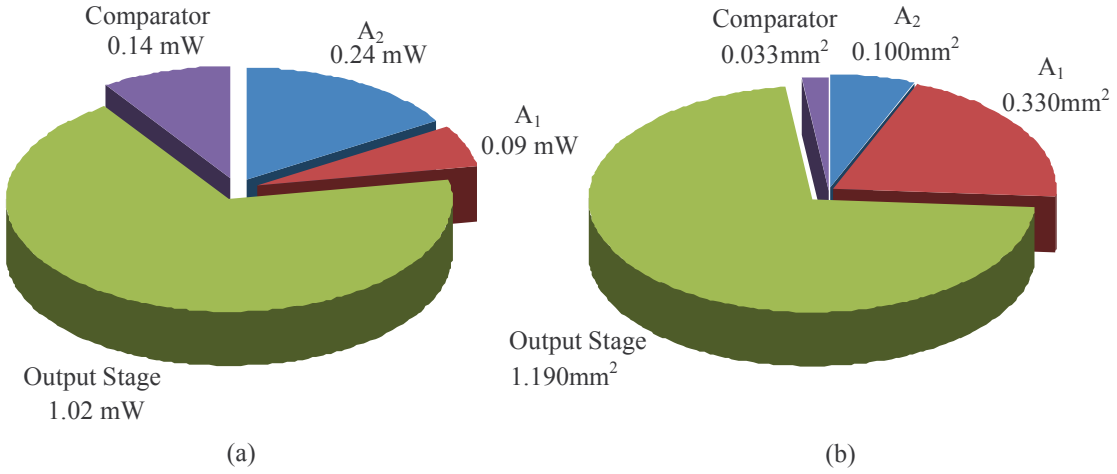

Figure B.6: (a) Power and (b) area distribution of the proposed audio amplifier.

The output spectrum of the system with $V_{in} = 2.82\ V_{pp}$ at 1 kHz is illustrated in Fig. B.7. As shown in the figure, the difference between the fundamental tone and the higher harmonic ($HD_3 = 3f_{in}$) is > 70 dB.

The total harmonic distortion plus noise (THD+N) and the efficiency (η) performance of the CDA are shown in Fig. B.8 and Fig. B.9, respectively. A THD+N of 0.02 % and an efficiency of 84 % were measured.

The proposed system achieves a maximum output power of 410 mW for 7 % THD+N. Thus, the system can provide approximately 90 % of the maximum theoretical power.

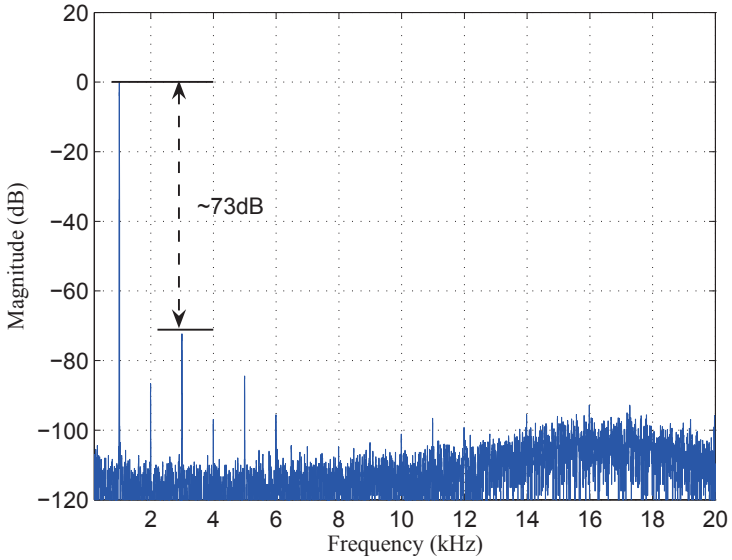

Figure B.7: Class-D audio amplifier output FFT when V_{in} = 2.82 V_{pp} at 1 kHz.

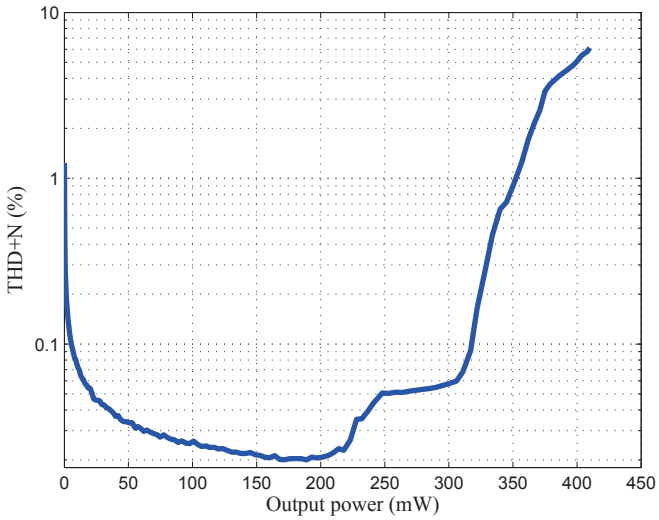

Figure B.8: Class-D amplifier with ISMC THD+N versus output power.

The voltage drop across R_s limits the maximum output voltage swing and hence limits the maximum power. Fig. B.10 shows the PSRR and SNR versus frequency.

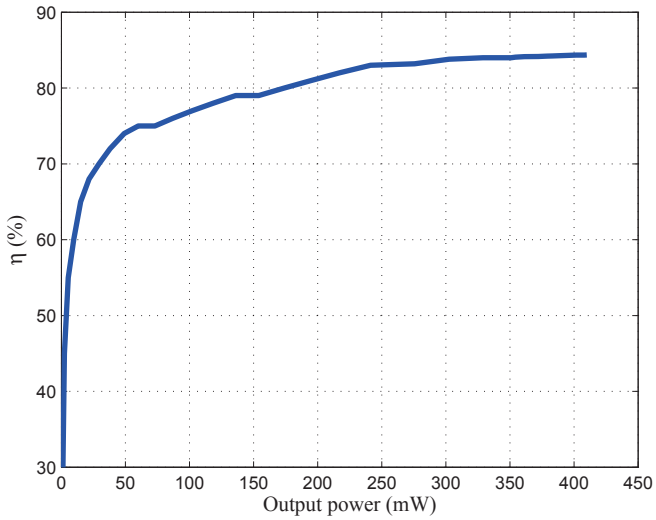

Figure B.9: Class-D amplifier with ISMC efficiency versus output power.

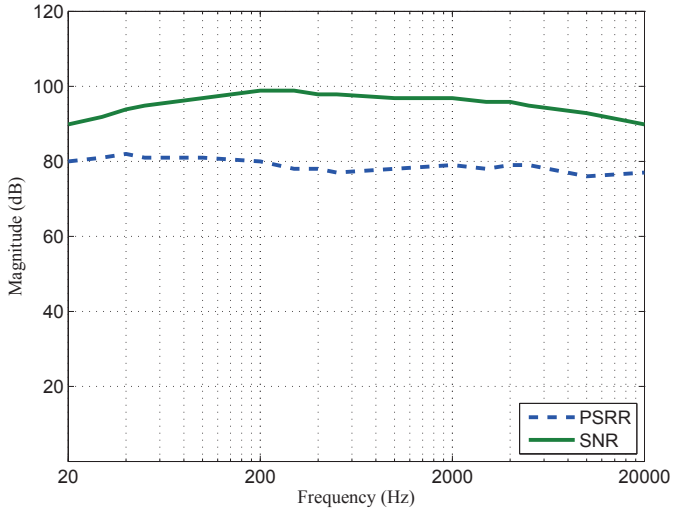

Figure B.10: Class-D audio amplifier PSRR and SNR versus frequency.

A maximum PSRR of 82 dB was obtained while applying a sine-wave ripple of 100 mV_{pp} on the power supply. The SNR was measured with respect to 410 mW into an 8 Ω resistor and was better than 90 dB across the entire audio band.

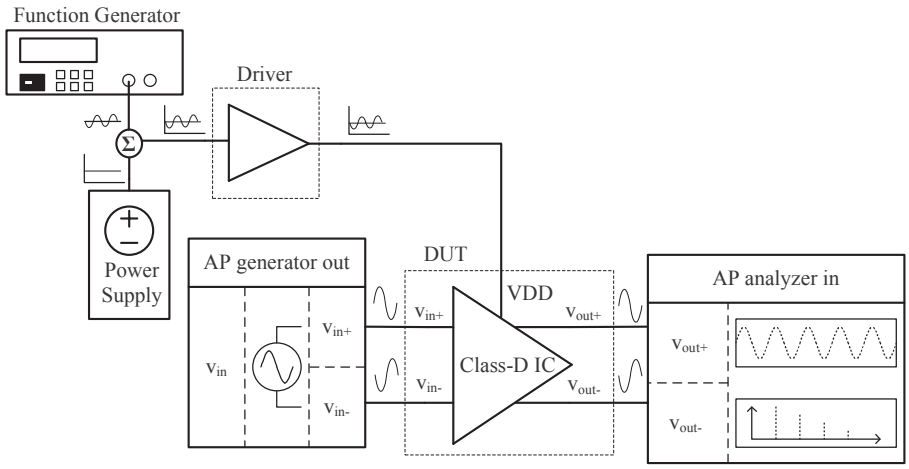

Figure B.11: Measurement setup for PS-IMD measurement.

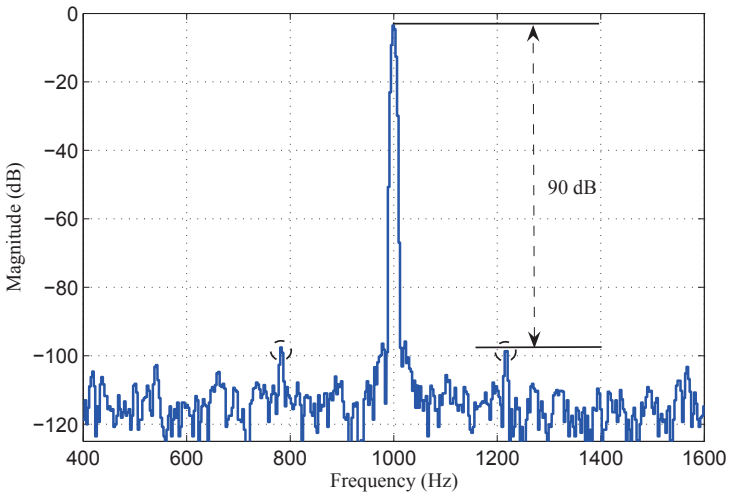

Figure B.12: Power supply induced intermodulation distortion measurement.

Class-D audio amplifiers may experience power-supply-induced intermodulation distortion (PS-IMD). Fig. B.11 shows the power supply induced intermodulation distortion measurement setup. We performed the power supply induced intermodulation test with an input voltage signal of 2 V_{pp} at 1 kHz and sinusoidal power-supply ripple of 300 mV_{pp} at 217 Hz superimposed on the DC level. A driver between the waveform generator and the VDD pin of the class-D amplifier provides the current required by the CDA. Fig. B.12 shows that the difference between the intermodulation products (783 Hz and 1217 Hz) and the fundamental is approximately -90dBc.

Table B.1: Performance Summary for CDA with ISMC

Design	[8]	[62]	[5]	[65]	[63]	This Work
P_c (mW)	-	50.00	-	40.00	0.68	**0.47**
P_Q (mW)	14.98	194.00	35.00	-	-	**1.49**
I_c (mA)	-	10.00	-	8.00	0.25	**0.17**
I_Q (mA)	4.70	12.00	7.00	-	-	**0.55**
PSRR (dB)	70	67	68	70	77	**82**
SNR (dB)	98	-	102	117	94	100
THD (%)	0.030	0.001	0.01	0.001	0.020	0.02
η (%)	76	88	85	85	89	84
Supply (V)	4.2	5.0	5.0	5.0	2.7	2.7
Load (Ω)	8	6	8	8	8	8
f_s (kHz)	410	450	1800	600	450	380
P_{OUT} (mW)	700	10000	1400	1400	250	410
Area (mm^2)	0.44	10.15	-	6.00	1.49	1.65
Process	90nm DCMOS	0.6μm BCDMOS	-	0.7μm CMOS	0.5μm CMOS	0.5μm CMOS
Topology	PWM	$\Sigma\Delta$	$\Sigma\Delta$	Hysteretic	SMC	ISMC

Table B.1 compares the performance of the presented CDA to that of the state-of-the-art audio amplifiers. We have included both controller's power P_c and quiescent power P_Q

because we do not have complete information about the total quiescent power of previous works. Compared to previously published CDAs, the proposed CDA with ISMC improves PSRR by at least 5 dB, and consumes at least 30 % less controller power.

B.4 Conclusion

This paper has presented the design, implementation, and experimental results of a high PSRR clock-free current-controlled class-D amplifier. The proposed audio amplifier is based on integral sliding mode control to ensure robust operation and to provide zero steady-state error. The prototype has linearity and efficiency comparable to the state-of-the-art yet requires 30 % less controller power and improves the PSRR. Furthermore, we measured a power supply induced intermodulation distortion of approximately -90 dBc for an input voltage signal of 2 V_{pp} at 1 kHz and sinusoidal power-supply ripple of 300 mV_{pp} at 217 Hz superimposed on the DC level.

APPENDIX C

PAPER CONTRIBUTIONS

- **A.I. Colli-Menchi**, J. Torres, and E. Sanchez-Sinencio, "A Feed-Forward Power-Supply Noise Cancellation Technique for Single-Ended Class-D Audio Amplifiers," *IEEE J. of Solid-State Circuits*, vol.49, no.3, pp.718-728, March 2014.

- **A.I. Colli-Menchi** and E. Sanchez-Sinencio, "High-efficiency Selfoscillating Class-D Amplifier for Piezoelectric Speakers," to appear in *IEEE Trans. on Power Electronics*, 2015.

- J. Torres, **A.I. Colli-Menchi**, M.A. Rojas-Gonzalez, and E. Sanchez-Sinencio, "A 470μW clock-free current-controlled class D amplifier with 0.02% THD+N and 82dB PSRR," *Proceedings of the ESSCIRC*, pp.326,329, 14-16 Sept. 2010

- J. Torres, **A.I. Colli-Menchi**, M.A. Rojas-Gonzalez, and E. Sanchez-Sinencio, "A Low-Power High-PSRR Clock-Free Current-Controlled Class-D Audio Amplifier," *IEEE J. of Solid-State Circuits*, vol.46, no.7, pp.1553,1561, July 2011

- B. Bhamidipati, **A.I. Colli-Menchi**, and E. Sanchez-Sinencio, "Low Power CMOS Class-G Audio Amplifier with Gradual Power Supply Switching," To appear in *IET Circuits, Devices & Systems*, 2015.

- X. Liu, **A.I. Colli-Menchi**, and E. Sanchez-Sinencio, "An Automatic Resonance Tracking Scheme with Maximum Power Transfer for Piezoelectric Transducers," under revision in *IEEE Transaction on Industrial Electronics*, 2015.