A 2.4 GHZ PHASE MODULATOR FOR A WLAN OFDM POLAR TRANSMITTER IN 0.18 UM CMOS

A Dissertation

by

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ABSTRACT

This research focuses on the design and implementation of a digital active phase modulator path of a polar transmitter in the case of orthogonal frequency division multiplex WLAN application. The phase modulation path of the polar transmitter provides a constant envelope phase modulated signal to the Power amplifier (PA) , operating in nonlinear high efficient switching mode. The core design of the phase modulator is based on linear vector-sum phase shifting topology to differential quadrature input signals. The active phase shifter consists of a DAC that generates binary weighted currents for I and Q branches and differential signed adder that vector-sums the generated quadrature currents to generate the phase at the output.6 bits control the phase shifter, creating 64 states with the resolution of 5.625 ° for the whole 360 °. The linear (binary weighted) vector-sum technique generates a reduction in the resultant amplitude that should be taken into consideration in case of nonlinear PA in polar transmission. On the other hand, the digital phase information is applied as the control bits to the phase shifter that determine the weightings and the signs of the I and Q vectors. The key point is the operation of the phase modulator in terms of phase accuracy, with the wideband modulation standard such as OFDM WLAN.

A technique has been proposed to enable the polar phase modulator to operate with a real-time wideband data and to compensate for the phase shifter output reduction. Since the reduction in gain is due to vector sum resultant of I and Q currents, it is compensated by modifying the I and Q currents for each 64 phase states. The design is implemented using 0.18 um CMOS technology and measured with maximum data rate of 64 QAM,OFDM modulation of WLAN standard. The

output amplitude of the phase shifter with the correction technique is approximately constant over the 64 states with maximum variation of 3.5mv from the constant peak to peak value. The maximum achieved phase error is about 2° with a maximum DNL of 0.257.

DEDICATION

To My Father, Mother, and Brother

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1. INTRODUCTION

It is critical to increase the power efficiency while minimizing the off-chip components for any radio frequency transmitter [15], [16]. Peak power efficiency of a RF transmitter directly determines the size of the power supply and heat dissipation, therefore playing a forceful part on final product miniaturization factor, reliability, yield, and cost [17],[6]. The efficiency of a transmitter system can be remarkably improved by using a highly efficient nonlinear RF power amplifier [18] [19]. Nonlinear Saturated or switch-mode PAs are more efficient than linear PAs and they may be fabricated easier on silicon since the driver stages do not need to be linear. The nonlinear PAs are also less noisy and less sensitive to changes in operating points caused by process-voltage-temperature (PVT) variations [16].

A high efficiency TX architecture utilizes the polar modulation techniques with nonlinear PAs, where the base-band signal is modulated in amplitude and phase domain (polar) instead of cartesian in-phase and quadrature (I and Q) domain [20] [21]. The resultant TX system is then called "polar transmitter". A number of recent polar transmitters have demonstrated their advantage through highly-integration systems [22], [23], [24],[25], but only for narrow band modulation standards such as GSM-EDGE. More recently, [26] [27] [28] polar architecture has migrated to wideband standards like WLAN.

The IEEE802.11a , WLAN standard allows high-speed wireless communication with maximum data rate of 54 Mb/s. Figure 1.1 shows the IEEE802.11a air interface and OFDM channelization [1]. It can be seen that the higher data rates employ condenser modulation schemes like OFDM. Also, wireless systems use OFDM to minimize the delay spread for higher data rates. On the other hand, using high

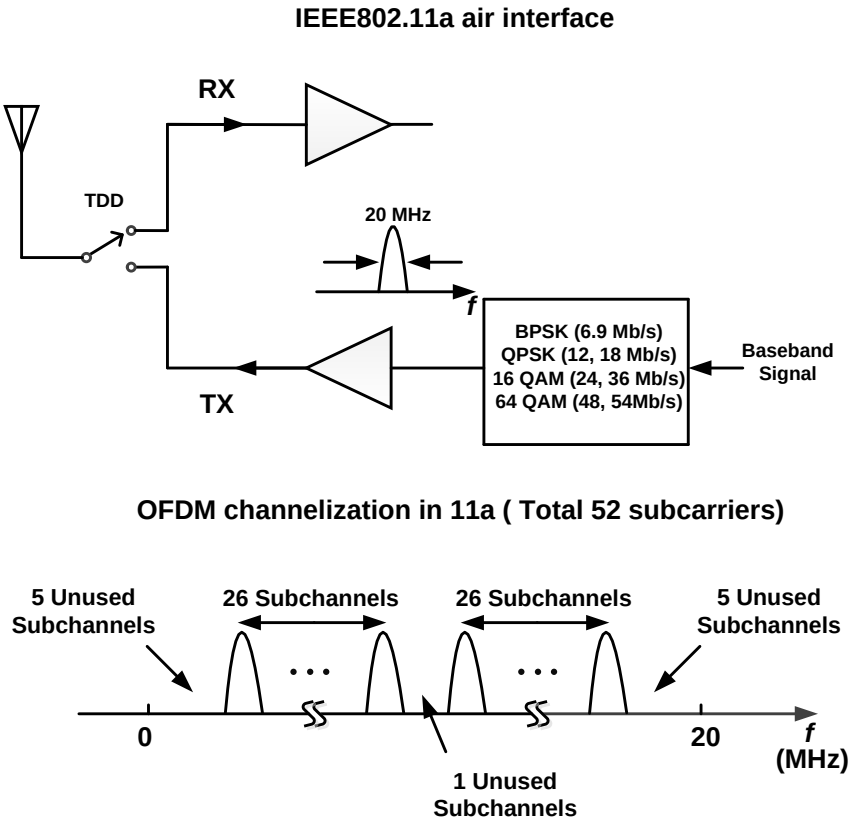

Figure 1.1: IEEE802.11a air interface and OFDM channelization

speed modulation results in tougher requirements on the TX and RX design. OFDM scheme forces severe linearity requirements on the power amplifiers. This is because the subcarriers shown in the OFDM channelization, are summed at the final stage of the whole system before the PA and the summation may be constructive for some points, creating a large amplitude, or destructive for some other points, generating a small amplitude. In other words, the peak to average ratio (PAR)that can be defined as the ratio of the largest value of the square of the signal divided by the average value of the square of the signal, $PAR = \frac{Max[x^2(t)]}{\overline{x^2(t)}}$, as illustrated in Figure 1.2 as large amplitude variation due to OFDM [1].

In Polar transmitters, the phase modulation is amplified separate from the ampli-

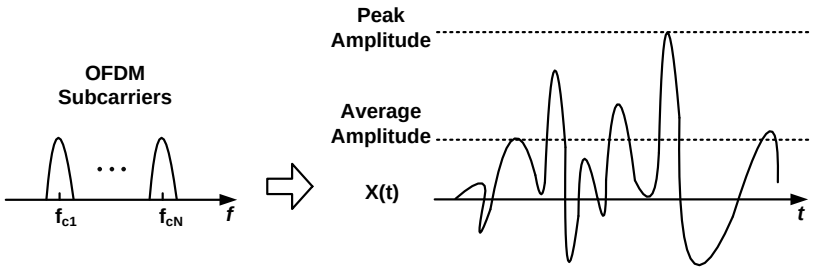

Figure 1.2: Large amplitude variation due to OFDM

tude envelope. So, the high level amplitude modulation that requires sever linearity specifications is accomplished by the amplitude modulation path and the resultant modulated amplitude is fed as the supply to the PA. Also, the phase path generates a constant envelope phase modulated signal with no linearity requirements which would be the input signals of the PA. As a result, PA that is in the nonlinear switching-mode, amplifies a constant envelope phase signal and the amplitude information is restored by the supply. There are various implementation techniques for polar transmitters such as using digitally controlled-PLL [4], pulse-modulation using a PWM generator [29] both for WCDMA applications, using Envelope Tracking (ET) for WiMAX, or digitally normalized I/Q vector summing [9] for OFDM transmitter. The proposed transmitter architecture is based on the last one for OFDM WLAN.

The focus of this research is on the design of the phase modulation path of the polar transmitter, creating a constant envelope phase modulated for the WLAN OFDM signal with the maximum data rate of 54 Mb/s. The are different types of phase shifting techniques including LC-based using distributed switches [11], continuous all-pass networks [12], switch-typed phase shifter with integrated VGA [13], and active vector sum [14], [30]. Most of the phase shifting architectures are implemented for phased-array applications. Phase shifters in phased-array systems are as

beam-steering elements and the real-time high speed phase response is not required. Whereas, for WLAN OFDM signal with high data rate, a modified version of the vector-sum architecture is needed to handle the high-speed data. Also, due to the nature of quadrature vector sum architecture in linear mode,[30] and [14], there will be an amplitude reduction at the resultant output of the phase shifter. This change in the output amplitude is detrimental in the case of phase modulated signal for polar transmitter, since the whole purpose of employing nonlinear efficient PA is to amplify a constant envelope phase signal. For these two reasons, the vector sum architecture with a correction block is design to provide the constant envelope phase signal for the maximum data rate of WLAN OFDM signal with high phase accuracy.

2. POLAR MODULATION AND EER

2.1 Polar transmitter and EER concept

Modern wireless data communications have been dominated by the tight compromise between spectral and supply power efficiency for a given transmission data rate. This led to complex modulation formats where amplitude and phase modulation are combined to code the source symbols. To achieve that, in-phase and quadrature (I/Q) versions of the RF carrier are simultaneously modulated with the appropriate real and imaginary components of the low-pass equivalent modulating envelope in an I/Q modulator. These two RF modulated signals are then combined to generate the desired AM and PM modulation format, which is then processed by a supposedly linear RF power amplifier (PA). This architecture is known as the Cartesian topology to distinguish it from the more recently investigated polar architecture. Unfortunately, this Cartesian architecture has an important drawback in power supply efficiency because high fidelity of amplitude modulation formats require highly linear, but, unfortunately, inefficient, class-A or class-AB PAs [31].

A modulation technique originally called "Envelope elimination and restoration" (EER) [32], also known as Khan technique circumvents this difficulty representing the complex envelope using amplitude and phase signals, respectively. The key concept of this approach is that the modulation is accomplished by a process in which the phase modulation component is amplified separate from amplitude envelope which will be restored at the final amplifier. This method offers very high efficient transmitters because of the ability to work with a highly nonlinear output stage. EER approach is more recently known as "polar modulation" because of processing the signal in the form of a envelope and phase component.

Polar modulation can operate in either a closed-loop or open-loop mode, and the resulting TX system is typically called as "polar transmitter". When one restricts the polar operation to the signal modulator only but not extending it to the high-power PA, the transmitter is called a "small-signal polar transmitter" or a "polar lite transmitter". In this case, the amplitude modulation AM signal at the output of the I/Q modulator can be read off from an AM detector or directly generated digitally at the baseband and then fed into the voltage control input of a variable gain amplifier VGA. The VGA will recreate the amplitude modulation by varying the signal level to the input of a linear PA. Therefore for the small-signal polar operation, the AM and phase modulated PM signals are recombined at the VGA. If, however, the AM and PM signals are recombined at the high-power PA (often off-chip), the transmitter is called as a "large-signal polar transmitter" or a "direct polar transmitter". When a polar transmitter applies closed-loop feedback control of both AM and PM portions of the signal from the high-power PA output, this closed-loop transmitter is called a "large-signal closed-loop polar transmitter" or simply a "polar loop transmitter". Strictly speaking, a polar loop TX system can use either large-signal or small-signal polar modulation and can have one or two feedback paths for AM and/or PM signals.

In general, the advantages of a large-signal polar transmitter include the improved PA efficiency, reduced wideband output noise floor (leading to elimination of bulky off-chip filters), and reduced sensitivity to PA oscillation with varying output load impedance over those of a linear PA system. Large-signal polar transmitters have recently demonstrated impressive results using the 57-year-old Envelope-Elimination-and-Restoration (EER; i.e., Kahn's technique) where the output power is directly modulated by the drain/collector voltage of the highly efficient nonlinear PA (i.e., "plate modulation"). In the past, polar transmitters were mostly used for high-power base station applications to effectively reduce heat dissipation; however, they have

recently become very successful for wireless handset TX design in volume production due to their significant better efficiency and lower cost [6].

Considering a band-pass signal as $V_{in}(t) = V_{env}(t)cos[\omega_0 t + \phi(t)]$, the envelope component $V_{env}(t)$ and the phase component $\phi(t)$ can be decomposed into envelope and phase signals. As shown in Figure 2.1,the block diagram of envelope elimination and restoration, a limiter eliminates the envelope, producing a constant-amplitude, phase-modulated carrier. The detected envelope is then amplified separately. The results of phase and amplitude paths are recombined by the amplitude modulation of the final RF power amplifier that restores the envelope to the phase-modulated carrier.

The envelope detector generates the amplitude envelope $V_{env}(t)$ and a limiter produces the phase signal, containing the carrier, $V_{Phase}(t) = V_0 cos[\omega_0 t + \phi(t)]$. The key point is that the final stage amplifies a constant-envelope phase signal and therefore can be nonlinear that will make the design highly efficient. Nonlinear RF power amplifiers (e.g., classes C, D, E, and F) offer more efficiency than linear PAs like classes A and B. High-efficiency high-level amplitude modulation is accomplished by AF power amplifier in class-S or -G , such as DC-DC converter, [33] while a class E/F amplifier, such as switching PA in class E amplifies the constant-envelope phase signal.

Finally, the recombination of phase and envelope paths is typically performed by applying the envelope signal to the supply voltage of the switching PA such that the output swing becomes a function of V_{DD}. So, to restore the amplitude, the supply voltage of the switching PA is modulated by the AM signal. Thereby, although the PA itself is operated in a nonlinear high-efficiency mode, the total transmitter shows linear behavior while maintaining the high efficiency.

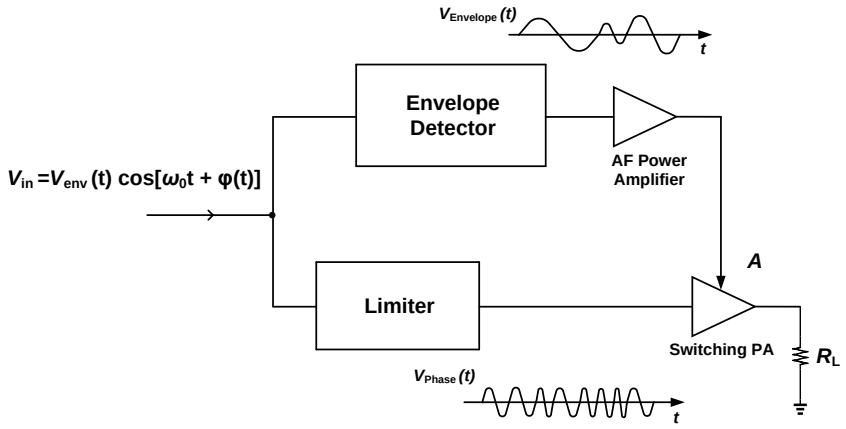

Figure 2.1: Block diagram of envelope elimination and restoration [1]

2.2 Polar modulation issues

From theoretical point of view, EER is a perfect system. However, it is followed by a number of difficulties and issues in practice. The EER requires a coordinate transform of the Cartesian digital in-phase and quadrature (I&Q) signals to polar amplitude (A) and phase-modulated RF ϕ signals. An ideal recombination of the A and signals ϕ in the output stage of the transmitter yields perfect amplified I&Q signals in the output of the transmitter. However, any small mismatch of delay between amplitude and phase paths or any bandwidth restrictions for both paths reveals the dominant nonlinearity due to the coordinate transform [34]. Therefore, the significant drawback of EER is that the transformation from Cartesian to polar coordinates are nonlinear:

$$A(t) = \sqrt{I(t)^2 + Q(t)^2} \tag{2.1}$$

$$\phi(t) = tan^{-1} \frac{Q(t)}{I(t)} \tag{2.2}$$

And amplitude and phase signals occupy wider bandwidths than the original Cartesian signal with in-phase (I) and quadrature (Q) components. While much of the information of A resides at low frequencies, a much wider bandwidth is required to reconstruct the original signal in Cartesian with sufficient precision [35]. The analog (A) and digital (ϕ) signals with relatively wider bandwidths are processed by circuits with finite bandwidths; a power supply modulator limits the A signal and a phase-locked loop (PLL) limits the phase signals. Therefore, A and ϕ are low-pass filtered before recombination and information is lost that degrades the fidelity of the recombined signal. To further study the imperfection of the conversion of I and Q signals to polar signals, let's consider the polar conversion is done all digitally in the following way [2]. Instead of generating a $\phi(t)$ signal, two signals $I_\phi = cos(\phi(t))$ and $Q_\phi = sin(\phi(t))$ are used and each of these components are multiplied by ω_C that is the RF carrier. So, when using Cartesian I and Q signals, the complex digital-modulated signal s_D becomes:

$$s_D(t) = I(t)cos(\omega_C t) + jQ(t)sin(\omega_C t) \tag{2.3}$$

Consequently, The EER technique should produce the same digitally modulated signal at the transmitter output. As mentioned earlier, the A(t) and $\phi(t)$ have a much broader spectra than I and Q signals and after phase modulation, the phase RF signal would becomes:

$$s_{RF}(t) = cos(\phi(t))\ cos(\omega_C t) - sin(\phi(t))\ sin(\omega_C t) = cos(\omega_C t + \phi(t)) \tag{2.4}$$

Considering the ideal case that the switching PA operates as a multiplier, it gives

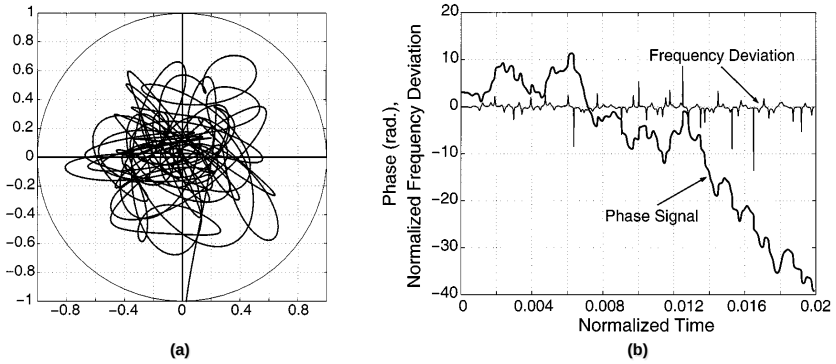

Figure 2.2: (a) Vector diagram of I and Q noise signals, (b) Phase and frequency variation of I and Q noise signals [2]

out the output signal as:

$$s_D(t) = A(t).S_{RF}(t) \tag{2.5}$$

$$s_D(t) = A(t).Ree^{j\phi(t)}.e^{j\phi(t)} \tag{2.6}$$

$$s_D(t) = I(t)cos(\omega_C t) + jQ(t)sin(\omega_C t) \tag{2.7}$$

As a result, in the ideal case the amplification is set to one and the $s_D(t)$ signal is equal again in the transmitter's output, thus, the spectra stays the same.

In reality, the spectral characteristic of the polar A(t) and $\phi(t)$ signals can be shown by the band limited Gaussian-noise-like signals, that have a Rayleigh amplitude distribution. Figure 2.2 (a) shows the vectordiagram of I and Q signals and (b) phase and frequency variation of I and Q noise signals. As shown in Figure 2.2 (a), the vector diagram of I and Q noise signals approaches to zero. This causes rapid changes in the phase and angle that corresponds to frequency deviations, leading to the frequency peaking shown in Figure 2.2 (b) phase and frequency variation of I and Q noise signals.

However, wedges or cusps of the amplitude signal and rapid phase changes of the phase signal, produce broad spectra of either these signals, and also of the SRF(t) signal. Also, the broader the spectra are, the worse the compensation in the PA stage becomes and the more out-of-band(OOB) emission comes up. Out-of-band emission is also known as adjacent channel power or spectral regrwoth. Thus, a straightforward idea to avoid all those problems is to punch a hole into the vector diagram.

It turns out that a "hole" in the vector diagram of the modulation scheme significantly reduces the OOB emissions. In other words, the amplitude and phase modulated are clipped to reduce the crest factor of the modulated signals. The amount of the modulated signal below the clipping threshold defines a clipping signal which is shaped as Gaussian to fit the modulated signals spectra. After wards, this clipping signal is added in vector mode to the I and Q signals and, thus, results in a hole into vector diagram as shown in Figure 2.3 (a) an example of vector diagram of complex noise with a "hole". Accordingly, amplitude and phase frequency responses are improved as shown in Figure 2.3 (b) the spectra of RF phase and modulated digital RF signal and Figure 2.3 (c) spectra of the I, Q, and, A signals, respectively.

So, the amount of unwanted emissions depends on the type of digital modulation used in the system and a modulation scheme that already has a "hole", like digital offset modulations, is better suited for EER techniques than others [2].

Another problem associated with EER is that the amplitude and phase paths delays are different. The phase signal that is up converted to RF frequencies, experience more delay than the amplitude path operating at lower frequencies. These delays should be matched for accurate reconstruction of the original signal at the output of the switching PA. Therefore, a very precise synchronization scheme is required.

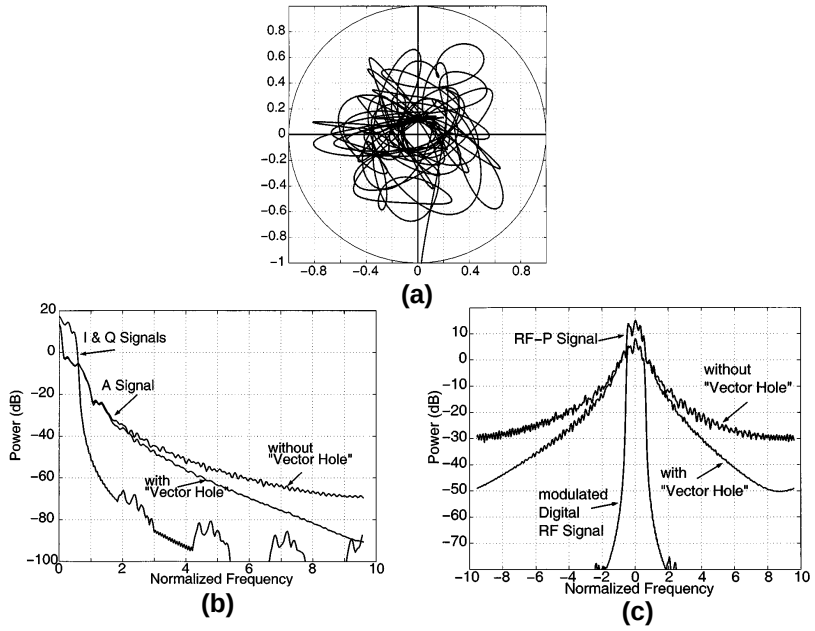

Figure 2.3: (a) Example of vector diagram of complex noise with a "hole", (b) Spectra of RF phase and modulated digital RF signal, (c) Spectra of the I, Q, and, A signals [2]

2.2.1 Nonlinear distortion of polar transmitters

Unfortunately, as any other engineering solution, polar architecture does not follow an ideal distortion-free operation, presenting a series of nonlinear impairment mechanisms. As aforementioned, two main sources of nonlinear distortion are finite AM modulator bandwidth and differential delay between the output amplitude $a_y(t)$ modulated signal and the phase $\phi_y(t)$ modulated carrier [33]. However, there are also other sources such as the amplitude signal $a_x(t)$ to $a_y(t)$ nonlinear supply voltage modulator transfer function and $a_x(t)$ to $\phi_y(t)$ parasitic AM to PM conversion. These two other sources of distortion are also known as, $v_D D(t)$ to $a_y(t)$ nonidealities and $v_D D(t)$ to $\phi_y(t)$ conversion [31].

The finite AM modulator bandwidth was first approximated by assuming an ideal

brick-wall reconstruction filter [33]. However, the analysis of the finite bandwidth can be further extended by considering a general reconstruction filter. To study the effect of finite AM modulation bandwidth, the IMD products that occur as a result of envelope filtering in an ideal EER system are observed which are derived based on a two-tone test. Considering two signals with unity amplitudes, with ω_m and ω_c being the angular frequencies of the modulating signal and the carrier, respectively.

$$v_i(t) = cos(\omega_m t)\ cos(\omega_c t) = \frac{1}{2}cos(\omega_c - \omega_m)t + \frac{1}{2}cos(\omega_c + \omega_m)t \tag{2.8}$$

$v_i(t)$ can also be represented as an amplitude and phase modulated wave, i.e.

$$v_i(t) = E_i(t)cos(\omega_c t + \phi_i(t)) = E_i(t)v_x(t) \tag{2.9}$$

where $E_i(t)$ is the envelope of the input signal and the $\phi_i(t)$ is the phase modulation of the RF carrier. Assuming the angular time by $\theta = \omega_m t$, for the two-tone signal, it is easy to see that

$$E_i(t) = |E_i(t)cos(\omega_m t)| \tag{2.10}$$

and

$$\phi_i(t) = \begin{cases} 0, & cos(\theta) \geq 0 \\ \pi, & cos(\theta) < 0 \end{cases} \tag{2.11}$$

Figure 2.4 shows the block diagram of the EER two-tone system. In case the of the two-tone signal, the phase variation $\phi_i(t)$ corresponds to reversals in the carrier polarity. Therefore, signal $v_x(t)$ which is fed to the input of the amplifier can be simply represented as the original RF carrier multiplied by the switching function

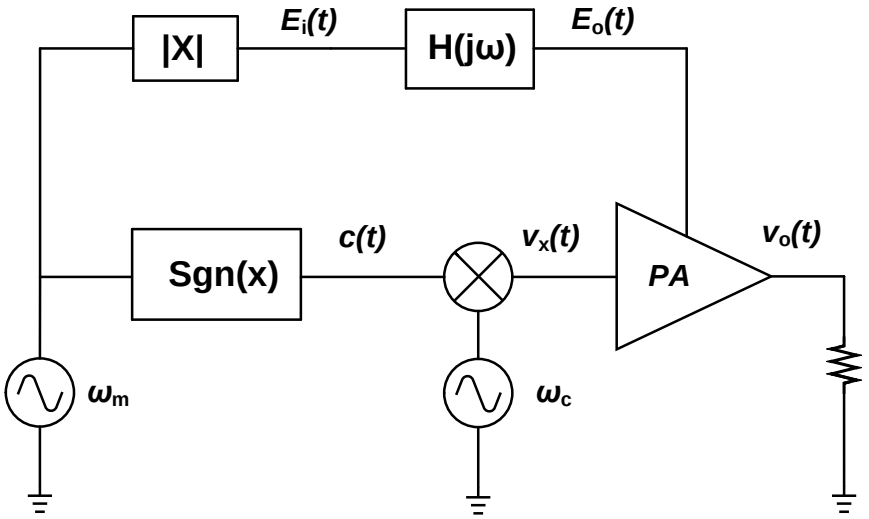

Figure 2.4: Block diagram of EER two-tone test system

$c(\theta)$,

$$v_x(t) = cos(\omega_c t + \phi_i(t)) = c(\theta)cos(\omega_c t) \tag{2.12}$$

where,

$$\phi_i(t) = \begin{cases} 1, & cos(\theta) > 0 \\ 0, & cos(\theta) = 0 \\ -1, & cos(\theta) < 0 \end{cases} \tag{2.13}$$

Since $E_i(\theta)$ and $c(\theta)$ are periodic signals, they can be expanded into Fourier series as

$$E_i(\theta) = a_0 + \sum_{m=2,4,6,...} (a_m cos(m(\theta))) \tag{2.14}$$

and

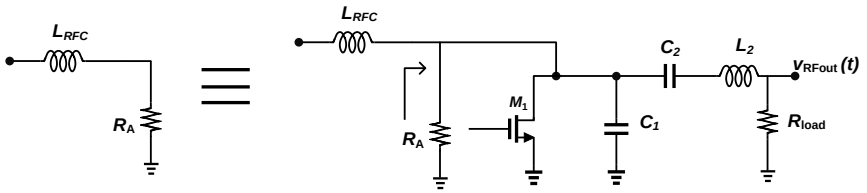

Figure 2.5: Low pass LR network in the class-E PA in EER system

$$c(\theta) = \sum_{m=1,3,5,...} (c_n cos(n(\theta))) \tag{2.15}$$

To further study the effect of finite bandwidth of AM modulator, let's consider the case where the envelope signal is passed through a simple low pass RL network shown in Figure 2.5 low pass LR network in the class-E PA in EER system. The LRFC is the DC-feeding inductance which is a consecutive part of circuitry and RA denotes the resistance that the circuit presents to the supply source in class-E-based EER.

The transfer function of the lowpass LR network is as follows:

$$H(j\omega) = \frac{1}{1 + j\frac{\omega}{\omega_t}} = H(\omega)e^{j\phi(omega)} \tag{2.16}$$

where $\omega_t = R_A/L_{RFC}$ representing the 3dB frequency of the filter and the amplitude and phase characteristic are,

$$H(\omega) = \frac{1}{\sqrt{1 + (\frac{\omega}{\omega_c})^2}} \tag{2.17}$$

and

$$\phi(\omega) = -arctan(\frac{\omega}{\omega_t}) \tag{2.18}$$

The amplitude and phase response of the filter at harmonic frequency of ω_m will be denoted as h_k and ϕ_k, respectively, where

$$h_k = H(k\omega_m) = \frac{1}{\sqrt{1 + (\frac{k\omega_m}{\omega_t})^2}}, \qquad k = 1, 2, 3, ... \tag{2.19}$$

and

$$\phi_k = \phi(\omega) = -arctan(\frac{k\omega_m}{\omega_t}), \qquad k = 1, 2, 3, ... \tag{2.20}$$

So, due to action of the lowpass RL circuit, the restored envelope of the output signal will be as following,

$$E_o(\theta) = a_0 + \sum_{m=2,4,6,...} (a_m h_m cos(m(\theta) + \phi_m)) \tag{2.21}$$

and the reconstructed signal at the output of the power amplifier can now be observed as the following,

$$v_o(t) = E_o(\theta)v_x(t) = E_o(\theta)c(\theta)cos(\omega_c t) = y(\theta)cos(\omega_c t) \tag{2.22}$$

where $y(\theta)$ is the modulating function. In order to analyze the IMD products of the output signal, it is necessary to consider the spectral content of the modulating function, $E_o(\theta)c(\theta)$.

$$y(\theta) = [a_0 + \sum_{m=2,4,6,...} (a_m h_m cos(m(\theta) + \phi_m))] \sum_{m=1,3,5,...} (c_n cos(n(\theta))) \tag{2.23}$$

Therefore, the spectral components of the modulating function are the result of mixing of each of the spectral component in $E_o(\theta)$ with each of the spectral

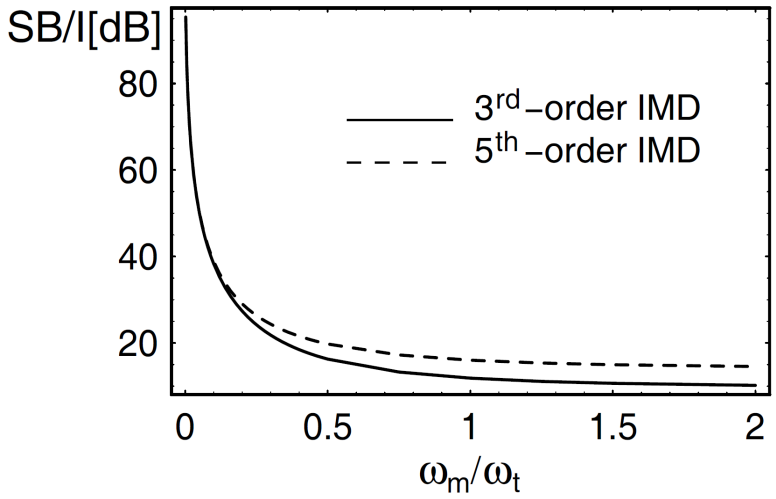

Figure 2.6: The calculated SB/I response of the EER system to the LR low pass filter [3]

component of $c(\theta)$. The presence of the phase term ϕ_m and the gradual roll-off of the lowpass transfer function require special attention and cause the analysis to be more complicated. To characterize the IMD behavior, the sideband-to-intermediation ratio is defined. the SB/I ratio gives a less optimistic picture of the intermodulation distortion in the EER-based transmitter than a carrier-to-intermodulation, since information is contained in the sideband product and not in the carrier. The results obtained from the one-pole low pass filter are shown in Figure 2.6 the calculated SB/I response of the EER system to the LR low pass filter. The dominant IM products are of the third and fifth order that have been plotted. At low values of ω_m/ω_t , SB/I3 and SB/I5 have virtually the same values. A rapid drop in the SB/I ratio can be noted as the frequency of the modulating signal ω_m approaches the corner frequency ω_t of low pass filter.

To analyze the IMD due to differential delay between the output amplitude $a_y(t)$ modulated signal and the phase $\phi_y(t)$ modulated carrier, let's consider first the linear

process of amplitude signal $a_x(t)$ to $v_{DD}(t)$. Also, the envelope amplitude is coded in a over-sampled 1-bit data stream either with or without quantization noise shaping in the digital class-S modulator with clock or sampling frequency of ω_s. To account for any possible differential delay τ, between this 1-bit digital signal and the $\phi_x(t)$ PM signal, it is reasonable to state that the reconstructed analog amplitude signal that is the supply voltage of the RF PA, will be a linear, but delayed replica of the AM input $v_{DD}(t) = a_x(t-\tau)$. Ideally, the low-pass reconstruction filter $F(\omega)$ should only preserve the time-varying component centered on dc, i.e., $a_x(t-\tau)$, eliminating all the other spectral replicas that are centered at the harmonics of ω_s. As previously derived, the low-pass filter is not ideal brick-wall filter and will thus introduce linear amplitude and phase distortions in the $a_x(t)$ to $v_{DD}(t)$ characteristics and let pass high-frequency quantization noise. Hence, the final result of this 1-bit modulation and demodulation process will be a supply voltage amplitude given by,

$$v_{DD}(t) = \frac{8A}{\pi}\left[\frac{1}{2}F(0) + \sum_{n_1 even}^{\infty} |F(n_1\omega_m)| \frac{(-1)^{\frac{n_1-2}{2}}}{{n_1}^2 - 1} \times cos(n_1\omega_m t + \phi(n_1\omega_m))\right] + n(t) \tag{2.24}$$

where $n(t)$, is the unfiltered high-frequency quantization noise and $\phi(n_1\omega_m)$ includes the $F(\omega)$ phase contribution at the $n_1 th$ even harmonic component of $a_x(t)$ and the constant delay phase component τ as,

$$\phi(n_1\omega_m) = -jln\left[\frac{F(n_1\omega_m)}{|F(n_1\omega_m)|}\right] - n_1\omega_m\tau \tag{2.25}$$

The above analysis indicates that the nonideal low-pass reconstruction filter and differential delay between the AM and PM paths are the nonlinear impairments of polar transmitter and should be taken care of in highly linear operations.

2.3 Different polar transmitter architectures

There are many approaches presented for the phase modulation of the polar transmitter. Each of them being suitable for different standards and applications. Here some of the most recent architectures will be presented.

2.3.1 Polar transmitter using all-digital phase-locked-loop (ADPLL)

The simplified block diagram of a polar transmitter using all-digital phase-locked-loop (ADPLL) is shown in Figure 2.7 simplified ADPLL-based polar transmitter. The baseband complex-number symbols are generated from the DBB processor at a rate f_{sym} (in sym/s). They are then up-sampled to a higher rate to be processed by the transmit (TX) pulse-shaping filter that constraints the transmitted bandwidth in a manner specified by the chosen communication standard. The symbol oversampling ratio (OSR) indicates the sampling rate increase. A Coordinate Rotation Digital Computer (CORDIC) circuit is utilized for the conversion of the Cartesian to polar complex-number-represented data, which are subsequently handed over to the polar modulation stage. At the heart of the polar modulator lies an all-digital phase-locked loop (ADPLL), which operates in the phase domain, Figure 2.8 [4], phase-domain ADPLL with two-point modulation.

It accepts input digital signals that carry phase/frequency information. The center frequency of the digitally controlled oscillator (DCO) variable clock (CKV) signal of frequency f_V is determined with respect to the reference clock (FREF) frequency f_R by the frequency command word (FCW).

Due to the existence of two asynchronous clock domains FREF and CKV, re-timing is performed by oversampling the FREF clock with CKV for synchronization purposes[36]. The re-timed clock CKR of average frequency is used to synchronize the ADPLL internal operations. The phase-modulating $\phi[k] = \phi(kT_(R))$data drive the

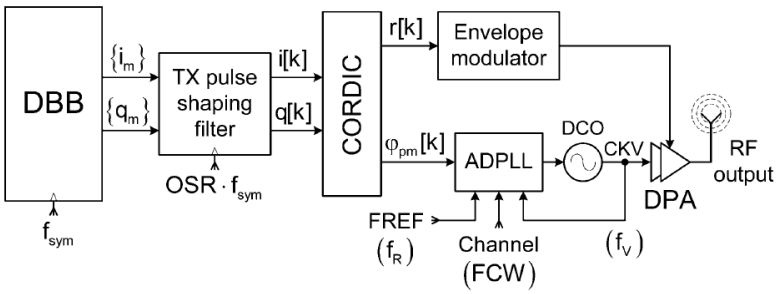

Figure 2.7: Simplified ADPLL-based polar transmitter [4]

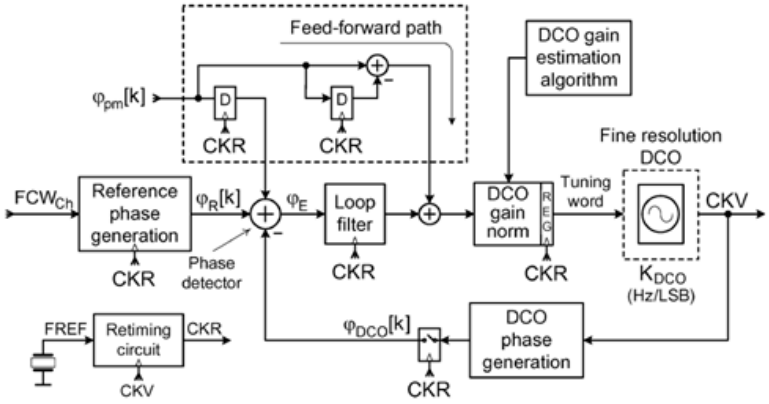

Figure 2.8: Phase-domain ADPLL with two-point modulation [4]

ADPLL as $\phi_{pm}[k]$ using a two-point modulation scheme [37]. The feed-forward path directly modulates the DCO oscillating frequency, and the resulting accumulated phase on the feedback path is corrected at the phase detector by the compensation path. This scheme allows the DCO to settle fast at a selected RF channel and, more importantly, opens the door to wideband modulation because of the broad low-pass $sinc^2(kT_R)$-type transfer function from the digital phase input to the DCO

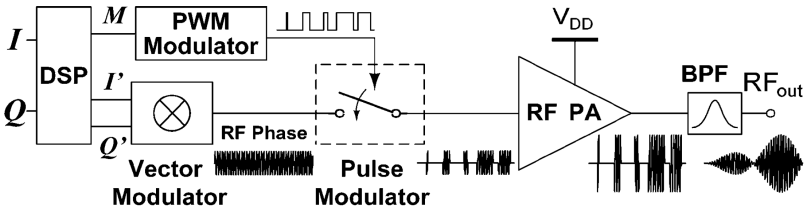

Figure 2.9: Block diagram of the polar transmitter using interleaving PWM [5]

RF output phase. The envelope modulator interpolates the envelope modulating data $r[k] = r(kT_R)$; its transfer function needs to be properly selected so that the nonlinear recombination of the envelope and phase modulations in the DPA produces a minimally distorted bandpass signal.

2.3.2 Pulse-modulated polar transmitter (PMPT) using pulse width modulation

The second phase modulation technique for polar transmitters is using pulse width modulation, shown in the Figure 2.9, the block diagram of the polar transmitter using interleaving PWM . The digital I and Q signals are processed by a digital signal processor (DSP) to calculate the signal magnitude, $M(t) = \sqrt{(I^2(t) + Q^2(t))}$, and normalize the IQ signals as $I'(t) = \frac{I(t)}{\sqrt{I^2(t)+Q^2(t)}} = \frac{I(t)}{M(t)}$ and $Q'(t) = \frac{Q(t)}{\sqrt{I^2(t)+Q^2(t)}} = \frac{I(t)}{M(t)}$. The normalized I' and Q' signals can be transformed to a constant-envelope RF signal by a vector modulator. The magnitude signal is modulated by a PWM modulator to generate a pulse train with different duty cycles. The pulse train will control the pulse modulator to modulate the constant-envelope RF signal to obtain a pulsed constant-envelope RF signal. Since the modulated RF signal has only two envelope levels (1 and 0), it can be amplified by a highly efficient switch-mode PA. It has been verified in [29] that the complex-modulated RF signal can be restored by bandpass filtering this kind of pulse modulated RF signal. The bandpass filtering

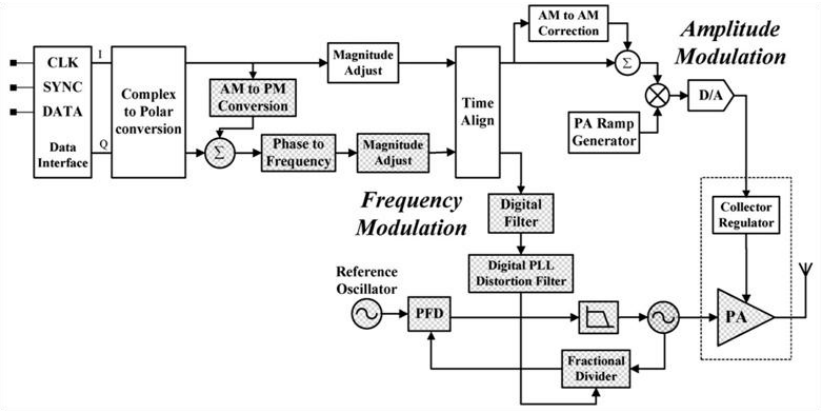

Figure 2.10: Block diagram of the open-loop large-signal polar transmitter (PM path shown in shaded blocks)[6]

can usually be done by a high-quality surface-acoustic-wave (SAW) filter already in commercial cellular handsets, such as a duplexer [5].

As shown in Figure 2.10, open-loop large-signal polar transmitter block diagram, can use feed-forward pre-distortion to linearize the AM-AM and AM-PM distortion in the PA. This enables elimination of power detectors, couplers, feedback circuits and many other functions required to support feedback loops. Power consumption is lower in open loop systems due to reduced complexity and less insertion loss after the PA. The TX data from the baseband is split into its AM and PM components with PM path shown in shaded blocks. The PM components are pre-distorted to compensate for the PLL loop filter roll-off and are then combined with the channel selection word of the fractional-N synthesizer, which provides the phase modulation of the 8-PSK (Phase Shift Keying) signal for EDGE modulation. The AM components are scaled according to the PA ramping control signal applied to the PA controller to modulate the saturated PA output directly, which PA control block offers a highly linear amplitude transfer function between the input control signal voltage and the

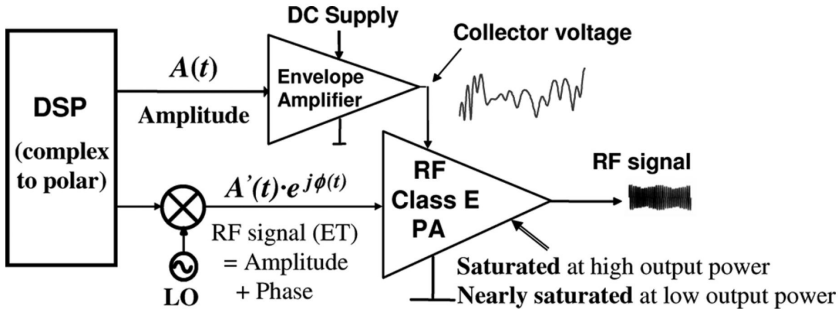

Figure 2.11: Block diagram of a RF polar transmitter system using ET technique [6]

output RF voltage. Carrier suppression is excellent as there is no upconversion in the TX system. This complete GSM/GPRS/EDGE radio system solution achieves higher functionality at lower cost for cellular handsets than one would obtain using the traditional I/Q transmitter approach.

2.3.3 Polar transmitter using envelope tracking (ET)

One latest development is to apply the Envelope-Tracking (ET) technique to implement monolithic large-signal polar transmitters for wireless applications, as excellent system efficiency and linearity has been demonstrated. Compared to EER-based large-signal polar TX system, it is found that an ET-based polar TX system (also known as hybrid-EER or H-EER architecture), and shown in Figure 2.11, the block diagram of RF polar transmitter system using ET technique , has the following benefits:

1) Higher gain at low output power. This is because the PA is "nearly saturated" but not always fully saturated as in the case of EER,

2) Lower sensitivity to timing mismatch between the RF versus amplitude paths than EER,

3) Lower bandwidth requirement for the envelope amplifier than that in the case

of EER. This can be critical as the efficiency of the envelope amplifier can be the limiting factor for an ET/EER system,

4) Relaxed bandwidth requirement for the circuits used in the RF path versus that in the case of EER. Since this ET-based polar TX architecture uses the RF modulation signal as the input to the saturated PA (instead of the PM signal), the PA needs to cover only the modulation signal bandwidth, making ET more suitable for broadband wireless applications than EER. The high bandwidth RF limiter required for EER can also be power hungry, while it is not needed for ET,

5) ET will have less RF feed-through signal that can appear as distortion in the TX output. Since the drive signal is hard-limited for the case of EER, it has sidebands that can cause intermodulation distortion (IMD) by the large gate-drain or base-collector capacitance in the final RF power device to couple to the output to cause EVM issues ;ET is better in this.

For reasons listed above, this ET architecture can be very attractive for implementing low power portable RF transmitter with excellent PAE [6].

2.3.4 All-digital polar RF modulation transmitter

Shown in Figure 2.12(a), all-digital polar RF modulator block diagram, has been proven to be susceptible to low-voltage nanoscale CMOS technology. The COordinate Rotation DIgital Computer (CORDIC) circuit transforms the baseband I and Q data streams to their polar equivalents, amplitude and phase, which gets differentiated to obtain frequency deviation $\Delta f = \Delta\theta/\Delta T_s$, where T_s is the sampling clock period. The frequency deviation is subsequently processed by the digital-to-frequency converter (DFC), whereas the amplitude signal is processed by the digital-to-RF-amplitude converter (DRAC). The DFC comprises a frequency modulator and a digitally-controlled oscillator (DCO). It could be realized, for example, as an all-

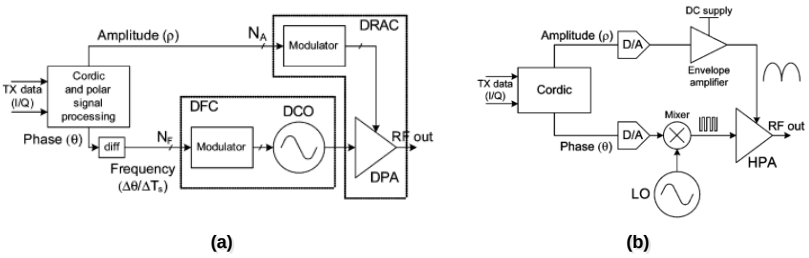

Figure 2.12: Block diagram of (a) an all-digital polar RF modulator, (b) analog-intensive polar RF modulator [7]

digital phase-locked loop (ADPLL) that also provides the negative feedback control of the DCO center frequency drift. The DRAC comprises an amplitude modulator and digitally-controlled prepower amplifier (DPA).

figure 2.12 (b) shows an analog-intensive polar RF modulator in which the DRAC is replaced by a digital-to-analog converter (DAC), baseband envelope amplifier and an external RF high-power PA (HPA). The frequency modulation is replaced there by the phase modulation using a mixer. This architecture completely avoids all the issues associated with the circuit limitations of the wideband frequency modulation by avoiding any phase-to-frequency conversions and performing the phase modulation directly [7].

2.3.5 EER system with FPGA controlled amplitude and phase commands

Utilizing digitally controlled passive phase shifter in the EER system with FPGA bias control is another phase modulation technique. Shown in Figure 2.13, block diagram of the EER system with FPGA controlled amplitude and phase commands, the FPGA allows the flexibility of generating arbitrary lookup-table-based periodic envelope and phase waveforms. The dc portions of the envelope is produced by the FPGA as the dc envelope command which controls the duty cycle of Q1 switch,

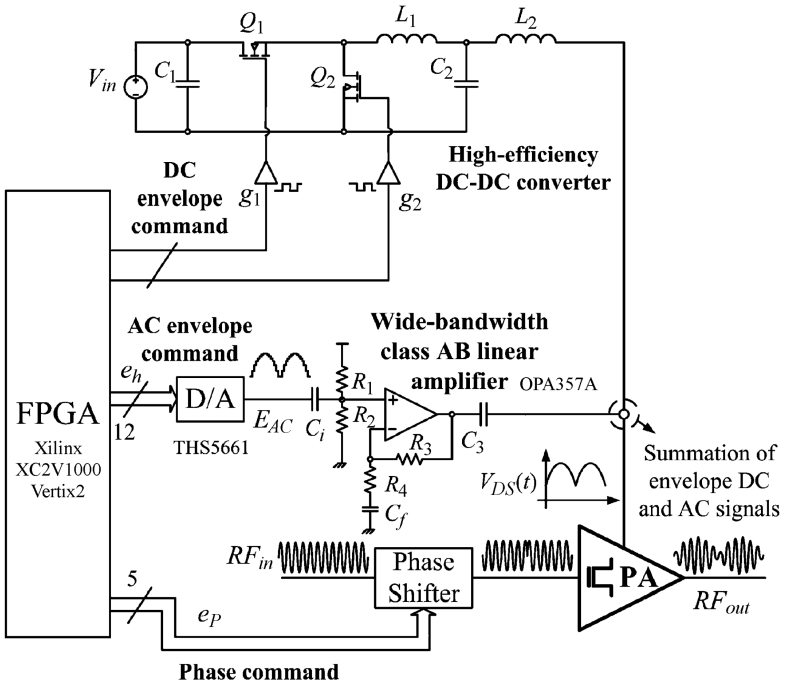

Figure 2.13: Block diagram of the EER system with FPGA controlled amplitude and phase commands [8]

adjusting the dc value of the envelope signal. The ac portion of envelope is also generated by the FPGA as 12-bit ac envelope command that passes through a 12-bit DAC. The dc and ac signals are coupled to obtain the supply voltage for the class-E PA. The phase of the RF input signal for the PA is controlled by a TriQuint TGP6336-EEU 5-bit X-band digitally controlled phase shifter. The phase shifter has around 9-dB loss, requiring a pre-amplifier at the input. The digital phase command is also generated by the FPGA controller.

The key function in this design is synchronizing the phase and amplitude delay by the FPGA look-up-table. There are two look-up-tables for envelope and phase command that both includes 50 samples per period of the equivalent sinusoidal wave form. Two identical counters are designed to select the envelope or phase sample.

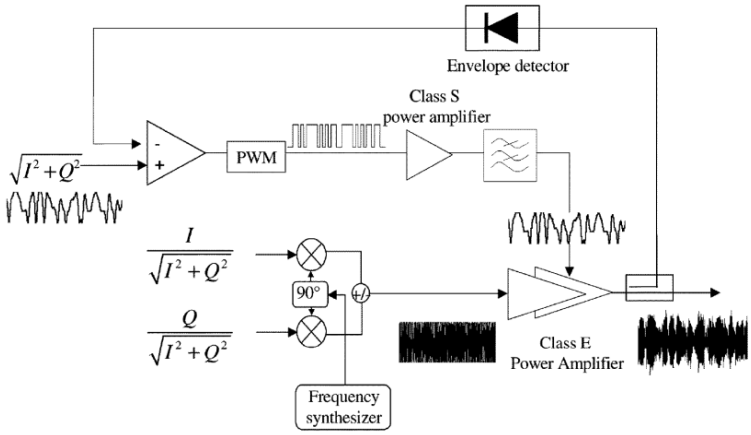

Figure 2.14: Block diagram of the EER system for OFDM transmitter [9]

Therefore, the phase and the ac envelope signals are synchronized. By shifting the phase or envelope data up or down in the lookup table, the delay between the envelope and phase command signals can be controlled in order to compensate for the delay in the envelope and phase signal paths[8].

2.3.6 EER architecture for WLAN OFDM transmitter

The EER system with the case of an orthogonal frequency division multiplex (OFDM) signal, the envelope is highly variable (Peak to Average Power Ratio is majored by N, where N is the number of sub-carriers). After amplification, the recombination of the envelope and phase information is accomplished by drain modulation of an amplifier such as class E type as illustrated in Figure 2.14, block diagram of the EER system for OFDM transmitter.

The polar transmitter for WLAN OFDM applications has the problem that the bandwidth for the envelope is very wide. The RF bandwidth of a WLAN 802.11a/g signal is 16.6 MHz while it is approximately 36.6 MHz for 802.11n. The envelope

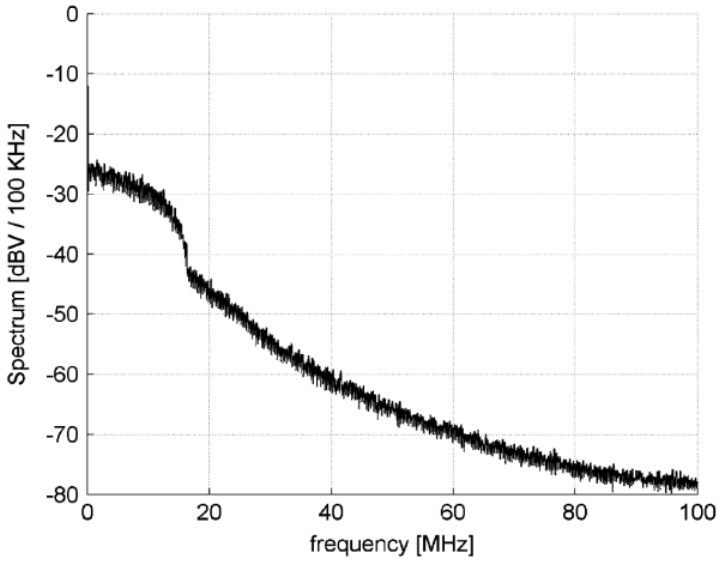

Figure 2.15: Envelope-spectrum for WLAN 802.11a [10]

bandwidth is much larger due to the nonlinear process of converting I- and Q-data to envelope data. Figure 2.15 shows the envelope-spectrum of the WLAN 802.11 a which is very wide, due to spectral regrowth. Efficient DC-DC converters have a too small bandwidth for coping with such envelope spectra, and can therefore not be used for WLAN-OFDM polar transmitters [10].

2.4 Phase modulator architectures

The focus of this thesis is mainly on the phase modulator path of the polar transmitter. First, let's review some of the state-of-the-art phase modulator designs. Several design topologies using standard silicon technology have been demonstrated to realize both digital and analog phase shifters for phase modulation. In general, digital phase shifters exhibit a high insertion loss and large chip area due to the cascade of several phase bits. In contrast, in analog phase shifters, the differential

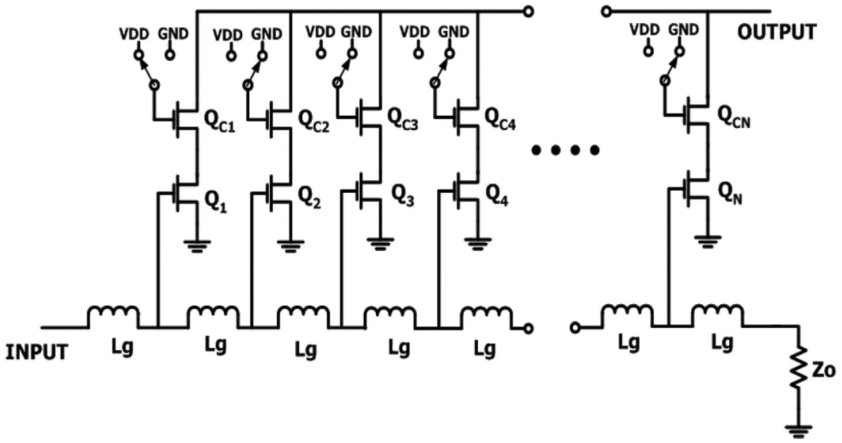

Figure 2.16: The digital phase shifter with distributed active switches topology [11]

phase shift is varied in a continuous manner by the capacitance change of a varactor or by the vector sum using active devices.

2.4.1 Digital phase shifter using distributed switches

The digital phase shifter with distributed active switches topology is shown in Figure 2.16 . The operation of the phase shifter is very similar to that of a traveling-wave amplifier. However, the circuit is associated with only one input artificial transmission line, unlike a conventional traveling-wave amplifier, which consists of input and output lines. The input line consists of a cascaded ladder network with series inductances and shunt capacitances. The shunt capacitors of the gate line are supplied by the gate capacitance C_{gs} of common source MOSFETs. The capacitance of transistors is related with the per-section phase shift and bandwidth. A low gate capacitance of transistors results in the high Bragg frequency,i.e. and the low per-section phase shift. It is beneficial to design high-frequency phase shifters as long as the of transistors is sufficiently high. A cascode design is chosen for the individual gain cells of the phase shifter. The cascode arrangement of two MOSFETs provides

high gain, high output resistance, and high reverse isolation. In addition, the cascode MOSFET operates as active switch, as the gate bias of the common gate MOSFET can be used as an effective means of switching between V_{DD} and GND. This enables the distributed phase shifter to be controlled digitally [11].

The input signal propagates through the gate line, tapping off some of the input power before being absorbed by a terminating resistor. The input signal sampled by the gate circuits at different phases is transferred to the output through each activated cascode cell. By switching the common gate MOSFETs in succession, the phase shift can be incremented by the steps of the phase constant of the input artificial transmission line. Therefore, the smallest phase shift is the unit phase shift of $\Delta\phi$ and the largest phase shift is $(N-1)\Delta\phi$.

An important parameter in phase shifters is the rms phase shift error. Most MMIC phase shifters exhibit a phase shift error due to manufacturing process variations and modeling inaccuracies of the circuit elements. For the proposed distributed phase shifter, the transistor capacitance variation C'_{gs} or the series inductance variation L'g results in the unit phase variation $\Delta\phi$'. The rms phase error S_{rms} can be obtained in terms of phase mismatch $\Delta\phi_{err} = |\Delta\phi - \Delta\phi'|$. it can also be computed as

$$S_{rms} = \sqrt{\frac{N(N-1)}{6}}\Delta\phi_{err} \tag{2.26}$$

In addition, the unit phase mismatch can be a function of the number of stages N needed for a required phase shift range. For a given gate capacitance or series inductance variation α, which is defined as C'_{gs}/C_{gs} or L'_g/L_g, the unit phase mismatch can be expressed by

$$\Delta\phi_{err} = \frac{\phi_{max}}{N-1}|1-\sqrt{\alpha}| \tag{2.27}$$

where ϕ_{max} is the maximum differential phase shift. As a result, the rms phase error can be calculated as

$$S_{rms} = \sqrt{\frac{N(N-1)}{6}}\frac{\phi_{max}}{N-1}|1-\sqrt{\alpha}| \tag{2.28}$$

Another important parameter of the phase shifter is the state-to-state variation of the insertion loss or gain. In practice, the gate voltage wave traveling throughout the gate artificial line will unequally excite the gates of common source MOSFETs due to the loss present in the gate artificial transmission line. Each successive common source MOSFET receives less signal voltage as the signal travels down the gate line. Hence, the current generators from the drains have different magnitudes. This results in a significant gain variation of the phase shifter. In order to equalize the current generators, it is necessary to change the transconductance of each cascode cell by adjusting the size of the common gate MOSFET. The magnitude of each current generator decreases as the differential phase shift increases, thereby increasing the size of the common gate MOSFET.

Figure 2.17 (a), transmission line circuit for the gate of the distributed phase shifter, shows a simplified equivalent circuit for the gate line of the distributed phase shifter. The input voltage wave propagating the gate line produces voltages $V_1, V_2, V_3, .., V_n$ across each gate capacitance C_{gs}. The voltage at the kth tap of the gate line is related to the gate lines segment length l_g and complex propagation constant γ_g.If the voltage across the input terminal of the distributed phase shifter is V_{in}, then $V_n = V_{in}e^{-n\gamma_g l_g}$.

Figure 2.17 (b) shows a simplified small-signal equivalent circuit of a single cas-

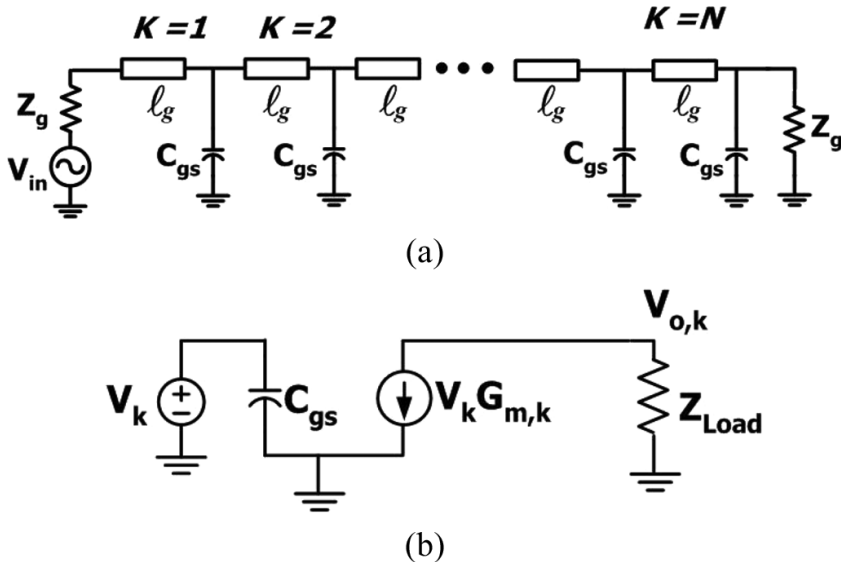

Figure 2.17: (a)Transmission line circuit for the gate of the distributed phase shifter. (b)Simplified small-signal equivalent circuit of a single cascode cell[11]

code cell. The current generator of each cascode cell can be expressed as $I_{o,n} = G_{m,n}V_n$, where $G_{m,n}$ is the effective small-signal transconductance of each cascode cell. The available gain of each phase state is given by $G_k = \dfrac{\frac{1}{2}|I_{o,k}|^2 Z_{Load}}{\frac{1}{2}|V_{in}|^2/Z_g}$ where $\gamma_g = \alpha_g + j\beta_g$, in which α_g and β_g are the attenuation and phase constant of the gate line, respectively.

The amplitude equalization of the distributed phase shifter is then obtained as $G_{m,k} = e^{(k-1)\alpha_g l_g} G_{m,1}$ and the transconductance of an MOSFET is directly proportional to the $\dfrac{W}{L}$ ratio. The effective transconductance of a cascode cell can be changed by varying the size of the common gate MOSFET. So, the width of the common gate MOSFET is given by $W_{c,k} = e^{(k-1)\alpha_g l_g} Wc, 1$. Indicating that the width of a common gate MOSFET increases as an exponential function of attenuation constant assuming that other parasitic losses are not considered. This is explained by the fact

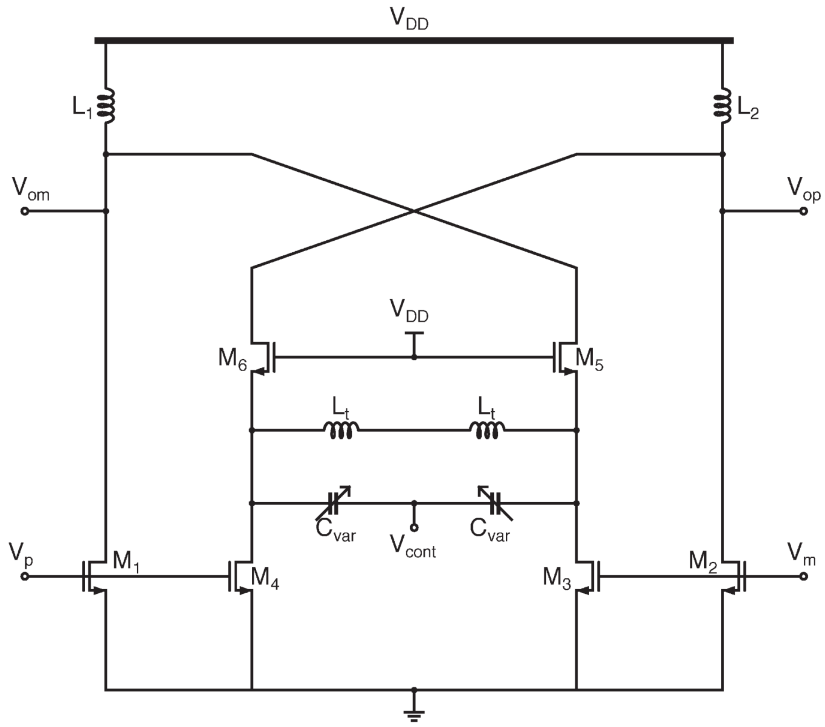

Figure 2.18: Schematic of the continuous differential active phase shifter [12]

that the input voltage on the gate line decays exponentially.

Process variation can affect the gain of the distributed phase shifter. If the transconductance of each cascode cell is changed at the same ratio by the process variation, there is no change of the gain deviation. The absolute gain value of each phase state can be higher or lower[11].

2.4.2 Continuous active phase shifter design for millimeter-wave phased-arrays

This design is a continuous active phase shifter for millimeter-wave phased-array transceivers with an all-pass network frequency response that provides continuous insertion phase control and nearly constant insertion loss regardless of the insertion phase variation.

Figure 2.18, schematic of the continuous differential active phase shifter, is com-

posed of two differential amplifiers and a resonant circuit. The main amplifier is a differential common-source structure implemented using transistors M_1 and M_2. The feed-through amplifier is a differential cascode common-source structure implemented using M_3, M_4, M_5, and M_6. While the outputs of the main and feed-through amplifiers are connected to each other, their input terminals are cross-connected to each other. A resonant circuit implemented by one inductor L_t and one capacitor C_var is inserted between the drain node of $M_{3,4}$ and the source node of $M_{5,6}$. C_{var} is a varactor and its capacitance value is controlled by voltage control V_{cont}, that tunes the frequency response of the tank.

The active phase shifter functions as a second-order all-pass network when $gm_{3,4}$ is about two to three times greater than $gm_{1,2}$. The advantage of the all-pass network-based phase shifter is its lower sensitivity to insertion phase variation. This feature is beneficial for large bandwidth circuits since its frequency response does not depend on the insertion phase.

Y-parameters are driven Based on Figure 2.19, the phase shifter small-signal model to derive the Y-parameter. The $Y_{21}(s)$ of the phase shifter can be defined as the ratio of the small-signal output current to input voltage with the ac grounded output terminals. The $Y_{21}(\omega)$ of the phase shifter can be defined as,

$$Y_{21}(\omega) = g_{m1}\frac{-\omega^2 + \omega_a^2 - j\omega\omega_a\sqrt{\frac{L_t}{C_a}}g_{m6}(1 + \frac{1}{g_{m6}R_a})}{-\omega^2 + \omega_a^2 + j\omega\omega_a\sqrt{\frac{L_t}{C_a}}g_{m6}(1 + \frac{1}{g_{m6}R_a})} \tag{2.29}$$

where ω_a represents $\frac{1}{\sqrt{L_t C_a}}$, with the phase response of

$$< Y_{21}(\omega) = -2tan^{-1}(\frac{\omega\omega_a}{Q(\omega_a^2 - \omega^2)}) \tag{2.30}$$

The S_{21} phase response can be also derived by transforming the Y-parameters to

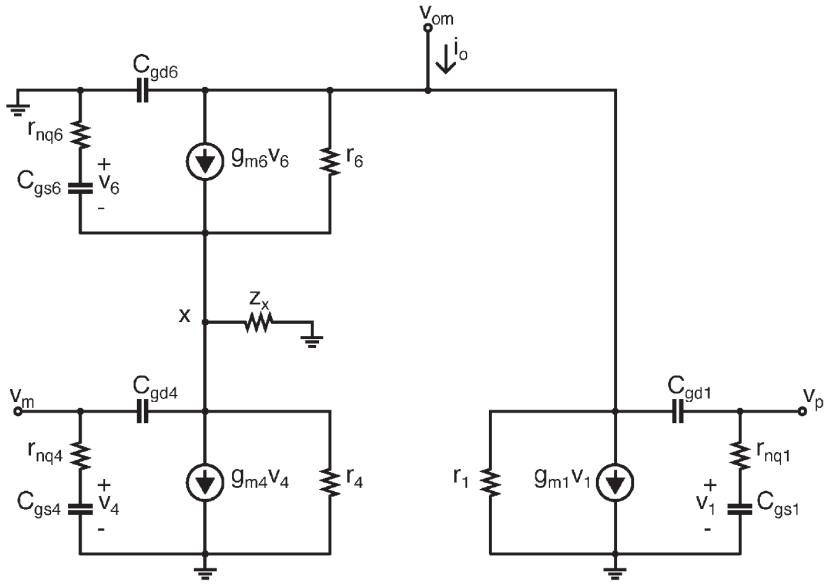

Figure 2.19: The phase shifter small-signal model to derive the Y-parameter[12]

S-parameters [12].

2.4.3 Switch-typed phase shifter with integrated VGA

Another topology that is mainly used for RF phased-array systems is switch-type phase shifter integrated with a low phase-variation variable gain amplifier (VGA). The main challenge associated with RF phase shifting is the accuracy of phase control. Using the phase compensation technique, the gain-compensated VGA can provide appropriate gain tuning with almost constant phase characteristics, thus greatly reducing the phase tuning complexity in a phased-array system.

When the phase shifter provides different phase-shifting states, the loss will be different for each state. Consequently, the VGA must provide different gain compensation for different phase-shifting states. Nevertheless, the gain tuning of the VGA will introduce additional phase variations for the whole phased-array system. Hence,the phase-compensated VGA is designed to compensate the phase variation

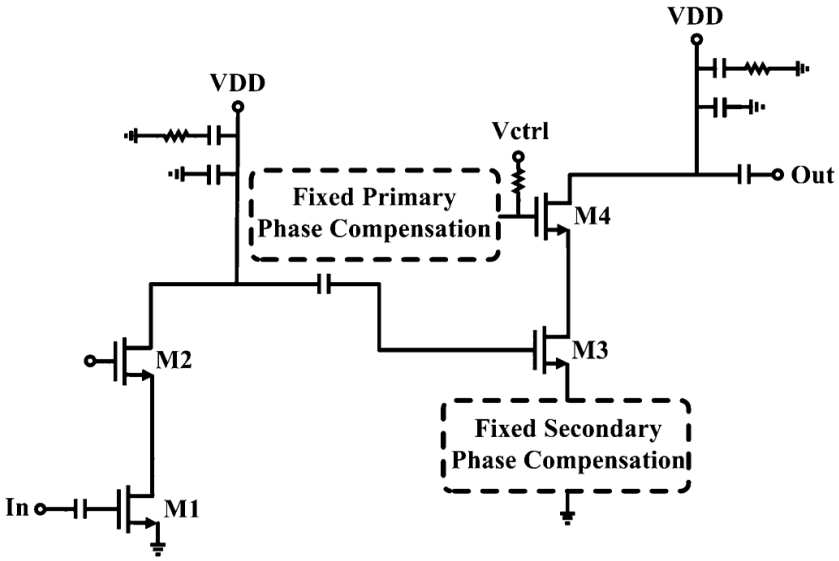

Figure 2.20: Fixed primary and secondary phase compensation technique[13]

for different gain-compensation states. For the low phase-variation VGA, a simplified phase-compensation technique can be used shown in Figure 2.20, fixed primary and secondary phase compensation technique. This technique requires only one auto gain control in the self-calibration phased-array system, which is using fixed phase-compensation blocks to simplify the control complexity. With the low phase-variation VGA and the high-resolution phase shifter, the phased array is suitable for the applications of satellite communications and radar systems [13].

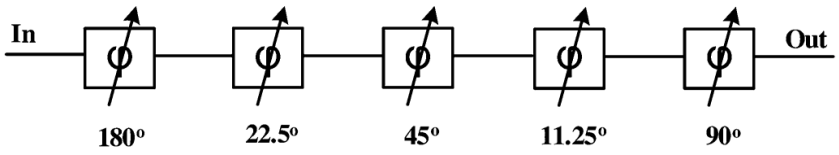

Figure 2.21: Schematic of the 5-bit switch-type phase shifter[13]

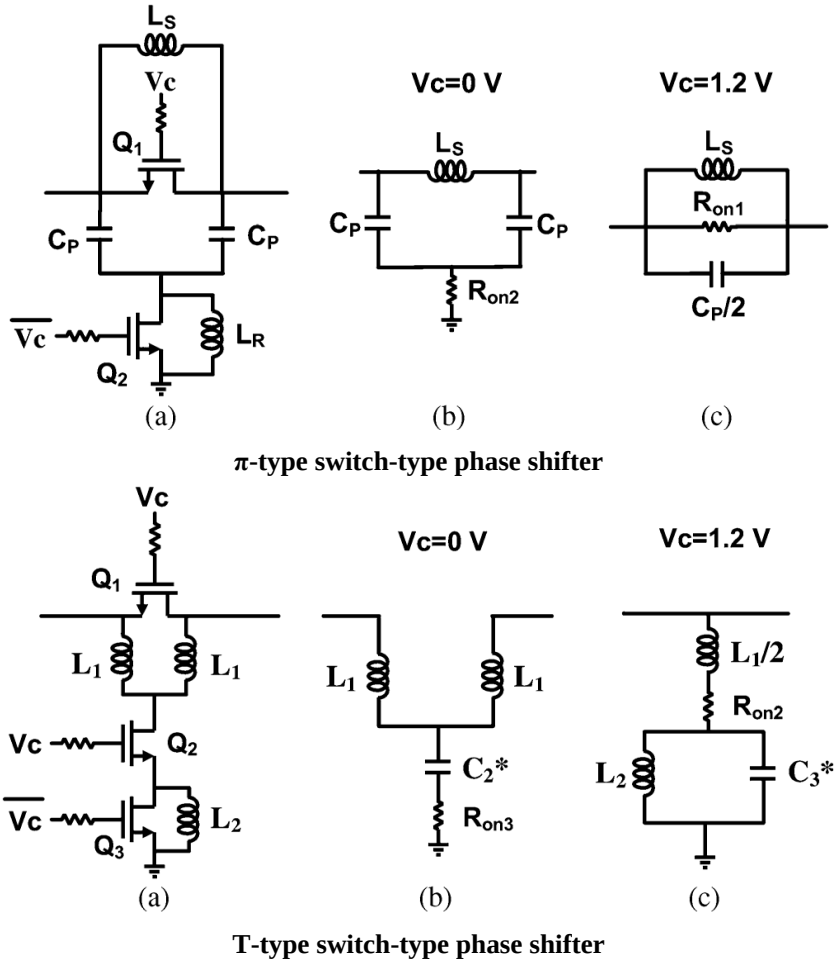

Figure 2.22: (a)π-type switch-type phase shifter. (b) Equivalent circuit when V_c= 0V. (c) Equivalent circuit when V_c=1.2 V. (a)T-type switch-type phase shifter. (b) Equivalent circuit when V_c= 0V. (c) Equivalent circuit when V_c=1.2 V.(* C_2 and C_3 are the parasitic capacitors of transistors Q_2 and Q_3)[13]

The sequence of phase-shifting stages is an important design consideration for the low phase-variation phase shifter. In order to achieve better EVM performance, the multiple phase-shifting stages has been chosen to be 5 bits, as shown in Figure 2.21, the schematic of the 5-bit switch-type phase shifter. However, individual stage performance could be affected by adjacent stages due to loading effects. The small phase-shifting stage (i.e., 11.25 and 22.5) has more mismatch and loading effect than

the large phase-shifting stage. Hence, the small phase-shifting stages are placed in between the large phase-shifting stages to reduce loading effects from adjacent stages and to achieve high phase linearity. Group delay is an important parameter that describes the phase linearity of transfer networks. For the phased-array systems, low phase variation, or low group-delay deviation, is required over the entire bandwidth to ensure the signal integrity during transmission. There are several ways to realize a switch-type phase shifter. π-type and T-type switches are two of the most popular topologies, shown in Figure 2.22 (a)π-type switch-type phase shifter. (b) Equivalent circuit when V_c= 0V. (c) Equivalent circuit when V_c=1.2 V. (a)T-type switch-type phase shifter. (b) Equivalent circuit when V_c= 0V. (c) Equivalent circuit when V_c=1.2 V.(* C_2 and C_3 are the parasitic capacitors of transistors Q_2 and Q_3). To choose the appropriate topology for designing a low group-delay deviation phase shifter, the insertion phase and group-delay deviation of the π-type and T-type switch-type phase shifter for a 90 phase-shifting stage are compared and T-type switch-type phase shifter has low group delay and low phase deviation.

As shwon in Figure 2.23, the schematic of the 60-GHz 5-bit phase shifter and low phase variation VGA, to reduce loading effects from adjacent stages, a 360 ° phase shift is implemented by cascading 180 ° , 22.5 ° , 45 ° , 11.25 ° , and 90 ° , respectively. For low insertion loss, the input transistor switches have body connected to source. To achieve a compact chip area and to minimize the influence caused by process variation, the inductors are implemented with microstrip lines.

The phase-compensation technique is achieved by utilizing the phase-compensation capacitor C_x and source degeneration inductor L_E . Due to the millimeter-wave (MMW) frequency, all the CMOS parasitic effects of C_x and L_E need to be considered carefully. C_x has a primary effect on phase-variation compensation, while L_E helps to reduce phase variation.

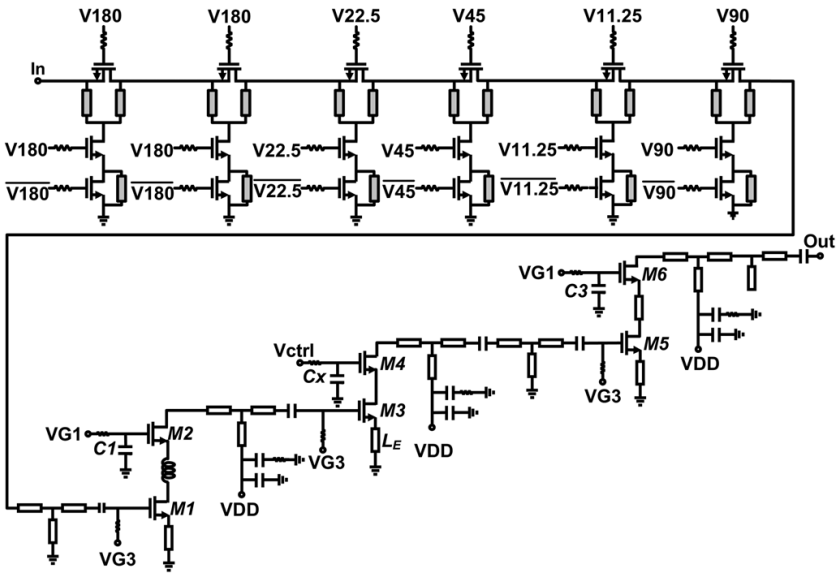

Figure 2.23: Schematic of the 60-GHz 5-bit phase shifter and low phase variation VGA [13]

When the control voltage,V_{ctrl} , of the VGA is adjusted, the transconductance g_m and matching conditions will also be varied accordingly. Therefore, the gain tuning stage is designed in the second stage to minimize the impact on input and output return loss. The gain tuning and phase compensation stage is composed of a common-source (CS) and a common-gate (CG) cascode topology. The equations of maximum and minimum S_{21} and the gain tuning range of the VGA are given by

$$S_{21,max} = 20log(g_{m,max}Z_L)dB \tag{2.31}$$

$$S_{21,min} = 20log(g_{m,min}Z_L)dB \tag{2.32}$$

$$\Delta S_{21} = 2 - log(\frac{g_{m,max}}{g_{m,min}}) \tag{2.33}$$

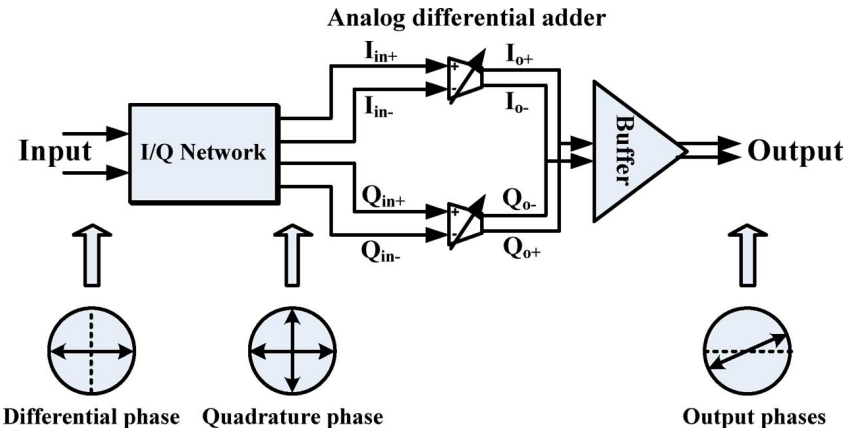

Figure 2.24: Building blocks of the 360° vector-sum phase shifter[14]

It is worth noted that the gain tuning range in 2.33 is determined by transconductance g_m , which is independent of load impedance. Since a constant gain at different phase-shifting states is required in the phased-array system, the gain tuning of the VGA should be wide enough to cover the loss variation of a phase shifter [13].

2.4.4 Vector-sum phase shifter

Another phase shifter topology that is mainly applied in phase array system, is active vector-sum technique. In the vector sum method, after the generation of the in-phase/quadrature signal by the I/Q network, the output phase is adjusted by adding them with appropriate I/Q amplitudes and polarities. A precise quadrature signal generation is therefore an important circuit element of the active approach for exact phase shifting. Unfortunately, the generation of quadrature signals using passive couplers/dividers is not an attractive method on account of their narrow bandwidth [14].

Building blocks of the 360° vector-sum phase shifter is illustrated in Figure 2.24. A differential input signal is split into quadrature phased - and -vector signals using an I/Q network, which also provides differential 50 Ω matching with the previous

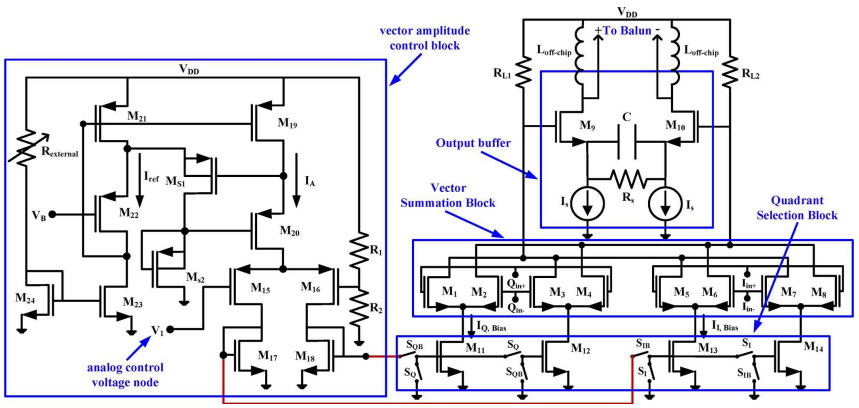

Figure 2.25: The phase shifter differential vector summing schematic [14]

stage. This stage, which is composed of three all-pass filters, generates very low quadrature phase error. In order to generate an interpolated output signal, a differential adder composed of two Gilbert-cell type signed variable gain amplifiers (VGAs) is used. It adds the I- and Q-inputs from the I/Q network with proper polarities and amplitude weights, giving an output signal with a magnitude of $\sqrt{I_0^2 + Q_0^2}$ and phase of $tan^{-1}(\frac{Q_0}{I_0})$. For phase resolution, the different amplitude weightings of each input of the adder can be accomplished by changing the gain of each VGA differently. A differential pair does this work by controlling the bias current of the VGAs.

Figure 2.25 shows the phase shifter differential vector summing schematic that adds the I- and Q-signal together in the current domain at the output node, synthesizing the required phase. The analog differential adder is composed of three blocks. The core of the network is the vector summation block where the vectors are added and it consists of eight transistors M_{1-8}. The second block is the quadrant selection block that switches the tail current from I-side to the Q-side to provide the 180 ° phase state. S_I and S_Q switches determine the quadrant selection. The voltage gain at the phase shifter output is approximated according to the square-law gain

dependency on bias current in CMOS as

$$A_v = 20log(k\sqrt{I_I + I_Q}) \ \ (dB) \tag{2.34}$$

Where k = constant and, and the output phase θ_{out} is determined by the I/Q current ratio given by

$$\theta_{out} = tan^{-1}\sqrt{\frac{I_Q}{I_I}} \ \ (deg) \tag{2.35}$$

In order to obtain the desired phases, the Vector amplitude control block is used to change the tail current amplitudes. In this block, a differential pair consisting of PMOS transistors M_{15} and M_{16} is biased with a supply current, I_A. A DC control voltage V_1 is applied to the gate of M_{15} to fully steer the I_A current from transistor M_{15} to M_{16} which are also the I and Q current branches, respectively.

One major advantage of the active phase shifter is the dependence of output phase on I-and Q-path bias current ratio rather than the absolute value of the current, so the ratio of I/Q will track temperature variations, resulting in constant phase versus temperature [14].

2.5 The proposed active phase modulator design of the polar transmitter for WLAN 802.11 a application

The proposed phase modulator block diagram is shown in Figure 2.26. The phase modulator is designed and fabricated in 180 nm CMOS technology. The core of the phase modulator is an active phase shifter that is digitally controlled by 6-bit phase information. The differential quadrature (I and Q) input signals of the phase shifter are created by a divider block that divides the local oscillator (LO) frequency of 1.6 GHz by two. The differential phase signal at 800 MHz is then up-converted to 2.4

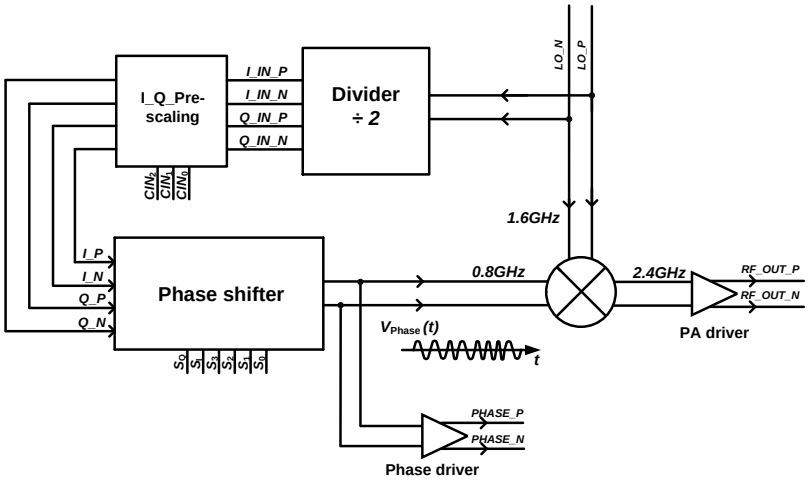

Figure 2.26: The proposed phase modulator block diagram

GHz by an active mixer with the local frequency at 1.6 GHz.

To reduce the local oscillator pulling effect, Local oscillator and the RF frequencies should be made sufficiently far from each other. So, the LO frequency is chosen to mix with half of its frequency at 0.8 GHz to result in 2.4 GHz RF frequency. Figure 2.27 shows the mixing of an LO output with half of its frequency to reduce the LO pulling for the up-conversion architecture. The targeted RF frequency is set to 2.4 GHz to be compatible with many of the wireless standards (i.e IEEE 802.11 a/g).

The divider by two generates differential quadrature signals at 0.8 MHz. The pre-scaling block controls the level of these differential qudrature signals and makes more accurate sinusoidal I and Q signals at the input of the phase shifter. It will be shown later on that the linearity of the phase shifter strictly depends on the input signal power level (i.e P_{1dB}). Three control bits control the voltage division of capacitances in pre-scaling block (C_{IN0} C_{IN1} C_{IN2}). The phase shifter creates a differential constant phase modulated signal based on the 6-bit of phase information

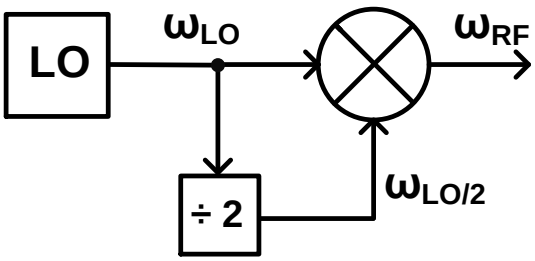

Figure 2.27: Mixing of an LO output with half of its frequency to reduce the LO pulling

(S_Q S_I S_3 S_2 S_1 S_0). For the system analysis of the phase modulator, the 6-bit phase information is applied to the phase shifter as 64 QAM to make the phase modulated signal that will be discussed in more detail in next section. A CML driver matched to 50Ω, is designed to monitor the output of the phase shifter before the up-conversion. The constant phase modulated signal is then up-converted by an active mixer with LO frequency of 1.6 GHz to generate the RF frequency at 2.4 GHz. The output signal at 2.4 GHz is then applied to a driver, matched to 50Ω, for measurements. This driver can also be considered as the PA pre-driver. The circuit design and fabrication of the phase modulator building blocks will be explained in detail in the following sections.

3. PHASE MODULATOR DESIGN AND IMPLEMENTATION

3.1 Phase modulator system design and simulation

The phase modulator system analysis is designed to find out the system response to real 6-bit phase information of OFDM with 64 QAM modulation. The 6-bit phase information is extracted as shown in Figure 3.1,64 QAM transceiver block diagram in Simulink. This system architecture is originally designed to monitor the transmitted and the received data, assuming a multipath Rayleigh fading channel effect. However for phase modulation system simulation, the 64 QAM phase information is extracted from the transmitter part of this system before the OFDM modulation block.

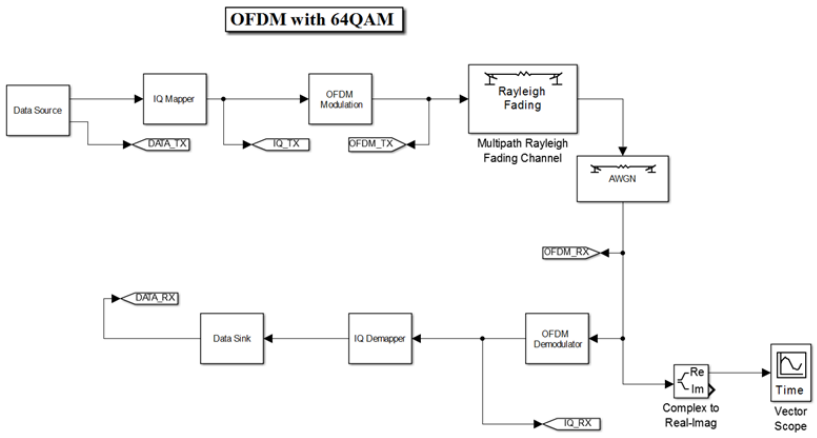

Figure 3.1: 64 QAM transceiver block diagram in Simulink

As shown in the Simulink block diagram, a data source block generates random data for I/Q mapper block to map the I and Q data 64 QAM constellation. Figure 3.2 shows the 64 QAM data source block diagram. Random integer generator block

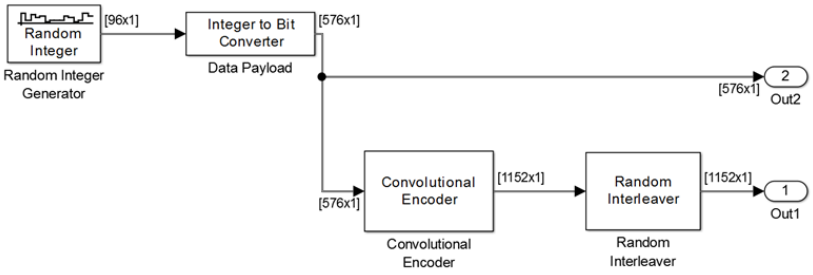

Figure 3.2: 64 QAM data source block diagram

generates random uniformly distributed integers in the range $[0, M-1]$ for the M-ary number. M in this case is 32 with 96 samples per frame that creates [96x1] frame-based outputs. Each of the generated integers are then converted to bits. Number of bits per integer is 6, so the output bit data becomes [576x1]. The convolutional encoder block encodes a sequence of binary input vectors to produce a sequence of binary output vectors. The convolutionally encoded binary data in the output of this block has the [1152x1] vector which is double of the input vector to further create I and Q data. Eventually, the random interleaver block rearranges the elements of its input vector using a random permutation.

The generated data is then applied to I/Q mapper, shown in Figure 3.3, the I/Q mapper block diagram. The purpose of this block is to generate 64 QAM baseband data. The amplitude and phase information of 64 QAM modulator are shown in Figure 3.4, 64 QAM constellation generated by Simulink. Finally, the phase information is extracted from the I and Q constellation.

3.1.1 64 QAM phase data

The extracted phase information is then applied to an ADC in Cadence to create digital 6 bit information. Since the phase modulator is designed to be compatible

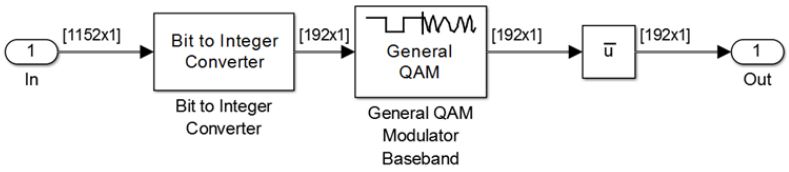

Figure 3.3: I/Q mapper block diagram

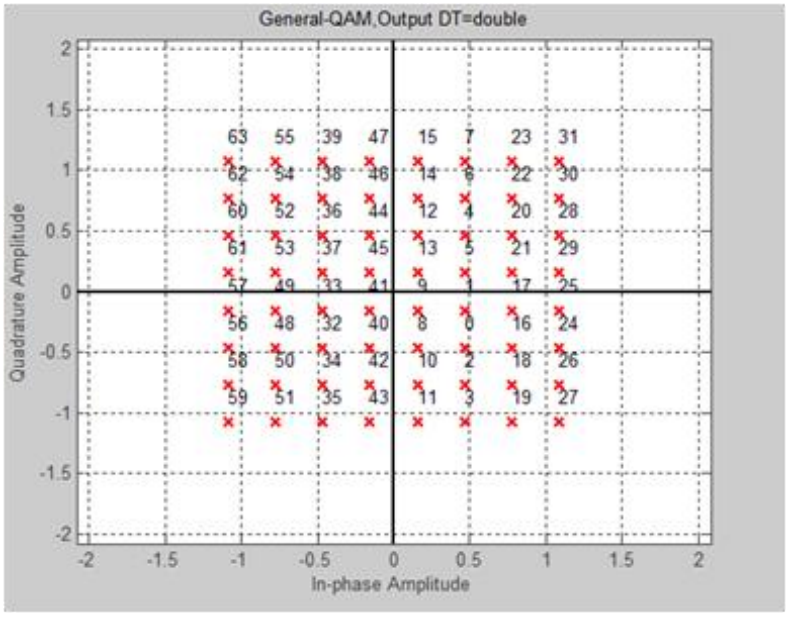

Figure 3.4: 64 QAM constellation generated by Simulink

with the IEEE802.11a standard, the highest data rate of the standard is being used in simulation to examine the reliability of the system. The IEEE802.11a standard employs 52 OFDM sub-carriers that 48 of them are for the data. Each of these 48 sub-channels with 64 QAM data and highest data rate of 54 Mb/s, carries the data rate of (54 Mb/s)/48/6 = 188 kb/s $\approx$ 200 kb/s. The maximum data rate of 200 kb/s

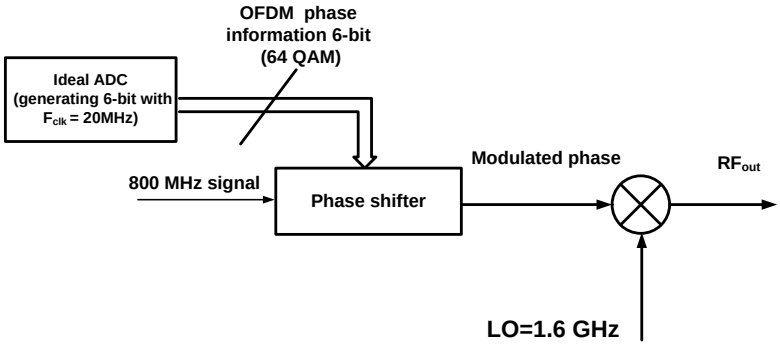

Figure 3.5: Phase modulator system test set up with 6 bit phase information of 64 QAM

is applied as the clock frequency of the ADC in cadence. Figure 3.5 shows the phase modulator system test set up with 6 bit phase information of 64 QAM.

Figure 3.6 illustrates transient signals of 6-bit phase information of 64 QAM., outputs of the ADC, applied to the phase shifter switches (S_Q S_I S_3 S_2 S_1 S_0). These 6 bits are changing with 200 kHz data rate.

3.1.2 6-bit consecutive phase data

As can be seen from the 64 QAM constellation, 6-bit phase information of 64 QAM is gray coded (i.e. two successive values differ in only one bit). To simulate the phase shifter with consecutive bits, another approach is applied to create the 6-bit phase data. The method is to apply 6 bit generator sources with the clock frequency of 200 kHz. So the (S_Q S_I S_3 S_2 S_1 S_0) switches are turning on and off with 200 kHz frequency.

Table 3.1, shows the generated 16 phase states of a quadrant based on the S_3 S_2 S_1 S_0, the bit stream applied to the input switches of the phase shifter and the corresponding phase at the output of the phase shifter for each case. The phase shifter is designed to have the phase step of 5.625 °. Four low significant bits of the

Table 3.1: Generated 16 phase states of a quadrant based on the S_3 S_2 S_1 S_0

S_3	S_2	S_1	S_0	Phase
0	0	0	0	0
0	0	0	1	5.652°
0	0	1	0	11.25°
0	0	1	1	16.875°
0	1	0	0	22.5°
0	1	0	1	28.125°
0	1	1	0	33.75°
0	1	1	1	36.375°
1	0	0	0	45°
1	0	0	1	50.625°
1	0	1	0	56.25°
1	0	1	1	61.875°
1	1	0	0	67.5°
1	1	0	1	73.125°
1	1	1	0	78.75°
1	1	1	1	84.375°

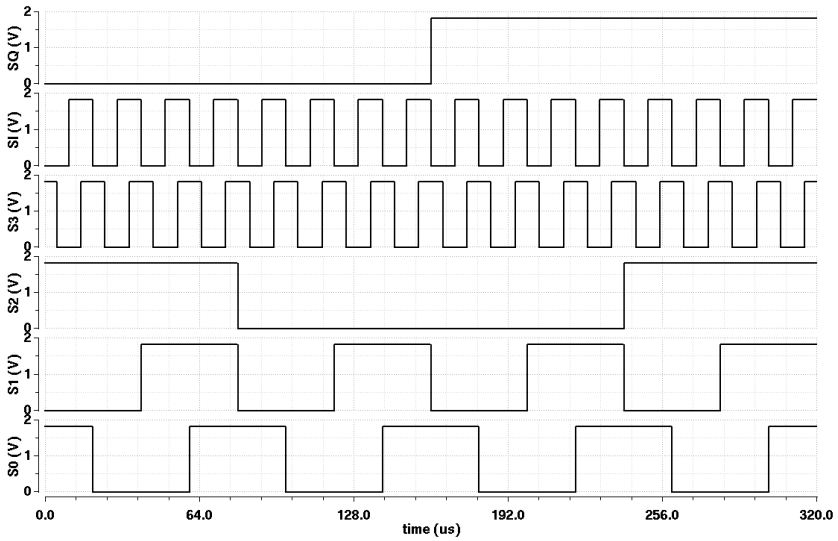

Figure 3.6: Transient signals of 6-bit phase information of 64 QAM

Table 3.2: Quadrant selection with S_Q and S_I switches

S_Q	S_I	Quadrant
0	0	1
0	1	2
1	1	3
1	0	4

phase information corresponding to S_3 S_2 S_1 S_0 switches of the phase shifter, specify any of the 16 possible phases with the step of $\frac{90^\circ}{2^4} = 5.625^\circ$. Two most significant bits of phase information corresponding to $S_Q S_I$ switches change the quadrants (changing the sign of the I and Q) to cover all the phases in 360°. Table 3.2 shows the quadrant selection with S_Q and S_I switches and the relationship between the state of S_Q and S_I switches.

3.2 Block diagram of the phase modulator design

As shown in the phase modulator block diagram, the differential quadrature signal at 0.8 MHz is generated by the divider and is applied to the input of the phase shifter. The phase shifter created the corresponding output phase based on the digital 6 bit phase information. The differential output phase is then mixed with the LO at 1.6 GHz to generate the RF output signal at 2.4 GHz. The circuit design of the building blocks of the phase modulation path will be explained in the following.

3.2.1 6-bit active phase shifter design

The proposed active phase shifter adopts an in-phase/quadrature phase (I/Q) network and exploit phase interpolation between the quadrature signals by adding them with appropriate I and Q amplitudes and polarities so as to synthesize the required phase [30]. The block diagram the 6-bit active phase shifter is presented in Figure 3.7. The differential quadrature signals are created by the divider by two,

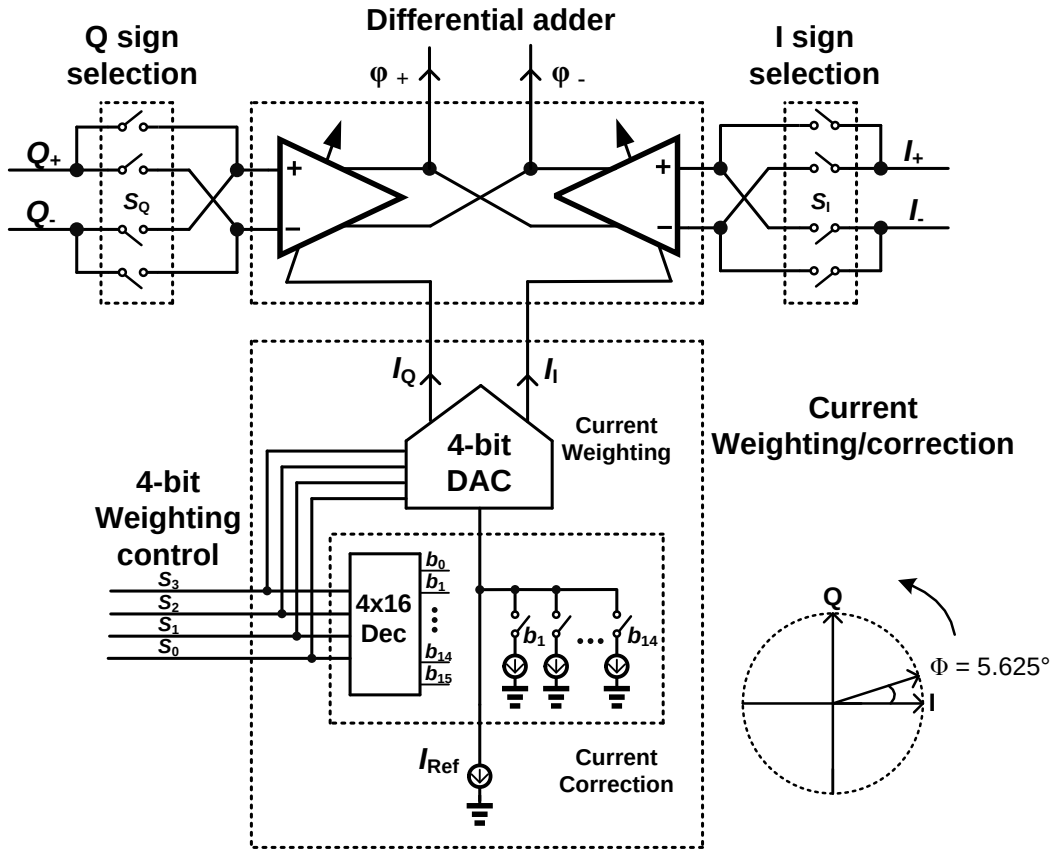

Figure 3.7: Block diagram the 6-bit active phase shifter

since a differential system provides a more convenient way of 360 ° phase rotation than a single-ended design.

A differential signed-adder with gain control and a current DAC are the core blocks of the phase shifter. In addition to these two main blocks, a current coefficient block is designed to control the reference bias current of the DAC for each phase. Four least significant bits of the 6-bit phase control S_3 S_2 S_1 S_0, determine the current weightings of each I and Q branches with the phase step of 5.625 °. Two most significant bits of phase command (S_Q S_I) specify the location between four

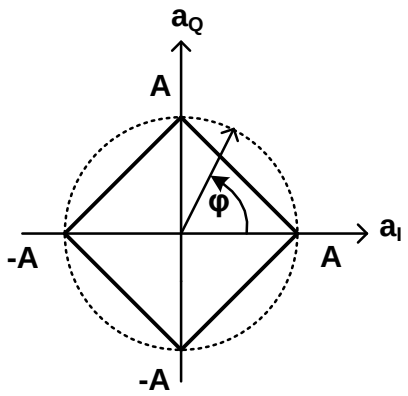

Figure 3.8: Linear vector summing technique

quadrants. Therefore, the I +/- and Q +/- currents are added to create phases according to the digital phase input. The key function of the proposed phase shifter is that it generates the output phase with constant amplitude. Although the phase shifter design is based on linear current weighting method that doesn't offer a constant output, the output phase signal stays constant with the proposed technique that changes the reference bias current of the DAC according to each state. Figure 3.8 [38] shows the linear vector summing technique, used in our design, creates the current vectors for I_I and I_Q in way to create $|I_I| + |I_Q| = B$ that the B is a constant value. However, the vector summation of $I_I + I_Q$ doesn't stay constant and leads to the square instead of the circle. So, to have a constant output, the relation ship between two currents should be $\sqrt{I_I^2 + I_Q^2} = A$ that A remains constant. To compensate for the reduction in the output amplitude due to linear vector summation of I and Q currents, a current coefficient block is designed to change the reference bias current of the DAC, based on the difference between the output phase amplitude and A for the 14 phases within the quadrants. The building blocks of the phase shifter

will be explained in the following sections.

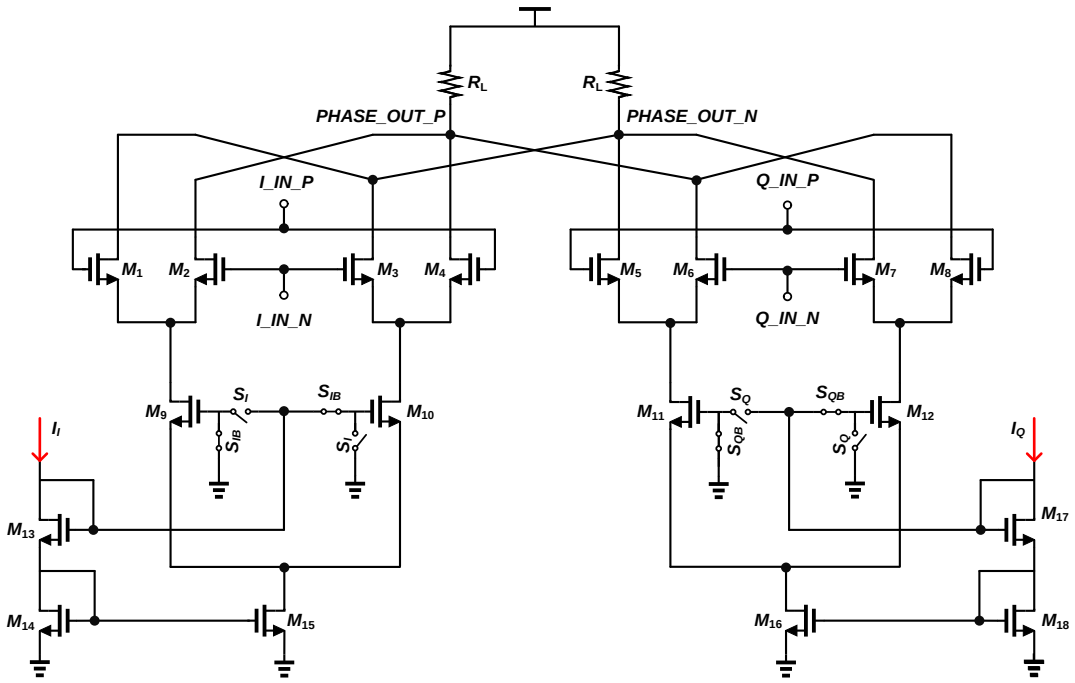

Figure 3.9: Differential signed adder (I/Q)

3.2.1.1 Differential adder

Two Gilbert-cells are merged at the output to sum I and Q signals in current mode, shown in the Figure 3.9 the differential signed adder (I/Q). The tail current generated from the 4-bit current-mode differential DAC, is switched by S_Q and S_I to provide 180° phase state (changing the sign of I and Q). The variable gain function is done by changing the bias current using the current-mode differential DAC. M_{13} with $M_{9,10}$ in I side and M_{17} with $M_{11,12}$ in Q side are the cascoded transistors of the current mirror with $6 \times \frac{2um}{180nm}$ and $30 \times \frac{2um}{180nm}$ to generate $\times 5$ current. The

lower transistors M_{14} with M_{15} in I side and M_{18} with M_{16} in Q side sizings are $12 \times \frac{2um}{500nm}$ and $60 \times \frac{2um}{500nm}$. The lower transistor lengths are chosen to be 500 nm to offer more accurate current mirrors. I_{BIAS} and Q_{BIAS} reference currents are generated by the DAC based on the current weighting coefficients according to 4-bit digital phase data.

The voltage gain at the phase shifter output is approximated as

$$A_v = \sqrt{\mu_n C_{ox} \frac{W}{L}(I_I + Q_Q)} \times R_{out} \tag{3.1}$$

and the output phase is determined by the control DAC I/Q current ratio of

$$\Theta_{out} = tan^{-1}\sqrt{\frac{I_Q}{I_I}} \tag{3.2}$$

3.2.1.2 4-bit current DAC

The main block of current weighting part is the DAC that generates binary weighted currents for each phase state. Based on the 6-bit digital phase information data S_Q S_I S_3 S_2 S_1 S_0, 64 phase shifts with step of 5.625 ° is created. As mentioned earlier, S_Q S_I switches in the differential adder determine the sign of I and Q current vectors. The other four bits specify the weight of I and Q currents.

As shown in Figure 3.10, 4-bit current DAC (controlled with S_3 S_2 S_1 S_0), four current mirrors associated with each of S_3 S_2 S_1 S_0 switches are weighted binary and are set such that $I_I + I_Q = constant$ for linear vector summing. To have more accurate portions for I and Q currents to cover all the phases up to 360 °, a constant $\frac{1}{2} \times I_{REF}$ current branch is added to I and Q bias current mirrors. This also improves the settling time, since a zero tail current is never applied to any of the I or Q branches [39]. The reference current mirror transistor size is $4 \times \frac{2um}{500nm}$ and again 500 nm

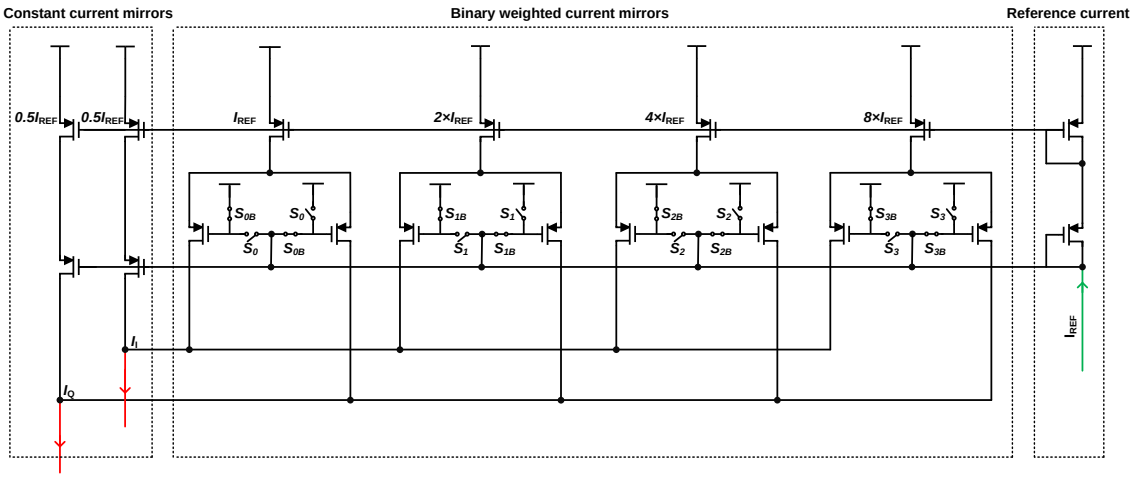

Figure 3.10: 4-bit current DAC (controlled with S_3 S_2 S_1 S_0)

length is chosen for the mirror transistors to generate more accurate currents.

3.2.1.3 DAC current source correction block

Due to the linear vector summing topology of this design, the output voltage of the phase shifter doesn't stay constant and there is a reduction in output phase signal amplitude for the phases in between the quadrants. Since the $I_I + I_Q = constant$ and the vector summation of I and Q currents results in the amplitude path on side of the square instead of the circle as shown in Figure 3.8. To have the constant output amplitude, I_I and I_Q must fulfill the equation $\sqrt{I_I^2 + I_Q^2} = constant$, that leads to the circle in the vector sum diagram.

A current correction circuit is designed to increase the DAC input reference current for the cases in which the resultant amplitude reduces due to linear vector summing (14 phases, when not considering 0 and 90 °). As shown in Figure 3.11 DAC reference current weighting correction block, for each phase that specified by S_3 S_2 S_1 S_0 code, the decoder makes one of the 14 current correction branches ON.

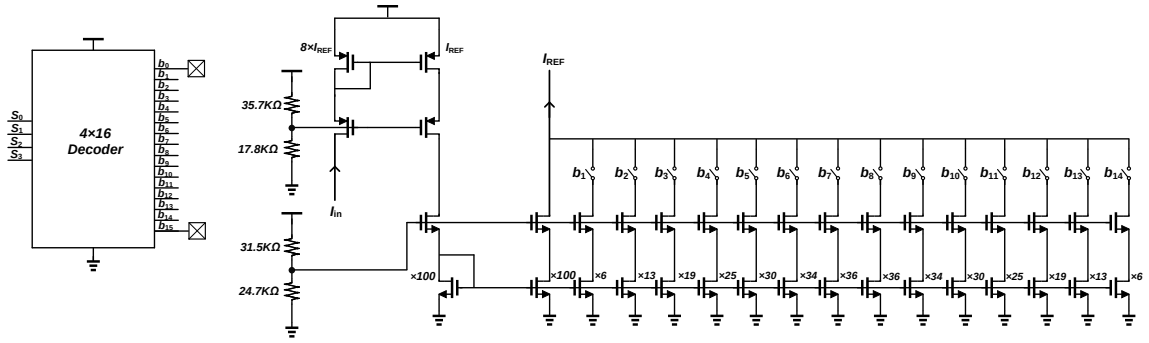

Figure 3.11: DAC reference current weighting correction block

Table 3.3: DAC reference current weighting coefficients

$I_Q(uA)$	$I_I(uA)$	$\sqrt{I_I^2+I_Q^2}(uA)$	S_i	D_i	C_i	A_i	Resultant (uA)	error
7.52	229.7	229.82	1000	0	0	0	229.82	0
22.5	215.1	216.27	1063	63	6	13.78	230.06	0.239
37.46	200.4	203.87	1127	127	13	28.11	231.99	2.16
52.41	185.8	193.05	1190	190	19	38.73	231.79	1.96
67.35	171.1	183.88	1250	250	25	48.26	232.14	2.32
82.27	156.4	176.72	1301	301	30	55.16	231.88	2.064
97.16	141.6	171.73	1338	338	34	60.08	231.81	1.99
112	126.8	169.18	1358	358	36	61.82	231	1.18
126.8	112	169.18	1358	358	36	60.90	230.08	0.26
141.6	97.16	171.73	1338	338	34	57.52	229.25	-0.56
156.4	82.27	176.72	1301	301	30	51.51	228.24	-1.58
171.1	67.35	183.88	1250	250	25	44.18	228.06	-1.76
185.8	52.41	193.05	1190	190	19	34.93	227.99	-1.83
200.4	37.46	203.87	1127	127	13	25.09	228.97	-0.85
215.1	22.5	216.27	1063	63	6	12.23	228.5	-1.31
229.7	7.52	229.82	1000	0	0	0	229.82	0

The correction current is then added to the reference current to result in a current that compensates for the reduction in the output amplitude. To find out the excess current that needs to be added to the I and Q currents in each 14 cases, the am-

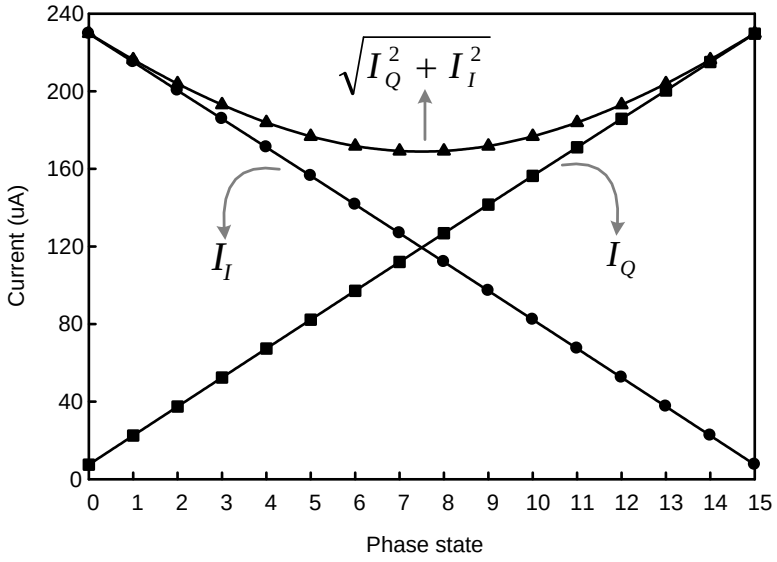

Figure 3.12: I_I and I_Q currents and the resultant amplitude of the summation

plitude of the summation of I and Q currents are calculated as shown in Table 3.3, DAC reference current weighting coefficients. Then, the first (or last) amplitude is set as the reference amplitude value and the sqrt coefficient in the Table 3.3 is then calculated by dividing each current amplitude by the reference current amplitude, times 1000. So, the first and last sqrt coefficient will result in 1×1000. The difference between the amplitude of the 14 phases and first phase determines the current correction coefficient for each case as shown in the last column of the Table 3.3.

Figure 3.12 shows the I_I and I_Q currents and the resultant amplitude of the summation $I_I + I_Q$ in a quadrant.It can be seen that the current amplitude has the expected reduction due to the vector summation. To formalize the correction process, current amplitude for each of 16 phase states of a quadrant can be expressed as $\sqrt{II_i^2 + IQ_i^2}$, $i = 0 \rightarrow 15$. So, the sqrt coeff, S_i and the difference, D_i can be

calculated as

$$S_i = \frac{\sqrt{II_0^2 + IQ_0^2}}{\sqrt{II_i^2 + IQ_i^2}} \times 1000 \tag{3.3}$$

$$D_i = S_i - S_0 \quad i = 0 \rightarrow 15 \tag{3.4}$$

Also, a current coefficient, C_i is set for each state, proportional to D_i

$$C_i \propto \frac{D_i}{10} \quad i = 0 \rightarrow 15 \tag{3.5}$$

and the added current is obtained by

$$A_i = \frac{\sqrt{II_0^2 + IQ_0^2} \times C_i}{100} \quad i = 0 \rightarrow 15 \tag{3.6}$$

The reference current for DAC is set to $15uA$, so the $I_{in} = 150uA$ that after division by $\frac{1}{8}$, it results in $15uA$. The main branch coefficient of I_{REF} is set to 100 to have decimal values for the correction branch coefficients.

Figure 3.13 shows the current amplitude with and without the correction block. The corrected amplitude can be found as

$$\sqrt{II_i^2 + IQ_i^2} + A_i = constant \quad i = 0 \rightarrow 15 \tag{3.7}$$

That is approximately constant with the error calculated in the last column of table 3.3 as the following, shown in Figure 3.14, the corrected current amplitude error.

$$error = (\sqrt{II_i^2 + IQ_i^2} + A_i) - \sqrt{II_0^2 + IQ_0^2} \quad i = 0 \rightarrow 15 \tag{3.8}$$

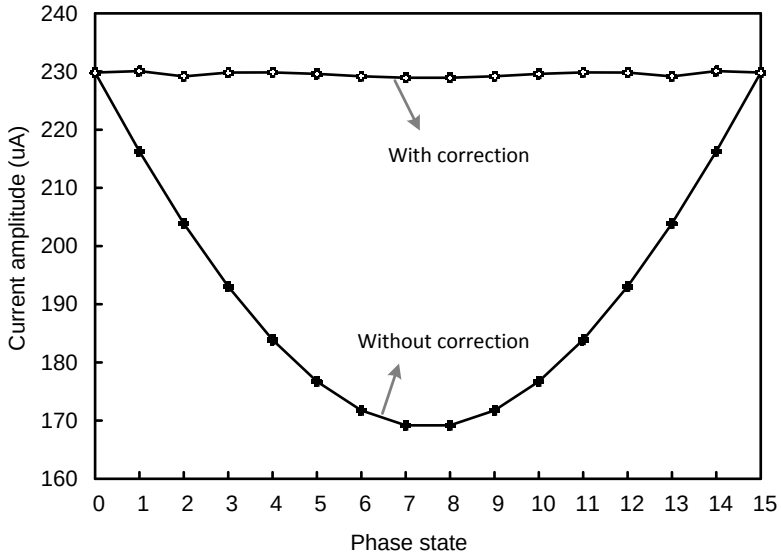

Figure 3.13: Current amplitude with and without the correction block

The phase shifter output is monitored by the phase output CML driver shown in Figure 3.15 matched to 50Ω. The CML input current is 1.2 mA that gets multiplied by $\times 10$ to create accurate sinusoidal signal at the output of the driver. The linearity of the phase driver is $IIP_3 = 3\ dBm$ from the two tone test.

3.2.2 Active mixer design

The active differential Gilbert-cell mixer is chosen to upconvert the 800 MHz phase modulated signal, shwon in Figure 3.16, the active mixer schematic. The local frequency is at 1.6 GHz to result the RF frequency at 2.4 GHz. The output load of the mixer is an LC band pass filter designed at 2.4 GHz to have a clear output at this frequency. For better linearity and have more headroom the pseudo differential architecture is applied in the design of the mixer. The differential IF input of the mixer at 800 MHz is ac coupled and the bias point is set by the bias circuit. The

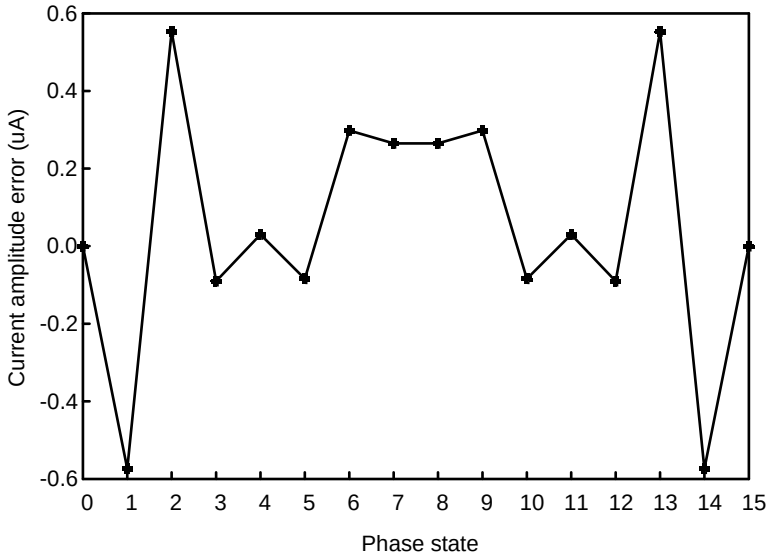

Figure 3.14: The corrected current amplitude error

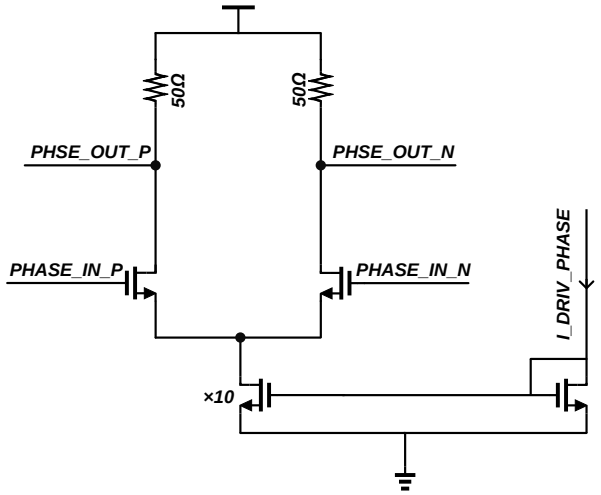

Figure 3.15: Phase output CML driver

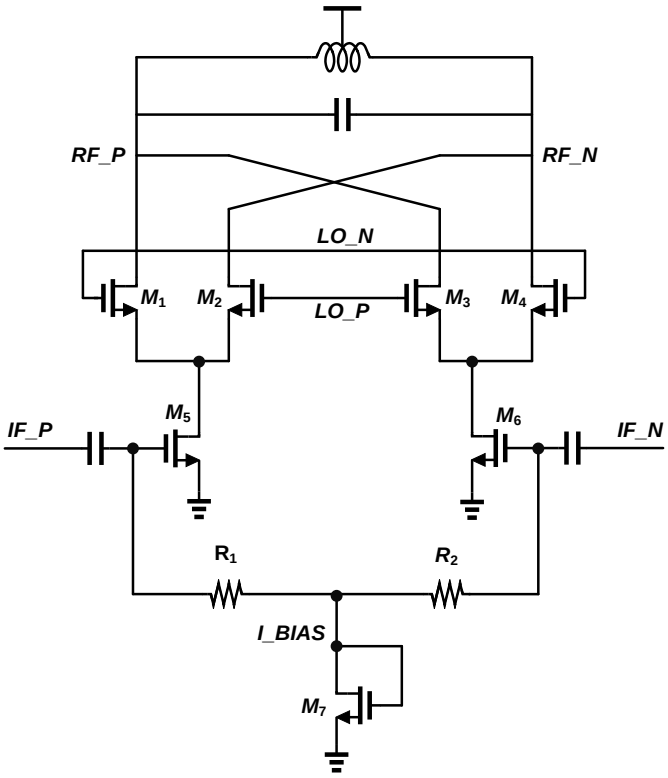

Figure 3.16: The active mixer schematic

Table 3.4: Differential inductor sizings

Outer dimension	Spiral Width	Number of turns	Spacing
175 um	3.24 um	4	5 um

reason is that the driver at the output of the phase shifter doesn't affect the input of the input signal of the mixer. Also, in the design of the mixer, to have better linearity and headroom, sizing of M_5 and M_6 transistors are chosen to result in high V_{DS}.

The differential inductor with the center tap connected to V_{DD} value is set to 3.9 nH with the sizings shown in Table 3.4 differntial inductor sizings. The capacitance

value is created by the parallel combination of two 533 fF MIM capacitors with the plates sizing of $W = L = 16.22um$.

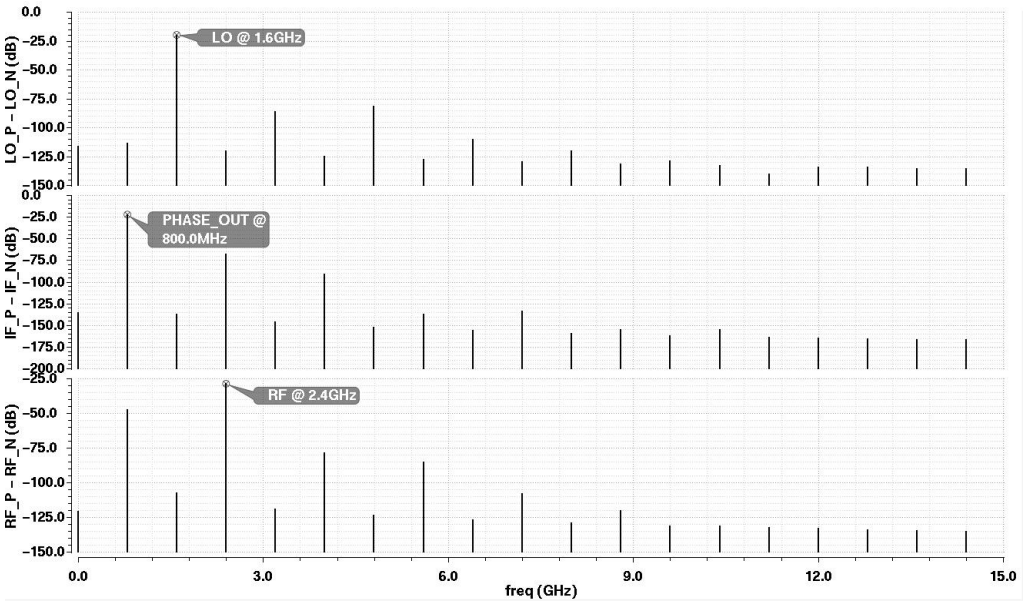

Figure 3.17: Active mixer PSS simulation results

Figure 3.17 shows the active mixer PSS simulation results that the RF signal at 2.4 GHz is created by mixing between LO signal at 1.6 GHz mixed with the IF at 0.8 GHz. The linearity of the mixer is examined by two tone test with tones at 800 and 810 MHz with -10 dBm power. These tones will create inter-modulated tones at 790 and 820 MHz that are mixed with LO and up-converted to 2.39 and 2.42 GHz.

Figure 3.18 shows the active mixer two tone PSS simulation results. The IIP3 is calculated from

$$IIP3 = \frac{\Delta P}{2} + P_{in} \tag{3.9}$$

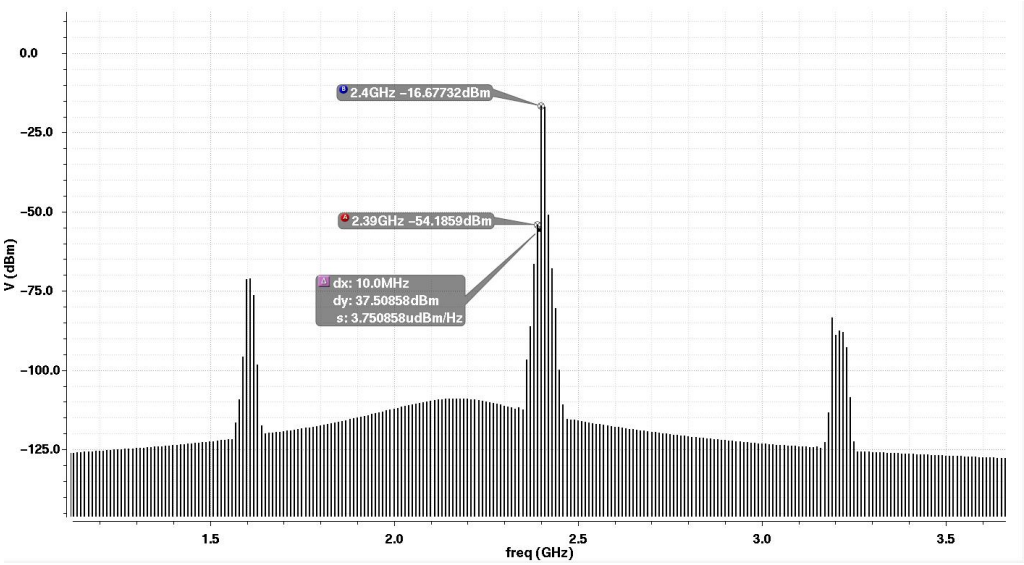

Figure 3.18: Active mixer two tone PSS simulation results

That will result in $IIP3 = \frac{37.5}{2} - 10 \approx 9dbm$.

The phase modulator output is connected to another CML similar to the phase shifter output driver, matched to 50Ω shown in Figure 3.19 RF output CML driver. The input current of the buffer is 2mA with linearity of $IIP_3 = 6\ dBm$ obtained from the two tone test.

3.2.3 Divider and pre-scaling block design

The Divide by 2 block with I, Q, and input buffers shown in Figure 3.20, consists of the divider and three self-biased buffers for LO signal at 1.6 GHz and I/Q signals at 800 MHz. The divider is designed to generate differential quadrature signals for the input of the phase shifter. The divider schematic is shown in Figure 3.21 which is the classic Razavi type frequency divider that inherently generates differential quadrature clock signals [40]. As can be seen in the Figure 3.21 , it consists of two D-latches in a negative feedback loop. The divider flips for a half period and

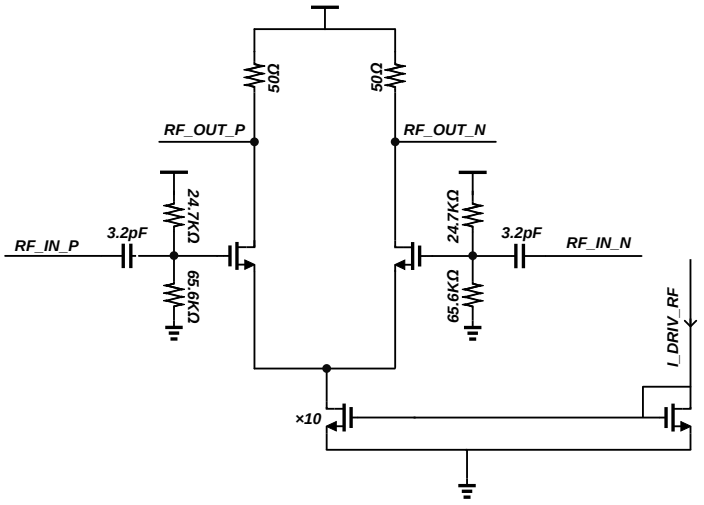

Figure 3.19: RF output CML driver

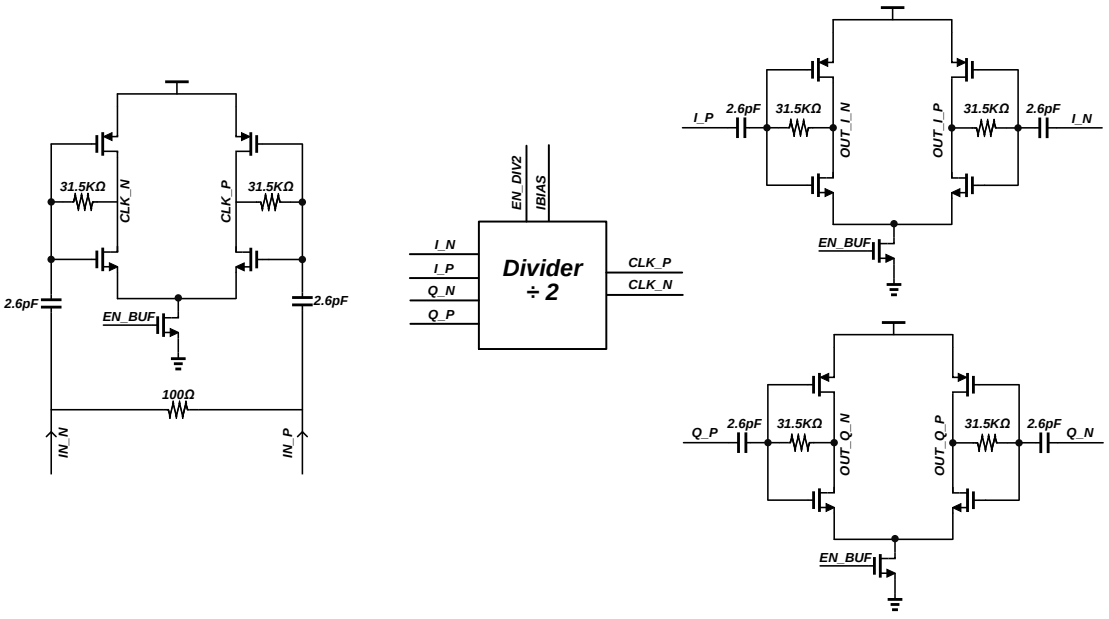

Figure 3.20: Divide by 2 block with I, Q, and input buffers

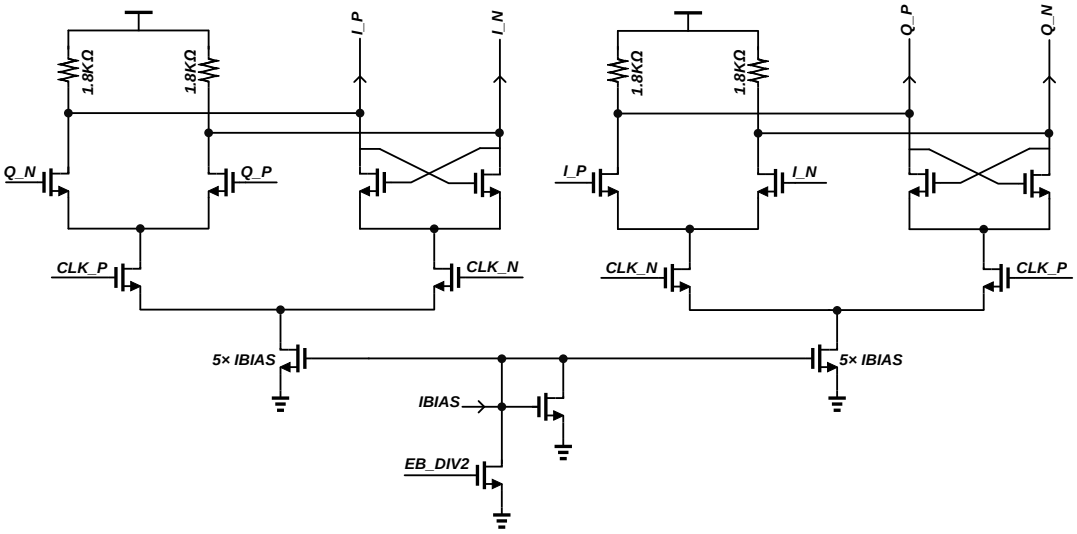

Figure 3.21: Divider schematic

latches for another half, resulting in a 50% duty cycle. The input buffer for the LO signal which is the main input of the whole phase modulator circuit, is terminated differentially with 100Ω resistance shown in the input buffers schematic. Figure 3.22 shows the differential LO inputs and the the generated differential guadrature outputs of the divider at 1.8V level.

The quadrature divider differential outputs are at 1.8 V level. The linearity of the phase shifter strictly depends on its input levels. So, quadrature signals need to be scaled down by the capacitor division block, shown in Figure 3.23 the differential I/Q signals input pre-scaling block. The value of the total scaling capacitance is determined by the digital input of C_{IN0} C_{IN1} C_{IN2}. Each of the switches C_{IN0} C_{IN1} C_{IN2} will add the $0.5pF$, $1pF$, and $2pF$,respectively. The dc level of the phase shifter input is set by a bias voltage VB as shown in the Figure 3.22 that is set to 1.3 V.

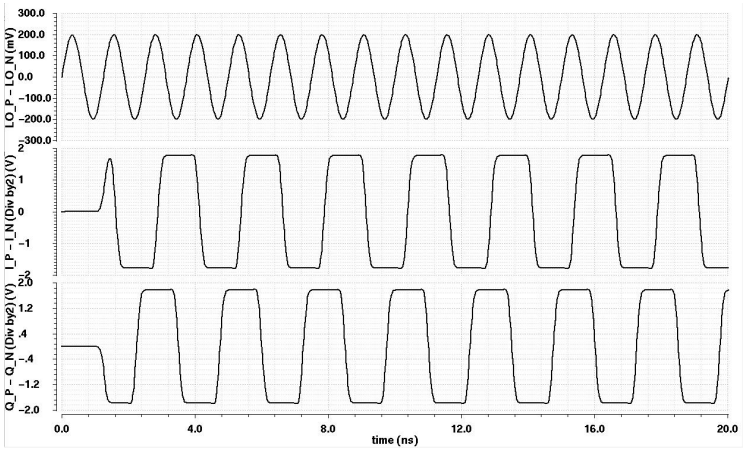

Figure 3.22: Differential input and the generated differential guadrature outputs of the divider

3.3 Simulation results

The transient simulation setup explained in section 3.1 is applied to the phase modulator. The consecutive digital input $S_Q S_I S_3 S_2 S_1 S_0$ is generated by a 6-bit ADC that is converting an input ramp with 200 kHz clock rate. Linearity of the phase shifter circuit is sensitive to the I and Q input levels. To find out a proper input level, input power is swept for the output phase response in the quadrant shown in Figure 3.24 the output phase shifts Vs. input signal power. It can be seen that the maximum input signal level for having no degradation in the phase response is around -10 dBm. The pre-scaling block, sets the input of the phase shifter to it linear region. Figure 3.25 shows the scaled differential I and Q signals, $IIN - P/N$ and $QIN - P/N$ are the inputs of the phase shifterare, scaled down by the factor of 0.03 when all of the C_{IN0} C_{IN1} C_{IN2} switches are ON.

First, let's consider the phase shifter without the DAC reference current weighting correction block. Figure 3.26 shows generated I and Q currents by DAC without the

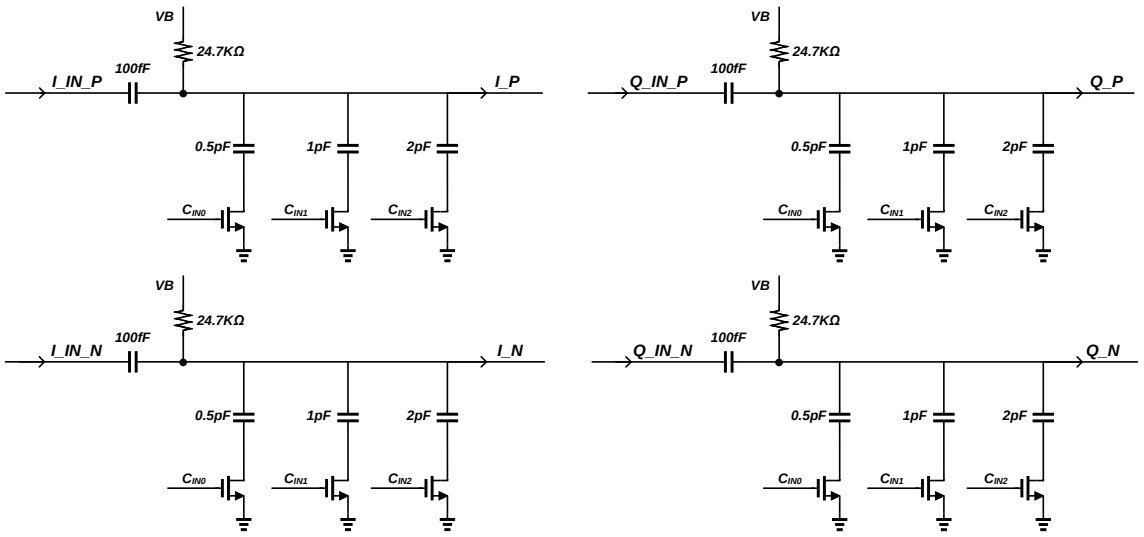

Figure 3.23: Differential I/Q signals input pre-scaling block

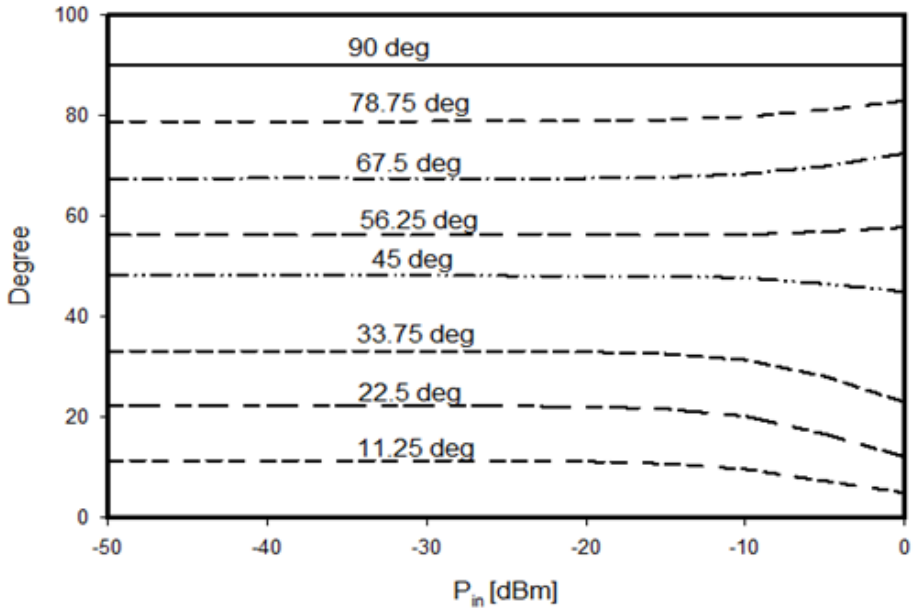

Figure 3.24: Output phase shifts Vs. input signal power

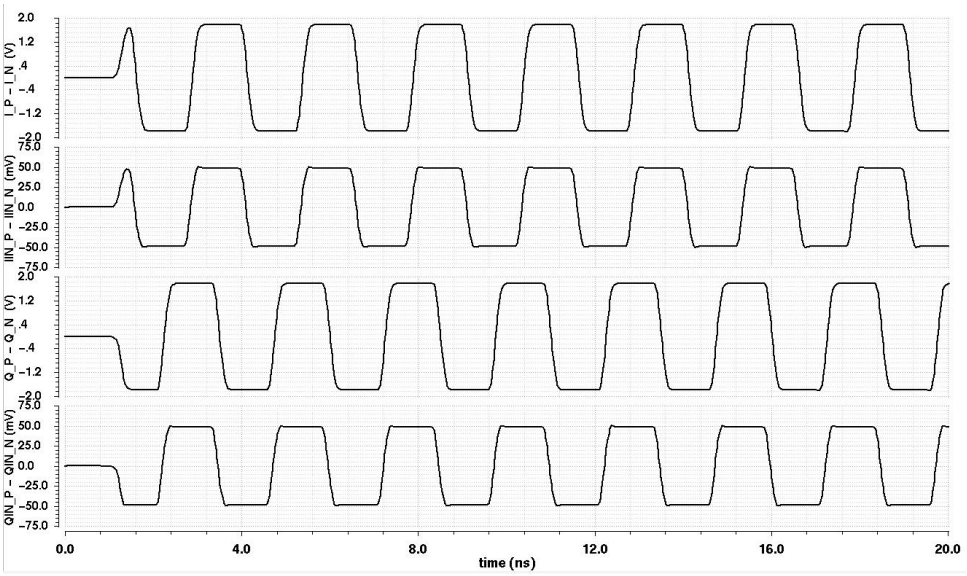

Figure 3.25: Scaled differential I and Q signals, $IIN - P/N$ and $QIN - P/N$ are the inputs of the phase shifter

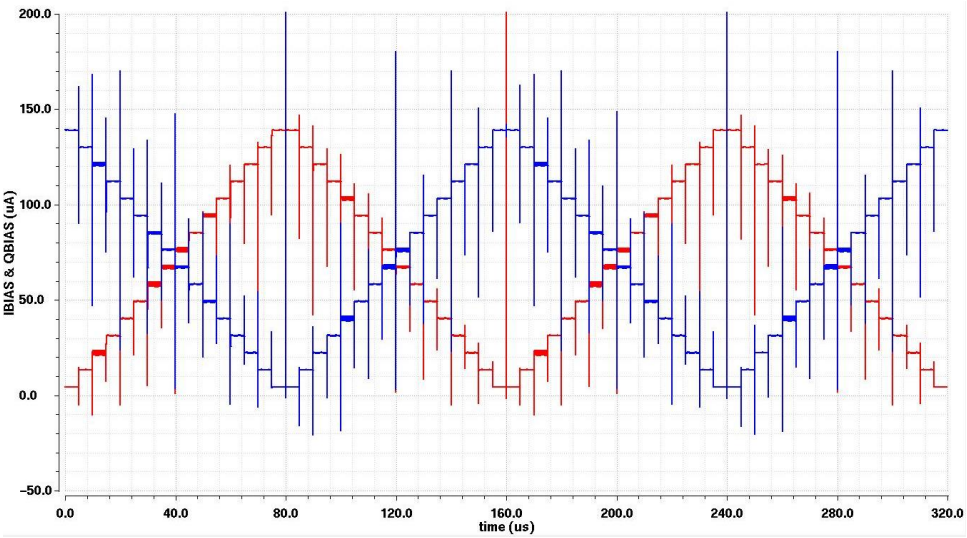

Figure 3.26: Generated I and Q currents by DAC without the DAC reference current correction block

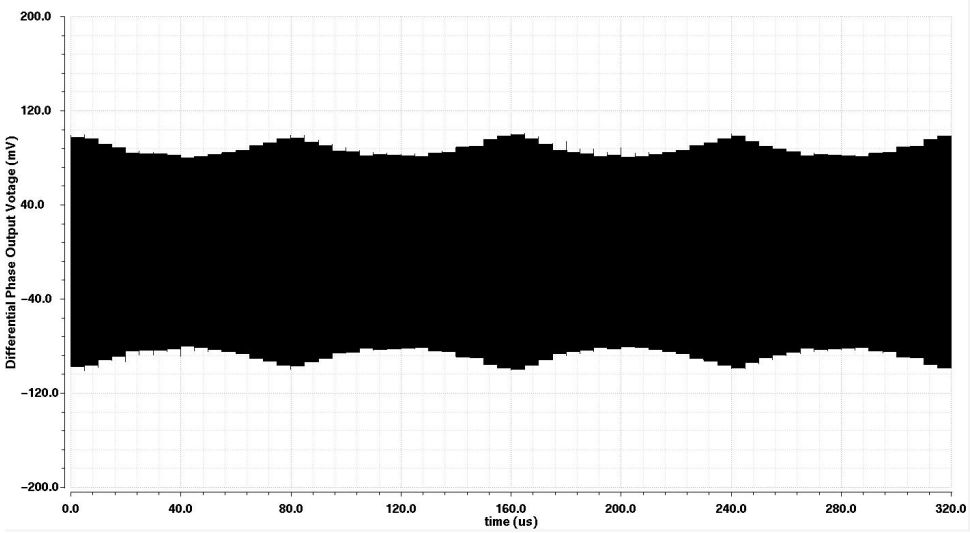

Figure 3.27: Output voltage of the phase shifter, without the DAC reference current correction block

DAC reference current correction block. It can bee seen that the variation of the I and Q currents in all of the quadrants is completely linear. As mentioned earlier, the linear summation of I and Q current will reduce the gain of the phase shifter for the 14 states in between each quadrants. Figure 3.27 shows the output voltage of the phase shifter, without the DAC reference current correction block and also, depicts the gain reduction analysis when the DAC correction block is not applied to the circuit.

To examine the phase shifter response to 64 states, the zero crossing points of the input and the phase shifted output signal at 800 MHz are plotted versus the cycle. Number of crossing point in each cycle with 200 kHz rate can be calculated as $\frac{800MHz}{200kHz} = 4k$. Then to find out the exact phase shift in each state, the difference of these two plots are plotted versus cycle. To convert the Y axis to degrees, the plot is divided by $1.25ns$ and multiplied to $360\,^{\circ}$. Figure 3.28 shows the phase shifter

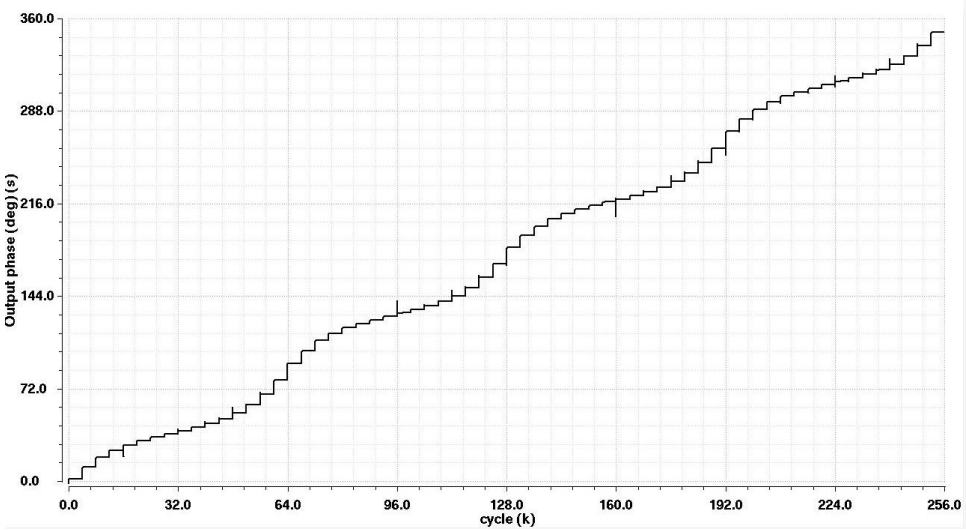

Figure 3.28: Phase shifter response to 64 states, without the DAC reference current correction block

response to 64 states, without the DAC reference current correction block. It can be seen that the output phase shift response has some deviation due to the linear vector summation of I and Q currents. The step size should be 5.625 ° and any deviation from this value is calculated to find out the DNL (Differential Nonlinearity) and INL (Integral Nonlinearity) of the DAC.

Now, let's consider adding the DAC current correction block that generates additional current for 14 states in between of each quadrants. Figure 3.29 shows generated I and Q currents by DAC with the DAC reference current correction block. Comparing this to Figure 3.26, the variation of quadrature currents is nearly sinusoidal and no longer linear. As a result, the output voltage of the phase shifter stays constant (moving on the circle, instead of the square), shown in Figure 3.30 output voltage of the phase shifter, with the DAC reference current correction block. Phase shifter response to 64 states, with the DAC reference current correction block is demon-

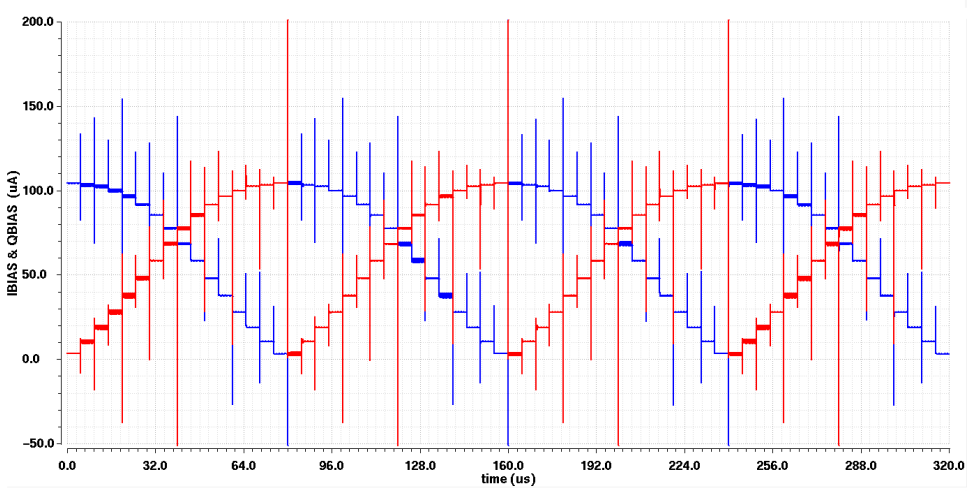

Figure 3.29: Generated I and Q currents by DAC with the DAC reference current correction block

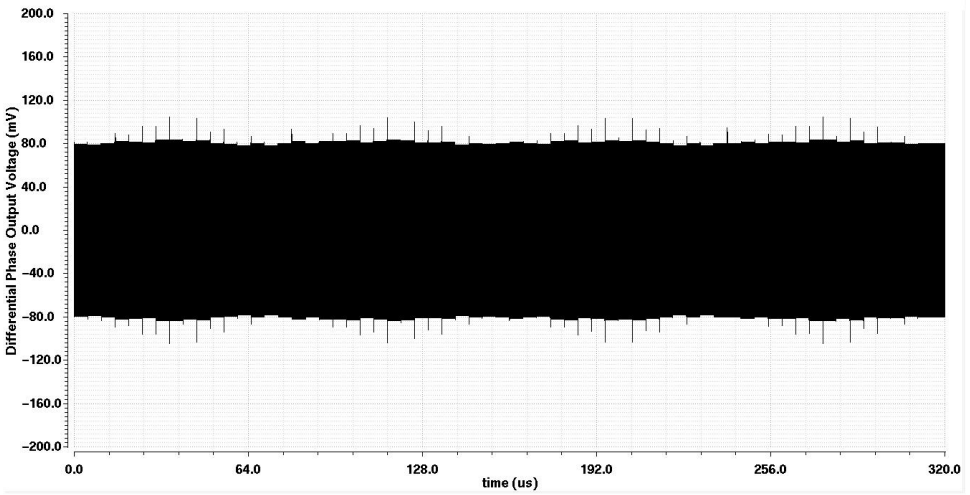

Figure 3.30: Output voltage of the phase shifter, with the DAC reference current correction block

strated in Figure 3.31. The resultant phase shifts of each step from Figure 3.31 is collected and the difference to 5.625 ° is calculated to find out the DNL in each state.

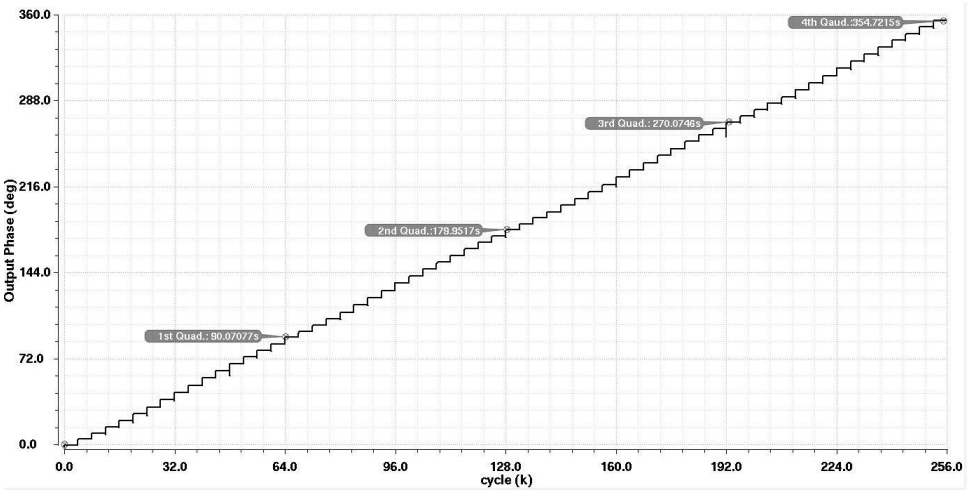

Figure 3.31: Phase shifter response to 64 states, with the DAC reference current correction block

Table 3.5: Minimum and maximum phase error and DNL

Max phase error	Max phase error	Minimum DNL	Maximum DNL
0.9 °	0.021 °	0.16	0.003

Table 3.5 summarizes the minimum and maximum phase error and DNL of the phase shifter for 64 states. Maximum and minimum DNL are calculated for the maximum and minimum phase errors, respectively. To find out the phase shifter response to changing quadrants, four phase codes associated with 45 °, 135 °, 225 °, and 315 ° are applied with 200 kHz rate. This test changes the quadrants starting from 45 °, creating 90 ° phase shifts in between quadrants. Figure 3.32 shows the phase shifter response to changing quadrants starting from 45 ° . The phase shifts and error results are summarized in Table 3.6 as phase shifts between quadrants. Finally, Figure 3.33 demonstrates transient response of phase shifter constant voltage output of 64 phase states , with 6bit phase signals at 200kHz rate.

Table 3.6: Phase shifts between quadrants

Quadrants	1st and 2nd	2nd and 3rd	3rd and 4th
Phase shift	91.49°	88.26°	92.3°
Phase error	1.49°	−1.74°	2.3°

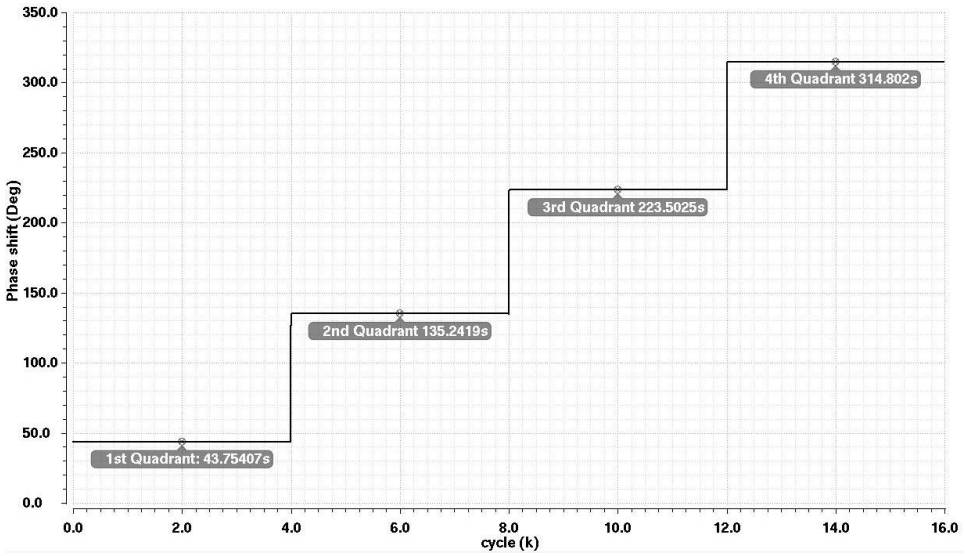

Figure 3.32: Phase shifter response to changing quadrants starting from 45°

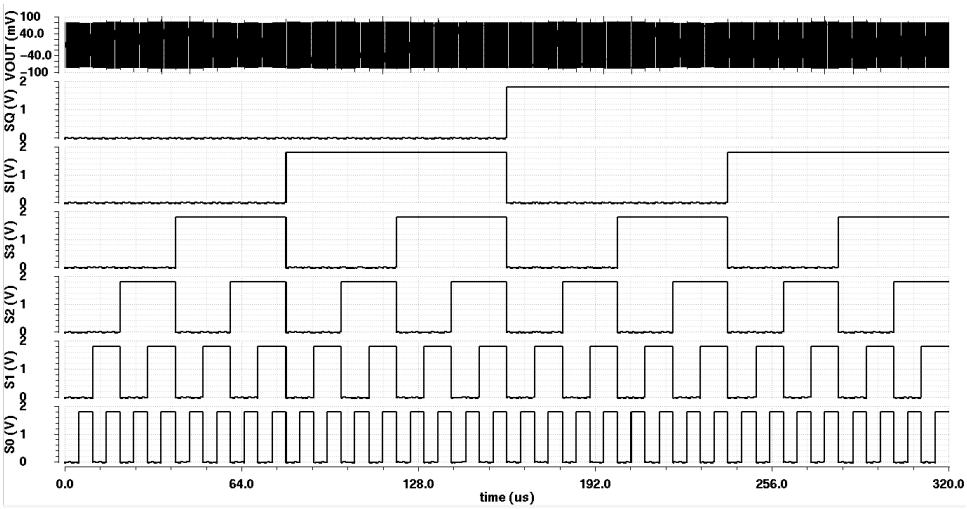

Figure 3.33: Phase shifter constant voltage output of 64 phase states , with 6bit phase signals at 200kHz rate

4. PHASE UP CONVERSION PATH FABRICATION AND MEASUREMENT

The phase modulator is implemented in 0.18 um CMOS technology with 6 metal stacks. In this section, the layout design of each block will be presented with the post layout simulation of the top chip. Then, the test plan and the PCB design will be explained. Finally, the measurement results will be compared to the simulation results.

4.1 Phase modulator layout design and Top chip

Figure 4.1 shows the phase modulator layout design. The position and rotation of the building blocks are modified to minimize the inter-block routings. In the layout design, metal 1 is set to V_{ss} and metal 2 is set to V_{dd}. Also, an effort has been made not to use more than fourth metal layer for interconnection of the devices in a block. All of the transistors have the RF layout model, except for the decoder transistors of the DAC correction block that have the nfetx and pfetx cell module with no guard ring.

Since the core of the phase modulator is the phase shifter that is based on the quadrature current summation, the matching between I and Q, let alone the DAC current mirrors is very critical. Therefore, Inter-digitization and common-centroid techniques along with dummy transistors are used in the layout design of phase shifter DAC and adder for better matching between devices. Also, the RF and phase drivers are placed next to their outputs to avoid any long connection parasitics. Figure 4.2 shows the chip layout with all the routings to the pads. The differential pair routings from the layout to the pads are drawn very symmetrical to provide the maximum matching between positive and negative signals. Total chip area is $1362 \times 1235 um^2$.

Table 4.1 summarizes the pin description of the chip with their design values.

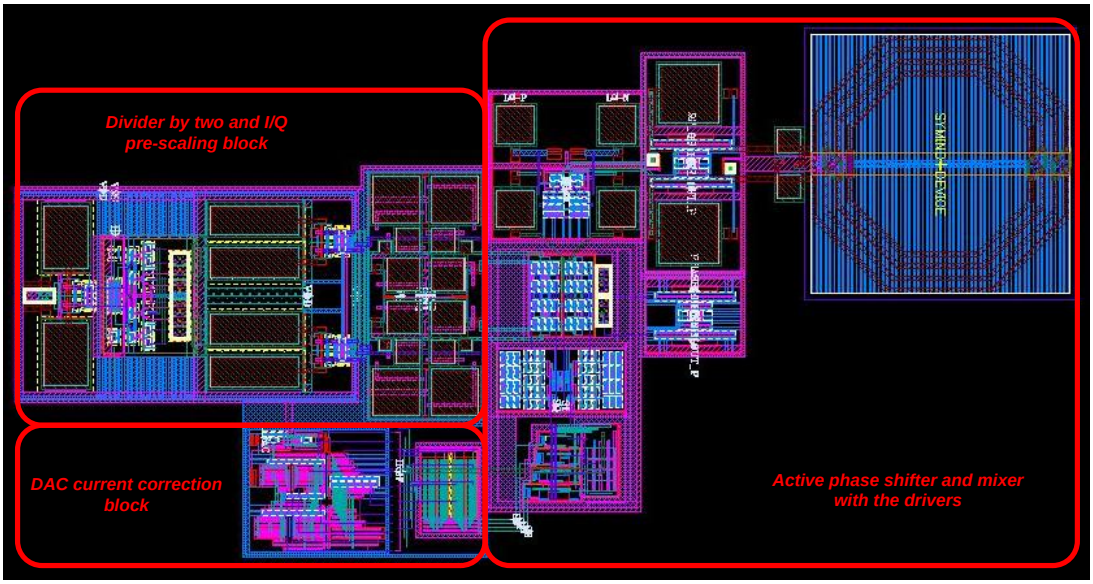

Figure 4.1: Phase modulator layout design

Table 4.1: Pin description of the chip

Pin names	Design value	Description
LO-P/N	-10dbm @ 1.6 GHz	Differential input
Phase-P/N	160mvp-p @ 0.8 GHz	Differential Constant output
RF-P/N	100mvp-p @ 2.4 GHz	Differential Constant output
I_B	150 uA	Divider bias current
I_{Bias}	500 uA	Mixer bias current
I_{DRV-RF}	500 uA	Mixer output driver bias current
$I_{DRV-PHASE}$	600 uA	Phase shiter output driver bias current
V_B	1.3 V	I/Q scaling block bias voltage
$S_Q S_I S_3 S_2 S_1 S_0$	0 or 1.8 V	Phase control
$C_{IN2} C_{IN1} C_{IN0}$	0 or 1.8 V	I/Q scaling control

The layout top chip design has total of 21 signal pins and 11 power pins (5 V_{SS} and 6 V_{DD}). Six pins of total 21 pins are associated with 3 differential pairs, $LO-P/N, PHASE-P/N$ and $RF-P/N$. Nine pins are set for the digital controls,

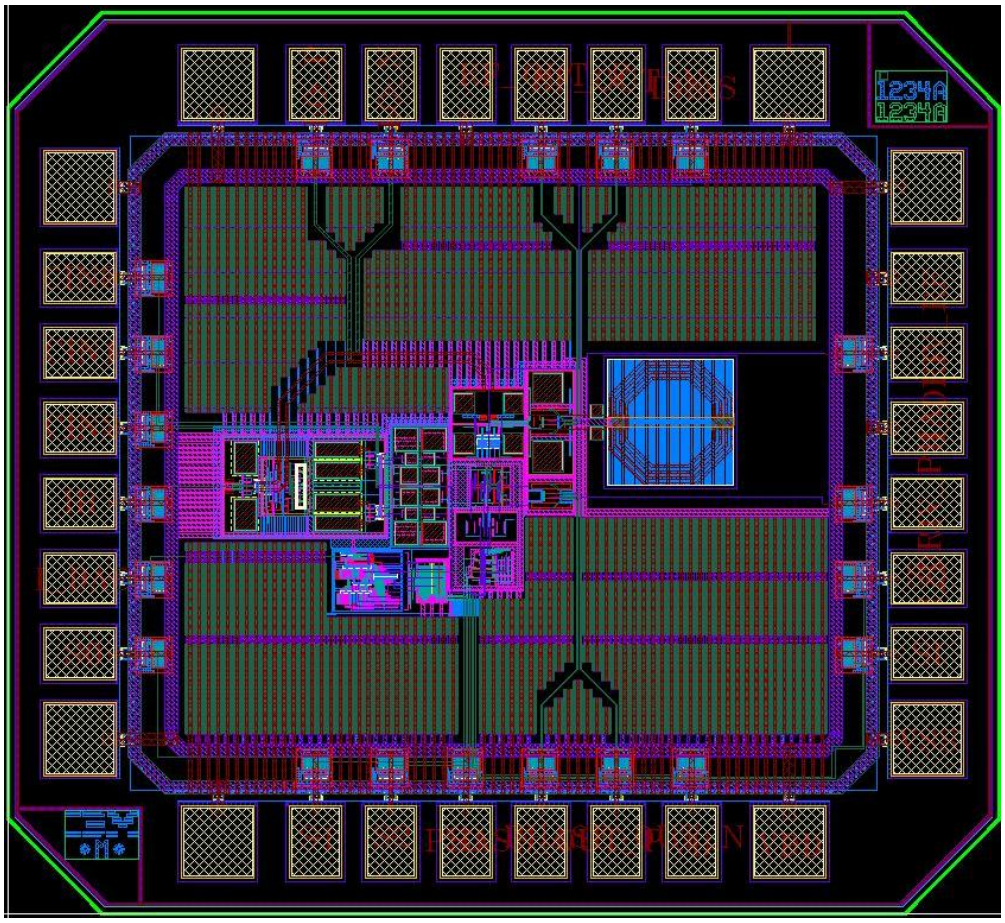

Figure 4.2: Chip layout

6 bits for phase and 3 bits for I/Q scaling block. The remaining 6 pins are used for biasing currents and voltages. After connecting the top chip layout pins to the package pads, the empty area is filled with decoupling capacitors between V_{DD} and ground to minimize the parasitics and noise.The top layout is simulated for the DRC (Design Rules Checking) to be compatible with the fabrication process and also for the LVS (Layout Vs. Schematic) to verifying the perfect match between the layout and the schematic design. Figure 4.3 shows the chip microphotograph.

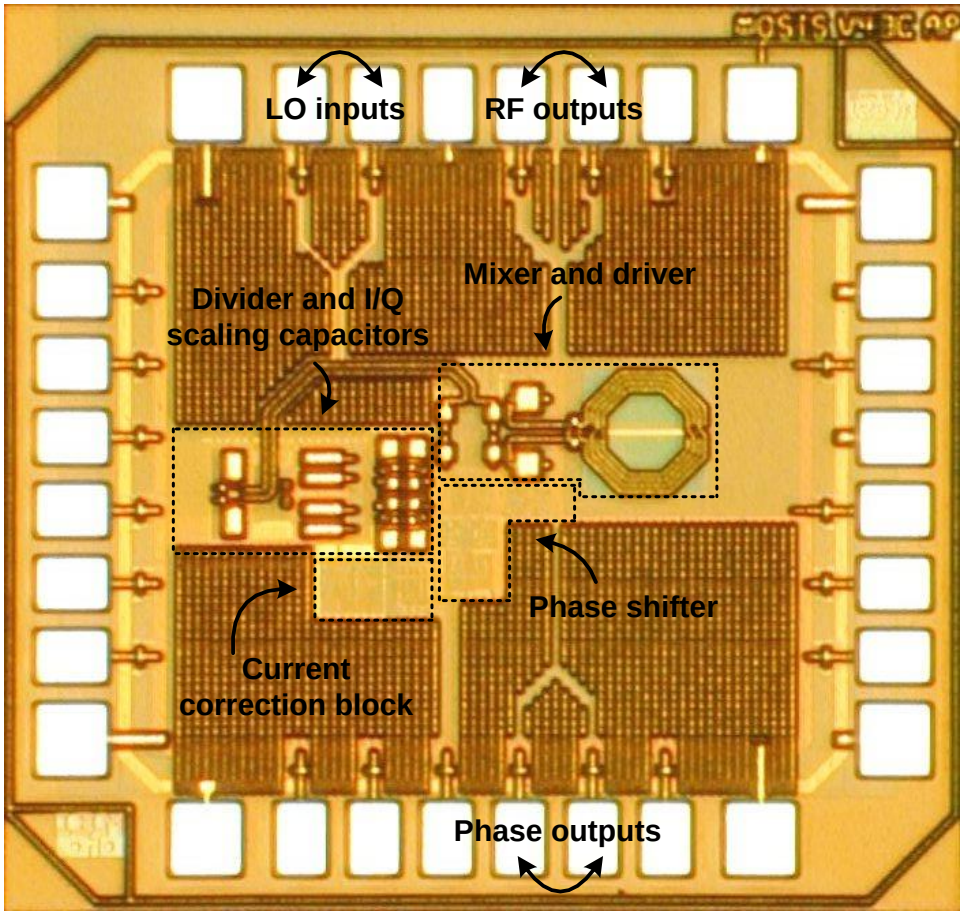

Figure 4.3: Chip microphotograph

4.2 Post layout simulation results

To verify the functionality of the layout design, parasitics extracted view of the layout is simulated. The parasitic extraction view of the layout is generated by running PEX which would add calibre view to the top chip cell. The simulations with layout parasitics extracted views takes much longer than the schematic view. So, the transient simulation is run just for a quadrant to verify the layout functionality. Also, all the DC operating points has been checked to make sure the circuit works

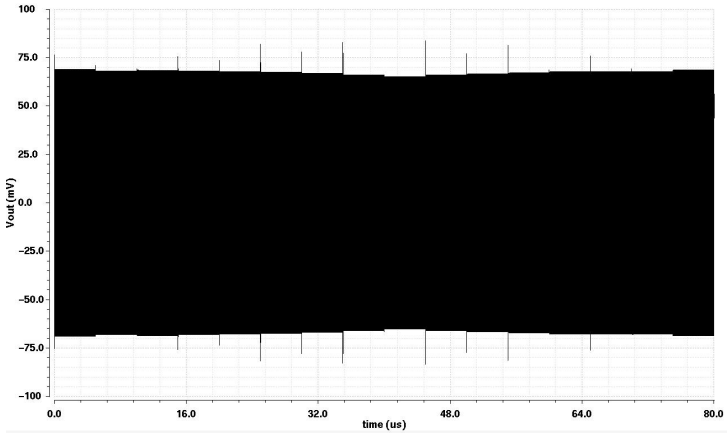

Figure 4.4: Post layout simulation results of the phase shifter output voltage

properly.

Figure 4.4 shows post layout simulation results of the phase shifter output voltage, and Figure 4.5 shows post layout simulation results of the phase shifter output phase Vs. cycle with 200 kHz rate data.

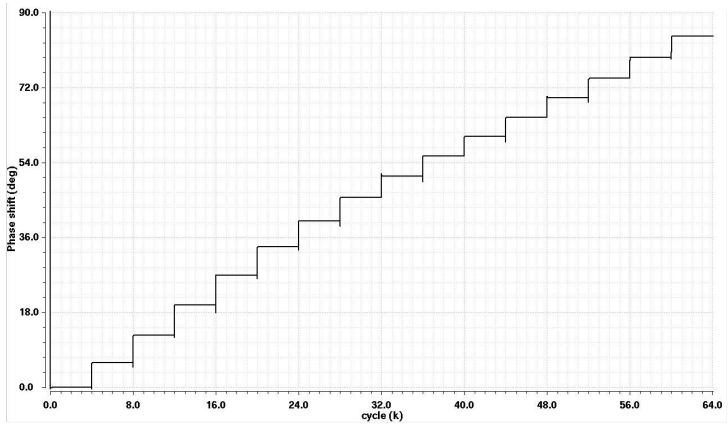

Figure 4.5: Post layout simulation results of the phase shifter output phase Vs. cycle

4.3 PCB design, test plan, and measurement results

To measure the chip, RF and DC signals are separated into two PCBs. The DC PCB contains all the biasing currents and voltages and the digital control bits. The RF PCB contains only three differential pairs for LO, phase, and RF signals and the chip. Figure 4.6 shows the RF and DC boards. Two pin headers are placed on each

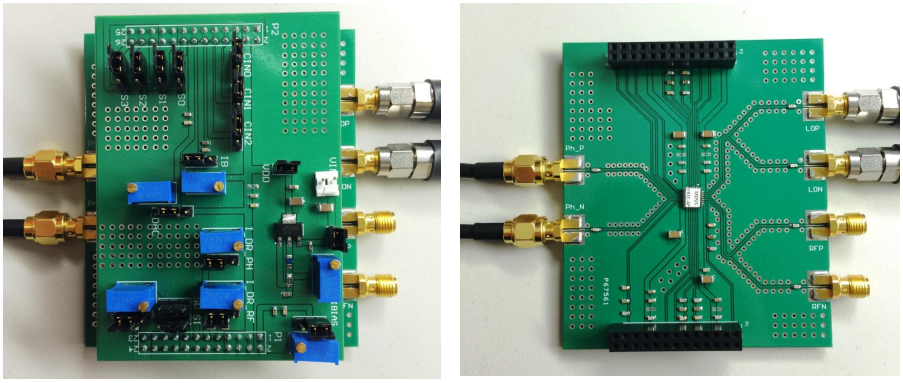

Figure 4.6: RF and DC boards

side of the RF and DC boards. The pin headers on the RF PCB board are female and the ones on the DC PCB are male and when they are connected together, all the bias signals will be connected to the chip located on the RF PCB. Through this technique, RF signals are not effected directly by the parasitics and noise on the bias signals. The DC board is hooked on top of the RF board. Two measurement setups are proposed to measure the phase response and constant envelope output signal. The first set up is the static phase response where the 6 phase control bits are changing by hand from zero to 1.8V for all the 64 states.In this setup, after fixing

all the DC operating points with DC supplies and potentiometers, a signal generator with -10 dBm power at 1.6 GHz is applied as the LO input of the phase modulator.

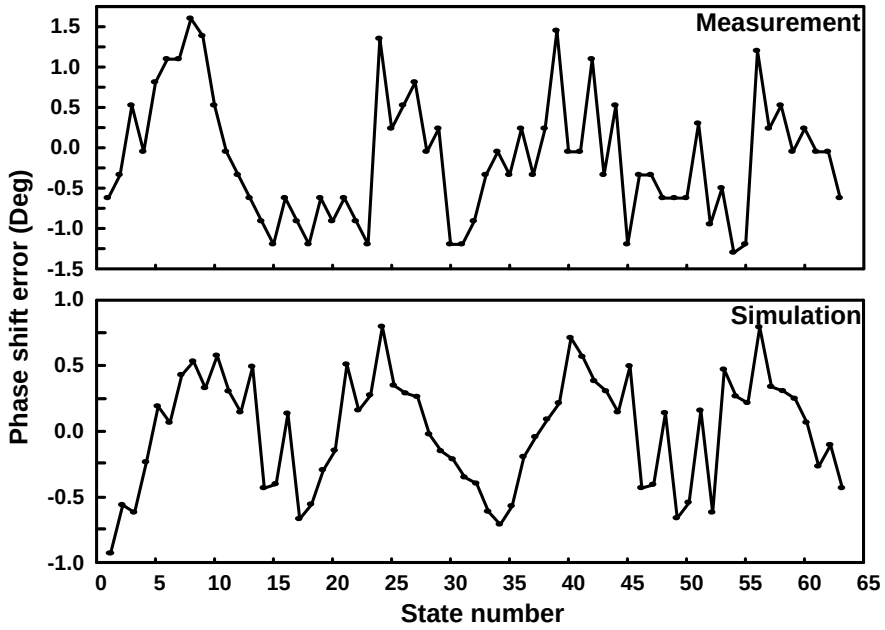

Figure 4.7: Phase shift error for all the 64 states at the output of the phase shifter, measurement versus simulation

Also, by using a splitter , a copy of the LO signal is applied to one of the channels of the oscilloscope as the reference.For each case after setting the S_Q S_I S_3 S_2 S_1 S_0 code, the zero crossing difference between the phase shifter output and the input which is set as the reference, determines the phase shifts. So, the phase shift is easily calculated by $\frac{\Delta t \times 360^\circ}{T}$, where T is 1.25 ns at 800 MHz.The same setup and calculation are used for the RF outputs at 2.4 GHz. The difference between the obtained value from the measurements and 5.625° would be the phase shift error. Figure 4.7 shows the phase shift error for all the 64 states at the output of the phase

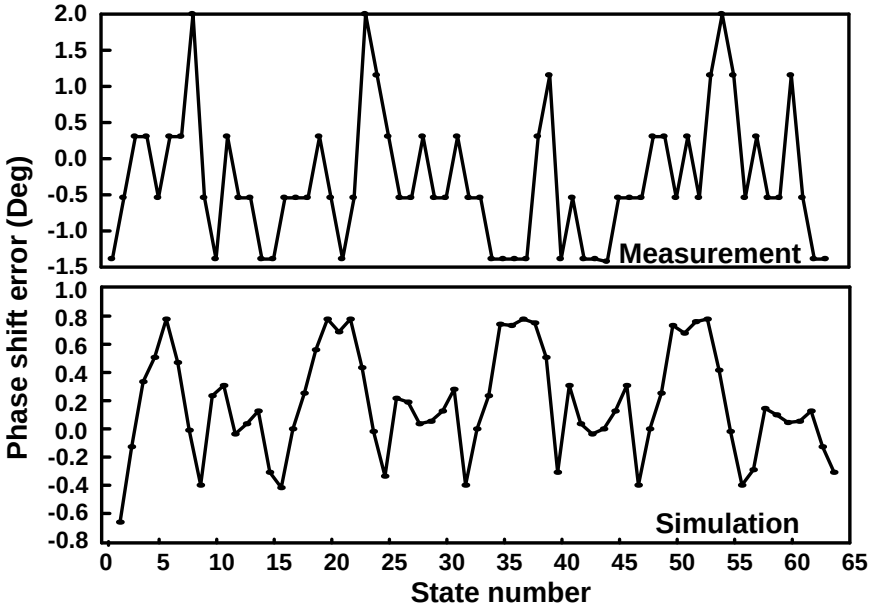

Figure 4.8: Phase shift error for all the 64 states at the RF output of the mixer, measurement versus simulation

shifter, measurement versus simulation. The same measurement process has been done at the RF output of the mixer and the results are shown in Figure 4.8, phase shift error for all the 64 states at the RF output of the mixer, measurement versus simulation. The output voltage for each case has been also captured and the variation from the constant value is plotted for each 64 states and shown in Figure 4.9, phase shifter output voltage variation from the constant envelope for all the 64 states , measurement versus simulation and Figure 4.10 mixer output voltage variation from the constant envelope for all the 64 states , measurement versus simulation. Table 4.2 and Table 4.3 summarize the output phase error and voltage variation of measurement versus simulation results for the phase shifter and mixer, respectively.

The second measurement setup it to apply dynamic 6-bit digital phase data with

Table 4.2: Phase shifter output phase error and voltage variation.

Results	Max phase error	Min phase error	Max voltage variation
Simulation	0.9°	0.12°	2 mv
Measurement	1.57°	0.185°	3.5 mv

Table 4.3: Mixer output phase error and voltage variation.

Results	Max phase error	Min phase error	Max voltage variation
Simulation	0.82°	0.12°	2.5 mv
Measurement	2°	0.15°	2.25 mv

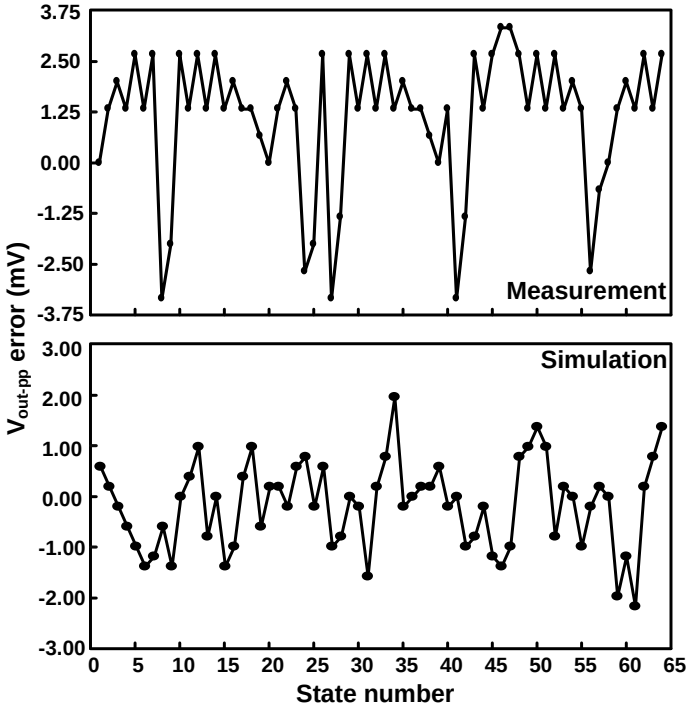

Figure 4.9: Phase shifter output voltage variation from the constant envelope for all the 64 states , measurement versus simulation

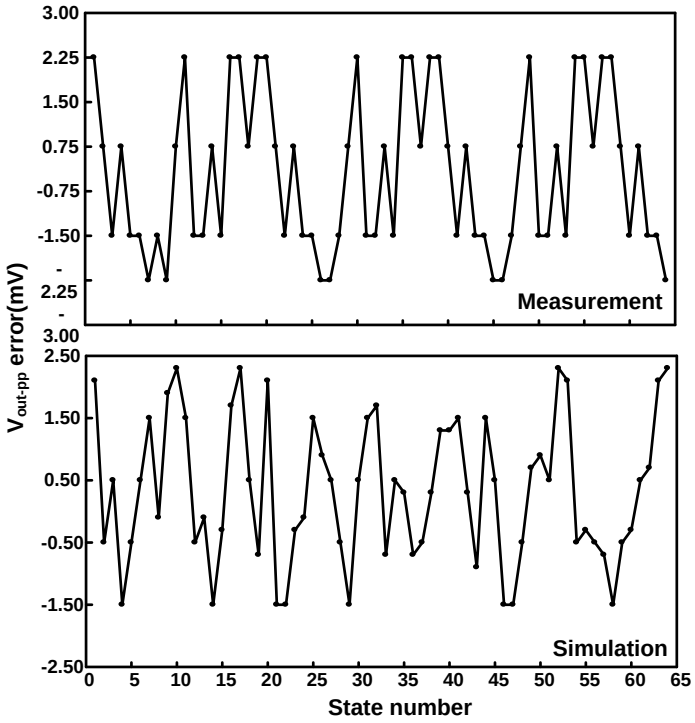

Figure 4.10: Mixer output voltage variation from the constant envelope for all the 64 states , measurement versus simulation

200 KHz rate to the phase shifter. An AVR micro-controller counter is used to generate the dynamic digital phase data. ATMEGA16 micro-controller has been chosen with AVR STK500 evaluation board and AVRISP MKII programmer. A program in C has been written, appendix, and programmed into the AVR to active its TIMER0 and set 6 bits of PORTA as the output. This counter, counts from 0 to 0XFF and when overflown, starts over again from 0. To set the speed of the counter, clock fuse bits of the micro-controller are set to divide the AVR core clock frequency of 1MHz by 5 to result in 200 KHz rate ($CK_{SEL0} = 1, CK_{SEL1} = 1, CK_{SEL2} = 1, CK_{SEL3} = 0$). Since the AVR generated outputs are at TTL level (5v), a resistive division has been applied to set the voltage levels to 1.8 V. The generated 6-bit

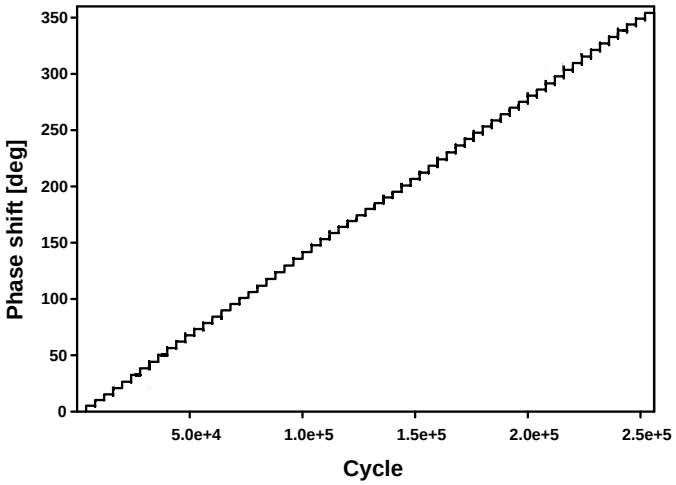

Figure 4.11: Phase shifter response to 200 kHz phase data Vs. cycle

Table 4.4: Phase shifter phase response to 200 kHz phase data

Results	Max phase error	Min phase error	Max DNL	Min DNL
Simulation	0.9°	0.021°	0.16	0.003
Measurement	1.45°	0.54°	0.257	0.096

phase data is then applied to the phase shifter and the output is monitored and saved by the oscilloscope. Input signal (LO @ 1.6 GHz)from the signal generator is also saved. The collected data is then applied to MATLAB for post processing. The zero crossing difference between phase shifter output and input versus cycle for each of 64 phase states has been calculated and shown in Figure 4.11 as the Phase shifter response to 200 kHz phase data Vs. cycle. Table 4.4 summarizes the phase shifter phase response to 200 kHz phase data measurement and simulation results.

5. CONCLUSION

In this thesis, a phase modulator path of polar transmitter using 6-bit active phase shifter and an upconversion mixer, for OFDM WLAN applications has been presented. 6 bits control the phase shifter, creating 64 states with the resolution of 5.625° for the whole 360°. The design is implemented using 0.18 um CMOS technology and the entire system is fully analyzed and measured. There have been two main targeted goals for the phase modulator. The first one has been the generation of constant envelope phase modulated signal so that it could have been applied to a polar transmitter with a nonlinear PA. The second goal's been to achieve a very high phase accuracy to a real time high speed OFDM data to be compatible with WLAN applications. The origin design of the phase shifter that's been based on the vector sum topology has been modified to provide the constant envelope phase modulated signal and also to handle the high speed OFDM modulation data. The 64 QAM OFDM modulation data has been applied to the phase modulator using 6 digital bits generated by AVR, Atmega16 micro-controller to examine the phase shifter response to a real time data with the maximum data rate of 54Mb/s. Phase response has been interpreted as the zero crossing difference of the system input and the output of the phase shifter for each cycle. The resultant phase response has the maximum phase error of 2° with maximum DNL of 0.257. The phase modulator output generates an approximately constant envelope phase modulated signal with the maximum variation of 3.5mv fro the constant peak to peak value.

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APPENDIX

```
/*****************************************************
This program was produced by the CodeWizardAVR V2.05.3 Standard.
Copyright 1998-2011 Pavel Haiduc, HP InfoTech s.r.l.
http://www.hpinfotech.com
Date : 6/25/2014
Author : Shokoufeh
Company : texas a&m
Chip type : ATmega16L
Program type : Application
AVR Core Clock frequency: 1.000000 MHz
Memory model : Small
External RAM size : 0
Data Stack size : 256
*****************************************************/
include ⟨mega16.h⟩
// Alphanumeric LCD Module functions
asm
.equ -lcd-port=0x18 ;PORTB
endasm
include ⟨lcd.h⟩
// Timer 0 output compare interrupt service routine
interrupt [TIM0-COMP] void timer0-comp-isr(void)
{
```

```
PORTA=PORTA+1;
if(PORTA==64)
{
PORTA=0;
}
}
// Declare your global variables here
void main(void)
{
// Declare your local variables here
// Input/Output Ports initialization
// Port A initialization
// Func7=Out Func6=Out Func5=Out Func4=Out Func3=Out Func2=Out
Func1=Out Func0=Out
// State7=0 State6=0 State5=0 State4=0 State3=0 State2=0 State1=0 State0=0
PORTA=0x00;
DDRA=0xFF;
// Port B initialization
// Func7=In Func6=In Func5=In Func4=In Func3=In Func2=In Func1=In Func0=In
// State7=T State6=T State5=T State4=T State3=T State2=T State1=T State0=T
PORTB=0x00;
DDRB=0x00;
// Timer/Counter 0 initialization
// Clock source: System Clock
// Clock value: 1000.000 kHz
// Mode: CTC top=OCR0
```

```
// OC0 output: Disconnected
TCCR0=0x09;
TCNT0=0x00;
OCR0=0x04;
// Timer/Counter 1 initialization
// Clock source: System Clock
// Clock value: Timer1 Stopped
// Mode: Normal top=0xFFFF
// OC1A output: Discon.
// OC1B output: Discon.
// Noise Canceler: Off
// Input Capture on Falling Edge
// Timer1 Overflow Interrupt: Off
// Input Capture Interrupt: Off
// Compare A Match Interrupt: Off
// Compare B Match Interrupt: Off
TCCR1A=0x00;
TCCR1B=0x00;
TCNT1H=0x00;
TCNT1L=0x00;
ICR1H=0x00;
ICR1L=0x00;
OCR1AH=0x00;
OCR1AL=0x00;
OCR1BH=0x00;
OCR1BL=0x00;
```

```
// Timer/Counter 2 initialization
// Clock source: System Clock
// Clock value: Timer2 Stopped
// Mode: Normal top=0xFF
// OC2 output: Disconnected
ASSR=0x00;
TCCR2=0x00;
TCNT2=0x00;
OCR2=0x00;
// External Interrupt(s) initialization
// INT0: Off
// INT1: Off
// INT2: Off
MCUCR=0x00;
MCUCSR=0x00;
// Timer(s)/Counter(s) Interrupt(s) initialization
TIMSK=0x02;
// USART initialization
// USART disabled
UCSRB=0x00;
// Analog Comparator initialization
// Analog Comparator: Off
// Analog Comparator Input Capture by Timer/Counter 1: Off
ACSR=0x80;
SFIOR=0x00;
// ADC initialization
```

```
// ADC disabled
ADCSRA=0x00;
// SPI initialization
// SPI disabled
SPCR=0x00;
// TWI initialization
// TWI disabled
TWCR=0x00;
// Global enable interrupts
asm("sei")
// Alphanumeric LCD initialization
// Connections are specified in the
// Project—Configure—C Compiler—Libraries—Alphanumeric LCD menu:
// RS - PORTB Bit 0
// RD - PORTB Bit 1
// EN - PORTB Bit 2
// D4 - PORTB Bit 4
// D5 - PORTB Bit 5
// D6 - PORTB Bit 6
// D7 - PORTB Bit 7
// Characters/line: 16
lcd-init(16);
lcd-clear();
lcd-gotoxy(0,0);
lcd-putsf("Programming complete");
}
```