ADVANCE THREE PHASE POWER FACTOR CORRECTION SCHEMES FOR UTILITY INTERFACE OF POWER ELECTRONIC SYSTEMS

A Thesis

by

MESAAD WALEED ALBADER

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Chair of Committee,	Prasad Enjeti
Co-Chair of Committee,	Hamid Toliyat
Committee Members,	Shankar P. Bhattacharyya
	Won-Jong Kim
Head of Department,	Chanan Singh

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ABSTRACT

Modern power electronic systems operate with different voltage and/or frequency rating such as Adjustable speed drive, Micro Grid, Uninterruptable Power Supplies (UPS) and High Voltage DC Transmission Systems. To match power electronic systems with the mains supply, DC link converters are used. The first stage of the DC link converter is the AC/DC conversion (rectifier). The rectifier type utility interface has substantial harmonics result in poor power quality due to low power factor and high harmonic distortion.

Power Factor Correction (PFC) schemes are effective methods to mitigate harmonics and address this issue. In this thesis, analyses of three approaches for high power density rectifiers are developed. In the first study, modular three phase boost rectifiers operating in DCM are coupled in order to increase the power density. Major drawback of this rectifier is the high currents ripple in both the source and the DC link sides which require large EMI filter size -could be larger than the rectifier component size- and large DC filter capacitor size. This thesis proposes coupling modular three phase boost DCM rectifiers, the currents in both source and DC link sides are interleaved and consequently the currents ripple dramatically decreased results in small component size of the EMI filter and the DC filter capacitor leading to high power density rectification. Also, optimization of the number of the rectifier modules to achieve maximum power density is presented. Moreover, the switching function of each rectifier employs harmonic injection technique to reduce the low order harmonics. And, the DC output voltage is

varied with the load power such that the operation is at the boundary between CCM and DCM to achieve maximum power density tracking.

In the Second study, a resonant three phase single switch PFC is presented to overcome the high 5^{th} and 7^{th} order current harmonics drawback in the conventional single switch three phase PFC circuits. The input current has low THD for each individual low order harmonics with high current ripple at the switching frequency. Interleaving the input current by coupling modular rectifiers is also presented to reduce the input current ripple. System equations and modes of operation is analyzed and derived to design the circuit parameters, switching frequency and duty ratio for the desired output voltage and load power.

In the Third study, an advancement of existing modular T-connected single phase PFCs by means of replacing the low frequency transformer with medium frequency electronic phase shifter to reduce the size and weight of the system. The approach has higher power density compared with the Y, delta and T-connected single phase PFC modules. The study examines the 3 to 2 phase conversion, system harmonics, switching technique for the AC chopper and the power flow of the system.

DEDICATION

I dedicate this thesis to my parents with full and sincere gratitude for their support, motivations, encouragements, good example, teaching, guiding force and drive to follow my dreams.

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CHAPTER I

INTRODUCTION AND LITERATURE REVIEW

1.1 Introduction

Power electronic supply with high electric power density operates from three phase system has two stage of conversion. Starting with rectifying the main ac voltage to DC voltage then adjusts the DC voltage to match the DC link requirements. The DC link configuration of power electronic supply are widely used in industries that use Uninterruptable Power Supply (UPS), Adjustable Speed Drives (ASD), induction heating systems, battery chargers and data centers etc. Also, high voltage DC (HVDC) systems employ rectifiers to convert ac input to DC output. HVDC is one example of the application of AC/DC conversion, in power system also, grid tie of two different power system use DC link converters. In renewable energy field, rectifiers are major part in the electric power generation stage for the wind generators. Micro grid systems employ rectifiers to interface with the surrounding AC systems. Furthermore, most of electronic devices are supplied by rectifier. Now a day, electric power supplies are highly relay on rectifiers as a major part to deliver the required load power.

Traditionally, rectifier type utility interface cause substantial harmonic currents and voltage distortion at the point of common coupling (PCC) which may lead to poor power quality due to ineffective energy transfer, equipment overheating , interface with telecommunication devices and electronic devices malfunctioning etc., more impact are discussed in the next section.

Power quality measurements of sinusoidal main and non-linear load interface generally characterized by:

- Power factor (PF): in linear circuit the term power factor refer to displacement power factor however in nonlinear circuit the term power factor is generalized to have two components distortion factor (DF) and displacement power factor. Where

$$DF = \frac{fundumental\ rms\ current}{total\ rms\ current}$$

Displacement power factor cos(θ) , where θ is the angle between voltage and current.

$$PF = (DF)(cos\theta)$$

-Total Harmonic distortion (THD): quantity index of the non-sinusoidal property of a waveform.

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} In\hat{}2}}{I1}$$

- Total demand distortion (TDD): percentage of harmonic current distortion in at maximum demand load current for 15 or 30 min demand.

-Form factor and crest factor are sometimes used to for non-sinusoidal waveforms:

$$Form\ factor = \frac{rms\ current}{avrage\ current} \quad , \quad Crest\ factor = \frac{peak\ current}{rms\ current}$$

1.2 Rectifier interface with the utility

Unlike the linear loads such as motors and heaters that draw sinusoidal currents proportional to the applied main voltage, nonlinear loads such as switch mode power supplies draw periodic current waveform that are not sinusoidal but can be expressed as sum of orthogonal sinusoidal set by using Fourier series. For rectifier type utility interface odd current harmonics (3^{rd}, 5^{th}, 7^{th}, etc.) are major concern. Voltage distortion at PCC and neutral current takes into account for this type of interface. In this section brief overview of typical current and voltage distortions and their impact on electrical apparatus are presented.

1.2.1 Typical rectifier current harmonics

Rectifiers draw harmonics current of frequency order and amplitude depend on the rectifier type. For diode bridge rectifier with neglecting the ac inductance and DC filter current ripple the harmonic order are (multiple of number of pulses±1) with amplitude equal to (fundamental current amplitude/harmonic order). For example, single phase 2-pulse rectifier has harmonics order (3,5,7,…) and three phase 6-pulse rectifier has harmonics order (5,7,11,13,….).The generated current harmonics are not in the same sequence. In fact, some of them are negative sequence harmonics and under supply unbalance condition zero sequence may exist. Table 1 shows each harmonic sequence for balance positive sequence 60 Hz supply. Also, triplen harmonics may appear in three phase diode bridge rectifiers depend on the DC link filter and bridge connection configuration. The triplen harmonics are source of zero sequence current and their effect is briefly described in the next subsection.

Table 1 Harmonic current sequence

Harmonic order	Frequency	Sequence	Harmonic rotation
1	60	Positive	Forward
5	300	Negative	Backward
7	420	Positive	Forward
11	660	Negative	Backward
13	780	Positive	Forward
The sequence interchanging manner between positive and negative is continuing for the rest of harmonic orders.			

However, taking into account ac inductance reduce the harmonics amplitude while the order does not effect. For passive diode bridge rectifier harmonics current amplitude is function of ac line inductance so that by increasing the ac line inductance the total harmonic distortion reduced for certain range. On the other hand, by considering the ac line inductance the rectifier input current will not transfer from one phase to another instantaneously and overlap between sequential conducted phases occur known as commutation period. Of course this overlapping cause short circuit in the PCC during

the commutation period which cause notches to the voltage of PCC. More detail described in 1.2.3.

Inrush current and overvoltage at turn on are facts of concern before presenting the effect of harmonics on electric apparatus. In the worst case scenario when the dc filter capacitor is completely discharged and the ac source input is at peak value at the turn on, an over voltage of factor 2.83 of nominal line voltage for three phase system or source voltage for single phase system appears across the dc link capacitor. The dc link voltage should be maintained about the design value since the loads are voltage sensitive. The starting current in this case reaches magnified value due to the transient response of LC circuit which may trip the supply circuit breaker and interrupt the connected loads. This problem can be overcome by adding a temporary resistance at the turn on time only which causes power losses for very short duration of time. This phenomenon occurs in transient and it is only mentioned here. Detail study of its effect is out of this thesis scope of work.

1.2.2 Effect of harmonics current

The harmonics current affect both the power quality as well as the electric apparatus. Harmonics currents affect the power quality and efficient energy transfer between the source and the load causing boor power quality. Harmonics are not contributing to produce real power that is transferred to type of energy that the electric loads design to deliver. Instead, harmonics creates reactive power that dissipated in the electric apparatus as undesirable kind of energy such as heat or vibrations. The tolerance of

electric apparatus to harmonic current is determined by their sensitivity to them. The least sensitive loads are the pure resistive that design to deliver heat such as oven and space heaters. In this case the harmonic function to deliver power but it cause excessive heating which result in insulation failure and reduce the equipment life time. The most sensitive loads are those design for pure sinusoidal current mostly found in the communication and data processing application [1]. The tolerances of the rest of electric loads are between those two limits. Examples of the effect of the harmonics on the electric loads from [1] are listed below:

- Generators and motors: current harmonics have harmful effect on rotating machinery starting with the heating of the stator and rotor winding due to currents at harmonic frequencies copper losses. In the developed air gap, current harmonic may cause torque pulsation, cogging, crawling (very high slip in induction machine) and mechanical oscillation. In the iron core, current harmonic may cause magnetizing saturation especially if triplen harmonic exist.
- Transformers: current at harmonic frequencies cause heating to the transformer windings and may cause saturation for the iron core.
- Power cables: increasing the current frequency force it to travel more in the surface of the conductors which known as skin effect. In power system the harmonic are in higher frequency than the fundamental current frequency. In order to handle the skin effect caused by the harmonics, power cable conductor size and spacing should be carefully designed. Still the copper losses increase with the existence of harmonic.

- Capacitor bank: capacitor bank absorb high frequency current which cause heating and dielectric stress to the capacitor bank.
- Electronics and instrument equipment: equipment that design to pick the zero crossing or the phase of the voltage or current wave form are disturbed by the harmonics since the harmonic may shift the wave form which cause them to malfunctioning.

1.2.3 Voltage distortion

Switching power supplies cause momentary short circuit to the supply voltage due to line commutation effect or switching shoot-through which lead to voltage notches at the PCC. The voltage wave form in the PCC may have component at frequencies other than the fundamental frequency. The severity of the notch depends on the time at which the short circuit occurs relative to the voltage wave form at that time. The most severe moment is when the short circuit occurs at the peak voltage, and the least sever or not effected when the short circuit occurs at the zero crossing of the voltage wave form. The notch depth and area depend on the impedances of the source and the load while the width or time period depends on the short circuit time. The voltage distortion due to voltage notching can be summarized to two points:

- Voltage at harmonic frequencies other than the fundamental frequency.
- Reduced amplitude (RMS or peak) of the fundamental component.

The effect of voltage distortion on the load is harmful since operating the loads at lower voltage than the rating voltage at rating power force them to draw higher current than the

rating current consequently overheat the load. The harmonic voltages mostly have the same effect of the above mentioned for the current harmonics.

1.3 IEEE 519 standard

Harmonic limits have been regulated by professional organization standards such as IEEE 519 and IEC 61000-3-6. In this section IEEE 519 current and voltage harmonic recommendation for the system voltage rating concern in this document (low voltage) will be presented. This recommendation made for harmonic measured at point of common coupling PCC and generated by single consumer. First, harmonic current limits are specified based on the size of the load relative to the supply size. Table 2 shows the harmonic current limits recommended by IEEE 519-1992 [1]. In table 2 the load current harmonics is calculated based on the total demand current TDD. Second, the voltage distortions are calculated according to the base voltage or the supply fundamental voltage at PCC. The first row in table 3 is of interest in this thesis since it specify the limit for the low voltage supply case.

Table 2 IEEE harmonic current limits

relative size of the load	Maximum Percentage of Current harmonics order (h) For voltage rating (120 V through 69 000 V)					
I_{sc}/I_L	h<11	11<h<17	17<h<23	23<h<35	h>35	TDD
<20	4.0	2.0	1.5	0.6	0.3	5.0
20<50	7.0	3.5	2.5	1.0	0.5	8.0
50<100	10.0	4.5	4	1.5	0.7	12.0
100<1000	12.0	5.5	5	2.0	1.0	15.0
1000<	15.0	7.0	6	2.5	1.4	20.0

Where I_{sc} is the short circuit limit of the supply and I_L is the maximum load current.

And table 3 shows the harmonic voltage limits recommended by IEEE 519-1992 [1].

Table 3 IEEE voltage distortion limits

Voltage rating	Individual voltage distortion (%)	Total voltage distortion THD (%)
69 KV and below	3.0	5.0
69 KV through 161 KV	1.5	2.5
161 KV and above	1.0	1.5

1.4 Electric power distribution system and Telecom industry power supply architecture

The electric power demand of telecom industry is increased by deploying more datacenters and servers to service all the networking, storage, computing, convergence, and application technologies used in telecom industry. According to GE datacenters consume approximately 3 percent of total U.S use [2]. The power supply is income from utility service company to telecom industry facilities and then processed within the facility power systems to supply different voltage rating load with reliable high quality power.

1.4.1 Electric power distribution system

Utility electric power distribution system mainly consist of three phase three wire or three phase four wire systems. In United State, Electric utility should comply with ANSI 284.1-1989 [3].

Interface between sensitive electronic equipment, their environment, and the utility generate transient disturbance or steady state distortions to the input voltage waveform [3]. Table 4 characterizes these disturbance and distortions for the input voltage.

Table 4 Disturbance and distortions characteristics for the input voltage

Voltage Parameter affecting loads	Typical range of power source
Over/Under Voltage	+6%, -13.3%
EMI (conducted) normal and common mode	10 V up to 200 KHz Less than at higher frequencies
Voltage distortion	5-50 % THD
Phase imbalance	2-10 %
Current parameter affecting source	Typical range of power load current
Power factor	0.85-0.6 lagging

Voltage Parameter affecting loads	Typical range of power source
Crest factor	1.4-2.5
Current distortion	0-10% total rms

Table 4 continued

The favored operation voltage for industrial plants is 480Y/277 V [4]. By such utilization three phase 480 V is directly connected to the supply, 277 V lighting loads can be connected in single phase line to neutral fashion and 120 V loads can be supplied with small rated transformers. Moreover, the usual AC source for Uninterruptible Power Supply (UPS) is 480/277 V 208/120 V for three phase systems [5]. In high power rating systems 5MW and above medium voltage 1 KV or greater is recommended for the stand by generators [6]. In this case the main supply switchgear is connected to medium voltage distribution system along with the stand by generator through bus coupler that transfer the supply between the main and the stand by generator as required by the design followed by medium voltage to low voltage transformer to fit the facility input voltage ratings.

1.4.2 Telecom industry power supply architecture

Modern telecom power system architecture use low voltage DC link bus either regulated 48V or semi-regulated (36V- 55V) , to take advantage of reduced distribution losses,

supplied through modular UPS systems to share the load power [7]. These modular UPS systems rectify the supply mains voltage, 480 Vac for example, and converted to the desired low voltage DC link which supplies different power strips that have multi-output voltage ,3.3V 5V 6V 12V .. etc. A proposed system with higher DC link voltage (380 V) is presented in [8]. The advantage of having higher DC link is:

- Lower I^2R losses.
- Less conversion stages in the overall system which result in less losses.
- Smaller size and weight.
- Longer battery backup.
- Single global voltage [8].

An industry example for this architecture is GE Total Efficiency Datacenter shown in figure 1. The DC and AC UPS consist of rectifiers in the AC low voltage end, DC link and batteries, and DC/DC converter for DC loads or inverter for AC loads. GE Galaxy Power System series used in DC UPS employ modular (4 or 6) 595LTA rectifier for 480 Vac 60 Hz 20A supplies each rectifier [GPS 4848 Galaxy Power] as shown in figure 2.

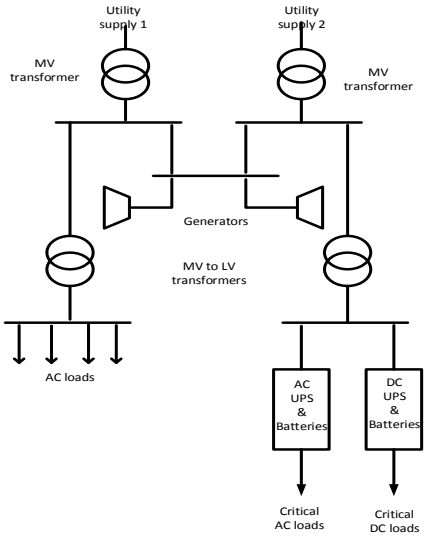


Figure 1 GE Total Efficiency Datacenter

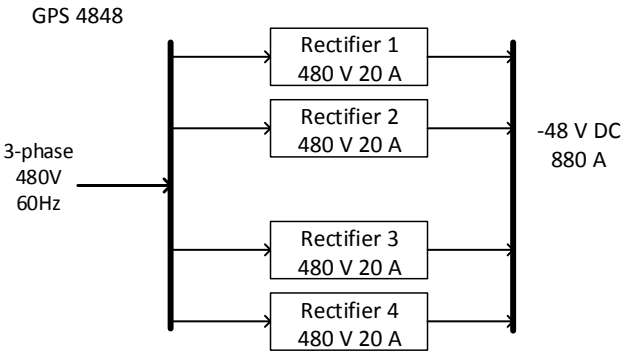


Figure 2 GPS 4848 Galaxy Power

1.5 Existing three phase PFC and harmonic filtering scheme

To meet the harmonic specification and power quality standards several techniques are used. Preference of one technique among others depends on the application, nature of the load, and system parameters to make use of the advantageous and avoid the disadvantageous. An over view of different major and common used techniques are presented in this section.

1.5.1 Multi-pulse rectifiers and phase staggered loads

Multi-pulse rectifier can be achieved by combining 6-pulse rectifier to form 12-pulse, 18-pulse, 24-pulse... etc. by shifting each 6-pulse with angle of (360/number of pulse) from each other. 18-pulse configurations are widely used in the marketplace and practically meet the IEEE 519 standards [9]. However 12-pulse rectifier can achieve same performance with some additional modification such as the system proposed in [10]. In multi-pulse techniques phase shifting transformers are used to create the phase shifting between the pulses and provide electric isolation between the load and the supply. Several designs and methods are used to eliminate the transformer size and power rating. Main advantages of multi-pulse rectifier are:

- Transformers provide electric isolation between the load and the supply.
- No control circuit required which make the system simple.
- Robust and less maintenance activity.
- The absence of high switching frequency eliminates the EMI noise.

- Transformers turn ratios could be adjusted to have low DC link voltage.

However, low frequency transformers (60/50 Hz) connected in series between the supply and the load yield in the following disadvantages:

- Occupied large space and has heavy weight compared with the other active techniques.
- Magnetic component used in the transformers core has high cost.
- In some topologies zero sequence block transformer is required which increase the size, weight and cost more.
- Typical transformer rating for 18-pulse is 68% to 80% of the DC load [9].
- Designed for specific system parameter.

This technique is suitable in high power application with an environment that does not limit the size and weight.

1.5.2 Active filters

Harmonics can be filtered with passive filters design for each harmonic order. Active Power Filter (APF) topologies designed to eliminate several order harmonics using less passive element and more active element. APF can be classified to shunt active power filter, series active power filter and hybrid power filter which is a compensation of active and passive filters to improve the performance with lower rating. Shunt APF is used to reduce the current harmonic while the series APF is used to reduce the voltage harmonic. Figure 3 shows the topologies of a) series

active power filter and b) shunt active power filter. Since the series APF connected in series between the supply and the load it is required higher power rating than the shunt APF. The shunt APF is of concern in this section because the main objective of this work deals with current harmonics elimination. The APF is suitable and cost-effective for low to medium power industry [11]. Unlike the multi-pulse rectifier, APF can be used to compensate several nonlinear load connected to the same PCC and can be used to eliminate neutrals current. Moreover, APF is much lower in size and cost compared with multi-pulse rectifier. On the other hand, the APF required complex control circuit.

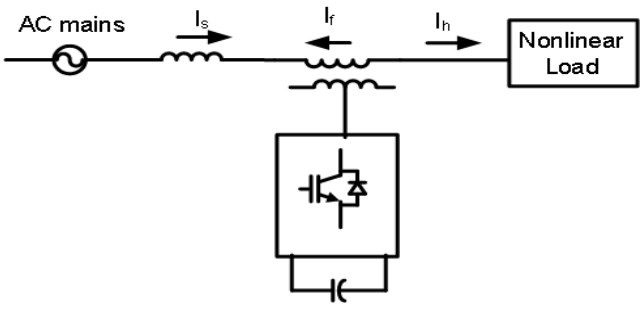


Figure 3 a) Series APF

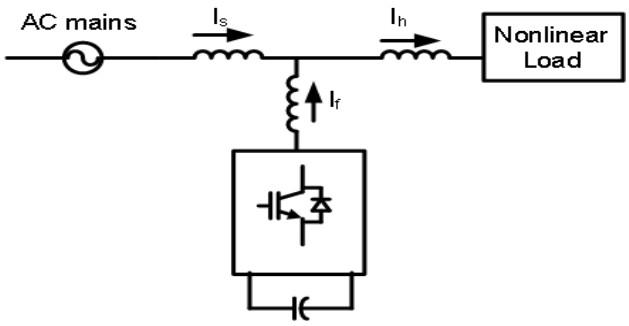


Figure 3 b) Shunt APF

The rating of the APF depends on the harmonics to be compensated. A Comparison of current rating of shunt APF compensating an inductive rectifier with various additional harmonic mitigation techniques is presented in [12]. Table 5 summarized the result found in [12].

Table 5 APF current rating

Number of current pulses	IAPF-rms (pu)
6-pulse	0.311
6-pulse with harmonic trap for 5th and 7th harmonics	0.191
12-pulse	0.152

Finally, The APF can be used to eliminate real power oscillation, improve power factor and provide harmonic damping besides eliminating current harmonics [13].

1.5.3 Phase modular rectifiers

Single phase boost PFC has high power density and fulfill the harmonic standard requirement and easy to control compared with the PWM rectifier [14].Modular single phase PFC can be connected to form three phase PFC system. Modular single phase PFC can be connected in Y or delta fashion to form three phase PFC. Using modular single phase PFC to form three phase PFC must balance the loading among the modules is vital to keep the system. The Y connected modular with open neutral line shown in figure (4 a) has the Advantage of low output DC link voltage [15]. However, it suffers from common mode noise and requires three output voltages to be regulated with balancing the input current which result in complex control compared to the delta connected modular [16].

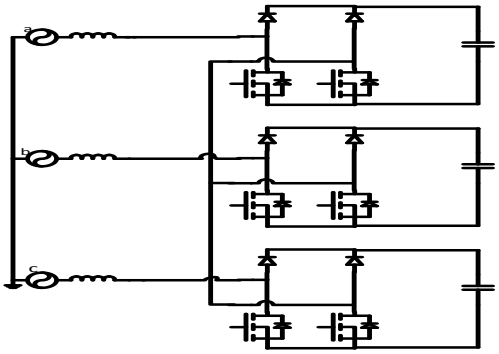


Figure 4 a) Y connected PFC modular

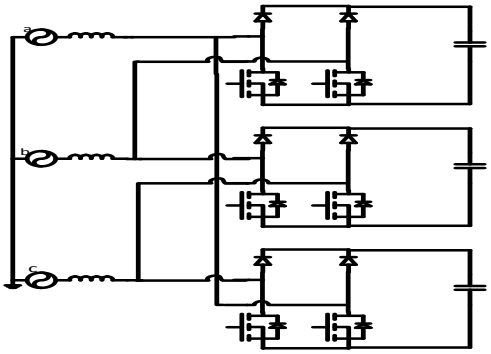


Figure 4 b) Delta connected PFC modular

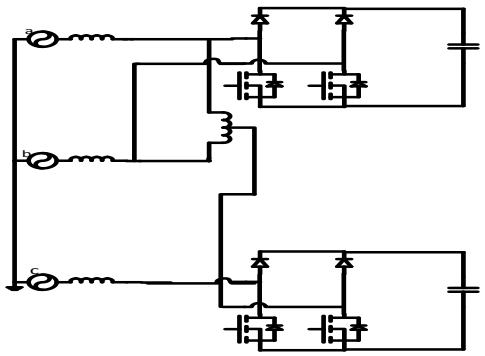


Figure 4 c) 3/2 phase Scott transformer based

Unlike the Y-connected modular, in Delta connected modular shown in figure (4 b) the control can be implemented individually for each module and the balance loading achieved in symmetrical main voltage [17]. Also, in case of one phase main voltage failure the Delta connected modular can be delver full output power without affecting the input current quality [18]. However, the DC link voltage is high (more than 1.4 times the line-line RMS input voltage).

Finally, three phase can be reduced to two phase system by three to two phase T-Scott transformer and two modular single phase can be used instead of three modular as shown in figure(4 c). The advantages of modular method are:

- Easy to implement.
- Can be operated for wide input range.
- High input current quality.

- More loads can be added by adding more modular.

And the disadvantages of the modular method are:

- Load balance between the modules is required to achieve symmetrical loading.
- Additional DC/DC converter is required to provide the electrical isolation.
- Each module has individual DC link and DC capacitor filter. [17]
- Neutral current may exist.
- Relatively high number of circuit element used.

An approach to reduce the number of element by combining 3 to 2 phases is presented in [19].

1.5.4 Direct three phase PWM rectifiers

The PWM rectifiers use the pulse width modulation technique to control 3-leg 6-switch (IGBT's) to have sinusoidal input current as shown in figure 5. PWM rectifiers classified as current Source rectifier or voltage source rectifier based on DC link type.

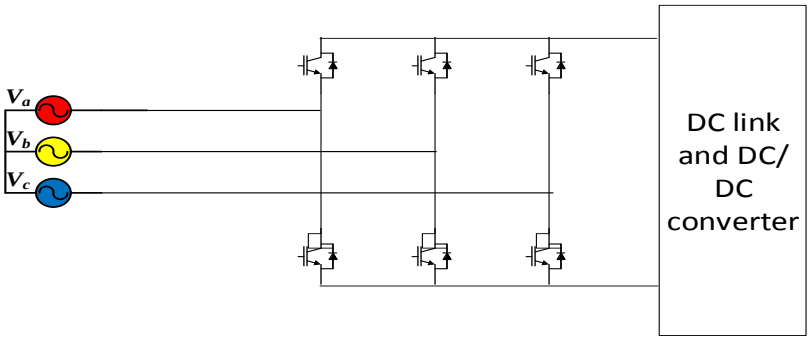


Figure 5 PWM rectifier

The current source rectifier has more component and lower performance [20]. The direct three phase rectifiers overcome the drawbacks of the modular single phase rectifiers else they still require additional DC/DC converter to provide the electrical isolation. Also, PWM rectifiers have excessive number of active switches. Several attempt proposed to reduce this number of switches such as [20] and [21].

1.5.5 Boost rectifier in DCM

The three phase boost rectifier operating in discontinuous current mode (DCM) is kind of direct three phase rectifiers that utilized single active switch. The system first proposed by [22]. The circuit topology is shown in figure 6. It main principal is to shape the inductor discontinuous current by the input voltage so that the input current has a fundamental sinusoidal modulated wave form along with high frequency carrier wave as shown in figure 7. The main advantageous of this topology are:

- Single active switch.
- Small reactive component.
- High power factor and low harmonics.
- Simple control circuit, similar to dc-dc converter.
- Zero current switching for the diode bridge which eliminates the switching losses in the bridge.

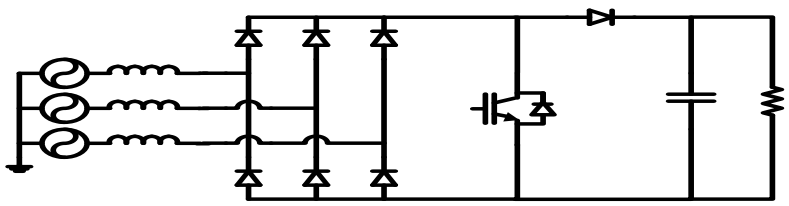


Figure 6 DCM boost rectifier

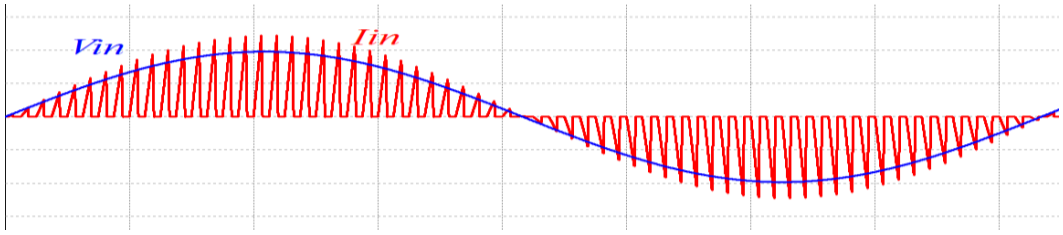


Figure 7 DCM Current wave form

Similar resonant topologies have same advantageous were derived and developed from same concept such as that proposed in [23] and [24].

1.5.6 VIENNA Rectifier

The drawback of the low order harmonics in the system presented in section 1.5.5 is overcome with multi-level PWM rectifiers by adding four-quadrant switches in symmetrical three phase shape to balance the input current path such as in Delta switch rectifier and VIENNA rectifier. VIENNA rectifier shown in figure 8 is of concern since it has high power density and it is designed for telecom applications.

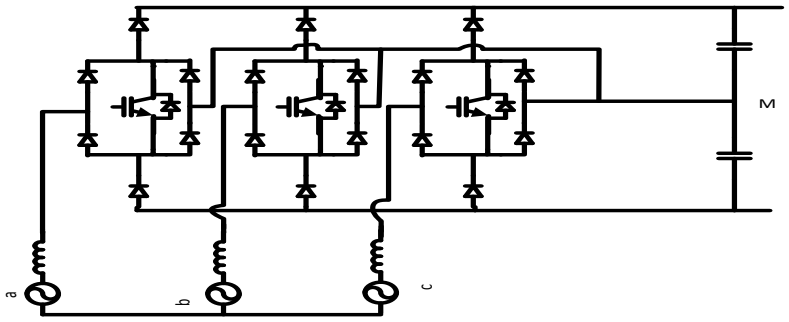


Figure 8 VIENNA rectifier

The main advantageous of VIENNA rectifier are summarized from [25]:

- Low input current harmonics due to out DC voltage mid-point to neutral voltage.
- Less device voltage stresses compared with PWM rectifier and Delta switch rectifier.
- High power density.
- Load power can be distributed over the negative and positive output partial voltage.
- Phase shift between the input current and input voltage is possible.

1.6 Research objective

The objective of this thesis is to analyze high power density three phase PFC system for AC/DC power conversion by combining modular three phase or/and single phase PFCs with reduced components size and adequate utility interface.

The thesis explores three approaches for high power density rectifiers. In the first study, modular three phase boost rectifiers operating in DCM are coupled in order to increase the power density. Major drawback of this rectifier is the high currents ripple in both the source and the DC link sides which require large EMI filter size -could be larger than the rectifier component size- and large DC filter capacitor size. This thesis proposes coupling modular three phase boost DCM rectifiers, the currents in both source and DC link sides are interleaved and consequently the currents ripple dramatically decreased results in small component size of the EMI filter and the DC filter capacitor leading to high power density rectification. Also, optimization of the number of the rectifier

modules to achieve maximum power density is presented. Moreover, the switching function of each rectifier employs harmonic injection technique to reduce the low order harmonics. And, the DC output voltage is varied with the load power such that the operation is at the boundary between CCM and DCM to achieve maximum power density tracking.

In the Second study, a resonant three phase single switch PFC is presented to overcome the high 5^{th} and 7^{th} order current harmonics drawback in the conventional single switch three phase PFC circuits. The input current has low THD for each individual low order harmonics with high current ripple at the switching frequency. Interleaving the input current by coupling modular rectifiers is also presented to reduce the input current ripple. System equations and modes of operation is analyzed and derived to design the circuit parameters, switching frequency and duty ratio for the desired output voltage and load power.

In the Third study, an advancement of modular T-connected single phase PFCs presented in [19] by means of replacing the low frequency transformer with medium frequency electronic phase shifter to reduce the size and weight of the system. The approach has higher power density compared with the Y, delta and T-connected single phase PFC modules. The study examines the 3 to 2 phase conversion, system harmonics, switching technique for the AC chopper and the power flow of the system.

1.7 Thesis outline

The content of this thesis is organized in chaptered manner. In chapter 1, Introduction of AC/DC conversion and associated distortions effect with industrial application example of telecom data center is presented. IEEE harmonic standards and literature review of previous work to mitigate harmonic distortions is also presented. Finally, research objective of building high power density AC/DC system is established.

In chapter 2, Three phase modular PFC consist of three 3-phase boost DCM rectifiers coupled in order to maximize the power density is presented. After the introduction of the boost PFC and their types, the analysis started with the analysis of the boost converter to identify the boundary of the mode of operation and to find the maximum power operating point. Then, three phase boost DCM rectifier and harmonic injection method is reviewed. Next, optimization of the number of the modules to achieve maximum power density is obtained. Afterward, Maximum power density tracking operation is derived by varying the DC link voltage with the variations of the load demand. Then, EMI input filter design is presented. Finally, design example and simulation results are performed.

In chapter 3, a resonant three phase single switch PFC is presented. In first section introduction of resonant rectifiers and the advantage of the purposed system is introduced. Next, proposed system topology and principal of operation is explained. Then, the proposed system is analyzed starting with the d-q frame analysis of the neutral voltage of three phase single switch rectifier and the neutral voltage shifting to overcome the low order current harmonics. Going through each mode of operation of the system

the equation and operation limit is derived. Based on the equation derived, system design characteristic is provided. Next, interleaving of modular rectifiers to reduce the input current ripple and to achieve constant power drawn from the supply is presented. In the next section, Example and simulation result is provided.

In chapter four, modular single phase PFC is combined to form three phase PFC. Starting with the introduction of modular single phase PFC and the existing T-connected modular single phase PFC system to introduce the proposed advancement of the T-connected modular single phase PFC by means of replacing the low frequency transformer with electronic phase shifter. In the next section, analysis of three to two phase conversions and AC/AC conversion are explained. Then, the harmonics associated with the switching of the ac chopper is analyzed. The four step switching technique used in the proposed system is explained. Example and simulation result is provided. Finally, Experimental results are show.

At the end chapter 5 summarize the results and the advantageous/disadvantageous of the proposed systems.

CHAPTER II

INTERLEAVING THREE PHASE DCM RECTIFIERS FOR HIGHER POWER DENSITY

2.1 Introduction

2.1.1 Boost PFC rectifiers

Boost power factor correction rectifiers have been widely used to achieve high input power factor and low harmonic distortion. The operation of the boost converter can be classified depending on the inductor current to three modes: continuous current mode (CCM), critical or boundary current mode (CRM), and discontinuous current mode. In (CCM) operation the inductor current waveform is continuous and has very small ripples which cause the inductor rms current to be nearly equal to the input rms current leading to low electromagnetic interface (EMI) and lower conduction losses in the inductor and lower conduction loss in the switches as well if compared with the other two modes of operation. However, the continuity of the current cause hard switching and consequently switching losses exist and diode reverse recovery current should take into account in the design. Boost PFC in CCM mode is mainly used in high and medium power application [26]. In both CRM and DCM the switches turn on in zero current and no switching losses occurs. In CRM high input power factor can be achieved but the frequency is not fixed and varies as required to keep the current wave form in the boundary between CCM and DCM which cause difficulty in designing the converter and the EMI filter. Also, variable frequency may cause peat phenomena and control problems. DCM mode has the advantage of zero-current turn on and constant switching frequency. Moreover,

DCM can be used in three phase rectifier as shown in section 1.5.5. By placing the inductors in the ac line side the commutation of the current through the bridge diodes allow continuity of the conduction in each phase if large duty cycle applied for the boost converter. This topology known as PZ circuit proposed by [22] is limited with high boosting ratio [27].

2.1.2 PZ circuit operation at low boosting ratio

The analysis is applied during the interval $0<\omega t<\frac{\pi}{6}$ with reference phase a = Van sin(ωt) and can be expanded with alternating the phases through the entire line period. In each duty cycle the PZ circuit has four mode of operation. Figure 9 shows the circuit. In Mode 1 [0, t1], when the switch S1 is closed the diode D1 will open and the three ac inductors are shorted through Da1,Dc1,Db2 and S1. As a result the current in each inductor will rise in a rate proportional to the line to neutral input voltage. In the DC side the capacitor is large enough to maintain constant voltage with small ripple during this time. Then the switch is open and Mode 2 [t1, t2] starts. The Diode D1 will close and the three diode bridge will remain conducted due to the line commutation of the ac inductors. The most positive or most negative phase in this case phase b discharged in a rate equal to the sum of the rate of the other two phases according to KCL. When the current in the inductor of the least positive or negative phase in this case phase a reach zero at t2 mode 3 [t2,t3] starts and the rate of discharge of the other phases are equal till all the currents reach zero at t3. Finally, Mode 4 [t3,T] all the switches are open. The current wave form is shown in figure 10.

The discontinuous currents follow an envelope of the line to neutral voltage as long as the three phases are conducting resulting in sinusoidal envelope in phase with the line to neutral voltages. However, in the operational mode 3 two phases are conducting and the currents follow the line to line voltage between the conducted phases which cause low order harmonic to appear in the envelope [27]. The harmonics contain odd harmonics only starting from the fifth-order harmonic [28]. The dominant harmonic is the fifth-order harmonic and its value depends on the boost ratio between the input and the output voltage as the boosting ratio increase the value of the harmonics decreases. The value of the fifth-order harmonic is eight times the value of the seventh-order harmonic which is the next largest harmonic at V0=1.62 VL-L and its vary from 30% of the fundamental component at V0=1.5 VL-L to 7% at V0=2.7 VL-L , where V0 is the output voltage and VL-L is the line to line input voltage [28]. To overcome the high distortion in the relatively low output voltage fifth-order harmonic filter can be used or variable duty ratio with harmonic injection can be added to the control circuit of the boost converter. The overall weight, size and coast of the DCM boost rectifier with fifth-order harmonic filter is higher than the DCM rectifier with harmonic injection and reach double in some design parameters [28].

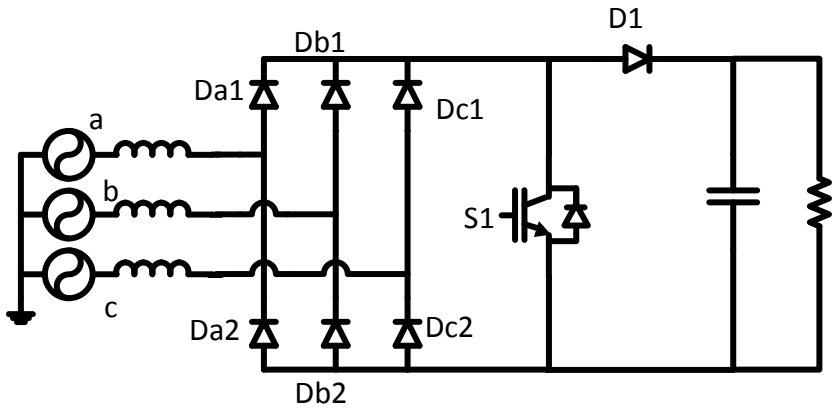


Figure 9 PZ topology

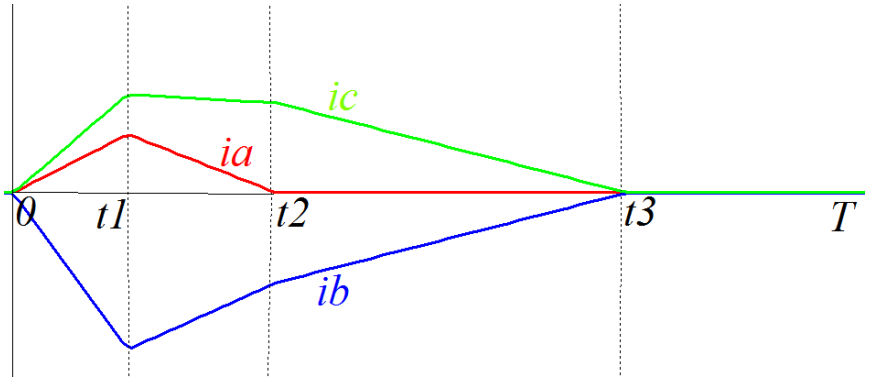


Figure 10 Input current wave form

2.2 Proposed system

The proposed three phase rectifier figure 11 consists of two main power converter stages. The first stage is three unites of three-phase rectifiers with three ac line inductors and three-phase diode bridge for each unit and a DC filter capacitor. The function of the first stage is to provide slightly variable DC voltage with input current complies with the harmonic standards. The variation of the voltage is due the variation of the DC load to maintain maximum power density as shown in the analysis in the next section.

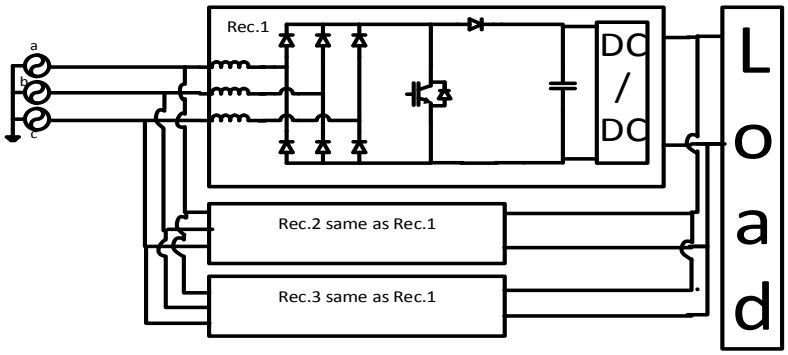


Figure 11 Proposed system of chapter 2

The second stage is a DC/DC convertor with high frequency transformer to provide galvanic isolation and to maintain the output DC voltage. Each of the three units is

basically PZ circuit with variable duty ratio control and relatively low output voltage. The objectives of having three units is to interleave the input currents such that the low order harmonic are reduced to acceptable limits and to reduce the size of the input filter so that high power density can be achieved. Moreover, the DC filter capacitor has lower current ripple as well. The boost switch in each unit is operated at constant frequency and its duty ratio is varied to meet the interleaving, harmonic reduction and DC level objectives. The reference signal for the PWM in each unit is same but the carrier signals is phase shifted 120 degree that is the first unit carrier phase shift is zero degree ,the second unit carrier phase shift is 120 degree and the third carrier signal phase shift is 240 degree. The input current for each unit is always discourteous shaped by reduced harmonic envelope while the total input current is continuous with same individual harmonic to fundamental ratio and less THD by 1.732 (√3). Since all current for each unit goes to before the end of the switching period, zero current switching is achieved. To maintain minimum output voltage for certain power level the operation of the converter is near the boundary between the continuous and discourteous mode as shown in the next section.

2.3 Analysis

In this section Analysis of the earlier mentioned proposed system is presented. Starting with the average analysis of PWM boost converter to identify the boundary between CCM and DCM modes of operation and to determine the switching frequency, inductors value, duty ratio and the output voltage for certain value of the load power. Then, analysis of direct three phase DCM rectifier is presented to determine the relation

between the boosting ratio, time at which the switching start and the duration of each of the four periods mentioned in section 2.1.2. Next, interleaving of three rectifiers to achieve harmonic reduction is presented. Also, the DC capacitor load sharing is shown.

2.3.1 Average analysis of PWM boost converter in DCM

To determine the circuit parameters value, the boundary between CCM and DCM must be known to ensure operation at DCM. The inductor current waveform at the boundary between CCM and DCM is shown in figure 12 From which

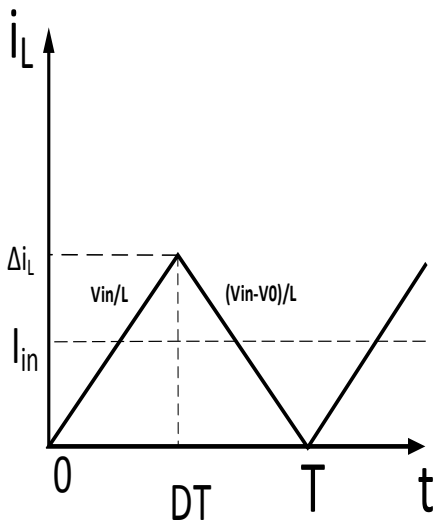


Figure 12 Boundary between CCM and DCM

$$\Delta iL = \frac{Vin * D * T}{L} \quad = \frac{V0 * D * (1 - D)}{fs * L}$$

In this case (at the boundary)

$$Iin = \ (\Delta iL/2) = \frac{V0 * D * (1 - D)}{2 * fs * L}$$

And the output current

$$I0 = \ Iin \ * \ (1 - D) = \frac{V0 * D * (1 - D)^2}{2 * fs * L}$$

Thus the output power,

$$P0 = \ V0 * I0 = \frac{V0^2 * D * \ (1 - D)^2}{2 * fs * L}$$

Figure 13 Shows the plot of the normalized output power with base= (V_0^2/ 2*f_s*L) as function of D where the curve in the figure defines the boundary between the CCM and DCM.

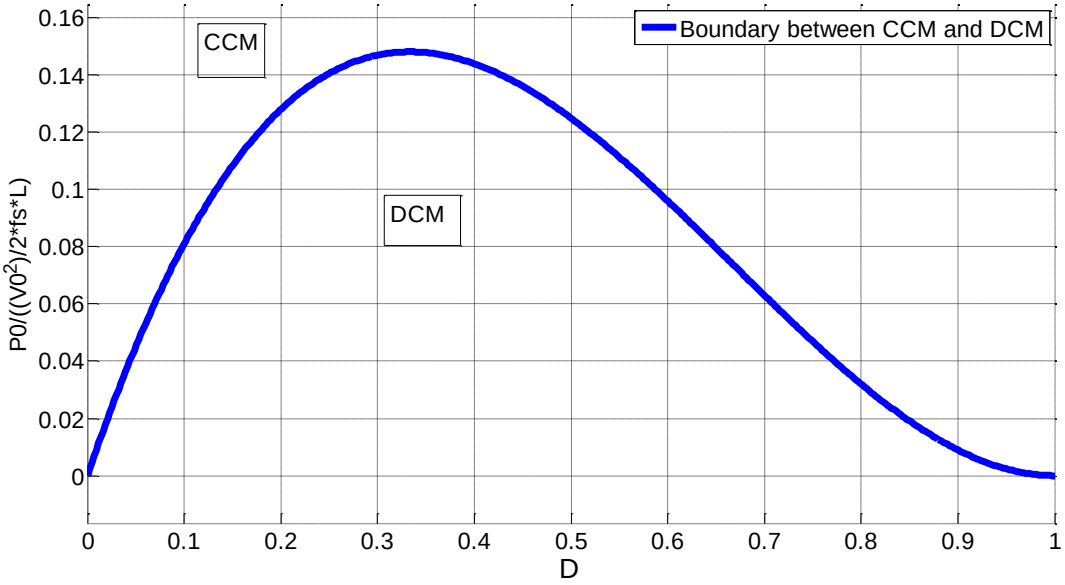


Figure 13 Normalized output power vs. D

Maximum point is point of interest. The derivative of P_0 with respect to D is

$dP_0/dD = (\frac{V0^2}{2*fs*L})$ *(1-4D+3D^2)

Equating to zero and solving for D yield P_0 maximum for DCM occurs at D=(1/3).

Substituting in the power equation above

$$P0max = \frac{4}{27}\frac{V0^2}{2*fs*L}$$

The DC voltage transfer function is given in [29]

$$MVDC = \frac{Vo}{Vin} = \frac{1 + \sqrt{\frac{2(D^2)Vo}{fsLIo}}}{2}$$

For $\frac{2fsLIo}{Vo} \leq \frac{\text{MVDC}-1}{\text{MVDC}^3}$

2.3.2 Analysis of direct three phase boost rectifier in DCM

In this section the analysis of PZ circuit with low boosting ratio presented in 2.1.2 is extended. The current in each mode operation is analyzed. As in 2.1.2, the analysis is applied during the interval $0<\omega t<\frac{\pi}{6}$ with reference phase a = Van sin(ωt) and can be expanded with alternating the phases through the entire line period. By using switching frequency much greater than the line frequency average analysis of the boost converter can be applied for each of the switching period. Table 6 introduced by [30] summarize the current in each mode and time duration of each mode.

Table 6 Current equations in DCM

Line	Mode 1	Mode 2	Mode 3
a*	$i_{a=}$ sin(θ)t	$i_{a=}$ (sin(θ)- $\frac{M}{3}$)t+$\frac{DM}{3}$	$i_{a=0}$
b*	i_b = - sin(θ+60)t	$i_{b=}$(-sin(θ+60)+$\frac{2M}{3}$)t-$\frac{2DM}{3}$	$i_{b=}$ ($\frac{M}{2}$ - $\frac{\sqrt{3}\cos(\theta)}{2}$)t- $\frac{DM}{2}$
c*	i_c=cos(θ+30)t	$i_{c=}$(- $\frac{M}{3}$+cos(θ+30))t+$\frac{DM}{3}$	$i_{c=}$ - ($\frac{M}{2}$ - $\frac{\sqrt{3}\cos(\theta)}{2}$)t+ $\frac{DM}{2}$
Time duration	DT	$\frac{3Dsin(\theta)}{(M-3\sin(\theta))}T$	$\frac{MD(\sqrt{3}\cos(\theta)-3\sin(\theta))}{(M-3\sin(\theta))(M-\sqrt{3}\cos(\theta))}$ T

* The values multiplies by $\frac{Van}{L\,T}$

Where M is $\frac{V0}{Van}$, V_0 is the output voltage and V_{an} is the line to neural voltage of the supply, θ is the time at which the switching occurs, T is the switching period and D is the duty ratio. In mode four all the currents are zero.

2.3.3 Interleaving n numbers of direct DCM rectifier for high power density

The objectives of interleaving n numbers of boost rectifiers operated in DCM are:

1. Reduce the input current harmonics to comply with the technical standards.
2. Reduce the input current ripple and consequently reduce the EMI filter size which reduces the overall volume, weight and cost of the rectifier.

3. Design the rectifier parameters to operate at maximum power density.
4. Reduce the DC link current ripple which reduces the capacitor filter size.

As presented earlier the DCM rectifier suffers from high fifth order harmonic if operated with constant duty ratio. The input current harmonics as a function of the DC voltage gain is presented in [27] and shown in figure 14. The input current wave form shown in figure 10 can be interleaved so that the second demagnetization interval of the inductors in phase b and c (in this case) can be reduced by interleaving the input current of multiple rectifiers. The duty cycle is varied opposite to the sixth order harmonic in the DC link side. As a result, by reducing the fifth harmonic in the ac line side seventh harmonic increased in the ac line side. The total interleaved current should have envelope with acceptable limit of the low order harmonics. It shown in this section that the highest power density is achieved by interleaving three rectifiers this operates near the boundary between DCM and CMM.

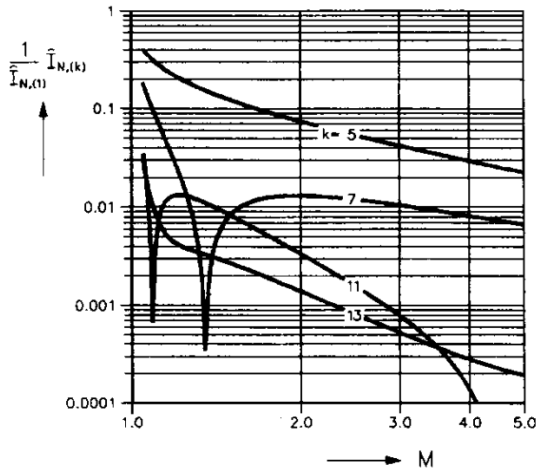


Figure 14 a) Harmonic spectrum for constant duty ratio [27]

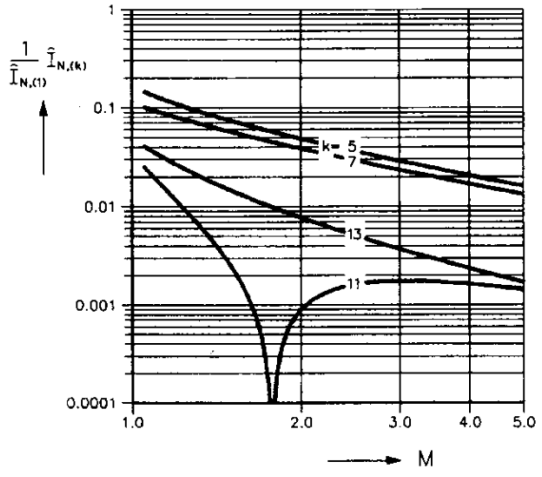


Figure 14 b) Harmonic spectrum with harmonic injection [27]

The input current of n interleaved rectifier is shifted by $\frac{T}{n}$ since the switching frequency is much larger than the line frequency. Interleaving two rectifiers result in $\frac{T}{2}$ phase shift between the switching moments of the rectifiers. From figure 13 and average analysis equations, the maximum power density occurs at D=0.333. So, for 0.5 average duty ratio, the operating point is away from the boundary between DCM and CCM which mean relatively low power density. Or, if the two rectifiers have 0.3 average duty ratio, the interleaved current has high ripple and could be discourteous. Interleaving four rectifiers limit the duty ratio to an average value of 0.25 which result in relatively low power density. Obviously, interleaving more than four rectifiers have lower power density as the rectifier numbers increase. Interleaving three rectifiers operated at average duty ratio of 0.3 results in maximum power density and low current ripple. Figure 15 shows the power density per maximum power density for 2,3,4 and 5 interleaved rectifiers.

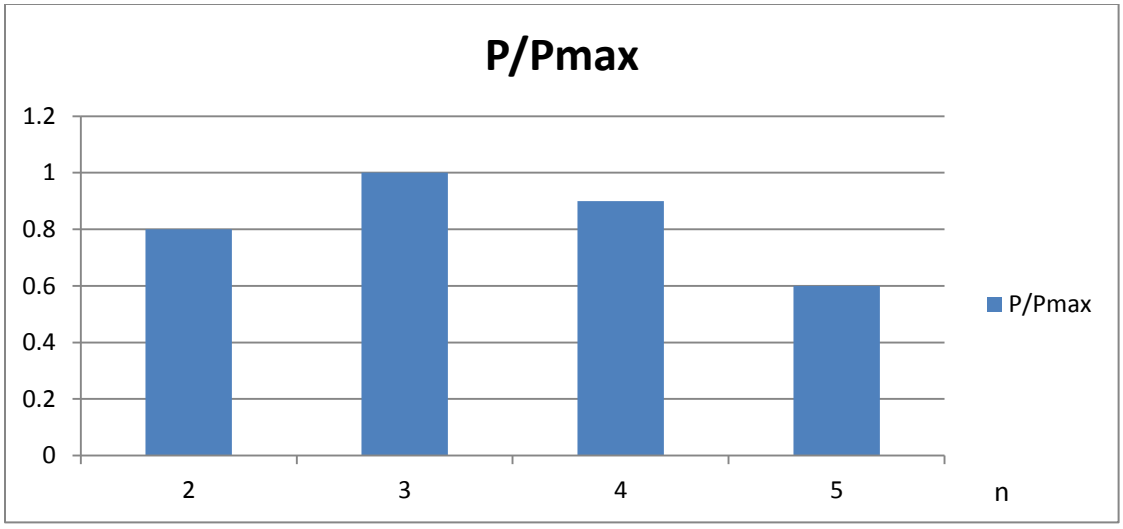


Figure 15 Numbers of modules versus power capacity

2.3.4 Maximum power density tracking

The rectifier circuit elements are design to operate at maximum power density (operating at the boundary between CCM and DCM) with constant frequency. If the output DC link voltage held constant when the load power reduced, the operating point will be in CCM region. So, to operate at the boundary, the DC link voltage should vary such that the operation point should be near the boundary between CCM and DCM.As can be seen in figure 13 at maximum power density P_o = rated power and M_{vdc}= 1.5 from which

$$\frac{Po}{2fs\,L\,Vo^2} = 0.15$$

And at M_{vdc}= 1.2

$$\frac{\text{Po}}{2fs\,L\,Vo^2} = 0.12$$

If one design for rated power at the maximum power density and track the boundary then:

$$\frac{Vo\ new}{Vo\ old} = (1.12)\sqrt{\frac{P\ new}{P\ old}}$$

2.3.5 Inputs filter design

For the three phase AC source the input filter should designed to attenuate the unwanted high frequency currents (at switching frequency) and not to cause and phase displacement between the input voltage and current to keep unity displacement power factor. Figure (16 a) shows the proposed system with the input filter. Since the filter is passive element, the design should be at the desired operating power in order to have best performance at the rating. On the other hand, the cut off frequency should be chosen to attenuate the highest possible harmonic currents which in this case in the lower power.

The filter characteristic equation is $Z_o = \sqrt{\frac{L}{C}}$ and the cutoff frequency is $f_c = \frac{1}{2\pi\sqrt{LC}}$

To avoid any phase shift at the desired power the characteristic impedance of the filter should match the equivalent resistance (R_e) of the load which for wye connected filter given by:

$$R_e = \frac{V_{L-L}^2\,(\sqrt{3}\,)}{power\ per\ phase}$$

The cutoff frequency should be selected based on the attenuation wanted at the harmonic frequency. According to [30] Table 7 give the loss per octave for the L-filter shown in figure (16 b).

Table 7 Loss per octave for the design

$\frac{fs}{fc}$	1	2	3	4	5	6
Loss per octave (dB)	12	24	36	48	60	72

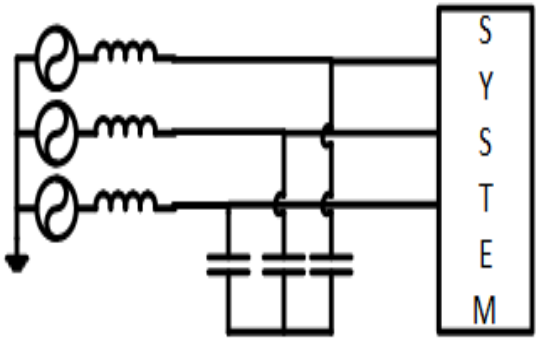


Figure 16 a) Input filter with the system

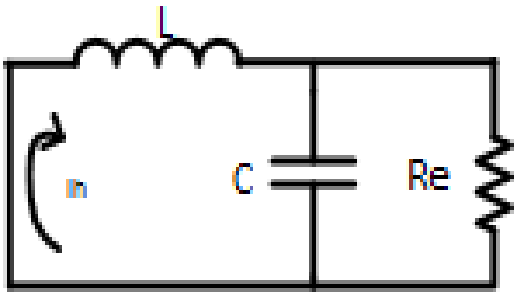


Figure 16 b) Equivalent circuit at high frequency

2.4 Design example and simulation result

Design for application of Data Center given in Chapter 1 the total output power for the rectifier is 12 KW (Po=12 KW, 4 KW in each module) from main input V_{in}=480 $V_{L\text{-}L\ rms}$. Design for maximum power Density at the rated power the boosting ratio and the DC voltage gain are m=2.47 and M_{vDC}=1.5 respectively. The output voltage is V_0= 973 V

accordingly. The switching frequency is chosen to be 70 KHz (f_s=70 KHz) at maximum power with the parameters above L can be calculated to be 100 uH (total 9). And for the input filter L_f = 53uH and C_f = 47.8 nF.

Simulation results are obtained at rated power and at half the rated power. For the rated power THD=12.4% without the input filter. After input filter THD=11.6%. Figure (17) shows the input current in each module in a) time domain wave form of the input current in each module. b) the frequency spectrum of current in a). The low order harmonics for current in a) are shown in c). It can be seen that the fifth order harmonic is reduced to 7% from figure (17 c).

Table 8 Design parameters at rated load

Rectifier inductor L	**100 uH (9 total)**
Switching frequency	**70 KHz**
Total power	**12 KW , 4KW in each module**
Input voltage Vin	**480 VL-L rms**
Output voltage V0	**973 V**
Voltage gain	**2.47**
DC voltage gain	**1.5**
Input filter inductor	**53 uH**
Input filter capacitor	**47 nf**

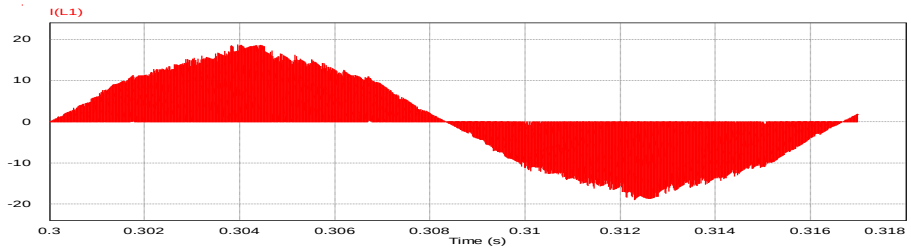


Figure 17 a) Current in each module

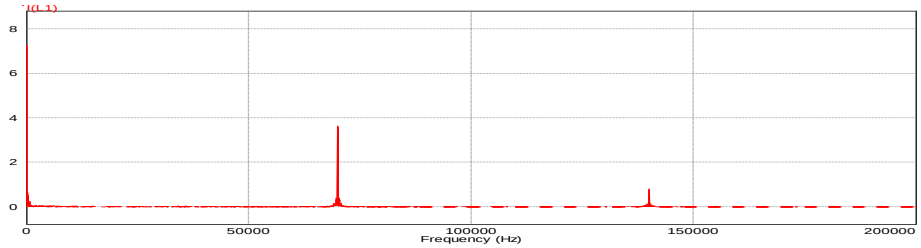


Figure 17 b) FFT for the input current for each module

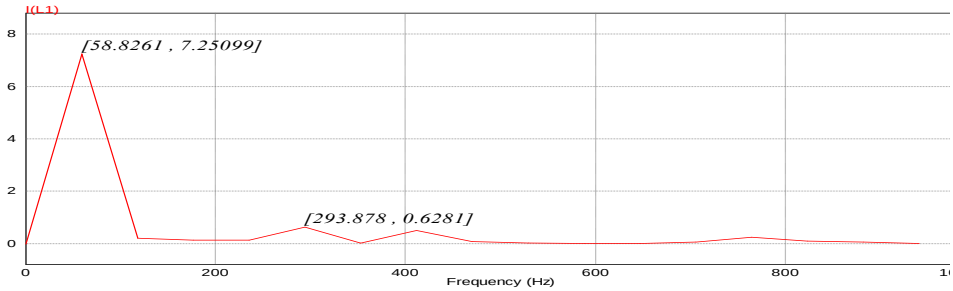


Figure 17 c) FFT for the low order harmonics in each module

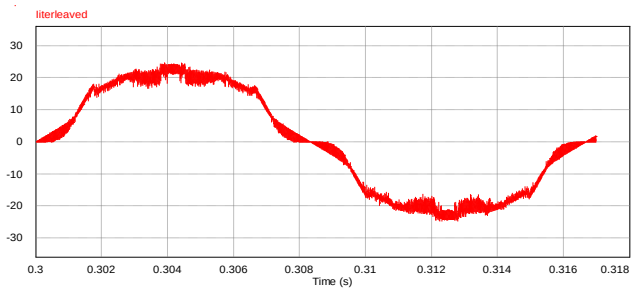


Figure 18 a) Interleaved current

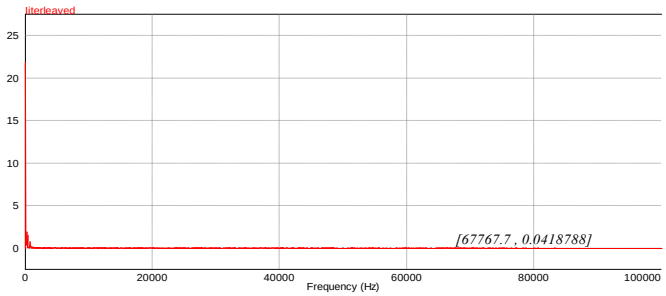


Figure 18 b) FFT for the interleaved current

Figure (18) shows the interleaved current (total input current for the rectifier) and its frequency spectrums. It can be seen that the high order harmonics (harmonics at switching frequency) are canceled which reduce the input filter size.

Figure (19 a) shows the input current and the input voltage are in phase (unity displacement power factor). Figure (19 b) shows the output voltage at rated power. And figure (19 c) shows the modulated signal of the PWM for harmonics injection.

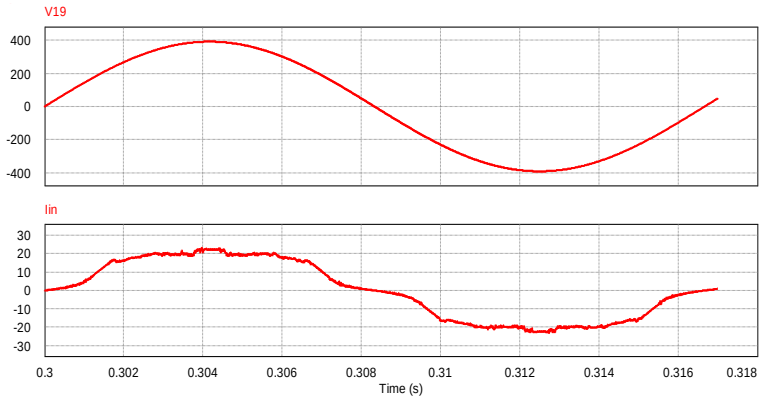


Figure 19 a) Input current after filtering and input voltage are in phase.

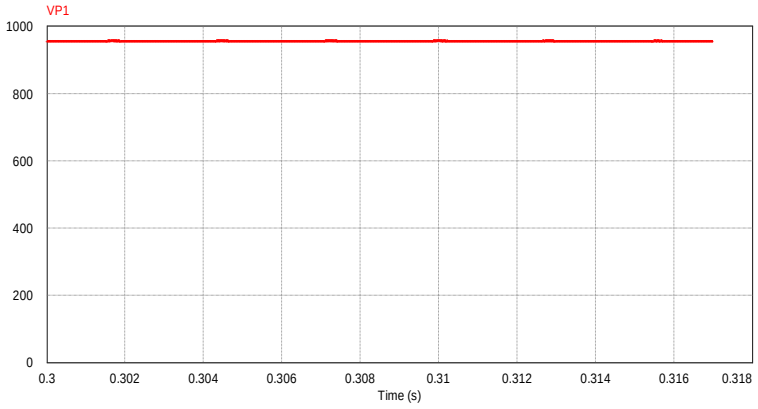


Figure 19 b) Output voltage at rated power

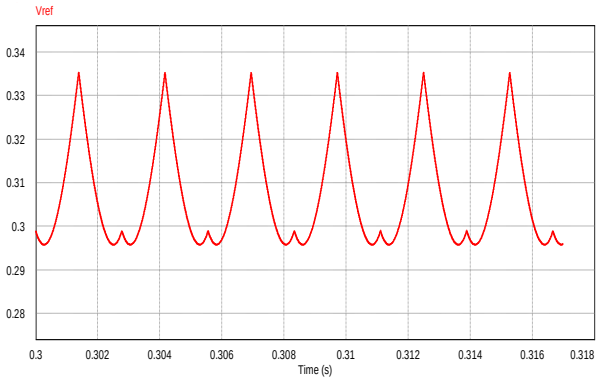


Figure 19 c) Modulated signal for harmonics injection

At half the rated (Po=6 KW, 2 KW in each module) power the passive elements remain same and the output voltage is vary to operate in DCM. According to the maximum power tracking equation the output voltage for the new power is V_0= 777 V which means m=1.97 and M_{vDC}=1.2. Simulation result for the proposed system at half the rated power gives THD=22% without input filter. And after input filter THD=16%

Table 9 Design parameters at half the load

Rectifier inductor L	**100 uH (9 total)**
Switching frequency	**70 KHz**
Total power	**6 KW , 2KW in each module**
Input voltage Vin	**480 VL-L rms**
Output voltage V0	**777 V**
Voltage gain	**1.97**
DC voltage gain	**1.2**
Input filter inductor	**53 uH**
Input filter capacitor	**47 nf**

Figure 20 shows the input current and the low order harmonics spectrum in each module at half the power the individual 5^{th} and 7^{th} order harmonics are 12% of the fundamental. The low order harmonic increased compared with the rated load case is due to the low voltage boosting ratio in case of half of the rated load.

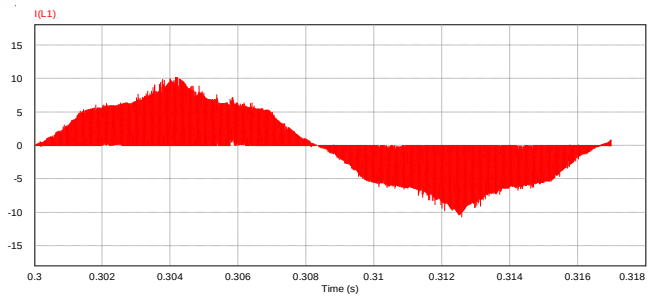


Figure 20 a) Input current for each module at half of the rated load

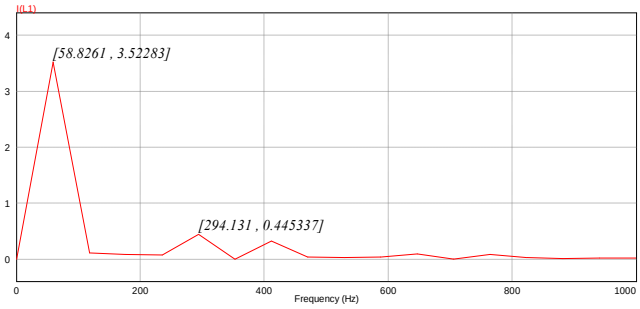


Figure 20 b) FFT for low order harmonic at half the rated load

Figure 21 shows the interleaved current (input current for the rectifier). Because the output voltage reduced according to maximum power tracking, the ripple in the interleaved current increased and hence the current amplitude at the switching frequency increased.

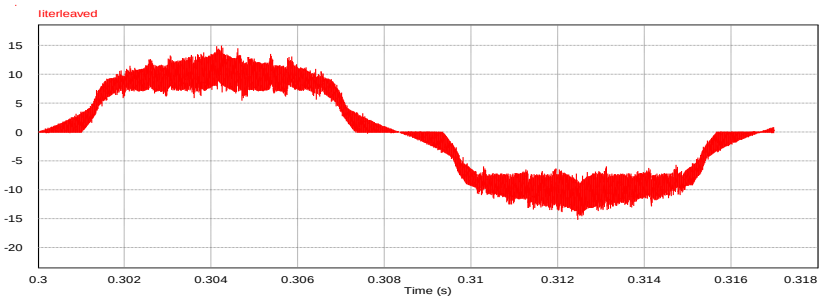


Figure 21 a) Interleaved current at half the rated load

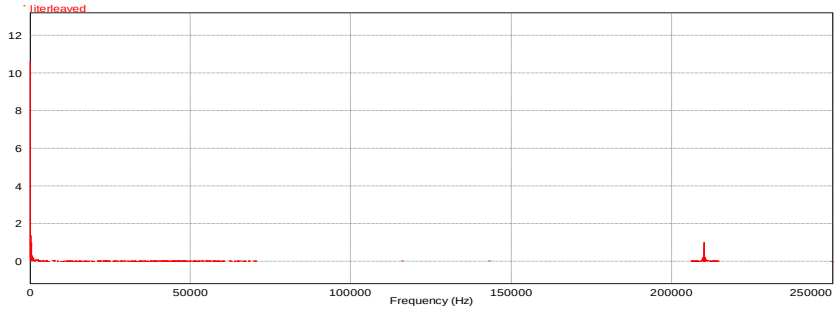


Figure 21 b) FFT for the interleaved current at half the rated load

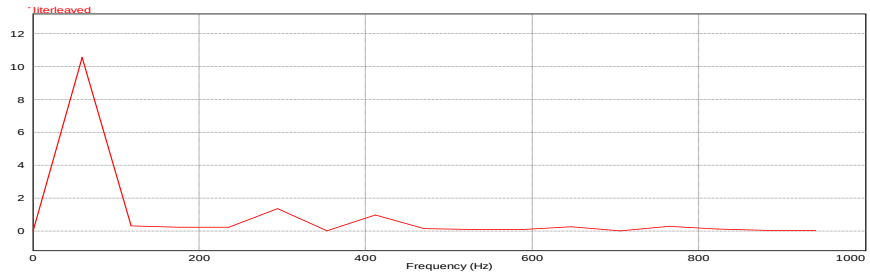


Figure 21 c) FFT for the low order harmonics for the interleaved current at half of the rated load

Figure 22 shows the input current and the input voltage after filtering in a). The phase shift just 0.132 rad. And in b) the amplitude of the input current at the switching frequency is filtered.

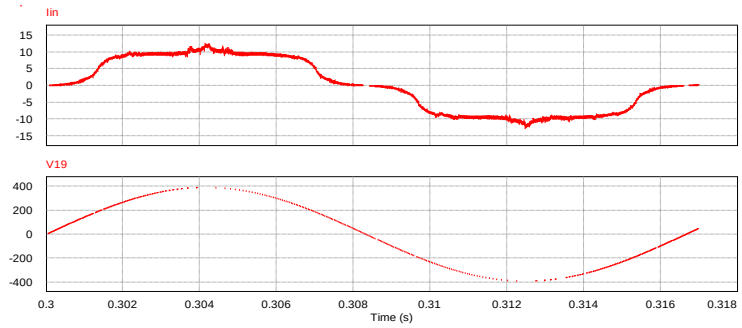


Figure 22 a) Input current after the input filter at half of the rated load

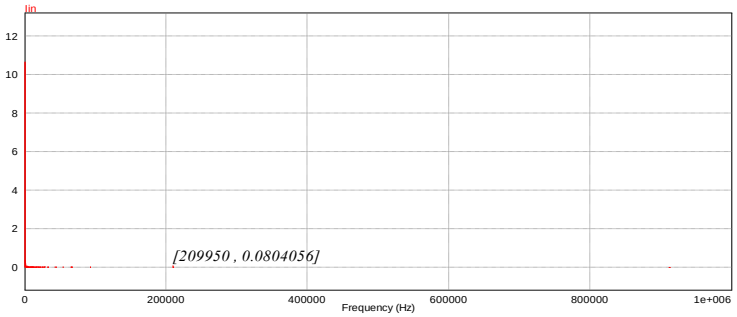


Figure 22 b) FFT for input current after input filter at half of the rated load

Figure 23 shows the output voltage. The voltage is reduced compared with rated load case to follow the maximum power density operating point. Figure 24 shows the modulated signal of the PWM for harmonic injection method.

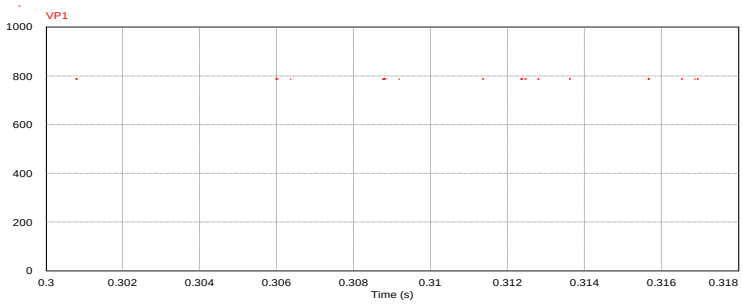


Figure 23 Output voltage at half of the rated load

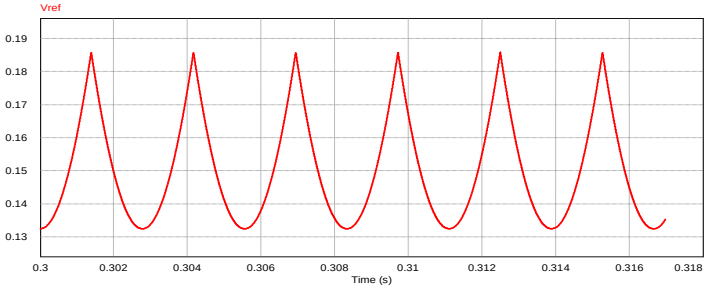


Figure 24 Modulated reference signal for harmonic injection at half of the rated load

2.5 Conclusions

In this chapter modular three phase rectifier with high power density were introduced. Interleaving the input current and vary the DC link voltage to operate at maximum power density result in the following advantages of the system:

- With semi-regulated DC link output voltage the power density increased by 3% at operation range of ($0.5P_o < P < P_o$) compared with the fixed output voltage.
- Input filter size is reduced by a factor of 15.
- Harmonic injection method reduces the fifth order harmonic of the input current from 20% to 7%.

CHAPTER III

THREE PHASE RESONANT RECTIFIER WITH HIGH INPUT POWER QUALITY AND HIGH POWER DENSITY

3.1 Introduction

Modular rectifier systems are the main supply of the telecommunication industry now a day due to the advantage of operational behavior, system technology, and coast [20]. The power conversion takes place in two stages in these systems. First, three phase diode bridge rectifier convert the ac main supply to a DC-link voltage. Second, output voltage is obtained from the DC-link voltage by a DC/DC converter with high frequency transformer connected in series with the rectifier. As can be seen from chapter 2, the conventional three phase diode bridge rectifier has high amplitude of low frequency main current harmonics. In chapter 2, harmonic injection method is used to reduce the main current harmonics. In this chapter, a resonant three phase rectifier with zero voltage switching method is used to further decrease the low order harmonics. Resonant rectifiers have been stated to be suitable for power supplies applications due to their high main current quality [31]. The proposed system in this chapter also has the advantageous of zero switching losses. The absence of the switching losses results in high over all system efficiency and high power density [32]-[33].

The proposed system equation and design aspects are derived in this chapter. Also, example and simulation results are provided.

3.2 Proposed system

The proposed system shown in figure 25 is consisting of three interleaved resonant rectifiers. Each rectifier is three phase single switch rectifier with zero voltage switching. The circuit originates from the circuit proposed in [34]. The purpose of using resonant circuit is to further reduce the low order harmonics in the direct three phase rectifier proposed in chapter 2 and to have zero switching losses due to zero voltage switching technique used. The purpose of interleaving the input current is to remove the input filter which reduces the overall rectifier size, weight and cost and to deliver constant power from the supply. The system has to stage of conversion first the interleaved resonant rectifiers cascaded DC/DC converter with high frequency transformer for each rectifier to provide galvanic isolation and to balance the output load between the rectifiers. The minimum output voltage of the proposed system is twice the line to line RMS of the source voltage and the input current has low THD. The output power is limited to a certain value due to the impedance matching of the resonant circuit. The analysis and design of the system is presented in the next section.

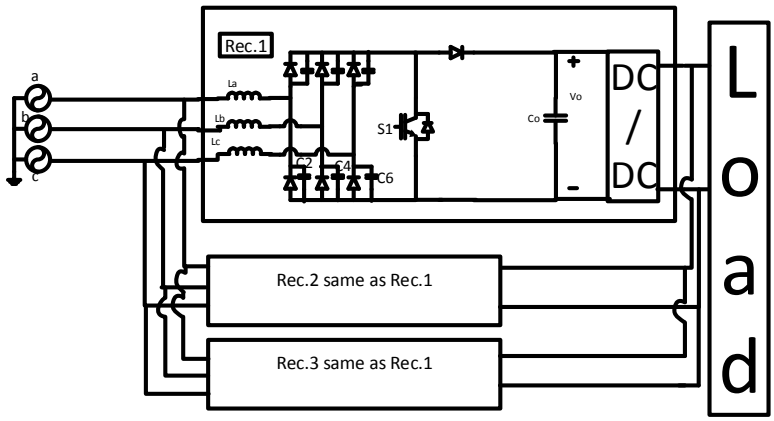


Figure 25 Proposed system of chapter 3

3.3 Analysis

In order to design the system and to know the operation limits, the analysis started with the analysis of mode of operation of each module. Next, the design characteristics and system equations are derived. Finally, interleaving the module to complete the system is presented.

3.3.1 Module mode of operations and equations

Figure 26 shows the topology of each module used in the proposed system. The DC/DC converter and the load are emulated as simple resister in the analysis in this section. The module consist of three resonant inductors in the ac side of the AC/DC converter and six resonant capacitors clamped across each diode in the three phase diode bridge as shown in figure 26. The notation in figures will be followed along the analysis in this chapter.

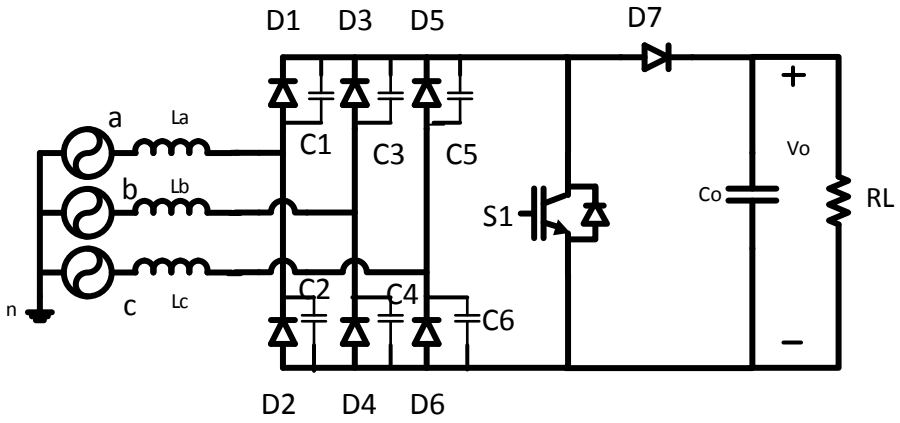


Figure 26 Module topology of the proposed system in chapter 3

Modes of operation

The analysis of the operation for one switching period is derived during the interval from θ=0 to θ=$\frac{\pi}{6}$ with input voltage $V_a = V_{PK} \sin(\theta)$ -in phase a- as a phase reference as shown in figure 27. and it can be generalized for the entire line interval with phases interchanged according to the three phase symmetry.

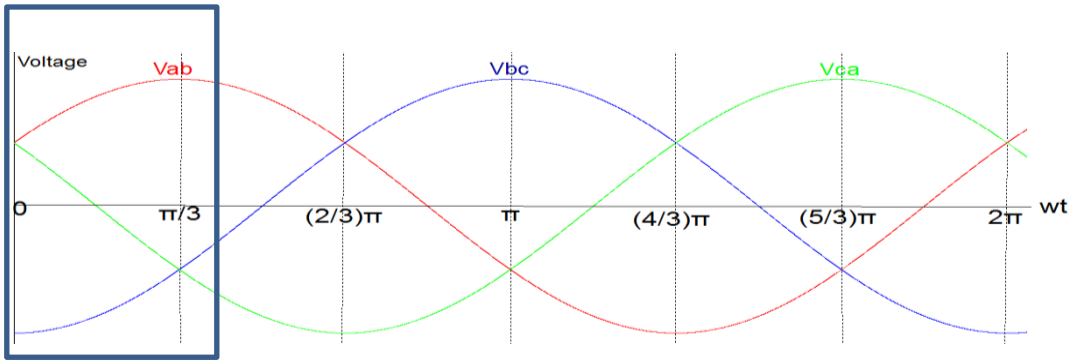


Figure 27 Main input voltage

During the switching period the current in each phase and the voltage across the resonant capacitors has six modes of operation. Figure 28 shows the modes of operation of the current in each phase with the time duration of each mode. Figure 29 shows the voltage across the resonant capacitors during each mode of operation.

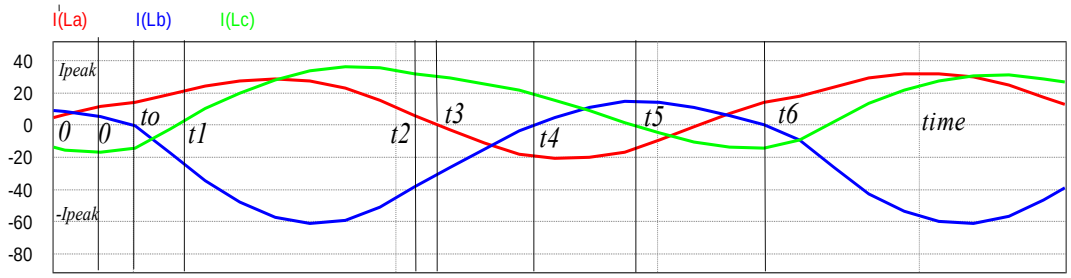


Figure 28 Main current during switching period

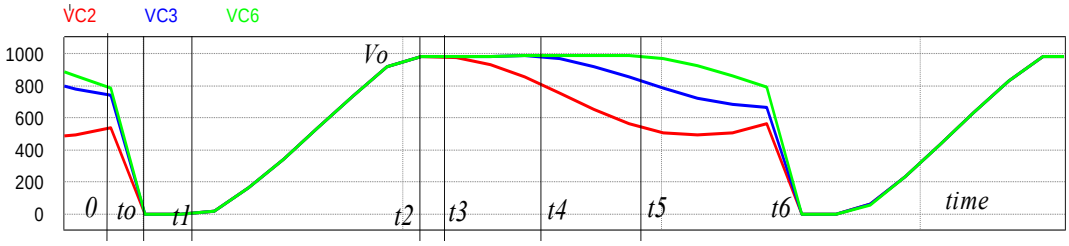


Figure 29 Voltage across the clamped capacitor during the switching period

The detailed analysis of each mode of operation is presented below:

Mode of operation 1

Operation mode 1 where the switch S1 in figure 26 is closed can be divided into interval first when the 6 clamped capacitors carry the current and no current pass through the bridge diodes till the voltage across them completely discharged as shown in figure(30 a). And the second interval of operation mode 1 when the capacitors are completely discharged and S1 closed here the currents passed through the diode bridge based on the input voltage line to neutral as shown in figure (30 b). Since the time duration of the first interval is small compared with the time duration of the second interval, the two intervals can be approximated to the second interval only which will be the case in this analysis. The effect of the first interval will be demonstrated in the capacitor current stress.

In this mode of operation and during the interval θ=0 to θ=$\frac{\pi}{6}$ D1, D5 and D4 carry the line current. The instantaneous currents equations are:

$$ian = \frac{VPK\ sin(\theta)}{L} \quad t$$

$$ibn = \frac{VPK\ sin(\theta - 120)}{L} \quad t$$

$$icn = \frac{VPK\ sin(\theta + 120)}{L} \quad t$$

for the interval from 0<t<t1 where t1=DT.

With the assumption of the current passing through the diode bridge and the resonant capacitors are completely discharged figure (30 b), the current in each phase is linearly increased in a ratio proportional to the line to neutral voltage in that phase as can be seen from the current equations above. In this mode of operation, the current equation is similar to the conventional discontinuous current mode boost rectifier equations as can be seen from the equations above and the equations of mode 1 in table 6.

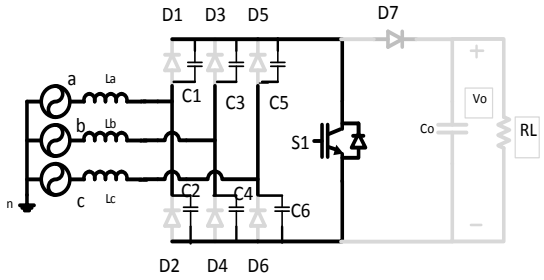


Figure 30 a) Circuit during mode 1

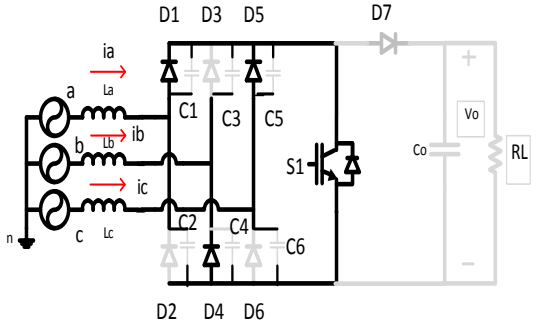


Figure 30 b) Circuit during mode 1

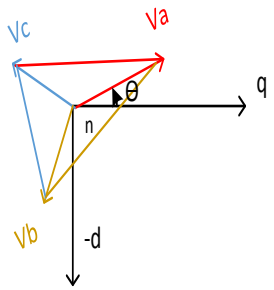


Figure 30 c) Voltage space vector during mode 1

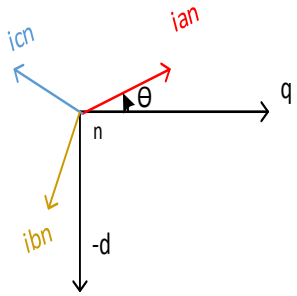


Figure 30 d) Current space vector during mode 1

Mode of operation 2

Switch S1 is open diode D7 still open since the clamped capacitors opposite to the conducting diodes is charging from zero to a final value equal to the output voltage. The

inductors current passed through diodes D1,D5 and D4 and capacitors C2, C3 and C6. The three capacitors are connected across the bridge DC terminal as shown in figure (31 a).

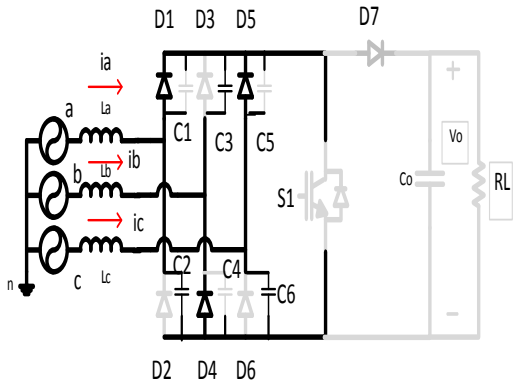


Figure 31 a) Circuit during mode 2

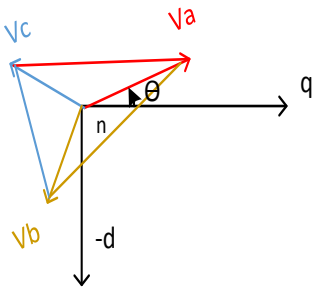


Figure 31 b) Voltage space vector during mode 2

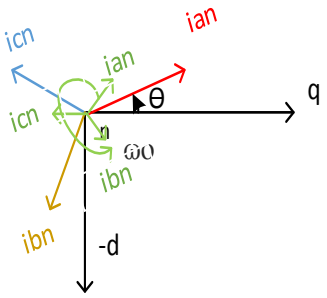


Figure 31 c) Current space vector during mode 2

With phase b as the return path for phases a and c, the instantaneous current is derived for phase b and from which the capacitor value is determined.

$$VPK\ sin(\theta - 120) + L\ di/dt\ \ + Vc = 0$$

Where V_c is the voltage across the three capacitors

From which

$$L\frac{d^2i}{dt^2} + \frac{i}{c} = 0$$

Solving for I yield

$$ibn = \frac{VPK\ sin(\theta - 120)}{L}\ DT\ cos(\omega ot) + \frac{VPK\ sin(\theta - 120)}{Zo}\ sin(\omega ot)$$

where $\omega_o = \frac{1}{\sqrt{LC}}$ and $Z_o = \sqrt{\frac{L}{C}}$

Similarly

$$ian = \frac{VPK\ sin(\theta)}{L}\ DT\ cos(\omega ot) + \frac{VPK\ sin(\theta)}{Zo}\ sin(\omega ot)$$

$$icn = \frac{VPK\ sin(\theta + 120)}{L}\ DT\ cos(\omega ot) + \frac{VPK\ sin(\theta + 120)}{Zo}\ sin(\omega ot)$$

The current in each capacitor is (1/3) i_{bn} so,

$$Vc = \frac{1}{3C}\int_{DT}^{t2} ibn\ dt$$

$$= \frac{1}{3C}\{\frac{VPK\ sin(\theta - 120)}{Zo}\ [DT\ (sin(\omega ot2) - sin(\omega oDT))$$

$$- \frac{1}{\omega o}\ (\ cos(\omega ot2) - cos(\omega oDT))\ ]\}$$

And at t2 $V_c = V_0$

Neglecting the supply resistance the peak value of the undammed system during this mode of operation occur at

$$t = \frac{\pi}{\omega o} \; that \; is \; t2 - t1 = \frac{\pi}{\omega o} \; or \; t2 = DT + \frac{\pi}{\omega o}$$

From which

$$V0 \; = \; \frac{1}{3C} \{ \frac{VPK \; sin(\theta - 120)}{Zo} \; (2) \; [\frac{cos(\omega oDT)}{\omega o} \; - \; DT \; sin(\omega oDT)]\}$$

Let A=$\frac{\omega o}{\omega s}$ where ω_s is the switching frequency

$$V0 \; = \; \frac{2 \; A \; VPK \; sin(\theta - 120)}{3} \; [\frac{cos(2\pi D)}{A} \; - \; 2\pi D \; sin(2\pi D)]$$

Operation Mode 3

Voltage across the capacitors C2,C3 and C6 reach the output voltage and the diode D7 conducted the capacitor currents are zero and the current flow through the load as shown in figure(32 a).

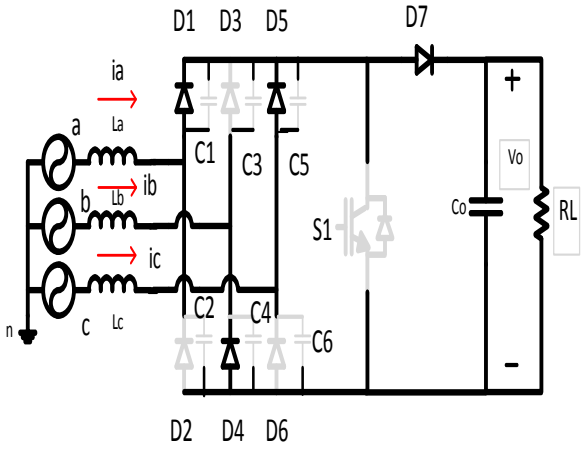


Figure 32 a) Circuit during mode 3

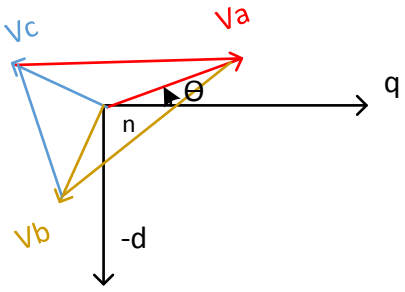


Figure 32 b) Voltage space vector during mode 3

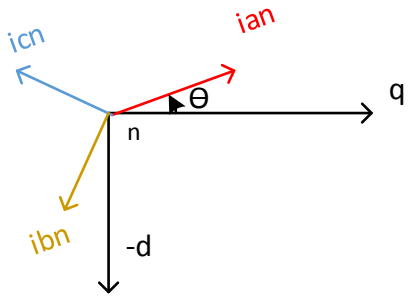


Figure 32 c) Current space vector during mode 3

The inductor current equations are

$$ian = \frac{\frac{1}{3}\,Vo - VPK\,sin(\theta)}{L}\quad(t-t2) + \frac{VPK\,sin(\theta)DT}{L}\quad cos(\omega ot2) + \frac{VPK\,sin(\theta)}{Zo}\quad sin(\omega ot2)$$

$$ibn = \frac{VPK\,sin(\theta-120) + \frac{2}{3}\,Vo}{L}\quad(t-t2) + \frac{VPK\,sin(\theta-120)DT}{L}\quad cos(\omega ot2) + \frac{VPK\,sin(\theta-120)}{Zo}\quad sin(\omega ot2)$$

$$icn = \frac{\frac{1}{3}\,Vo - VPK\,sin(\theta + 120)}{L} \quad (t - t2)$$

$$+ \frac{VPK\,sin(\theta + 120)DT}{L} \quad cos(\omega ot2)$$

$$+ \frac{VPK\,sin(\theta + 120)}{Zo} \quad sin(\omega ot2)$$

$$iD7 = ibn$$

At the end of this mode (at t3) i_{an}=0. Result in

$$t3 = t2 - [(\frac{VPK\,sin(\theta)}{\frac{1}{3}\,Vo - VPK\,sin(\theta)})\,(DT\,cos(\omega ot2) + \frac{sin(\omega ot2)}{\omega o})]$$

Or in term of A

$$t3 = t2 + (\frac{VPK\,sin(\theta)}{\frac{1}{3}\,Vo - VPK\,sin(\theta)})(\frac{1}{\omega s})\,(2\pi D\,cos(2\pi D) + \frac{sin(2\pi D)}{A})$$

And the final value of i_{bn} in this mode of operation (at t3) is

$$ibn(t3) = [\frac{-Vo}{\left(VPK\,sin(\theta) - \frac{1}{3}\,Vo\right)L}]\,(DT\,cos(\omega ot2) + \frac{sin(\omega ot2)}{\omega o})$$

With t2= DT+$\frac{\pi}{\omega o}$

$$ibn(t3) = [\frac{Vo}{\left(VPK\,sin(\theta) - \frac{1}{3}\,Vo\right)L}]\,(DT\,cos(\omega oDT) + \frac{sin(\omega oDT)}{\omega o})$$

In term of A

$$ibn(t3) = [\frac{Vo}{\left(VPK\ sin(\theta) - \frac{1}{3}\ Vo\right) L\ \omega s}]\ (2\pi D\ cos(2\pi D)\ +\ \frac{sin(2\pi D)}{A}\ )$$

Operation Mode 4

The diode D1 open and the current passed through C1 and C2 to balance their voltage with the output voltage as shown in figure (33 a)

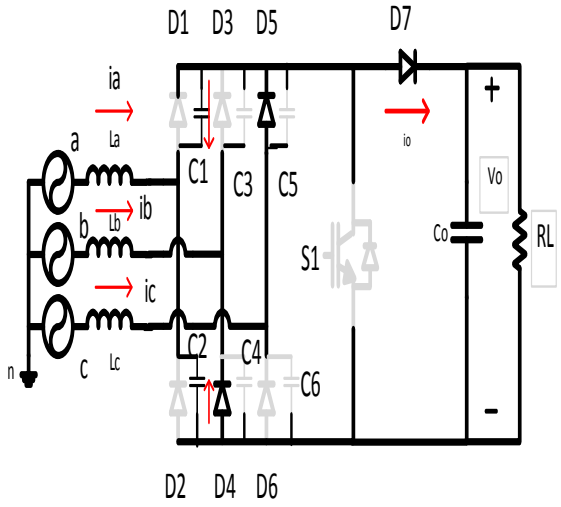


Figure 33 a) Circuit during mode 4

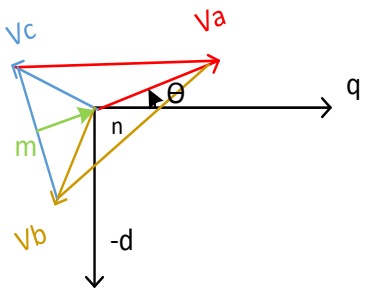


Figure 33 b) Voltage space vector during mode 4

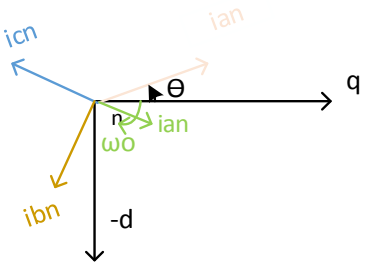


Figure 33 c) Current space vector during mode 4

The system equations are:

$$-Vcn + LC\,\frac{d^2\,Vc1}{dt^2} + L\,\frac{di_{D7}}{dt} + Vc1 + Vmn = 0$$

$$-Vbn + LC\frac{d^2 Vc2}{dt^2} + L\frac{di_{D7}}{dt} + Vc2 + Vmn = 0$$

$$Vc1 + Vc2 = Vo$$

Solving for V_{c1}, V_{c2} and i_{D7}

$$Vc1(t) = \frac{V_o}{2} + \left(\frac{V_{bn-V_{cn}}}{2}\right)\left[1 - cos\left(\omega 0(t-t3)\right)\right]$$

$$= \frac{V_o}{2} - \frac{\sqrt{3}V_{PK}cos(\theta)}{2}\left[cos(t-t3)) - 1\right]$$

$$Vc2(t) = \frac{V_o}{2} - \left(\frac{V_{bn-V_{cn}}}{2}\right)\left[cos\left(\omega 0(t-t3)\right) - 1\right]$$

$$= \frac{V_o}{2} + \frac{\sqrt{3}V_{PK}cos(\theta)}{2}\left[cos(t-t3)) - 1\right]$$

$$iD7(t) = \frac{-CV_o}{2}\delta(t) + ibn(t3) + \left[\frac{V_{cn} + V_{bn} - V_o - 2V_{mn}}{2L}\right]t$$

With balance three phase supply $V_{cn} + V_{bn} = -V_{an}$ and for neutral shifting to reduce the input current harmonics $V_{mn} = -0.5\,V_{an}$ and with small capacitance value.

$$iD7(t) = ibn(t3) + \left[\frac{-V_o}{2L}\right]t$$

$$i_{c1} = -C\frac{dv_{c1}}{dt} = -\frac{\sqrt{3}V_{PK}cos(\theta)}{2\,Z_o}sin(\omega_o(t-t3))$$

$$i_{c2} = -C\frac{dv_{c2}}{dt} = -\left(\frac{\sqrt{3}V_{PK}cos(\theta)}{2\,Z_o}sin(\omega_o(t-t3))\right)$$

$$i_{an} = (i_{c1} + i_{c2}) = -\frac{\sqrt{3}V_{PK}\cos(\theta)}{Z_o}\sin\big(\omega_o(t-t3)\big)$$

At the resonant rotating reference frame

$$(i_{bn})_{resonat\ part} = |i_{an}|\cos(\theta\text{-}120)\sin\big(\omega_o(t-t3)\big)$$

$$(i_{cn})_{resonat\ part} = |i_{an}|\cos(\theta\text{+}120)\sin\big(\omega_o(t-t3)\big)$$

$$i_{bn} = -\big[|i_{an}|\cos(\theta-120)\sin\big(\omega_o(t-t3)\big) + i_{D7}\big]$$

$$i_{cn} = \big[-|i_{an}|\cos(\theta+120)\sin\big(\omega_o(t-t3)\big) + i_{D7}\big]$$

$$\text{Where } |i_{an}| = \frac{\sqrt{3}V_{PK}\cos(\theta)}{Z_o}$$

At the end of this period $i_{bn} = zero$ at t=t4 and for balance three phase system i_{bn} should start resonate with angle 120 ahead of phase a since in the resonant reference frame the sequence is negative. So, at t4 resonant current in phase a will be at angle θ+60

$$\omega_o\,(t4-t3) = \theta + \frac{\pi}{3}$$

From which

$$(t4-t3) = \frac{\theta+\frac{\pi}{3}}{\omega_o}$$

Or in term of A

$$(t4 - t3) = \frac{\theta + \frac{\pi}{3}}{2A\pi f_s}$$

Mode of operation 5

In this mode of operation i_{bn} reach zero, capacitor C4 start charging and capacitor C3 start discharging as shown in figure (34 a).

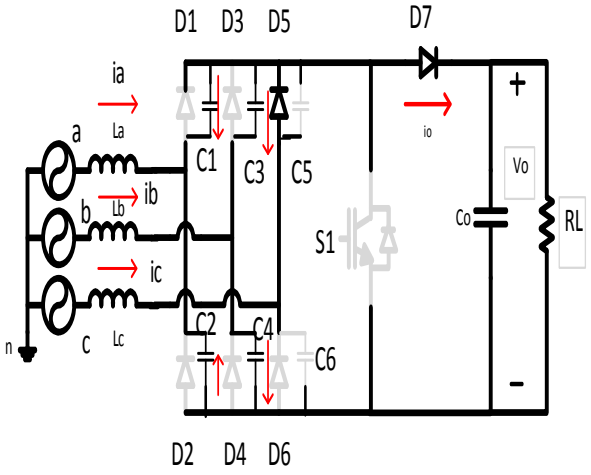


Figure 34 a) Circuit for mode 5

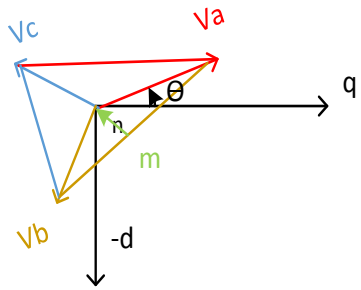


Figure 34 b) Voltage space vector in mode 5

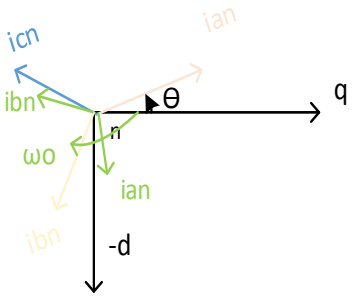


Figure 34 c) Current space vector in mode 5

The current equations are:

$$i_{C1} = i_{C2} = \frac{i_{an}}{2}$$

$$i_{C3} = i_{C4} = \frac{i_{bn}}{2}$$

$$i_{D7} = \frac{i_{cn}}{2}$$

The current in capacitor C1 and C2 continue in the same rate as in mode 4. Consequently the current in phase a continue resonating in same equation as in mode 4.

$$i_{c1} = \frac{\sqrt{3}V_{PK}cos(\theta)}{2\,Z_o} sin\big(\omega_o(t-t3)\big)\ or = \frac{\sqrt{3}V_{PK}cos(\theta)}{2\,Z_o} \sin(\,\omega_o(t-t4)) + i_{c1}(t4)$$

$$i_{c2} = \frac{\sqrt{3}V_{PK}cos(\theta)}{2\,Z_o} sin\big(\omega_o(t-t3)\big)\ or = \frac{\sqrt{3}V_{PK}cos(\theta)}{2\,Z_o} \sin(\,\omega_o(t-t4)) + i_{c2}(t4)$$

$$i_{an} = -\frac{\sqrt{3}V_{PK}\cos(\theta)}{Z_o} \sin\big(\omega_o(t-t3)\big)\ or = \frac{-\sqrt{3}V_{PK}cos(\theta)}{Z_o} \sin(\,\omega_o(t-t4)) + i_{an}(t4)$$

$$i_{c3} = \frac{\sqrt{3}V_{PK}cos(\theta+60)}{2\,Z_o} sin\big(\omega_o(t-t4)\big)$$

$$i_{c4} = -\frac{\sqrt{3}V_{PK}cos(\theta+60)}{2\,Z_o} sin\big(\omega_o(t-t4)\big)$$

$$i_{bn} = -\frac{\sqrt{3}V_{PK}cos(\theta+60)}{Z_o} \sin(\,\omega_o(t-t4))$$

$$i_{cn} = -2|i_{an}|co\,s(\theta+120) - 2|i_{bn}|cos(\theta+120)$$

At the end of this period $i_{bc} = zero$ at t=t5 and for balance three phase system i_{cn} should start resonate with angle 120 ahead of phase b since in the resonant reference

frame the sequence is negative. So, at t5 resonant current in phase a will be at angle θ+120

$$\omega_o\, t5 - t4 = \theta + \frac{2\pi}{3}$$

From which

$$t5 - t4 = \frac{\theta + \frac{2\pi}{3}}{\omega_o}$$

Or in term of A

$$t5 - t4 = \frac{\theta + \frac{2\pi}{3}}{2A\pi f_s}$$

Mode of operation 6

In mode of operation 6 all the diodes and the switch are open and the current pass throw the resonant capacitors as shown in figure (35 a). The current is resonating in each phase in LC circuit. The voltage and current phase vector in dq-plan are shown in figure (35 b) and figure (35 c) respectively.

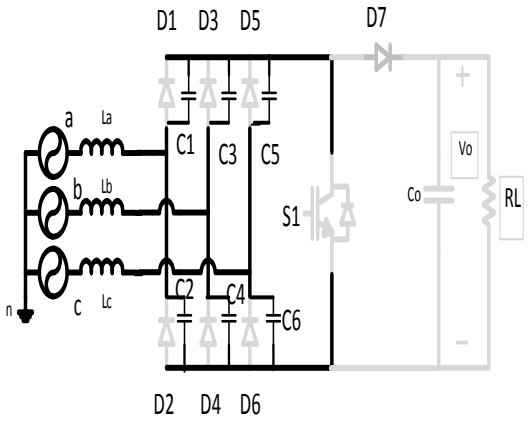


Figure 35 a) Circuit in mode 6

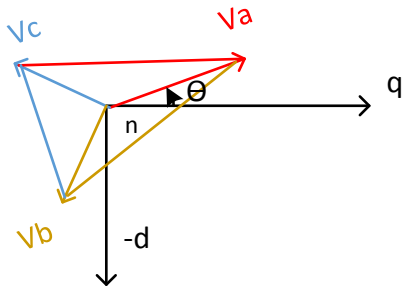


Figure 35 b) Voltage space vector in mode 6

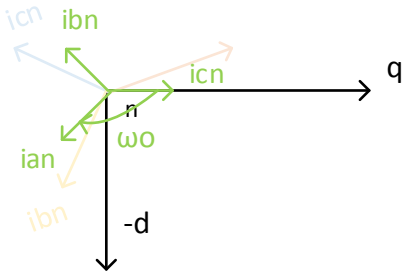


Figure 35 c) Current space vector in mode 6

$$i_{c1} = \frac{\sqrt{3}V_{PK}cos(\theta)}{2\,Z_o} sin\big(\omega_o(t-t3)\big)$$

$$i_{c2} = \frac{\sqrt{3}V_{PK}cos(\theta)}{2\,Z_o} sin\big(\omega_o(t-t3)\big)$$

$$i_{c3} = \frac{\sqrt{3}V_{PK}cos(\theta+60)}{2\,Z_o} sin\big(\omega_o(t-t4)\big)$$

$$i_{c4} = -\frac{\sqrt{3}V_{PK}cos(\theta+60)}{2\,Z_o} sin\big(\omega_o(t-t4)\big)$$

$$i_{c5} = \frac{\sqrt{3}V_{PK}cos(\theta-60)}{2\,Z_o} sin\big(\omega_o(t-t5)\big)$$

$$i_{c6} = \frac{\sqrt{3}V_{PK}cos(\theta-60)}{2\,Z_o} sin\big(\omega_o(t-t5)\big)$$

$$i_{an} = -\frac{\sqrt{3}V_{PK}\cos(\theta)}{Z_o} \sin\big(\omega_o(t-t3)\big)$$

$$i_{bn} = -\frac{\sqrt{3}V_{PK}cos(\theta + 60)}{Z_o} \sin(\omega_o(t - t4))$$

$$i_{cn} = -\frac{\sqrt{3}V_{PK}cos(\theta - 60)}{Z_o} \sin(\omega_o(t - t5))$$

Table 10 summarizes the current equation and the time duration of each of the mode of operation.

Table 10 Current and time duration in each mode

Phase	Mode 1	Mode 2	Mode 3
i_{an}	$\frac{VPK\ sin(\theta)}{L}\ t$	$\frac{VPK\ sin(\theta)}{L}\ DT\ cos(\omega ot)$ $+\ \frac{VPK\ sin(\theta)}{Zo}\ sin(\omega ot)$	$\frac{\frac{1}{3}\ Vo - VPK\ sin(\theta)}{L}\ (t - t2)$ $+\ \frac{VPK\ sin(\theta)DT}{L}\ cos(\omega ot2)$ $+\ \frac{VPK\ sin(\theta)}{Zo}\ sin(\omega ot2)$
i_{bn}	$\frac{VPK\ sin(\theta - 120)}{L}t$	$\frac{VPK\ sin(\theta - 120)}{L}\ DT\ cos(\omega ot)$ $+\ \frac{VPK\ sin(\theta - 120)}{Zo}\ sin(\omega ot)$	$\frac{VPK\ sin(\theta - 120) + \frac{2}{3}\ Vo}{L}\ (t - t2)$ $+\ \frac{VPK\ sin(\theta - 120)DT}{L}\ cos(\omega ot2)$ $+\ \frac{VPK\ sin(\theta - 120)}{Zo}\ sin(\omega ot2)$

i_{cn}	$\frac{VPK\ sin(\theta+120)}{L}\ t$	$\frac{VPK\ sin(\theta+120)}{L}\ DT\ cos(\omega ot)$ $+\ \frac{VPK\ sin(\theta+120)}{Zo}\ \ sin(\omega ot)$	$\frac{\frac{1}{3}\ Vo-\ VPK\ sin(\theta+120)}{L}\ \ (t-t2)$ $+\ \frac{VPK\ sin(\theta+120)DT}{L}\ \ cos(\omega ot2)$ $+\ \frac{VPK\ sin(\theta+120)}{Zo}\ \ sin(\omega ot2)$
i_{D7}	0	0	ibn
Time duration	DT	$\frac{\pi}{A\omega_s}$	$(\frac{VPK\ sin(\theta)}{\frac{1}{3}\ Vo-\ VPK\ sin(\theta)})(\frac{1}{\omega s})\ (2\pi D\ cos(2\pi D)$ $+\ \frac{sin(2\pi D)}{A}\ )$
Phase	Mode 4	Mode 5	Mode 6
i_{an}	$-\frac{\sqrt{3}V_{PK}\cos(\theta)}{z_o}$ $\sin(\omega_o(t-t3))$	$-\frac{\sqrt{3}V_{PK}\cos(\theta)}{z_o}\sin(\omega_o(t-t3))$	$-\frac{\sqrt{3}V_{PK}\cos(\theta)}{z_o}\sin(\omega_o(t-t3))$
i_{bn}	$-[\lvert i_{an}\rvert\cos(\theta$ $-120)\sin(\omega_o(t$ $-t3))+i_{D7}]$	$-\frac{\sqrt{3}V_{PK}cos(\theta+60)}{Z_o}\sin(\omega_o(t$ $-t4))$	$-\frac{\sqrt{3}V_{PK}cos(\theta+60)}{Z_o}\sin(\omega_o(t-t4))$
i_{cn}	$[-\lvert i_{an}\rvert\cos(\theta$ $+120)\sin(\omega_o(t$ $-t3))+i_{D7}]$	$-2\lvert i_{an}\rvert cos(\theta+120)$ $-2\lvert i_{bn}\rvert cos(\theta+120)$	$-\frac{\sqrt{3}V_{PK}cos(\theta-60)}{Z_o}\sin(\omega_o(t-t5))$
i_{D7}	$ibn(t3)+[\frac{-V_o}{2L}]\ t$	$\frac{i_{cn}}{2}$	0
Time duration	$\frac{\theta+\frac{\pi}{3}}{2A\pi f_s}$	$\frac{\theta+\frac{2\pi}{3}}{2A\pi f_s}$	$T\text{-}t5$

Table 10 Continued

The average neutral voltage during the switching cycle is

$$V_{mn\,@t4} * \Delta t4 * \sin(\theta) + V_{mn\,@t5} * \Delta t5 * \sin(\theta + \frac{2\pi}{3})$$

$$|V_{mn\,@t4}| = 0.5\,|V_{an}|$$

$$|V_{mn\,@t5}| = 0.5\,|V_{cn}|$$

$$\overline{V_{mn}} = 0.5\,V_{PK}\left(\frac{\theta+\frac{\pi}{3}}{2A\pi f_s}\sin(\theta) + \frac{\theta+\frac{2\pi}{3}}{2A\pi f_s}\sin(\theta + \frac{2\pi}{3})\right) \text{ for } 0<\theta<\frac{\pi}{6}$$

For A=2 and $V_{L\text{-}L\ rms}$=480 V the waveform of the voltage between the midpoint and the neutral is shown in figure 36. It can be seen from figure 36 that the neutral voltage is shifted every 60 degree of the line frequency. This neutral shifting compensate the modulated input currents envelopes change that occur in the conventional DCM rectifier mentioned in chapter 2 where the modulated input currents envelopes follow the line to neutral voltage of the source in the first demagnetizing interval of the inductors and the line to line voltage of the source at the second demagnetizing interval of the inductors causing low order harmonics to exist in the input currents.

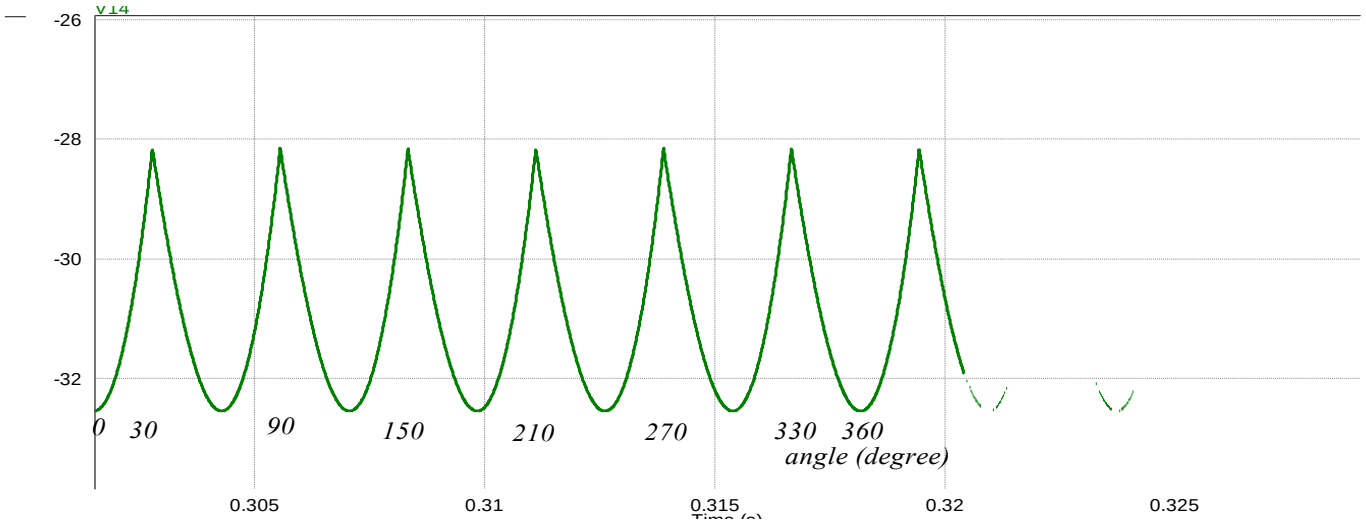


Figure 36 Neutral voltage

Because of the voltage neutral shifting shown in figure (36) the current low order harmonic is reduce.

3.3.2 Design characteristics

Two main parameters are of concern in the design of the proposed system. First, the output voltage which should be around twice $V_{L\text{-}L\ rms}$ of the supply voltage in order to operate in the operation modes mentioned in the previous subsection and consequently satisfy the neutral shifting principle to eliminate the low order harmonics in the input current. This can be clearly observe in mode of operation 4 and 5 in order to satisfy KVL half of the DC link voltage should be equal to the $V_{L\text{-}L\ rms}$. The second parameter is the output power or the effective load resister seen looking by the resonant circuit in order to match the resonant impedance. The effective resister is a factor of the D7 conduction

time (t2<t<t5) as shown later in this section. Varying the duty ratio leads to variation of the effective resistance which could be design to match range of output load power. However, in order to get proper neutral voltage t4 and t5 are of balance since the average neutral shift is the resultant of the average of the neutral voltage during these two modes of operation. In this section exploration of the circuit parameter and their effect on the operation is accomplished.

The system operates in frequency range below or equal half of the resonant frequency in order to catch the desired modulation. The output voltage is designed to be twice $V_{L\text{-}L\ rms}$ as explained based on equation

$$V0 = \frac{2\,A\,VPK\,sin(\theta - 120)}{3}\,[\frac{cos(2\pi D)}{A} - 2\pi D\,sin(2\pi D)]$$

Derived in the previous subsection the duty ratio should satisfy the conditions of design over the range (0<θ<30) degree which was the assumption of the derivation. Figure 37 shows the relation between the duty ratio and the ratio between the resonant to switching frequencies.

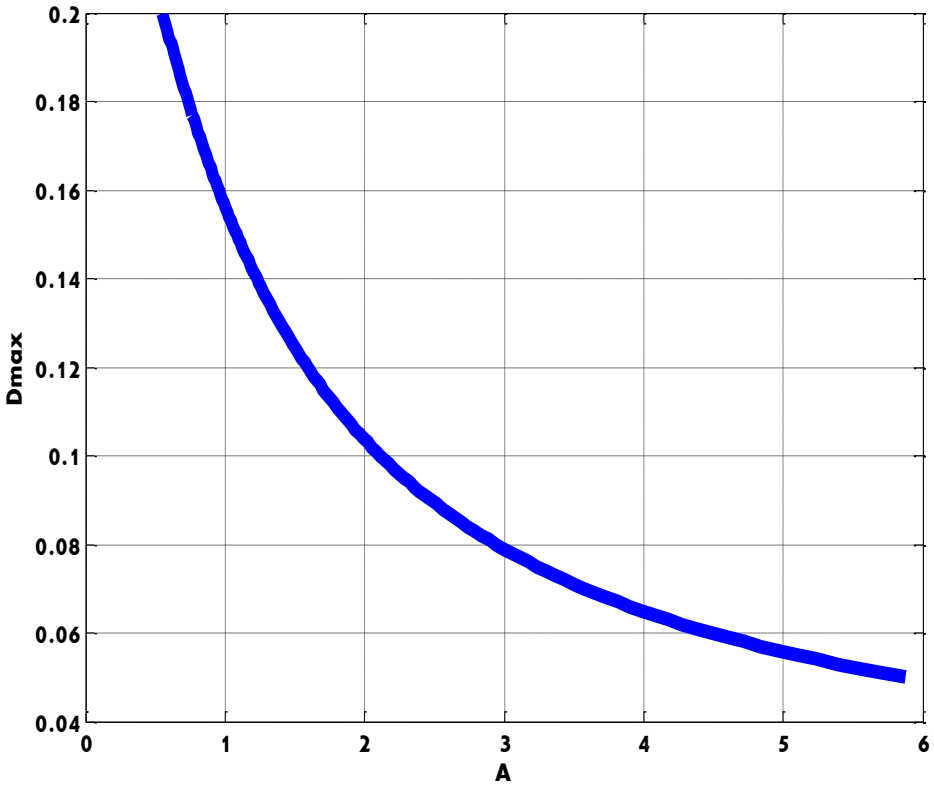


Figure 37 D versus A

The output power is limited to match the effective impedance with the resonant characteristic impedance in order to suppress the harmonics. Figure 38 shows the equivalent circuit where R_e is the effective impedance and R_L is the actual load impedance.

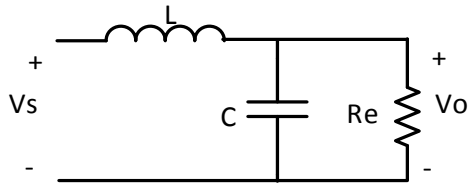


Figure 38 Equivalent circuit

$$\frac{V_o}{V_s} = -j\,\frac{R_e}{Z_o}$$

For $V_o = 2\ V_{L\text{-}L\ rms}$

$R_e = 2.7\ Z_o$

$$R_e = \frac{t3 + t4 + t5}{T} R_L$$

From which the load resistance can be found and hence the output power.

3.3.3 Interleaving system input currents

Interleaving the modules analyzed above reduce the input current ripple which reduce the input filter size and provide current path in the mode of operation where the current flow in opposite direction refer to the supply which make the supply deliver constant power. From modes of operation 1 and 2 the time at which the current rise is 0.35 the total switching time result in the maximum number of the interleaved module is three. So, interleaving 2 and 3 is analyzed.

Figure 39 shows the current waveform and the frequency spectrum of the current in each module and the interleaved current with two modules system. From which interleaving two modules result in:

- Reduce current at switching frequency but doubled the ripple at resonant frequency.
- Still have high current ripple.

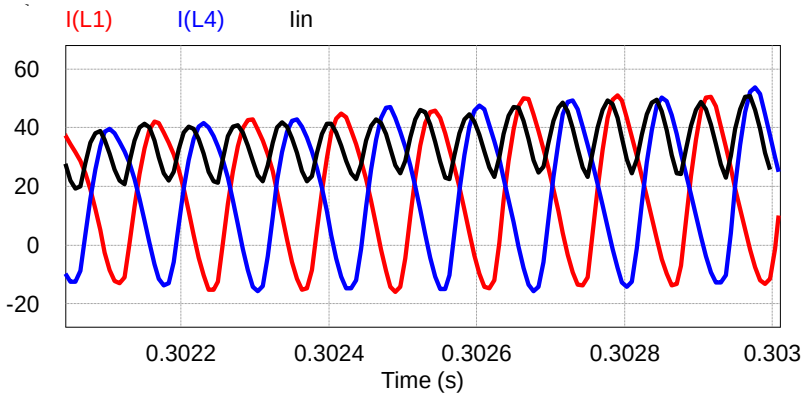
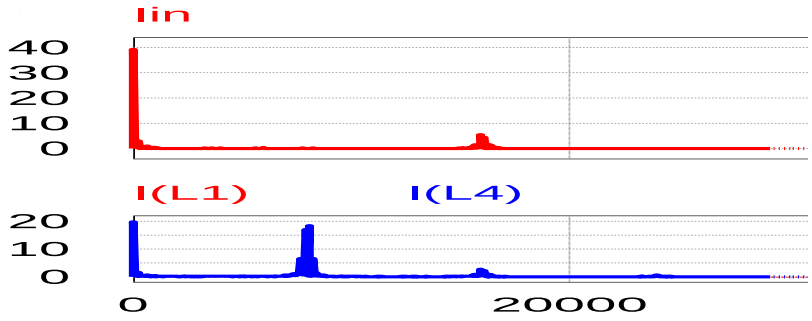
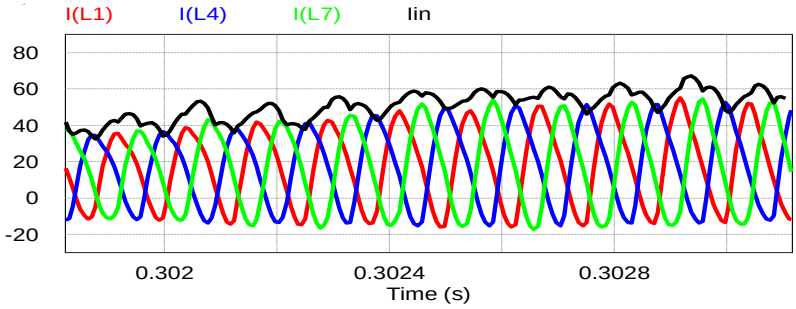


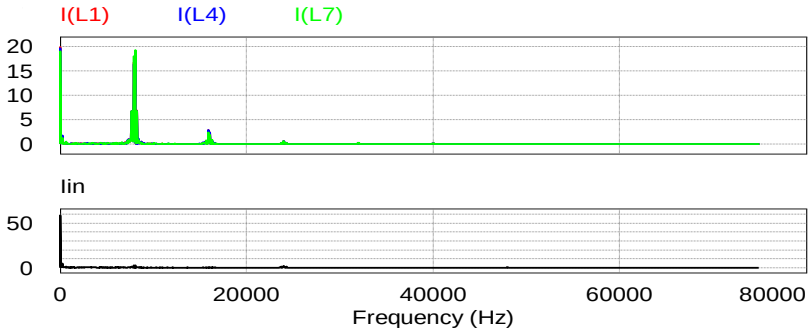
Figure 39 a) Current wave form for interleaving 2 modules



modules

While interleaving three modules reduce the current ripple at both the switching and resonant frequencies and have minimize the current ripple. Figure 40 shows the current waveform and the frequency spectrum of the current in each module and the interleaved current with three modules system.





modules

Interleaving the input current effect the average time in modes of operation 4 and 5 which effect the voltage between the midpoint of the diode bridge and the neutral and hence the input line current harmonics.

3.4 Example and simulation results

An example of 18 KW (6 KW in each module) load supplied from 480 $V_{L\text{-}L\ rms}$ supply is given. The output voltage is twice the input line-line voltage V_o= 2(480)= 960 V. load resistance for this output voltage and 6 KW power is 153.6 ohm from which the equivalent resistance is 40.5 ohm and the characteristic impedance of the resonant circuit to match the load is 15 ohm. The resonant frequency is 16 KHz and the switching frequency is half of the resonant frequency (8 KHz). From figure the duty ratio is 0.11 constant. The resonant inductor and capacitor can be found from the characteristic impedance and the resonant frequency to be 150 uH and 0.667 uF respectively. Table 11 summarizes the values for the individual module. And figure 41 shows the individual resctifier.

Table 11 Simulation parameters for individual module

$V_{L\text{-}L\ rms}$	**480 V**
P	**6KW**
La	**150 uH**
C1	**0.667 uF**
fs	**8KHz**
V_o	**960 V**

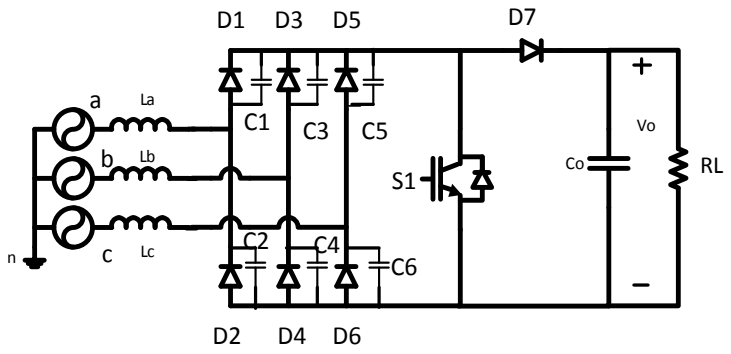
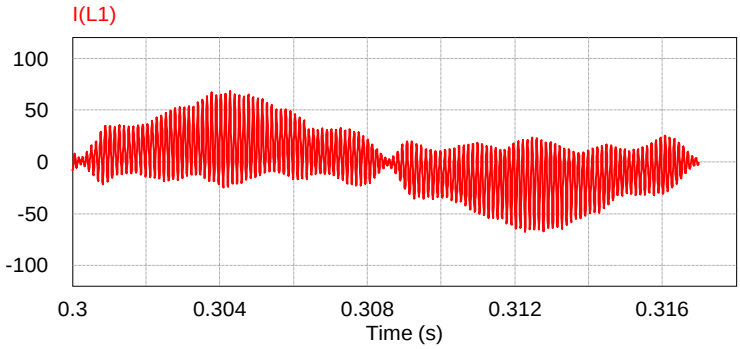


Figure 41 Circuit for parameters given in table 3-2

The input current for individual module and its low frequency spectrum are shown in figure 42. It can be seen that the 5^{th} order harmonic is 4.5% .



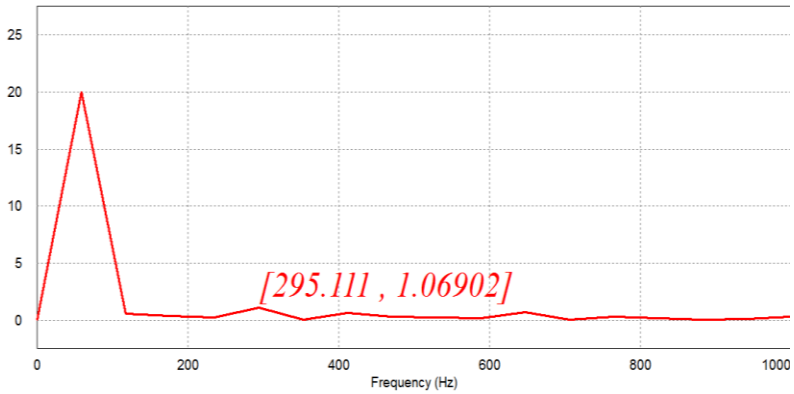


Figure 42 b) Frequency spectrum for the individual module input current

And table 12 summarize the values for the system and figure 43 shows the system.

Table 12 Parameters for the system

$V_{L\text{-}L\ rms}$	**480 V**
P	**18KW**
La	**150 uH**
C1	**0.667 uF**
fs	**8KHz**
V_o	**960 V**

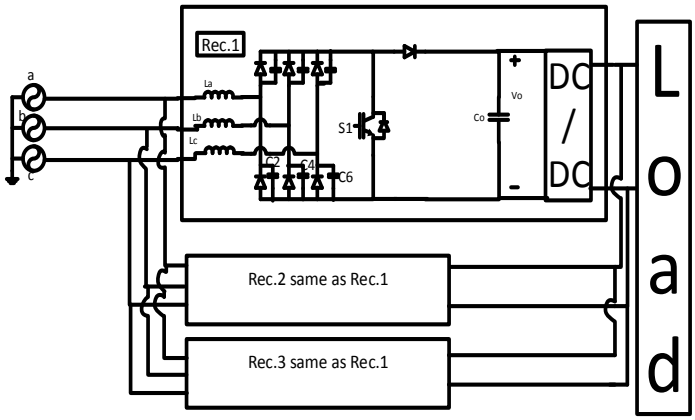
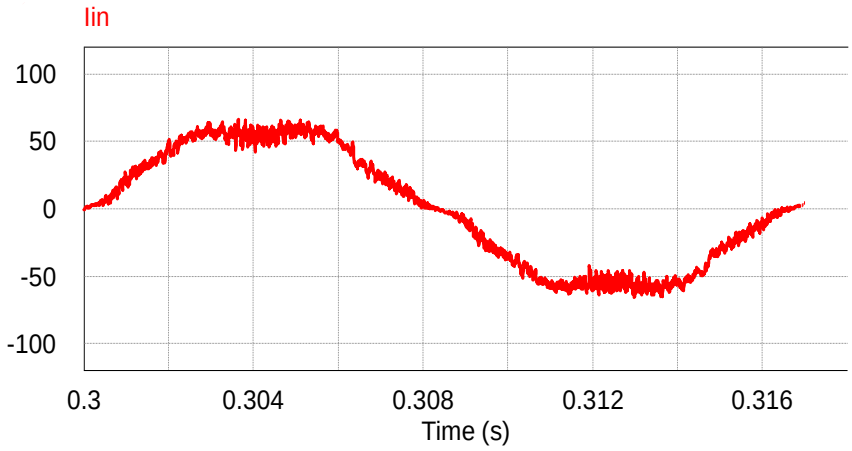


Figure 43 Circuit for the parameters given in table 12

The input current for interleaved system and its low frequency spectrum are shown in figure 44. It can be seen that the 5th order harmonic is 8.3% and the 7th harmonic is very low. The total THD is around 8.3%.



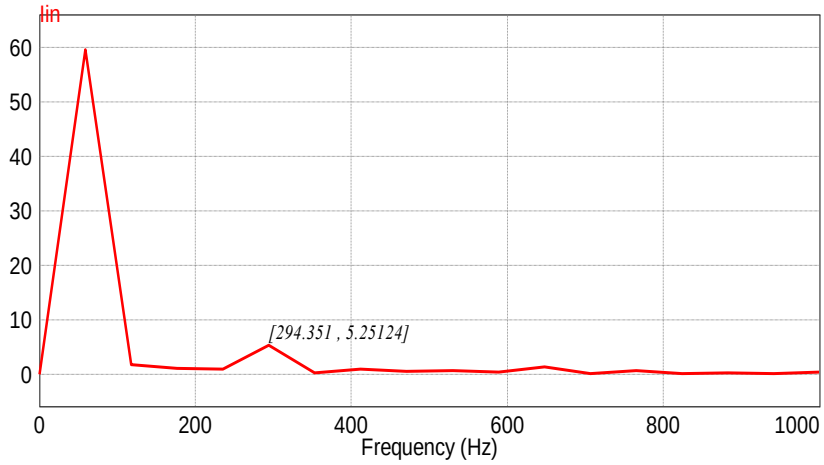


Figure 44 b) Frequency spectrum for the system input current

Figure 45 shows the full frequency spectrum. It can be seen that the interleaving suppress the current at the switching and resonant frequencies in the top compared with the individual module in the bottom.

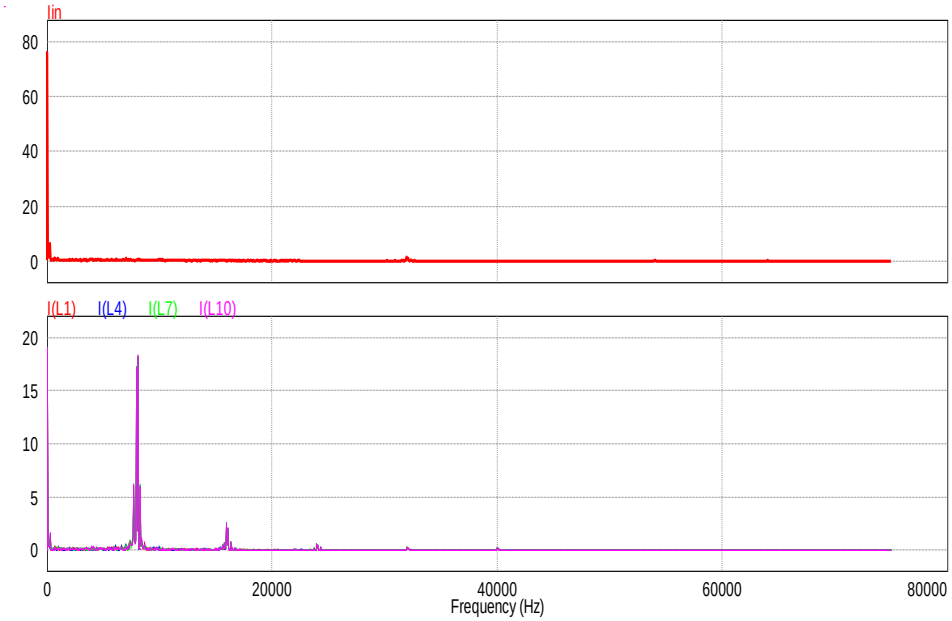
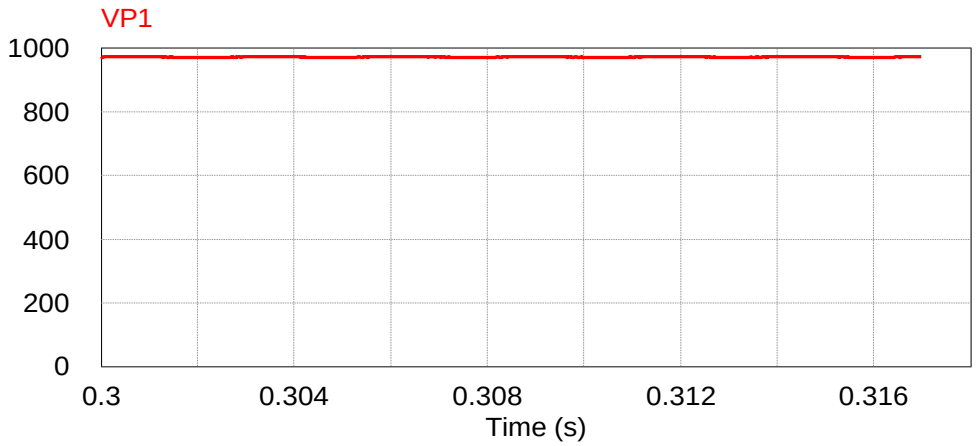


Figure 45 System input current frequency spectrum (above) versus module input current frequency spectrum (below)



Finally, Figure 46 shows the output DC voltage.

3.5 Conclusions

In this chapter modular resonant three phase rectifier with high input power quality were introduced. System equation and design characteristics were derived. Finally, example and simulation results were provided. The result can be summarized as the following:

- High input current quality utilizing single switch rectifier were achieved.
- Constant power delivered by the supply.
- No input filter required.
- No switching losses.
- Operate for certain output voltage $V_o=2\ V_{L\text{-}L\ rms}$.
- Operate for narrow output power rang if individual low order harmonics limited to 4%.

CHAPTER IV

A MODULAR THREE PHASE POWER FACTOR CORRECTION (PFC) APPROACH WITH TWO SINGLE PHASE PFC STAGES AND AN ELECTRONIC PHASE SHIFTER

4.1 Introduction

Rectifiers are widely used to convert main sinusoidal voltage to a DC voltage. The rectifier inputs are connected to the grid through a line transformer to provide a galvanic isolation between grid voltage and load. The rectified voltage used to supply a DC load such as telecommunication and network server industries or act as first stage power conversion process such as uninterruptable power supplies (UPS), variable speed drive (VSD) and HVDC. Three phase classic diode bridge rectifiers draw nonlinear currents with harmonics of order 6nω where, w is the angular frequency and n=1,2,3,…., Along with the fundamental frequency component which result in a high total harmonic distortion (THD) and consequently poor distortion factor (DF) and power factor (PF). IEEE standard (512-1992) recommend to limit harmonics to THD <5% for 69KV and below and provide basis for limiting the harmonic [1]. In order to meet these quality requirements, improvement of the utility interface with power electronic devices is applied by adding active filter on the point of common coupling with the utility interface or by embedded power factor correction (PFC) topology in the rectifier. Several techniques of PFC are used. Multi-pulse rectifier which consists of phase shifting transformer and three phase diode bridge rectifier are used to reduce the harmonics to multiples of the number of pulses used. This technique is mainly used in high power

applications (> 100 KW) due to their relative simplicity and robustness compared with other technique [17]. Other method employs additional resonant elements with control circuit instead of the phase shifting transformer such as boost convertor operated in discontinuous current mode with the three phase bridge rectifier. Three single phase modules with boost converter also used to reduce the THD and improve the power factor. Their output varies from 12 Vdc to 400 Vdc [3]. Main advantages of using modular PFC in three phase rectification are:

- Individual module does not effect by unbalance or distorted source.
  Each phase is controlled individually.
- Can be used for both continuous and discontinuous current mode which can be used to minimize the switch stress. [4].

Main disadvantage of this method is the amount of component used [22].One approach to minimize the modules number is presented in [19]. This approach used a transformer to combine two phases into one phase with phase shift of 90 degree with respect to the third phase as shown in figure (49(c)) and used two single phase PFC module.

In this chapter an improvement to system in [19] is proposed by replacing the transformer with AC chopper and using high frequency transformers in the DC/DC side to provide galvanic isolation as shown in figure 47.

The AC chopper is less in size, weight and cost compared with the low frequency transformer which results in higher power density.

4.2 Proposed system

The proposed system is consist of two single phase PFC module and an AC chopper consist of two bidirectional switches by means of two pairs of common emitter connected IGBTs with parallel diode as shown in figure 47 and several kilohertz input filter.

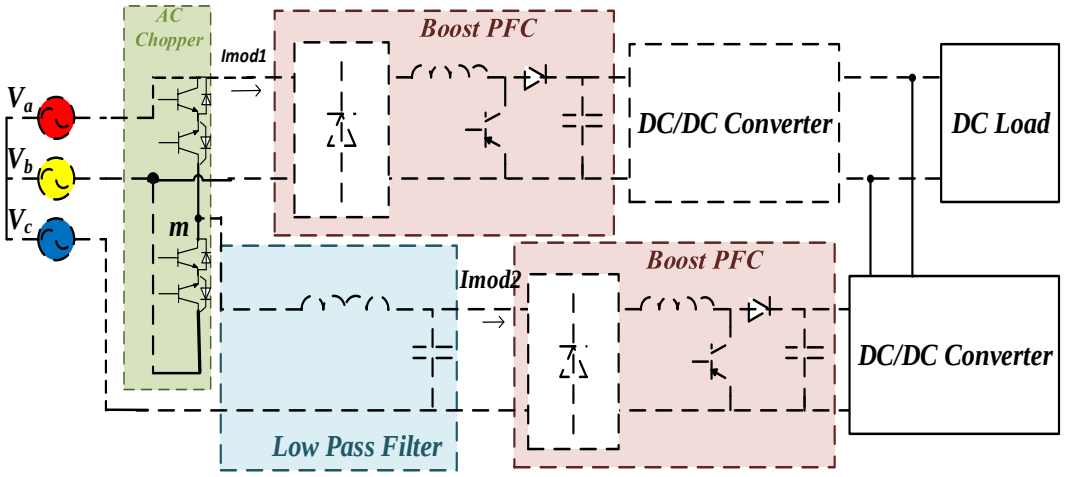


Figure 47 Proposed system of chapter 4

The proposed system is advancement of the system presented in [19] with increased power density by replacing the low frequency transformer with AC chopper. The function of the AC chopper is to generate the midpoint of two phases in a three phase system so that the phase angle between these two phases and the voltage across the

midpoint and the third phase is 90 degree as shown in figure (49 c). This transformation of three phase system to two phase system reduces the single phase module from three modules to two modules.

4.3 Analysis

Phase vector diagram of a balanced three phase line voltages form an equilateral triangle as shown in figure 48. The midpoint m lies between a and b where the vector V_{mc} is perpendicular to V_{ab} and it magnitude is equal to V_{ab} sin(60)= (0.866) V_{ab}.

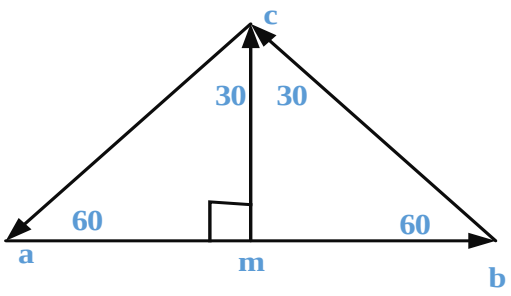


Figure 48 Phase vectors

Thus, the phase shift between V_{ab} and V_{mc} is 90 degree and V_{mc}=(0.866)V_{ab} as shown in

figure 48. The AC chopper, in figure 1, is used as electronic phase shifter to physically obtain V_{mc} from V_{bc} and V_{ca}. The AC chopper switches should operate alternatively with 0.5 constant duty ratio to get precise 90 degree phase shift. The Fourier series of the output voltage is given by

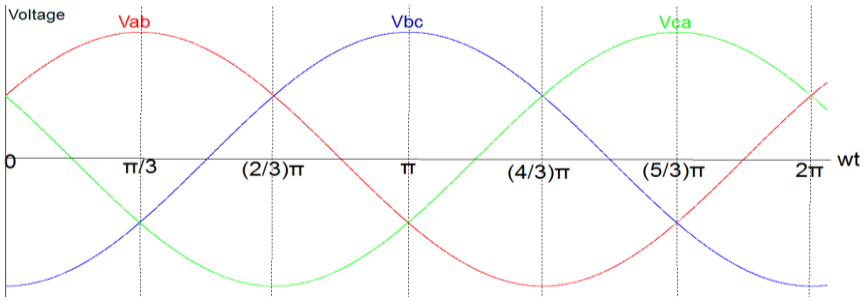
$$V_{mc} = V_{an}\, S1(t) + V_{bn}\, S2(t)$$

Where S1(t) and S2(t) is the switching function of the upper leg and the lower leg of the ac chopper respectively.

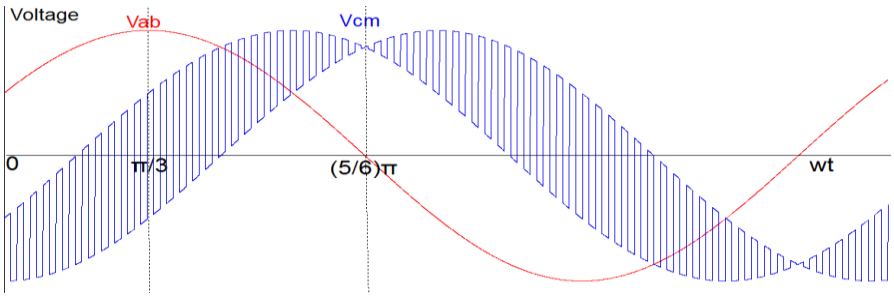
$$V_{mc} = V_{mc}\ at\ fundamental + Harmonic\ order\ at\ the\ switching\ frequency.$$

For switching frequency >> line frequency.

The three phase sinusoidal time domain waveforms are shown in Figure (49(a)) the output of ac chopper is shown in Fig (49(b)) finally the input voltage of the two PFC modules is shown in Figure (49 (c)) after being filtered with low pass filter.



(a)



(b)

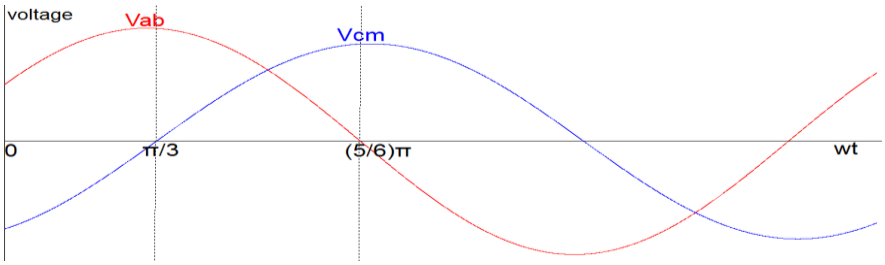


Figure 49(a) Three phase voltage wave form.
(b) The output of the AC chopper with the V_{ab}
(c) Two phase system with 90 degree phase shift.

$P_a + P_b = P_{mod1} + (1/3)\ P_{mod2}$

$P_c = (2/3)\ P_{mod2}$

For balance loading P_{mod1} should be equal to P_{mod2} results in $P_a = P_b = P_c = (1/3)\ P_{total}$.

Obviously, the power delivered from each phase should be equal in order to maintain balance currents. From equations above, the balance loading occur when the two single phase modules share the load equally. This can be achieved by controlling the single phase PFC modules to have equal DC link voltage. As a result module2, which has lower input voltage, has to boost it rectified voltage more than module1 by a factor of 0.866 which leads to $I_{mod1} = (0.866)\ I_{mod2}$ and $P_{mod1} = P_{mod2}$. Then the DC/DC convertors transform the output voltage to the desired voltage value. The two output voltages have the same value and connected in parallel to share the load.

The voltage across the bidirectional switch is $V_{L\text{-}L}$ and the current passing through it is $I_{mod2} = P_{total}/(\sqrt{3}\ V_{L\text{-}L\ rms})$. The PWM operation with dead time to avoid shorting a voltage source or overlap time to provide a path for a current in the circuit is not practical in ac/ac conversion with bidirectional switches [35]. The four step switching method proposed in [35] can be used to realize the electronic phase shifter. Figure 55 shows the gating of the switches with this method. Finally, In order to balance the filter element between the phases, three EMI filters are used which are the input line current filter, the ac chopper output voltage filter, and a filter identical to ac chopper output voltage filter placed between phases a and b. Unbalance filter impedance cause transfer

between the CM and DM noises [36], [37] and [38].

4.4 Simulation result

The design is continued for 12KW rectifier supplied from $V_{in\ L\text{-}L\ rms}$= 480 V as in chapter 2 and 3 for datacenter power supply applications. Table 13 shows the system parameters, Table 14 shows the ac chopper output filter parameters and table 15 shows the input current filter parameters. In table 15, delta connected LC filter is used as shown in figure 50.

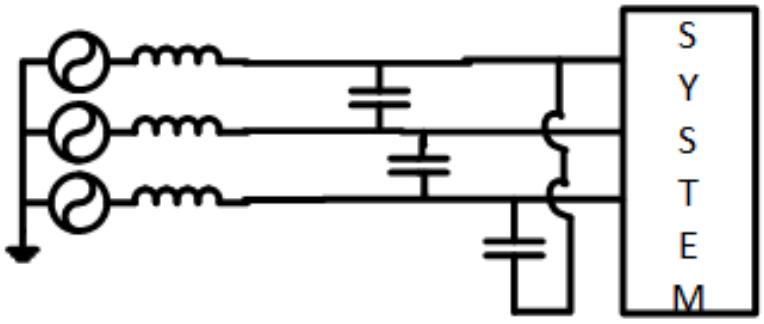


Figure 50 Delta connected LC filter

Table 13 System parameters (simulation)

$V_{L\text{-}L\ rms}$	480 V
P	12KW
fs	15KHz
V_{out}	48 V

Table 14 AC chopper output filter parameters (simulation)

AC chopper output filter	
L	100 uH
C	25 uF

Table 15 Input current filter parameters (simulation)

Input Current filter	
L	120 uH
C	25 uF

Figure 51 shows the input voltage for each PFC module as expected in the analytic results the wave forms are 90 degree apart. And the input current drawn by each PFC module for 12KW load is shown in figure 52. The total three phase input currents are shown in figure 53. It can be seen that all the currents and voltages are pure sinusoidal waves. Finally, Figure 54 shows the output DC link voltage 48V constant.

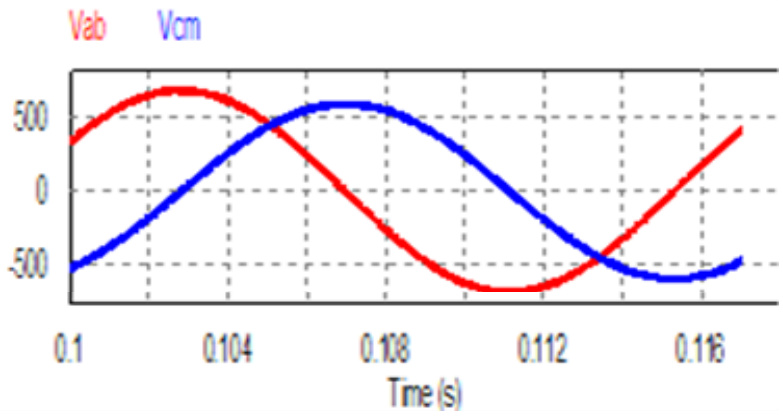
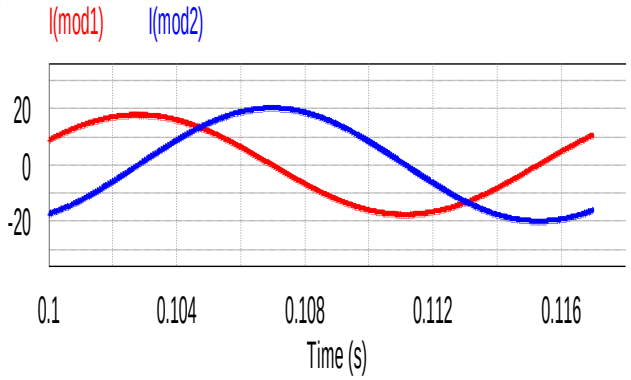
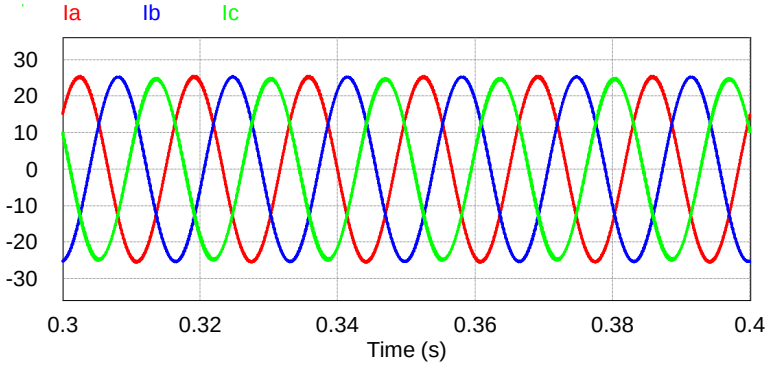


Figure 51 Input voltage for each PFC module for 480 V supply


I(mod1)
I(mod2)
20
0
-20
0.1
0.104
0.108
0.112
0.116
Time (s)

F
lo


Ia
Ib
Ic
30
20
10
0
-10
-20
-30
0.3
0.32
0.34
0.36
0.38
0.4
Time (s)

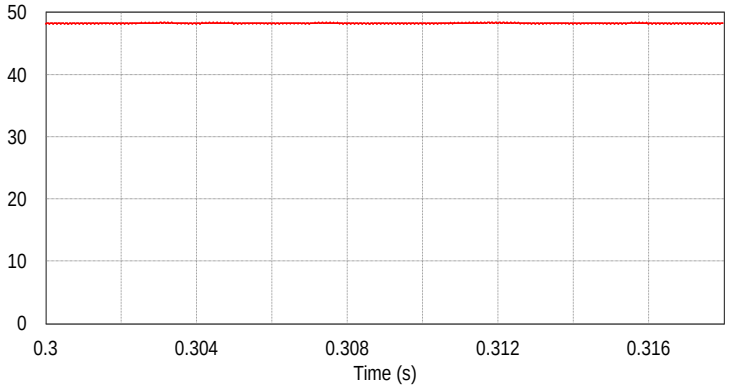


Figure 3 : Shows the output voltage of a RL load

4.5 Experimental results

A validation of the proposed system by experimental results is conducted. In the experiment, two single phase module were used with four IGBT to construct the electronic phase shifter by connecting each pair common emitter fashion to build the bidirectional switch. Four step switching method were used with load current reference to operate the electronic phase shifter. Two high frequency filters one for the ac chopper output voltage and the other for the input currents were used. The parameters of the experiment are shown in table 16, 17 and 18 for the system parameters, ac chopper output filter parameters and input line currents filter parameters respectively.

Table 16 System parameters (experimental)

$V_{L\text{-}L\ rms}$	174 V
P	420 W
fs	15KHz
V_{out}	52 V

Table 17 AC chopper output filter parameters (experimental)

AC chopper output filter	
L	330 uH
C	25 uF

Table 18 Input current filter parameters (experimental)

Input Current filter	
L	200 uH
C	25 uF

Figure (55 a) shows the four step switching method used to control the electronic phase shifter by sensing the load current and feed it back to the microcontroller to choose the switching sequence based on the load current direction. The switching frequency is 15 KHz and the duty ratio is 0.5 constant. A zoom on the edges of the wave form in figure (55 a) is shown in figure (55 b) to show the switching sequence.

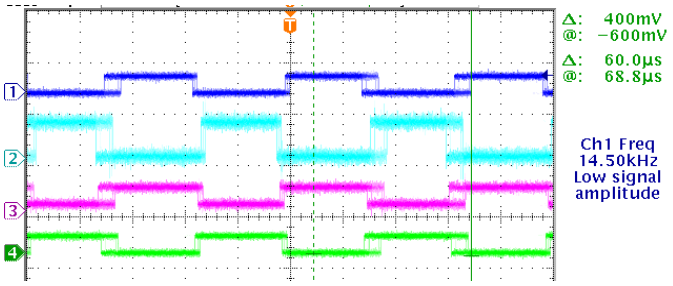


Figure 55 a) Four step switching wave form

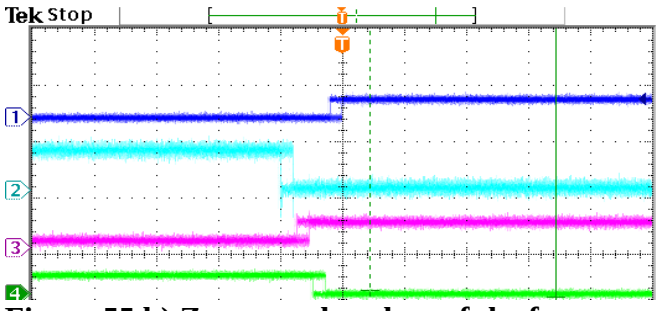


Figure 55 b) Zoom on the edges of the four step switching wave form

Figure 56 shows the input voltage for each PFC module the blue and red wave form. As expected the wave forms are 90 degree apart with amplitude 0.866 V_{L-L} for the ac chopper output voltage. Figure 57 shows the input line currents after the input filter. Finally, Figure 58 shows the input line current for phase a in the blue line (sine wave) and the red line is the frequency spectrum of the current wave from.

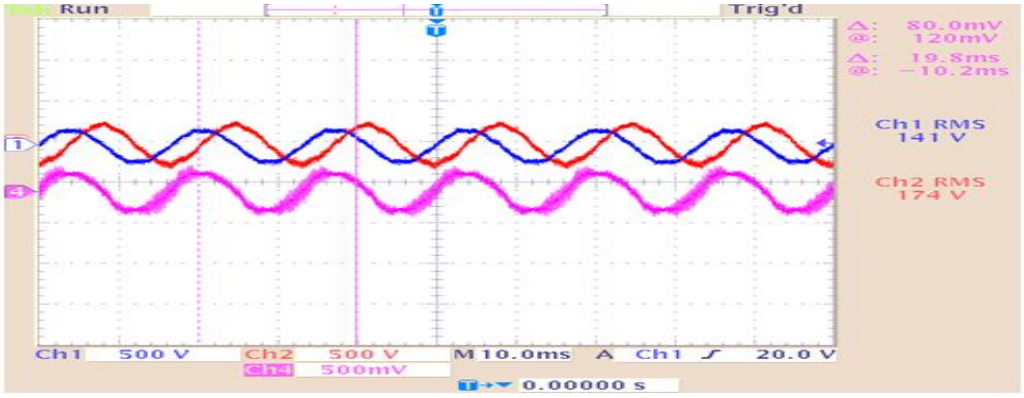


Figure 56 Input voltage for each module (Blue and Red) Input current with the input voltage (Blue and Pink)

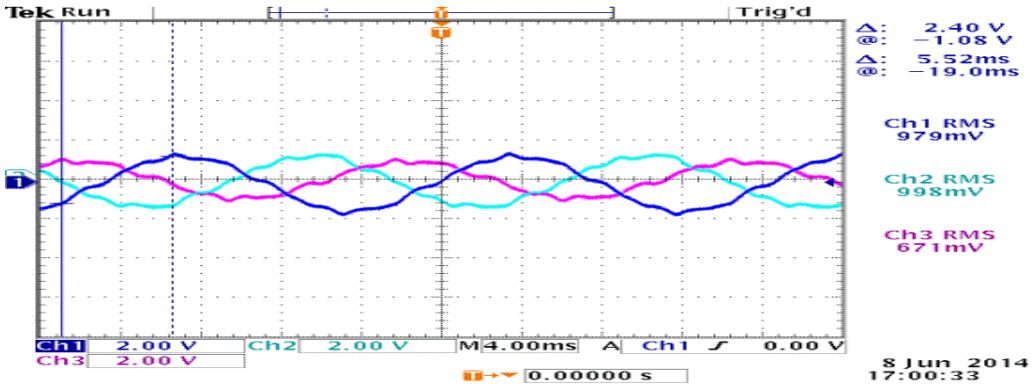


Figure 57 Input line current after filtering

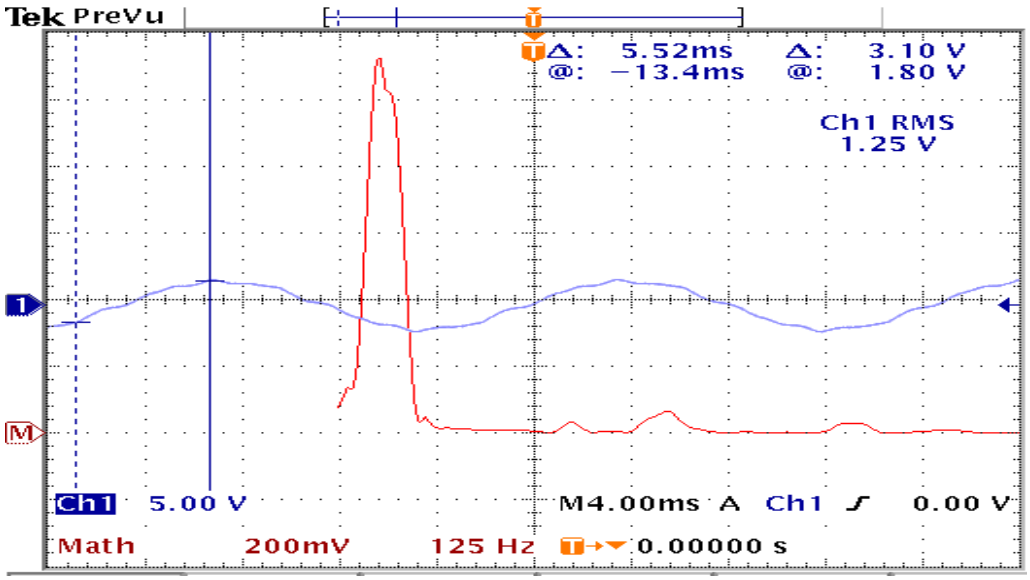


Figure 58 Input line current (blue line) and frequency spectrum (red line)

4.6 Conclusion

In this an advancement of the system presented in [19] is proposed by means of replacing the low frequency transformer with electronic phase shifter. The analyses of the system were presented. Simulation and experimental results were provided. The advantages of the proposed system are:

- Only two single phase modules are used.
- No low frequency transformer required.
- High input current quality.
- Can be operate for wide output power range.

CHAPTER V

CONCLUSION

In this thesis, three advanced active power factor correction approaches of higher power density have been proposed via development of the system in chapter 3 or interleaving the input current in chapters 2 and 3.

In the first approach (chapter 2) three modular three phase DCM boost rectifier have been interleaved for high power density by reducing the input current filter size and by having semi-regulated DC-link voltage to operate at maximum power density point. The system operates with harmonic injection method to reduce the input line current low order harmonics. In this approach, wide range of output power can be supplied. The galvanic isolation is provided by high frequency transformer in the second stage of conversion so that no low frequency transformer required. Analysis, Design example and simulation results have been presented in chapter 2. In the second approach (chapter 3), three resonant three phase modular rectifiers are interleaved to further decrease the low order input line current harmonics. In this approach the switching losses are zero, no input filter required, and no low frequency transformer. However, the system operates for narrow range of output power. The equation of each mode of operation and the design equations have been derived in chapter 3. Design example and simulation results have been provided in chapter 3. Finally, the third approach in chapter 4 is an advancement of existing system proposed in [19] by replacing the low frequency transformer with electronic phase shifter to decrees the system size and weight leading to higher power density. The system in chapter 4 can be operated for wide output power

with high input power quality and no low frequency transformer. However, the system suffers from hard switching. Design example, simulation results and experimental results have been provided in chapter 4. Table 19 shows comperes among the three approaches.

Table 19 Comperes among the three approaches

Approach	**Input line current Harmonics**	**Power Range**	**Switching Power Losses**	**Control Circuit**	**EMI Filters**	**Low Frequency Transformer**
Approach1	Medium	Wide	Low	complex	small	None
Approach2	Low	Narrow	None	simple	None	None
Approach3	Very Low	Wide	Hard switching	complex	small	None

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