POWER CONDITIONING FOR PLUG-IN HYBRID ELECTRIC VEHICLES

A Dissertation

by

BABAK FARHANGI

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Chair of Committee,	Hamid A. Toliyat
Committee Members,	Shankar P. Bhattacharyya
	Karen L. Butler-Purry
	Behbood B. Zoghi
Head of Department,	Chanan Singh

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ABSTRACT

Plugin Hybrid Electric Vehicles (PHEVs) propel from the electric energy stored in the batteries and gasoline stored in the fuel tank. PHEVs and Electric Vehicles (EVs) connect to external sources to charge the batteries. Moreover, PHEVs can supply stand-alone loads and inject power to the grid. Such functionalities have been defined as Vehicle to House (V2H) and Vehicle to Grid (V2G) and promoted by national and international policies such as the Energy Independency and Security Act (EISA) of 2007, enacted by the United States Congress. Exchanging energy between the vehicle and external sources is performed by the vehicular power conditioner (VPC). This dissertation proposes a design procedure for VPCs. The research mainly focuses on the VPC's power converter design.

A conceptual design approach is proposed to select the proper power converter topologies according to the determined power conditioning needs. The related standards and previous works are reviewed to determine the design guidelines. A set of specifications are introduced for a three port onboard VPC. This VPC is a reference for designs, simulations and experiments.

The reference VPC is implemented with a modular three-stage isolated topology that utilizes voltage source ac-dc converters as the power conditioning stages. The multiport extension of this topology extends the vehicular power conditioning concept into a novel vehicular integrated power system. All the vehicle's electric sources and loads can exchange energy in the described multiport integrated power system.

Novel design methods are proposed for the power converter, filters, magnetic circuit and control of the VPC. The practical challenges of the VPC development are analyzed. The major contributions of this dissertation include a pioneer grounding scheme for VPC considering the vehicular standards, a novel modeling approach for the Snubberless Dual Active Bridge (DAB) commutation, an innovative integrated ac inductor, and a new experimental modeling method for multiwinding transformers. The contributions are supported by analyses, simulations, and practical experiments.

DEDICATION

To Nahid, my late mother who graduated me from the school of love;

To Shahrokh, my father who graduated me from the school of life;

And, To my love Paria whom we will build our happy life.

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1. INTRODUCTION

1.1. Background

This dissertation is dedicated to power conditioning of Plugin Hybrid Electric Vehicles (PHEVs). A power conditioner processes power between the vehicle and external sources and loads. From the power conditioner standpoint, there is no difference in PHEVs and Electric Vehicles (EVs); hence, the term Vehicular Power Conditioner (VPC) is dedicated to this apparatus, which is the main subject of this research.

Power conditioning of the PHEVs is a broad research. This dissertation's scope is focused on the power converter development of VPCs. The dissertation begins with the current chapter, introduction. The introduction starts with a brief overview of electric powered vehicles and the necessity of the VPC. A survey of relevant standards introduces how the VPCs are classified and indicates the design guidelines. A conceptual design method is proposed for synthesizing the power converter topologies according to the power conditioning needs. The previously used topologies are reviewed and the novel topologies are suggested for future works. Finally, the introduction chapter presents the dissertation outline.

1.2. Problem Statement

1.2.1. Electric Powered Vehicles

Electric powered vehicles are propelled using electric motors. The EVs' history begins in the 19^{th} century. The early EVs did not last long, and the automotive industry evolved depending on Internal Combustion Engines (ICE), which are fueled by gasoline

or diesel. The limited capacity of the fossil fuels and the ICE's pollution suggested reconsidering electrical energy for transportation in the 1990's. The conceptual models of EVs have always been around; however, the first modern mass produced electric powered vehicle was a Hybrid Electric Vehicle (HEV) that has been produced since 1997. In a HEV, an electric motor and an ICE contribute to the vehicle propulsion system [1]. The early generation of HEVs consists of vehicles with an electric motor smaller than the ICE and a high voltage battery to power the electric motor. This battery has a higher voltage compared to the 14V battery, which is a common source for the starter and utility services of the vehicle. The propulsion batteries' voltage may vary between 100V to 500V in different vehicles [2]. The HEV's high voltage battery does not connect to the grid and cannot be charged from an external source. This battery is charged by regenerative breaking and is discharged contributing the acceleration of the vehicle. The battery management of an HEV tries to keep the battery's state of charge (SOC) within the desired range and maximizes the battery life. This technique can improve the fuel economy within city driving cycles that include several breakings and accelerations. However, it does not contribute as much in the highways.

In contrast to HEVs, the PHEVs connect to the electric grid. A PHEV has a larger battery that can be charged from the outside and can operate in a pure electric mode for more than 10 miles [3]. The first production PHEV models have been produced since 2011. The connection to the grid enables energy exchange between the vehicle and external sources and loads through the power conditioner. The VPC is a means of processing power. It includes a power converter circuit, control circuitry,

protections, the communication module, user interfaces and the proper enclosure. Several functionalities may be integrated into a VPC. The next subsection describes the current status and the envisioned roadmap of VPCs.

1.3. Necessity of Vehicular Power Conditioners (VPCs)

Primarily, the necessity of VPCs is due to the necessity of PHEVs and EVs. The VPCs are essential for charging PHEVs and EVs and engaging them into the smart grid functions. Electric powered vehicles can offer a number of benefits such as producing less harmful emissions, improving fuel economy, and consuming less fossil fuel. They may also offer better performance regarding noise pollution, riding comfort, and acceleration [1]. Improving the fuel economy and the vehicle and electric transportation technologies are promoted in the Energy Independence and Security Act (EISA) of 2007 by 110^{th} congress of the United States of America (Title I, subtitle B) [4]. EISA promotes energy storage for transportation and electric power in Title VI, subtitle D; moreover, Title XIII mentions the devices that allow the vehicle to engage in smart grid functions. EVs and HEVs have energy storage elements such as batteries to store energy. Such vehicles can connect to the electric grid to charge their batteries. Beyond charging the battery from the grid, a bidirectional power conditioner can inject power to the grid. This function is called Vehicle to Grid (V2G). Likewise, Vehicle to Home (V2H) is the case the battery's energy supplies the standalone loads. Increasing the prevalence of EVs and PHEVs will provide a considerable amount of energy storage capacity that can be connected to the distribution grid.

The Electric Advisory Committee (EAC) recommends policies to the United States Congress and the Department of Energy (DoE). The EAC's report investigates the PHEVs' potentials as an energy storage for the grid in three phases [5]. In phase 1, PHEV owners are encouraged to charge their vehicles off pick during nights. In phase 1, the drivers need to park their vehicles in garages with access to electric plugs. PHEVs should have smart chargers and no bidirectional power flow is needed. In phase 2, the V2H integrates the PHEV battery to the houses or the small business buildings. In this case, the battery can provide backup emergency power for the building. The other benefit of this concept is optimization of the onsite renewable energy sources by introducing the storage. The V2H requires bidirectional power flow between the grid and the battery. Phase 3 is dedicated to the full bidirectional power flow between the vehicle and the grid. Utilities may control or monitor the power flow of PHEVs to benefit the grid for load leveling, regulation, and spinning reserve. Owners receive cash back in return of their collaboration with utilities, which can encourage PHEV market penetration, as well as enabling the smart grid concepts [6].

The long term goal to 2020 and beyond is suggested in [5] to achieve full V2G implementation. Meanwhile, the short term and mid-term goals are applied research on the battery technology, the required hardware, the impact on grid, and developing standards and regulations. Establishing research centers and funding research institutes and small businesses through DoE, small and large scale demonstration activities, and supportive policies such as tax redemption benefits encourage users and big industries to move through the V2G envisioned roadmap.

Recent policies such as EISA and the related DOE programs endorse the importance of this research. As mentioned earlier, the main objective of this dissertation is proposing the suitable power converters for the VPCs. The proposed VPC will be able to perform charging, V2G, and V2H functions for the connected vehicles. As of today in 2014, such a solution is not commercialized. A few manufacturers have introduced the first generation of PHEVs; however, these vehicles have unidirectional chargers and they are not able to demonstrate the V2G concept.

1.4. PHEV Standards

Similar to the current status of PHEVs and EVs, the related standards are currently in the early stages of the development. The current standards are more focused on chargers; however, they can be extended to the bidirectional VPCs. The VPC as a distributed generator follows IEEE 1547 standard [7]. The specified vehicular standards may focus more on the inverter function of the VPC when this function would be closer to commercialization.

A PHEV needs five major components to exchange energy with the grid: the grid, a power converter, the connection between grid and the VPC, and the battery. Accordingly, a charging system includes the following components: the charging station, charging plug and charging inlet, the battery charger, and the battery. The related standards are developed for the mentioned categories by the Society of Automotive Engineers (SAE) International, Underwriters Laboratories (UL), and the International Electrotechnical Commission (IEC). Fig. 1-1 shows a diagram of a vehicular charging system and Table 1-1 includes a list of the available standards from three mentioned

institutes [8-12]. This section briefly reviews the related standards developed by SAE. In addition to SAE standards, IEEE 1547 [7], Federal Motor Safety Standards (FMVSS) [13], UL 2231-2 [14] , and National Electric Code (NEC) [15] are considered through this dissertation.

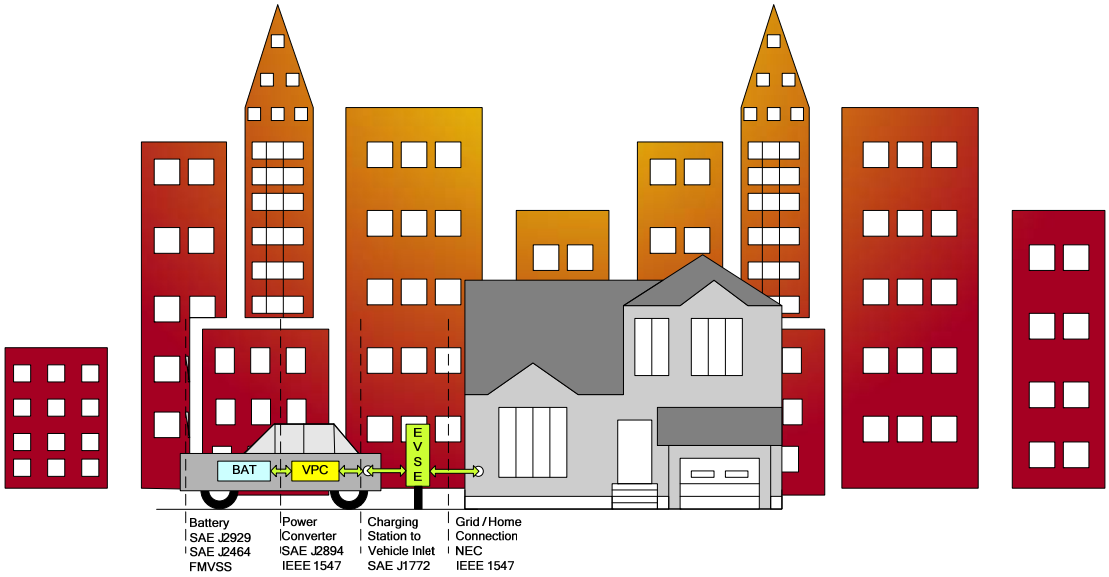

Fig. 1-1- Vehicular charging system

Table 1-1- PHEV Standards

	SAE	UL	IEC
Grid	J2293	2594, 2231-1, 2231-2	61851, 60950
Charging Plug and Charging Inlet	J1772	2251	62196
Battery Charger (On Board)	J2894	2251	61851
Battery	J2929, J2464	2202	61982, 62133

1.4.1. Grid Side Standards

The electric grid is a well established ac power system. Mature standards such as NEC [15] exist for the grid. These standards are continuously modified in order to adopt new technologies such as distributed generation. Injecting power as a distributed source is investigated in IEEE 1547 standard [7]. Also, standards have been developed describing the charging connection scheme or generally exchanging power between the grid and the vehicle.

As an example, SAE J2293 proposes a scheme to interconnect the vehicle's battery to the grid. It has two parts; SAE J2293-1 [16] describes the hardware structure and SAE J2293-2 [17] describes the communication protocol. This standard tends to describe the fundamentals of the power conversion between the grid and the battery. It states the grid has the ac electrical energy and the battery is a dc energy storage element. SAE J2293-1 proposes a power conversion scheme through an ac-ac stage and an ac-dc stage.

The ac-ac stage is not a power electronics converter and is described as a control and protection module. In the SAE scheme, this stage is the Electric Vehicle Supply Equipment (EVSE). The ac-dc stage is the charger. Both the grid and the battery have switches (relays) in the described scheme. The second part of the code describes the communications protocol in detail. This code may be followed by a compatible product; however, the content is not utilized for the dissertation's research.

Today, EVSE is considered as the charging station flagship. It is a box installed between the outlet and the cable that attached to the vehicle's inlet. The details about

EVSE have been further described in SAE J1772 [18]. Although details of the EVSE operation are not within the scope of this dissertation, the author believes such function has to be integrated into the VPC. The benefit of an integrated EVSE is that the vehicle is not limited and can access any available outlet.

1.4.2. Grid and Charger Interface

The vehicular power system is an isolated hybrid dc and ac system and the grid is a distributed grounded ac system. When these two power systems exchange energy, the interconnection is the key point to look at for the required regulations. Similarly, SAE J1772 [18] is the key standards for EV and PHEV chargers. This standard concerns the conductive charge coupler.

The conductive chargers are classified into a few categories in SAE J1772. The chargers are classified into ac and dc chargers. The ac chargers are ac-dc converters, whereas the dc chargers are dc-dc converters. The most accessible points to the grid are the residential plugs, which are 110 V or 240 V in the USA; hence, the ac chargers are more convenient. In contrast, the stationary chargers are more feasible as dc chargers.

Both ac and dc chargers are classified into three power levels. Level 1 is the lowest power level, under 1.9 kW, which is suitable for the single phase plug. Level 2 chargers can be up to 19.2 kW that is suitable for the split phase or three phase grid connections. Level 3 is the highest power level and can be up to 240 kW. The higher the power level, the shorter the charging time is. In contrast, the lower the power level, the more accessible and the more convenient it is to charge the vehicle.

The chargers are either onboard or stationary. The onboard chargers are installed on the vehicle. The onboard chargers power level can be as high as the level 2 charger. On the other hand, the stationary chargers are located outside the vehicle. The stationary chargers power level can be as high as the level 3 category. Table 1-2 summarizes the charger classifications.

Table 1-2- Charger Classification [18]

Charging Method	Supply voltage	Maximum current	Rated Power
Ac Level 1	120 V, 1 Phase	16 A	1.9 kW
Ac Level 2	208-240 V, Split Phase	80 A	19.2 kW
Ac Level 3	208-600 V 1 &3 Phase	400 A	>20 kW
Dc Level 1	200-500 V	80 A	< 40 kW
Dc Level 2	200-500 V	200 A	< 100 kW
Dc Level 3	600 V (max)	400 A	240 kW

The latest revision of SAE J1772 concerns ac level 1, ac level 2, and dc chargers. The EVSE and the connection plug are described in detail. A connection scheme between the grid, the EVSE, and the charger is described. Furthermore, SAE J1772 proposes a grounding scheme. The grounding scheme is investigated and is compared with alternative grounding methods in the second chapter of this dissertation.

SAE J1772 describes the operating sequence of the EVSE during charging and disconnection from the grid and introduces a communication protocol. As mentioned earlier, the instrumentation details are not within the scope of this dissertation.

1.4.3. The Charger Standards

SAE J2894-1 is dedicated to the PHEV charger power quality [19]. SAE J2894-1 refers to IEEE 1547 standard as the major reference and follows a similar format. The power quality factors are listed as power factor, efficiency, THD, and inrush current. Furthermore, SAE J2894 reviews the ac grid boundaries determining the grid's normal operating window.

As a summary, the recommended power factor is mentioned as more than 95%, the full power efficiency more than 90%, THD less than 10%, and inrush current has to be less than 120% of the maximum nominal current.

1.4.4. Battery Standards

The SAE battery related standards are SAE J2464 [20] and SAE J2929 [21]. SAE J 2464 is about safety and abuse testing of vehicular energy storage elements including capacitors and batteries that are above 60 V. This standard proposes routines for abuse testing of the batteries and may be considered for the battery manufacturers. SAE J2929 focuses on integration of the high voltage battery into the vehicle.

SAEJ2929 proposes test routines similar to the faults the battery may experience where located in the vehicle. Drop and mechanical shock tests and simulating vehicle fire are among the examples of test routines described by SAE J2929. From the electrical point of view, the protection failure of overcharge, over discharge, and thermal control system are investigated. In addition, the high voltage exposure protection is recommended.

SAE J2929 primarily focuses on the battery and its enclosure. A few fault scenarios may also be considered during the charger, or generally the power conditioner, design. As an example, SAE J2929 indicates the failure of the overcharge protection system should not exceed the battery's voltage. Besides a solution in the battery design, this constraint can be considered designing the VPC for more reliability. The need for manually disconnecting the high voltage system is another point raised in SAE J2929. The manual disconnection needs prompt discharging of passive elements and releasing the contactors within five seconds. The finger-proof access to the high voltage conductors is also suggested in this regard.

Noticeably, SAE J1772 refers to FMVSS 305 [13] as a safety standard available in the USA. The isolation is defined as "the electrical resistance between the high-voltage system and any vehicle conductive structure." These two facts support the investigation presented in the second chapter of this dissertation and published in [8] prior to the SAE J2929 latest release.

As the bottom line, the SAE's battery standards are oriented towards the battery manufacturing and its integration in the vehicle. Although reviewing the mentioned battery standards provided an insight, the VPC needs to operate within the safe operation area of the battery that is published by the battery manufacturer.

The presented review of the recently published standards validated the current status of the PHEVs. Several of the mentioned standards have been published or have been revised after the dissertation's proposal approval in 2010. Thankfully, the standards agree with the research performed in the dissertation. The major criticism to the SAE

recommended practice for surface vehicles is the presence of EVSE as mandatory off board equipment to charge the vehicle. This limits the convenient residential plugs for charging the EVs and PHEVs. Alternatively, this dissertation suggests integrating the EVSE into the VPC. Indeed, the alternative grounding schemes that are presented in the second chapter are within the same scope and try to make the level 1 charger compatible to all the residential grids. This attempt contributes to the prevalence of PHEVs. The VPC functionalities and classifications were introduced in this section. The introduction will present an evolutionary power converter topology review in the next section.

1.5. Power Converter Topologies

In this section, the feasible power converter topologies for the VPC are reviewed. Conventionally, the surveys read through the earlier related works and summarize and classify them. Alternatively, in this section a conceptual design approach will be provided to synthesis the power converter topologies according to the power conditioning needs of the VPC. The examples of derived topologies will be listed and the novel topologies will be highlighted for future investigation. The proposed VPC realization method is among the contributions of this dissertation. Furthermore, novel contributions are resulted from this approach that will be presented through this seciotn.

A VPC may be realized by different power converter topologies. A power converter is a non-linear time variant circuit that includes the switching networks and passive elements (inductors and capacitors). Each switching network is a power converter stage and a power conditioner may consist of a few stages.

The basic VPC exchanges energy between two major sources, the high voltage battery on the vehicle and the ac grid. The VPC is a bidirectional dc-ac converter, upon this definition. Fig. 1-2 shows a functional block diagram of a VPC. A VPC is a two-port power conditioning system that establishes a bidirectional power flow between a dc source and an ac source. In the next sub section the simplest power converter topology that enables this functionality is introduced. More complex topologies will be introduced through the section by adding more features to the VPC.

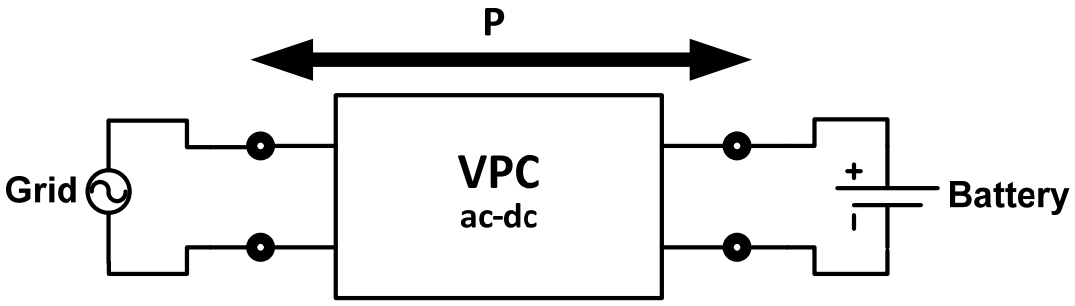

Fig. 1-2- VPC as two-port system

1.5.1. Voltage Source Differential Buck Topology

The simplest VPC topology, is realizing it with a voltage source inverter. The switches have to be two-quadrant positive blocking such as IGBTs and Power MOSFETs. This is a well practiced topology in the industries, which enhances the product development. The voltage source dc-ac inverter is derived by differentiating basic buck converters and promises low cost and high power density. For a single phase grid, an h-bridge serves as a single phase two-quadrant inverter. For a three phase, or a two phase with neutral ac grid configurations, a three phase bridge can be employed.

The voltage source dc-ac converter has a buck nature; it means the ac voltage amplitude can be as high as the dc side voltage amplitude. In the described configuration the dc side source is the battery. The batteries' voltage varies from the minimum value to the maximum value according to the state of charge and the battery's technology. This configuration may be implemented when the minimum battery voltage, at the minimum allowed state of charge, is greater than the maximum possible grid voltage.

$$V_{BAT\,(\min)} \geq A_{Line\,(\max)} \tag{1-1}$$

This is a non-isolated topology and this topology cannot be used if the galvanic isolation is required. The single-stage two-quadrant voltage source dc-ac converter is previously suggested as onboard charger [22], on board VPC [23-25], and integrated charger [11, 26-28]. An integrated-VPC utilizes the propulsion drive while the onboard VPC is a power converter separated from the propulsion drive.

This is a fully coupled power converter topology; the passive elements (filters) are located at the terminals. This is a drawback for a single phase application due the double frequency ripple. Generally the passive elements may be either placed at the line terminal, or the battery terminal. If they are located at the line terminal the switching ripple will be added to a low frequency ripple. If they are located at the battery side they will have a dc offset. This topology can also condition the dc sources as a dc-dc converter when needed. Such operation is not investigated by the literature for this particular application. The examples of stationary dc-dc converters are reviewed in [29-31]. The dual of this topology would be a current source boost inverter in which the battery voltage has to be always lower than the grid voltage [32].

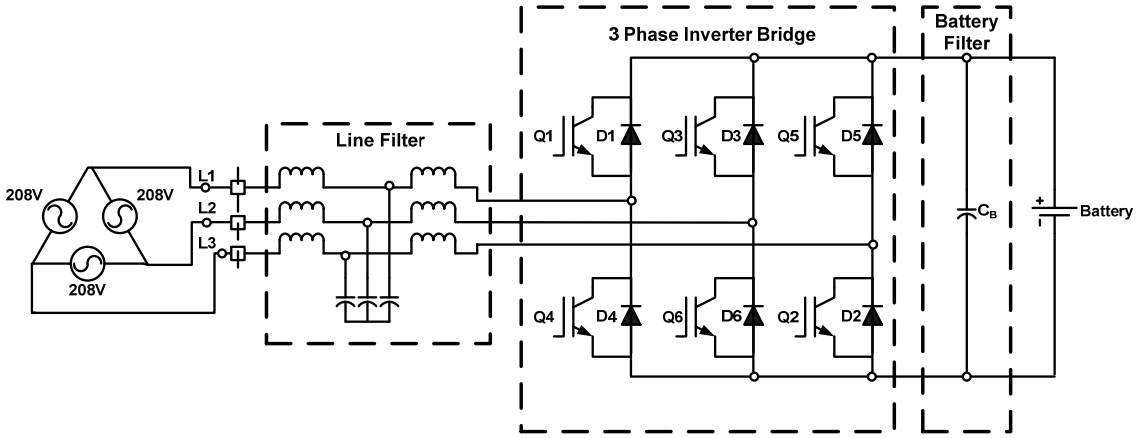

Fig. 1-3- Three phase voltage source inverter as a three phase VPC

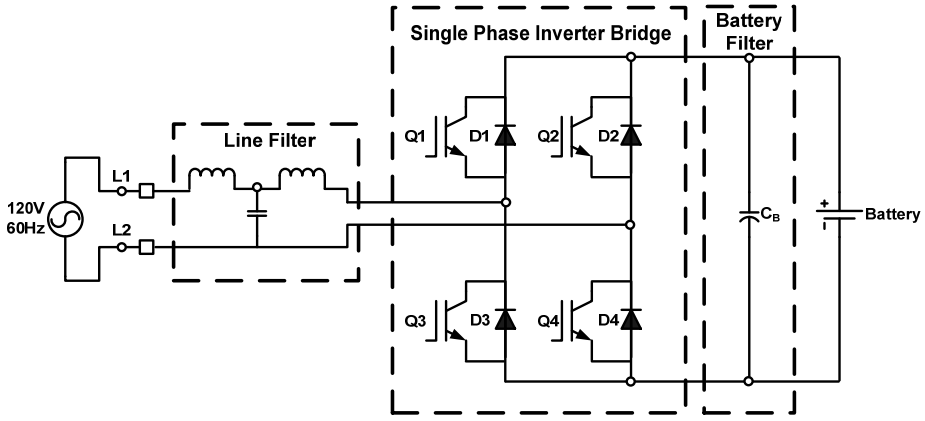

Fig. 1-4- Single phase voltage source inverter as a single phase VPC

1.5.2. Two-Stage Cascade Boost-Buck Topology

If (1-1) is not satisfied, then a boost-buck topology is required to enable a flexible power conversion between the battery and the line, independent of either side's voltage level. A boost-buck topology may be derived from differential basic buck-boost topologies including Cuk and Sepik. Fundamentally, buck-boost topologies are derived from cascading basic buck and boost converters [33, 34], and such converters are all

fundamentally two-stage converters. On the contrary, the z-source converters are single-stage solutions for implementing boost-buck converters with one switching stage [35].

The z-source converters suggest a reduced switch solution. In the single-stage solutions, the passive elements will be placed at the terminals and will have the similar drawbacks as described for differential buck topologies. Specifically, for the single phase inverters they will induce high reactive power along the converter and the passive elements will have high component losses [36, 37]. Fig. 1-5 shows a bidirectional z-source VPC. Although Z-source topology is called a single-stage approach in the literature, the presence of Q_Z in Fig. 1-5 makes it a two-stage topology according to the definition used in this dissertation.

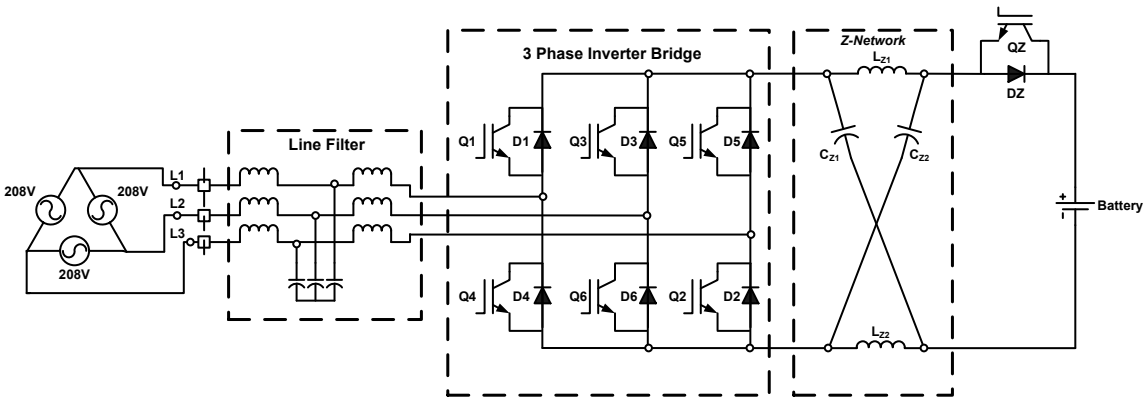

Fig. 1-5- Bidirectional z-source VPC topology

Instead of single-stage topologies, two-stage topologies can be employed. In two-stage topologies a passive network can be implemented in between of the switching stages. The passive network can be designed in a way that decouples the power conditioning of the dc side and the ac side. While in some literature the coupled

configurations are counted as innovative, the decoupling comes with advantages. In a decoupled power conditioner, the control routines of either side can be isolated from the other side; the ripple can be canceled in middle of the power conversion path; also, protections and fault isolation are easier. Thus, in a decoupled power conditioner there is more design flexibility for designing passive elements. Moreover, the switching networks can condition the passive elements.

The most basic decoupled voltage source two-quadrant power conditioner topology can be realized by cascading a synchronous buck converter and an h-bridge converter, which was introduced in the previous subsection. A capacitor is placed in between the stages as the dc link. This capacitor decouples the dc and ac sides if it is large enough. Fig. 1-6 shows the generic decoupled non-isolated power conditioner, and Fig. 1-7 shows a realization using two-quadrant cascaded boost-buck converter topology. Examples of non-isolated boost-buck topologies are proposed in [25, 31, 32, 38-51].

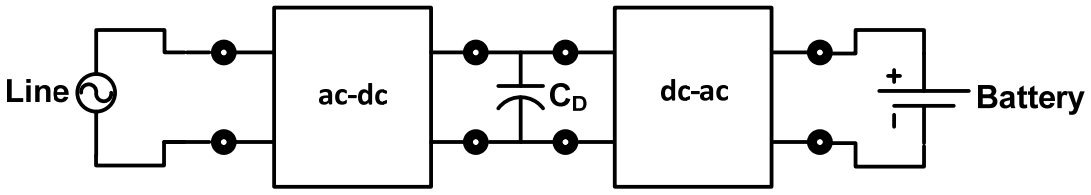

Fig. 1-6- Two-stage dc link decoupled non-isolated VPC

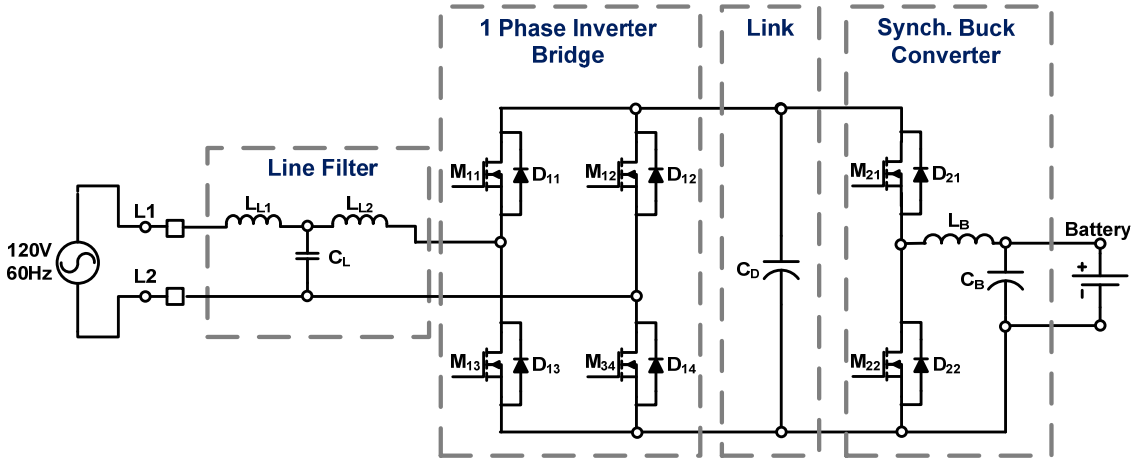

Fig. 1-7- Two-stage single phase non isolated VPC, realized with MOSFET switches

1.5.3. Isolated Topologies

Today both isolated and non-isolated vehicular chargers are available in the market [8, 11]. The isolation regulations are not quite clear as the related standards are still under development. The second chapter of this dissertation thoroughly investigates this matter in the vehicular power conditioners.

The isolation transformer provides galvanic isolation in power converters. The transformer's volume is proportional to the inverse square of the switching frequency; hence, a higher switching frequency results in a smaller and lighter isolation transformer. The onboard VPC is located on the vehicle and the size matters for this application. Therefore, the isolation transformer has to operate at a higher frequency compare to the line frequency. The battery has limited energy capacity and the power conversion efficiency matters for the vehicular applications. It is preferred to condition the magnetic

circuit in a way there is not dc offset. This design constraint fully utilizes the B-H curve of the magnetic cores.

Implementing the high frequency galvanic isolation will introduce a new power conversion stage to modulate the battery's voltage with a high frequency career as shown in the Fig. 1-8. The second stage will be an ac-ac converter. The isolation transformer is the high frequency ac link. Introducing it to the power conversion path will replace the basic converter that used to condition the battery with a differential converter. The ac link may be conditioned by a few different approaches that will be described in the next subsection.

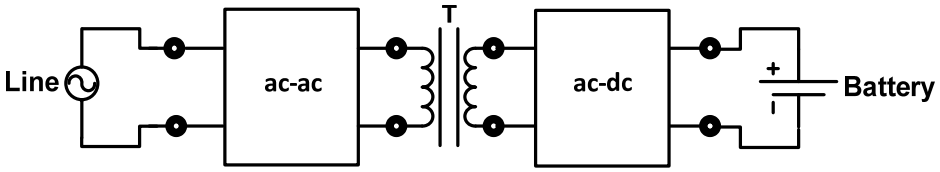

Fig. 1-8- High frequency isolated two-quadrant VPC

1.5.3.1. Two-Stage Isolated Approach

In this approach, a high frequency two-quadrant dc-ac inverter conditions the isolation transformer. A four-quadrant ac-ac converter conditions the grid [52, 53]. The examples of this approach are practiced in [53-59] for a VPC. A single phase realization of this approach is shown in Fig. 1-9.

In [60] a four-step switching strategy is suggested for four-quadrant two-stage ac-ac converters. This modulation technique is employed for a hybrid four-quadrant and

two-quadrant ac-dc converter in [61]. A drawback of the four-step modulation for the two-stage isolated topology, is that the switching frequency of transformer side bridges has to be lower than the switching frequency of the line side bridge. This is the opposite of what is desired, as the magnetic circuit needs a high frequency modulated power, whereas the line has much lower frequency. In [52], the phase shift modulation is employed for a four-quadrant Dual Active Bridge (DAB) ac-ac converter. The DAB topology will be introduced in detail in the three-stage isolated VPC subsection. A variation of the Fig. 1-9 topology is proposed in [53]. They have used a hybrid modulation method combining the phase shift and the frequency modulation methods. The line side power conditioning stage is the four-quadrant half bridge, and the battery side power conditioning stage is the two-quadrant h-bridge.

Employing a four-quadrant power conversion stage for a VPC brings a few disadvantages. The four-quadrant switches are not popular in the industries and need to be implemented with two-quadrant switches; this adds complexity to the circuit. Similar to non isolated single-stage solution, there is no place to implement a dc link, and it is a directly coupled topology. This is not preferred for single phase applications. It is possible to connect a capacitive bank to the transformer [62]. This adds a winding to the magnetic circuit and a power conditioning stage. Another variation of an isolated power conditioner has been practiced with at least one four-quadrant stage and the dc link in the power conditioner such as [61]. These are sub-optimal solutions since adding the capacitor to the power conversion path adds one power conditioning stage; whereas,

with an additional power conditioning stage the four-quadrant switching network is not mandatory.

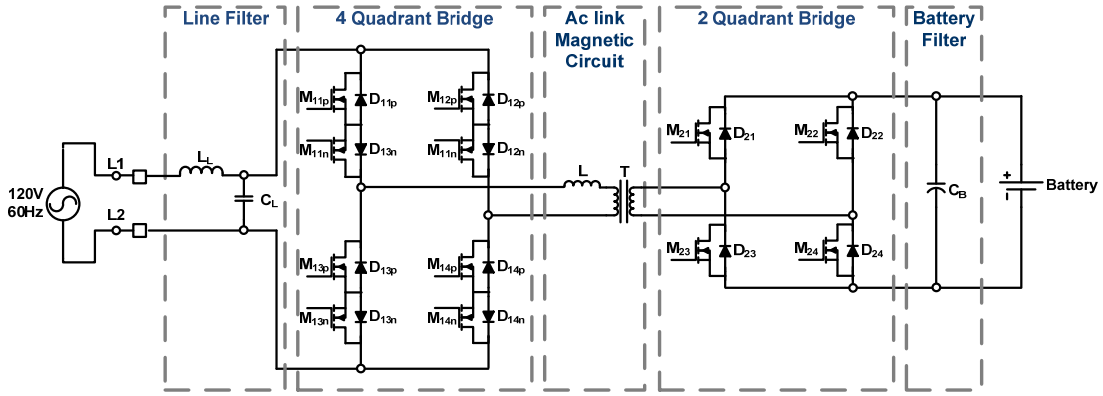

Fig. 1-9- High frequency isolated two-stage VPC, series ac link

1.5.3.2. Two-Stage Four-Quadrant Approach

Unlike the hybrid four-quadrant two quant, two-stage isolated topology, which is described in the previous subsection, a four-quadrant two-stage isolated approach is proposed in [63] for ac-dc photovoltaic application. This topology has not specifically proposed for a VPC, yet. This subsection is a comparison of this power converter family and the previous power converter family as two-stage isolated candidates. A basic definition to contrast the topologies is presented, and the subsection proceeds to a fundamental comparison between the mentioned topologies.

A two-quadrant h-bridge is a dc-ac converter. This topology includes two legs. Each leg has two switches; the upper sides of high side switches are connected to positive dc terminal and the lower sides of the low side switches are connected to the negative dc terminal. The common points of the switches, within each leg, are connected

to one of the ac terminals. With this definition, the dc side of h-bridge is called the dc port of the h-bridge, and the ac terminal of the h-bridge is called the ac port of the h-bridge. If the ac port of the h-bridge is connected to the ac port and the ac port of the h-bridge is connected to the dc port, the switching network can still operate; however, the switches have to be realized with four-quadrant components. Such a solution is suggested in [63] for the photovoltaic application. This topology is called the parallel high frequency ac link in this dissertation. Fig. 1-10 shows a fully bi-directional derivation of the parallel ac link topology for a two-stage four-quadrant VPC. Similar to the previous two-stage isolated approach, this is a coupled solution.

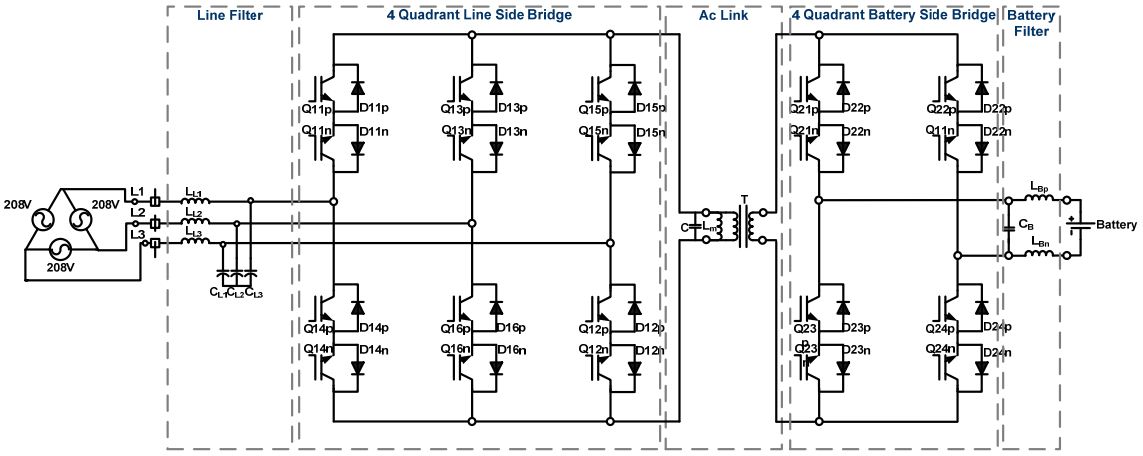

Fig. 1-10- High frequency isolated two-stage VPC, parallel ac link

Comparing parallel to series ac link topology, on the positive side the parallel ac link configuration can easily be expanded to multiphase ac lines by increasing the line side bridge legs. This is not the case for the series ac link configuration. On the negative side, the parallel ac link topology has a few drawbacks for the onboard vehicular

application. The current waveform is triangular, as sketched in Fig. 1-11. As a result of triangular link current, there is just one instance that the maximum power can be transferred through the power converter. This is the fundamental drawback of this solution for any application that demands high power density.

In order to have a metric compaction between the ac link topologies, the ac link Utilization Factor (UF) is defined as (1-2) in this dissertation. The ac link UF is the ratio of the average power to the maximum power transferred through the ac link. The ac link is cascaded with the power path; thus, this definition determines the power utilization of VPC; furthermore, evaluates the VPC's power density. In (1-2), i_{link} is the link current and v_{sec} is the transformer's secondary side voltage, which is the battery side voltage in the mentioned VPCs.

$$UF = \frac{\frac{1}{T_s}\int_{T_s}(i_{link}(t).v_{\sec}(t))dt}{i_{link(\max)}.v_{\sec(\max)}} \tag{1-2}$$

The ac link UF will be calculated for the discussed topologies considering the ac link waveforms. The diagrams of Fig. 1-11 and Fig. 1-12 are the ac link waveforms of parallel and series ac link topologies, respectively. In parallel ac link topology, the link is parallel with the power conversion path. All the transferred power is charged into the link inductor and then discharges to the output port alternatively during each switching cycle. In contrast, the series ac link is in series with the power conversion path. With phase shift modulation square wave form voltages applies to each side of the link, with a phase shift. Only the difference of primary and secondary sides' voltages will store

energy into the link. Thus, the ac link inductance causes less circulating power for the series configuration with the phase shift modulation.

The proposed ac link UF criterion supports the previous statement about the series ac link configuration's excellence. Following (1-2), suggests the most UF for a square waveform, which is 1. The phase shift modulation with low phase shift is the closest to a unity UF. Despite, UF is less than 0.5 for a triangular link current. Since only a half of the switching cycle is dedicated to each side in parallel series ac link converter, the UF is less than 0.25 for this configuration. The UF for the discussed topologies is approximately calculated as follows. The parallel ac link converter's UF is estimated as (1-3). If the resonating cycles are neglected the UF is 0.25 for this topology. Similarly, the series ac link converter' UF is calculated in (1-4). In (1-4), PS is the phase shift between the bridges in radians. The phase shift is always below 180^{o}; hence, the UF is always more than 0.5; even better, avoiding excessive reactive power the phase shift is controlled below 90^{o} that results a UF of more than 0.75 for the series ac link topology.

$$UF_{Par} \approx \frac{\frac{1}{Ts} . V_{Bat} . I_{L\max} . \frac{T_s}{4}}{V_{Bat} . I_{L\max}} = \frac{1}{4} \tag{1-3}$$

$$UF_{Ser} \approx 1 - \frac{PS}{2\pi} \tag{1-4}$$

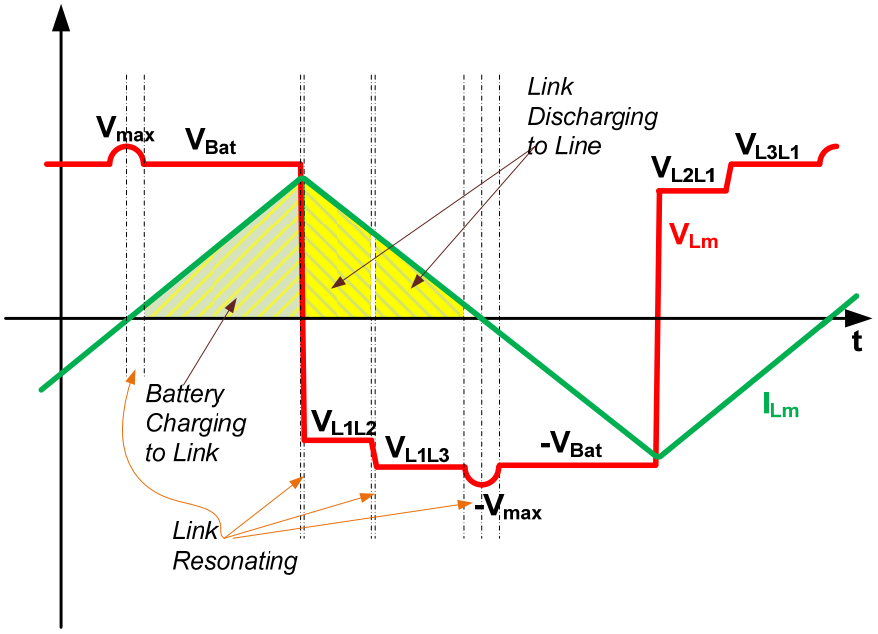

Fig. 1-11- Ac link waveforms of parallel ac link converter

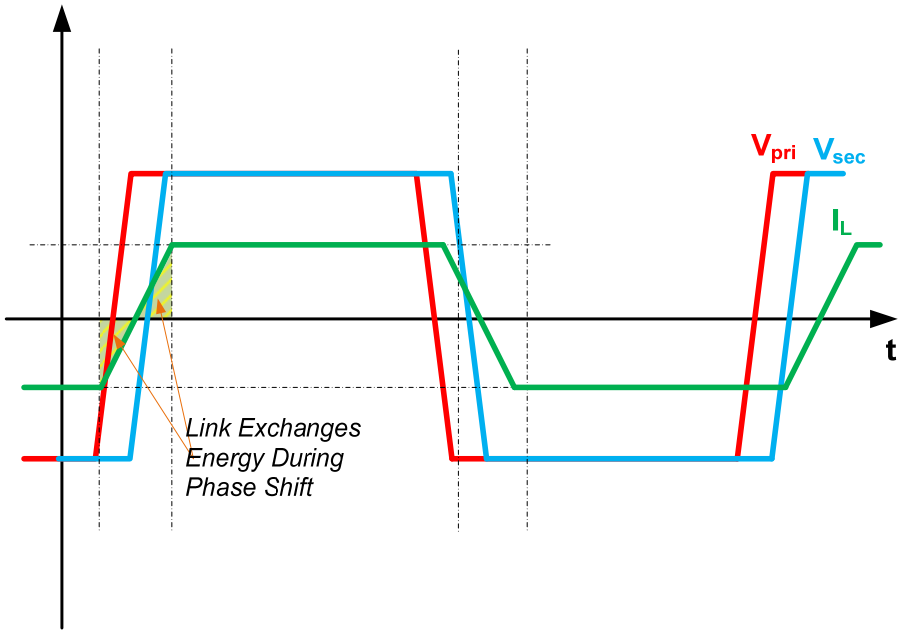

Fig. 1-12- Ac link waveforms of DAB as series ac link converter

When the galvanic isolation is required, the magnetizing inductance will be the ac link. In other words, the energy needs to be stored in the magnetizing inductance, and the magnetizing inductance acts as an ac inductor. The magnetizing inductance easily saturates, hence an air gap needs to be integrated into the core. This reduces the magnetic coupling and increases the leakage flux. The leakage inductance is not utilized in this topology and leads to a low efficiency for the magnetic circuits.

1.5.3.3. Three-Stage Decoupled VPC

The decoupling is desired between the dc and ac sources that are connected to different terminals of the power conditioner. In fact, some regulations need the hold off time requirements. The hold off time is defined as the time delay the equipment has to remain powered after the source is lost or disconnected. This requirement needs an energy buffer within the power converter. The dc link can be employed in the power conditioner for satisfying such requirements. Additionally, the dc link reduces the double frequency ripple for the single phase grids. In this configuration, the dc link capacitor is placed right after the line power conditioning stage. This placement suggests the least possible unnecessary circulating power.

Fig. 1-13 shows the system diagram of an isolated two-quadrant power conditioner. This is a three-stage topology and can be realized by three voltage source dc-ac converters, as shown in Fig. 1-13. This configuration includes three two-quadrant voltage source inverters. The first stage conditions the battery and is called the battery side bridge in this dissertation. The second bridge is between the isolation transformer magnetic circuit and the dc link capacitive bank. This bridge is called the middle bridge.

The third bridge conditions the grid and is called the line side bridge. There is a self similarity between the power conditioner and its sub modules. Three dc-ac cascaded stages operate as a dc-ac power conditioner. This is desired for a practical solution; since, it is easier to educate the industry about this solution. The variations of three-stage isolated topology are suggested by [25, 44, 64-71] for the energy storage and vehicular applications.

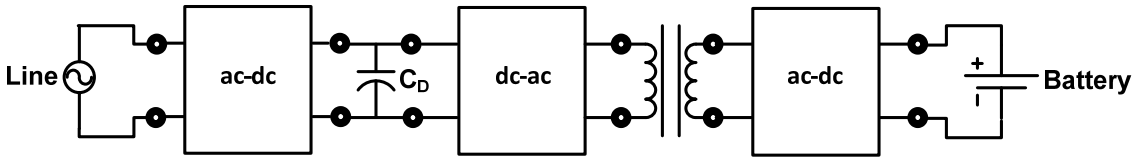

Fig. 1-13- High frequency isolated three-stage decoupled VPC

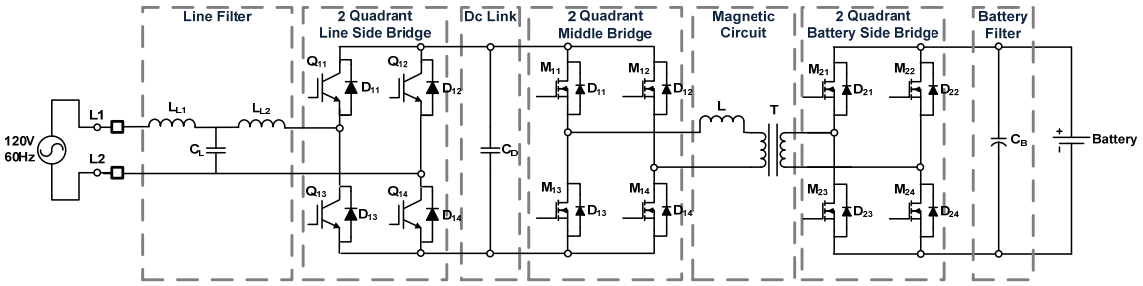

Fig. 1-14- High frequency isolated three-stage VPC realized with three h-bridges

As an example, Fig 1-13 shows a realization of three-stage isolated VPC. The line side bridge is realized with IGBTs and the middle and the battery side bridges are realized with MOSFETs. In the configuration of Fig. 1-13, the line side bridge is an inverter similar to a single-stage non-isolated VPC. The middle bridge and the battery

side bridge operate as a DAB converter. The switching frequency of the DAB is relatively higher than the switching frequency of the line inverter, in order to reduce the size and volume of the magnetic circuit.

The DAB topology was introduced in the early ‘90s [72] and has been attractive to various applications dealing with isolated dc sources [52, 53, 64, 72-102]. This topology offers promising characteristics for a portable dc-dc power converter system such as an onboard automotive power conditioner. The ac inductor L shown in Fig. 1-14 is the key component to transfer power between the bridges. The power flow is controlled by controlling the phase shift between the battery side bridge’s ac voltage and the line side bridge’s ac voltage.

The fundamental difference between the three-stage isolated VPC of Fig. 1-14 and the two-stage isolated VPC of Fig. 1-9, is in presence of the dc link capacitor. Thanks to the engagement of two power conditioning stages; there is more freedom on manipulating the phase shift of the ac-link. In the three-stage isolated configuration, the phase shift modulates the power that passes through the magnetic circuit. The phase shift can be solely designed in favor of the magnetic circuit. In the two-stage isolated approach, the phase shift modulates the power that passes through the isolation transformer; simultaneously, modulates the power injected to the grid. Thus, there are more constraints that can act against the desired design parameters, as described previously in the subsections 1.5.3.1 and 1.5.3.2, which were dedicated to two-stage isolated topologies.

The two-stage isolated ac-dc converter of Fig. 1-10, the two-stage isolated dc-dc converter of Fig. 1-14, and the two-stage ac-ac converter of [52] are all the variations of the DAB converter topology. In all, there is a series ac link in between of two bridges. Each bridge is connected to a source; if the source is dc, the bridge is a two-quadrant converter; if the source is ac, the bridge is a four-quadrant converter. The comparison described between the series and parallel ac link converter topologies, in 1.5.3.1 previous subsection is valid for all the DAB variations.

As mentioned earlier, the link inductance in parallel ac link topology integrates to the magnetizing inductance and negatively reflects the isolation transformer design. In contrast, the ac link inductance adds to the leakage inductance in the ac link topologies. The series ac link inductor may also be either integrated to the transformer's leakage inductance or be placed outside of the transformer. This promises more design flexibility, higher magnetic coupling, less possibility for core saturation, better windows utilization, and better magnetic circuit utilization for the series ac link topologies such as DAB.

Generally, the series ac link configurations excel to the parallel ac link configuration in term of the higher ac link UF. Specifically, the three-stage isolated VPC excels in conditioning the ac link magnetic circuit. The DAB is connected to the dc link and dc link can be conditioned by the line side bridge. The dc link may be conditioned by three different control scenarios. Firstly, the dc link is removed and the line side bridge operates at the line frequency. There will be no switching losses for the line side bridge. On the negative side, the ac link has to modulate the rectified line voltage.

Indeed, this is the two-quadrant variant of coupled isolated series ac link topology of Fig. 1-10. This control scenario is investigated in [103]. Secondly, the dc link is regulated at a fixed dc voltage and the DAB will not modulate any line frequency power. Thirdly, the dc link voltage is controlled to match the battery voltage and the DAB will always operate at an optimal condition. The experimental ac link waveforms of two-quadrant DAB are displayed Fig. 1-15. The dc voltages are equal and the DAB operates at an optimal operating point in this figure. The first and the third scenarios were suggested in this dissertation's proposal as variable control of the dc link in three-stage VPC.

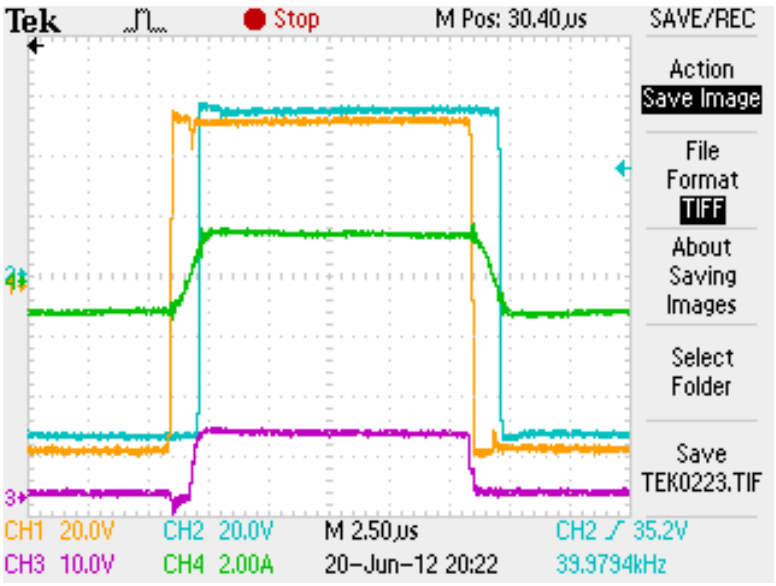

Fig. 1-15- Experimental waveforms of DAB's ac link

Due to the counted benefits, the DAB based isolated three-stage two-quadrant topology is selected for the VPC. This topology will be fully analyzed in the third

chapter. The magnetic circuit design details will be covered in the fourth chapter. This topology is able to perform all the described tasks of a vehicular power conditioner. Moreover, it is expandable from the single phase to the multi-phase grids. The two-port power conditioner can be easily extended to multiport configuration, as will be described in the next section.

1.5.4. Multiport Power Conditioning Topologies

As mentioned earlier, the high voltage battery and the grid are the primary sources to be conditioned on an electric powered vehicle. There are more sources available on an electric vehicle including the low voltage battery. As the technology advances, the new sources will be introduced to the vehicles. Photovoltaic panels, fuel cells, ultra capacitors, and flywheels are among the new sources that would be integrated to a vehicular integrated power system.

The multiport power converter topologies can extend the power conditioner functionality to conditioning additional sources, loads, and energy storage elements. The low voltage battery is the next source that may be added to the vehicular power conditioner. Due to the safety standards, such as FMVSS 305 [13], the low voltage battery has to be isolated from the high voltage battery. Thus, the multiport power conditioner has to be an isolated topology.

In [43], a unidirectional auxiliary power conditioning pass is added to a two-stage non isolated VPC. The auxiliary pass consists of an isolation transformer and a diode rectifier. When the grid is disconnected, the converter can be reconfigured to a dc-dc isolated full bridge converter. The high voltage battery is the input, the line inverter

adds to the transformer and the rectifier to form a full bridge converter. Generally, it is not desired to reconfigure a power electronics converter. Reconfiguration needs to add relays or solid state switches to the circuit. The converter is a switching circuit and it is preferred to design the switching networks and power conditioning stages in a way that control and modulation perform all operating modes. The other drawback is that there is no pass to transfer energy from the low voltage battery to the high voltage battery. In [104], an isolated three-stage charger connects to the high voltage dc bus and segregated a dc-dc converter interconnects the low voltage battery bus to the high voltage dc bus.

In contrast to the previous solutions proposed in [43, 104], the multiport converters that are introduced in this section can condition several sources with no reconfiguration and with the flexibility of the bidirectional power flow. Both the series and parallel ac link topologies can be extended to a multiport configuration. In [105], an example of a multiport parallel ac link converter is presented. In [106-118] the examples of multi active bridge converters are suggested. Fig. 1-16 shows a triple active bridge converter, as an example of a multi active bridge topology. Similarly, Fig. 1-17 shows a system based on the three-port parallel high frequency ac link topology.

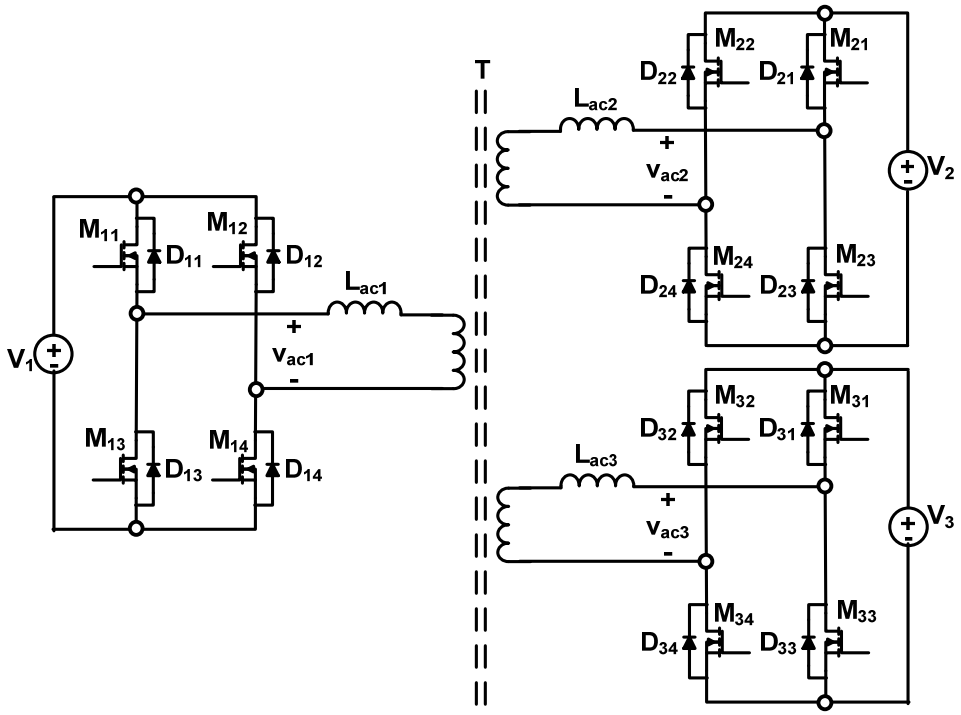

Fig. 1-16- MOSFET realization of dc three-port power conditioner

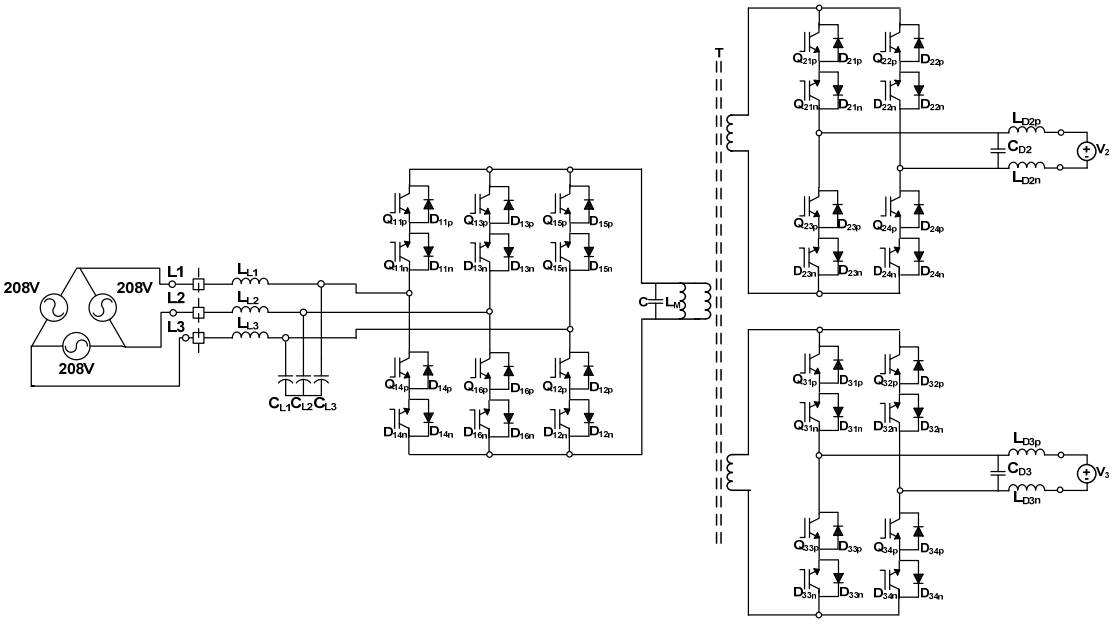

Fig. 1-17- Three-port parallel high frequency ac link converter

The multiport variations of these two topologies inherit the similar characteristics that were discussed in the previous section. Additionally, the multi-active bridge is more flexible for the power flow control between the ports. All the ports may add or remove the magnetic flux to the magnetic circuit simultaneously. Unlike, in the parallel ac link multiport converter the link is charged and discharged sequentially by the ports and it is not possible that several ports charge or discharge the link at the same time. Thus, the UF can potentially approach the unity for the multi active bridge topology and the UF will be less than 0.25 for any of the sources that are attached to the parallel ac link converter. Indeed, the more sources are added the less UF they share from the ac link. This translates to more power density and more flexibility for the series ac link configuration that utilizes the phase shift modulation.

In conclusion, the fundamental comparison between the multiport topologies suggested the multi-active bridge topology as the superior topology to interconnect all sources within a vehicle. This proposes extending the vehicular power conditioning concept to an integrated vehicular power system. In such a system, all the sources, the loads, and the energy storage elements are inter-connected. This idea will be presented later in this section.

1.5.5. Series Parallel Hybrid Multiport Topology

The series and the parallel high frequency ac link topologies were introduced in previous subsections. Both of the topologies are rational for a medium power application only if the isolation is required. The ac link in the series topology is integrated in the leakage and this topology promises a high power density solution. Instead, in the parallel

topology the link is integrated into the magnetizing inductance. This topology is based on the four-quadrant power conversion stages that suffer from low power density however promises low switching losses.

Consider an application with a primary power conversion requirement that needs a high power density solution and an auxiliary power conversion requirement that may be served with a low power density solution. This can be integrated into a unified transformer design. Thus, a series-parallel high frequency ac link topology is proposed, that promises a highly integrated multiport power conversion solution. This idea not previously investigated and is suggested for the future work. An example of possible power converter circuit is shown in Fig. 1-18.

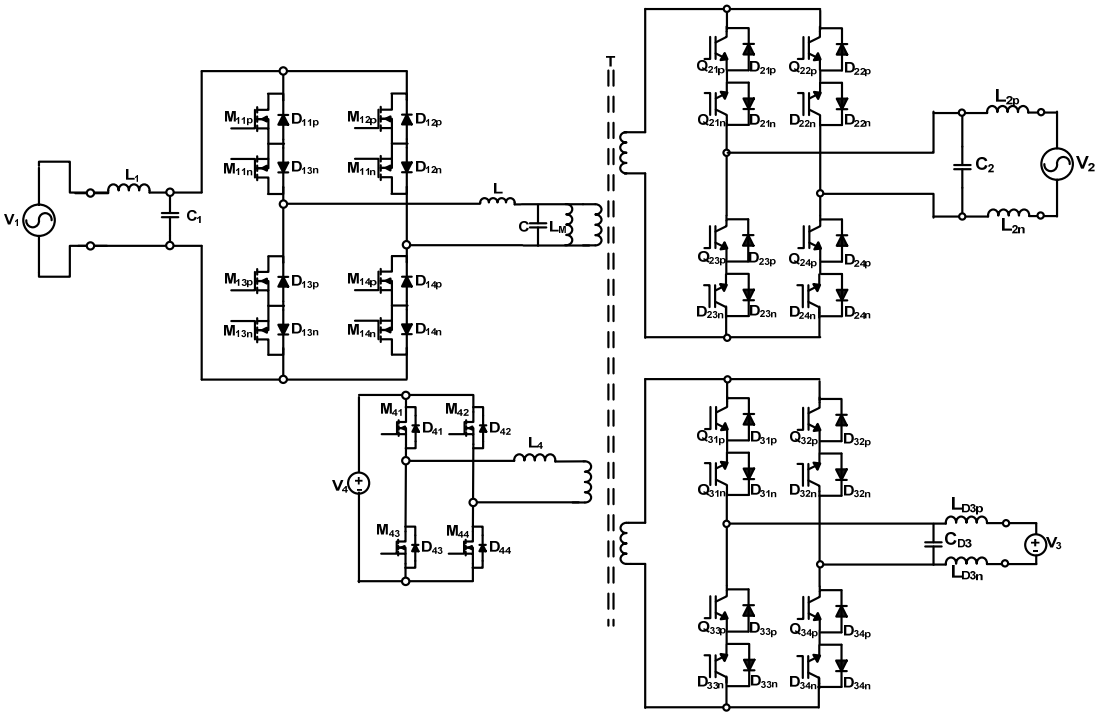

Fig. 1-18- Four-port hybrid series-parallel high frequency ac link converter

1.5.6. Vehicular Integrated Power System

During this section, the vehicular power conditioning concept is evolved from a unidirectional charger to a multi-function multiport power converter system. In each step, adding features and functionalities to the VPC employed additional power conditioning stages. The multiport power conditioner topologies enable the power flow between multiple sources and loads within the vehicular system as well as the outside networks. The power conditioning of electric powered vehicles can be further extended to an integrated power system. This subsection proposes a modular structure to integrate all the sources and loads within an electric powered vehicle into a fully connected integrated power system.

The vehicular power system has all the components of a power system. It includes sources, energy storage elements, power storage elements, loads, interconnections, communicational modules, control units, and protections. All these components are gathered on a vehicle that moves and is isolated from the earth. The vehicle can exchange energy with the external power systems with flexible protocols. The conductive ac and dc and inductive charging methods that classified in the standard review section (section 1.4) are examples of the vehicular integrated power system interaction with the terrestrial power system.

The electric components of the vehicular system are classified to ac and dc components. They may have different voltage levels. Unlike the terrestrial power system, the voltages can widely vary. As of today, the major dc sources are the batteries. The battery voltage may vary around 60% depending on the state of the charge. The low

voltage battery supplies the cabin services. The demand for the low voltage battery is constantly increasing; in mid size luxury cars, the low voltage power generating is close to 4 kW [2]. This is comparable to a class-two charger's power rating. The traction motor rating is more than ten times larger than the services; however the interconnection to the other sources does not need to follow the similar power capacity. The power transfer capacity through the series ac link can be customized for every power conditioning stage. Moreover, the power flow between the windings can be fully controlled with the phase shift modulation in between of each power sending stage and power receiving stage.

An example of a notional vehicular integrated power system is illustrated in Fig. 1-19. The core of this vehicular integrated power system is the series ac link multi port dc-dc converter. Each power conditioning stage is a high frequency dc-ac converter that conditions the magnetic circuit. The magnetic circuit includes the windings and the series inductances adding up to the leakage inductance. The windings may be wounded around the core in series [71] or mesh [102, 117, 119] configurations. Alternatively, the coaxial winding configuration may be employed [120, 121]. The dc source may be battery packs, capacitive banks, or renewable sources as photovoltaic panels. The mentioned dc sources may be regulated at a fixed voltage or have a varying voltage level. Each dc voltage level can serve multiple dc sources in parallel [122-127], or ac sources through dc-ac power conditioning stages. The grid and the propulsion system are the examples of ac sources and loads in Fig. 1-19. The grid is a bidirectional source with

the stiff voltage and the fixed frequency, whereas the propulsion system is a bidirectional variable ac load, which can return energy during regenerative breaking.

As described, the extensive VPC can integrate all the electric components of the vehicle into the vehicular integrated power system. This integrated power system is a hybrid dc and ac system. All the power conditioning system may be implemented on a cold plate.

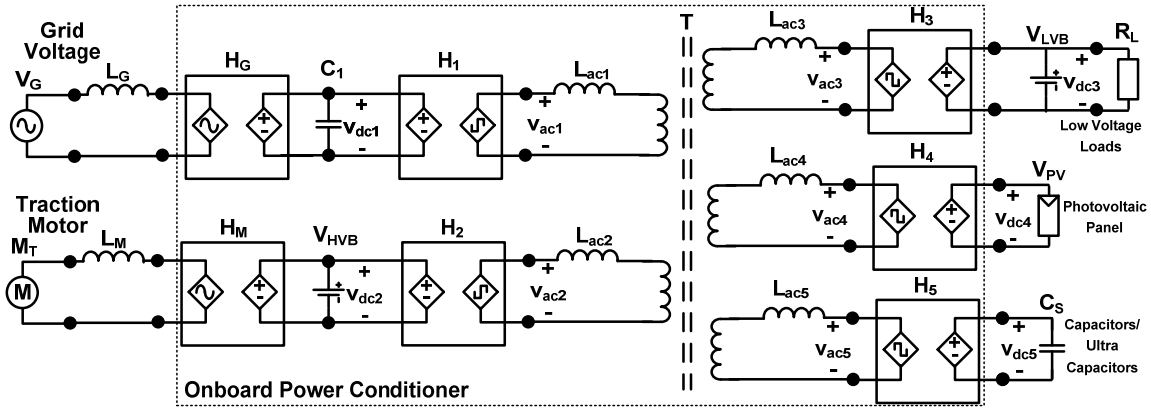

Fig. 1-19- Evolution of VPC to a vehicular integrated power system

1.6. Dissertation Outline

The next chapters will explain the contributions that have been made during this research. The second chapter will investigate the grounding schemes of the VPCs. The galvanic isolation's role in the VPC design and the safety concerns will be evaluated through the developed simulation test bed.

The third chapter is dedicated to the VPC design. A notional VPC will be introduced. This notional system will be the reference for verifying the proposed

concepts through the dissertation. The experimental setup design will be summarized in the third chapter. The design approach for the DAB converter used in the VPC will be proposed in the third chapter. Additionally, the commutation of the Snubberless DAB converter will be analyzed in the same chapter. Both, the design procedure and the analysis of Snubberless DAB will be among the dissertation's contributions.

The contributions regarding the VPC's magnetic circuit will be presented in the fourth chapter. The magnetic circuit includes including the ac inductors and the multiwinding transformer. A novel integrated series ac inductor with common mode interference rejection capability will be suggested in this chapter. Moreover, a novel experimental modeling method for multiwinding transformers will be explained. This novel modeling method enables modeling the capacitive elements of each winding.

The fifth chapter will focus on the control scheme. The developed simulation test-bed will be introduced in the fifth chapter. The closed loop control schemes for charging, V2G, and V2H functionalities will be employed in this chapter. Various case studies will verify the proposed control routines in steady state operating points and transient scenarios.

The developed experimental setup will be overviewed in the sixth chapter. The experimental results have been used through the dissertation. In the sixth chapter, a summary of the various case studies performed with the experimental setup will be reported.

Finally, the dissertation's contributions will be highlighted and the future works to continue this research will be envisioned in the conclusion chapter.

1.7. Conclusion

The fundamental concepts that have been subject of this dissertation were defined in the introduction chapter. The necessity of the VPC was described according to the national and international policies that had emphasized on the need for power conditioning of EVs and PHEVs. The outline of the research was introduced and the dissertation's focus was emphasized. This dissertation has been dedicated to the power conditioning of the EVs and the PHEVs. The main focus of the research would be innovative power conditioning solutions for the vehicular application.

The relevant VPC standards were reviewed. It was described the present standards have been mainly focused on the chargers. The design guidelines for the notional VPC were sketched in respect to the automotive standards, distributed generation standards, reports and the road map of EVs and PHEVs.

A modular design approach was suggested synthesizing various VPC power converter topologies upon the functional description of the VPC. The functional evolution of VPCs started from the bidirectional single-stage ac-dc power converter. It was described; introducing the passive elements between the switching networks introduces additional features to the VPC. Addition of the dc link capacitor, ac link filters, and the isolation transformer increase the power conditioning stages of the VPC. The examples of synthesized topologies in the earlier works were surveyed. In contrast, the novel topologies that have not been investigated were highlighted.

The ac link converters were categorized to the series and parallel classifications; furthermore, the ac link UF was defined to compare these topologies. The ac link UF is

the ratio of the average power to the maximum power transferred through the ac link, and estimates the power density of a VPC. The two-port VPC can be extended to the isolated multiport VPC by extending the power conditioning stages through the ac link. The possibility of the accommodating extra sources and loads through the multiport VPC suggested extending the power condoner to the vehicular integrated power system that connects all the electric components potentially available in a futuristic vehicle.

2. HIGH IMPEDANCE GROUNDING FOR ONBOARD PLUGIN HYBRID ELECTRIC VEHICLE POWER CONDITIONERS*

2.1. Background

The PHEVs and their current status were introduced in the introduction chapter. This chapter investigates different grounding schemes that may be practiced when the onboard VPC is connected to the grid. Much like the present status of PHEVs, the related standards are either in the early stages of practice or under development. Reviewing the related standards can define certain guidelines and regulations affecting the design and development of power converters used in the vehicular applications. This influences the topology, cost and efficiency of VPCs.

This chapter will investigate the available VPC standards in respect of the grounding requirements when connected to the grid to perform charging, V2H and V2G functionalities. The role of galvanic isolation will be evaluated by analyzing the two-stage non isolated charger and the three-stage isolated charger. The idea of high impedance grounding of the onboard VPC to the grid will be suggested, which is among the dissertation's contributions.

A few case studies will compare fault conditions in all four possible configurations, including the isolated and non-isolated topologies for both direct and high impedance grounding. The grounding schemes are usually associated with the

safety concerns. A human body model will be employed to evaluate the human to the line fault scenarios. These case studies will evaluate the outcome of the isolation and grounding schemes into the human safety.

2.2. VPC's Grounding Requirements

According to the envisioned VPC roadmap, the short term goal of this application is to provide a means of charging the vehicle. At the time of writing this dissertation, the released standards are about chargers. Chargers may be stationary or onboard. The onboard chargers are within this dissertation's scope. The SAEJ1772 standard is about the requirements of conductive charging of EVs and PHEVs in North America [18]. FMVSS 305 [13] is another related standard. The IEEE 1547 standard [7] addresses interconnecting distributed resources with the electric grid. The V2G operation of the VPC is the subject of this standard. Both IEEE 1547 and SAEJ1772 refer to the National Electric Code (NEC) [15] for grounding requirements in the United States. The grounding requirements of the VPC will be investigated in this section.

Two nodes of an electric circuit are isolated when there is no electrical connection between them; such nodes can be separately grounded. The high voltage battery in a PHEV should be isolated from the vehicle chassis. In the connection scheme illustrated in [18], the ac ground is connected to the vehicle electric ground, which is the vehicle chassis. If the charger is a non-isolated converter, the battery terminals are connected through the charger circuit ac line terminals to the grid during normal converter operation. If there is a connection between neutral and ground, the battery terminal is electrically connected to the vehicle ground; this violates FMVSS 305 [13].

Because 240 V lines are never connected to ground, the battery remains isolated from the vehicle chassis. In contrast, during 120 V operation an ac neutral line is connected to the charger input terminal. This neutral line is often grounded (bonded) at the ac circuit breaker panel thus completing an electrical conduction path from battery terminal to the chassis ground. If the charger is isolated, the battery terminals are isolated from the ac terminals and are therefore always isolated from the vehicle ground. When the charger is not an isolated converter**,** a high impedance ground may be used as described in this chapter.

SAE J1772 refers to NEC-article 625 for the onboard ac charging system configuration [15]. Article 625 refers to Article 250 for ground pole requirements. In a vehicular electric system, it is not possible to provide an effective ground fault path to the earth. The vehicle is a mobile system on wheels isolated from the earth. The electric system is grounded to the vehicle chassis which complies with NEC-Article 250.4.B. It limits the chassis voltage to ground voltage potential. At the point of common coupling, an isolated ungrounded dc system is allowed to be grounded to the ac ground through the ac neutral conductive ground path or a high impedance ground.

A high impedance ground limits the ground fault current. A high impedance grounded system needs to be serviced by qualified persons; must have ground-fault detectors installed on the system; moreover, should not serve line to neutral loads. According to [15], the low voltage electric system of the vehicles with voltages less than 50 V does not need grounding. Due to the fact that the high voltage side of the vehicle's electric system should not be connected to the ac ground through a low

impedance path, implementing a high impedance ground before the equipment ground pole achieves reference grounding as required by NEC-250.4.B. Hence, a high impedance ground can isolate the vehicle electric system from the ac system that satisfies all present standards. Fig. 2-1 shows the addition of Z_{GND} to the configuration illustrated by [18] in order to implement high impedance grounding.

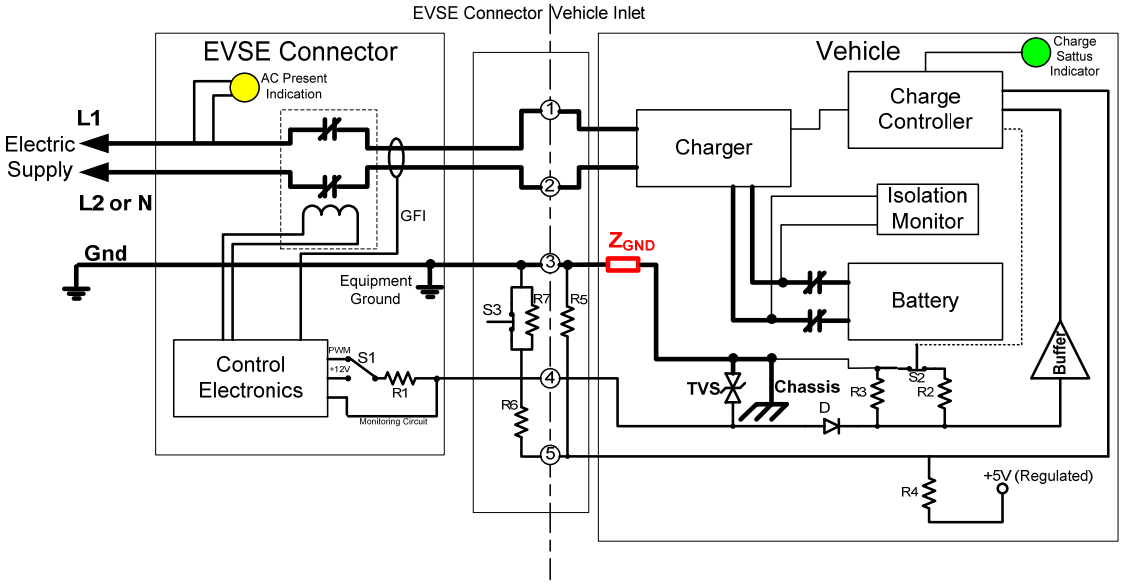

Fig. 2-1- Redrawing SAEJ1772 system configuration with high impedance grounding through Z_{GND}

2.3. Case Studies

This section investigates isolated and non-isolated PHEV chargers both during normal operation and when the ground is connected to the neutral. Both conductive and high impedance grounding are investigated. First, the investigated topologies are introduced; then, the simulation test bed is briefly explained. The case studies are reported afterwards.

2.3.1. Investigated Topologies

A VPC employed in PHEV is a two-port power converter. It has an ac port at the line side and a dc port at the high voltage battery side. In V2G and V2H applications, bidirectional power flow is required; whereas, a charger needs only a unidirectional power flow from the line to the battery. This power converter is placed where the charger block is located in Fig. 2-1. Fig. 2-2 shows a realization of a non-isolated charger using voltage source converters. This topology includes a boost rectifier with unity power factor control and a regulated dc link from the ac power. If the minimum battery voltage is less than the peak amplitude of the ac line voltage, a buck dc-dc converter is required to charge the battery from the dc link. Replacing the dc-dc converter with an isolated converter, results in an isolated VPC, as shown in Fig. 2-3. Compared to the non-isolated converter, the isolated topology adds complexity, cost, and may decrease the conversion efficiency.

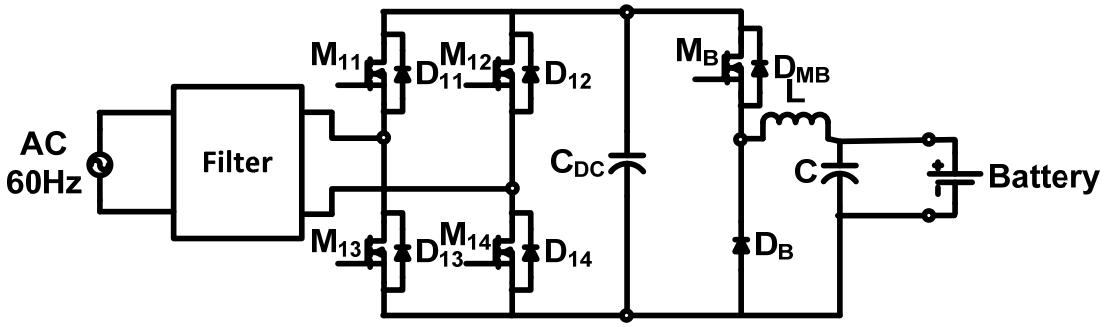

Fig. 2-2- Non-isolated charger topology

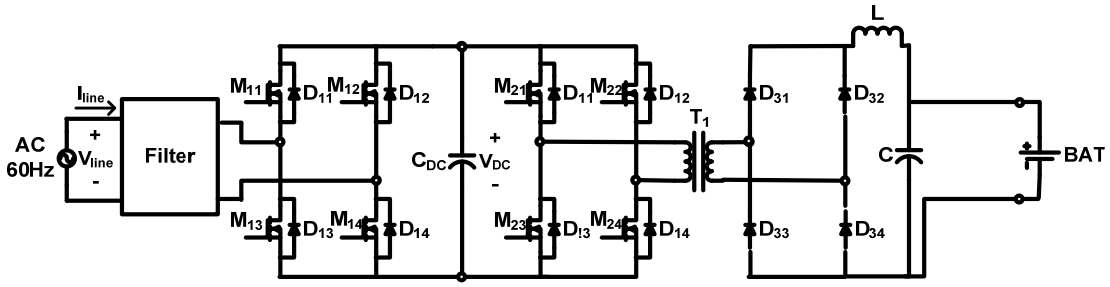

Fig. 2-3- Isolated charger topology

2.3.2. Simulation Test Bed

Fig. 2-4 shows the block diagram of the simulation test bed implemented in MATLAB SIMULINK. The charger block contains the converters presented in Fig. 2-2 and Fig. 2-3. The rectifier stage is identical in both converters and it has a closed loop controller to deliver unity power factor. The non-isolated charger uses a current controlled buck converter and the isolated charger uses a dual active bridge as the dc-dc stage. The battery is modeled as a 350 V_{dc} source and an internal resistance. The simulation test bed includes a human body model as shown in Fig. 2-5 [14]. This model is used to investigate what happens when a person touches the line.

The switches marked as 1 to 4 are used to configure different case studies. Arranging these switches as shown in Fig. 2-4 makes a vector representing each simulation case study. If the switch value is 1 it means the switch is connected. Each case study will be described verbally in the text and the readers may refer to Fig. 2-4 according to the case study vector to determine how the simulation test bed is configured.

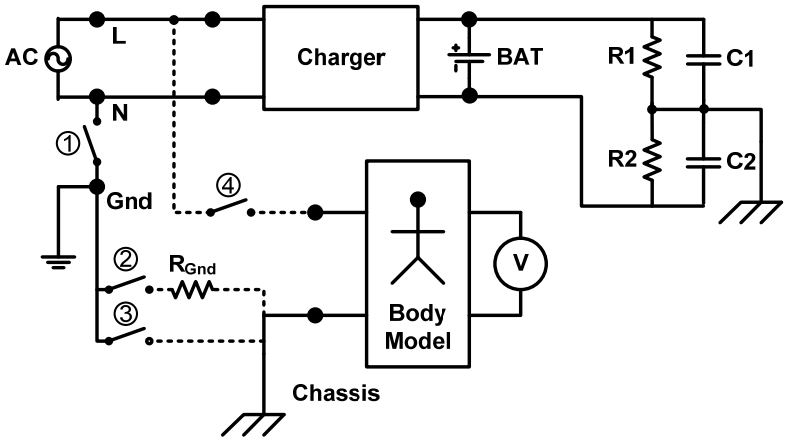

Fig. 2-4- Simulation test bed

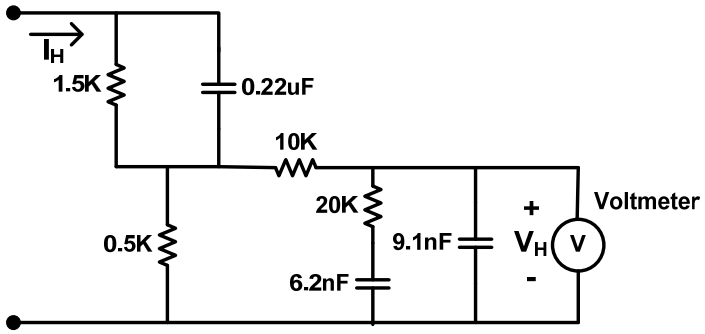

Fig. 2-5- Human body model [14]

2.3.3. Normal Operation

2.3.3.1. Case Study (0010): Neutral Not Grounded

In the first case study, both chargers operate at 6 kW 240 V line. The line and neutral terminals are connected to the charger; the chassis is grounded while the neutral is not bonded to the ground (0010). Both chargers operate properly as the rectifier stage waveforms are presented in Fig. 2-6.

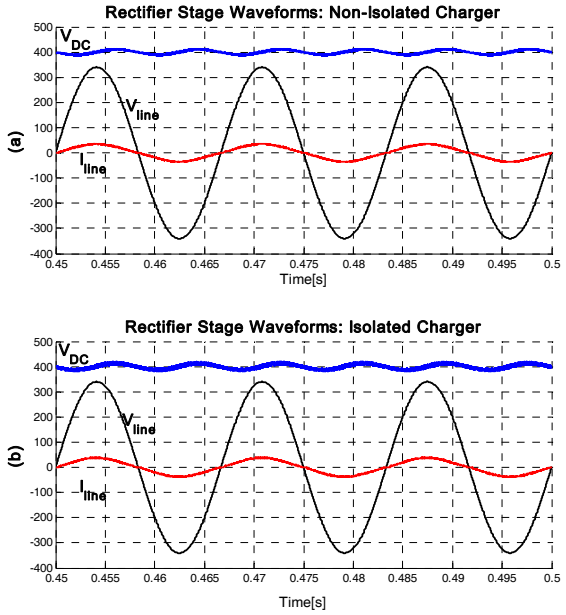

Fig. 2-6- Rectifier waveforms, a: non-isolated charger, b: isolated charger operating at 6kW, simulation case study (0010)

2.3.3.2. Grounded Neutral: Conductive Ground (1010) versus High Impedance Ground (1100)

In the second case study, the neutral is bonded to ground and ground is connected to the chassis, case study (1010). This may be due to a fault or a practice in wiring the single-phase 120 V panel. The non-isolated charger cannot operate in this condition while the isolated charger works fine as shown in Fig. 2-7. The charger protection mechanism will shut down in this case for the non-isolated charger. In contrast, when the neutral is connected to the chassis through a 5 MΩ high impedance ground both chargers operate well as shown in Fig. 2-8, case study (1100).

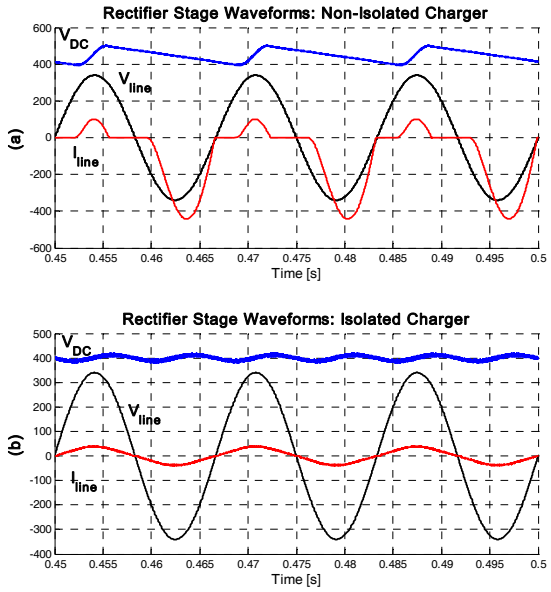

Fig. 2-7- Case study (1010): The non-isolated charger will not work if the neutral is connected to the chassis through the conductive ground connection.

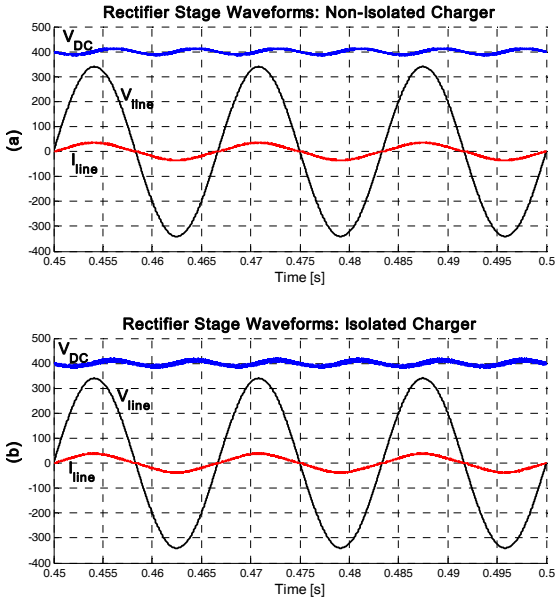

Fig. 2-8- Case study (1100): Both chargers work if high impedance ground connection is employed.

2.3.4. Human to Ground Fault

Human safety is an important concern for the onboard VPC. It is common to relate the isolation requirements to the safety issues. The following case studies analyze how these facts are related. The next case studies investigate the outcome of a human touching the line while he/she is connected to the chassis ground. As a residential line is more accessible, compared to a PHEV battery which is sealed, there is a higher chance of occurrence for this fault, as compared to a fault on the battery side. The SAEJ1772 connection plug prevents such an event when the person does not work with any other ac equipment, and the ground fault indicator shuts down the charger before neutral current exceeds a safe limit of 5 mA.

According to simulations, whenever someone touches the line in the case of non-isolated charger, he/she can get shocked. While for the isolated charger, if there is no connection between the neutral and the ground or the chassis has a high impedance ground connection, the person is not shocked, even though there is no ground fault indicator installed. The details are provided in the following case studies.

2.3.4.1. Case Study (1011): Human to Line Fault, Grounded Chassis

The neutral is bonded to the ground and the chassis is directly grounded. Referring to the case study A, only the isolated charger is able to operate in this configuration. If someone touches the line, as can be seen in Fig. 2-9, a high current would shock the person. The high frequency isolation of the onboard charger is placed in middle of the VPC and does not help in this case. The current I_H and the voltage V_H can be seen in Fig. 2-9. Fig. 2-5 shows where these meters are located.

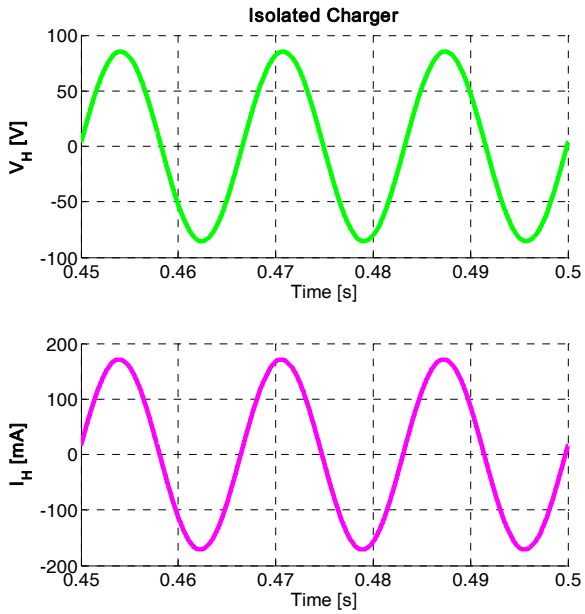

Fig. 2-9 Simulation case study 1011 waveforms, isolated charger, green:V_H [v], magenta: I_H [mA]

2.3.4.2. Case Study (1101): Human to Line Fault, High Impedance Grounded Chassis

The same fault is simulated when the chassis is connected to the neutral through a 5 MΩ resistor (1101). If the charger is non-isolated the current shocks the person as shown in Fig. 2-10, left. In contrast, the current is controlled below 0.1 mA and would not shock the person if the charger is isolated, Fig. 2-10, right.

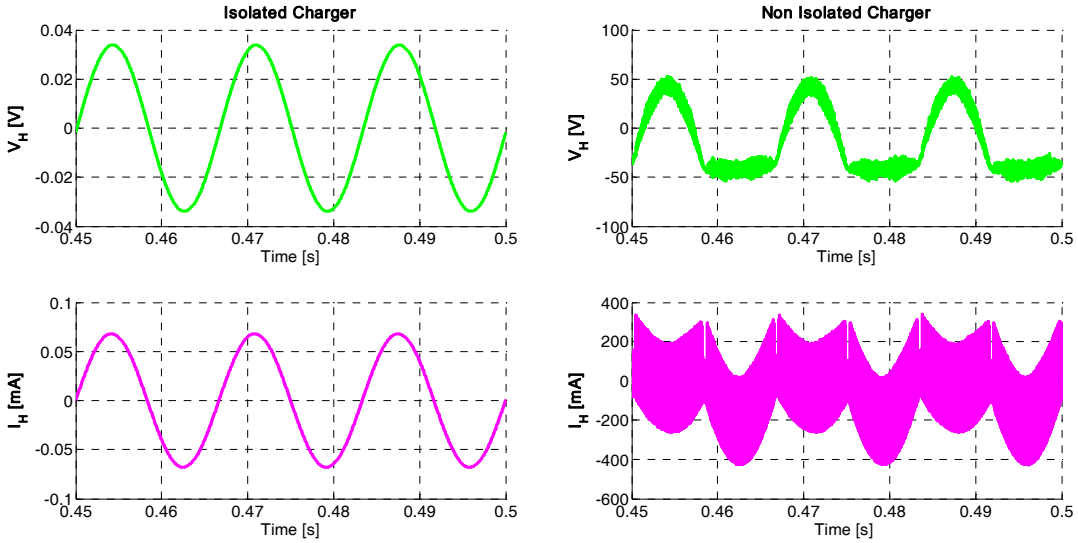

Fig. 2-10- Case study 1101 waveforms, left: non-isolated charger, right: isolated charger, green:V_H [v], magenta: I_H [mA]

2.4. Conclusion

The brief introduction to the status of PHEVs and the VPC roadmap described the importance of this product. Reviewing the related standards provided guidelines for the design procedure of the VPC. Grounding schemes and isolation requirements of VPCs were also investigated.

The main contribution of this study evaluated the novel idea of implementing a high impedance reference grounding connection at the point of common coupling between the vehicle chassis and the electric network ground, which has not been foreseen in the latest edition of the SAEJ1772 standard. This approach lets a non-isolated converter operate with both 240 V and 120 V plugs whether or not neutral is bonded to ground. The provided case studies offered a tool to compromise between

protection facilities and selected power converter topologies to achieve a cost effective VPC for different applications. This is important to increase market penetration of PHEV and their functionalities. The suggested grounding scheme needs to be further evaluated by different standards before utilization.

3. POWER CONVERTER DESIGN

3.1. Background

A variety of power converter topologies were introduced in the introduction chapter. The most preferred topology was the high frequency isolated three phase VPC that can be extended to the multiport configuration through the series ac link. A notional onboard VPC needs to be designed as the reference system to conduct the research. Furthermore, the notional VPC design needs to be implemented in a simulation test bed as well as an experimental setup for validation and demonstration purposes. The notional VPC will be introduced in this chapter. The developed experimental setup will be presented in this chapter, and the developed simulation test bed will be presented in chapter 5 that is dedicated to control schemes.

This chapter will propose a building block based power converter design procedure for developing the experimental setup. An h-bridge converter is selected as the building block for different VPC configurations. The high frequency isolated three-stage VPC and the multiport extension of this topology all can be implemented with h-bridges. The DAB and the triple active bridge converters are formed by the developed h-bridges. The operation of the Snubberless DAB converter is analyzed through a novel physics based piecewise linear approach.

The second section of this chapter introduces the notional VPC. The system ratings and the sources used in the experimental setup will be explained in this section. The third section is dedicated to the building block based power converter design

approach. The design considerations will be included in this section to enhance reproduction of the ideas investigated through the dissertation. The third section investigates the DAB converter. The fundamentals of the operation from the earlier works will be presented and the contributions made in design and analyzing this topology will be reported. The final section is the conclusion of this chapter.

3.2. VPC's Design Specifications

A level one three-port VPC is considered as the design reference for the simulation test bed and the experimental setup. The level one onboard VPC is predicted to have the highest prevalence as described in the first chapter. Additionally, this power level is more compatible with the laboratory facilities and the university regulations.

The schematic of the notional VPC is shown in Fig. 3-1. The power topology is the isolated three-stage VPC that is extended to the third port through the series high frequency ac link. The control and modulation are implemented in a Ti C2000 F2812 DSP controller board. The h-bridges and the controller board have onboard power supplies that are supplied from the laboratory power supplies. The control and power supplies are grounded. The power converter grounding schemes may be practiced as described in the second chapter. Both the high voltage and low voltage batteries are selected under 50 V due to the safety concerns described in the second chapter.

The nominal voltage levels are listed in Table 3-1. The nominal line voltage in the USA is 120 V 60 Hz. Plus and minus 5% deviation is allowed from the nominal voltage. Hence, the line voltage can vary between 114 V and 126 V [15, 19]. The standard low voltage battery on the vehicle is the 12 V battery. There are different high

voltage levels on different vehicles from 100V to 600V [2]. The low voltage high current battery systems with a voltage level below 60V are also proposed for supplying the propulsion drive [128]. The experimental setup batteries are 12 V and 48 V to avoid shocking hazard in the laboratory environment.

The onboard VPC of Fig. 3-1 is implemented in a simulation test bed that will be introduced in the control chapter. The control routines include all the VPC's functionalities including energy exchange with the grid. Due to the laboratory restrictions, the energy exchange with the campus grid is avoided. Hence, the experimental setup only includes the dc section of the VPC. The experiments are valid due to the decoupling of the dc link in this topology. The dc link is replaced with the high voltage laboratory dc supplies, and batteries are set up as will be described in the next section.

Table 3-1 Reference VPC Ratings

	Line (60Hz)	**Dc Link**	**Battery 1**	**Battery 2**
Nominal Voltage	120 V	200 V	48 V	12 V
Minimum Voltage	114 V	161.2 V	38.4 V	9.6 V
Maximum Voltage	126 V	178.2 V	59.6 V	14.9 V
Current	15 A	15 A	35 A	35 A
Power	1650 W	1650 W	1650 W	412.5 W

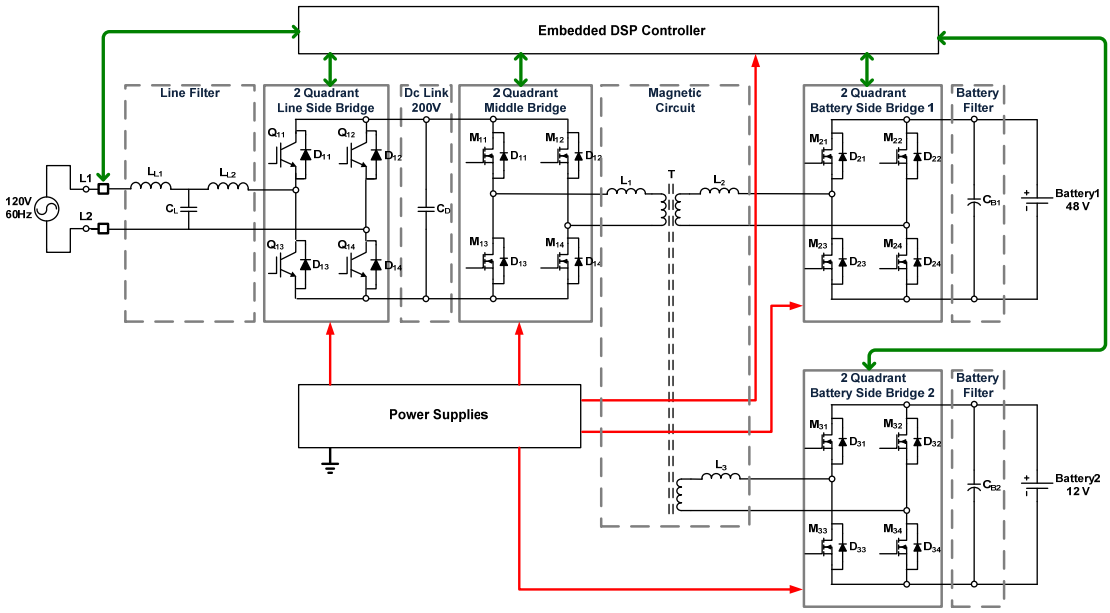

Fig. 3-1- Onboard reference VPC

3.3. Batteries

The experimental setup batteries include five UB12350 (12 V, 35 Ah) sealed lead acid batteries. These batteries are widely available for lawn mowers. A 12 V battery is used as the low voltage battery, and four 12 V batteries are connected in series to form a 48 V battery as shown in Fig. 3-2. The battery setup is equipped with four 100 A automotive fuses (LittleFuze#157.5701.6101) placed at each terminal. These fuses are well above the nominal current protecting the catastrophic faults such as the short circuit fault. This will prevent blowing up the batteries as well as the potential electric and chemical hazards during unforeseen faults. A three phase contactor is utilized as a dc switch for the setup. The converters are also equipped with lower current fuses at their dc terminals.

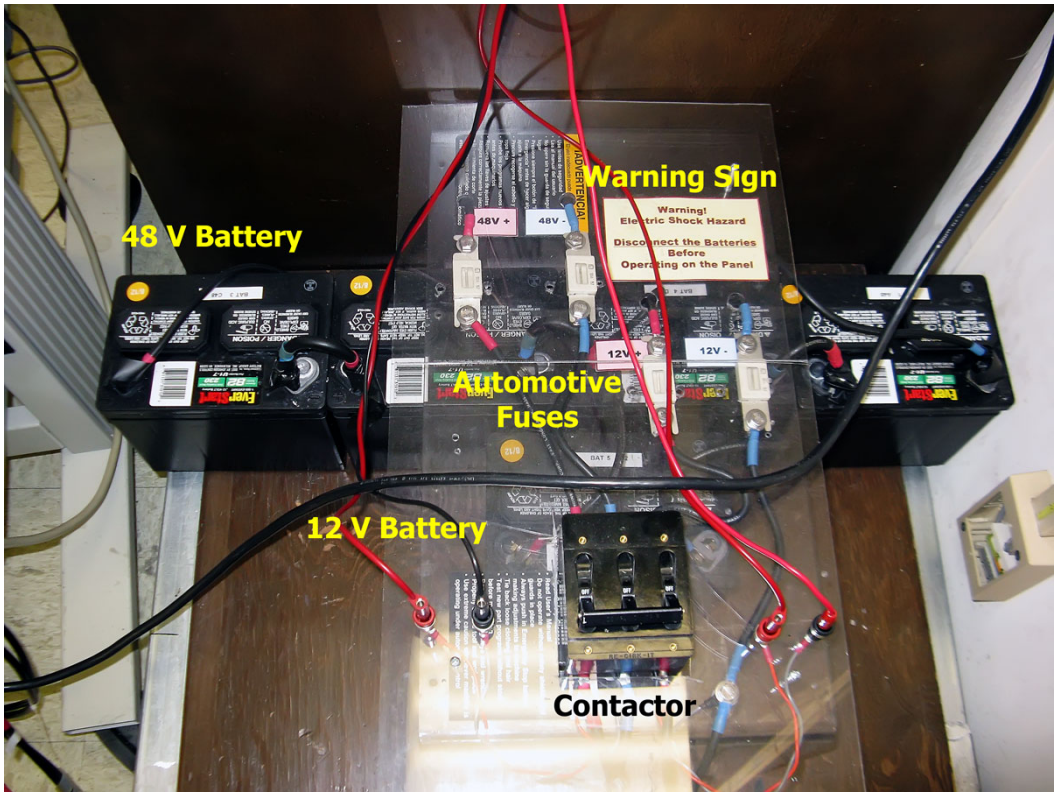

Fig. 3-2- Experimental setup's batteries installation

3.4. Power Converter Stages

The onboard VPC was synthesized based on the three-level voltage source converters to serve all the power conditioning needs. The VPC displayed in Fig. 3-1 is realized with the h-bridges and passive components. The VPC is self-similar to its building blocks within this modular design. The VPC inherits its properties from its building blocks. The modularity of the proposed VPC is utilized in developing the experimental setup.

Thanks to the modularity of the design, all the power conditioning stages have the same power converter topology. A robust and well thought h-bridge design is adopted for developing the VPC prototype. The h-bridges share the same onboard power supplies, gate drive circuitry, and communication interface with the controller board. The design can host TO-247 switches. Both power MOSFET and IGBTs are available in the compatible package. This is a discrete design approach that fits the research purposes of the dissertation.

The h-bridges produce three isolated voltages onboard for gate drivers. The gate drivers are selected as HCPL-3120. This gate driver includes an optocoupler for isolating the gate drive signal and an amplifier output stage that can supply 2.5 A gate current. The high Common Mode Rejection (CMR) of 25 kV/μs is necessary for high frequency switching frequencies.

The h-bridge converter design is well practiced in the author's previous works [36, 37, 129]. A summary regarding the vehicular application is included in this section. The power conditioning stages between the grid and the 48 V battery have the same power ratings of P_{nom}. The 14 V bridge's power rating is a quarter of the other bridges (0.25 P_{nom}). The h-bridge converter is shown in Fig. 3-3. This topology is a differential buck converter and has a buck nature. In other words, at each instance the voltage at the ac port is smaller than or equal to the dc port voltage (V_d). Hence, the highest voltage constantly applied to the h-bridge is the dc link voltage. At each instance, in each leg, one switch is conducting and the other switch is blocking; hence, the maximum blocking voltage of each switch (V_{sw}) equals to the dc link voltage. During the transients, the

switches may be exposed to voltage spikes; therefore, switches need to have higher voltage ratings as (3-1). The switches' current (I_{sw}) is selected according to the rated power and the rms voltage as formulated in (3-2).

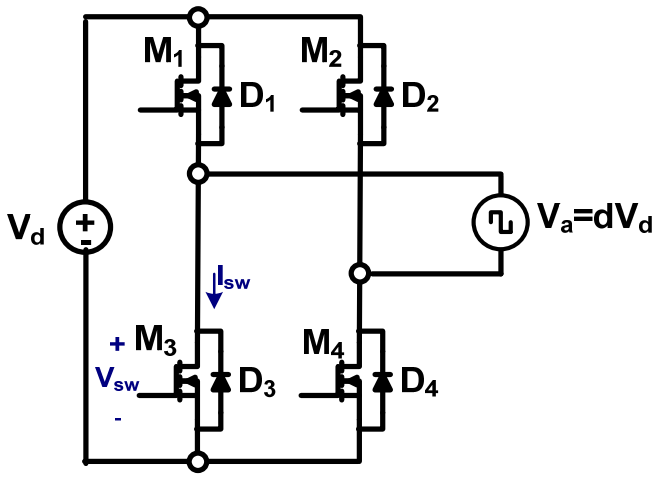

Fig. 3-3- H-bridge converter, V_d: dc port voltage, V_a: ac port voltage, dϵ[-1,+1]: switching function

$$V_{sw} > V_d \tag{3-1}$$

$$I_{sw} \geq \frac{P_{nom}}{\sqrt{D_{\max}} V_d} \tag{3-2}$$

The dc link voltage is the highest voltage in the system; hence, the line side bridge and the middle bridge have to be rated more than the nominal dc link listed in Table 3-1. The dc link voltage needs to be higher than the maximum amplitude of the line voltage. The higher voltage ratings of the dc link capacitors and the switches will result in improved reliability and life cycle. Conservatively, the switches ratings are selected more than twice of the nominal bridge voltages. The battery side bridges are exposed to the battery voltages and the ratings are selected accordingly. The dc side of

VPC is conditioning the high frequency transformer and the switching frequency needs to be relatively high. The MOSFET switches promise more efficient operation at higher switching frequencies. Considering the price, market availability, and design boundaries the switches listed in Table 3-2 are selected for the bridges.

Table 3-2- Switches' Parameters

Port	Switch #	V_{DS} [V]	I_D [A]	$R_{DS(on)}$ [mΩ]	$T_{d(on)}$ [ns]	$T_{d(off)}$ [ns]	V_{SD} [V]	t_{rr} [ns]	$R_{g(int)}$[Ω]	R_g [Ω]
Dc Link	IPW60R070C6	600	53	70	16	83	0.9	720	0.85	10
48 V	IRFP4568	150	171	5.9	27	47	1.3	110	1	5.6
12 V	IRFP4004	40	195	1.7	59	160	1.3	130	6.8	3.0

All the parameters listed in Table 3-2 are related to operation at 25^{o}C junction temperature. The on resistance at actual junction temperature would be twice of the reported value. Similarly, the actual current that the device can deliver continuously is about %50 to %60 of the nominal reported rating. Rg(int) is the internal gate resistance and Rg is the gate resistance placed externally in the h-bridge PCB. The implemented h-bridges are displayed in Fig. 3-4 and Fig. 3-5.

Fig. 3-4- H-bridges front view

Fig. 3-5- H-bridges behind view

3.5. Line Side Bridge

The power converter topology of the line side bridge was described in the previous section. The line side bridge is a hard switching converter. The switching frequency can be selected between 10 kHz to 25 kHz in order to compromise between the output THD and switching losses. Additionally, the audible switching noise is important for the residential applications. The switching frequencies above 16 kHz are not audible.

3.5.1. Line Side Filter

Both L and LCL filters have been proposed as proper configurations for the line side filter [36-38, 129-134]. Design examples will be provided for both configurations in this section.

3.5.1.1. L Configuration

For the single inductor line filter configuration, the design equations are (3-3) to (3-6). The design is inspired from the author's previous works [36, 37, 129]. The desirable THD is designed below 5% according to the standards as was previously mentioned in 1.4.1 and 1.4.3. The inductor L_{ac} is designed as 10.5 mH according to the equations.

$$I'_{L_{ac}(rms)} = \frac{V_{dc}}{2 f_{sw} L_{ac}} \frac{1}{2\sqrt{3}} \sqrt{\frac{1}{2} m_a{}^2 - \frac{8}{3\pi} m_a{}^3 + \frac{3}{8} m_a{}^4} \tag{3-3}$$

$$THD = \frac{I'_{L_{ac}(rms)}}{I_{L_{ac}(1)(rms)}} \times 100 \le THD_{(req)} \tag{3-4}$$

$$m = \frac{V_{o(\max)}}{V_{dc}} \tag{3-5}$$

$$I_{L_{ac}(1)} = \frac{P_{ac(\max)}}{V_{ac(\min)}} \tag{3-6}$$

$$L_{ac} \geq 10.478\ mH \rightarrow L_{ac} = 10.5 mH \tag{3-7}$$

3.5.1.2. LCL Configuration

The LCL design procedure is adopted from [131]. The LCL filter components are name as shown in Fig. 3-6. A per-unit design is provided. The base values are listed below:

$$Z_b = \frac{V_b^{\,2}}{P_b} = \frac{200^2}{1.66 \times 10^3} = 24.0964\,\Omega \tag{3-8}$$

$$C_b = \frac{1}{\omega_b Z_b} = \frac{1}{120\pi \times 24.0964} = 110.082\,\mu F \tag{3-9}$$

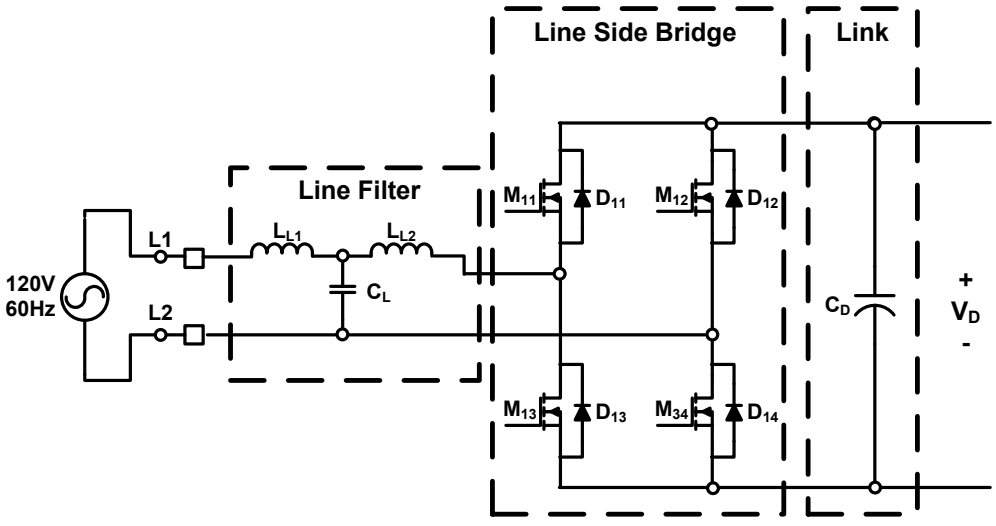

Fig. 3-6- LCL filter for Line Side Bridge

The L_{L2} has to limit the current ripple generated by converter switching. This inductor is designed to limit the highest switching harmonic generated by the SPWM modulation according to (3-10). In (3-10), v(k) is the k^{th} generated voltage harmonic.

$$L_{L2} = \frac{v_{\max}(k)}{k\omega_b i(k)} \tag{3-10}$$

The L_{L1} is designed to limit the worse current harmonic according to the grid standard. In this design, r is assumed as 1.67.

$$L_{L1} = rL_{L2} \tag{3-11}$$

Finally, the capacitor is selected according to (3-12). It is recommended to employ a damper resistor of R_L in series with C_L.

$$C_L = \frac{L_{L2}}{Z_b^{\,2}} \tag{3-12}$$

The summary of line filter design for both the single inductor and the LCL solutions is listed in Table 3-3.

Table 3-3- Line Filter Parameters

L_{ac}	L_{L1}	L_{L2}	C_L	R_L
10/5 mH	1.5 mH	2.5 mH	2.6 μF	10 Ω

3.5.2. Dc Link Capacitor

The dc link capacitor (C_D) can be selected according to the desired ripple factor (RF). The equation is given in (3-13), in which S is the apparent power. As calculated in

(3-14), the required dc link capacitance is 1 mF. The voltage rating should be around 450 V.

$$C_D = \frac{S}{2.RF.V_d^2.\omega_n} \tag{3-13}$$

$$C_D = \frac{1600}{2 \times 0.05 \times 200^2 \times 120\pi} = 1mF \tag{3-14}$$

3.6. Snubberless Dual Active Bridge Converter

The DAB is a two-stage power converter topology that is formed by two voltage source dc-ac converters connected through an inductive ac link [72, 102]. The DAB topology offers inherent soft switching at certain boundaries and good voltage utilization of the switches; such characteristics promise a high power density solution for various applications dealing with bidirectional power flow between the isolated dc sources [64, 71, 73-76, 78]. Fig. 3-7 shows a DAB converter, which is realized by MOSFETs. The series ac link is a passive network cascaded to the ac ports of the bridges. The ac link includes a magnetic circuit containing an ac inductor of L and an isolation transformer of T. The inductor is the key element of exchanging power between the bridges; the transformer is needed to provide the galvanic isolation between the dc ports of the DAB converter.

According to the modulation method, the switches' commutation may occur at the Zero Voltage Switching (ZVS) condition during turn on, or the Zero Current Switching (ZCS) condition during turn off [80, 135-137]. The basic and the most common modulation method is the phase shift modulation. In the phase shift modulation, both active bridges generate square waveforms with a certain phase shift

over the ac link inductor to control the power flow between the bridges. The phase shift modulation method offers the highest power transfer capacity, high efficiency, and low Electromagnetic Interference (EMI) while ZVS happens. The alternative modulation methods [80, 135-137] try to extend the soft switching region and try to improve the efficiency when the converter operates at a lower power level. Both the modulation method and the circuit parameters affect the DAB commutation in a desired operating point. The commutation cycle analysis provides a valuable insight into the DAB operation boundaries.

In [72, 78], commutation is modeled between snubber capacitors in parallel with switches and the ac inductor. The output capacitor of the device is neglected compared to the snubber capacitor. The parallel snubber capacitor acts as a turn off snubber, assuming the switches have the ZVS condition at the turn on. The snubber capacitor works against the turn on commutation when the converter is out of the soft switching region; moreover, there is a tendency to reduce the component count in the commercial applications. The counted facts suggest that the switches' output capacitors be utilized for the commutations. The modulation methods suggested by [137] considers a Snubberless DAB circuit; however, the commutation is not analyzed, and the authors suggest an approximated boundary to have ZVS phase shift modulation. In [138], the presence of nonlinear switch capacitors in DAB operation is discussed; however, the approximated linearization only includes one equivalent capacitor depending in the operating mode. The solution when soft switching happens is similar to the case a turn off snubber exists in the circuit.

This section provides a novel analytic method to model the commutation of the DAB converter, and the effect of nonlinear output capacitors is addressed. The analyses are developed for a power MOSFET based DAB prototype suitable for a vehicular power conditioner. The analyses are inspired by phenomena realized during experiments that were performed on the experimental setup, and the results are verified by the same prototype.

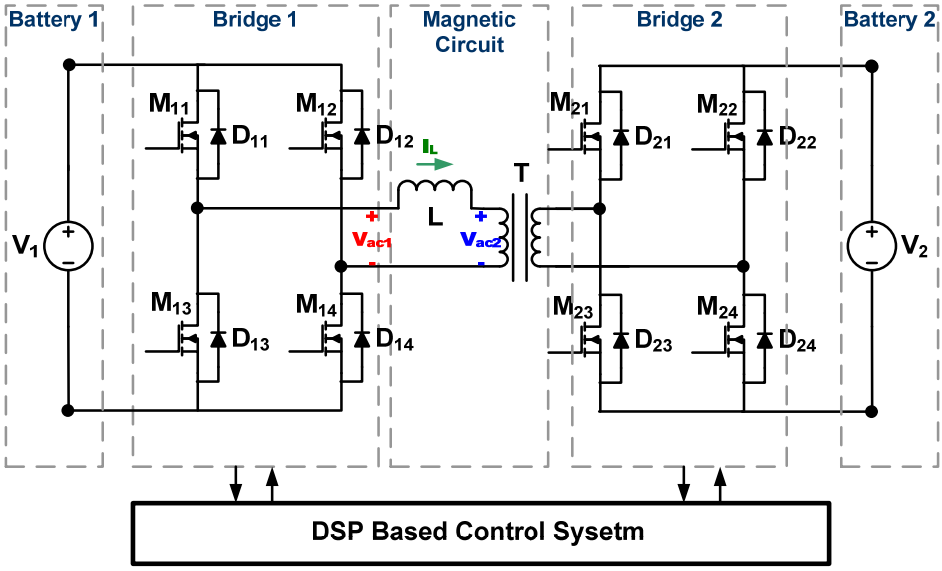

Fig. 3-7- DAB Converter

3.6.1. Dual Active Bridge Fundamentals

The simplified dual active bridge converter can be modeled when V_{ac1} and V_{ac2} in Fig. 3-7 are replaced with the equivalent sources and the magnetic circuit is replaced with the equivalent series inductor as shown in Fig. 3-8. In this model, the circuit is transferred to the primary side. Each active bridge can generate an ac waveform in one

side of the equivalent series inductor. The power flow is controlled by shaping the inductor current.

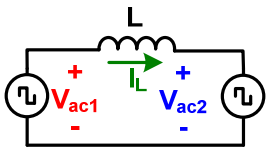

Fig. 3-8- Equivalent DAB converter model

In the phase shift modulation, the inductor L is supplied by two ac sources of V_{ac1} and V_{ac2} where there is a phase shift of ϕ between the ac sources. Both V_{ac1} and V_{ac2} are square waveforms alternating with the switching frequency of f_{sw}. The power flow will be towards the ac source that leads in phase. The amplitude of the ac waveforms does not affect the power flow's direction. Fig. 3-9 helps to visualize the phase shift modulation.

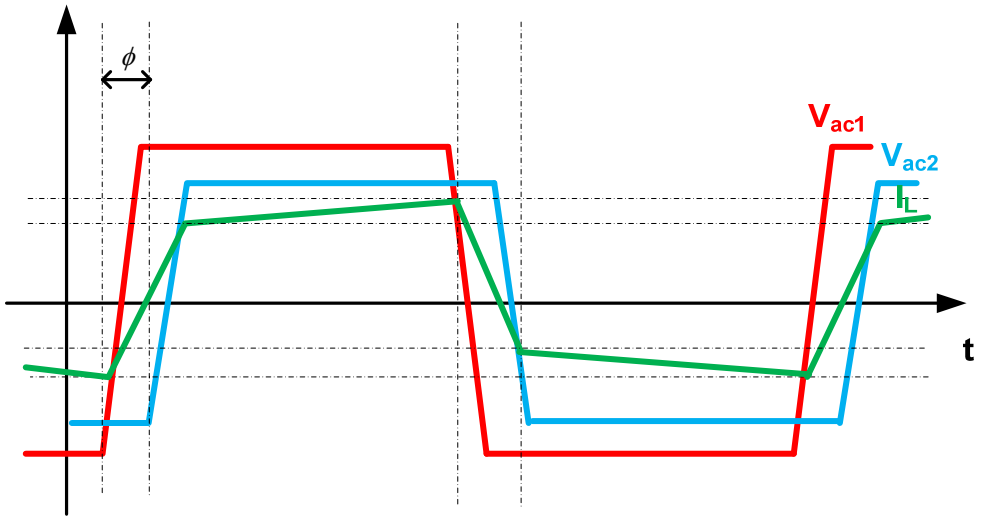

Fig. 3-9- DAB waveforms during phase shift modulation

The average power transferred between two ac sources is determined by (3-15) [102, 139]. According to (3-15), the transferred power P through series ac link is related to the frequency of ac sources f_{sw}, the amplitude of the ac source V_{ac1} and V_{ac2}, the inductance L, and the phase shift ϕ between the ac sources.

$$P = \frac{V_{ac1} V_{ac2} \phi(\pi - \phi)}{2\pi^2 f_{sw} L} \tag{3-15}$$

In (3-15), all the values are transferred to transfers primary side. Specifically, V_{ac2} is defined as the transformers primary voltage and includes the transformer's turn ratio of n. The phase shift modulation power equation can be adopted for the dc-dc converter of Fig. 3-7 as (3-16). V_1 and V_2 are the dc sources that can be replaced with the dc link voltage and the battery's voltage in the three-stage isolated VPC.

$$P = \frac{n V_1 V_2 \phi(\pi - \phi)}{2\pi^2 f_{sw} L} \tag{3-16}$$

The transferring power equation (3-16) is an approximating model that does not count several operating details and several second order effects as reported in the previous works [102, 137, 140-148] and as investigated in this dissertation. Nevertheless, this equation is a strong and insightful tool in analyzing the DAB fundamentals. The transferring power equitation is utilized in the design approach explained in the next subsection.

3.6.1.1. Dual Active Bridge Design Considerations

In this sub section, a DAB design approach is proposed. The parameters determining the power transferred through the series ac link are investigated as potential design parameters.

Assuming V_1 is the dc link voltage and V_2 is the battery voltage in (3-16), these two parameters are determined by the system. The battery voltage is determined by the vehicle designer and the dc link voltage is limited by the grid. Hence, for a single phase line V_1 is limited by maximum line amplitude according to (3-17). This is not a traditional DAB design parameter; however, it is utilized in the variable dc link control method of the decoupled three-stage isolated VPC, which is a contribution of this dissertation. This method will be described later in this chapter.

$$V_1 \geq \sqrt{2}V_{ac(\max)} \tag{3-17}$$

The link frequency can be varied to control the transferred power. In this dissertation, the switching frequency is constant and is not utilized as a control variable. The switching frequency is a design variable. The switching frequency affects the size and the efficiency of the magnetic circuit as it will be described in chapter 4. The switching frequency also affects the converter efficiency although the converter has soft switching properties. The switching frequency can be selected during an optimization process to meet certain design criteria [149, 150]. The converter optimization is not a goal of this dissertation and the switching frequency is selected as 40 KHz due to a few practical considerations.

The inductance L is the specific parameter that can be designed for the series high frequency ac link operation. According to (3-18), the maximum power transfer through the ac link can happen at π/2 phase shift. Thus, the maximum transferred power is formulated as (3-19). In (3-19), L is the only link parameter that can limit the transferred power. This property can be utilized for increasing the reliability of the design. The larger series ac link inductance results in the lower sensitivity to phase shift perturbations and the lower power limit. In contrast, the larger ac inductor and the lower utilization factor is the price paid.

$$P_{\max}\Big|_{\phi=\frac{\pi}{2}} = \frac{nV_1V_2}{8f_{sw}L} = \frac{k}{L} \tag{3-18}$$

It is preferred to set the maximum transferred power happening at a phase shift below π/2 to avoid excessive reactive power and improve the ac link utilization factor. As an example, if the maximum phase shift is set at π/6, and the transformer is set at 4, the L would be designed as 43 μH for the ratings of (3-16). According to (3-18), the maximum power is limited by 2.9 kW for this design.

$$L = \frac{nV_1V_2\phi(\pi-\phi)}{2\pi^2 f_{sw}P_{nom}} \tag{3-19}$$

$$L = \frac{4\times 200\times 50\times \frac{\pi}{6}\times(\frac{5\pi}{6})}{2\pi^2\times 40\times 1.6\times 10^6} = 43.40\,\mu H \tag{3-20}$$

3.6.1.2. Dual Active Bridge Operation Curves

As described, all the parameters present in (3-16) are used in the DAB's design procedure. The reaming parameter is the phase shift between the ac sources that can be manipulated as the control variable for determining the power flow during the operation.

The DAB converter is implemented in the SIMULINK environment, as shown in Fig. 3-10, in order to investigate the behavior of DAB versus phase shift angle. According to the component model details an approximate efficiency curve is realized from this study.

The DAB efficiency and transferred power are plotted versus the phase shift delay in Fig. 3-11 and Fig. 3-12, respectively. A per-unit (pu) design is considered for this case study. The power base is selected at 1 pu to happen at 30^o phase shift. The rated voltage is considered as the voltage base.

$$\begin{cases} P_{base} = 1.6kW \\ V_{base} = 180V \quad , L = 35.15\mu H = 1.74\mu(pu) \\ Z_{base} = 20.25\Omega \end{cases} \tag{3-21}$$

Simulation shows maximum power can be transferred at 91° and maximum efficiency occurs at 14°. In this simulation dead-time is assumed at 1μs and the nominal power occurs at a phase shift less than 30°. The phase shift should be limited in order to prevent the converter to operate at power above the designed value.

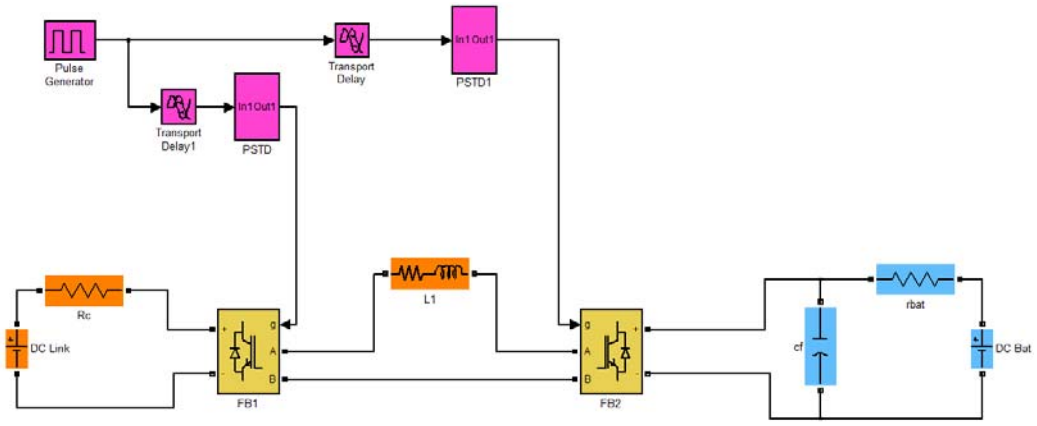

Fig. 3-10- Equivalent circuit of DAB in MATLAB SIMULINK

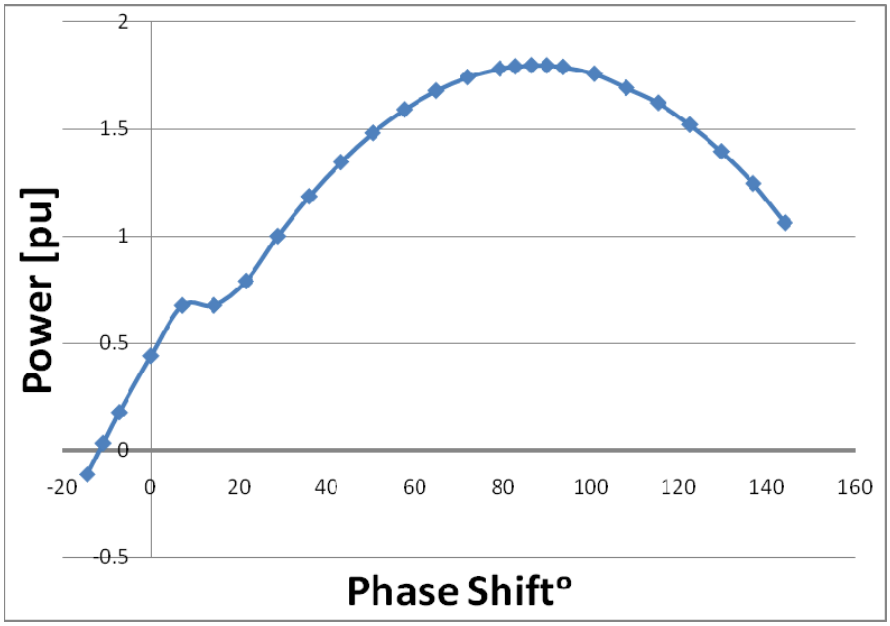

Fig. 3-11- Transferred power curve versus phase shift

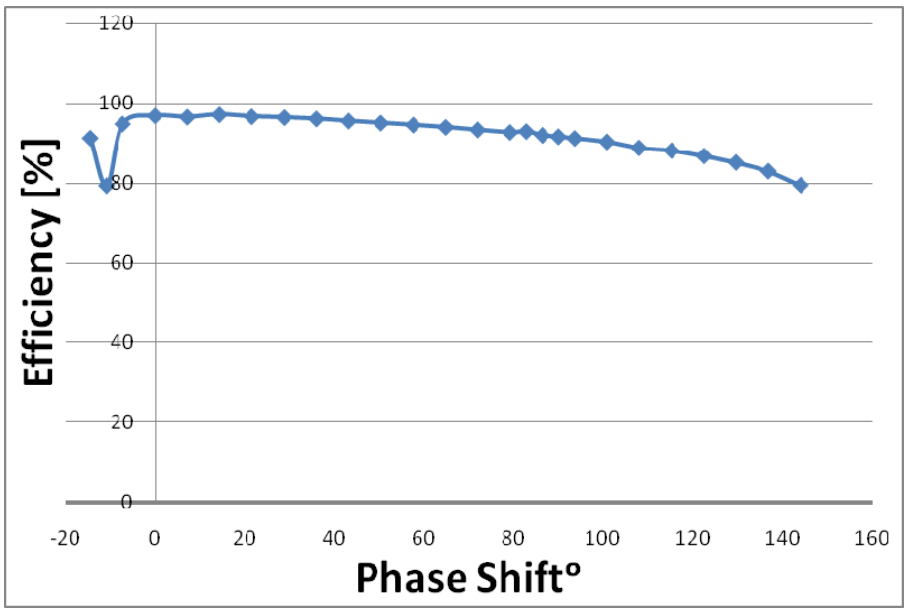

Fig. 3-12- Efficiency versus phase shift

3.6.1.3. DAB Dc Capacitors

In the previous subsections, the DAB was always supplied by the ideal dc sources at both ends. In the integrated vehicular power system, an active load may be placed at the DAB or multi active bridge output. In this case, the output capacitor needs to be selected appropriately to maintain the DAB's dc voltage. Similarly, the capacitors are needed when the batteries are conditioned with DAB. The dc capacitors decrease the batteries' ripple.

In [80], the DAB dc capacitors are designed in a way the time constant of the output capacitor and the series inductor are five time slower than the switching frequency. Adopting this design consideration, the minim dc capacitor is calculated as (3-23). The frequency according to the series ac link inductance and DAB's output capacitor is defined as f_{LC}. C_B is the DAB dc capacitor as shown in Fig. 3-1 (C_{B1} and C_{B2}). The designed DAB dc port capacitors are listed in Table 3-4. C_{ds} is the dc link snubber capacitor on the middle bridge. This capacitor is parallel with C_d. The best material for these capacitors is Polypropylene that is also known as MKP in industries.

$$f_{LC} = \frac{1}{2\pi\sqrt{LC_B}} \leq 5 f_{sw} \tag{3-22}$$

$$C_B = \frac{1}{4\pi^2 f_{LC}^2 L} \geq \frac{1}{100\pi^2 f_{sw}^2 L} \tag{3-23}$$

Table 3-4- DAB Output Capacitors

Middle Bridge	48 V Battery Bridge	12 V Battery Bridge
C_{ds} = 1 µF, 600 V	C_{B1} = 26 µF, 300 V	C_{B2} = 220 µF, 50 V

The experimental waveforms shown in Fig. 3-13 and Fig. 3-14 both belong to the DAB operation with 50 µH inductance and 25° phase shift. The primary is supplied with 30V dc voltage and the secondary supplies a 25.1 Ω resistive load. The ac link waveforms and the dc output are shown. In Fig. 3-13, C_{B1} is 1 µF and the output voltage is not dc. The output voltage is pulsed and has also becomes negative. The ripple also affects the ac link waveforms specifically the secondary side ac voltage and the ac link current. In contrast, C_{B1} is increased to 26 µF in Fig. 3-14 when all other experiment parameters are similar to Fig. 3-13. As can be seen, the output capacitor is able to maintain the output dc voltage and the ac link waveforms are as expected for DAB. For more information about these two experiments, please refer to the section 6.2.

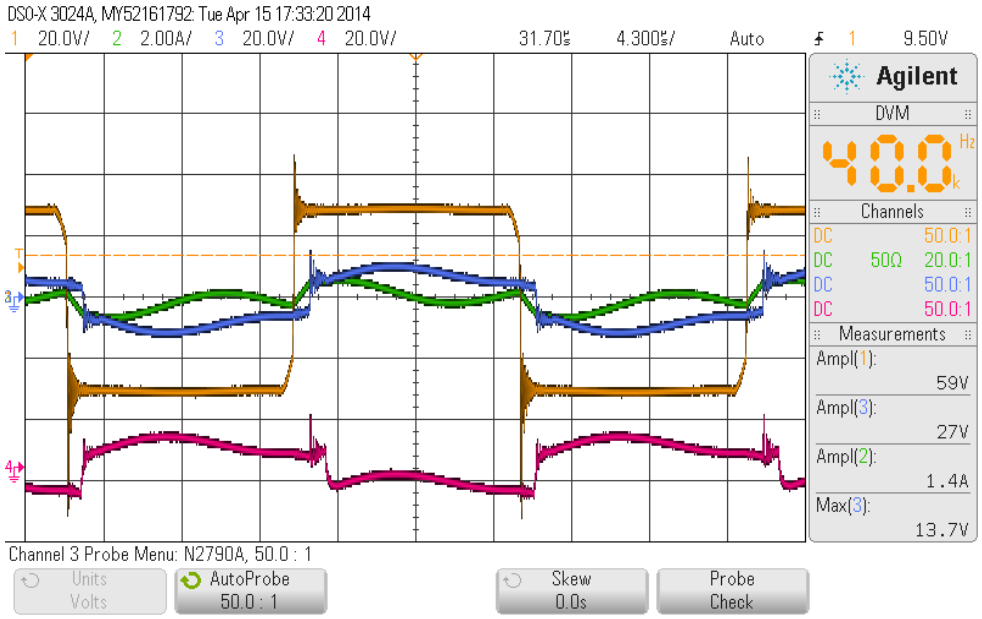

Fig. 3-13- DAB supply R_L=25.1 Ω , V_{in}=30 V , ϕ=25°

yellow: V_{ac1}, blue: V_{ac2}, green: I_L, magenta: V_{RL}

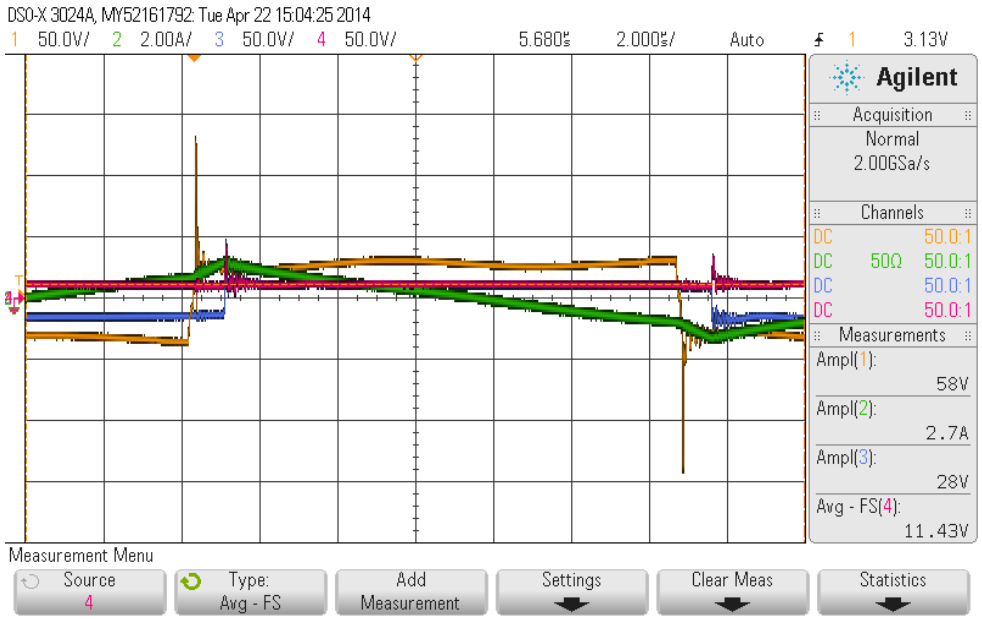

Fig. 3-14- DAB supply R_L=25.1 Ω , V_{in}=30 V , ϕ=25°

yellow: V_{ac1}, blue: V_{ac2}, green: I_L, magenta: V_{RL}

3.6.2. Snubberless Commutation of DAB

The fundamental operation of the DAB was described in the previous section. In practice, the second order details affect the DAB operation. The effect of switches output capacitances and the deadtime of the bridges are among such details. The Snubberless commutation of the DAB is presented in this section to address effects of the dead time and the switches' output capacitors. This is among the contributions of this dissertation.

An experiment is presented to emphasize the motivation of this study. In theory, the soft switching region is not limited when the dc voltages of DAB are equal [72]. To demonstrate this condition, the transformer is removed from the circuit, and the primary bridge is supplied through a dc link. The dc link is supplied from an auto transformer and a rectifier circuit. The phase shift is set at 15° over the series gapped inductor of 42.6

μH, and the 48 V battery is charging at 0.76 A. The waveforms look neat in Fig. 3-15; however, in the next screenshot, the waveforms become like Fig. 3-16. In Fig. 3-16, the input voltage has changed due to the double frequency ripple of dc link. The inductor current is not enough to perform the commutation in this instance and undesirable resonances happen. The dead time of switches and the minimum current of the ac link inductor are the effective parameters to secure a successful commutation in phase shift modulation. These quantities will be analyzed in this section.

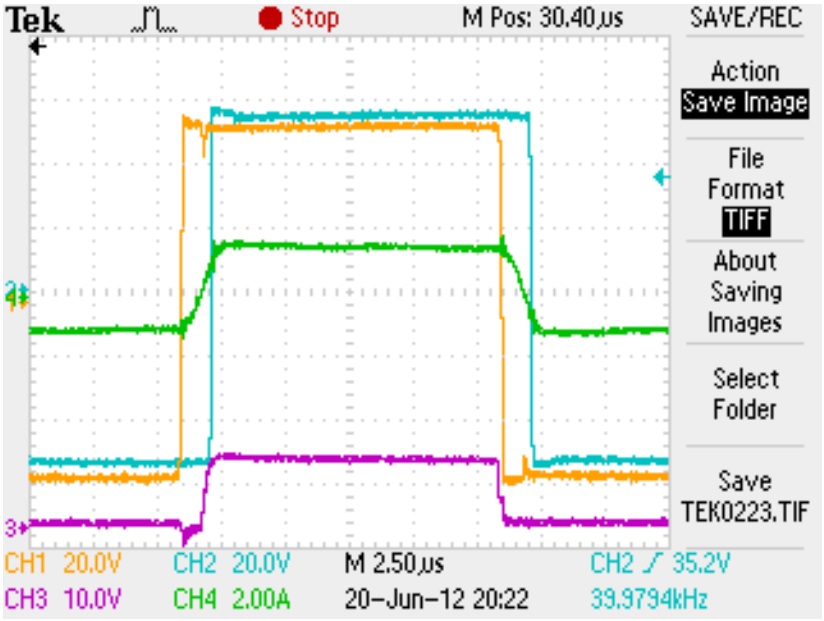

Fig. 3-15- Charging 48 V battery (V_2) from dc link (V_1), 15° phase shift, $V_{1(avg)}$=48.4 V, $I_{1(avg)}$=0.80 A, $V_{2(avg)}$=52.9 V, $I_{1(avg)}$=0.76 A, orange: V_{ac1}, blue: V_{ac2}, green: I_L magenta: $V_{GS(21)}$

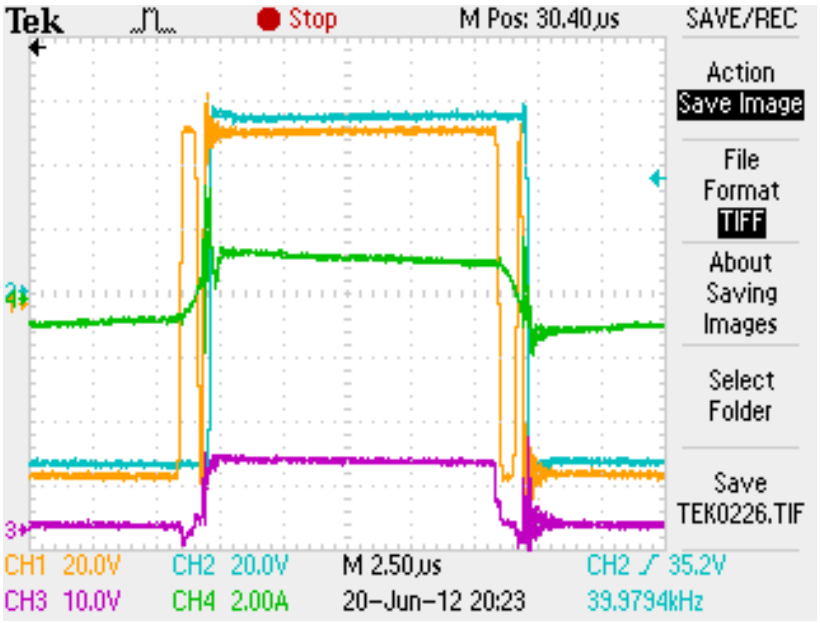

Fig. 3-16- V_1 changes due to dc link ripple versus Fig. 3-15, $V_{1(avg)}$=48.4 V, $I_{2(avg)}$=0.80 A, $V_{2(avg)}$=52.9 V, $I_{1(avg)}$=0.76 A, orange: V_{ac1}, blue: V_{ac2}, green: I_L, magenta: $V_{GS(21)}$

The DAB's switching states during the phase shift modulation are partitioned in Fig. 3-17. The ac link waveforms are explored through half of the switching period; the other half period has a symmetrical behavior. In Fig. 3-18, the sequences are sketched for more clarity. The same color codes are selected for both figures. The switching states are summarized in Table 3-5.

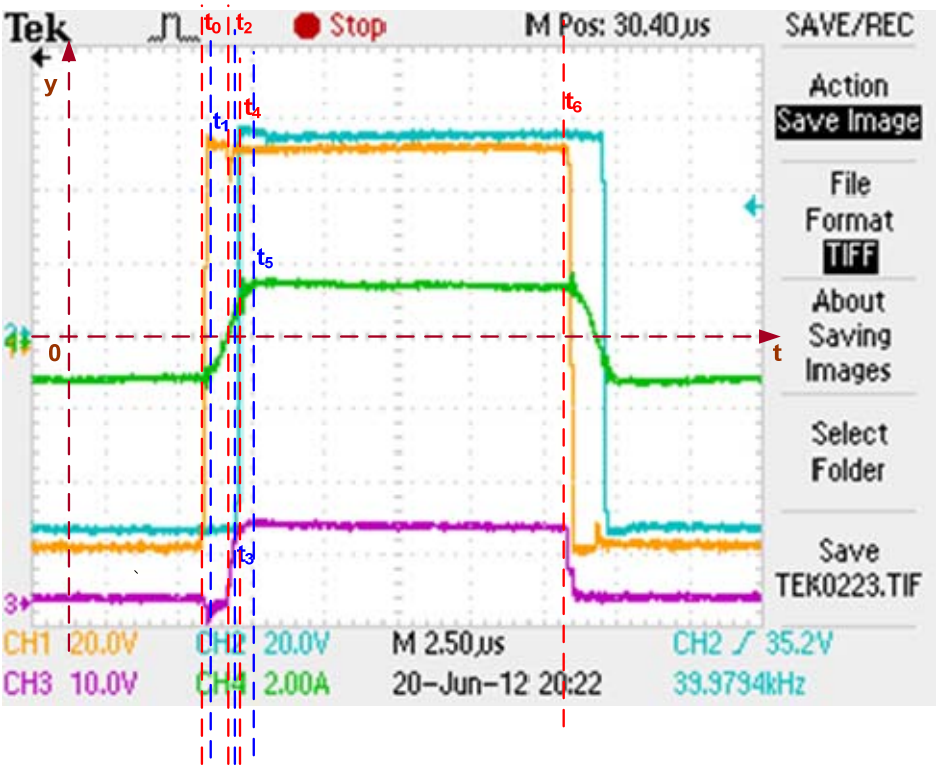

Fig. 3-17- Switching intervals of DAB operation, $V_{1(avg)}$=48.4 V, $I_{1(avg)}$=0.80 A, $V_{2(avg)}$=52.9 V, $I_{2(avg)}$=0.76 A

orange: V_{ac1}, blue: V_{ac2}, green: I_L magenta: $V_{GS(21)}$

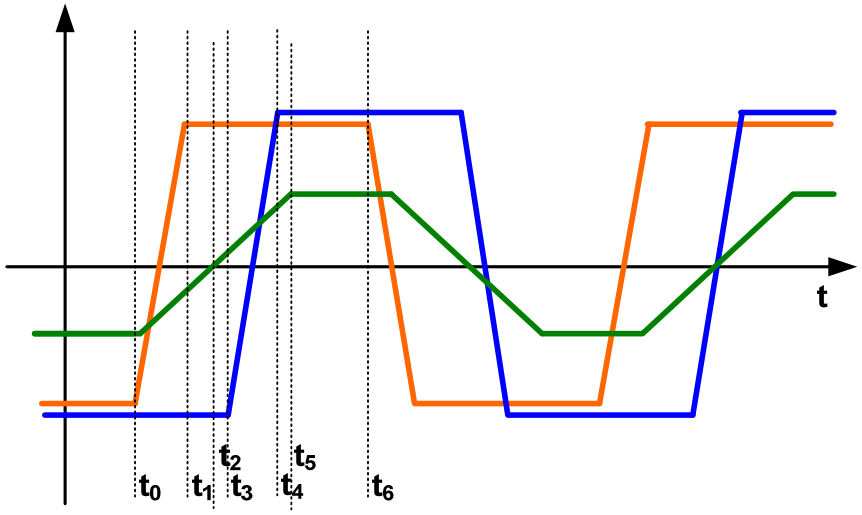

Fig. 3-18- Exaggerated switching intervals of DAB operation, orange: V_{ac1}, blue: V_{ac2}, green: I_L

Table 3-5- DAB's Switching Sates during Phase Shift Modulation

	Before t_0	**t_0**	**t_1**	**t_2**	**t_3**	**t_4**	**t_5**	**t_6**
Bridge1	M_{13} M_{12} ON	M_{13} M_{12} OFF	C_{11},$C_{14}\downarrow 0$ C_{13},$C_{12}\uparrow V_1$	D_{11} D_{14} ON	M_{11} M_{14} ON	M_{11} M_{14} ON	M_{11} M_{14} ON	M_{11} M_{14} OFF
Bridge2	D_{22} D_{23} ON	D_{22} D_{23} ON	D_{22} D_{23} ON	M_{23} M_{22} ON	M_{23} M_{22} OFF	C_{21},$C_{24}\downarrow 0$ C_{23},$C_{22}\uparrow V_2$	D_{21} D_{24} ON	D_{21} D_{24} ON

The state space analysis of the commutation period between t_0 to t_1 leads to:

$$\frac{dq_{11}}{dt}+\frac{dq_{13}}{dt}=i_L \tag{3-24}$$

$$\frac{q_{11}}{C_{11}}+\frac{q_{13}}{C_{13}}=V_1 \tag{3-25}$$

$$L\frac{di_L}{dt}=-V_2+\frac{q_{11}}{C_{11}}-\frac{q_{13}}{C_{13}} \tag{3-26}$$

The component names are in a similar fashion that is shown in Fig. 3-1. The boundary conditions are described below:

$$\begin{aligned}&\text{at } t=t_0:\ q_{13}=0\,,v_{13}=0\,,q_{11}=Q_{GS}\,,v_{11}=V_1\\&\text{at } t=t_1:q_{13}=Q_{GS}\ v_{13}=Q_{GS}\,,q_{11}=0\,,v_{11}=0\end{aligned} \tag{3-27}$$

The critical current boundary condition determines the minimum required deadtime:

$$t_1-t_0=t_{deadtime}\,,\ \ i_L(t_0)=i_{L(\min)}\,,\ i_L(t_1)=0 \tag{3-28}$$

The state variables q_{11} and q_{13} can be reduced to:

$$\begin{bmatrix} \dot{q}_{11} \\ \dot{i}_L \end{bmatrix} = \begin{bmatrix} 0 & \dfrac{1}{1+\dfrac{C_{13}}{C_{11}}} \\ \dfrac{2}{C_{11}} & 0 \end{bmatrix} \begin{bmatrix} q_{11} \\ i_L \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}, \begin{cases} t = t_0 : q_{11} \approx Q_{gd} \\ t = t_1 : q_{11} = 0 \end{cases} \tag{3-29}$$

If the switch capacitors, C_{11} and C_{13}, are to be assumed as equal constant capacitors, (3-29) will lead to the similar results of [64, 72]. This assumption is not true for the Snubberless DAB. The output capacitor of MOSFET is related to its channel voltage, as is modeled in (3-30), [33].

$$q_{11} = C_0' \sqrt{v_{11}} \tag{3-30}$$

$$V_1 = \left(\frac{q_{11}}{C_0'}\right)^2 + \left(\frac{q_{13}}{C_0'}\right)^2 \Rightarrow q_{11}^2 = V_1 C_0'^2 - q_{13}^2 \tag{3-31}$$

If (3-30) is replaced in (3-29), this will result in a nonlinear differential equation that can be solved by numerical methods. An analytic approach is preferred to the numerical solution, because its results can be better utilized in the design process. The nonlinear capacitor can be modeled by a number of linear capacitors; then, it is possible to solve (3-29) for each linear step. Fig. 3-19 shows an example of dividing a switch output capacitor into two linear capacitors referring to the device datasheet [151].

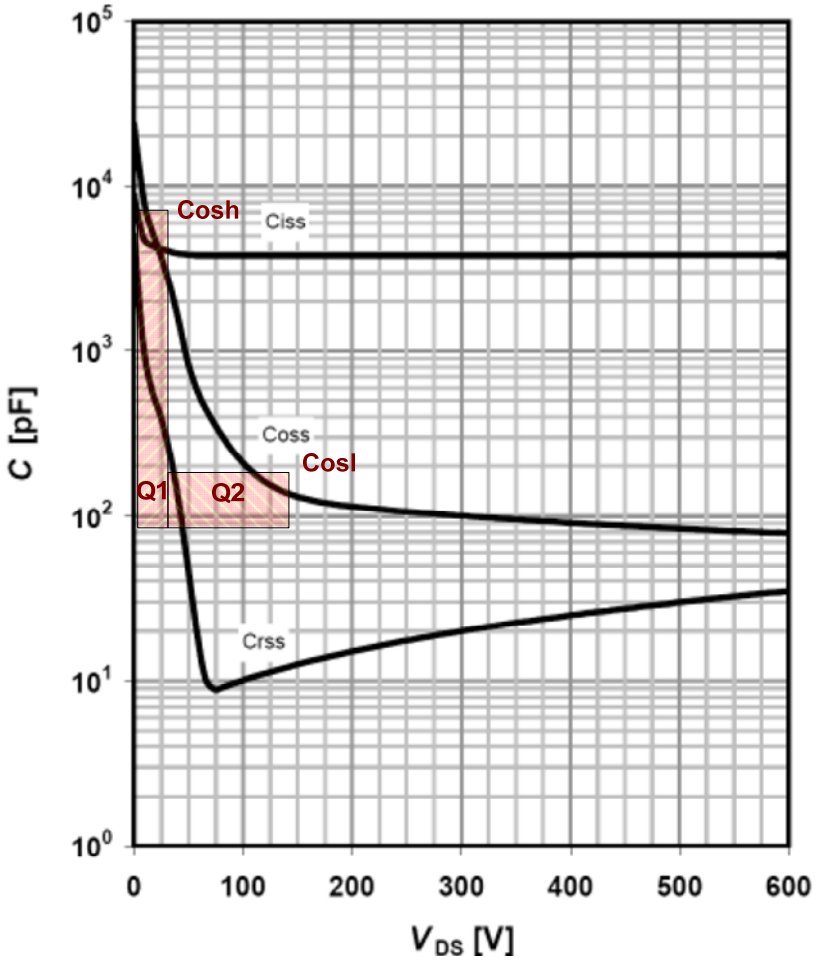

Fig. 3-19- Piecewise linear model of switch capacitor according to device datasheet

The MOSFET output capacitor is modeled by two capacitors, C_{osh} and C_{osl}, in respect to Q1 and Q2 in Fig. 3-19. This breaks the transient between the upper and lower switches (such as M_{21} and M_{23}) into three steps. The solution to the state space equations for the transient phase in between t_0 to t_1 is :

$$\begin{bmatrix} v_{11} \\ i_L \end{bmatrix} = \begin{bmatrix} Z_{eq}Sin(\omega_{eq}t) & Cos(\omega_{eq}t) \\ Cos(\omega_{eq}t) & -\frac{1}{Z_{eq}}Sin(\omega_{eq}t) \end{bmatrix} \begin{bmatrix} v_{11}(0) \\ i_L(0) \end{bmatrix} + \begin{bmatrix} 1-Cos(\omega_{eq}t) \\ \frac{1}{Z_{eq}}Sin(\omega_{eq}t) \end{bmatrix} (V_{DC1}+V_{DC2}) \quad (3\text{-}32)$$

Firstly, the upper switch is on and the lower switch is off:

$$t = t_0 : C_{11} = C_{osl}, C_{13} = C_{osh}$$

$$Z_{eq} = \sqrt{\frac{L}{2(C_{osl} + C_{osh})}}, \omega_{eq} = \frac{1}{\sqrt{\frac{L}{2}(C_{osl} + C_{osh})}} \tag{3-33}$$

Secondly, both switches are in transient and have C_{osl} as output capacitors.

$$t = t_x : C_{11} = C_{osl}, C_{13} = C_{osl}$$

$$Z_{eq} = \sqrt{\frac{L}{4C_{osl}}}, \omega_{eq} = \frac{1}{\sqrt{LC_{osl}}} \tag{3-34}$$

Finally, the commutation has happened. The upper switch is off, and the lower switch is conducting:

$$t = t_1 : C_{11} = C_{osh}, C_{13} = C_{osl},$$

$$Z_{eq} = \sqrt{\frac{L}{2(C_{osl} + C_{osh})}}, \omega_{eq} = \frac{1}{\sqrt{\frac{L}{2}(C_{osl} + C_{osh})}} \tag{3-35}$$

3.7. Conclusion

This chapter introduced a three port onboard VPC as the reference system for the dissertation's research. The ratings of the system and the design considerations were reported briefly. A modular building block based design approach was proposed for the onboard VPC as a contribution of this dissertation. The design method was practiced for developing the experimental setup.

The fundamentals of the DAB converter and the phase shift modulation were reviewed and the important DAB design considerations for the vehicular application were heighted. This chapter emphasized the benefits of the well practiced phase shift modulation for the high power DAB converter applications. The Snubberless implementation of the DAB converter is preferred for practical applications. The phase shift modulation soft switching boundary conditions are an important design criterion. An experiment was presented to show the behavior of the converter at the soft switching boundary conditions. The main contribution of this chapter is analyzing the commutation of the Snubberless DAB. The DAB's commutation cycles during the phase shift modulation were formulated by the state space analysis. The equations are nonlinear due to the device capacitors' presence. A numerical method and a linearization method were proposed. The advantage of the proposed piecewise linear modeling method is the relation of devices' data to the analytical model.

4. MAGNETIC CIRCUITS*

4.1. Overview

The VPC's magnetic components include the low frequency line side inductors and filters, the high frequency ac inductors and the isolation transformer. The low frequency filters are investigated in the previous works [36, 37, 129] and the dissertation focuses on the high frequency ac inductors and the isolation transformer. These magnetic components form the high frequency ac link of the proposed VPC. This chapter is dedicated to the magnetic circuit of the VPC. The design and implementation methodology will be summarized and the contributions will be presented.

The second section of this chapter will introduce an optimized design of the three-winding isolation transformer. Integrating the series ac link inductor into the transformer's leakage will be evaluated. The design will be verified analytically and experimentally. In the third section, three design approaches will be presented for the ac inductors. A novel and innovating design approach that integrates a common mode blocking transformer into the coupled ac inductors will be proposed. The transformer's parasitic capacitors effect on the DAB operation will be demonstrated experimentally. In the fourth section, a novel experimental modeling method will be introduced for modeling multiwinding transformers in detail. The more detailed transformer's model

will be analyzed and verified through simulations and experiments. Finally, the conclusion section will highlight the achievements and contributions of this chapter.

4.2. Quantitative Sweep Design Approach for Isolation Transformer

The multiwinding transformer design procedure will be presented in this section. In the first step, the turn-ratios are selected in order to implement the variable dc link control of the three-stage isolated VPC as described in the following subsection.

4.2.1. Transformer Turn Ratios for Variable Dc Link Control of Three-stage Isolated VPC

The reference VPC has three voltage levels that were introduced in Table 3-1. The goal of the variable dc link control is to supply the DAB with a voltage that is almost equal to the battery voltage at each instance. This rule can be described as (4-1). In this subsection, n is the turn ratio between primary and secondary. The auxiliary winding that supplies the low voltage battery is not discussed. Satisfying (4-1), the minimum allowed high voltage battery ($V_{BAT1(min)}$) needs to be smaller than the maximum allowed line voltage amplitude according to (4-2).

$$V_{dc} \approx nV_{BAT1} \tag{4-1}$$

$$n_{\min} V_{BAT1(\min)} \geq \sqrt{2} V_{line(\max)} \tag{4-2}$$

$$n_{\min} \geq \frac{\sqrt{2} V_{line(\max)}}{V_{BAT1(\min)}} \tag{4-3}$$

According to (4-3), if the variable control method needs to be applied for all the voltage range the minimum turn ratio will be:

$$n_{\min} = \frac{178.2}{38.4} = 4.64 \tag{4-4}$$

In this case, the maximum dc link voltage from the battery side will be:

$$V_{dc(\max)} = n_{\min} V_{BAT1(\max)} = 4.64 \times 59.6 = 276.54\,V \tag{4-5}$$

This will result in an increased maximum dc link voltage when compared to the case the dc link is designed based on maximum allowed line voltage. This will need to increase the ratings and also will have more stress and losses on the line side bridge. A compromised solution between the mentioned design scenarios is satisfying (4-1) for the nominal battery voltage. The battery voltage will stay around the nominal voltage in the majority of the time during the charge and discharge cycles. Thus, the compromised minimum turn ratio is:

$$n_{\min} = \frac{178.2}{48} = 3.71 \tag{4-6}$$

The maximum dc link voltage will be:

$$V_{dc(\max)} = n_{\min} V_{BAT1(\max)} = 3.71 \times 59.6 = 221.1\,V \tag{4-7}$$

The tertiary to secondary winding turn ratio is selected as 0.25 in respect to the nominal voltages of the high voltage and low voltage batteries.

4.2.2. Multiwinding Transformer Design

The initial step in the transformer design is selecting the maximum magnetic field (B_m) to start with. The magnetic field is initially selected as 0.2 T.

$$B_m = 0.2\,T \tag{4-8}$$

The transformer's area product (A_P) is defined as product of the core's cross-section area (A_C) by the core's window area (A_W). The area product is calculated as (4-9) [152]. The core size can be estimated by the transformer's area products. In (4-9), the nominator is sum of the windings currents multiplied by the voltage. It can be approximated as the apparent power for an n-winding transformer. The denominator is product of windows utilization factor of k_u, the career frequency of passing energy, which is equal to the switching frequency of f_s, the maximum magnetic field of B_m, and the winding's current density of J.

$$A_P = A_C A_W = \frac{\sum_{i=1}^{n} V_i I_i}{\sqrt{2}\pi . k_u f_{sw} B_m J} \tag{4-9}$$

According to the VPC's specifications, the A_P is calculated as (4-10). The apparent power with a design overhead is considered as 2 kW for primary and secondary windings and 500 W for the tertiary winding.

$$A_P = \frac{4500 \times 10^8}{\sqrt{2}\pi \times 0.4 \times 40 \times 10^3 \times 0.2 \times 3 \times 10^6} = 10.55 cm^4 \tag{4-10}$$

The minimum A_p is 8.44 cm^4. Upon the availability, the ETD59 core is selected. The A_p for this core is 18.69 cm^4 that provides an extra space to integrate more leakage into the transformer's design. The turn numbers for primary (N_p), the secondary (N_s), and the tertiary (N_t) are calculated as follows:

$$N_p = \frac{D_{\max} V_p}{4 f B_m A_C} = \frac{0.5 \times 220}{4 \times 40 \times 10^3 \times 0.2 \times 256 \times 10^{-6}} \approx 14 \tag{4-11}$$

$$N_s = \frac{D_{\max} V_s}{4 f B_m A_C} = \frac{0.5 \times 60}{4 \times 40 \times 10^3 \times 0.2 \times 256 \times 10^{-6}} \approx 4 \tag{4-12}$$

$$N_t = \frac{D_{\max} V_t}{4 f B_m A_C} = \frac{0.5 \times 15}{4 \times 40 \times 10^3 \times 0.2 \times 256 \times 10^{-6}} \approx 1 \tag{4-13}$$

$$N_{ps} = \frac{N_p}{N_s} = \frac{15}{4} = 3.75 \geq n_{\min} \tag{4-14}$$

The current density for the windings is designed to be less than 4 A/mm^2. Accordingly, the conductors' cross section (A_{cu}) are determined. The primary windings are designed with the Litz wires. The Litz wire minimizes the skin effect, which is 0.33 mm at 40 kHz, and improves the proximity effect. In (4-15) to (4-20) a design example for the primary winding with the Litz wires are presented. D_{cu} is the required conductor diameter, D_s is the strands diameter, δ_{cu} is the effective skin depth (at 40 kHz), A_s is the strands cross-section area, and Ns is number of strands in the Litz wire.

$$I_P = \frac{P}{V_s N_{ps}} = \frac{1.6 kW}{48 \times 3.75} = 8.89 A \tag{4-15}$$

$$A_{cu} = \frac{I_p}{J} = \frac{8.89}{4} = 2.25 A/mm^2 \tag{4-16}$$

$$D_{cu} = \sqrt{\frac{4 A_{cu}}{\pi}} = 1.69 mm \tag{4-17}$$

$$D_s \approx \delta_{cu} = 0.35 mm \tag{4-18}$$

$$A_s = \frac{\pi D_s^2}{4} = 0.09621 mm^2 \tag{4-19}$$

$$N_s = \frac{A_{cu}}{A_s} = 23.386 \approx 24 \tag{4-20}$$

The secondary current is relatively higher when compared to the primary and the number of strands will be impractical for the laboratory prototyping. Hence, the primary winding is designed with the copper foil. The tertiary has the same current rating and shares the same winding design with a quarter of turns. The secondary winding height (h_{foil}) will be the core window's height minus a clearance according to (4-23). The foil thickness is selected as 0.1 mm, which is narrower than the skin depth and all the cross section can be utilized. The foil thickness (d_{foil}) is calculated in (4-24). Two layers of copper foil will be paralleled to achieve the desired cross-section.

$$I_s = I_P N_{ps} = 8.89 \times 3.75 = 33.34\ A \tag{4-21}$$

$$A_{cu} = \frac{I_s}{J} = \frac{33.34}{4} = 8.33\ A/mm^2 \tag{4-22}$$

$$h_{foil} = 41.2 - 4 = 37.2\ mm \tag{4-23}$$

$$d_{foil} = \frac{A_{foil}}{h_{foil}} = \frac{8.33}{37.2} = 0.22\ mm \tag{4-24}$$

4.2.3. Design Optimization

The transformer's losses can be partitioned into two sections, the core loss and the copper losses. The core loss can be calculated from the Steinmetz model [153-155] as of (4-25). The winding losses are defined as sum of resistive windings as (4-26), in which k is number of windings. The ac resistance of each winding needs to be calculated. The skin and proximity effects [156-159] cause the ac resistance of the winding be more than the dc resistance of the windings.

$$P_{core} = \left(\frac{f}{f_0}\right)^m \left(\frac{B_m}{B_0}\right)^n P_0, m = 1.6, n = 2.6 \tag{4-25}$$

$$P_{cu} = \sum_{i=1}^{k} R_{aci} I_i \tag{4-26}$$

$$P_{trans} = P_{core} + P_{cu} \tag{4-27}$$

The ac resistance is related to the dc resistance of the conductor in the winding according to the $F_R(X)$ which is the Dowell model. The ac resistance of the windings that have used Litz wire as the conductor is described as follows. Initially the dc resistance (R_{dc}) is calculated from (4-28). In this equation, l_{mean} is the average length per turn of the winding. And N is the number of turns. The parameter k_{layer}, which is used in the Dowell's model, is calculated from (4-29), in which N_S is the number of strands, d_s is the diameter of the strand, and D_L is the diameter of the Litz wire. X is related to k_{layer} based on (4-30). Finally, the $F_R(X)$ is calculated in (4-31). M_L is the number of layers to the maximum MMF.

$$R_{dc} = \frac{N l_{mean}}{54 A_{cu}} \tag{4-28}$$

$$k_{layer} = \frac{\sqrt{\pi N_S} d_S}{2 D_L} \tag{4-29}$$

$$X = \frac{d_s}{2\delta_{cu}} \sqrt{\pi k_{layer}} \tag{4-30}$$

$$F_R(X) = 1 + \frac{5 M_L^2 N_S - 1}{45} X^4 \tag{4-31}$$

For the windings with foil conductors, k_{layer} and X will be different. In (4-32), k_{layer} is formulated for foils. N_L is the number of turns in each layer, which is 1 for the described design example. The h_{window} is the window height and h_{foil} is the foil ribbon height. X and $F_R(X)$ are modified for the foil windings as (4-33) and (4-34).

$$k_{layer} = \frac{N_L h_{foil}}{h_{window}} \tag{4-32}$$

$$X = \frac{d_{foil}}{\delta_{cu}} \sqrt{k_{layer}} \tag{4-33}$$

$$F_R(X) = 1 + \frac{5M_L^2 - 1}{45} X^4 \tag{4-34}$$

The losses of the transformer can be calculated using (4-25) to (4-34). If the number of turns per each winding is increased, B_m and P_{core} will decrease. On the other hand, P_{cu} will increase due to extending the windings length. An optimized design compromises between the P_{cu} and P_{core}. The number of turns for each winding is a discrete value and the design domain is limited. All the candidate designs can be evaluated looking for minimum losses and maximum efficiency using spread sheet software. The design is formulated in an Excel file. Firstly, the secondary turns are varied around the initial design. This investigation suggests varying B_m by 0.1 T provides accurate resolution for the design. Hence, B_m is varied as a design parameter from 0.1 T to 0.2 T. The design process is performed both for an interleaved transformer layout and a non-interleaved transformer layout. The design results around the optimum design are listed in table Table 4-1. By comparing the designs, B_m of 0.14 T turns out as

an optimum design. The non-interleaved approach is selected to integrate more leakage between the windings.

Table 4-1- Transformer Designs Varying B_m

B_m [T]	N_p	N_s	N_{ps}	P_{cup} [W]	P_{cus} [W]	P_{CU} [W]	P_{core} [W]	P_{trans} [W]	Eff [%]
Non-Interleaved									
0.1	33	9	3.66667	4.975	2.62913	7.60413	1.05462	8.65876	99.1341
0.12	29	8	3.625	3.73703	2.23969	5.97672	1.69422	7.67094	99.2329
0.13	26	7	3.71429	2.9717	1.8846	4.8563	2.08617	6.94247	99.3058
0.14	22	6	3.66667	2.14161	1.55956	3.70116	2.52948	6.23064	99.3769
0.16	20	5	4	1.84957	1.29963	3.1492	11.4235	14.5727	98.5427
Interleaved									
0.1	33	9	3.66667	2.54816	2.2379	4.78606	1.05462	5.84069	99.4159
0.12	29	8	3.625	2.15993	1.96492	4.12484	1.69422	5.81906	99.4181
0.13	26	7	3.71429	1.80794	1.70052	3.50846	2.08617	5.59464	99.4405
0.14	22	6	3.66667	1.48124	1.44364	2.92488	2.52948	5.45435	99.4546
0.15	22	6	3.66667	1.43657	1.44364	2.88021	3.02646	5.90667	99.4093

4.2.4. Multiwinding Transformer Prototype

The three-winding transformer design was optimized in the previous subsections. This subsection describes how the design is implemented. The transformer is implemented completely in-house. To control skin and proximity effects, Litz wires are wound for the primary, and copper foils are selected for the secondary and tertiary. The transformer design summary is presented in Table 4-2. The secondary winding is the first winding, which is wound on the bobbin. The winding layers are isolated using 0.064 mm Polyimide tape with Silicone adhesive, and 0.1 mm Milar film isolates the windings from each other. The tertiary winding is the second winding, between the secondary

winding and the primary winding. The windings are not interleaved to integrate more leakage into the transformer, which contributes to the required ac inductance. When primary and secondary are working as a DAB, the tertiary winding can be either grounded to act as a shield or left disconnected. Fig. 4-1 shows the windings layout, and Fig. 4-2 shows the implemented transformer. The inductive parameters of the transformer are listed in

Table 4-3. The windings are noted as primary, secondary, and tertiary in respect to the dc link, the high voltage battery, and the low voltage battery. L_{lp} is the leakage inductance measured at the primary side, from short circuit test. L_{mp} is the magnetizing inductance, measured from open circuit test, at the primary side.

Table 4-2- Transformer Design Optimization Summary

Bm [mT]	**N1 [turns]**	**N2 [turns]**	**N3 [turns]**	**P_{CU} [W]**	**P_{CORE} [W]**	**η [%]**
Optimal Flux	**150 V winding**	**48 V winding**	**12 V winding**	**Calculated Copper loss**	**Calculated core loss**	**Calculated efficiency**
0.14	22	6	1.5	3.7	3.02	99.33
Core: ETD 59/31/22, material: mf102						

Table 4-3-Transformer's Measured Inductances

	Primary	**Secondary**	**Tertiary**
Leakage inductance	L_{lp} = 7.7 µH	L_{ls} = 0.46 µH	L_{lt} = 1.9 µH
Magnetizing inductance	L_{mp} = 2.56 mH	L_{ms} = 0.175 mH	L_{mt} = 12.66 µH
Winding Resistance	R_p=0.166 Ω	R_s=0.0115 Ω	R_t=0.0051 Ω

Parameters measured with Fluke PM6306 LCR meter

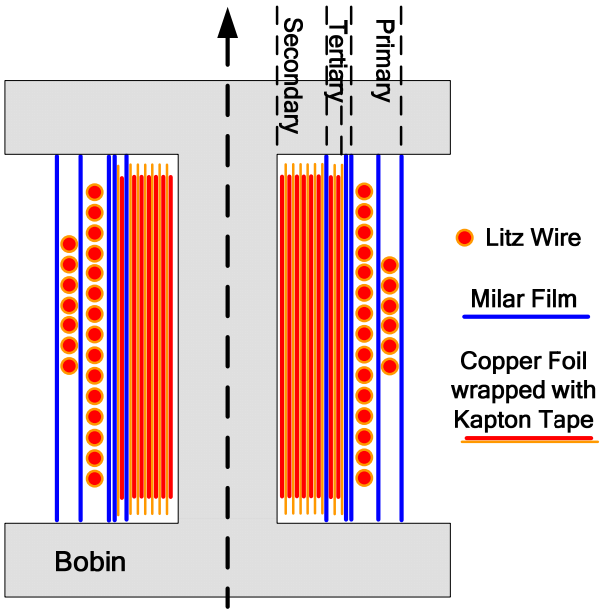

Fig. 4-1- Transformer's windings diagram

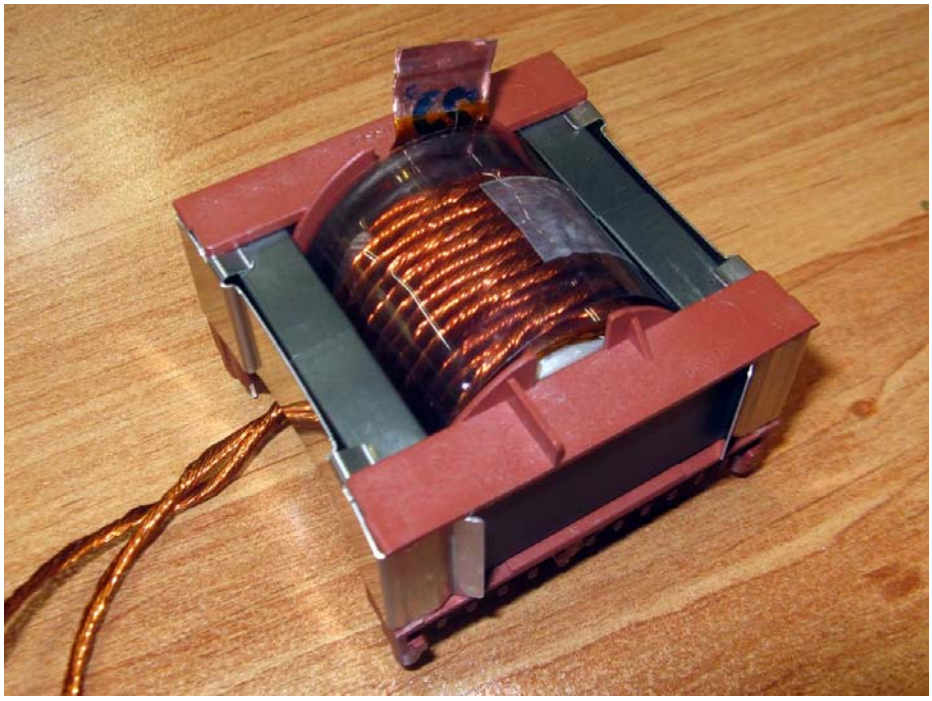

Fig. 4-2- Implemented transformer

4.3. Ac Inductors

The magnetic component design references usually refer to the procedures proposed for the high frequency transformers when they address a design procedure for ac inductors [152, 160]. On the other hand, the references have mainly focused on dc inductors rather than ac inductors. The main difference between dc inductors and ac inductors is how B-H curve is utilized. In the dc inductors, the current has a dc component and the flux will have a dc bias. The B-H loop will be unbalanced. In contrast, there is no dc component in current and flux of the ac inductors and the isolation transformers.

The major difference between ac inductors and ac transformers is storing energy in the core. The energy storage in transformers is limited to the leakage inductance and there is high magnetic coupling between the windings. Looking at the model, the leakage inductance is relatively small and the magnetizing inductance is relatively large in the isolation transformers. In contrast, the ac inductors have to store more energy. Hence, the series inductance will be larger, and the magnetizing inductance will be smaller due to introducing air gap to the transformer.

In this section, three design approaches will be presented for the ac inductors that act as the series high frequency ac link. These design approaches include the gapped ac inductor, the distributed air gap approach and the coupled ac inductors. The gapped ac inductor design method is practiced for the onboard VPC as the reference design. The distributed air gap method is presented as it may be practiced by industries. Finally, the coupled ac inductor is a novel method that is presented as one of the contributions of this

dissertation. The proposed design integrates the common blocking inductance to the linear coupled ac inductor and can improve the VPC by reducing the common mode EMI.

4.3.1. Gapped Ac Inductor

The soft magnetic materials such as ferrites are not suitable for storing energy. They have nonlinear magnetic properties and easily saturate. Hence, an air gap is introduced to the magnetic core and the energy will be stored in the air gap. Introducing the air gap to the magnetic path reduces the effective permeability of the core; however, the air gap results in a linear ac inductor. The air gap volume can be calculated by multiplying the cross-sectional core's area (A_C) by the height of air gap (g). A challenge in design of the gapped ac inductors is controlling the fringing effect around the air gap. Due to the fringing effect no winding can be wound around 2.5g of the air gap.

The design of 40 μH 40 kHz inductor using the UR 57/28/16 core is explained in this subsection. The core material is 3C8 with permeability of 2700. Firstly, the maximum energy stored in the inductor (W_{max}) is calculated.

$$W_{\max} = \frac{1}{2} L_1 I_1^{\,2} = \frac{1}{2} \times 40 \times 10^{-6} \times 6.75^2 = 0.912\, mW \tag{4-35}$$

The required air gap volume (V_g) is calculated according to (4-36). The air permeability is indicated with μ_0.

$$V_g = 2\mu_0 \frac{W_{\max}}{B_m^2} = 8\pi \times 10^{-7} \frac{1.139 \times 10^{-3}}{0.2^2} = 57.2555 \times 10^{-9}\, m^3 \tag{4-36}$$

The air gap height is calculated from the air gap volume in (4-37).

$$g = \sqrt[3]{\frac{V_g}{100}} = \frac{V_g}{A_C} \approx 0.9\,mm \tag{4-37}$$

Finally, the number of turns can be calculated as (4-38).

$$N = \sqrt{\frac{gL_1}{\mu_0 A_C}} = 10\,turns \tag{4-38}$$

The presented design procedure is repeated for all the gapped inductors used for the experimental setup. The winding is implemented with the same Litz wire that was designed for the transformer's primary as was described in 4.2.2. The implemented inductor is shown in Fig. 4-3. The described 43.73 μH inductor is wounded in left leg of the core using Litz wire. The blue winding on the right side is another inductor designed in a similar fashion for the secondary side with value of 7.45 μH. The LCR meter measurements are listed in Table 4-4. The measurements are performed at 40 kHz using Fluke PM6306 LCR meter. The gapped ac inductor design is verified by experiments of subsections 4.4.1 and 0.

Table 4-4- Gapped Inductor Parameters

L_1		**L_2**	
Inductance	***Resistance***	***Inductance***	***Resistance***
43.73 μH	0.0416 Ω	7.45 μH	0.0130 Ω

Measured with Fluke PM6306 LCR meter at 40 kHz

Fig. 4-3- Gapped ac inductor

4.3.2. Distributed Air Gap Approach

The distributed air gap materials are popular solutions for dc and low frequency inductors. Iron powder cores and cool-mu cores are among the materials available commercially in a variety of shapes, sizes, and permeabilities. These materials have iron which is not a good choice for high frequency ac inductors. In some situations, the industries intend to use these cores for high frequency ac inductor design. The main reason is that the practitioner may not determine the difference between the ac inductor and the dc or low frequency ac inductor. The difference was described previously at the beginning of this section. In such cases, it is recommended to utilize multiple cores with

relatively low permeability. This solution is not further discussed in the dissertation considering the dissertation's scope.

4.3.3. Coupled Ac Inductors

Coupled dc and low frequency ac (50 Hz and 60 Hz) inductors have been investigated in the literature [56, 119, 161-165]. The converters using coupled inductors are also named as ripple free converters [166-170]. In the mentioned earlier works, the coupled high frequency ac inductor is not proposed. In this subsection, a novel coupled ac inductor technique is proposed that is a promising candidate for a series high frequency ac link inductor. The proposed coupled ac inductor has an integrated common mode blocking transformer and contributes to the common mode EMI suppression of the isolated VPC.

The coupled ac inductor is wounded in equal turns in two sides of soft ferrite material. A material with relative permeability of 5000, in a UU or UI shape is an ideal core for the proposed technique. The same core that was used for the gapped ac inductor is used for demonstrating a coupled ac inductor. The core's geometry is preferable and the relative permeability is slightly lower than what is desired. The benefit of square-shape core is that the fringing effect will be controlled and the adjacent windings will not heat up.

Calculating the number of turns for a desired value is a complicated task that is heavily dependent on the geometry. A practical solution is proposed in this regard. Initially, one or two turns are wound in each side (n1) and the leakage inductance of L_1

is measured. The required number of turns (n2) to have the desired inductance of L_D is calculated according to (4-39).

$$n_2 = n_1\sqrt{\frac{L_D}{L_1}} \tag{4-39}$$

The proposed coupled ac inductor can be looked at as a zero blocking mesh transformer whose leakage inductance acts as the series differential inductance (L_D). The coupled ac inductor can be modeled as shown in Fig. 4-4.

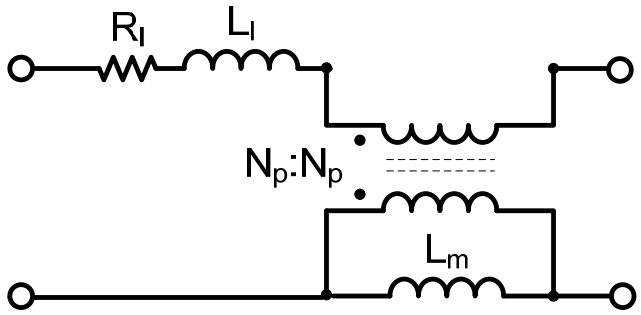

Fig. 4-4- Coupled ac inductor model

During the normal operation, the differential current is applied to the coupled inductor. To test this situation with the LCR meter, the dotted heads are connected to the LCR meter and the other heads are shorted as shown in Fig. 4-5. In this case, the equivalent series inductance is approximately equal to the leakage inductance as (4-40). The actual measurement shows the differential inductance is slightly larger than the leakage inductance.

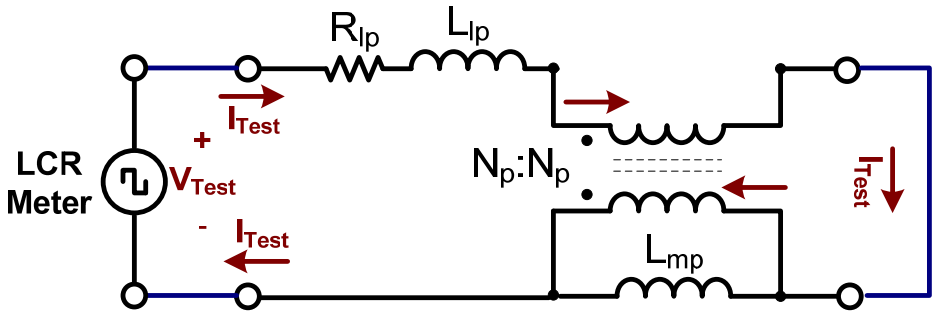

Fig. 4-5- Measuring L_D

$$L_D \approx L_l \tag{4-40}$$

The zero sequence inductance of the coupled ac inductor is defined as the common mode inductance (L_{CM}) in this dissertation. In order to apply the common mode current to the coupled inductor, the test circuit is configured as Fig. 4-6. In this configuration, the test current flows in the same direction through both dotted terminals. Hence, the zero sequence current is applied to the coupled ac inductor. The test condition is compared to the experiment that magnetizing inductance is measured. During the magnetizing inductance measurement, the current passes through the primary winding while the secondary is open. In contrast, the test current passes through both windings in series during the L_{CM} measurement. Hence, the number of turns is twice of the case in which the magnetizing inductance is measured. Therefore, the equivalent inductance (L_{CM}) will be four times of the magnetizing inductance when the common mode (zero sequence) current is applied to the coupled inductor.

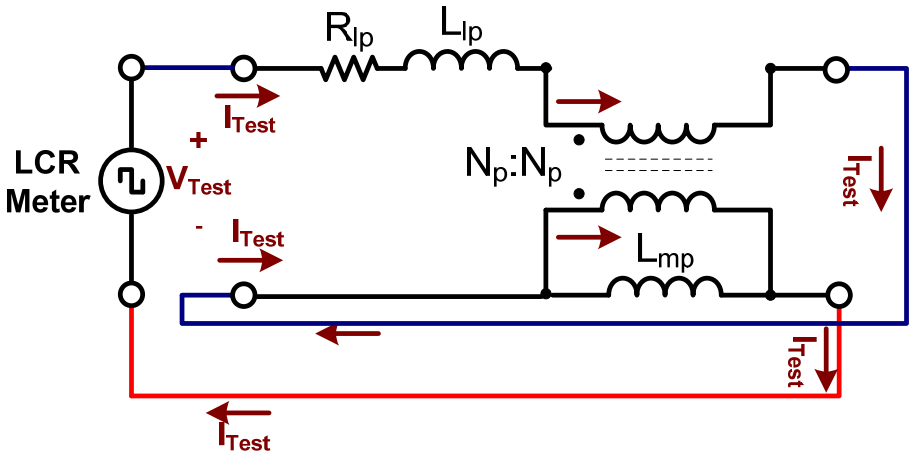

Fig. 4-6- Measuring L_{CM}

$$L_{CM} = 4L_m \tag{4-41}$$

The coupled inductor is implemented with the same Litz wire that was used for transformer's primary and the gapped inductor. The prototype is shown in Fig. 4-7, and the measured parameters are listed in Table 4-5. In Table 4-5, the mesh transformer parameters are measured as a transformer. Alternatively, the coupled ac inductor parameters are measured as described in respect to Fig. 4-5 and Fig. 4-6. Fig. 4-8 shows how the coupled ac inductor can be utilized in the DAB converter. The performance of the implemented coupled ac inductor is successfully verified in the experimental setup. The common mode blocking transformer used in 4.4.1 is the coupled inductor shown in Fig. 4-7. Indeed, an ordinary common mode filter will not pass a 40 kHz waveform due to the high leakage for this frequency and this novel integrated solution is the only practical method for blocking common mode interference at the high frequency ac link.

Table 4-5- Coupled Ac Inductor Parameters

Mesh Transformer			Coupled Ac Inductor		
L_l	R_l	L_m	L_D	R_{LD}	L_{CM}
37.22 µH	0.09 Ω	183.5 µH	41.49 µH	0.0541	731.9 µH

Measured with Fluke PM6306 LCR meter at 40 kHz

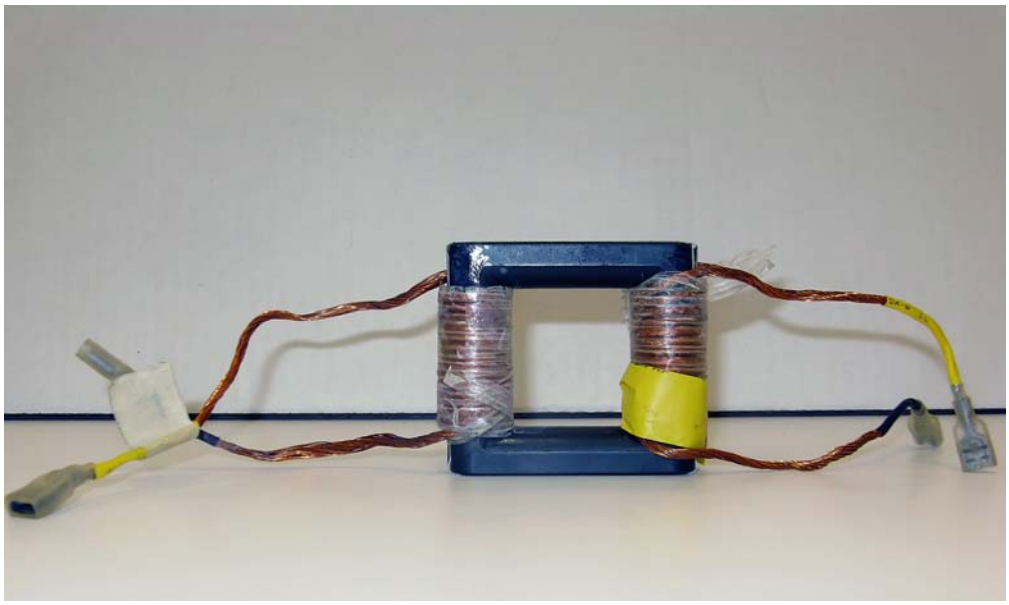

Fig. 4-7- Coupled inductor prototype

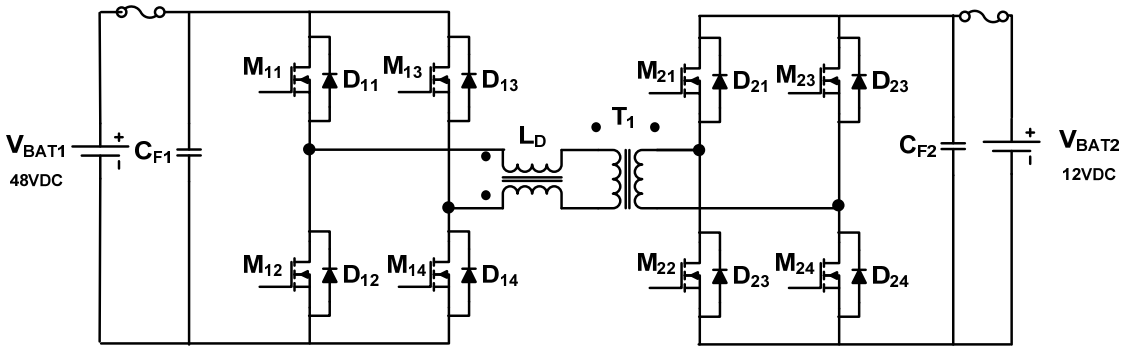

Fig. 4-8- Coupled ac inductor utilized in DAB converter

4.4. Experimental Modeling of Multiwinding Transformer Using Short Circuit Resonance Frequency

The transformer's capacitive elements are distributed over the transformer's structure. Analytic methods suggest calculating these parameters in lumped or distributed form [171-177]; however, the equations can easily become complicated when more details or complicated geometries are introduced. Finite Element Analysis (FEA) can model such elements after describing the structure of the transformer in the FEA tool [104, 178-181]. FEA solvers promise high accuracy; however, the challenge is to draw an accurate geometry. Specifically, manufacturing tolerances are hard to predict and to implement in the tool.

Calculation based methods including FEA analyses are all suitable tools in the design phase of a magnetic circuit. Engineers and researchers also need methods to evaluate the manufactured prototypes and products. Such methods also include the manufacturing tolerances; moreover, the experimental methods are handier for engineers who may not be in charge of magnetic design, or may not access to the FEA tools. The experimental methods, such as frequency response methods, perturb the transformer with a certain set of signals and analyze the observed responses of the circuit [152, 182, 183]. The frequency response methods include a test procedure that leads to a lumped model. A (Line Impedance Stabilization Network) LISN network may or may not be required depending on the procedure. In [152, 182-184], the frequency response of the transformer is measured while the windings are open circuit. In this section, a novel experimental modeling method using the short circuit resonance frequency of the

transformer is proposed, which is among the major contributions of this dissertation. This method will bypass the effect of magnetizing inductance on the test result and estimates the winding capacitors. The inter-winding capacitors are divided into two lumped elements for more accuracy. The detailed procedure to measure and calculate all the model parameters are provided in the following subsections.

Emphasizing the transformer's parasitic capacitances effects, the next subsection presents a few experiments. Moreover, these experiments test the multiwinding transformer that was designed and prototyped for the experimental setup. The modeling procedure will be described afterwards. The more detailed transformer model will be simplified to a third order Π circuit analytically. The transient response of the transformer will be analyzed mathematically. Finally, the proposed modeling method and the analyses will be verified through simulations and experimentally.

4.4.1. Experiments Demonstrating Effects of Transformer's Parasitic Capacitances

A few experiments are presented in this subsection to demonstrate the effect of the transformer's parasitic capacitances in DAB operation. The experimental setup is set to demonstrate the DAB converter as shown in Fig. 4-9 and Fig. 4-10.

The first experiment is charging the 12 V battery from the 48 V battery at 6.58 A. The 50 μH external ac inductor of L is connected to the high voltage side, and the phase shift between bridges is 45°. The waveforms are included in Fig. 4-11. The blue waveform is the ac voltage of the primary side inverter. The yellow waveform is the ac voltage of the secondary side inverter. The magenta waveform is the gate to source

voltage of M_{21}, $V_{GS}(M_{21})$. The green waveform is the inductor current, I_L. There is an overshooting spike over the low side ac voltage transients. This overshoot transient couples to the gate signal.

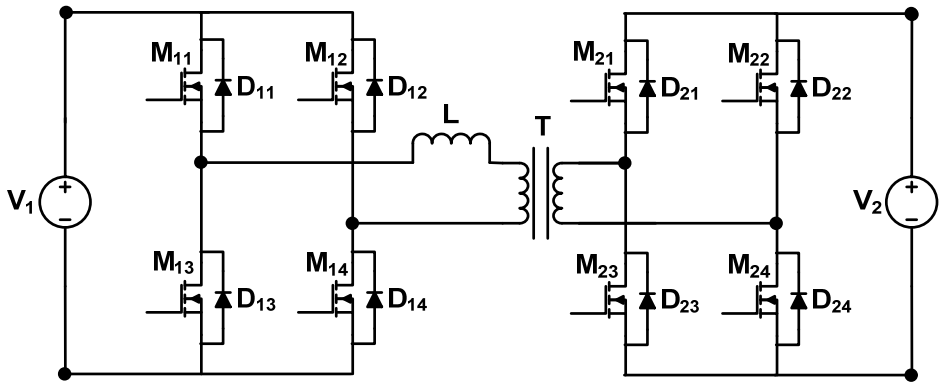

Fig. 4-9- DAB Topology

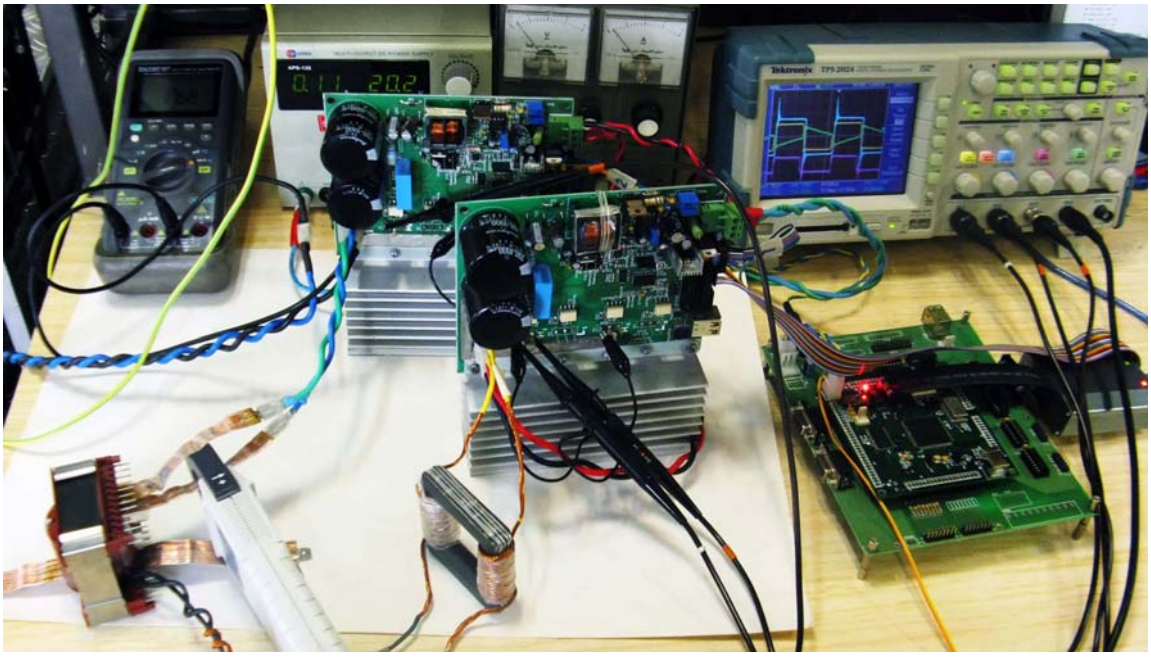

Fig. 4-10- Experimental setup configured for DAB operation

To evaluate the solution suggested by [185], a zero sequence blocking transformer is added to the circuit. This is the integrated coupled inductor designed in subsection 4.3.3. In another experiment, the tertiary winding is grounded to act as a shield between the primary and secondary according to the technique proposed by [186]. None of the mentioned solutions suggested by [185, 186] help in this regard. The waveforms are similar to Fig. 4-11 in both experiments. In contrast, the voltage spike disappears when the transformer is removed.

Fig. 4-12 shows an alternative experiment in which the transformer is removed. The secondary bridge is connected to a dc link that is supplied from an autotransformer and a rectifier circuit. The primary bridge is still connected to the 48 V battery. The waveform assignment is similar to Fig. 4-11. The phase shift is 30^{o} and the 48 V battery is charging at 53.4 V 1.95 A. It is not possible to repeat the exact experiment shown in Fig. 4-11 since the transformer turn ratio is removed from the circuit. The waveforms are clean in this experiment and the spikes have disappeared.

As a summary, the DAB waveforms have an overshoot with the 20 MHz transient that disappears when the transformer is removed from the circuit. These experiments are explained with more detail in section 6.2.3. Such observations suggest the capacitive elements of the transformer contribute to this transient. A more detailed transformer model is suggested in the following subsection that includes the capacitive elements of the transformer.

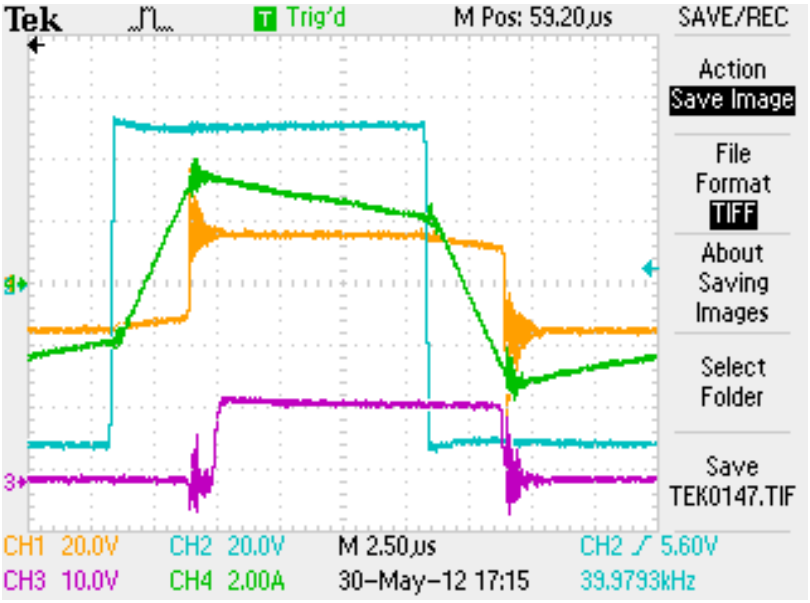

Fig. 4-11- Power flow from 48 V battery (51.4 V 1.98 A) to 12 V battery (13.54V 6.6A), ϕ=45^{o},

blue: bridge 1 ac voltage, yellow: bridge 2 ac voltage, green: ac inductor current I_L, magenta: V_{GS}(M21)

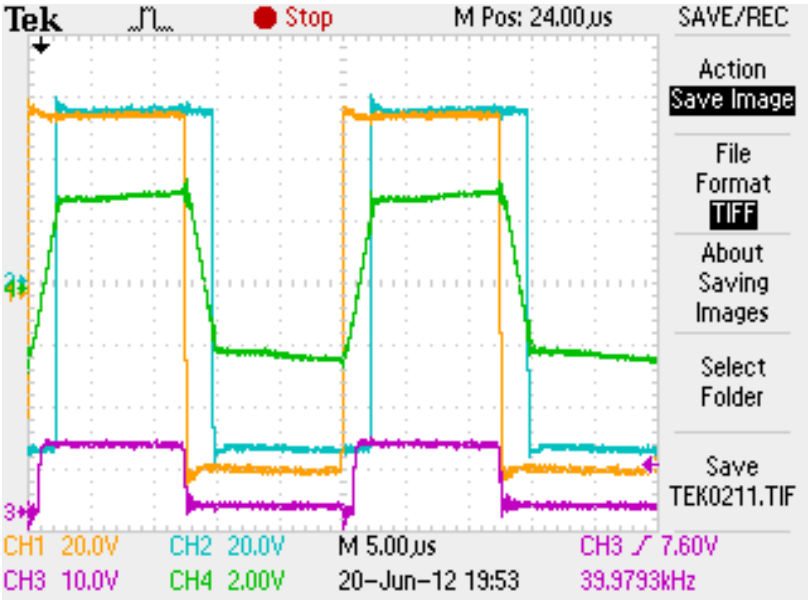

Fig. 4-12- Chagring 48 V battery (53.4 V 1.95 A), transformer is removed, ϕ=30^{o},

blue: bridge 1 ac voltage, yellow: bridge 2 ac voltage, green: ac inductor current I_L, magenta: V_{GS}(M21)

4.4.2. More Detailed Transformer Model

The experiments presented in the previous section suggested investigating the effect of the transformer capacitive elements as a potential source of resonating transients. Parasitic capacitors of a transformer are distributed elements. A novel more detailed transformer model is suggested in this dissertation in Fig. 4-13. This novel model incorporates distributed capacitive elements as lumped capacitors. The model is inspired by [187, 188]. Winding capacitances are placed at the windings' terminals. Distributed inter-winding capacitors are divided into two elements between the windings' corresponding upper terminals and lower terminals.

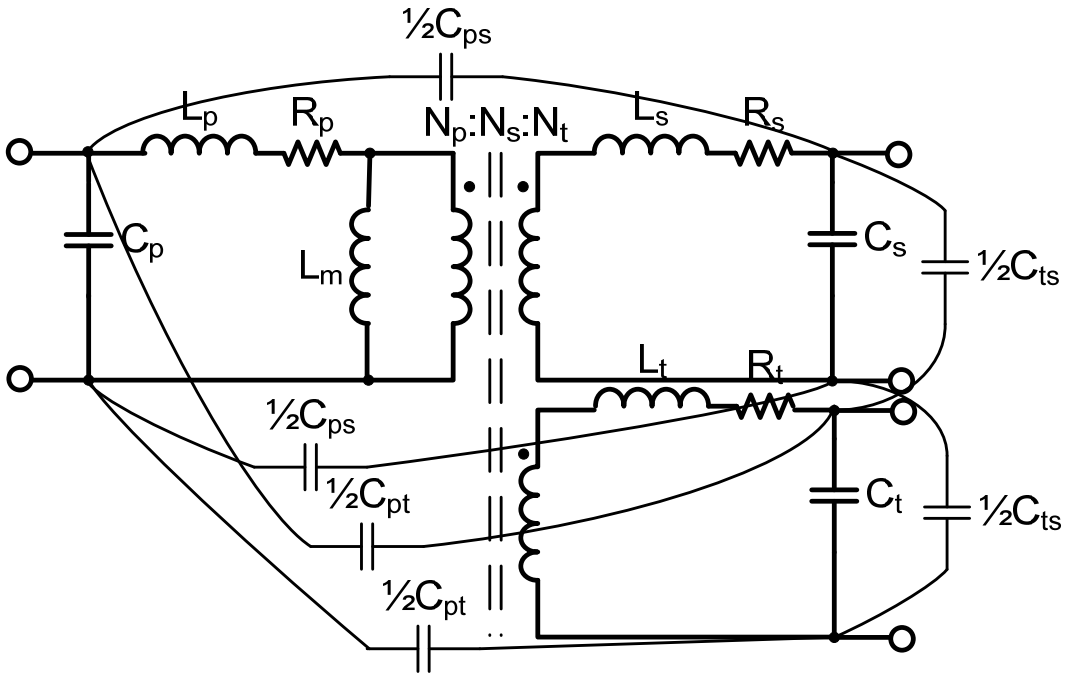

Fig. 4-13- Three-winding transformer model including capacitive elements.

The inductances and inter-winding capacitances can be measured with an LCR meter among the parameters of the proposed model. The winding capacitances cannot directly be measured. An experimental measurement is preferred to a calculation method due to the complicated geometry and the uncertainties of the actual implementation. The frequency response of the transformer is evaluated through two sets of experiments. In both experiments, one of the transformer windings is supplied with a high frequency signal generator through a resistor, Rg. Voltages of both sides of Rg are monitored on an oscilloscope. The voltage amplitude of the transformer terminal shows a peak at any of the resonating frequencies during the frequency sweep. In the first set of experiments, the windings that are not connected to the signal generator are left open circuit. In the second set of experiments, these windings are short circuit. The measured resonance frequencies are listed in Table 4-6. The derivation of the required parameters from the mentioned experiments is described in the following subsections.

Table 4-6- Measured Resonance Frequencies

Other windings are open circuit			**Other windings are short circuit**		
f_p	f_s	f_t	f_p'	f_s'	f_t'
400 kHz	400 kHz	384 kHz	6.9 MHz	24.4 MHz	1.35 MHz

4.4.2.1. Open Circuit Test

This method is suggested in [183] using an impedance analyzer and in [152] using an oscilloscope. In [184], both approaches show a similar result. An oscilloscope and a signal generator are available in almost any power electronics laboratory; hence,

the frequency response tests are performed with an oscilloscope and a signal generator. The equivalent circuit of this experiment for the primary winding is driven as Fig. 4-14. The equivalent capacitor of C_{eqp} is calculated in (4-42). The same method is applicable for the secondary and the tertiary windings. The calculated capacitors are presented in Table 4-7.

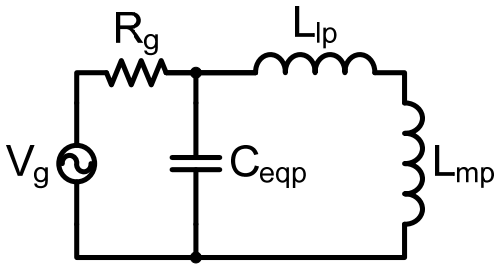

Fig. 4-14- Equivalent circuit of open circuit frequency response test, while the signal generator Vg is connected to the primary winding.

$$f_p = \frac{1}{2\pi\sqrt{L_p C_{eqp}}} \Rightarrow C_{eqp} = \frac{1}{4\pi^2 f_p{}^2 L_p} \tag{4-42}$$

$$L_p = L_{lp} + L_m \tag{4-43}$$

Table 4-7- Results of Open Circuit Test

Equivalent Capacitors			**Nps**		**Nst**		**Npt**	
Ceqp	**Ceqs**	**Ceqt**	**|(Ceq)**	**|(Lm)**	**|(Ceq)**	**|(Lm)**	**|(Ceq)**	**|(Lm)**
61.84pF	904.6pF	13.56nF	3.82	3.82	3.87	3.72	14.81	14.22

All the winding capacitances and the miller effect of the inter-winding capacitances contribute to the equivalent capacitor, which is measured from the open

circuit experiment; thus, this method does not lead to the self capacitances of the windings. The inversed square root of equivalent capacitances, from the open circuit test, is compared to the turn ratios of the windings. These turn ratios are based on the measured value of the magnetizing inductance, at each port of the transformer. As an example, under column of N_{ps}, the L_m column is the primary to secondary turn ratio. In the same table, the value listed under C_{eq} is the corresponding ratio of the equivalent capacitances. The equivalent capacitances can be transferred between windings with a ratio similar to the magnetizing inductances ratio. The ratios are much closer when the tertiary winding, which has a large per unit leakage, is out of the equation. Data from Table 4-6 indicates that measured resonance frequencies of all the windings are within the same range while the primary and the secondary windings have the same resonance frequency. Such observations suggest that the magnetizing inductance is the major element to determine the resonating frequency in the open circuit test. This component is transferred among all the windings; also, the magnetizing inductance is the only nonlinear component of the transformer model of Fig. 4-13. The circuit is excited with relatively low currents when the frequency response is measured and when the LCR meter is applied; hence, the values can relate for (4-42). In contrast, the magnetizing inductance will be set at a different operating point in the actual operation of the circuit. The short circuit frequency response test is performed and analyzed in the next subsection.

4.4.2.2. Short Circuit Test

The equivalent circuit of the short circuit frequency response test for the primary winding is presented in Fig. 4-15. The magnetizing inductance does not contribute to this experiment. Considering the transformer model of Fig. 4-13, the equivalent capacitor of C'_{eqp} is derived in (4-44) when the secondary and the tertiary windings are short circuited.

$$C'_{eq1} = C_p + \frac{C_{ps}}{4} + \frac{C_{pt}}{4} \tag{4-44}$$

$$f'_1 = \frac{1}{2\pi\sqrt{L_{l1} C'_{eq}}} \tag{4-45}$$

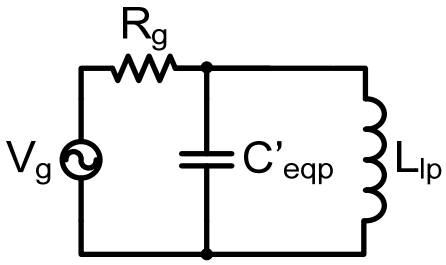

Fig. 4-15- The equivalent circuit of short circuit frequency response test, while the signal generator Vg is connected to the primary winding.

The inter-winding capacitances are measured with LCR meter, and from (4-44) and (4-45) C'_{eqp} is calculated. The mentioned components are listed in Table 4-8. These parameters complete the proposed transfer model of Fig. 4-13. The tertiary winding has the largest capacitance, which agrees with the geometry of this winding. The tertiary winding is one and a half turns of copper foil, which is isolated by very thin Kapton tape.

The analyses suggest looking over the design of this winding, in order to improve its leakage inductance and its capacitance. The secondary winding utilizes the same type of conductor and insulator as the tertiary winding; however, the secondary winding does not have similar issues due to its number of layers, and full coupling of the layers. The outcome of analyzing the mentioned isolation transformer has been insightful to improve the transformer's design, and promises to overcome its performance flaws.

Table 4-8- Capacitive Elements of Transformer Model

Inter-Winding Capacitances*			**Windings Self Capacitances****		
Cps	***Cpt***	***Cst***	***Cp***	***Cs***	***Ct***
67pf	100pf	163pf	27.31pF	35.07pF	7.25nF

*Measured with Fluke PM6306, **Short circuit frequency response test results

4.4.3. Proposed Procedure for Experimental Modeling of Multiwinding Transformers

In the previous subsections, the fundamentals of the proposed experimental modeling method were explained. The difference between measuring short circuit resonance frequency and open circuit resonance frequency were discussed accordingly. In this subsection, the procedure will be summarized in a practical language.

The modeling procedure is developed utilizing the equipments that are commonly available in power electronic laboratories. In the first step, an LCR meter is used for measuring the leakage inductance, the winding resistances, the magnetizing inductance, and the interwinding capacitances. If the LCR meter can apply a variable

measurement frequency, it is recommended to measure the parameters at the nominal switching frequency of the circuit.

The leakage inductance and the windings' resistances are measured at corresponding winding's terminal when the other windings are short circuit. The measured leakage inductance is an equivalent leakage inductance. All the leakage inductances contribute to this measured value.

The equivalent magnetizing inductance at each terminal is measured when other windings are open circuit. The result is the equivalent magnetizing inductance transferred into the corresponding winding. The actual turn ratios between the windings are calculated by the square root of the magnetizing inductances ratios.

The interwinding capacitors are measured by connecting the LCR meter probes to the corresponding transformer winding heads. The author did not notice a difference in measurements whether the other windings are short circuit or open circuit. These capacitors have a distributed nature. To have a more accurate lumped model, half of the measured interwinding capacitance is placed between the positive winding terminals and the other half is placed at the negative terminals as shown in Fig. 4-16.

The proposed method measures the resonance frequency of each winding when the other windings are short circuit. This is the major contribution of the proposed method when compared to the earlier works [182, 183, 189, 190]. In the earlier works, the winding's resonance frequency is measured when the other windings are open circuit. The fundamental advantage of the short circuit resonance frequency measurement is that the magnetizing inductance does not contribute to this value. The

magnetizing inductance is a non-linear component in the transformer model while the leakage inductances and the parasitic capacitances have linear nature. Moreover, the magnetizing inductance is a dominant factor when compared to the parasitic capacitive elements. Hence, an approximate capacitance can be modeled at each winding thanks to the short circuit resonance frequency.

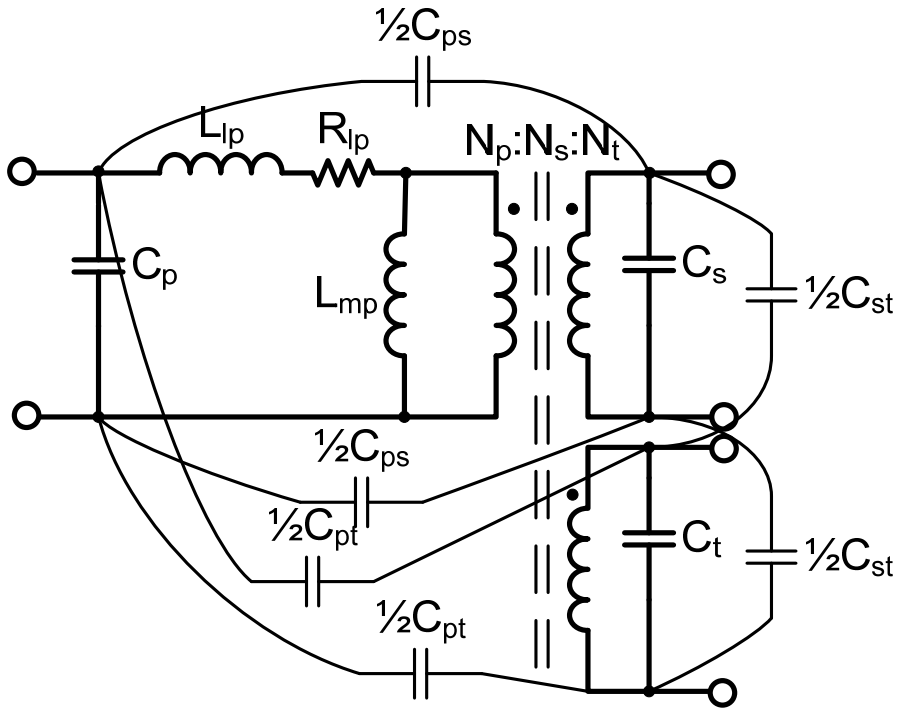

Fig. 4-16- Three-winding transformer model

The short circuit resonance frequency of each winding can be measured with an impedance analyzer or an oscilloscope and a signal generator that are more accessible. The winding is supplied from a high frequency signal generator (V_g) through a resistor (R_g) while the other windings are short circuit. Both the signal generator side and the

transformer side voltages of the resistor are monitored simultaneously on the oscilloscope. Fig. 4-17 shows the equivalent circuit of the primary winding while connected to the described setup. The signal generator sweeps from low frequency until reaches the resonance frequency. At the resonance frequency, the monitored voltages will be in phase and will show a peak.

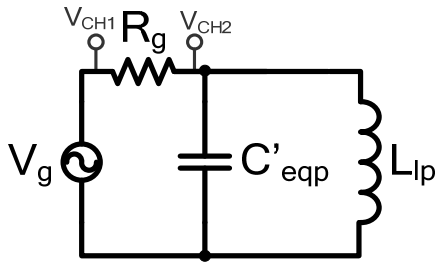

Fig. 4-17- Primary windings' equivalent circuit during short circuit frequency response test

After measuring the resonance frequency of each winding, when the other windings are short circuited, the equivalent short circuit capacitance of each wining are calculated as (4-46). This will lead to the winding's capacitance according to (4-47). In the equations, the suffix p stands for the primary values, s for secondary values, and t for tertiary values. In (4-46) and (4-47) f'_1 is the primary side short circuit resonance frequency, which is measured as described in this section. L_{lp} is the leakage inductance at primary. The interwinding capacitors between primary and secondary and tertiary windings are C_{ps} and $C_{pt,}$ respectively. C_p is the primary capacitance which is calculated in (4-47) according to the lumped model. The other windings capacitances can be calculated similarly.

$$C'_{eqp} = \frac{1}{4\pi^2 L_{lp} f_1'} \tag{4-46}$$

$$C_p = C'_{eqp} - \frac{1}{4}\left(C_{ps} + C_{pt}\right) \tag{4-47}$$

4.4.4. Analyzing Multiwinding Transformer Model

The experimental modeling method based on short circuit resonance frequency was described in the previous section. In this section, the proposed modeling method is applied to the three-winding of Fig. 4-2. The described modeling approach is applied to this transformer and the model parameters are listed in Table 4-9.

Table 4-9- Transformer Lumped Model Parameters

Leakage Inductance	L_{lp}=7.7 µH	L_{ls}=0.46 µH	L_{lt}=1.9 µH
Winding AC Resistance	R_{lp}=0.166Ω	R_{ls}=11.5mΩ	R_{lt}=5.1mΩ
Magnetizing Inductance	L_{mp}=2.56 mH	L_{ms}=0.175 mH	L_{mt}=12.66 µH
Interwinding Capacitance	C_{ps}=67pF	C_{pt}=100pF	C_{st}=163pF
Winding Capacitance	C_p=27.31 pF	C_s=35.07pF	C_t=7.52nF

p : primary (150 V), s : secondary (48 V) and t : tertiary winding (12 V)

In Fig. 4-16, all the inductive elements are reflected into the primary side, which is corresponding to the measured values of Table 4-9. The winding self capacitances are kept at the corresponding winding side where they have been calculated. It is preferred to look at the magnetic circuit electric response at a certain transformer port such as the primary side. This eases the envisioned study by eliminating turn ratios from the equivalent circuit. The self capacitances can easily be transferred to the primary side;

however, this is not the case for the interwinding capacitances. The Fig. 4-16 model is a linear circuit at the nominal operating point. The interwinding capacitors can be reflected to the winding terminals by application of the Miller theorem. The procedure will be described as follows.

The windings are sorted out based on the turn ratios (4-48). In the assigned nomination system N_{ps} is the turn ratio between the primary and the secondary. C_{psp} is the effect of C_{ps} to the primary side (4-49) and C_{pss} is the effect of C_{ps} at the secondary side (4-50). The same procedure is applied to all the interwinding capacitors to derive the transformer model that is presented in Fig. 4-16.

$$N_P > N_S > N_t$$

$$\frac{V_p}{V_s} \approx \frac{N_p}{N_s}, \frac{N_p}{N_s} = N_{ps}, (N_{ps} > 1) \tag{4-48}$$

$$C_{psp} = \frac{N_{ps} - 1}{N_{ps}} C_{ps} \tag{4-49}$$

$$C_{pss} = (1 - N_{ps}) C_{ps} \tag{4-50}$$

The resulted capacitors are formulated in (4-51) to (4-53). These equivalent capacitors can be used when the model is transferred to any arbitrary terminal. A contribution of the analysis presented in this subsection when compared to earlier works originating in [182] is that only one equivalent Miller capacitors contributes to the response viewed from a desired terminal. As an example, only C_{psp} contributes to the forward transfer function of $V_2(s)/V_1(s)$. $V_2(s)$ and $V_1(s)$ are the respective secondary

and primary voltages in frequency domain when the circuit is transferred to the primary side. This fact is verified through simulation and experiments.

$$C_{pi} = C_p + C_{psp} + C_{ptp} = C_p + \frac{N_{ps} - 1}{N_{ps}} C_{ps} + \frac{N_{pt} - 1}{N_{pt}} C_{pt} \tag{4-51}$$

$$C_{si} = C_s + C_{pss} + C_{sts} = C_s + (1 - N_{ps}) C_{ps} + \frac{N_{st} - 1}{N_{st}} C_{st} \tag{4-52}$$

$$C_{ti} = C_t + C_{ptt} + C_{stt} = C_t + (1 - N_{pt}) C_{pt} + (1 - N_{st}) C_{st} \tag{4-53}$$

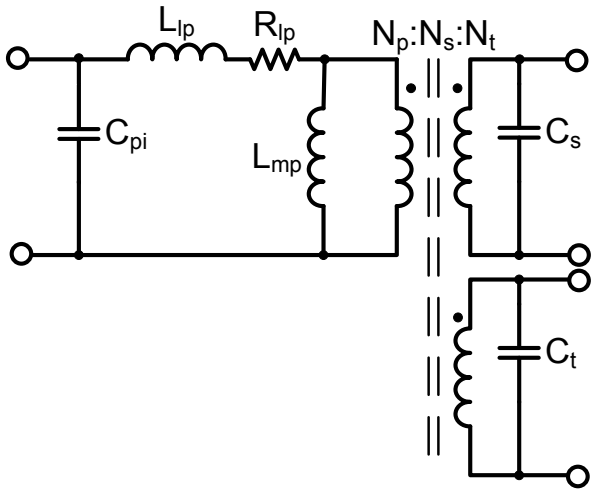

Fig. 4-18- Equivalent transformer model, Miller theorem applied

The transformer model of Fig. 4-18 forms a Π circuit at the primary by transferring C_s and C_t to the primary side. Fig. 4-19 shows this model when the magnetizing inductance is neglected compared to the impedance of C_{po}.

$$C_{po} = \frac{C_s}{N_{ps}^2} + \frac{C_t}{N_{pt}^2} \tag{4-54}$$

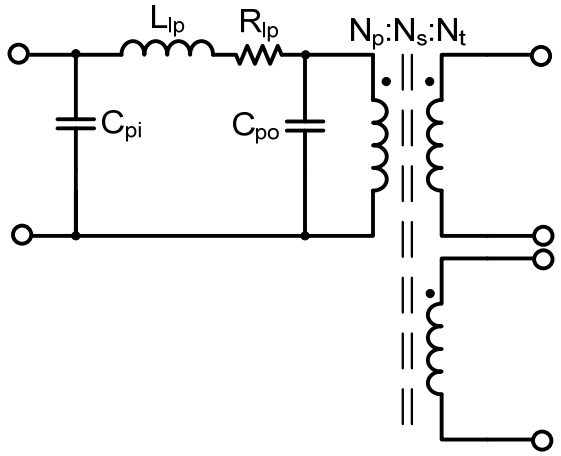

Fig. 4-19- Π equivalent circuit at primary side

4.4.5. Transient Analyses Using Equivalent Transformer Model

The previous subsection leaded to a simplified Π model that reflects all the effective capacitances into the model. This model can be used for further analyses as shown in Fig. 4-20. The model is excited with the source V_1, and the resistor R_2 represents the load of the transformer. The transfer function of V2/V1 is derived as (4-55)-(4-57). In the equations, s is the Laplace variable.

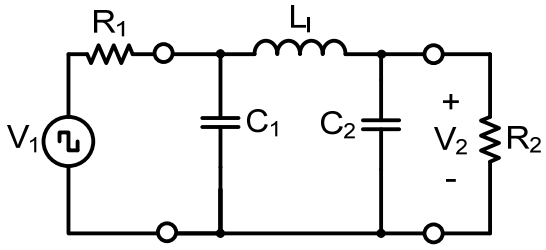

Fig. 4-20- Examining Π equivalent circuit

$$\frac{V_2}{V_1} = \frac{R_2}{f(s)} \tag{4-55}$$

$$f(s) = C_1 C_2 R_1 R_2 L_l s^3 + (C_1 R_1 + C_2 R_2) L_l s^2 + (C_1 R_1 R_2 + C_2 R_1 R_2 + L_l) s + R_1 + R_2 \tag{4-56}$$

$$C_1 = C_{pi}, C_2 = C_{po}, L_l = L_{lp} \tag{4-57}$$

The f(s) parameters for the transformer are calculated according to (4-48)-(4-57), and are listed in Table 4-10. In this case study C_1 is much smaller than C_2; hence, the transfer function will be simplified as (4-58).

$$\frac{V_2}{V_1} = \frac{1}{s^2 + \left(\frac{R_1}{L_l} + \frac{1}{R_2 C_2}\right) s + \frac{1 + R_1}{L_l C_2}} \tag{4-58}$$

Table 4-10- Π Model Parameters for Fig. 4-2 Transformer

C_1	C_2	L_l	R_1	R_2	N_{ps}	N_{st}	N_{pt}
1.70pF	38.25pF	7.7μH	0.40Ω	366.3Ω	3.82	3.87	14.22

The resultant transfer function of (4-58) is a second order system with two dominant poles due to presence of L_l and C_2. R_1 and R_2 are two parameters that relate to the actual power converter. R_2 represents the active load of the system at each instance. R_1 is sum of the source resistance, the input cable resistance, the MOSFET channel resistances, and the winding resistance. R_2 corresponds to a 108W load that is reflected to the primary side. The time domain step response of the system is given in (4-59) and (4-60). These equations reveal qualities of the transformer's response such as rise time, overshoot and ringing. ζ is the damping factor of a second order system [191].

$$V_2(t) = \frac{1}{\omega_n^2}\left[1 - e^{-\zeta\omega_n t}\left(\cos\omega_d t + \frac{\zeta}{\sqrt{1-\zeta^2}}\sin\omega_d t\right)\right] \tag{4-59}$$

$$\omega_n = \sqrt{\frac{1+R_1}{L_l C_2}}, \zeta\omega_n = \frac{1}{2}\left(\frac{R_1 R_2 C_2 + L_l}{R_2 C_2 L_l}\right), \omega_d = \omega_n\sqrt{1-\zeta^2} \tag{4-60}$$

Table 4-10 parameters result in a damping factor of ζ=0.52. This predicts an under-damped response for this condition. When ζ=1, the system will be critically damped. If the transformer design can be modified, then C_2 needs to be 10.33 pF to achieve a critically damped response with R_2=366.3 Ω. Alternatively, a 189.6 Ω load (12.99 Ω at secondary) will result in a critically damped response, which translates to 208 W load. Such analyses are insightful from the system design perspective. A larger load, lower R_2 in the model, or a smaller parasitic capacitance, lower C_2 in the model, both will conclude lower ringing over the transformer response.

4.4.6. Model Verification

To verify the proposed transformer model, the model is implemented in SIMULINK environment as shown in Fig. 4-21. The signal generator provides a 40 kHz 150 V square wave that applies positive and negative steps to the transformer model. The resultant V_2 voltage is divided by N_{ps} relating to the experimental waveforms.

The proposed modeling method and simulation results are verified by the experimental setup that is shown in Fig. 4-22. V_1 is the output of the 40 kHz primary side inverter, and R_2 is a resistive load connected to the secondary winding. The inverter is controlled with the square wave modulation through a C2000 based DSP controller board.

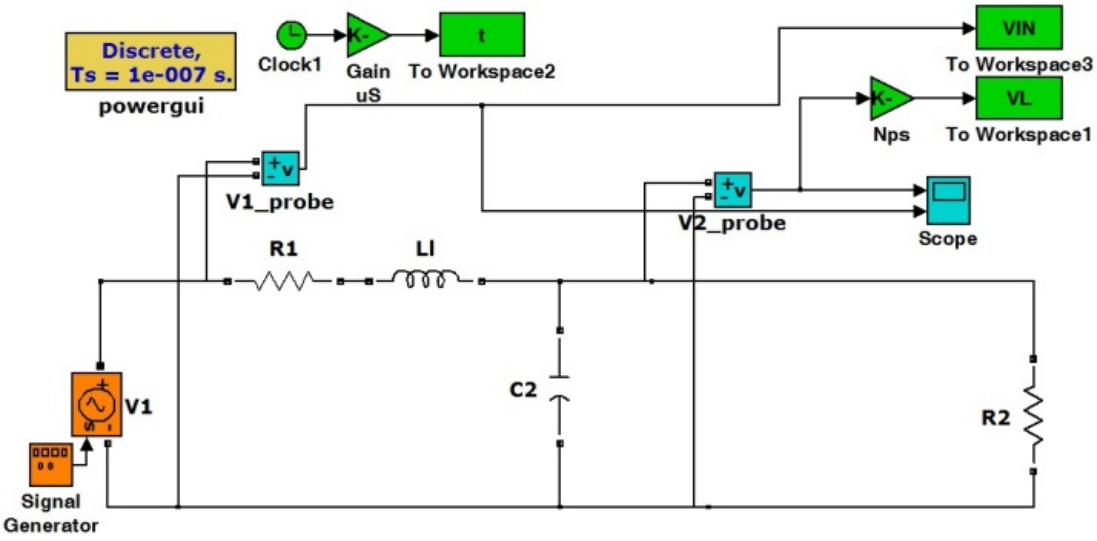

Fig. 4-21- Model of Fig. 4-20 in MATLAB SIMULINK

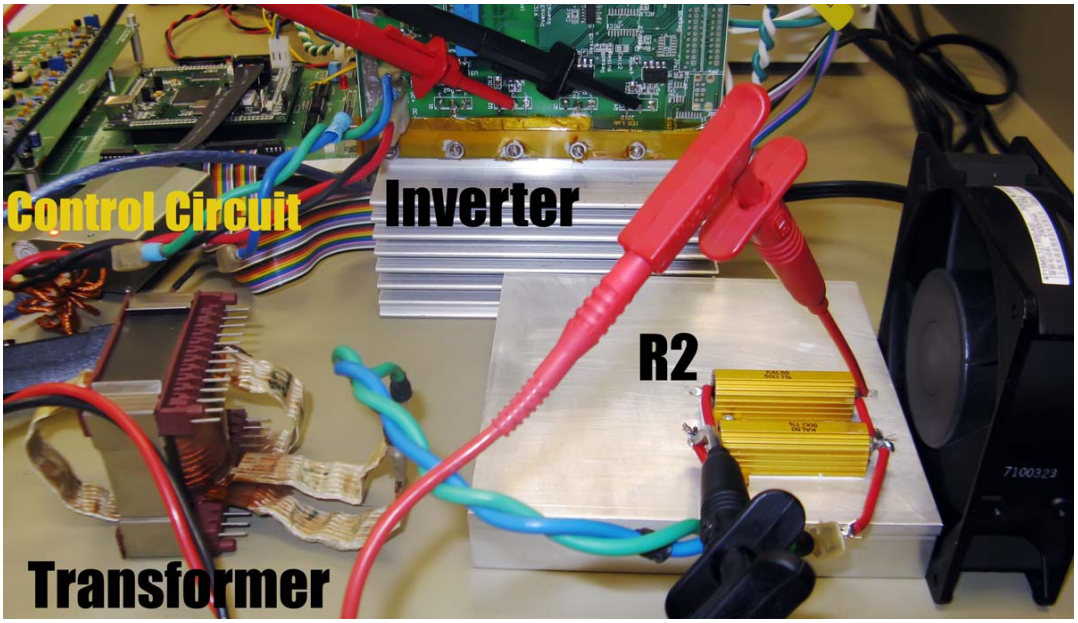

Fig. 4-22- Experimental Setup for Fig. 4-20 model

A 25.1 Ω load is connected to the secondary, which is equivalent to 366.3Ω at primary side. The simulation and the experiment agree as both of the step responses show an under-damped response with a low overshoot as illustrated in Fig. 4-23. Noticeably, this response completely agrees with the 0.52 damping factor that was calculated in the previous section. There is a difference between the sources used in the simulation and in the experiment. The inverter provides a smoother transient in comparison to the sharp ideal step function that applies to the model in the simulation study. Other than this difference, both the simplified model simulation result and the actual system in the experiment show an identical dynamic transient behavior.

The load resistor, which is connected to the secondary winding, is decreased to 5 Ω (72.96 Ω at primary). As this value is less than 12.99 Ω (189.6 Ω at primary), the mathematical analysis predicts an over-damped response for this case study. The power supply hits the current limit to supply this load at 150 V; thus, the V_1 amplitude is decreased to 120 V for this case study. The experimental result agrees with the simulation result as shown in Fig. 4-24. Both simulation and experimental results show over-damped responses that verify the validity of the proposed model. As can be seen, the actual transformer, the simplified model, and the mathematical analysis show similar behaviors with excellent accordance.

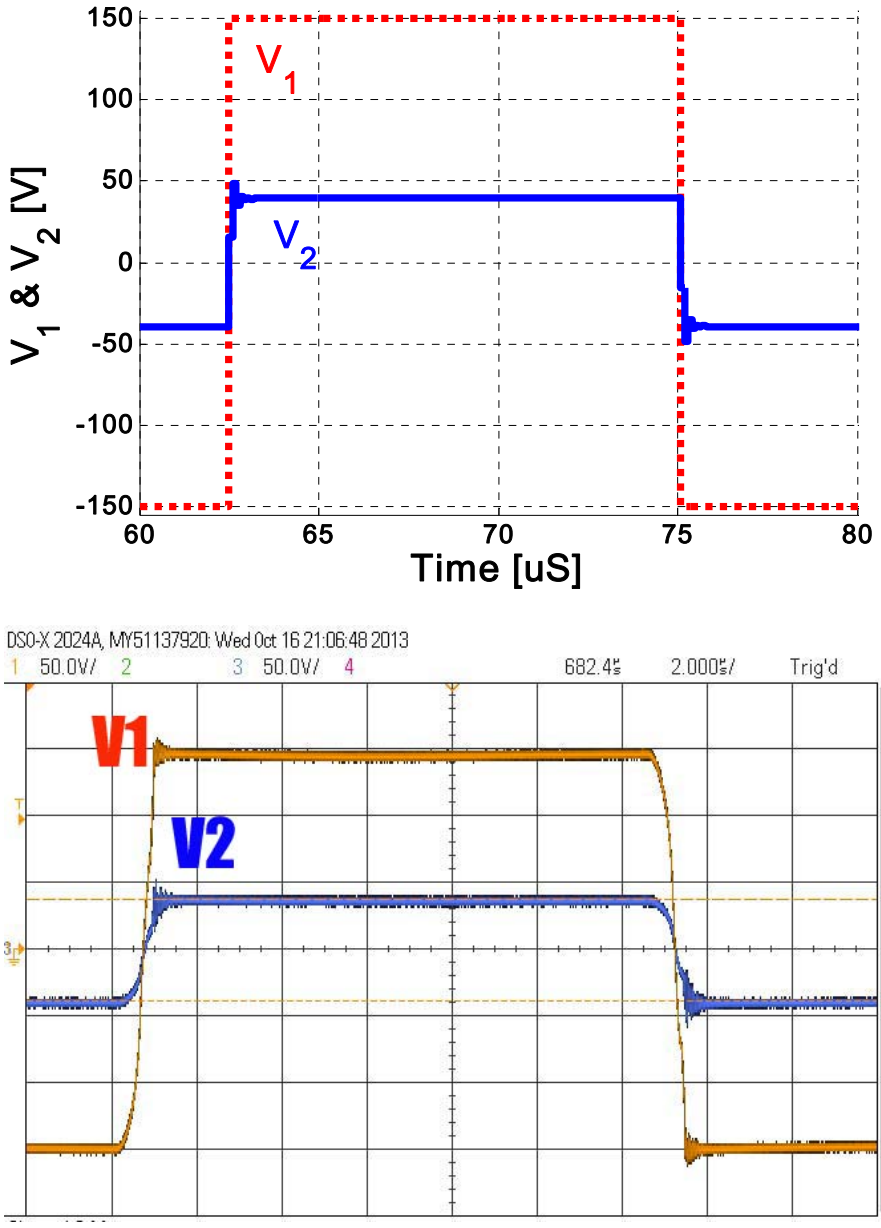

Fig. 4-23- Under-damped step response, Top: simulation, Bottom: experiment

V_1=150 V, 40 kHz, R_2=25 Ω @ secondary side, red: V_1, blue: V_2

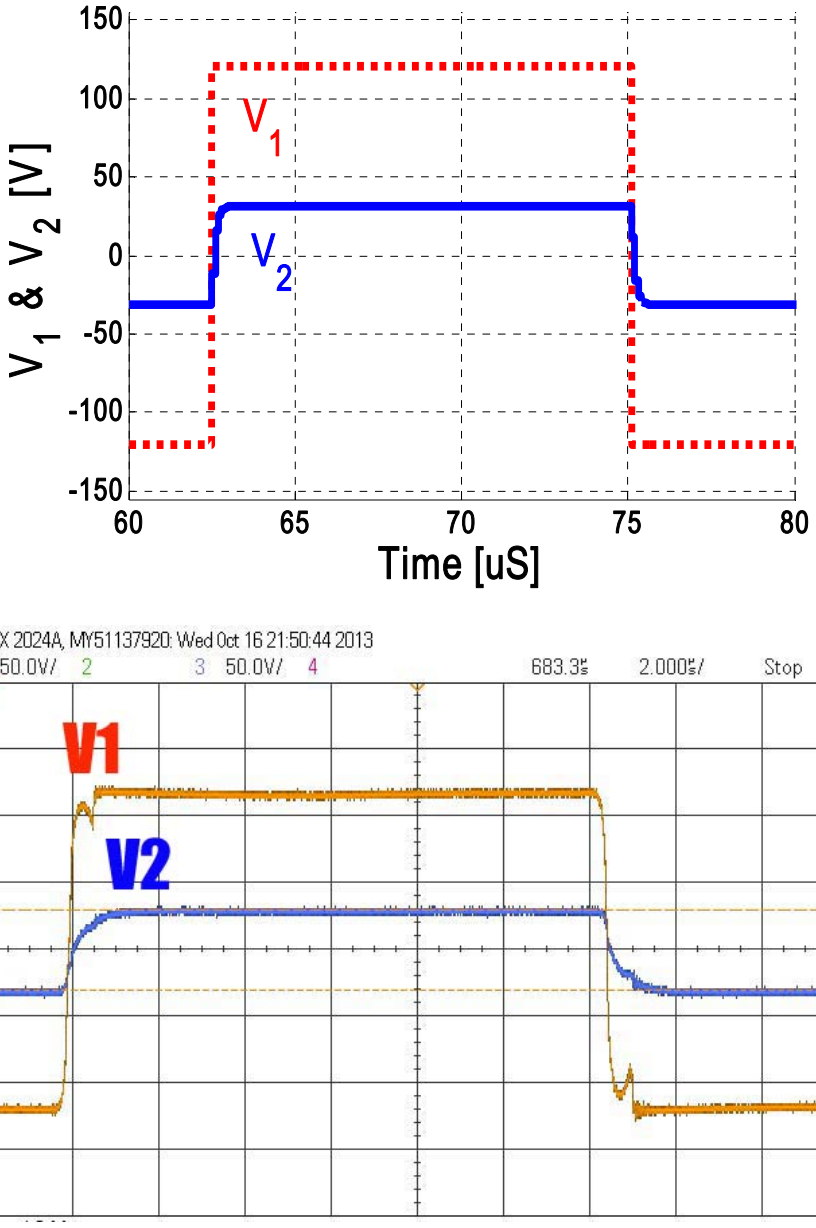

Fig. 4-24- Over-damped step response, Top: simulation, Bottom: experiment

V_1=120 V, 40 kHz, R_2=5 Ω @ Secondary side, Red: V_1, Blue: V_2

4.5. Conclusion

This chapter presented the proposed design procedures for the high frequency ac components of the VPC's magnetic circuit including the isolation transformer and the ac inductors. The three-winding isolation transformer were designed optimizing the area product method with help of spread sheet software. The experiments highlighted the effect of the transformer's parasitic capacitances in the VPC's performance.

Three design approaches were introduced for implementing the ac inductors. The gapped ac inductor and the novel coupled ac inductor design procedures were developed for the series high frequency ac link applications. The proposed coupled ac inductor integrates a zero blocking transformer into the coupled ac inductor design that can mitigate common mode interference in the VPC. The implemented prototypes were verified through the experimental setup.

An experimental modeling procedure was proposed in this chapter that incorporates capacitive elements of the multiport transformers, which are used in isolated dc-dc converters. The proposed electric model of the magnetic circuit introduces capacitive elements of the transformer into the model by measuring the short circuit resonance frequency of the transformer's windings. The winding capacitances are measured by the described modeling method. The mathematical procedure presented in this chapter simplifies the model into a third order Π equivalent circuit that is transferable to any desired winding side.

The three-winding transformer developed for the multiport VPC was investigated as a case study for the proposed modeling and analyzing method. The modeling

procedure further simplified the transformer's model into a second order model. The system step response was analyzed in the frequency domain and the time domain. According to the mathematical analysis, the transformer's step response has lower ringing and lower overshoot at higher loads and lower parasitic capacitances.

The accuracy of the mathematical analysis was verified through simulations and experiments observing the step response of the magnetic circuit connected to two different loads. The loads were selected to represent under-damped and over-damped operating points. The accordance of the results among the mathematical analysis, simulations, and experimental results verified the accuracy of the experimental modeling method as well as the mathematical analysis.

5. CONTROL SCHEMES

5.1. Overview

The VPC functions were introduced in the initial section of the introduction chapter, and a variety of VPC power converter topologies were evaluated in the same chapter. During the topology survey, the modulation methods were introduced. In this chapter, the proposed control solutions needed to perform the VPC functionalities will be presented.

Although the VPC power converter design is the main focus of this dissertation, the control routines are needed to evaluate the power converter for the vehicular application and developing the case studies. Thus, the control routines are adopted from the literature into this new application. This provides more contributions to the research developed in this dissertation. As an example, the case studies evaluating grounding schemes and fault scenarios in the second chapter all have been developed utilizing a simulation test bed that includes closed loop control routines and switching modulation. This chapter will describe the employed control routines and will explain the developed simulation test bed.

5.1.1. Embedded Digital Control for VPC

The control routines developed for this dissertation are implemented in a digital embedded DSP controller [109, 129, 192]. F2812, a Ti C2000 DSP controller, is used on the experimental setup. The C2000 DSP controllers are developed for the power electronics and electric drives applications. They include a fixed point or a floating point

digital signal processor and a few peripherals. The processor core is optimized for mathematical operations that are used in the control routines. The peripherals are different hardware modules needed for embedded digital control. To name a few, the ADC module is used for sampling and the PWM module enhances modulation of the switches.

The main advantage of an embedded solution is the flexibility. The control circuitry is easily modified by programming the software as the control solutions are developed. The included peripherals offer a system on a chip solution and reduce the component count. A powerful DSP controller can handle a few control tasks; indeed, all the control routines can be implemented in a central embedded controller. Moreover, the switches modulation, the communications, the user interface, and the soft protections can be implemented into the central embedded controller.

The control routines are intended for the topology displayed in Fig. 5-1. This is a decoupled three-stage isolated VPC. Thanks to presence of the dc link, the control routines of the dc side can be decoupled from the ac side's control.

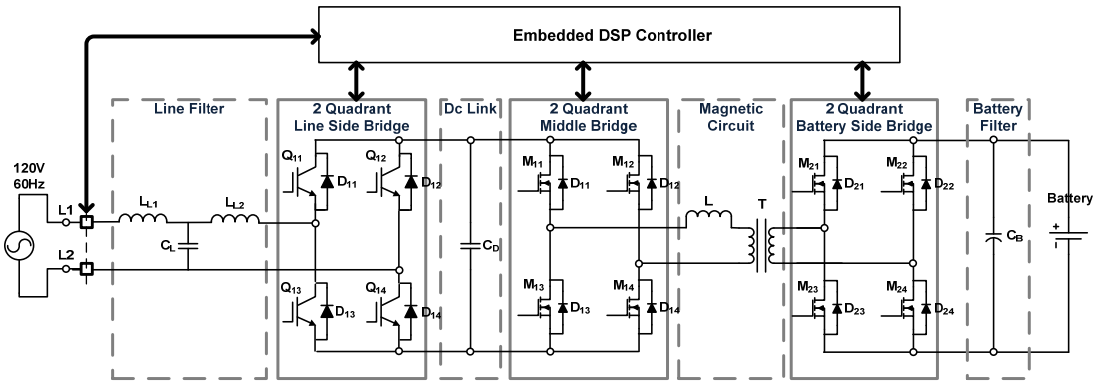

Fig. 5-1- Embedded DSP controller for single phase three-stage isolated VPC

5.1.2. Ac Current Tracking Control Routines

The two-quadrant line side bridge operates as a synchronous rectifier and charges the dc link during the charge mode. In the V2G mode, the line side bridge acts as a grid connected inverter. In both cases, the power factor can be controlled and the current controller has to follow a sinusoidal reference; thus, the basic PI controller will have a steady state error [193, 194]. The sinusoidal waveforms transform to dc waveforms in the dq domain. Control of synchronous rectifier is possible with two PI controllers in the dq domain [195, 196]. If the PI controllers be transformed back from the dq domain, a second order controller is derived in the abc domain that is called a Proportional Resonant (PR) controller [196-199]. In fact, according to the linear control theory a sinusoidal tracker has to be a second order controller. The selective harmonic compensation can be added to PR controller to enhance the current control loop [200-202]. Alternative current control methods use digital hysteresis [203, 204], dead-beat control [129, 205, 206], model predictive control [207, 208], and space vector modulation [32]. This dissertation does not intend to investigate all the mentioned control routines. The dead-beat controller as a fast and simple solution will be adopted for the VPC.

5.1.3. Dc-Dc Converter Controller

The batteries are dc sources and a discrete PI controller can regulate the desired voltage or current [209, 210]. If the required dynamic of dc side is much slower than the time constants of the dc-dc converter, a feed forward control of the converter using phase shift can be implemented.

5.1.4. Dc Link Controller

Regulating dc link synchronizes the power flow between the dc-dc converter and the line side bridge. A slow PI controller with a low pass filter is adopted as the dc link controller as described in [129, 206, 211]. The details will be presented in the next section.

5.2. Charger Control

In this section, the VPC control solution for charging mode is explained. The control routines are implemented and verified in SIMULINK environment. Firstly, the simulation model will be presented in the next subsection.

5.2.1. Simulation Model in Charge Mode

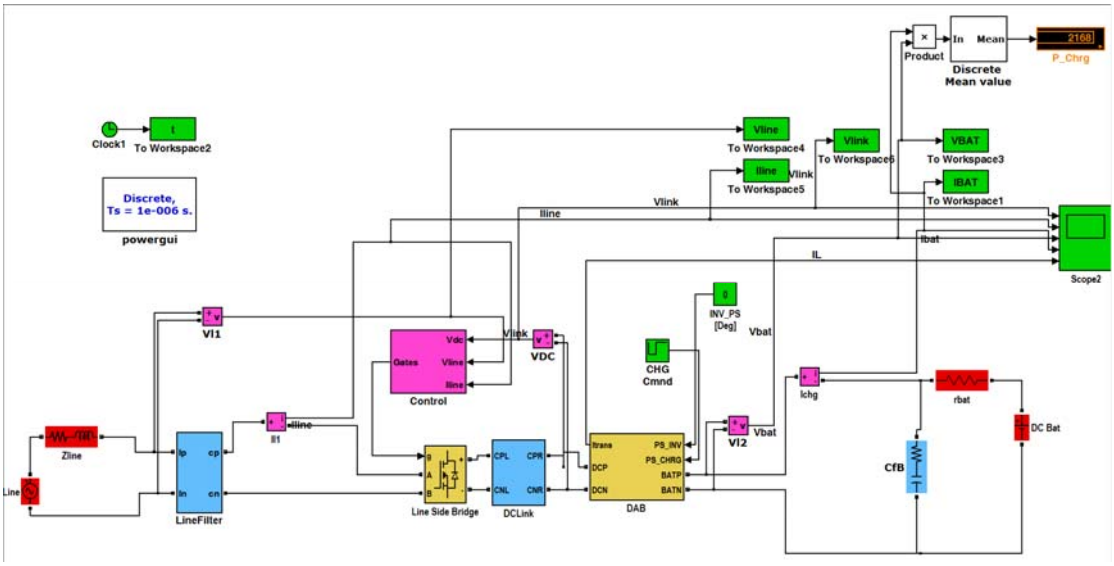

Fig. 5-2- Simulation test bed during charge mode

The SIMULINK model of the charger is shown in Fig. 5-2. The grid is modeled with 60 Hz ac source and connection impedance. Converter blocks are yellow, passive elements are blue, control and measurement blocks are magenta, sources are red and interfacing blocks are green in the simulation model. Interfacing blocks include parameters that the user sets during case studies and monitoring blocks. Monitoring blocks include scopes and data interface blocks to the MATLAB workspace.

The line side bridge is modeled with the two leg bridge model. The switch parameters are $R_{ds(on)}$ and switch output capacitor that have been set according to the switches listed in Table 3-2. The passive elements were designed in the section 3.5.

5.2.2. Line Side Bridge Control

The line side bridge becomes a boost active Power Factor Correction (PFC) rectifier in the adopted control scheme. The lower switches short the line in boosting intervals. All the switches are open on other intervals [212]. The controller block diagram is shown in Fig. 5-3. Fig. 5-4 shows the SIMULINK implementation of this block. The outer loop is relatively slow and regulates the dc link voltage, the inner loop control the current in phase with the line voltage.

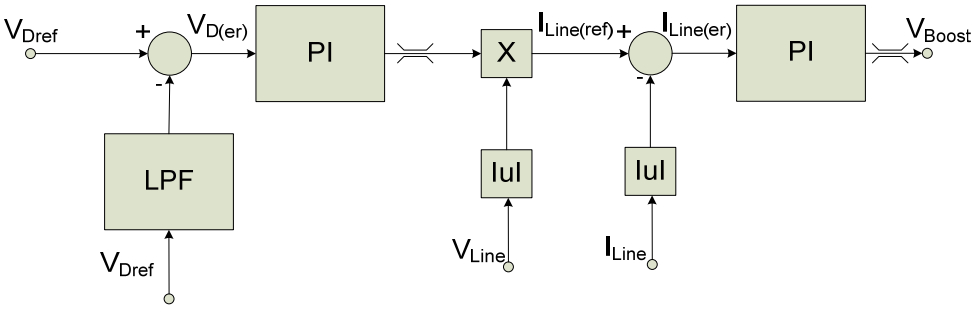

Fig. 5-3- Line side bridge controller for charging mode

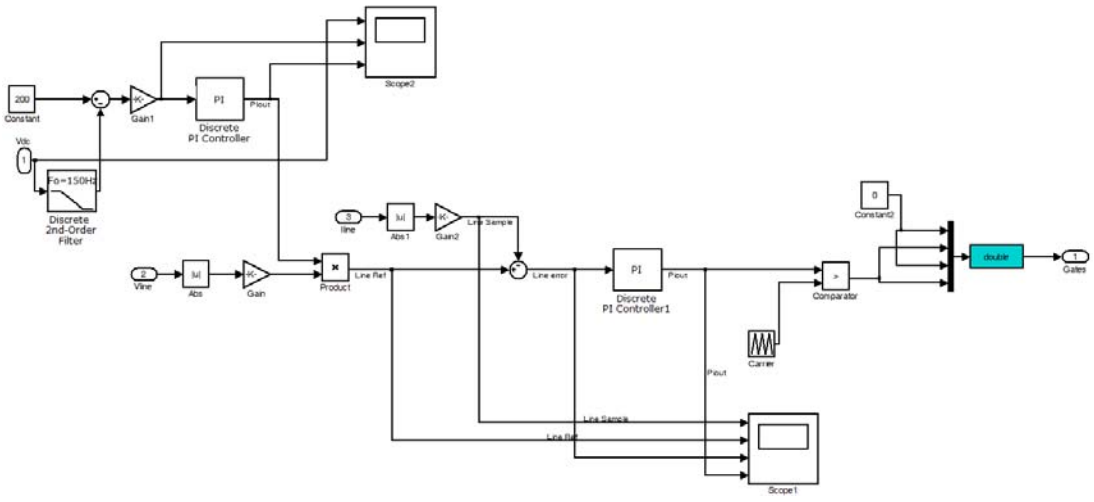

Fig. 5-4- Line side bridge controller for charging mode in SIMULINK

The analogue PI controller is (5-1) and the discrete form is (5-2). In the discrete form, the sampling time of T_s is a part of integral gain. The sampling time is usually greater or equal to the switching period of T_{sw}.

$$G_{PI}(s) = k_P + \frac{k_I}{s} \tag{5-1}$$

$$G_{PI}(z) = k_P + k_I T_s \frac{z}{z-1} \tag{5-2}$$

The integral gain is selected according to (5-3). It controls the dc link average over n line cycles. In the case studies n will be set at 5.

$$\begin{cases} k_I = 2\pi n f_{line} \\ k_p = 8 \end{cases} \tag{5-3}$$

One implementation of the digital PI controller loop is [210]:

$$\begin{cases} m_I(k) = k_I T_s e(k) + m_I(k-1) \\ m(k) = k_p e_I(k) + m_I(k) \end{cases} \tag{5-4}$$

The current controller is designed as follows [210]:

$$k_p = \frac{M_{\max}}{2V_d}\frac{R_{Lac}}{G_I}\sqrt{1+\left(\omega_{CL}\frac{L_{ac}}{R_{ac}}\right)} \tag{5-5}$$

$$k_I = \frac{\omega_{CL}k_P}{tg\left[-90^o + PM + 2tg^{-1}\left(\omega_{CL}\frac{T_s}{4}\right) + tg^{-1}\left(\omega_{CL}\frac{L_{ac}}{R_{ac}}\right)\right]} \tag{5-6}$$

In (5-5) and (5-6), M_{max} is the maximum amplitude of the modulator (such as 3.3 V or 5 V), L_{ac} is the line filter and R_{ac} is the resistor in series with L_{ac}, ω_{CL} is the closed loop bandwidth, and PM is the phase margin, which is selected more than 60^o.

5.2.3. Simulation Case Studies for Charging

The performance of the employed charge controller is verified through simulations.

5.2.3.1. Charging at Nominal Power

In the first case study, the charger starts and regulates the dc link at 200 V. The DAB is set at 36^o phase shift to charge the battery at nominal power. The case studies show this control method needs smaller line filter inductance than what is calculated in 3.5.1 subsection. This is due to the difference in the modulation method and the presence of closed loop controller. The line filter is designed at 1 mH (L_{ac}=1mH). The dc link voltage, the input current, and input voltage waveforms are shown in Fig. 5-5. The current THD is 3.99% which is below the allowed THD of 10% for chargers. The charge current THD is calculated using SIMULINK Power GUI as shown in Fig. 5-6.

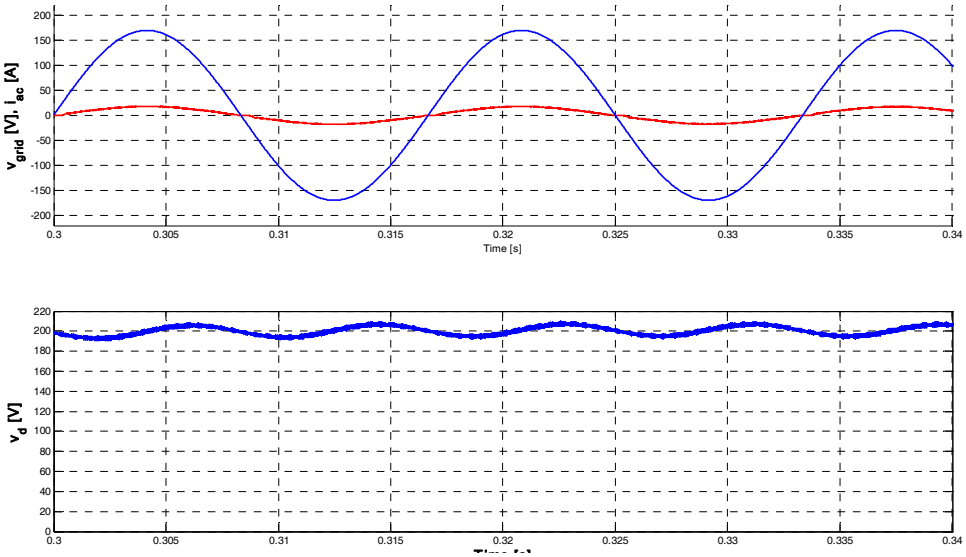

Fig. 5-5- Charger controller, nominal condition

Top: blue: line voltage, v_{grid}, red: input current, i_{ac} Bottom: dc link voltage, v_d

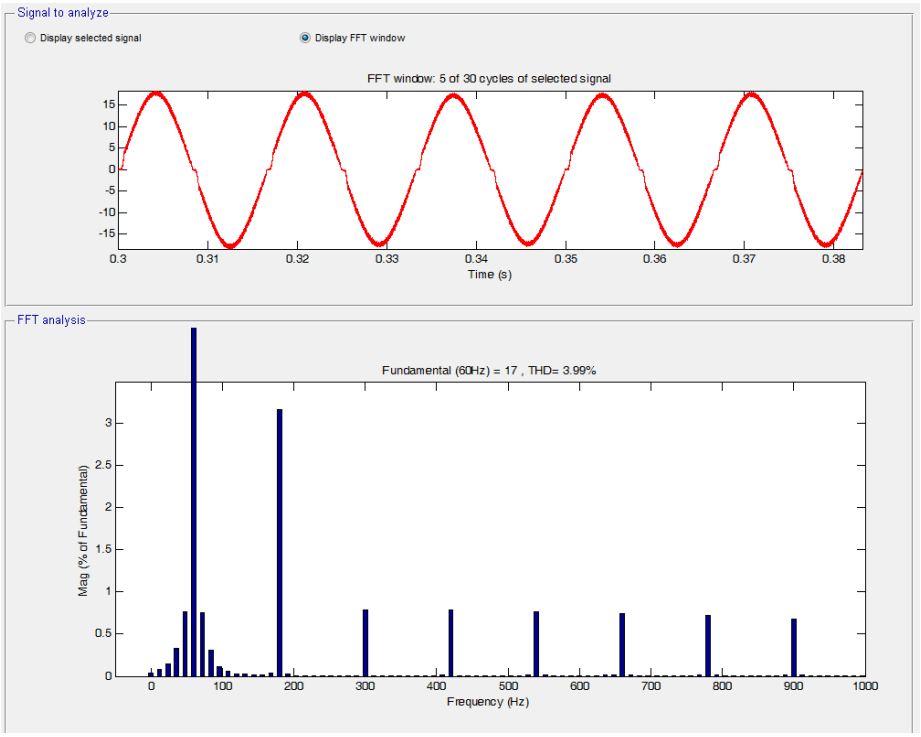

Fig. 5-6- Input line current THD during charge mode, nominal condition

5.2.3.2. Charging at 50% of Nominal Power

In the second test study the battery is charged at 50% of nominal power. The DAB phase shift is set at 15°. The waveforms are shown in Fig. 5-7 and Fig. 5-8 similar to the previous case study. The charger drains 6.9 A rms current with THD of 3.82%.

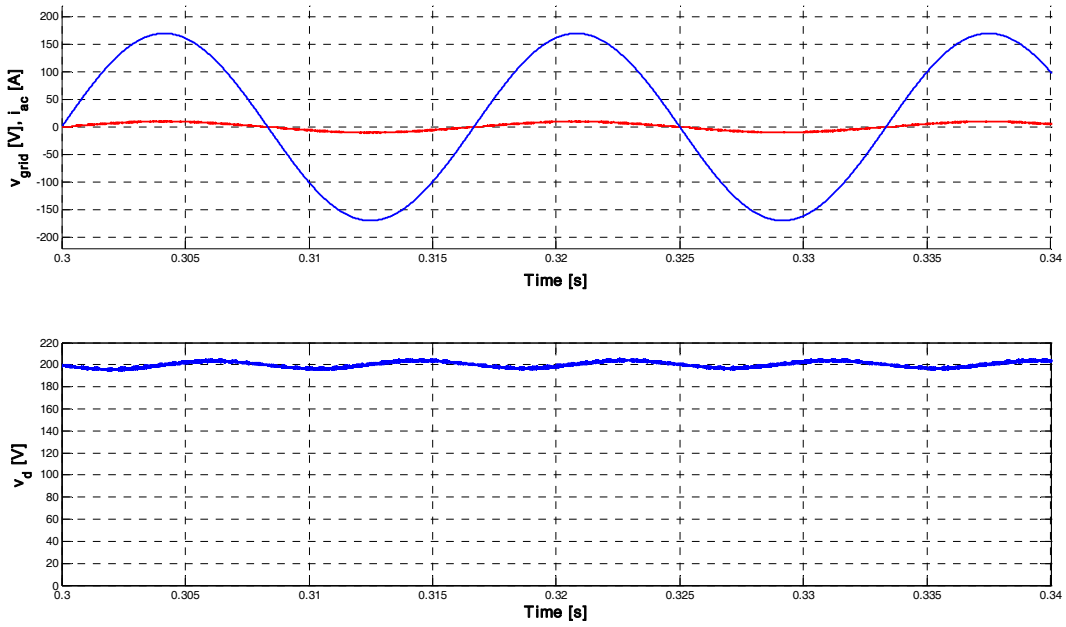

Fig. 5-7- Charging at 50% power

Top: blue: line voltage, v_{grid}, red: input current, i_{ac} Bottom: dc link voltage, v_d

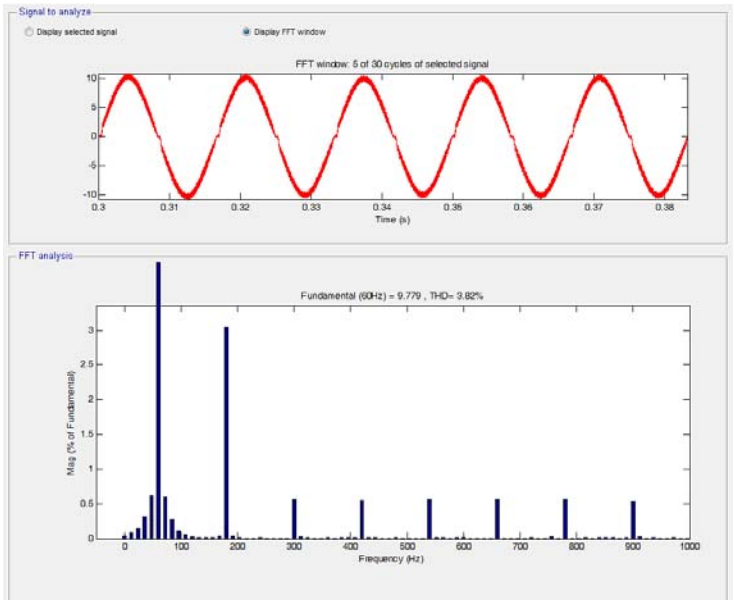

Fig. 5-8- Line current THD, charging at 50% power

5.2.3.3. Dc link Regulator Response versus Charger Step Change

In this case study, the behavior of dc link regulator is investigated versus a disturbance in the battery charger command. The DAB phase shift is initially set at 15^{o}. The phase shift is changed to 25^{o} at 0.2 s. The charger's line current increases from 7.39 A to 11.47 A. The dc link shows about 12 V (6%) deep and returns to the regulated value after about 5 line cycles (0.083 s). The waveforms are shown in Fig. 5-9. The dc link regulator was intentionally designed for a similar time constant according to (5-3). Hence, this behavior is expected from the design perspective.

The performance of charger controller and the dc link regulator has been verified through simulation case studies in this section. The dc link regulator will be replaced with an equivalent source for the case studies performed in the next section. The next section is dedicated to the V2G controller.

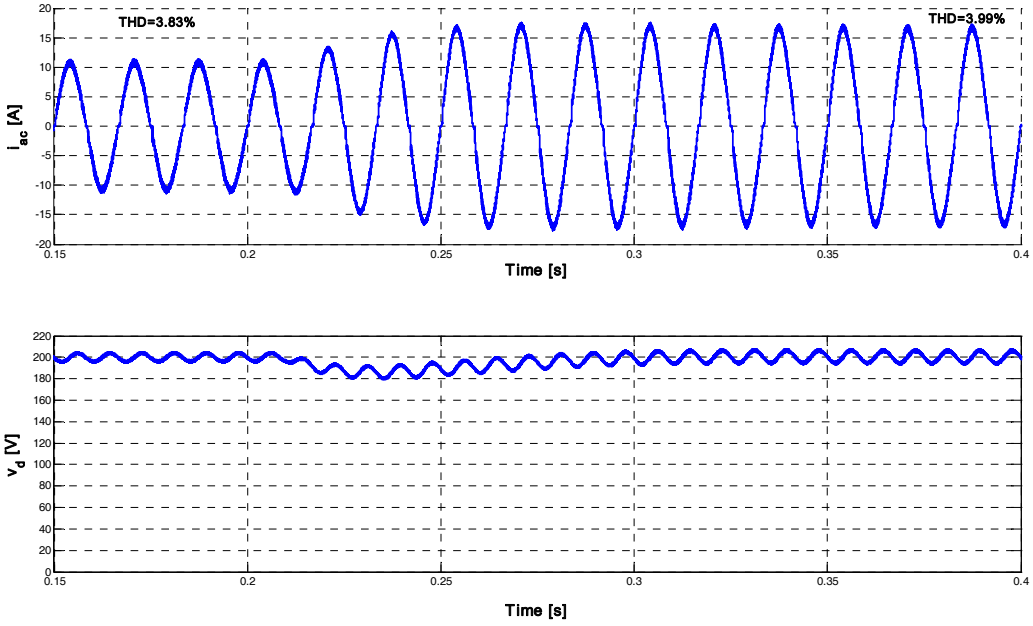

Fig. 5-9- Dc link regulator performance versus charger step change

i_{ac} : VPC input current, v_d : dc link voltage

5.3. V2G Control

During the V2G mode, the line side bridge injects current to the grid. The dc-dc converter regulates the dc link. The equivalent circuit of the line side bridge during injecting power to the grid is shown in Fig. 5-10. The inverter voltage v_{inv} relates to the injected current i, the measured line voltage v_{grid}, and the impedance between the voltage sources according to (5-7). The discrete form of this equation is (5-8). The impedance between line and grid are including the inverter filter and the line connection impedance.

The line voltage is measured at the inverter terminal. The major component of the series impedance between the measured line impedance and the inverter is L_{ac} as R_{ac}

is small and negligible in the power transfer equation. In (5-8), R_{ac} is neglected and $\overline{v}_{grid}$ and $\overline{v}_{inv}$ are the local average of the line and the inverter voltages. The voltage values are dependent on the present sample (n) to generate the next instant current sample [n+1].

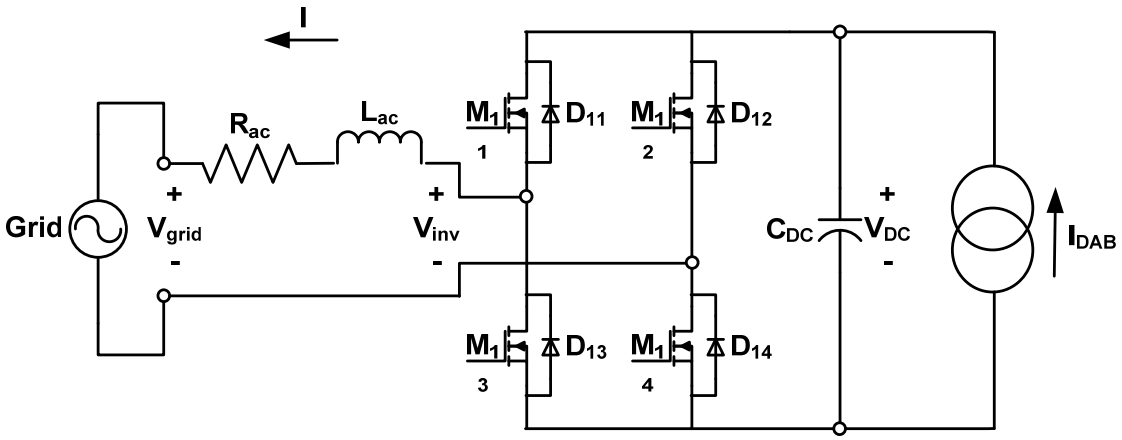

Fig. 5-10- Equivalent circuit during V2G mode

$$v_{inv} - v_{grid} = L_{ac}\frac{di}{dt} + R_{ac}i \tag{5-7}$$

$$\overline{V}_{inv}[n] - \overline{V}_{grid}[n] = \frac{L_{ac}}{T_{SW}}\left(i[n+1] - i[n]\right) \tag{5-8}$$

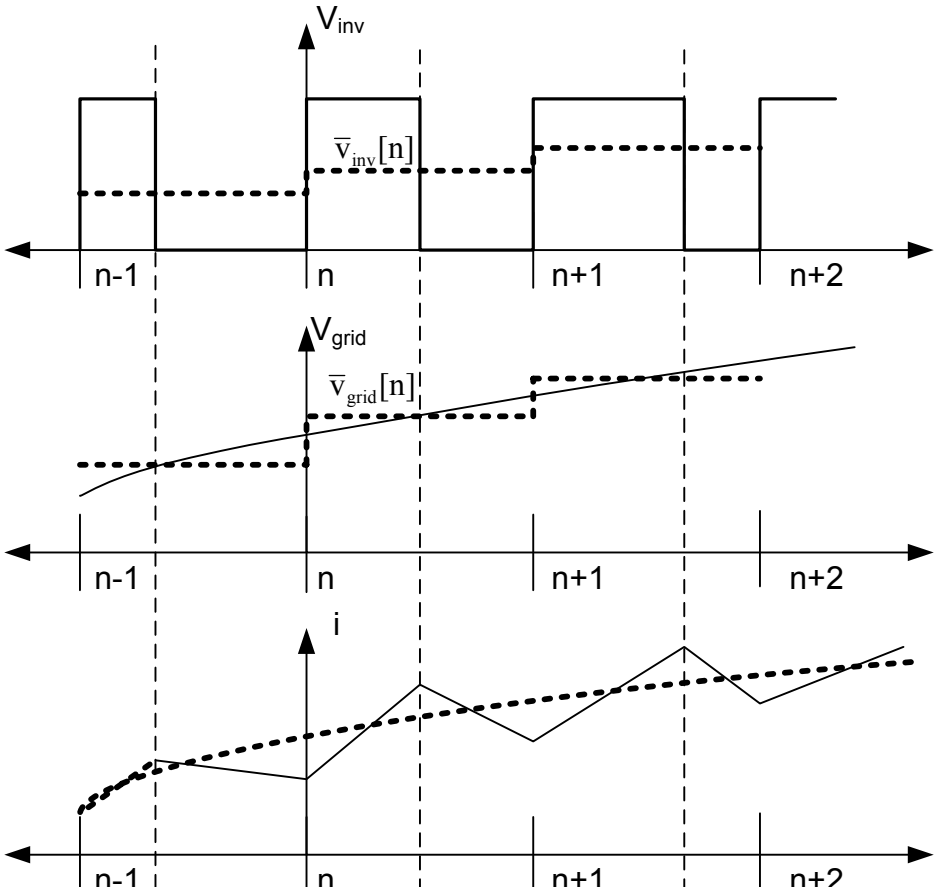

Fig. 5-11- Inverter voltage, measured line voltage, and injected current in three consecutive cycles

dotted lines: local average waveforms, solid lines: instantaneous waveforms

5.3.1. Dead-Beat Controller Application for VPC

The dead-beat controller is adopted for the V2G operation. This control method was successfully practiced by the author for the photovoltaic application [129]. In this section, the application of the control method for VPC is practiced. The dead-beat controller intends to calculate the voltage of the next cycle ($\bar{v}_{inv}[n+1]$) in a way the current at the end of that cycle ($i[n+2]$) reaches the reference:

$$i[n+2] = i_{ref}[n+2] \tag{5-9}$$

Therefore, the inverter voltage will be as (5-10):

$$\overline{V}_{inv}[n+1] - \overline{V}_{grid}[n+1] = \frac{L_{ac}}{T_{SW}}\left(i_{ref}[n+2] - i[n+1]\right) \tag{5-10}$$

In (5-10), $i[n+1]$ and $\overline{V}_{grid}[n+1]$ cannot be measured in the current cycle and need to be calculated:

$$\overline{V}_{grid}[n+1] = \overline{V}_{grid}[n] + \Delta\overline{V}_{grid} \tag{5-11}$$

$$\overline{V}_{grid}[n] = \overline{V}_{grid}[n-1] + \Delta\overline{V}_{grid} = \frac{3}{2}v_{grid}[n] - \frac{1}{2}v_{grid}[n-1] \tag{5-12}$$

$$\overline{V}_{grid}[n+1] = \overline{V}_{grid}[n-1] + 2\Delta\overline{V}_{grid} = \frac{5}{2}v_{grid}[n] - \frac{3}{2}v_{grid}[n-1] \tag{5-13}$$

From (5-8) and (5-10) by considering (5-12) and (5-13), the deadbeat current controller equation is calculated as (5-14):

$$\overline{V}_{inv}[n+1] = \frac{5}{2}v_{grid}[n] - \frac{3}{2}v_{grid}[n-1] + \frac{L_{ac}}{T_{SW}}(i_{ref}[n+2] - 2i[n] + i[n-1]) \tag{5-14}$$

The next cycle's duty cycle is resulted by dividing $\overline{V}_{inv}[n+1]$ by the dc link voltage during the next cycle. The dc link in the next cycle may be estimated from (5-15) for three phase systems or the systems that have lower dc link ripple. For single phase systems, (5-16) may be used. Alternatively, this value may be calculated from the dc link control routine. If the current control routine is much faster than the double frequency ripple, (5-15) is also valid for single phase systems.

$$\overline{V}_{dc}[n+1] \approx V_{dc}[n] \tag{5-15}$$

$$\overline{V}_{dc}[n+1] = \frac{5}{2}V_{dc}[n] - \frac{3}{2}V_{dc}[n-1] \tag{5-16}$$

The current reference is related to the VPC power according to (5-17). In (5-17), m is the sampling cycle according to the grid frequency. In other words, the current reference will be updated within every line cycle.

$$I_{ref}[m] = \frac{\sqrt{2}\left|\overline{P}_{VPCU}[m]\right|}{V_{rms}[m]} \tag{5-17}$$

Calculating the current reference for the switching cycles, the $i_{ref}[n+2]$ can be calculated as follows:

$$I_{ref}[n+2] = I_{ref}\frac{Sin(n+2)f_{ac}}{f_{sw}} \times 2\pi, N_S = \frac{f_{sw}}{f_{ac}} \Rightarrow I_{ref}[n+2] = I_{ref}Sin(\frac{2\pi n}{N_S} + \frac{4\pi}{N_S}) \tag{5-18}$$

In (5-18), n is the sampling instances by switching period of T_{sw} and varies from 1 to N_S.

5.3.2. Simulation Case Studies for V2G Operation

The simulation test bed of Fig. 5-2 is updated with dead-beat control module which was described in the previous subsection. The dead-beat controller's implementation in SIMULINK is shown in Fig. 5-12. The case studies will be presented in the following subsections.

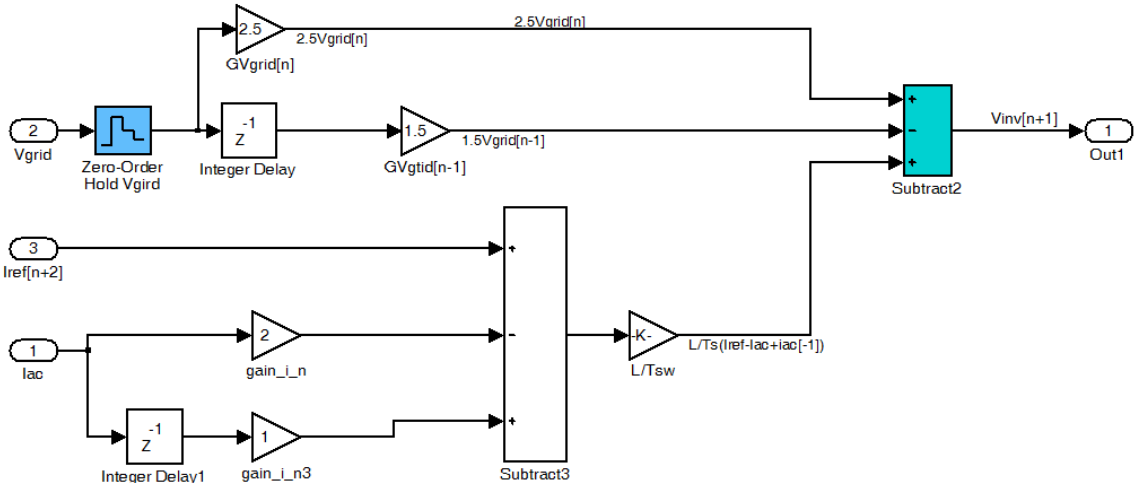

Fig. 5-12- Deadbeat controller implementation in SIMULINK

5.3.2.1. V2G Operation at Nominal Power

The nominal ratings are used for verifying the operation of converter at the maximum power. The simulation parameters are summarized in Table 5-1. The key waveforms to investigate the performance of the line side bridge are the line voltage V_{grid}, the injected current I_{ac} and the dc link voltage V_d. These waveforms are shown in Fig. 5-13. As can be seen the VPC perfectly injects power to the grid with low THD and unity power factor. The line current THD is analyzed in Fig. 5-14. THD is measured as 1.88%, which is well below the desired ratings.

The current controller's details are investigated in Fig. 5-15. This figure includes output current waveform, reference current ($i_{ref}[n+2]$), dc link voltage, inverter input current $i_{inv(in)}$, inverter switching voltage V_{inv}, and amplitude modulation index (m_a) waveforms during one line cycle. Fig. 5-15 shows how the controller tracks the current reference.

Table 5-1- Simulation Parameters for Nominal Power Operation

P_{out} [kW]	I_{ac} [A]	V_{grid} [V]	V_d [V]	L_{ac} [mH]	f_{sw} [kHz]
1.599	13.32	120	200±10	10	20

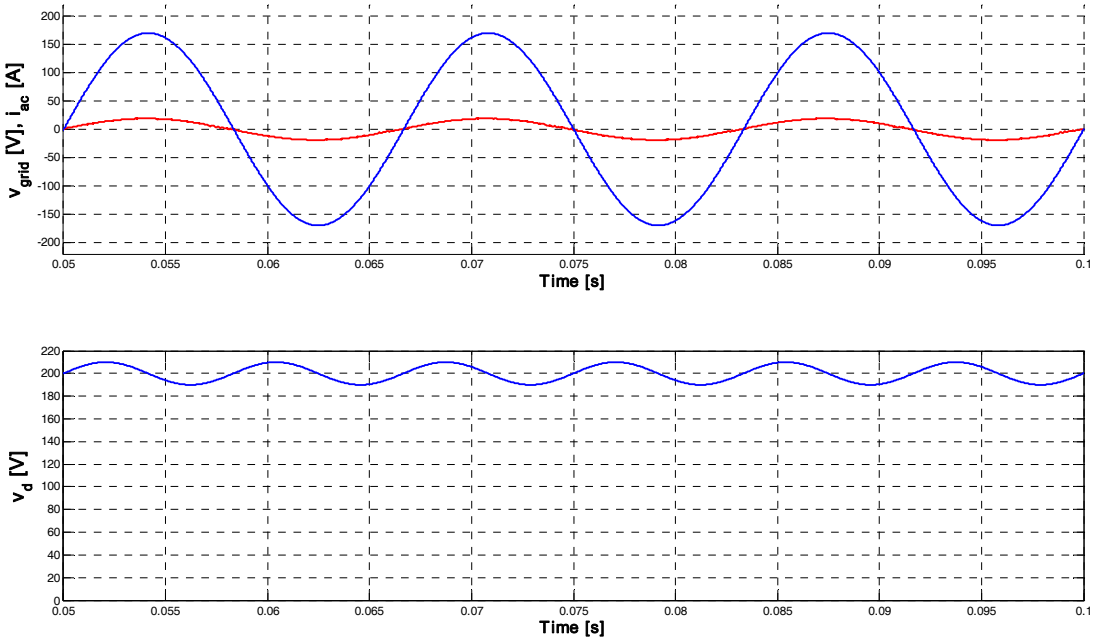

Fig. 5-13- V2G simulation at nominal power

Top: blue: line voltage, v_{grid}, red: output current, i_{ac}, Bottom: dc link voltage, v_d

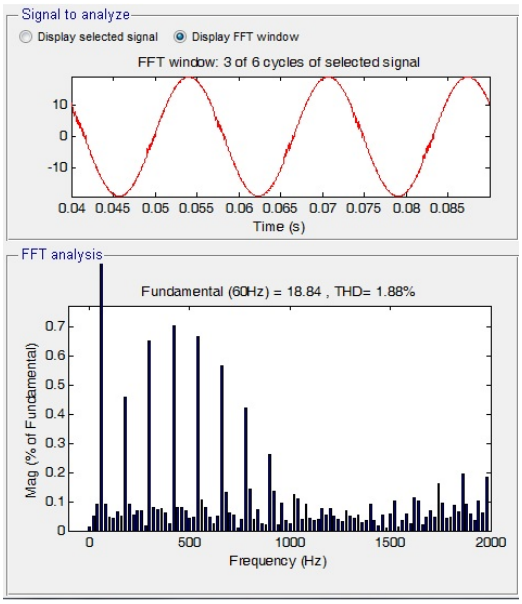

Fig. 5-14- Injected current THD at nominal V2G operation

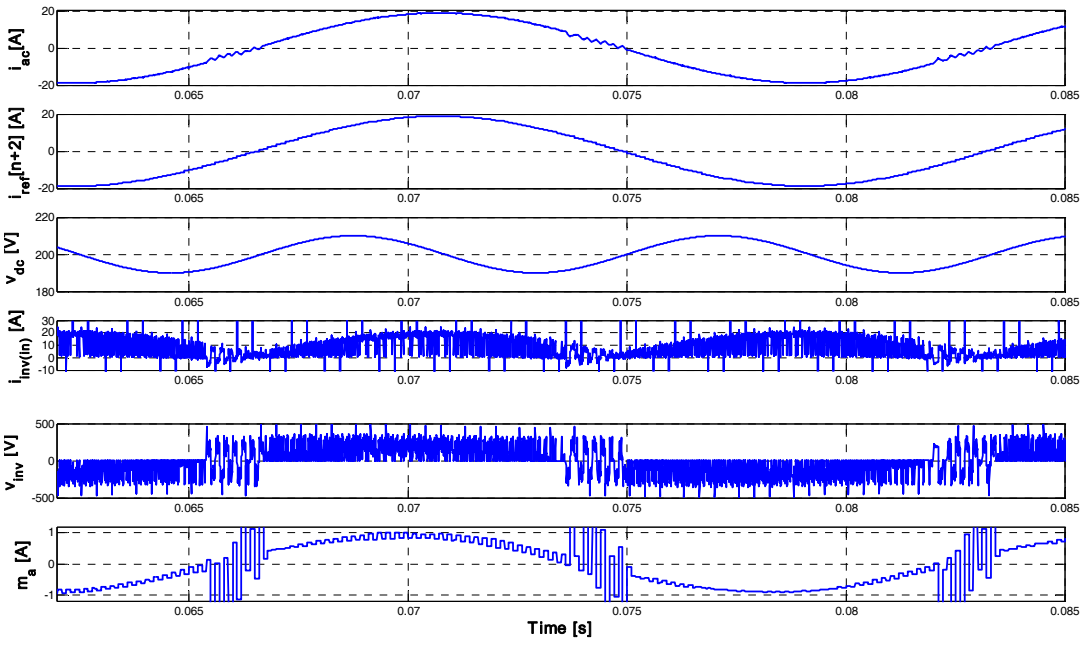

Fig. 5-15- Controller performance during nominal operation

i_{ac}: injected current, $i_{ref}[n+2]$: current reference, v_d: the dc link voltage ripple, $i_{inv(in)}$: inverter input current, v_{inv} inverter switching voltage, m_a: amplitude modulation index

5.3.2.2. Investigating L_{ac} Variations

Line inductance variations are investigated from two different points of view, the design perspective and the operation perspective. From the design perspective, it is preferred to employ a smaller line filter to reduce the cost and improve the converter dynamics. As shown in the previous section, THD is well below the required value and the line inductance can be further reduced. From the operation perspective, controller performance versus unforeseen variations of L_{ac} is important. The inductances can be different from the designed value due to the manufacturing tolerances and operating conditions. The distributed air gap cores that are usually utilized for 60 Hz filters show a variable permeability according to the operating point variations.

Firstly, the current THD is investigated when the inductor current is reduced from the design perspective. In this investigation, the controller parameters are varied in respect to the line inductance. The output current THD is listed in Table 5-2. All the other simulation parameters are same as Table 5-1 and only L has been changed. As can be seen, THD remains within desired limit when the inductance is 50% of the initial designed value. The initial design that was performed at 3.5.1.1 was based on an open loop steady state operation. In contrast, the closed loop control contributes in improving the current THD in this study. Fig. 5-16 shows the operation of VPC with a 5 mH inductance and Fig. 5-17 shows the calculated THD.

Table 5-2- Varying L_{ac}, Design Perspective

L_{ac} [mH]	10	7.5	5	2.5	1
THD [%]	1.88	2.49	3.19	6.6	19.9

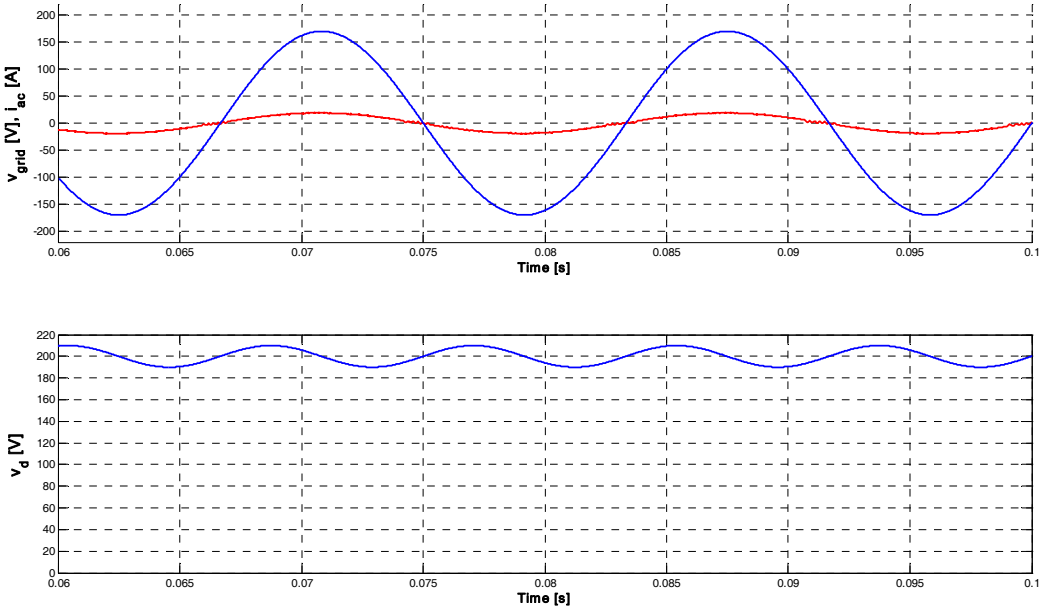

Fig. 5-16- V2G simulation at nominal power, L_{ac} = 5 mH

Top: blue: line voltage, v_{grid}, red: output current, i_{ac} Bottom: dc link voltage, v_d

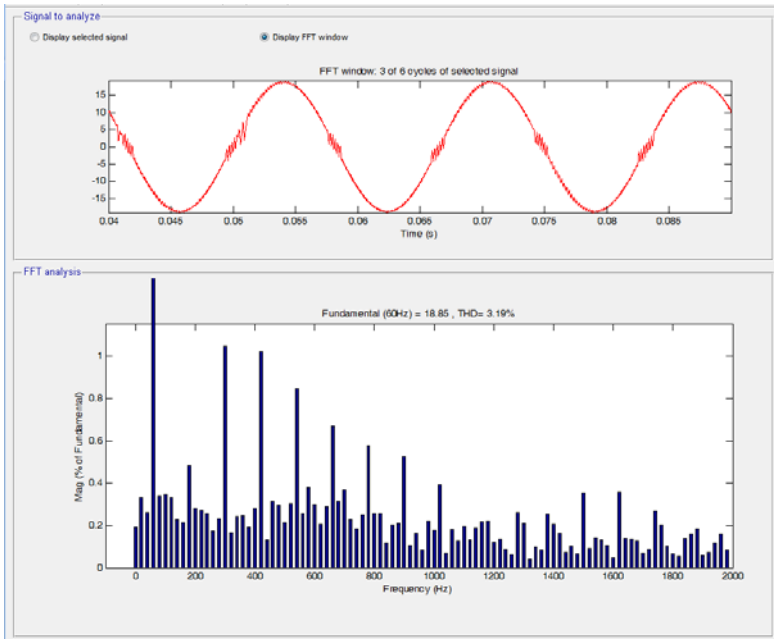

Fig. 5-17- Output current THD at nominal V2G operation, L = 5 mH

In this set of experiments, the control routine's sensitivity to the inductance parameter is examined. In Table 5-3, the inductance value at the controller is set at the designed value of L_{ac} and the actual inductance in the simulation test bed is varied form half of the designed value to twice of the designed value. The case studies are repeated for 5 mH and 10 mH designs. In each case study, THD is measured and listed in Table 5-3. The case studies show the controller remains effective versus larger inductances. In contrast, the controller is very sensitive to the inductances smaller than the set value. This investigation suggests a design trend that is setting the L_{ac} parameter in the controller with a value smaller than the physical inductance. This idea is investigated in a set of case studies summarized in Table 5-4.

Table 5-3- Investigating Controller Performance versus Inductance Tolerances

	$0.5L_{ac}$	$0.75\ L_{ac}$	$0.9L_{ac}$	L_{ac}	$1.1L_{ac}$	$1.25L_{ac}$	$1.5L_{ac}$	$2L_{ac}$
L_{ac}[mH]	2.5	3.75	4.5	5	5.5	6.25	7.5	10
THD[%]	17.46	9.91	7.55	3.19	2.19	1.92	1.93	1.57
L_{ac}[mH]	5	7.5	9	10	11	12.5	15	20
THD[%]	10.10	5.11	3.17	1.88	1.29	1.23	1.02	2.61

The idea behind the case studies listed in Table 5-4 is to tune the L_{ac} parameter in the deadbeat current controller of (5-14) with a value smaller than the physical inductance. L_{cnt} is defined in order to contrast between the controller's parameter and the physical line inductance value. In other words, L_{cnt} is the value set in the controller; L_{ac} is the inductance set in the simulation circuit to filter the inverter current. This nomination is followed in Table 5-4.

The case studies listed in Table 5-4 show tuning L_{cnt} to a smaller value than L_{ac} improves the current controller's performance. Additionally, this modification improves the sensitivity of the controller to the L_{ac} tolerances. According to these case studies, L_{cnt} around 1 mH is close to an optimum value for L_{ac} of 5 mH. This preliminary case study suggests adjusting L_{ac} by 20% in the controller as formulated in (5-19)-(5-21). The same case study suggests moving to a further smaller inductance for the line filter. This design procedure needs to be engaged with an optimization process and verified by experimental results in the future works.

$$\overline{V}_{inv}[n+1] = \frac{5}{2} v_{grid}[n] - \frac{3}{2} v_{grid}[n-1] + \frac{L_{cnt}}{T_{SW}} (i_{ref}[n+2] - 2i[n] + i[n-1]) \tag{5-19}$$

$$L_{cnt} < L_{ac} \tag{5-20}$$

$$L_{cnt} \approx \frac{1}{5} L_{ac} \tag{5-21}$$

Inspiring from the case studies of Table 5-3 and Table 5-4, the L_{ac} is further reduced to 1 mH. The controller value of L_{cnt} is set to 200 µH. This inductance value is a good design if THD at lower powers is less important. A higher inductance value is needed to have good power quality in low power operation. The operating waveforms are shown in Fig. 5-18. THD is measured 2.34% as shown in Fig. 5-19. THD is improved with a smaller inductance when compared to Fig. 5-17 and Fig. 5-15. Additionally, the current tracking is improved as it is noticeable in the zero crossings. The controller performance can be seen in Fig. 5-20. The modulation index does not go to the over modulation regions in this configuration.

Table 5-4- Investigating Controller Parameters Adjustment versus Inductance Tolerances

	$0.5L_{ac}$	$0.75\ L_{ac}$	$0.9L_{ac}$	L_{ac}	$1.1L_{ac}$	$1.25L_{ac}$	$1.5L_{ac}$	$2L_{ac}$
L_{ac}[mH]	***2.5***	***3.75***	***4.5***	***5***	***5.5***	***6.25***	***7.5***	***10***
THD[%] (L_{cnt}=5mH)	17.46	9.91	7.55	3.19	2.19	1.92	1.93	1.57
THD[%] (L_{cnt}=4mH)	14.42	8.3	2.70	2.20	2.05	1.77	1.54	2.01
THD[%] (L_{cnt}=3mH)	11.06	2.94	2.00	1.98	1.10	1.23	1.81	2.16
THD[%] (L_{cnt}=2mH)	4.38	2.62	1.32	1.43	1.55	1.87	2.19	2.77
THD[%] (L_{cnt}=1mH)	1.53	1.32	2.09	2.31	2.53	3.14	3.79	5.12

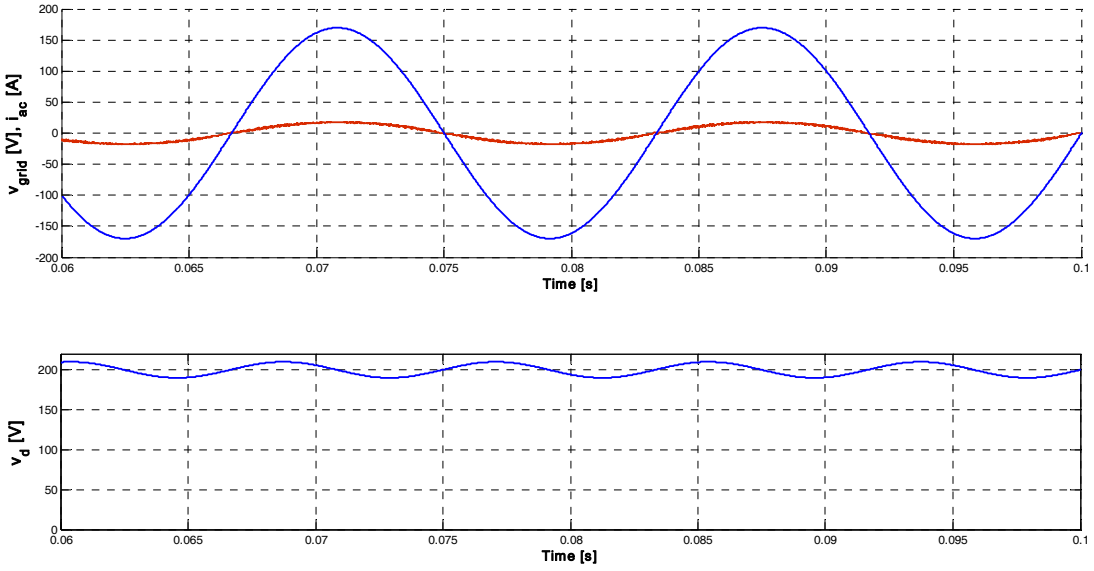

Fig. 5-18- V2G simulation at nominal power, Lac = 1 mH

Top: blue: line voltage, v_{grid}, red: output current, i_{ac}, Bottom: dc link voltage, v_d

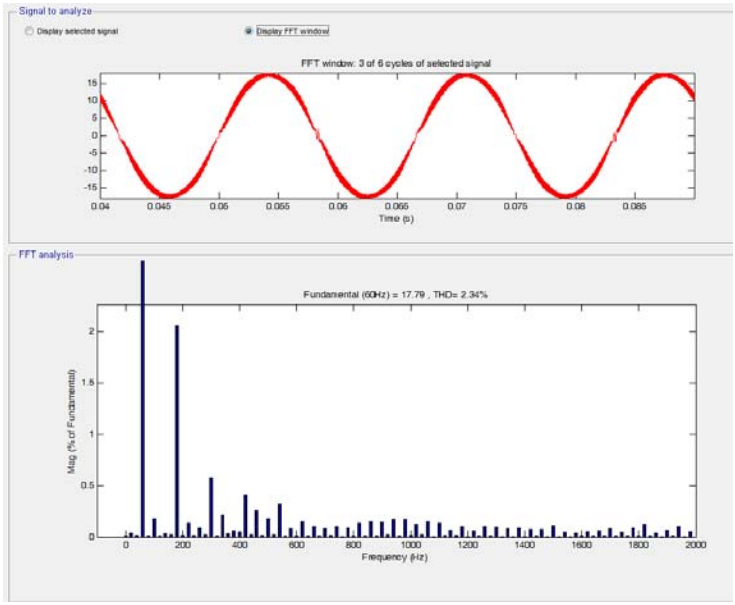

Fig. 5-19- Output current THD at nominal V2G operation, L = 1 mH

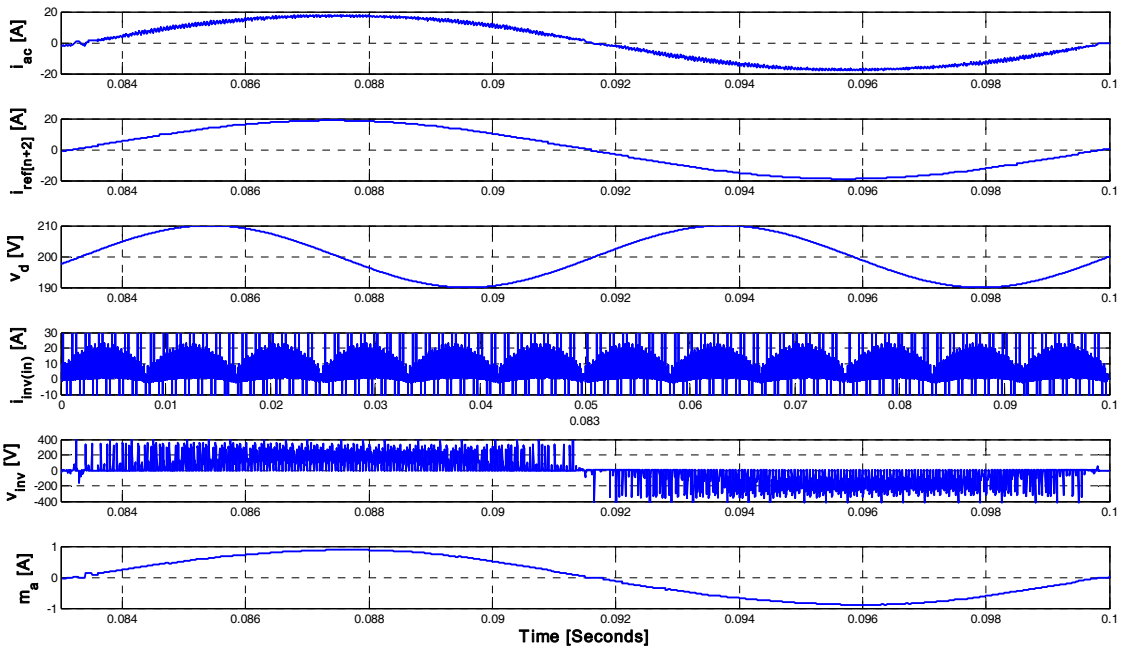

Fig. 5-20- Controller performance during nominal operation L_{ac}=1 mH, L_{cnt}=200 µH

i_{ac}: injected current, i_{ref}[n+2]: current reference, v_d: the dc link voltage ripple, $i_{inv(in)}$: inverter input current, v_{inv} inverter switching voltage, m_a: amplitude modulation index

5.3.2.3. Varying Current Reference

In this subsection, the deadbeat controller's response to the current reference changes is investigated. All case studies are performed with the simulation parameters listed in Table 5-5. The nominal rms current is 13.32 A (18.84 A amplitude). In Fig. 5-21, the current reference is reduced from 100% to 50%. The controller perfectly tracks the current step change. In Fig. 5-22, the current reference is changed from 10% to 80% and controller tracks perfectly.

Table 5-5- Simulation Parameters for 5.3.2.3

$I_{ac(nom)}$ [A]	V_{grid} [V]	V_d [V]	L_{ac} [mH]	L_{cnt} [mH]	f_{sw} [kHz]
13.32	120	200±10	1	0.2	20

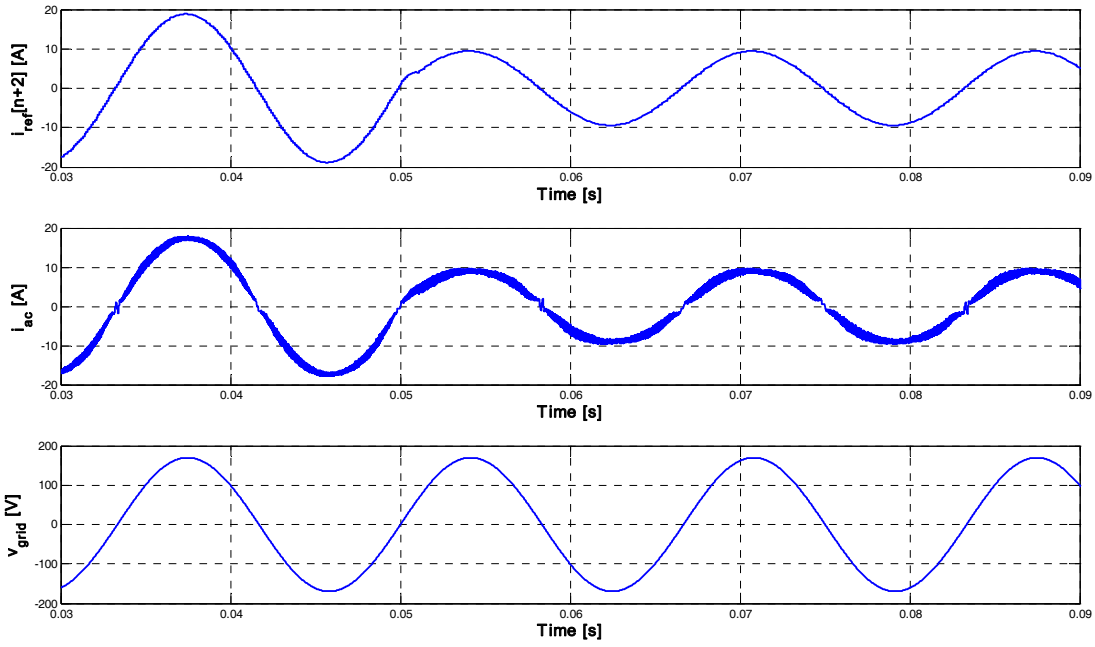

Fig. 5-21- Current reference step changes from 100% to 50%

$i_{ref}[n+2]$: current, i_{ac}: output current, v_{grid} : grid voltage

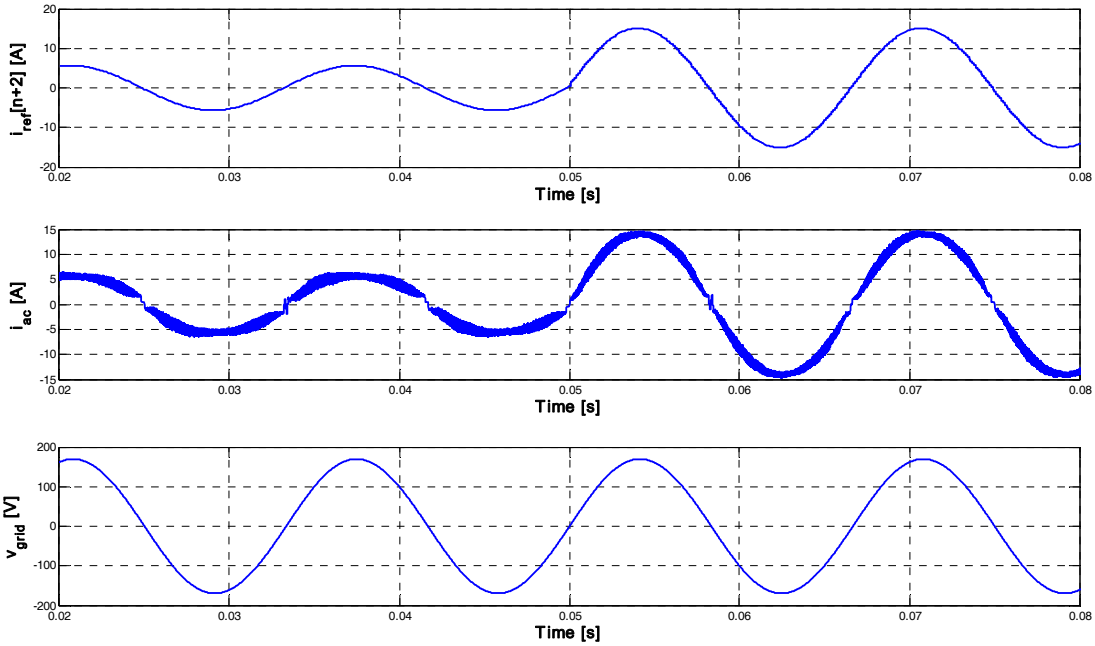

Fig. 5-22- Current reference step changes from 30% to 80%

$i_{ref}[n+2]$: current, i_{ac}: output current, v_{grid} : grid voltage

The response to a ramp change in current reference is evaluated in this case study. The current reference rises from 30% to 120% within 0.016 s to 0.16 s and returns to 40% in 0.3 s. The controller is able to track the ramp function as show in Fig. 5-23.

The behavior of 5 mH design is also evaluated in Fig. 5-24. The simulation parameters of Table 5-6 are used for this case study. The current reference is increased from 10% at 0.016 s to 120% at 0.3 s. The reference remains at 120% till 0.36 s and is decreased to 30% from 0.36 s to 0.53 s. The deadbeat controller is able to track the ramp function. The current has relatively lower ripple in lower powers when compared to Fig. 5-23.

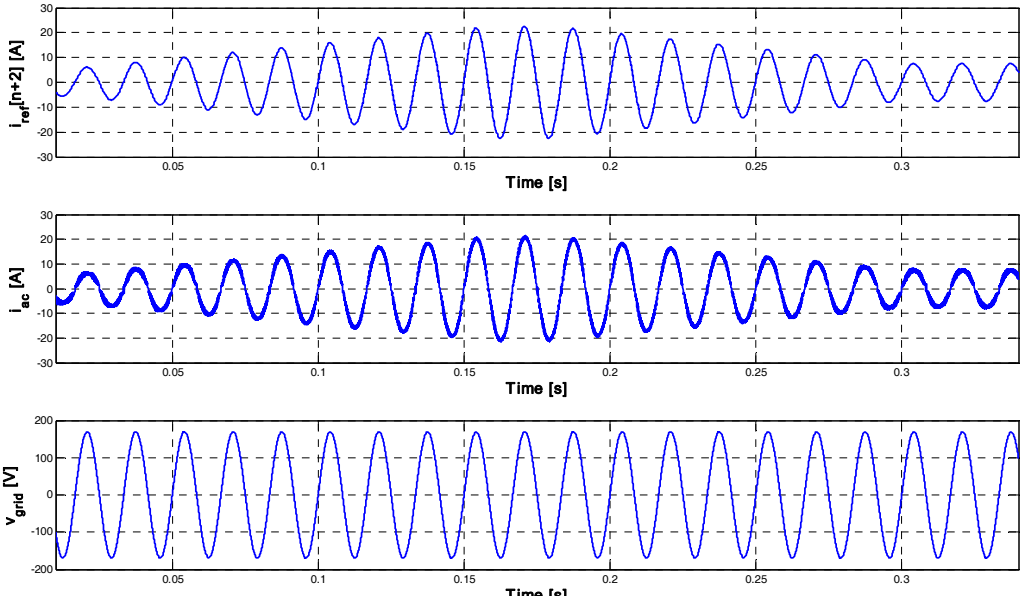

Fig. 5-23- Changing current reference with a ramp function

$i_{ref}[n+2]$: current, i_{ac}: output current, v_{grid} : grid voltage

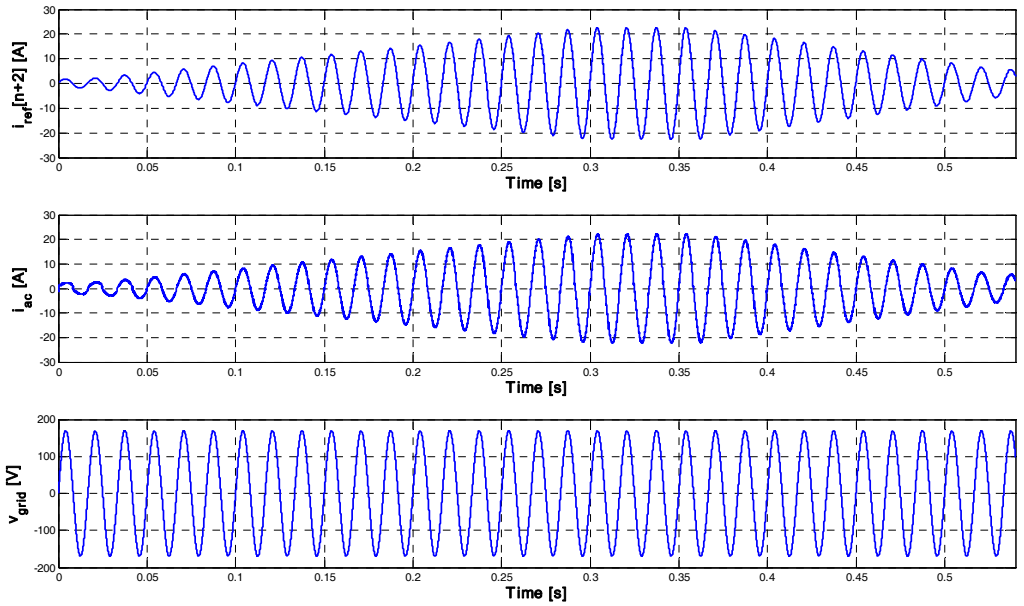

Fig. 5-24- Changing current reference with a ramp function, Table 5-6 Parameters

$i_{ref}[n+2]$: reference current, i_{ac}: output current, v_{grid} : grid voltage

Table 5-6- Simulation Parameters for L_{ac} = 5mH Design

$I_{ac(nom)}$ [A]	V_{grid} [V]	V_d [V]	L_{ac} [mH]	L_{cnt} [mH]	f_{sw} [kHz]
13.32	120	200±10	5	1	20

5.3.2.4. Deadbeat Controller Behavior During Grid Voltage Perturbations

The line voltage is allowed to change within 5% of the nominal voltage as mentioned in the 1.4 section. The controller's performance during the grid voltage perturbations is investigated in the following case study. The grid voltage is initially at its nominal value (120 V). The voltage is increased to the maximum value (126 V) suddenly at 0.1 s and stays till 0.2 s that is suddenly reduced to the minimum value (114V). The current is set at the nominal value (13.32 A) during this case study. The controller and system is set according to Table 5-6 parameters. Fig. 5-25 shows the system performance. Despite the voltage changes, the controller is able to maintain the current at the reference value.

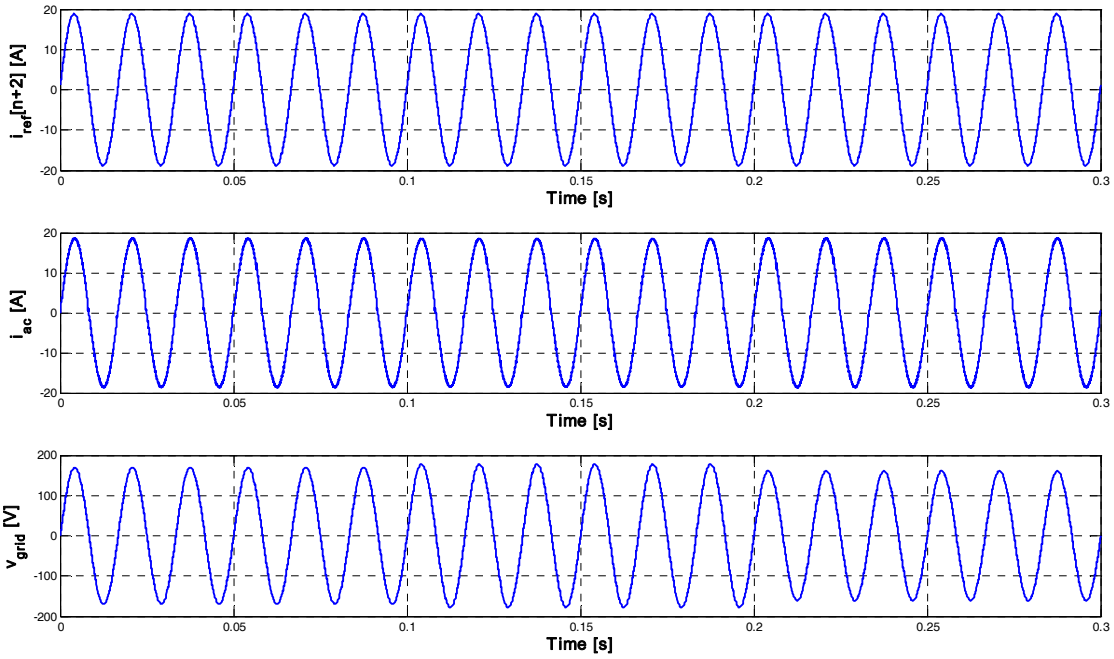

Fig. 5-25- Deadbeat controller performance during grid voltage changes

iref[n+2]: current, i_{ac}: output current, v_{grid} : grid voltage

5.3.2.5. Deadbeat Controller During Charge Mode

If the current reference is set to have 180^o phase shift according to the line voltage, the deadbeat controller will operate in the charge mode. According to the simulations the deadbeat controller is able the track the current; however the controller needs to be tuned for an acceptable THD. In Fig. 5-26, the dead-beat controller is operating at the charge mode at the nominal conditions. L_{cnt} is set as 1.2 L_{ac} and the measured THD is 4.43% (Fig. 5-27).

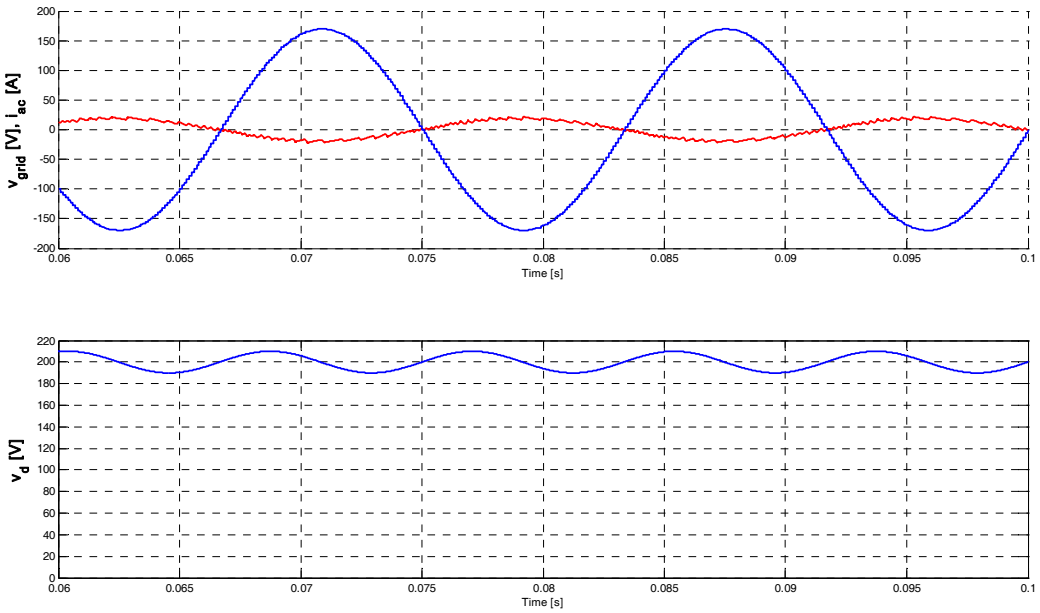

Fig. 5-26- Deadbeat controller during charge mode

Top: blue: line voltage, v_{grid}, red: output current, i_{ac}, Bottom: dc link voltage, v_d

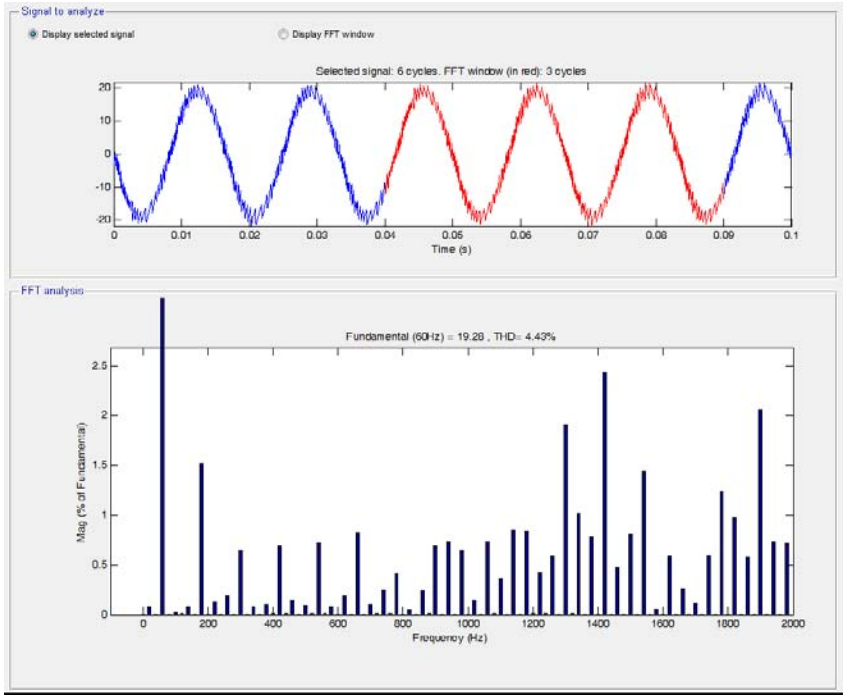

Fig. 5-27- Input current THD, deadbeat controller during charging

5.4. V2H Control

In V2H mode, the VPC acts as a voltage source or a power panel. In this mode the controller regulates the output voltage. This mode is easier than V2G as the load is not a stiff voltage source. In V2H the load can be modeled as a resistor or impedance with little reactive power. The operation of VPC during the nominal operation is verified in a case study. The inverter supplies a 9 Ω load. The voltage THD is 2.22% in this case study as shown in Fig. 5-28 and Fig. 5-29.

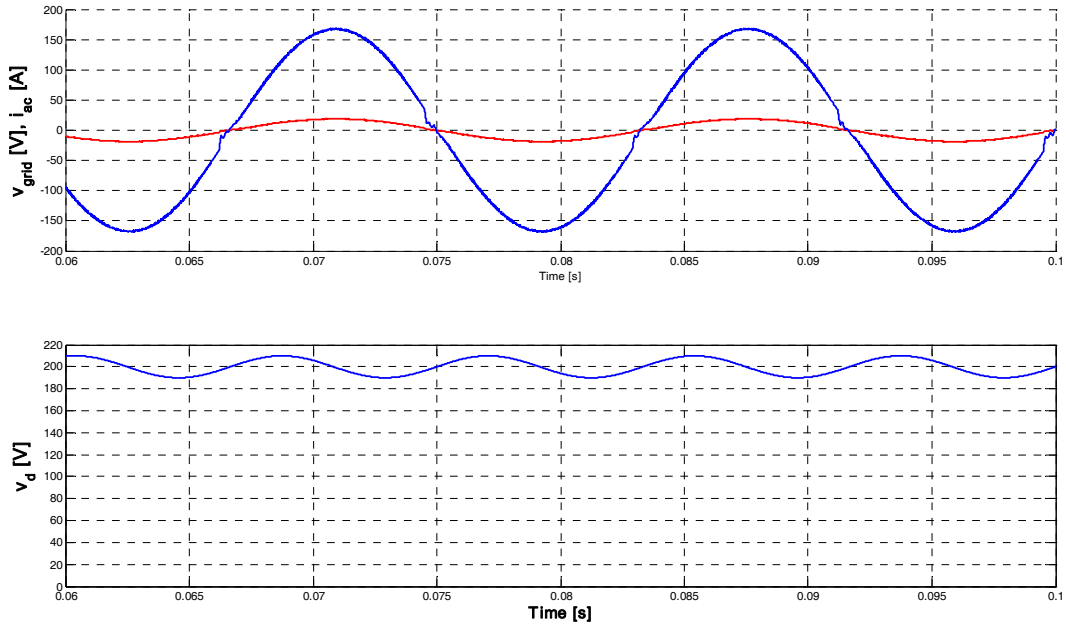

Fig. 5-28- V2H operation, full load

Top: blue: generated voltage, v_{grid}, red: load current, i_{ac}, Bottom: dc link voltage, v_d

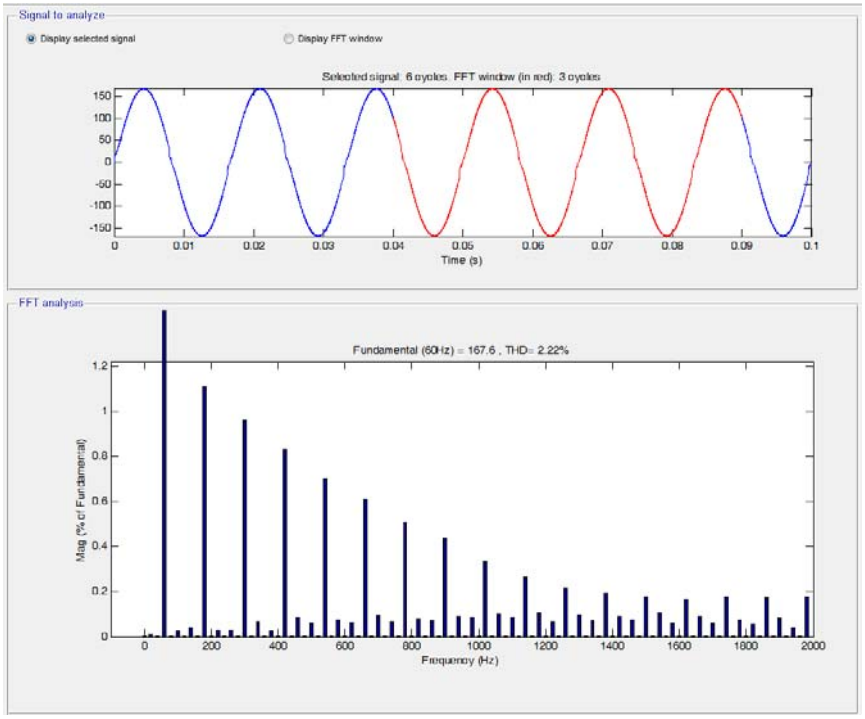

Fig. 5-29- Voltage THD during V2H operation, full load

5.5. Conclusion

The controller routines for performing major VPC functionalities were introduced in this chapter. The dc link is controlled with a slow PI controller. The charger mode employed a PFC controller that modifies the line bridge to a hybrid active rectifier. The dead-beat controller was investigated for the V2G operation.

The controllers' were implemented and verified in the simulation test bed in MATLAB SIMULINK environment. The dead beat current controller's behavior was fast with acceptable THD at different operating points. The line filter and the controller parameters were tuned according to the case studies. A preliminary design trend suggested tuning the dead-beat current controller's time constant to a value slower than the physical time constant. The V2H were employed by engaging a voltage controller

with the deadbeat controller. All the controllers were verified through different case studies at a variety of operating points. The controllers were evaluated through step response and ramp response analyses. The simulations approved the performance of the adopted control algorithms.

6. EXPERIMENTAL RESULTS

6.1. Overview

The VPC components that were developed in the previous chapters are gathered into a modular experimental setup. The experimental results are reported through the dissertation verifying the novel contributions achieved through the research. This chapter includes various case studies performed with the experimental setup to demonstrate the performance of the proposed VPC. The experimental results shown in the previous chapters were narrowly focused on detailed concepts. In contrast, the experimental results reported in this chapter intend to demonstrate the behavior of the proposed VPC. The ac link waveforms will be presented through this chapter.

The experimental setup is developed according to the described specifications of section 3.2. The sources include the 200V, 33 A Magna Power and Sorensen 150 V, 7 A, 1250 VA laboratory supplies and the batteries described in section 3.3. The power converters are H-bridge inverters discussed in section 3.4. The magnetic circuit components include ac inductors and the multiwinding transformer that were developed in chapter 4. The loads include, the 800W programmable load, the laboratory ac load module, and costume resistive loads. Fig. 6-1 shows a configuration of the experimental setup. The ac link waveforms are key waveforms to analyze DAB operation. The series ac link waveforms of the DAB at different operating mode will be presented in this chapter. The expected DAB operation as well as bad practices and the problematic operating points will be highlighted.

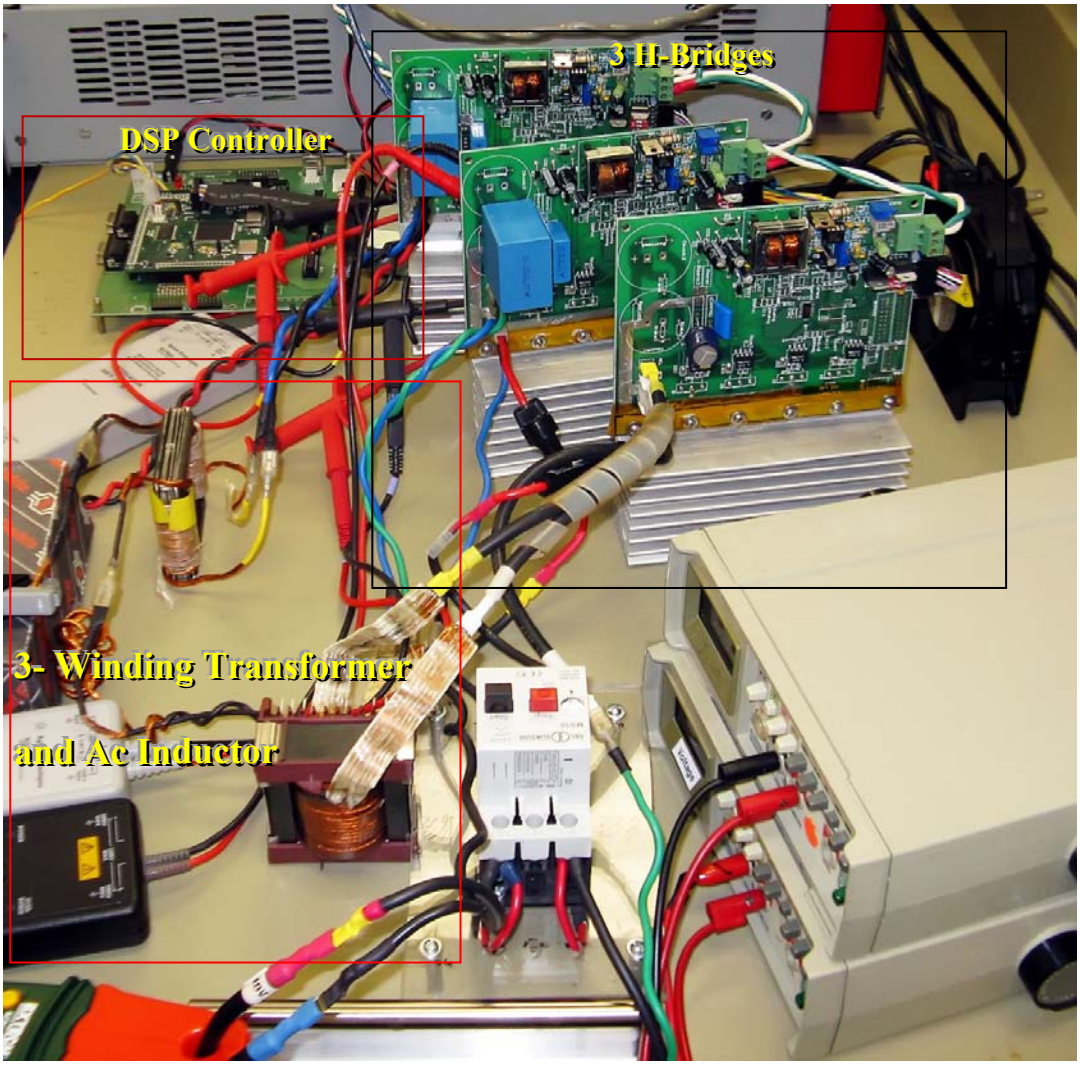

Fig. 6-1- Experimental Setup

6.2. Supplying Resistive Loads

The setup is configured as the DAB converter. The experiment parameters are listed in Table 6-1. The schematic for this set of experiments is shown in Fig. 6-2. The primary bridge is supplied with the 200 V source and a 25.1 Ω resistor is the load. The gapped ac inductor L is placed at the transformer's primary.

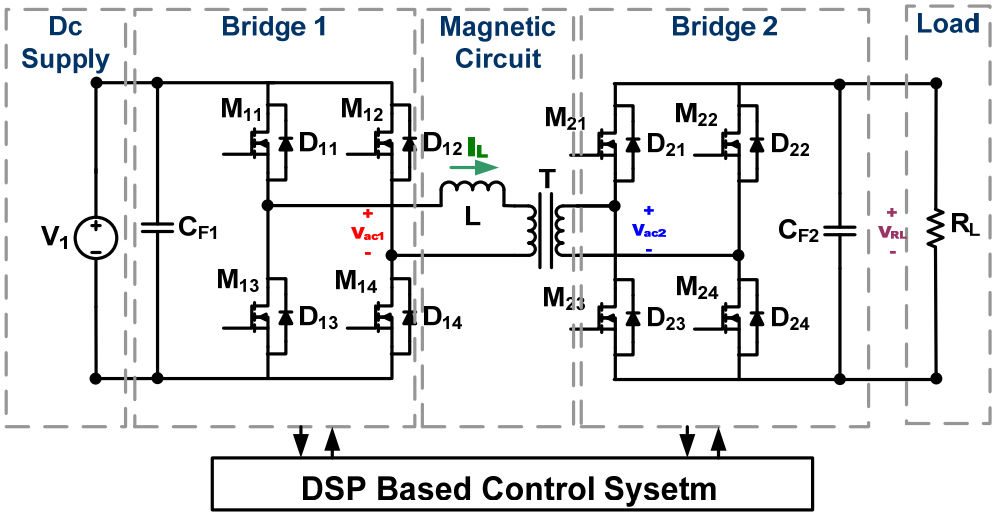

Fig. 6-2- Experimental setup configuration for supplying resistive load

Table 6-1- Experimental Setup Configuration for Supplying Resistive Loads

Bridge 1	Bridge 2	T	L	R_L
600 V	150 V	N_{PS} = 3.82	50 µH	25.1 Ω

6.2.1. Source: 30 V to 180 V, Load: 25 Ω, Phase Shift 15°

The input voltage is raised from 20 V to 200 V. The phase shift is always set at 15°. All the converter components stay below 100° F, which verifies the reliability of the developed experimental setup. The key waveforms are monitored on the oscilloscope during these experiments. The monitored waveforms include the primary bridge output (yellow), the secondary bridge output (blue), the ac link inductor current (green), and the switch M_{11} gate to source voltage (magenta). In Fig. 6-3 to Fig. 6-5, the waveforms are shown when the input voltage is 50 V, 100 V, and 180 V. The inductor current shows a curve. This is because the output capacitor of C_{F2} in Fig. 6-2 is too small for the

secondary bridge. This capacitor will be increased in subsection 6.2.3. All the measured points are listed in Table 6-2.

Table 6-2- Case Study Measurements for Supplying R_L=25.1 Ω, ϕ=15°

V_{in} [V]	I_{in} [A]	V_{out} [V]	I_{out} [A]	ϕ [°]	Pin [W]	Pout [W]	ŋ [%]
52.1	0.38	13.3	1.94	15	19.80	25.80	130.33
75.4	0.35	19.4	1.39	15	26.39	26.97	102.18
90.2	0.40	23.2	1.68	15	36.08	38.98	108.03
100.8	0.46	26.1	1.89	15	46.37	49.33	106.39
120	0.8	32.2	2.33	15	96.00	75.03	78.15
136.0	0.9	35.0	2.56	15	122.40	89.60	73.20
140	0.9	34.8	2.60	15	126.00	90.48	71.81
150	1.0	23.5	2.87	15	150.00	67.45	44.96
160	1.1	13.9	3.06	15	176.00	42.53	24.17
179	1.4	5.8	3.3	15	250.60	19.14	7.64

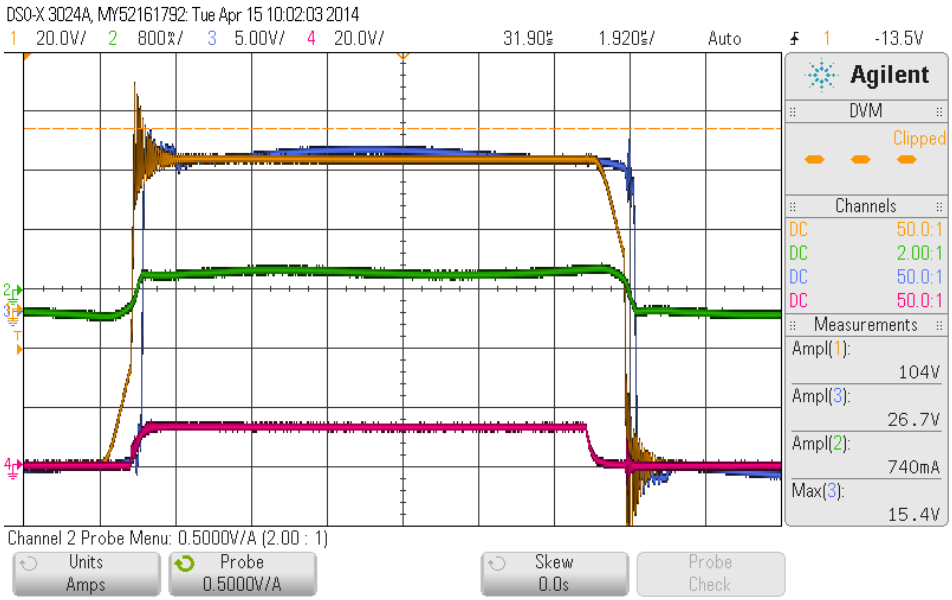

Fig. 6-3- DAB supplying R_L=25.1 Ω , V_{in}=50.2 V , ϕ=15°

yellow: V_{ac1}, blue: V_{ac2}, green: I_{Lac}, magenta: $V_{gs(M11)}$

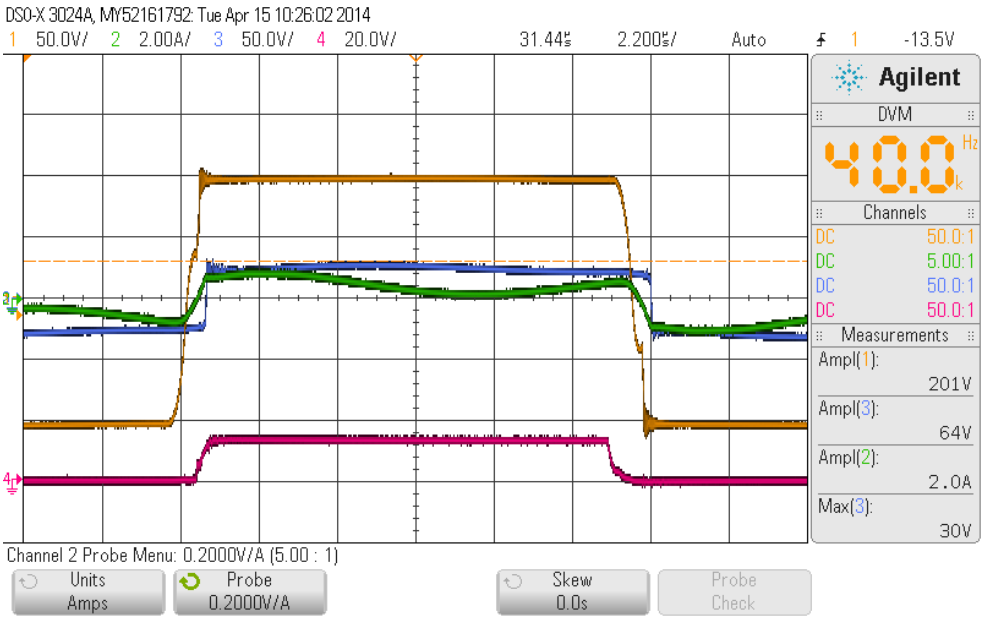

Fig. 6-4- DAB supplying R_L=25.1 Ω , V_{in}=100 V , ϕ=15°

yellow: V_{ac1}, blue: V_{ac2}, green: I_{Lac}, magenta: $V_{gs(M11)}$

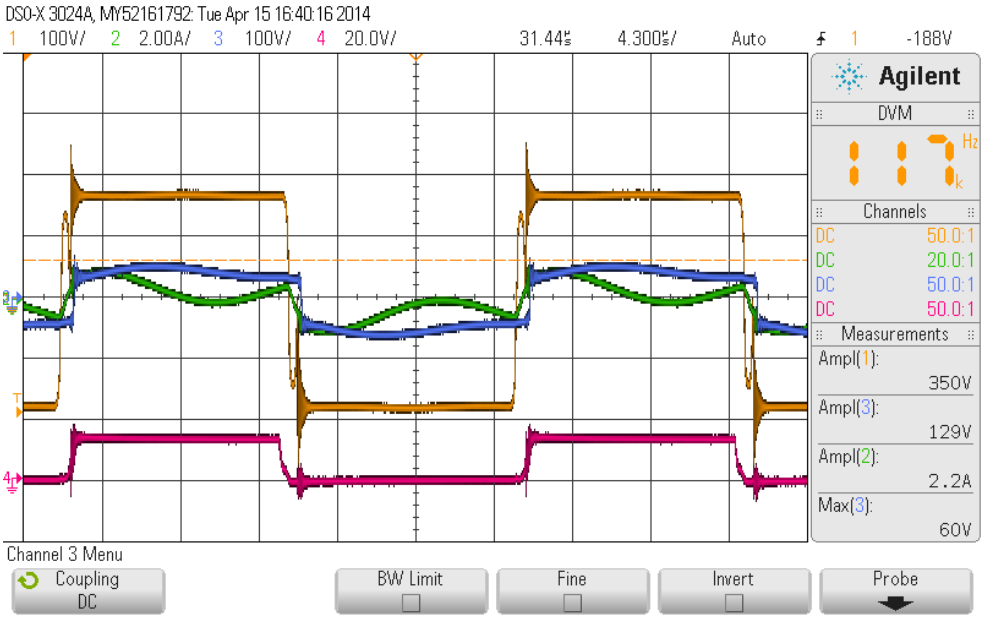

Fig. 6-5- DAB supplying R_L=25.1 Ω , V_{in}=180 V , ϕ=15°

yellow: V_{ac1}, blue: V_{ac2}, green: I_{Lac}, magenta: $V_{gs(M11)}$

6.2.2. Source: 30 V to 180 V, Load: 25 Ω, Phase Shift 25°

The previous case study is repeated for 25° phase shift. The captured waveforms include the primary bridge output (yellow), the secondary bridge output (blue), the ac link inductor current (green), and the load resistor voltage (magenta). The load resistor voltage shows how the DAB output voltage is pulsed when the output filter is not chosen properly. Noticeably, it causes reactive power through the converter at lower powers as shown in Fig. 6-6. The waveforms are displayed in Fig. 6-6 to Fig. 6-8 for the input voltage of 40 V, 60 V, and 180 V. The measurements are listed in Table 6-3.

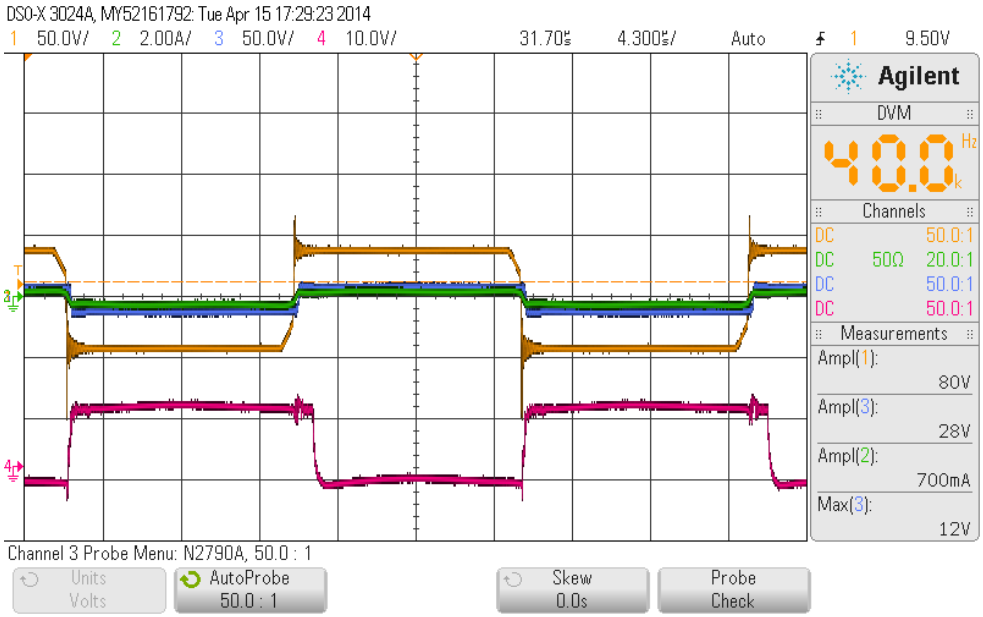

Fig. 6-6- DAB supplying R_L=25.1 Ω , V_{in}=40 V , ϕ=25°

yellow: V_{ac1}, blue: V_{ac2}, green: I_{Lac}, magenta: $V_{gs(M11)}$

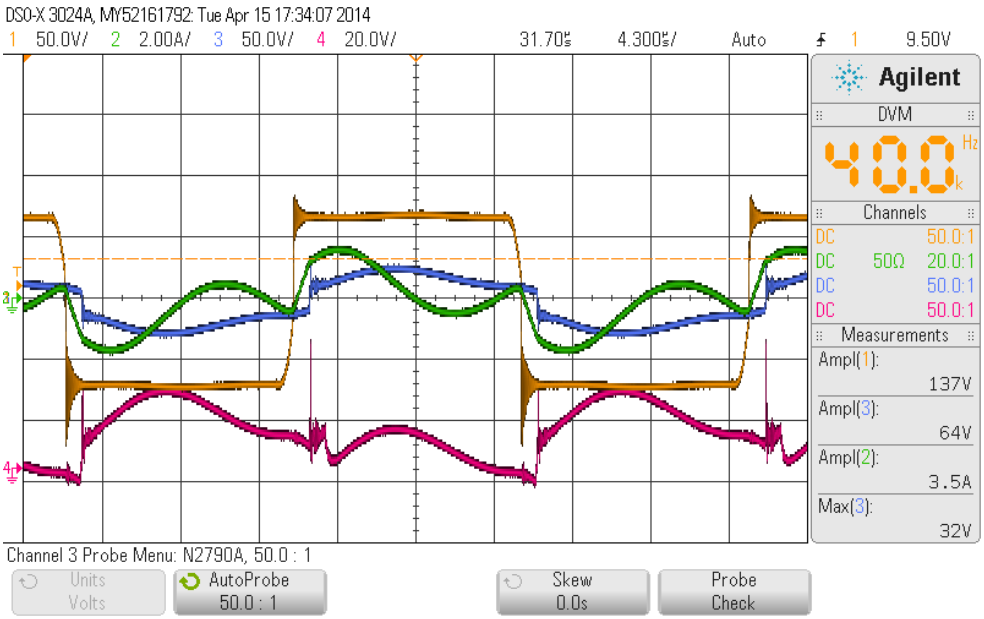

Fig. 6-7- DAB supplying R_L=25.1 Ω , V_{in}=60 V , ϕ=25°

yellow: V_{ac1}, blue: V_{ac2}, green: I_{Lac}, magenta: $V_{gs(M11)}$

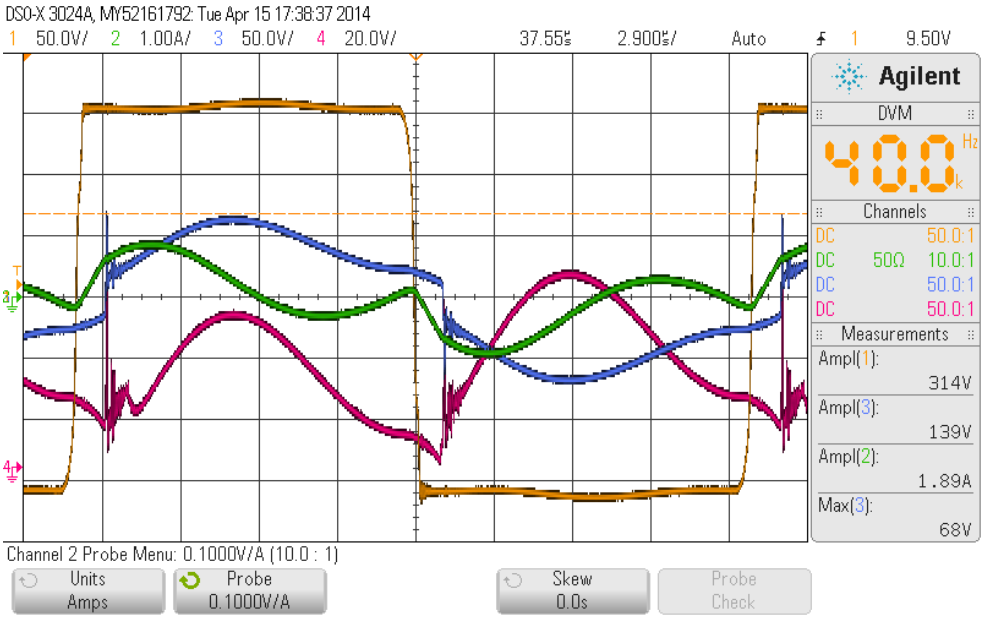

Fig. 6-8- DAB supplying R_L=25.1 Ω , V_{in}=178 V , ϕ=25°

yellow: V_{ac1}, blue: V_{ac2}, green: I_{Lac}, magenta: $V_{gs(M11)}$

Table 6-3- Case Study Measurements for Supplying R_L=25.1 Ω, ϕ=25°

V_{in} [V]	I_{in} [A]	V_{out} [V]	I_{out} [A]	ϕ [°]	Pin [W]	Pout [W]	ŋ [%]
30	0.3	7.8	0.55	25	9.00	4.29	47.67
69	0.5	18.3	1.3	25	34.50	23.79	68.96
107	0.8	28.3	2.14	25	85.60	60.56	70.75
160	1.3	42.4	NA	25	208.00	NA	NA

6.2.3. Supplying Resistive Load, Increased DAB Capacitors

The DAB capacitors are increased to the values that were calculated in the subsection 3.6.1.3. Fig. 6-9 shows how the experimental setup is configured for this experiment. For this load, the current is low and goes negative. The experiments are listed in Table 6-4. As can be seen in the experimental results, the output dc voltage will be maintained constant and the current is straight. The ac link waveforms and the dc output voltage are displayed for two different operating points. Fig. 6-10 belongs to the input voltage is 30 V and the phase shift is 25° (the ac current scale is not set correctly in this particular oscilloscope snapshot). Fig. 6-11 belongs to the input voltage at 120 V and the phase shift of 15°.

An unforeseen fault happened at the end of this experiment and computer and programmer were reset. Fortunately, the circuit was not damaged. The next day the DSP programmer frequently halted. These issues were due to the bad power quality of the three phase mains at the laboratory's building. Specifically, when the adjacent power electronics laboratories draw or inject unbalanced or polluted current the conductive EMI conducts through the three phase panel and causes such problems. Due to these issues, the 3-phase Magana power supply was replaced with the single phase Sorensen

power supply. Similar issues did not happen with the single phase power supply; however, the Sorensen power supply is a low power source and the tests need to be conducted at lower voltages.

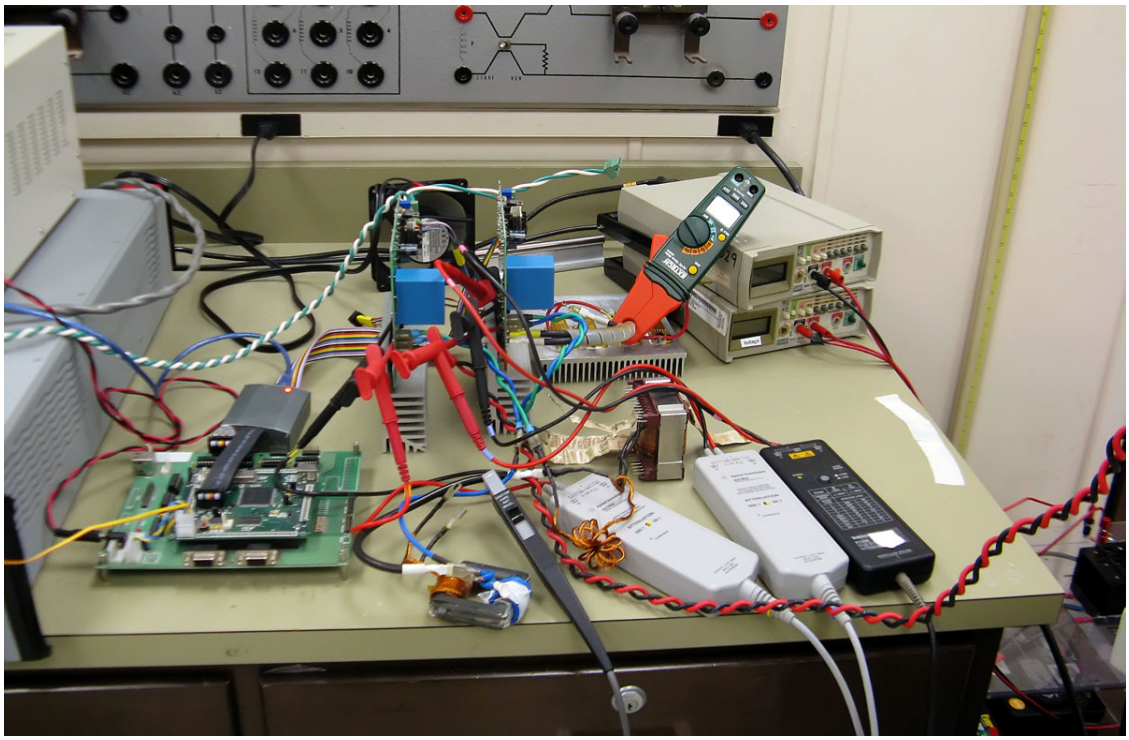

Fig. 6-9- Experimental setup for supplying resistive load, increased DAB capacitors

Table 6-4- Case Study Measurements for Supplying R_L=25.1 Ω, Increased DAB Capacitors

V_{in} [V]	I_{in} [A]	V_{out} [V]	I_{out} [A]	ϕ [°]	Pin [W]	Pout [W]	Ɗ [%]
30	0.9	11.56	0.54	25	27.00	6.24	23.12
30	0.2	4.5	0.28	15	6.00	1.26	21.00
52.1	0.3	12.44	0.53	15	15.63	6.59	42.18
75	0.9	18.2	0.726	15	67.50	13.21	19.58
90	1.1	19.6	0.973	15	99.00	19.07	19.26
100.8	1.1	22.61	1.08	15	110.88	24.42	22.02
120	1.21	28.3	1.19	15	145.20	33.68	23.19

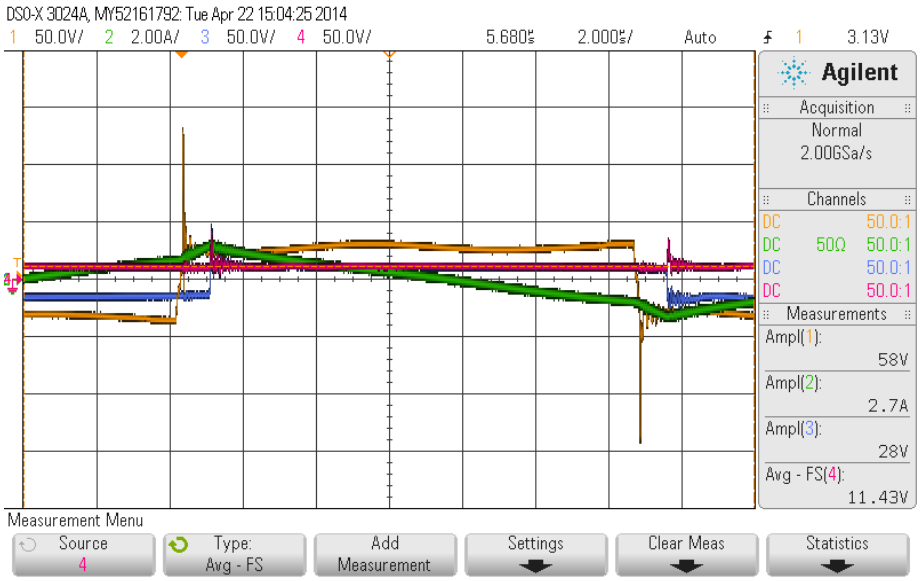

Fig. 6-10- DAB supplying R_L=25.1 Ω , V_{in}=30 V , ϕ=25°

yellow: V_{ac1}, blue: V_{ac2}, green: I_{Lac}, magenta: $V_{gs(M11)}$

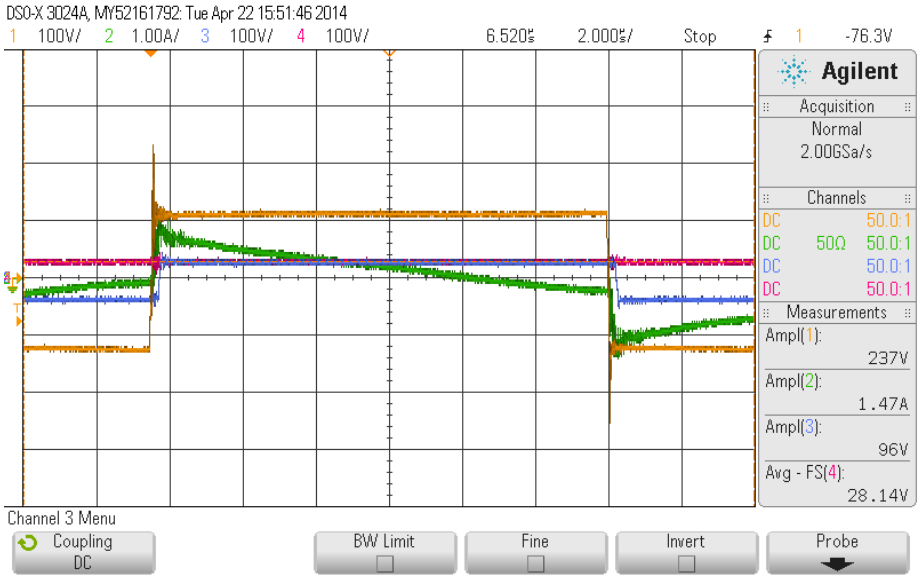

Fig. 6-11- DAB supplying R_L=25.1 Ω , V_{in}=120 V , ϕ=15°

yellow: V_{ac1}, blue: V_{ac2}, green: I_{Lac}, magenta: $V_{gs(M11)}$

6.2.4. Supplying Resistive Load, Investigating Dead Time

For the following experiments presented in this subsection, the source is changed with the 150 V Sorensen power supply. The ac inductor is replaced with the smaller 7.45 μH gapped ac inductor that was designed in subsection 4.3.1. The dead time (t_d) was set at 1 μs in previous subsections. The dead time is decreased for different operating points as listed in Table 6-5. The primary side bridge uses 150 V switches and the secondary side bridge uses the 40 V switches. The resistive load and transformer are set similar to the previous subsections.

The experiments have not shown a different ac link signature when the dead time modified. An example is shown in Fig. 6-12. The dead time below 0.5 μs looks too aggressive for high power DAB operating points according to the observations. Concluding the experiments, the phase shift modulation is not a proper modulation for supplying resistive loads for such low powers. The experiments suggest designing DAB output capacitors at higher values. The main goal of the experiments of supplying the resistive loads at low power has been verifying the power conditioning stages prior connecting to the batteries. The batteries have very high current capacities and can easily destroy the power conditioner if a mistake happens. In the next sections, the VPC conditions the batteries.

Table 6-5- Case Study Measurements for Supplying R_L=25.1 Ω, Different Dead Times

V_{in} [V]	I_{in} [A]	V_{out} [V]	I_{out} [A]	ϕ [°]	t_d [µs]	Pin [W]	Pout [W]	Ƞ [%]
30	0.84	8.98	0.44	20	0.6	145.20	33.68	23.19
30	1.19	9.29	0.46	20	0.3	25.20	3.95	15.68
30	1.55	9.89	0.47	20	0.15	35.70	4.27	11.97
30	2.69	10.70	0.5	30	0.3	46.50	4.65	10.00

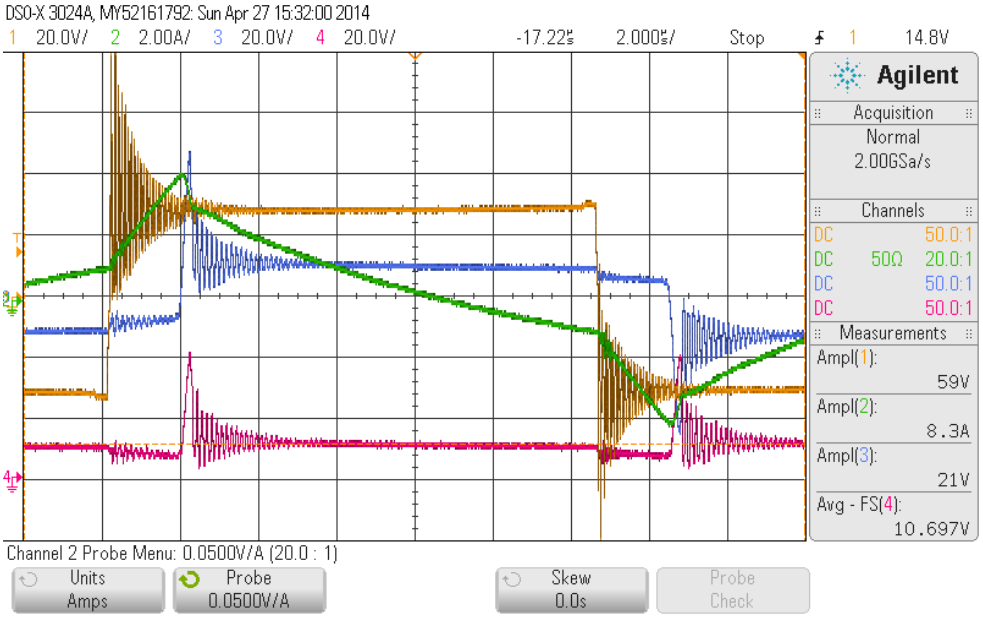

Fig. 6-12- DAB supplying R_L=25.1 Ω , V_{in}=30 V , ϕ=20°, t_d=0.15 µs

yellow: V_{ac1}, blue: V_{ac2}, green: I_{Lac}, magenta: $V_{gs(M11)}$

6.3. Charging Batteries from Grid

In this set of experiments, the DAB is supplied from the grid. The grid voltage is adjusted through an auto-transformer and rectified through the full-wave rectifier which has been replaced the line side bridge. The experimental setup configuration is shown in Fig. 6-13. This set of experiments was used for supporting sections 3.6.2 and 4.4.

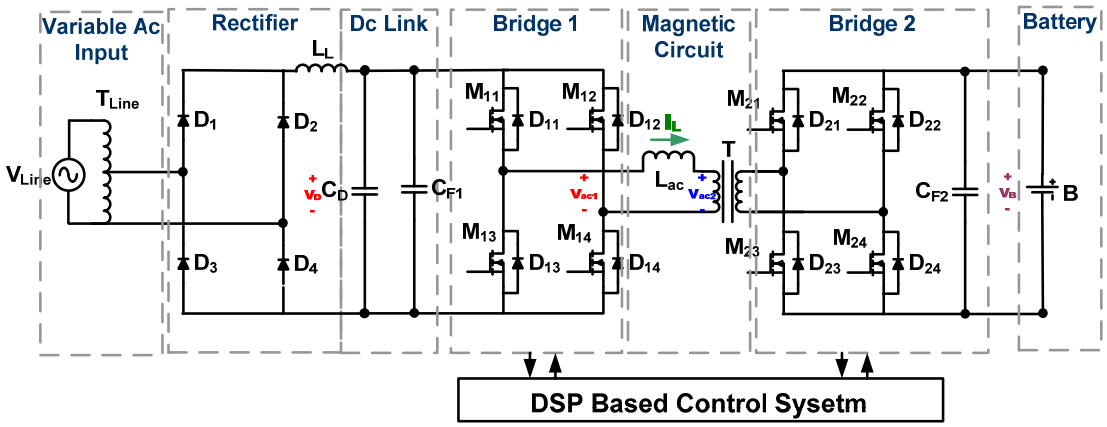

Fig. 6-13- Charging battery from grid

6.3.1. Charging 12 V Battery from Grid through Dc Link, Transformer Exists

During these experiments the input voltage is varied around 50 V and the phase shift is set at 30°. Both the bridges use 300 V switches (IXTQ25N30P), which were used in the earlier version of the experimental setup. The dc link is connected to the primary winding and the battery bridge is connected to the secondary winding. L_{ac} including the leakage is 50 µH at the primary. The measurements are listed in Table 6-6. The waveforms shown in Fig. 6-14 are captured in this experiment when the input voltage is 48.8 V. The secondary waveforms show a large spike as was discussed in the 4.4.1 section. In Fig. 6-14, the yellow waveform is the gate to source voltage of M_{22}. The blue waveform belongs to the channel voltage of M_{22}. The secondary ac voltage and current are displayed in magenta and green, respectively.

Table 6-6- Charging 12V Battery from Grid

V_{in} [V]	I_{in} [A]	V_{out} [V]	I_{out} [A]	ϕ [°]	Pin [W]	Pout [W]	ŋ [%]
48.6	1.08	14.46	3.17	30	52.49	45.84	87.33
48.8	0.87	14.08	2.78	30	42.46	39.14	92.20
49.1	0.977	14.10	3.04	30	47.97	42.86	89.35

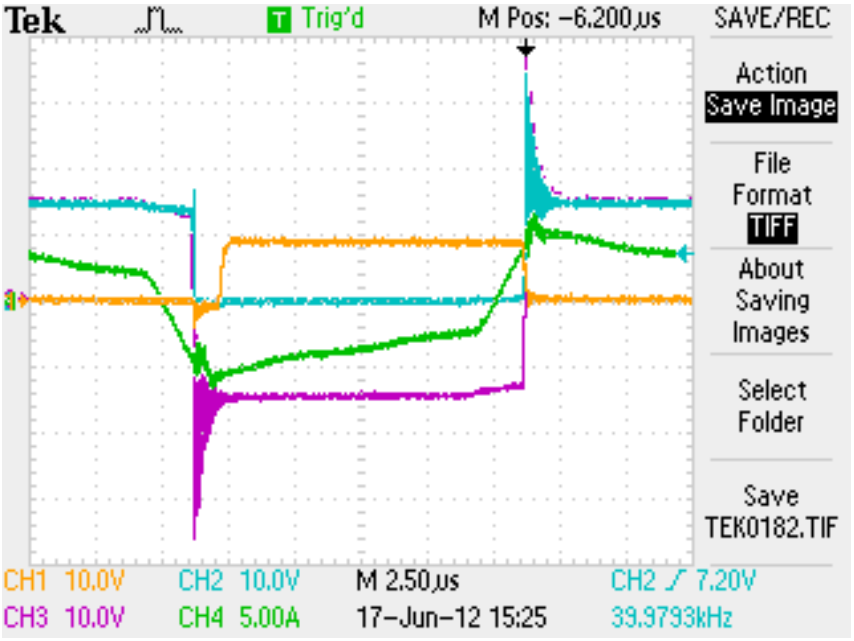

Fig. 6-14- DAB operation during charging low voltage battery form grid

yellow: $V_{gs(m22)}$, blue: $V_{ds(m22)}$, green: $I_{ac(sec)}$, magenta: V_{ac2}

6.3.2. Charging 48 V Battery from Grid through Dc Link, Transformer Removed

In this experiment for charging the high voltage battery, the transformer is removed and the 12 V battery is replaced with the 48 V battery. The experimental setup

configuration is displayed in Fig. 6-15. The experiments listed in Table 6-7 are performed in order to achieve a relating operating point to the previous case studies. In contrast to the experiments of the previous subsection, the waveforms are clean in this experiment. This effect was analyzed in the subsection 4.4.1.

Due to the presence of the double frequency ripple, dc link varies. At each phase shift two readings are recorded. The power and efficiency measurements are not accurate. They are calculated from the voltage and current meters readings. This power converter topology needs a high frequency power analyzer which was not available. It does not affect the contributions of this dissertation as the major intention of the experimental setup is proving the novel proposed concepts.

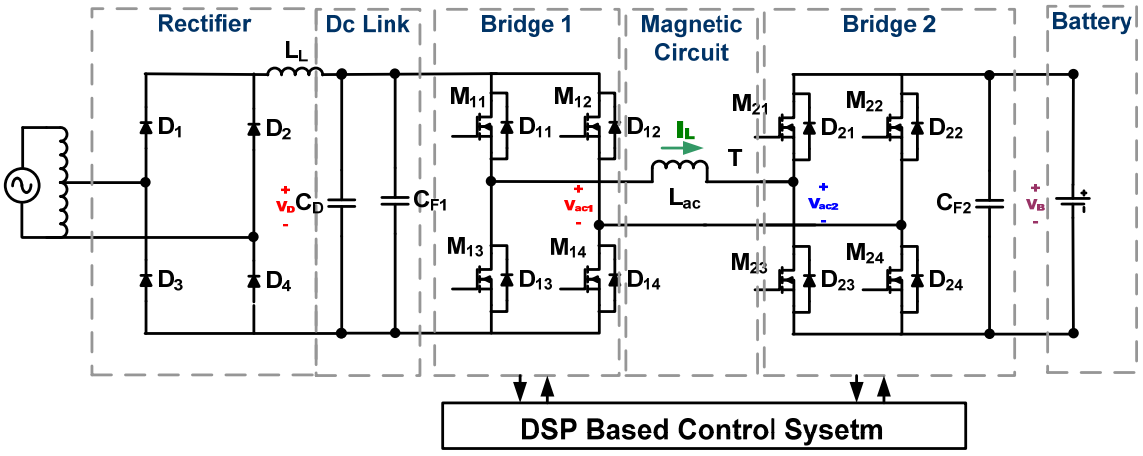

Fig. 6-15- Charging high voltage battery from grid, transformer is removed

The ac link waveforms including V_{ac1}, V_{ac2}, and I_L are captured. The M_{11} gate to source voltage is also captured. The oscilloscope snapshots for the 30^o phase shift are displayed in Fig. 6-16 and Fig. 6-17. Fig. 6-16 is captured at the minimum dc link

voltage and the DAB is operating at boost mode. Alternatively, Fig. 6-17 is captured when the dc link has its minimum value and the DAB is operating in the buck mode. Fig. 6-18 is captured when the dc link voltage is almost identical to the battery voltage.

Table 6-7- Charging 48V Battery from Grid

V_{in} [V]	I_{in} [A]	V_{out} [V]	I_{out} [A]	ϕ [°]	Pin [W]	Pout [W]	η [%]
46.1	1.9	53.1	1.68	30	87.59	89.21	101.85
53.8	2.05	53.4	1.95	30	110.29	104.13	94.41
47.4	1.62	53.3	1.28	25	76.79	68.22	88.85
54.4	1.76	53.4	1.82	25	95.74	97.19	101.51
48.4	1.22	53.2	1.21	20	59.05	64.37	109.02
48.4	0.8	52.9	0.76	15	38.72	40.20	103.83

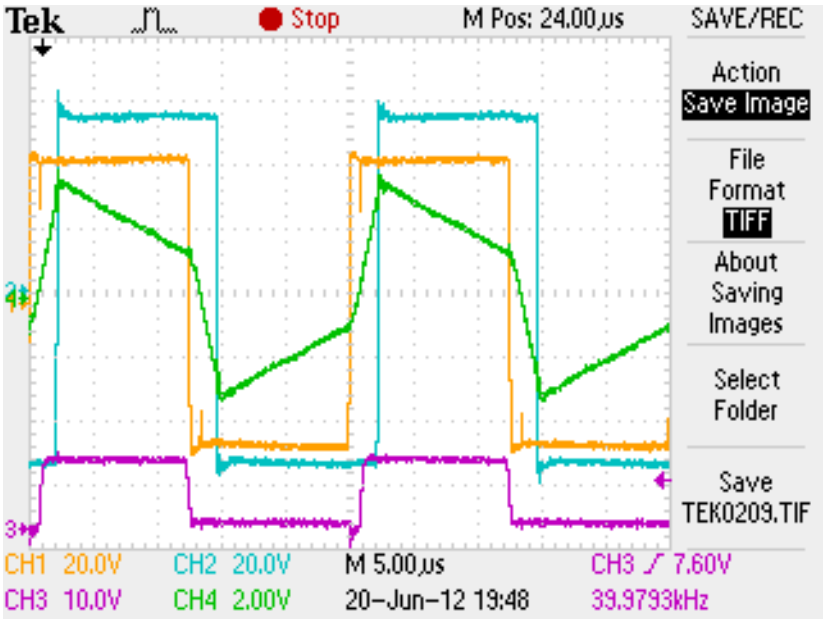

Fig. 6-16- Charging high voltage battery form the grid, transformer is removed, V_{in}= 46.1 V, ϕ= 30°

yellow: V_{ac1}, blue: V_{ac2}, green: I_{Lac}, magenta: $V_{gs(M11)}$

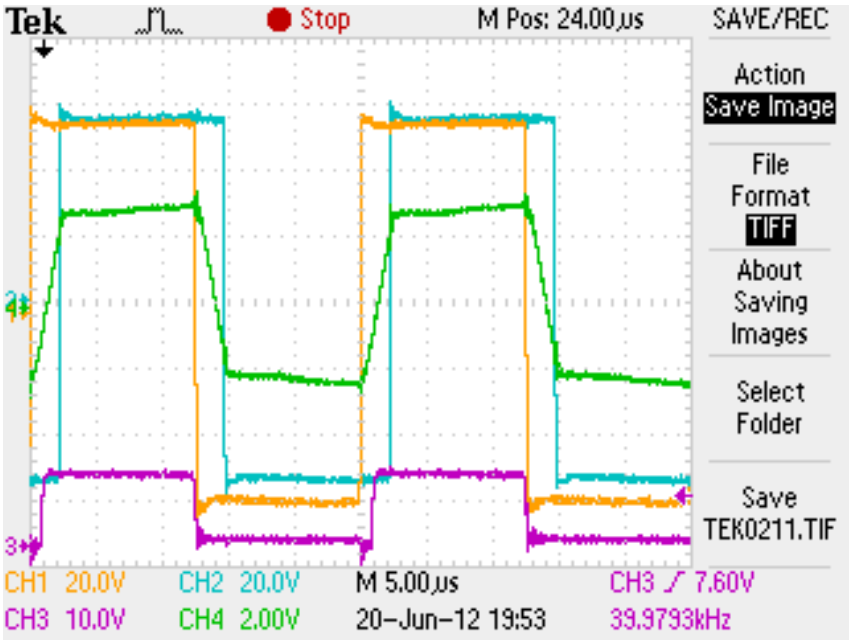

Fig. 6-17- Charging high voltage battery form grid, transformer removed V_{in}= 53.8 V, ϕ= 30^{o}

yellow: V_{ac1}, blue: V_{ac2}, green: I_{Lac}, magenta: $V_{gs(M11)}$

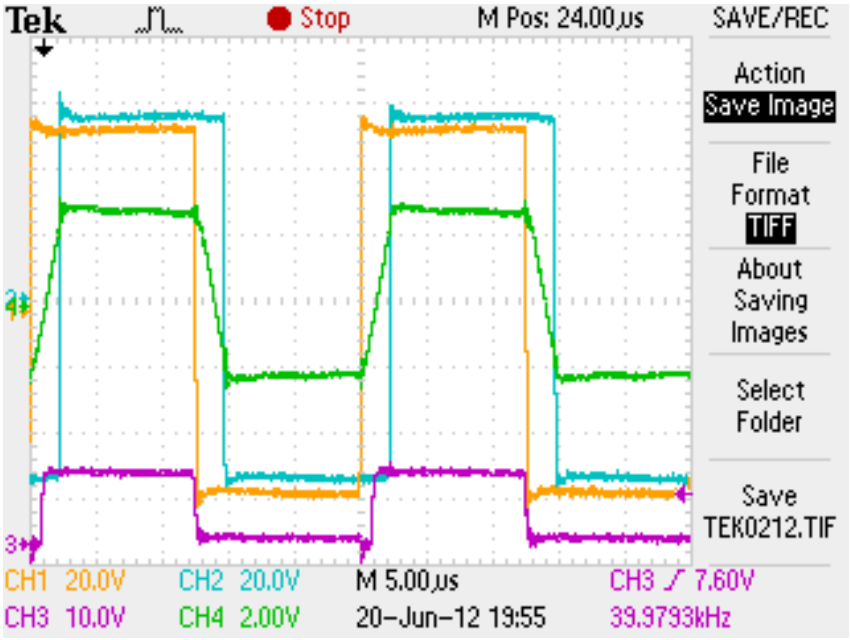

Fig. 6-18- Previous experiment, dc link voltage is almost identical to battery voltage

yellow: V_{ac1}, blue: V_{ac2}, green: I_{Lac}, magenta: $V_{gs(M11)}$

6.4. Charging Batteries from Laboratory Power Supply

The dc link ripple adds uncertainties for the static measurements. The presence of double frequency ripple was demonstrated in the previous section. In this section, the dc link has been replaced with the 150 V laboratory power supply as the input of the primary bridge. The secondary and tertiary bridges will supply the batteries.

6.4.1. Charging 12 V Battery

The experimental setup is configured as described in Table 6-8. The 600 V bridge is placed at the transformer's primary and the 150 V bridge is placed at the secondary side winding. In order to control the dc capacitor's surge current, two start-up resistors are foreseen between the batteries and the VPC. The start-up resistors are designed as 4 Ω and 16 Ω for 12 V and 48 V batteries respectively. A three phase contactor is in parallel with the start-up resistors. The contactor shorts the start-up resistors after the initial charge and prior operating the experiment. In the next subsections, charging the 12 V battery from the laboratory dc source will be tested. Moreover, the gapped ac inductor and the novel coupled ac inductor will be compared.

Table 6-8- Experimental Setup Charging 12 V Battery from Power Supply

Bridge 1	Bridge 2	T	L	Source	Load
600 V	150 V	N_{PS} = 3.82	50 µH	150 V Supply	12 V Battery

6.4.1.1. Charging 12 V Battery Using Gapped Ac Inductor

Initially, the 42 µH gapped ac inductor is placed at transformer's primary. The dead time is set at 0.6 µs. The input voltage is set at 50 V and the phase shift is set at

30°. The ac link wave forms are shown in Fig. 6-19 and the measurements are reported in the first column of Table 6-9. Similar to the results of the subsection 6.3.1, the secondary ac voltage has spikes.

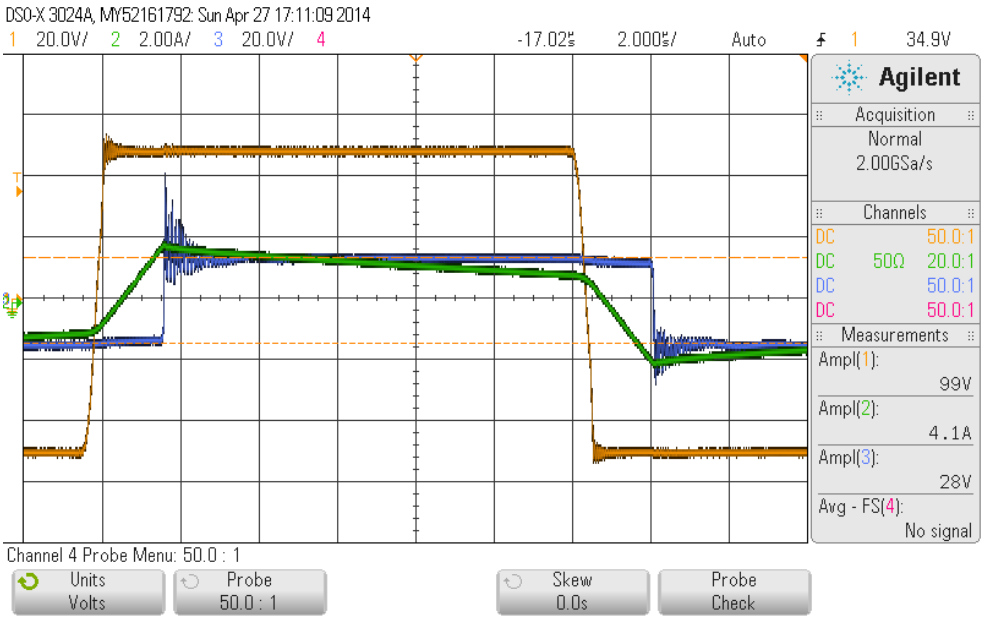

Fig. 6-19- Charging low voltage battery from 50 V dc source, gapped ac inductor, yellow: V_{ac1}, blue: V_{ac2}, green: $I_{ac(pri)}$

6.4.1.2. Charging 12 V Battery Using Coupled Ac Inductor

The coupled ac inductor is replaced with the gapped ac inductor. All other experiment settings are identical to the previous experiment. The coupled ac inductor was designed in subsection 4.3.3. The experiment configuration is similar to the circuit diagram of Fig. 4-8. The ac link waveforms are shown in Fig. 6-20. The results are almost identical. The secondary voltage is slightly cleaner in case of the coupled inductor when Fig. 6-19 and Fig. 6-20 are compared side by side. However, the voltage

spike exists in both figures. This experiment's measurements are listed in the second row of Table 6-9.

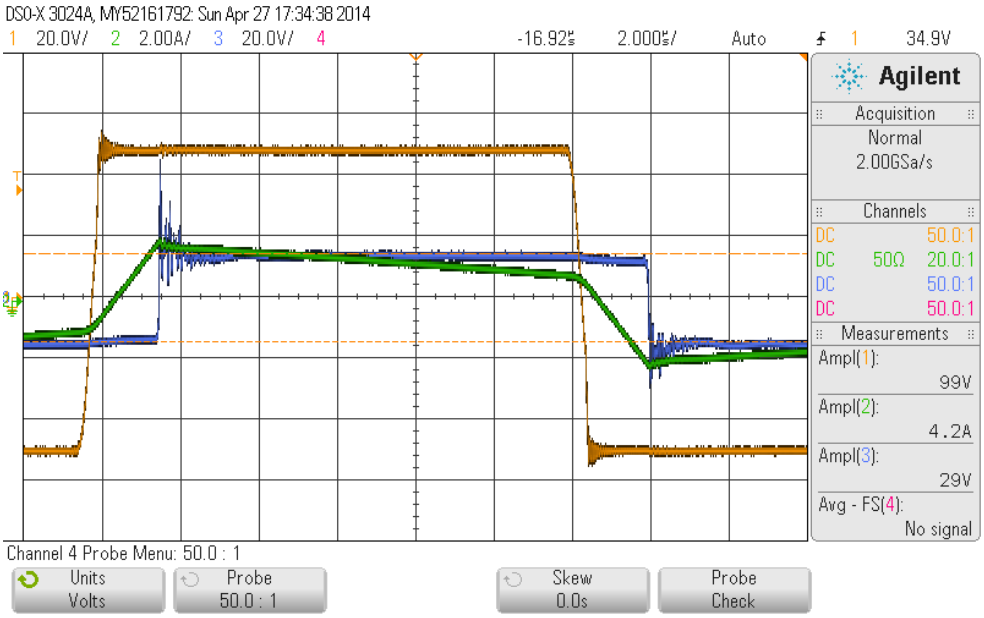

Fig. 6-20- Charging low voltage battery from 50 V dc source, coupled ac inductor, yellow: V_{ac1}, blue: V_{ac2}, green: $I_{ac(pri)}$

Table 6-9- Charging 12V Battery from Laboratory Supply

V_{in} [V]	I_{in} [A]	V_{out} [V]	I_{out} [A]	ϕ [°]	Pin [W]	Pout [W]	η [%]
50	1.35	13.85	3.9	30	67.50	54.02	80.02
50	1.43	13.83	4.3	30	71.50	59.47	83.17
59.6	1.67	14.83	5.6	30	99.53	83.05	83.44
65.4	1.77	15.2	6.4	30	115.76	97.28	84.04
55.5	1.55	13.85	5.2	30	86.03	72.02	83.72
55.5	2.19	15.1	6.5	40	121.55	98.15	80.75
55.5	2.77	15.76	7.6	50	153.74	119.78	77.91
50	2.57	14.75	6.6	50	128.50	97.35	75.76
50	3.09	15.41	7.2	60	154.50	110.95	71.81

The efficiencies are improved in the charging experiments in respect to the resistive load although the efficiencies are still below the expected value. The designed inductor is intended for 200 V and 1.5 kW power level. This is a limited test due to the laboratory considerations. The secondary voltage spikes and lower utilization factor due to the oversized inductor are the reason the efficiencies are around 10% to 15% lower than the expected value. All the experiments in this subsection are performed with the coupled ac inductor. The input voltage is increased to 65.4 V to achieve the flat ac link current as shown in Fig. 6-21. After this test, the voltage is controlled in a way the output voltage does not damage the battery. The phase shift is increased with 10^{o} steps to 60^{o}. The ac link waveforms at 60^{o} phase shift are shown in Fig. 6-22.

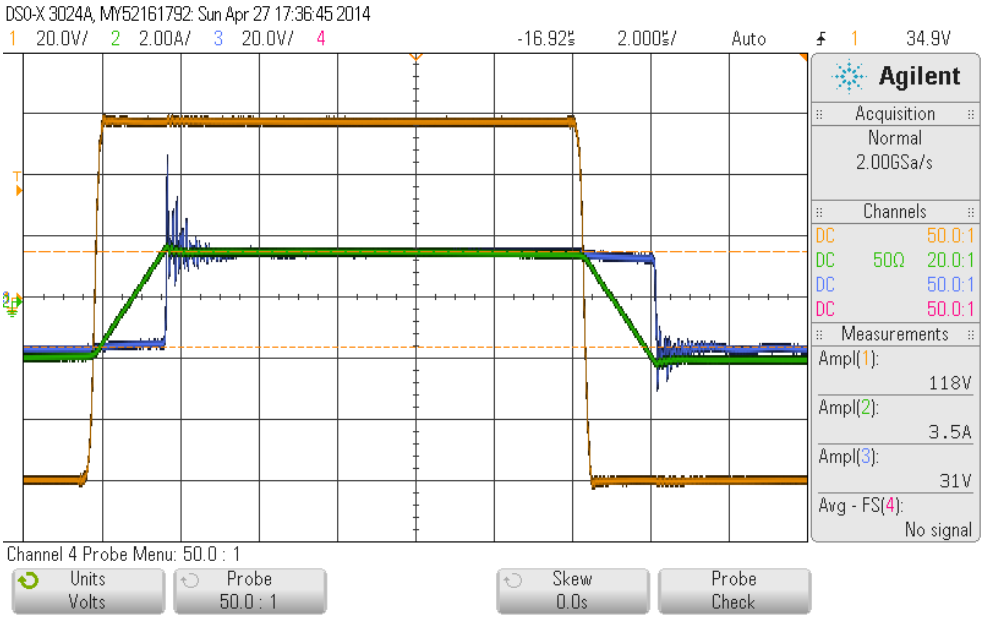

Fig. 6-21- Charging low voltage battery from dc source, V_{in}=59.6 V, ϕ=30^{o}, coupled ac inductor, yellow: V_{ac1}, blue: V_{ac2}, green: $I_{ac(pri)}$

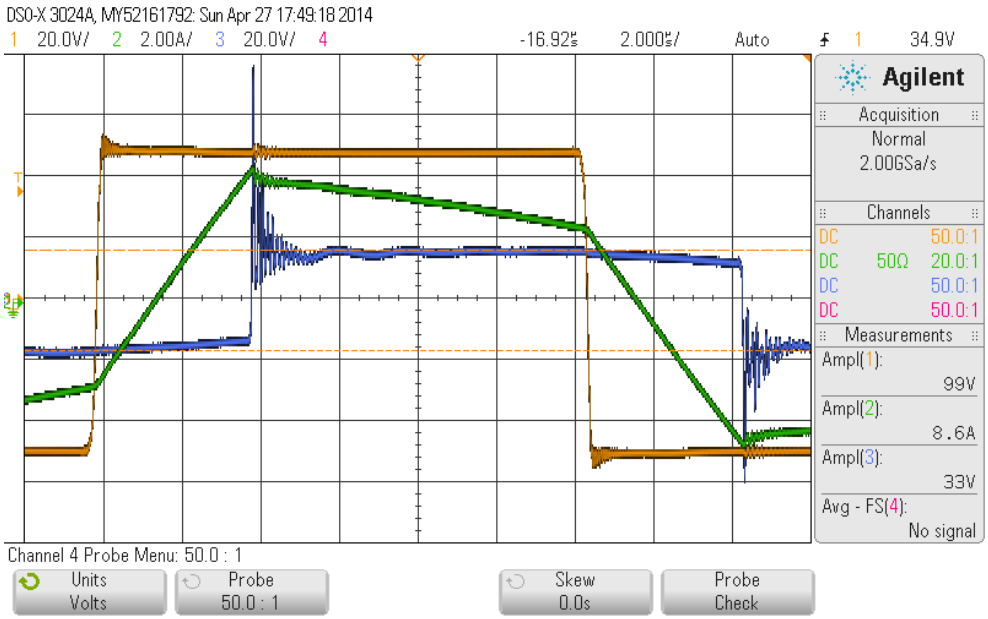

Fig. 6-22- Charging low voltage battery from dc source, V_{in}=50 V, ϕ=60^o, coupled ac inductor, yellow: V_{ac1}, blue: V_{ac2}, green: $I_{ac(pri)}$

6.4.2. Charging 48 V Battery from Laboratory Supply

Due to the hesitations explained in subsection 6.2.3, the dc voltage is not raised to 180 V in this case study. Instead, the transformer is removed to relate the case study explained in the subsection 6.3.2 where the 48 V battery was charged from the grid. The coupled ac inductor is between the bridges in this case study.

Initially, the input voltage is 48 V and the phase shift is 20^o. The waveforms are clean as shown in Fig. 6-23 similar to the subsections 4.4.1 and 6.3.2. The input voltage is increased to 55 V and the waveforms are still clean. The voltage is decreased to 48.3 V and voltage spike appears in the primary voltage as shown in Fig. 6-24. In Fig. 6-24, the current is too low. The phase shift is increased to 60^o with 10^o steps. At 60^o phase shift, the input is decreased from 48 V (Fig. 6-25) to 33.3 V (Fig. 6-26). In Fig. 6-26 the

waveforms are still clean since the ac link current is high enough to maintain the soft switching region. The experiments measurements are listed in Table 6-10. The efficiencies approach 94% as the power level is about the 10% of the nominal power.

Table 6-10- Charging 12V Battery from Laboratory Supply

V_{in} [V]	I_{in} [A]	V_{out} [V]	I_{out} [A]	ϕ [^{o}]	Pin [W]	Pout [W]	η [%]
50	1.25	52.4	1.0	20	62.50	52.40	83.84
55	1.1	54.0	1.2	20	60.50	64.80	107.11
48.3	1.16	53.1	0.9	20	56.03	47.79	85.30
52	2.09	55.2	1.7	30	108.68	93.84	86.35
52	2.73	56.2	2.2	40	141.96	123.64	87.09
52	3.3	56.7	2.7	50	171.60	153.09	89.21
48	3.21	55.5	2.5	50	154.08	138.75	90.05
48	3.61	55.5	2.8	60	173.28	155.40	89.68
33.3	3.44	53.5	2	60	114.55	107.00	93.41

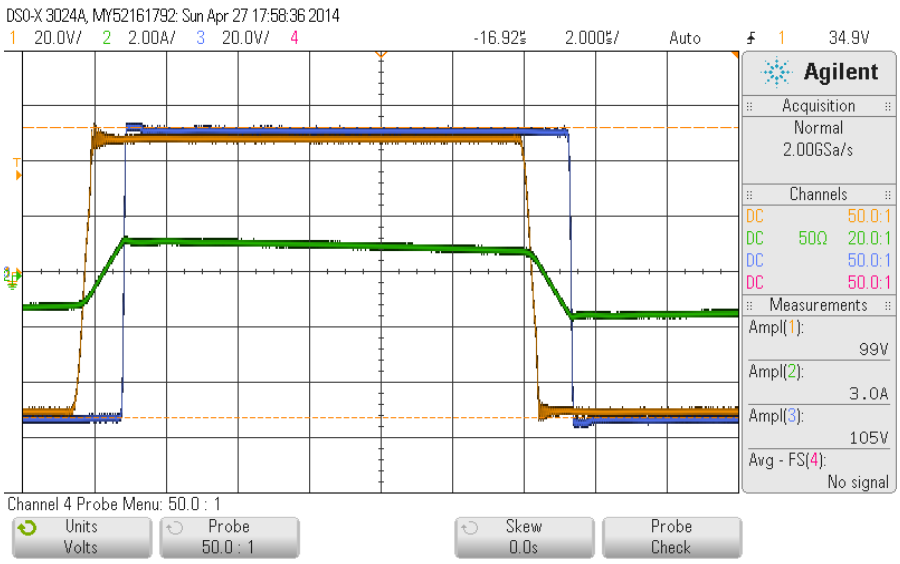

Fig. 6-23- Charging 48 V battery from dc source, V_{in}=50 V, ϕ=20^o, coupled ac inductor, yellow: V_{ac1}, blue: V_{ac2}, green: $I_{ac(pri)}$

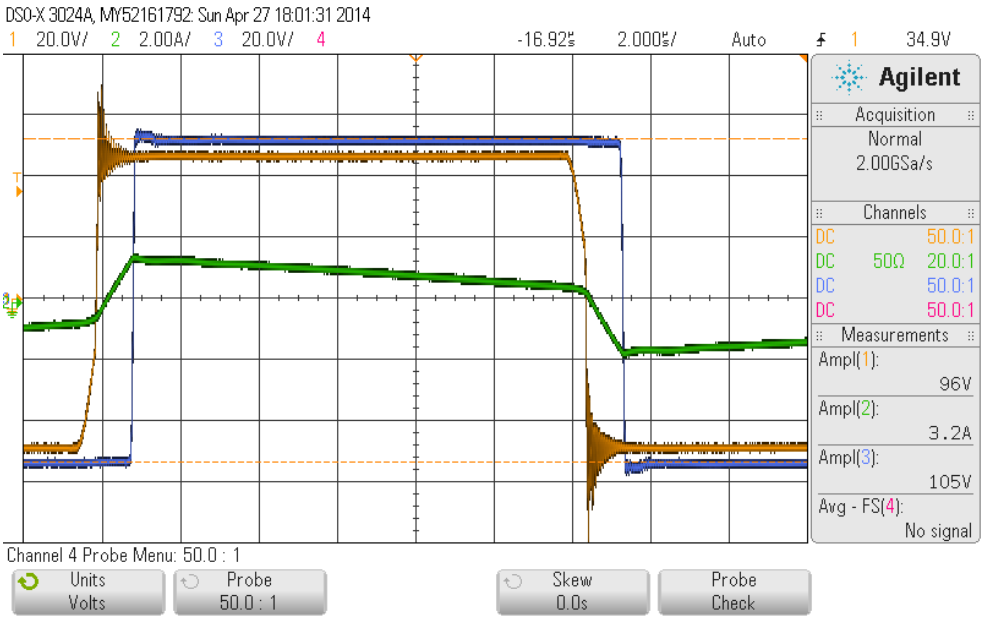

Fig. 6-24- Charging 48 V battery from dc source, V_{in}=48.3 V, ϕ=20^{o}, coupled ac inductor, yellow: V_{ac1}, blue: V_{ac2}, green: $I_{ac(pri)}$

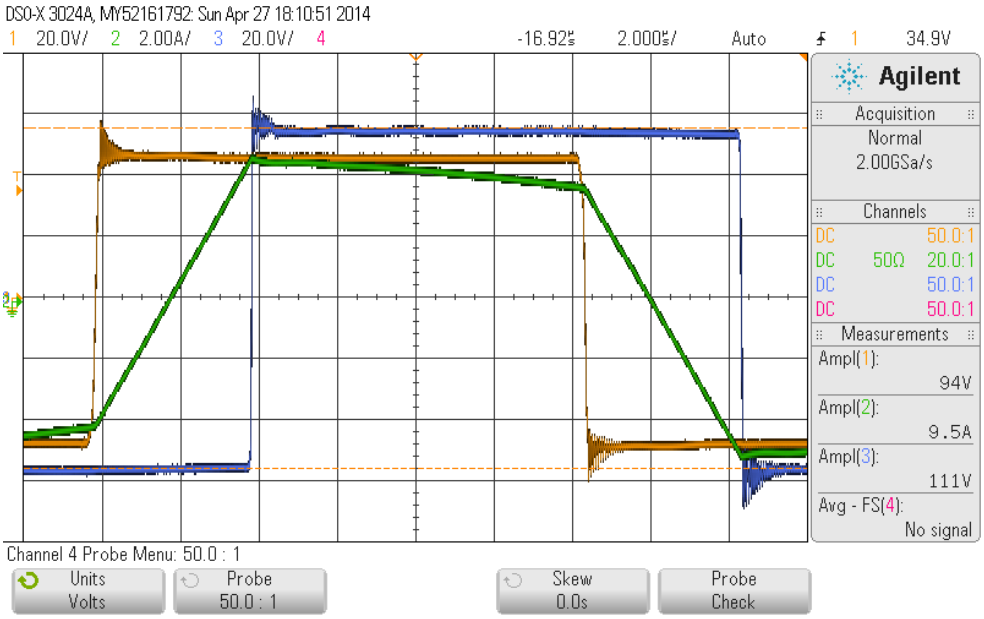

Fig. 6-25- Charging 48 V battery from dc source, V_{in}=48 V, ϕ=60^{o}, coupled ac inductor, yellow: V_{ac1}, blue: V_{ac2}, green: $I_{ac(pri)}$

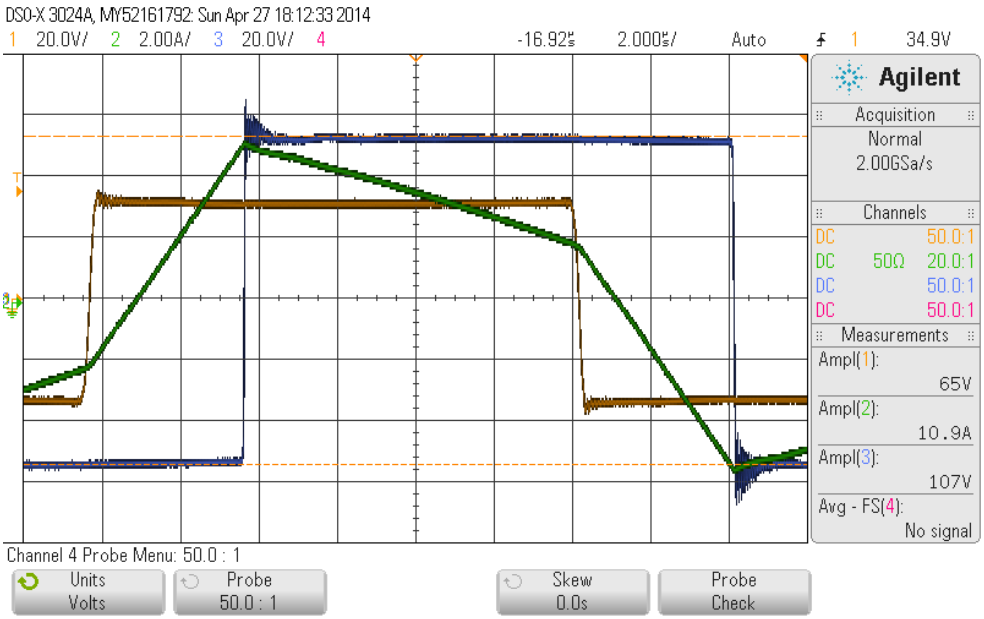

Fig. 6-26- Charging 48 V battery from dc source, V_{in}=33.3 V, ϕ=60^o, coupled ac inductor, yellow: V_{ac1}, blue: V_{ac2}, green: $I_{ac(pri)}$

6.5. Energy Exchange Between Batteries

In this experiment, the high voltage battery is located at the primary side and the low voltage battery is located at the secondary side. The gapped inductor L is located at the primary side. The total series inductance is 50 µH. The h-bridges are the earlier version with 300 V IXYS switches. The phase shift is changed from 10^o to 65^o and the measurements are listed in Table 6-11. The ac link waveforms are captured with the oscilloscope. The snapshots for 25^o, 35^o, 45^o, and 65^o phase shift are shown in Fig. 6-27 to Fig. 6-30. The VPC is able to exchange power between batteries. This verifies an extensive functionality of the proposed multi port VPC for integrating sources in a vehicular integrated power system.

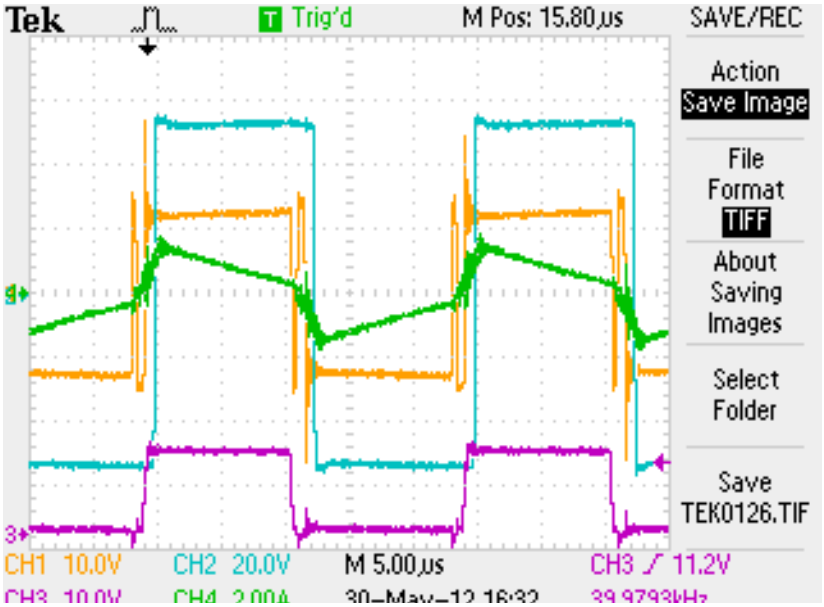

Fig. 6-27- Ac link waveforms during power transfer from 12 V battery to 48 V battery, $\phi = 25^{o}$

yellow: V_{ac1}, blue: V_{ac2}, green: I_{Lac}, magenta: $V_{gs(M11)}$

Table 6-11- Power Transfer from Low Voltage Battery to High Voltage Battery

V_{in} [V]	I_{in} [A]	V_{out} [V]	I_{out} [A]	ϕ [^{o}]	Pin [W]	Pout [W]	η [%]
12.79	0.12	51.4	0.011	10	1.53	0.57	36.84
12.65	1.519	51.6	0.345	20	19.22	17.80	92.64
12.58	3.085	51.9	0.66	25	38.81	34.25	88.26
12.53	4.84	51.9	0.99	30	60.65	51.38	84.72
12.47	6.43	52.3	1.26	35	80.18	65.90	82.19
12.46	7.28	52.6	1.40	40	90.71	73.64	81.18
12.45	7.99	52.6	1.47	45	99.48	77.32	77.73
12.43	8.65	53.0	1.53	50	107.52	81.09	75.42
12.42	9.25	52.9	1.57	55	114.89	83.05	72.29
12.41	9.8	52.9	1.60	60	121.62	84.64	69.59
12.39	10.28	53	1.64	65	127.37	86.92	68.24

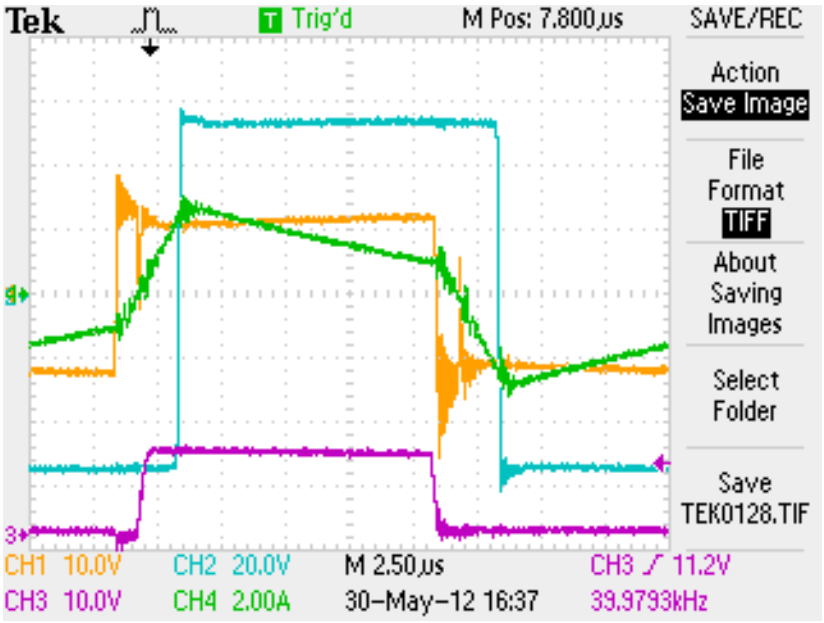

Fig. 6-28- Ac link waveforms during power transfer from 12 V battery to 48 V battery, $\phi = 35^{o}$

yellow: V_{ac1}, blue: V_{ac2}, green: I_{Lac}, magenta: $V_{gs(M11)}$

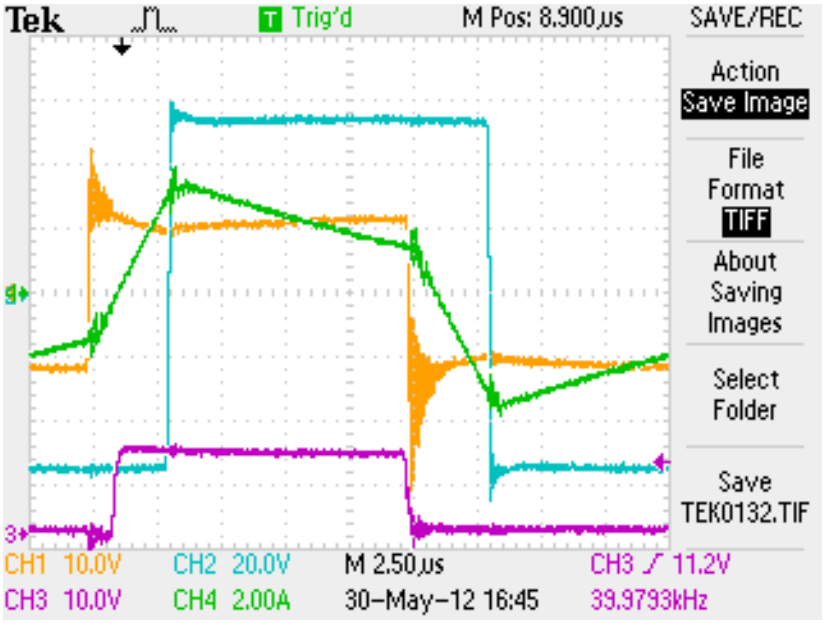

Fig. 6-29- Ac link waveforms during power transfer from 12 V battery to 48 V, $\phi = 45^{o}$

yellow: V_{ac1}, blue: V_{ac2}, green: I_{Lac}, magenta: $V_{gs(M11)}$

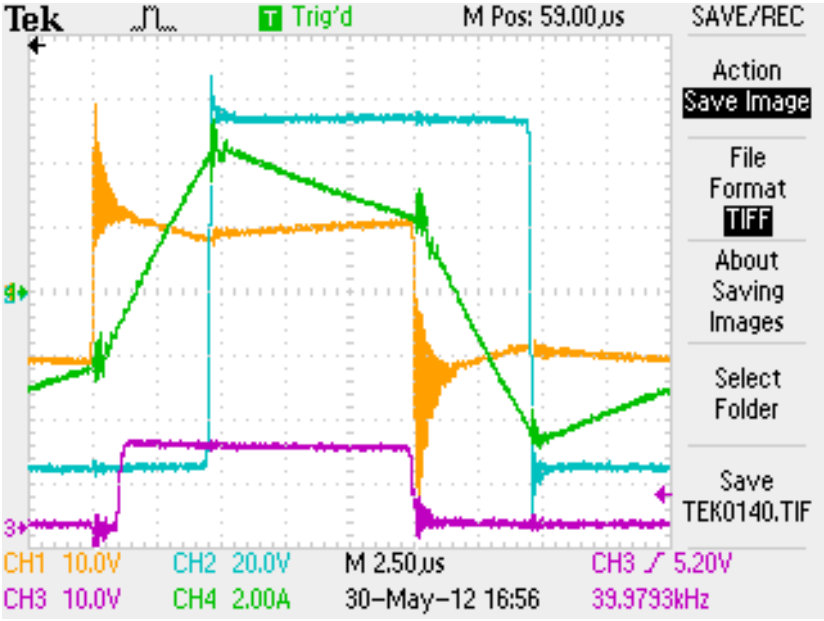

Fig. 6-30- Ac link waveforms during power transfer from 12 V battery to 48 V, $\phi = 65^{o}$

yellow: V_{ac1}, blue: V_{ac2}, green: I_{Lac}, magenta: $V_{gs(M11)}$

6.6. Conclusion

The experimental setup was configured to evaluate the performance of the components designed through the dissertation. Initially, 600 V, 150 V and 40 V developed h-bridges were tested in a DAB configuration. The DAB was operated with the variable input from 30 V to 180 V and a 25.1 Ω resistive load at the output. The importance of the proper dc capacitor design and proper dead time selection for DAB were emphasized by the presented case studies.

The main functionality of VPCs is charging the batteries. Both 12 V and 48 V batteries were charged from the grid through the dc link for proving the capability of the proposed VPC topology. The experiments with presence of the double frequency ripple verified the dissertation's contribution on modeling DAB commutations that were

presented in the third chapter. These experiments emphasized on the relation of dead time and minimum current with the soft switching region of DAB converter when the phase shift modulation is employed.

The batteries were also charged using the high voltage laboratory power supply. The results observed during charging the batteries through the grid were verified by repeating the results using the laboratory voltage source. Using the laboratory voltage source, the measurements are more accurate as the double frequency ripple does not exist.

The effect of the multiwinding capacitive components on DAB commutation was discussed in the fourth chapter. This discussion was supported through the experiments charging the batteries. Both set of experiments for charging the batteries, using the grid and the laboratory power supply, agree with the statements made regarding the parasitic capacitors of the multiwinding transformer in series ac link power converters.

The energy exchange between the batteries is among the functionalities of proposed vehicular integrated power system. The experiments demonstrated the energy exchange between the batteries in order to approve the validity of the proposed extensive VPC for the vehicular integrated power system.

7. CONCLUSION AND FUTURE WORK

This dissertation proposed a design procedure for Vehicular Power Conditioners (VPCs). The novel contributions of this dissertation will be summarized in this chapter. Suggestions for future research will be included at the end of this chapter.

A conceptual design approach was explained in the introduction chapter. The design approach synthesized the VPC's power converter topologies according to power conditioning needs. Examples of the derived power converter topologies were reviewed. Among derived topologies, there were novel topologies that had not previously been investigated, including the parallel and the hybrid series parallel ac link multiport VPCs.

High frequency isolation is a key feature in developing VPCs. The ac link utilization factor was defined in this dissertation as the ratio of the average power to the maximum power passed through the ac link. The isolated power converter topologies were compared according to the calculated ac link utilization factor. It was analytically demonstrated that the suggested ratio is an index that reveals the VPC's relative power density.

A futuristic view of the sources and loads that would be employed in a vehicular power system suggested evolving VPC by interconnecting all the vehicle's sources and loads into a vehicular integrated power system.

In the second chapter, the VPC's grounding schemes were investigated. The SAE standards suggest having an interface between the charger and the grid. This dissertation suggested integrating this interface into the onboard VPC. The relation between galvanic

isolation and safety concerns were evaluated. A novel high impedance grounding scheme was suggested that contributes to the cost reduction of the level-one VPCs and the prevalence of PHEVs and EVs. The proposed contributions to the grounding schemes and safety concerns were verified through simulations.

A three-port onboard VPC was introduced in the third chapter as the reference design for developing the simulation test bed and the experimental setup. The reference VPC was implemented with the three-stage isolated VPC. Additionally, the extension of this VPC was investigated employing three-port series ac link topology. The three-stage isolated VPC includes three power conditioning stages including the line side bridge, the middle bridge, and the battery bridge. The three-port variation was extended through the isolation transformer and the low voltage battery bridge was added to the VPC. A design procedure was introduced for the ac-dc line side bridge as well as the isolated dc-dc converter. The Dual Active Bridge (DAB) and multi active bridge were the adopted power converter topologies for the VPC's dc-dc power converter.

The Snubberless DAB converter was investigated in the third chapter. The design considerations of the Snubberless DAB were highlighted. This dissertation's contribution on the DAB design is the piecewise linear modeling of the Snubberless DAB. In earlier works, a turn-off snubber or single capacitor were assumed analyzing the DAB commutation. In practice, using turn-off snubbers are not feasible. The Snubberless DAB utilizes the nonlinear output capacitors of the switches as the turn off snubbers for the commutations. The proposed piecewise linear model of the output capacitors related the physical characteristics of the switches to the DAB commutation.

The analyses revealed the role of the switching dead time to the DAB commutation. The analyses were verified through experiments.

The optimized design approach for the VPC's magnetic circuit was presented in the fourth chapter. Three design approaches were suggested for implementing ac inductors. The gapped ac inductor and the novel coupled ac inductor design procedures were developed for the series high frequency ac link converters. The proposed coupled ac inductor integrates a zero blocking transformer into the coupled ac inductor design that reduces the common mode interference in the VPC. The implemented prototypes were verified through the experimental setup.

Low voltage batteries on vehicular systems demand high frequency and high current power conditioning stages. The magnetic circuit needs conductor planes such as copper foils or bus bars as windings. These winding types introduce more parasitic capacitances to power converters. The implemented multiwinding transformer used copper foils for the battery side windings. The experiments demonstrated the effect of the transformer's parasitic capacitors in the DAB operation. An experimental modeling procedure was proposed in the fourth chapter that models the capacitive elements of the multiwinding transformers. The previous modeling methods had used the resonance frequency or the step response of the transformer when the windings were open circuit. The earlier methods resulted an approximate stray capacitance, which is an equivalent of all the stray capacitances at the measured winding. In contrast, the novel modeling method suggested in this dissertation uses the short circuit resonance frequency of the transformer's windings. This method is able to model the stray capacitance of each

winding separately. The benefit of the proposed modeling method is mandatory from the design perspective for multiwinding transformers. The parasitic capacitor of each winding can be modeled separately with this modeling method. The proposed modeling approach was applied to the developed three-winding transformer and the winding capacitances were measured. The proposed model was further simplified mathematically into a third order Π equivalent circuit that was transferable to any desired winding side. The system step response was analyzed in the frequency and time domains. According to the mathematical analysis, the transformer's step response has lower ringing and lower overshoot at higher loads and lower parasitic capacitances. The accuracy of the mathematical analysis was verified through simulations and experiments. The accordance of the results among the mathematical analysis, simulations, and experimental results verified the accuracy of the experimental modeling method as well as the mathematical analysis.

The validity of closed loop control routines were verified through the simulation test bed in the fifth chapter. The dc link was controlled with a slow PI controller. The charger mode controller employed a Power Factor Correction (PFC) controller that modifies the line bridge to a hybrid active rectifier. The dead-beat controller was investigated for the V2G operation. The current controller's behavior was fast with acceptable THD at different operating points. The line filter and the controller parameters were tuned according to the case studies. The preliminary investigation suggested a design trend for improving the dead-beat controller's performance by adjusting the dead-beat current controller's time constant to a value slower than the

physical time constant. The V2H controller proposed to engage a voltage controller with the deadbeat controller. All the controllers were verified through different case studies at several operating points. The controllers' transient behaviors were evaluated with the step response and ramp response analyses. The simulations approved the performance of the adopted control solutions.

In the sixth chapter, the experiments performed with the experimental setup were reported. The majority of the case studies were already used through the dissertation; however, more detailed results were presented in the sixth chapter to enhance following the research in future. Different case studies verified the practicality of the proposed power conditioning method. The case studies included supplying resistive load, charging batteries from the grid and laboratory power supply, and exchanging energy between the batteries. The challenges in DAB operation were highlighted and the practicality of the proposed hardware validated experimentally in the sixth chapter.

The suggestions to continue the research include employing the parallel ac link converters for VPCs as well as implementing the novel hybrid series parallel multiport configuration. These topologies can be approached from design, control, and application perspective.

The idea of the vehicular integrated power system was introduced and the capable hardware was implemented in this dissertation. The energy management using the proposed hardware was not discussed in this dissertation. The energy management strategies can be investigated from the control perspective and the power system automation perspective. Additionally, designing VPC for the vehicular integrated power

system from the reliability perspective needs to be researched in future. Fault prognoses analyses would potentially help growing the vehicular integrated power system concept for fault tolerant applications.

The proposed integrated ac link converter integrated the common mode blocking feature into the series ac inductance. Reducing common mode interference is very important for the grid connected applications. Further details need to be investigated with a researcher specialized in EMI and EMC for power electronics. The suggested research will also need laboratory facilities including spectrum analyzer, EMI probes, Line Impedance Stabilization Network (LISN), and impedance analyzer.

The experimental results emphasized the problematic operating points of the DAB. The challenges regarding these operating points are subject of the future research for academia and industries who intend to commercialize the high power density series ac link converters.

The proposed transformer experimental modeling approach can be practiced for various magnetic circuit geometries including planar and memes magnetism for various applications that deal with resonant and soft switching high frequency power converters.

The adopted control routines can be compared with other available control techniques for the VPC application. The researchers will need to fully access the grid. Experimental results are needed to verify such comparisons.

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