LOW-POWER WIRELESS MEDICAL SYSTEMS AND CIRCUITS FOR INVASIVE AND NON-INVASIVE APPLICATIONS

A Dissertation

by

JESUS EFRAIN GAXIOLA-SOSA

Submitted to the Office of Graduate and Professional Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

Chair of Committee,	Kamran Entesari
Committee Members,	Edgar Sanchez-Sinencio
	Arum Han
	James Moore
Head of Department,	Chanan Singh

May 2014

Major Subject: Electrical Engineering

ABSTRACT

Approximately 75% of the health care yearly budget of public health systems around the world is spent on the treatment of patients with chronic diseases. This, along with advances on the medical and technological fields has given rise to the use of preventive medicine, resulting on a high demand of wireless medical systems (WMS) for patient monitoring and drug safety research.

In this dissertation, the main design challenges and solutions for designing a WMS are addressed from system-level, using off-the-shell components, to circuit implementation. Two low-power oriented WMS aiming to monitor blood pressure of small laboratory animals (implantable) and cardiac-activity (12-lead electrocardiogram) of patients with chronic diseases (wearable) are presented. A power consumption vs. lifetime analysis to estimate the monitoring unit lifetime for each application is included. For the invasive/non-invasive WMS, *in-vitro* test benches are used to verify their functionality showing successful communication up to 2.1 m/35 m with the monitoring unit consuming 0.572 mA/33 mA from a 3 V/4.5 V power supply, allowing a two-year/88-hour lifetime in periodic/continuous operation. This results in an improvement of more than 50% compared with the lifetime commercial products.

Additionally, this dissertation proposes transistor-level implementations of an ultra-low-noise/low-power biopotential amplifier and the baseband section of a wireless receiver, consisting of a channel selection filter (CSF) and a variable gain amplifier (VGA). The proposed biopotential amplifier is intended for electrocardiogram (ECG)/

electroencephalogram (EEG)/ electromyogram (EMG) monitoring applications and its architecture was designed focused on improving its noise/power efficiency. It was implemented using the ON-SEMI 0.5 µm standard process with an effective area of 360 μm^2. Experimental results show a pass-band gain of 40.2 dB (240 mHz - 170 Hz), input referred noise of 0.47 µVrms, minimum CMRR of 84.3 dBm, NEF of 1.88 and a power dissipation of 3.5 µW. The CSF was implemented using an active-RC 4^{th} order inverse-chebyshev topology. The VGA provides 30 gain steps and includes a DC-cancellation loop to avoid saturation on the sub-sequent analog-to-digital converter block. Measurement results show a power consumption of 18.75 mW, IIP3 of 27.1 dBm, channel rejection better than 50 dB, gain variation of 0-60dB, cut-off frequency tuning of 1.1-2.29 MHz and noise figure of 33.25 dB. The circuit was implemented in the standard IBM 0.18 µm CMOS process with a total area of 1.45 x 1.4 mm^2.

The presented WMS can integrate the proposed biopotential amplifier and baseband section with small modifications depending on the target signal while using the low-power-oriented algorithm to obtain further power optimization.

DEDICATION

To my parents: Lupita and Efrain, siblings: Sac-Nicte, Jose Luis, Diego and Rodrigo; grandparents: Nide and Jose, the rest of my family, all my friends, and to Cynthia.

ACKNOWLEDGEMENTS

I would like to thank my advisor, Dr. Kamran Entesari, for his support through all these years. His constant advice and guidance helped me grow not only as student but as a person. I am deeply grateful for the way he always challenged me and made me put that little extra effort that ended up making a big difference.

I also want to thank Dr. Edgar Sanchez-Sinencio for inviting me to become part of the Analog and Mixed-Signal Center (AMSC), for his professional and academic advice, and for his friendship. I want to express my appreciation to Dr. Arum Han and Dr. James Moore for being part of my graduation committee, for their comments and suggestions to improve the quality of this research.

My deepest gratitude to my parents, siblings and all the members of my family: grandparents, uncles, aunts and cousins. Their constant support, prayers and unconditional love were always a permanent source of inspiration.

Special thanks to my friends and colleagues at the AMSC for fruitful discussions and long periods of team work. Thanks to Salvador, Carlos, Alfredo, Felix, Jesse, Hajir, Jiayi, Adrian, Jorge, Joselyn, Reza, Marcos, Chengliang, Javier, Moises and Fernando. I also want to thank William, Renan, Alex, Luis Miguel, Jorge B., Ana Karen, Alvaro and all my childhood and college friends, for their friendship and support.

Many thanks to Ella, Tammy, the ECE department staff members and the Sponsored Student Programs Office staff for all their help and support.

I would like to thank my professors from Instituto Tecnologico de Merida, Professor Johan Estrada Lopez, Professor Ramon Atoche Enseñat and Professor Victor Sandoval Curmina for all their patience, support and encouragement.

I am deeply indebted to the Mexican National Council for Science and Technology (CONACYT) for providing me with economic support during most of the doctoral program.

Finally, I want to thank Cynthia for her unconditional love, kindness, enduring support and for being a continuous source of inspiration for my academic and personal life.

NOMENCLATURE

ADC	Analog-to-Digital Converter
AFE	Analog Front-End
ASIC	Application Specific Integrated Circuit
BS	Base Station
CMRR	Common-Mode Rejection Ration
CPU	Central Processing Unit
DMA	Direct Memory Access
ED	End Device
FCC	Federal Communications Commission
FSK	Frequency Shift Keying
GUI	Graphical User Interface
IA	Instrumentation Amplifier
IC	Integrated Circuit
IMD	Implantable Medical Device
ISM	Industrial Scientific and Medical
ISR	Interrupt Service Routine
LNA	Low Noise Amplifier
LO	Local Oscillator
MAC	Media Access Controller
MCU	Microcontroller

MICS	Medical Implant Communication Service
OOK	On/Off Key
OSR	Oversampling Ratio
PA	Power Amplifier
PSoC	Programmable System on Chip
RAM	Random Access Memory
SAR	Successive Approximation Register
SPI	Serial Peripheral Interface
USB	Universal Serial Bus
WMS	Wireless Medical System

TABLE OF CONTENTS

Page

Page

Page

Page

LIST OF FIGURES

Page

Page

Page

Page

Page

LIST OF TABLES

Page

CHAPTER I

INTRODUCTION

Motivation

Public health systems of developed countries spend around 75% of their healthcare yearly budget on resources used to treat patients with chronic conditions such as heart/respiratory/oral related diseases, cancer, diabetes, arthritis and obesity among others [1-3]. Only in the U.S., these conditions lead the causes of death and disability, thus becoming a major concern and challenge within the medical community [4]. At the same time, recent advances in physiological research and complementary metal-oxide-semiconductor (CMOS) technology have resulted in significant progress on the medical, analog circuit design and wireless communications fields.

The imminent impact of chronic diseases along with the aforementioned boost on the medical and technological disciplines has given rise to the use of preventive medicine, embracing early detection efforts [4] and ambulatory monitoring for patients with existing conditions as their secondary and tertiary illness prevention stages [5]. Therefore, a major emphasis has been placed on prevention rather than on treatment, resulting in a high demand of wireless medical systems (WMS) able to provide reliable monitoring along with high accuracy diagnosis [6] for home care and short stays in health centers. Furthermore, the use of WMS is expected to lead patients and health care costumers to enhance rehabilitation, information and involvement in their own treatment[7]. Similarly, the use of WMS on preclinical studies aimed to determine

physiological and pharmacological issues has helped to reach key milestones on these fields.

Wireless Medical Systems Overview

The simplified block diagram of a typical WMS is shown in Fig. 1. The system includes an end device (ED) in charge of collect, digitize and wirelessly transmit the desired signal, a base station (BS) that receives the digital information and sends it to a graphical user interface (GUI) implemented in a personal computer (PC).

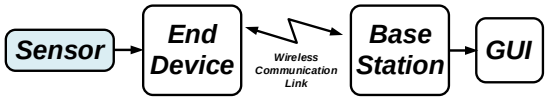

Fig. 1. Block diagram of a typical wireless medical system.

The sensor translates a specific physiological or biochemical parameter into an equivalent signal of another type of quantity, for example, an electrical or optical signal, acting as a transducer that converts the *measurand* (a quantity or a parameter) into a signal carrying the desired information [8]. The sensor enables the detection of biologic events through variations of the sensing element properties, thus becoming the interface between a biological system and the WMS.

Depending of the type of sensor, different interfaces are required to successfully acquire the signal of interest. For electrical sensors, a change on the *measurand* is reflected in a variation of a voltage, current or impedance. This variation is detected by an analog front-end (AFE) composed of an amplifier and an analog-to-digital converter (ADC) which in turn transfers the collected data to a microcontroller (MCU) or to a

digital signal processing (DSP) unit. This is illustrated in Fig. 2 where the last block consists of a wireless transceiver in charge of transmitting the information to the BS through a wireless communication channel. Depending on the application, the ED can be implantable (invasive) or wearable (non-invasive). In both cases, the main design concerns are size, power, cost and lifetime. Key aspects to deal with these challenges will be presented on this dissertation for invasive and non-invasive applications.

The BS acts as a gateway between the ED and the GUI. Fig. 3 presents a simplified block diagram of a typical BS and GUI. The BS consists of a wireless transceiver that handles the communication with the ED, an MCU or DSP and an interface, in this case universal serial bus (USB) channel, to communicate with the GUI.

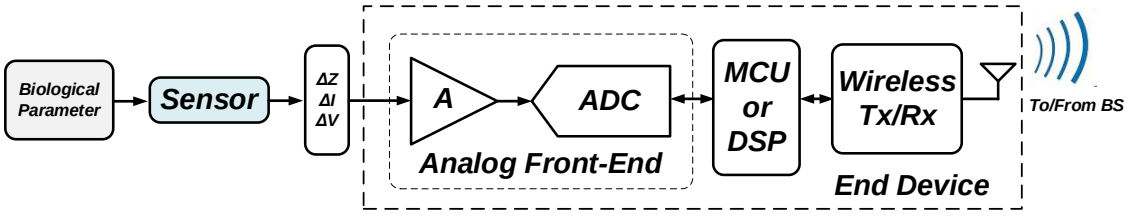

Fig. 2. Simplified block diagram of typical ED showing the interaction between a biological parameter and the sensor used to translate the *measurand* into an electrical signal.

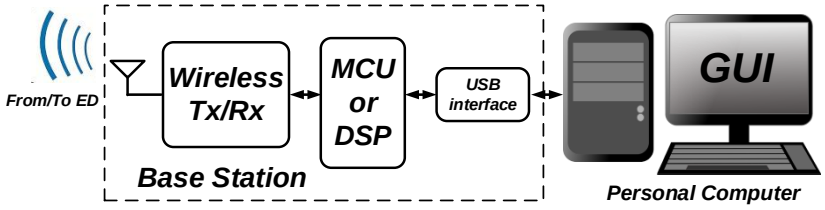

Fig. 3. Simplified block diagram of a typical BS with the GUI implemented in a personal computer.

The GUI is implemented in a personal computer and is in charge of storing the received data or sending it to a health care center or physician's office, depending on the application. In some cases, the user can modify the operation of the ED through the GUI, changing settings such as period of operation (for non-continuous monitoring systems) or signal resolution.

Dissertation Organization

The first and major part of this dissertation will present the design, implementation and testing of two low-power oriented WMS for invasive and non-invasive applications along with a fully integrated ultra-low-power low-noise biopotential amplifier for electrocardiogram (ECG)/ electroencephalogram (EEG)/ electromyogram (EMG) monitoring applications.

Chapter II presents a WMS to monitor the blood pressure of laboratory animals for drug safety research using an implantable medical device (IMD) as the ED unit. The implementation of the IMD provides general picture of design issues faced while implementing a WMS for implantable applications. The IMD and BS units are designed using on off-the-shelf integrated circuits. A low-power-oriented control algorithm aimed to optimize the current consumption of the IMD is introduced as the strategy to increase its lifetime. The main details regarding the analog front-end used for signal acquisition, the aforementioned low-power-oriented algorithm and an analysis of power consumption vs. lifetime are explained. Similarly, the main considerations for link budget calculations in implantable applications using the medical implant communication service (MICS) and are explained. Finally, the *in-vitro* test bench used to characterize the WMS

application and the obtained results are discussed.

In Chapter III, a wearable WMS intended for continuous cardiac-activity monitoring is presented. The WMS is proposed as mean to provide early detection and diagnosis of cardiac diseases, allowing physicians to identify abnormalities likely to progress and cause permanent damage. This WMS includes a more complex analog front-end consisting of 8-channels dedicated to the extraction of a standard 12-lead ECG. The system is also implemented using off-the-shelf components and although the size/power specs are relaxed, the required range of operation is more demanding (about 30 to 35 m). The WMS uses an RF link that operates in the industrial, scientific and medical (ISM) band at 2.45 GHz. The main design considerations, implementation challenges, the *in-vitro* test bench and measured results are discussed.

Chapter IV presents a fully integrated integrated ultra-low-noise/low-power biopotential amplifier for electrocardiogram ECG/EEG/EMG applications. First, the main design concerns for biopotential acquisition are presented. Then, a literature review summarizing the existing solutions provides an overview of the current trends and challenges on biopotential amplifier's design. The architecture of the bioamp is then presented, including a fully-differential OTA with chopper modulators at its input and output in order to reduce the effect of the OTA's 1/f noise/systematic offset. Also, a feedback network consisting of capacitors and a high resistance implemented by a T-network composed of MOS-bipolar pseudo resistors and a triode-region transistor is used to obtain a high-pass cut-off frequency in the mHz range without the need of external components. Finally, a negative capacitance is introduced to boost the OTA's

input impedance and preserve the negative feedback properties of the bioamp. The measured results of the bioamp fabricated using 0.5 μm CMOS technology and the test bench designed for the circuit characterization, including the considerations for noise performance measurements, are discussed.

Chapter V is dedicated to the system-level design and transistor-level implementation of the baseband section of an extravehichular activity (EVA) radio receiver. EVA is commonly known as spacewalk and allows astronauts to conduct experiments in the space shuttle's payload bay, to test new equipment in space and to repair satellites in orbit. These tasks demand versatile radio systems with high levels of integration, low power consumption, light weight and small volume, characteristics shared with RF transceivers used by WMS. In both applications, EVA and WMS, the radios transmit/receive information (audio/video and physiological signals respectively) through frequency bands (S-band and ISM/MICS band) used by other services, resulting in a crowded spectrum that includes undesired spectral content (blockers) that may limit the dynamic range of the receiver. This chapter starts discussing the specifications for the EVA radio receiver. The architecture used to implement the baseband section, consisting of a channel selection filter and a variable gain amplifier designed to reduce the effect of blockers on the EVA radio receiver, effectively increasing its overall linearity. The circuits were implemented in 180 nm CMOS technology and the measurement results including frequency response, noise and linearity are presented. Due to the similarities between the two applications, the presented topology can be used to implement the baseband section for an ISM/ MICS band receiver.

Finally, Chapter VI concludes the discussion about the proposed WMS, the implemented biopotential amplifier and the baseband circuit for EVA radio presented in this dissertation.

Research Contribution of this Dissertation

This dissertation provides insight for the design and implementation of WMS starting from the system level point of view and concluding with the transistor-level implementation of blocks relevant specifically to the signal acquisition and radio frequency signal reception. A design methodology aimed to optimize the design time and power consumption of wireless medical systems for implantable [9] and non-implantable [10] [11] is presented. The proposed biopotential amplifier architecture [12] improves the noise power efficiency of the first element on the analog acquisition stage of a WMS while the implemented channel selection [13] and VGA topologies effectively increase the linearity of the radio receiver they are part of.

The presented low-power-oriented algorithm and life-time vs. power analysis complement each other providing an accurate estimation of the ED power performance along with a fast design and debugging process. The *in-vitro* measurements reported in this dissertation demonstrate that the proposed methodology can be used for the implementation of wearable or implantable WMS, allowing the designer to experiment/debug the main issues that would be found by the final version of the ED.

The architecture of the presented ultra-low-noise/low-power biopotential amplifier can be used to implement analog front-ends for other low frequency signals sensitive to flicker noise with reduced power consumption thus improving the power

performance of the required application without compromising the quality of the acquired signal.

Finally, the results for the implemented channel selection filter and variable gain amplifier demonstrate strong rejection to in-band blockers present on the band of interest for the giving receiver, resulting in an increase of the sensitivity of the system. Although the circuit was designed for an EVA radio receiver, the same architecture can be applied for an ISM band radio, currently used by a diverse set of radio systems and therefore very sensitive to the presence of in-band blockers.

The results obtained from the different techniques presented on this work invokes interest from the industry/academia as a way for fast prototyping/defining educational projects based on the proposed WMS design methodology. Additionally, this work demonstrates the feasibility of using long-channel silicon-based technologies for implementing biopotential acquisition circuitry keeping low power consumption while optimizing the integrity of the amplified signal.

CHAPTER II

A WIRELESS MEDICAL SYSTEM PROTOTYPE FOR IMPLANTABLE APPLICATIONS*

Introduction

Advances in medical technology have allowed physicians to improve the patients' quality of life through the use of wireless medical systems (WMS) aimed to provide reliable monitoring and high accuracy diagnostics [6]. A typical WMS includes an end device (ED) and a base station (BS) complemented by a graphical user interface (GUI) implemented in a computer [10]. The ED is in charge of collecting information about a specific physiological or biochemical parameter while the BS acts as a gateway between the ED and the GUI. Depending on the application, the ED can be wearable (non-invasive) or implantable (invasive) and the WMS can be targeted to complement the patient's treatment or as part of a research study.

The main issues related with the implementation of such systems are size, cost and lifetime, especially when the monitoring unit is an implantable medical device (IMD) [14]. Key solutions to these issues are the selection of the right hardware along with the use of a smart software control algorithm to optimize the power consumption. In terms of hardware, designers have three main options to choose from: application specific integrated circuits (ASICs), programmable systems on chip (PSoCs) and off-the-

*©[2013] IEEE. Reprinted, with permission, from "A wireless medical system prototype for implantable applications," by J. E. Gaxiola-Sosa and K. Entesari, in 2013 *IEEE Fourth Latin American Symposium on Circuits and Systems (LASCAS)*, 2013, pp. 1-4.

shelf components. ASICs offer the highest level of innovation, small size and the best power performance. However, their design implies high cost and long development periods. Programmable SoCs provide some design flexibility, modest cost and relatively fast implementation. Nevertheless, system optimization is limited to the performance of each individual block. Finally, the use of commercial ICs allows fast prototyping while keeping a low price, but the size and power consumption of the system become restricted by the characteristics of the chosen components. Regarding the software, power optimization can be achieved by using only a microprocessor core in ASICs and PSoCs instead of a complete microcontroller (MCU), as in the off-the-shelf case. Taking this into consideration, careful analysis of the application, available resources and time restrictions should be done in order to determine the optimum way to implement the WMS.

This chapter presents a WMS prototype intended for implantable applications. The implantable unit design takes advantage of the qualities of the three hardware options mentioned before while minimizing the cons that come along with each of them, resulting in a fully programmable system-on-board. The presented BS allows power optimization of the IMD radio through the use of two different radio bands for wake-up and data transmission.

The aim of the system is to monitor the blood pressure of laboratory animals for drug safety research. However, the approach employed in this study can be used to implement an IMD targeted to monitor other physiological or biochemical parameters such as pH, temperature, phosphorus-based blood gases, etc. Moreover, the WMS

includes the option of modifying the signal resolution and frequency of data collection according to the specific needs of the user.

This chapter starts with a discussion of the design and implementation of the WMS. Then, the IMD low-power-oriented control algorithm and the IMD power vs. lifetime analysis are explained. Finally, the obtained results are presented.

System Design and Implementation

A block diagram of the WMS, including simplified versions of the IMD and the BS, is presented in Fig. 4. Both units are based on two off-the-shelf integrated circuits (ICs) intended for ultra-low-power applications: the Texas Instruments MSP430FG4618 [15], a mixed-signal MCU; and the Microsemi (formerly Zarlink) ZL70101 [16], a medical implantable radio transceiver. The MCU enables the design of a low-power-oriented control algorithm through its capability of shutting down peripherals that are not used at know time intervals. This provides PSoC characteristics to the IMD in the sense of power performance. The transceiver is an ASIC that operates at the medical implant communication service (MICS) band at 402 MHz-405 MHz to send/receive biological information/instruction-commands to/from the BS unit and includes an on-chip ultra-low power wake-up mechanism operating in the industrial, scientific and medical (ISM)

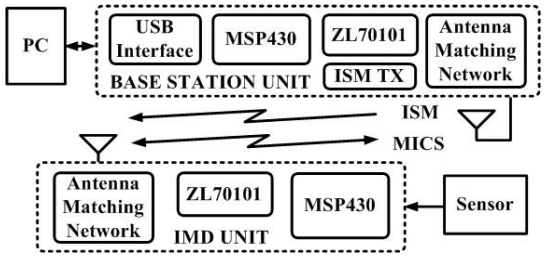

Fig. 4. Block diagram of the WMS.

band at 2.45 GHz to listen for a wake-up signal from the BS unit. The media access controller (MAC) of the transmitter allows it to operate as an extra MCU peripheral, enabling the integration of a system-on-board capable of supporting a software control algorithm to optimize the overall power consumption of the IMD.

The basic operation principle of the WMS can be summarized as follows: the BS transmits a wake-up signal to the IMD using the ISM band and the IMD replies with an acknowledge message using the MICS band. Once the link is established, further communications are handled using the MICS band. This frequency band is regulated by the Federal Communications Commission (FCC) for implantable biotelemetry applications [17]. After a given number of physiological measurements is stored in the IMD, the collected data is sent to the BS which in turn, will transmit it to the PC via universal serial bus (USB) connection. Once in the computer, the GUI allows the user to view the information in real-time and stores the samples in text files available for future analysis. In the next subsections the IMD and the BS unit are described in more detail.

Implantable Medical Device

The most critical section of the presented WMS is the IMD. A detailed block diagram describing its main components is presented in Fig. 4, including a MCU, a wireless transceiver, a dual-band matching network and a few external components such as bypass capacitors, crystal oscillators and resistors as part of the analog front-end (AFE).

Signal Acquisition and Analog-to-Digital Conversion

A sensor translates the physiological parameter into an electrical signal. The signal is injected into instrumentation amplifier (IA) built using the MCU's on-chip op amps and

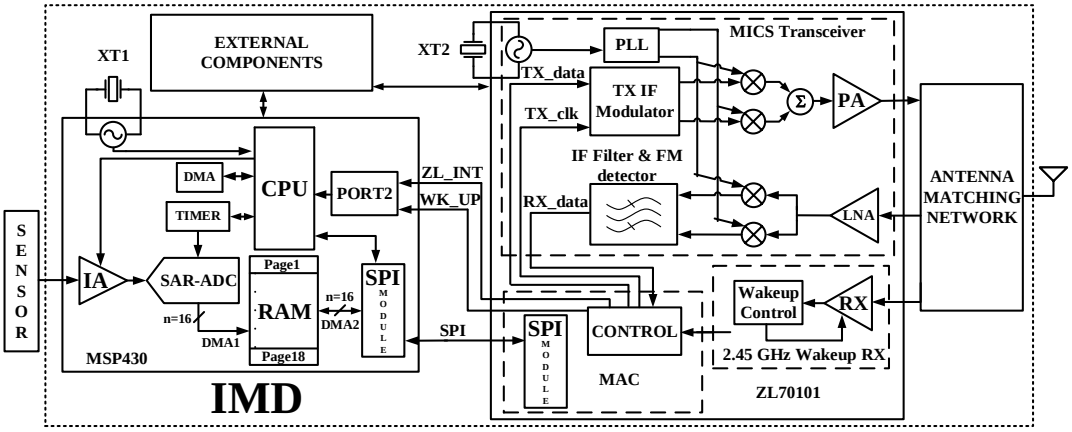

Fig. 5. Detailed block diagram of the IMD unit.

external passive components. The MCU has the ability to turn the op amps off when they are not being used, in order to reduce the power consumption of the IMD. A three op amp IA topology including an antialiasing filter is selected as the IMD's analog front-end and its schematic diagram is presented in Fig. 5. This IA implementation rejects electromagnetic and electrostatic interferences with a common-mode rejection ratio (CMRR) better than 80 dB [18-20]. The first stage of the IA is composed of two op amps in non-inverting configuration in order to provide high input impedance to the incoming differential signal. The second stage is configured as a difference amplifier [21] and includes an antialiasing filter to remove out of band interferences whose folding after the analog to digital conversion would corrupt the signal band [22]. The gain and cut-off frequency of the IA are given by eqs. (2.1) and (2.2). The external passive components used on the IA are: R1 (variable) = 0-250KΩ, R2 = 1MΩ, R3 = 200KΩ, R4 = 10MΩ and C = 1nF.

The output of the IA is connected to a 12-bit successive approximation register

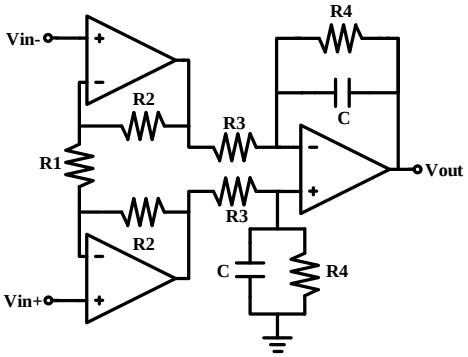

Fig. 6. A three op amp IA with embedded anti-aliasing filter.

$$V_{OUT} = (V_{IN+} - V_{IN-})\left(1 + \frac{2 \cdot R2}{R1}\right)\left(\frac{R4}{R3}\right) \tag{2.1}$$

$$f_{3dB} = \frac{1}{2\pi \cdot R4 \cdot C} \tag{2.2}$$

analog-to-digital converter (SAR-ADC), also included as part of the MCU. This module can be shut down after a conversion is completed and includes a buffer where the samples are stored before being sent to the random access memory (RAM) [15]. Since most physiological signals have similar bandwidths (from DC up to 250 Hz) [23, 24] and because of the low power features of the SAR-ADC topology [22], it is possible to modify the ADC's oversampling ratio (OSR) up to 30 in order to increase the accuracy of the conversion without compromising the power consumption. Having this relatively high OSR relaxes the specifications of the anti-aliasing filter and allows its integration by just adding external capacitors to the IA's second stage as showed in Fig. 6. The gains of the 1st and 2nd stages of the IA are 8 V/V and 50 V/V respectively, resulting in a total gain of 400V/V with a cut-off frequency of 15Hz. The cut-off frequency was

selected based on the bandwidth of the signal that will be monitored in this application, blood pressure of small animals.

Digital Communication and RAM Organization

Since the MCU has a 16-bit central processing unit (CPU) and the SAR-ADC has a 12-bit resolution, the 4 most significant bits of each stored sample are kept as reserved bits. The MCU's direct memory access (DMA) module uses a transfer channel (DMA1) to send the data from the ADC's buffer to the 8KB RAM with no CPU intervention [15]. The RAM is organized in 18 pages. Each page includes 217 words of 16 bits, and a data packet consists of 9 of these pages. When a data packet is ready to be transmitted, a second transfer channel of the DMA module (DMA2) sends the data to the serial peripheral interface (SPI) module. Again, no CPU intervention is needed to transport the information from the RAM to the SPI module, thus allowing reduction of the power consumption. Using the SPI module, the sampled data and control commands are transferred from the MCU and to the transceiver. The transceiver has its own SPI module and receives the 8-bit words sent by the MCU with a data rate of 2 mega

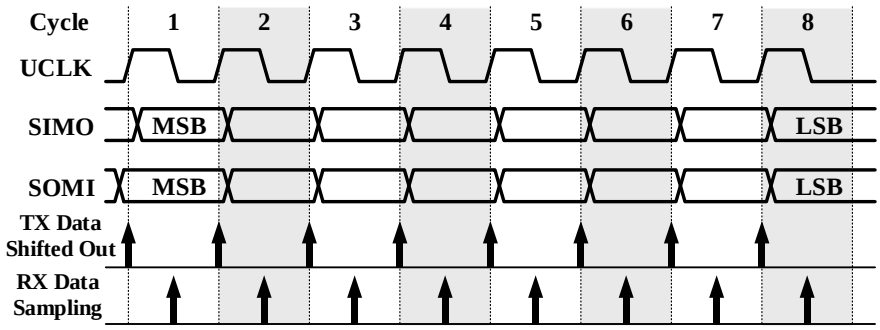

Fig. 7. Timing diagram of the SPI link between the MCU and the transceiver.

samples per second using a shared clock provided by the MCU. Fig. 7 shows a timing diagram of the master device (MCU) while it transmits and receives data. The SPI module uses three pins to operate, a clock (CLK), the slave-input master-output (SIMO) and the slave-output master-input (SOMI). Depending on the clock polarity, SIMO will start transmitting at the rising or falling edge of CLK and SOMI will sample the incoming data at the opposite clock edge [15].

Wireless Transceiver and Matching Network

Once in the transceiver, the data is codified and encrypted in the MAC. Then, an intermediate frequency (IF) modulator receives the digital data and a clock stream from the MAC, and converts the data into in-phase and quadrature (I&Q) signals at IF = 450 KHz [16]. The resulting scheme is a four-level frequency shift keying (4FSK) modulation with a maximum effective data rate larger than 200 Kbps [16]. The modulated signals pass through a pair of balanced mixers, fed by I&Q pairs of both IF and local oscillator (LO) signals, for up-conversion to the selected channel in the MICS band. The outputs of the mixers are added and result in a single-sideband signal with suppression on the unwanted opposite sideband. This signal passes through a power amplifier (PA) stage which provides a maximum output signal of -3dBm. Finally, the signal goes into an external matching network and is radiated by the antenna.

When the IMD receives information using the MICS band, the signal from the antenna passes through the matching network and then is injected to the on-chip Low Noise Amplifier (LNA). Then, the signal passes over a pair of balanced mixers similar to the ones used in the transmitter. The mixers produce a pair of I&Q signals at

IF = 450 KHz [16]. This is followed by an IF Filter and a FM detector which translates the frequency deviations to a time-varying voltage level. The resulting baseband signal is converted to the digital domain by a 2-bit quantizer [16]. The digitized data is sent to the MAC for correlation and clock recovery. Finally, the recovered data is transferred to the MCU using the SPI link described before.

Fig. 8 shows the external matching network needed to operate the transceiver in the ISM and MICS bands while using a dual-band antenna. The RF signal received by the antenna goes through a capacitor (C_X) for AC coupling and is followed by an LC tank (C_Y and L_Y) that acts as notch to filter out signals centered at the ISM band. A surface acoustic wave (SAW) filter is used to limit the incoming information to content centered at the MICS band. The SAW filter used in this work is a customized design from Kyocera with a center frequency of 403.5 MHz and bandwidth of 3 MHz [25]. A pi-network (C_{P1}, C_{P2} and L_P) is used to match the impedance of the SAW filter at port 2 (P_2) to the impedance of the antenna while a high-pass LC network (C_{Z1} and L_{Z1}) performs impedance transformation between port 1 (P_1) and the RX/TX MICS band pin of the transceiver. When a wake-up signal (ISM band) is received by the antenna, it is

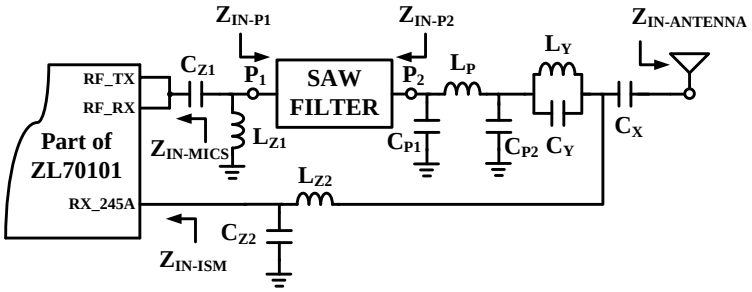

Fig. 8. Dual-band matching network of the IMD.

rejected by the notch filter mentioned above and passes through a low-pass LC network (C_{Z2} and L_{Z2}) that conducts impedance transformation between the wake-up pin of the transceiver and the antenna. The values of the matching network components are presented in Table I.

Table I. Values of the matching network components.

Component	**Value**	**Component**	**Uplink**
$\mathbf{C_{Z1}}$	120pF	$\mathbf{C_{Y}}$	1.2pF
$\mathbf{L_{Z1}}$	19nH	$\mathbf{L_{Y}}$	2.7nH
$\mathbf{C_{P1}}$	5.6pF	$\mathbf{C_{X}}$	30pF
$\mathbf{C_{P2}}$	5.6pF	$\mathbf{L_{Z2}}$	3.3nH
$\mathbf{L_{P}}$	18nH	$\mathbf{C_{Z2}}$	0.75pF

As mentioned before, the wireless link using the MICS band can be used for data and commands transmission, and it can even work to start communication between the IMD and BS. Nevertheless, using it to periodically listen for the BS's wake-up signals would result in excessive power consumption since the receiver is composed by several power hungry blocks. In order to provide an ultra-low-power wake-up mechanism, a receiver using an On/Off Key (OOK) modulation employing a dedicated frequency band with modest power consumption for the start-up process was implemented in the transceiver IC. By using the OOK scheme there is no need for a local oscillator while the use of a predefined frequency (a channel within the ISM band) for the wireless transmission reduces the complexity of the receiver [16]. On this way the on-chip ultra-

low-power receiver is being used instead of the MICS receiver in order to start the IMD operations.

Base Station and Graphical User Interface

The base station of the ZL70101 application development kit from Microsemi is employed as BS unit in this work. Its design is similar to the IMD in the sense that it is based on the same transceiver and that the employed MCU belongs to the MSP430 family. A block diagram of the BS is presented in Fig. 9. The signal from the IMD is received by a multi-band helical antenna and passes through the matching network and transceiver similarly as explained in the previous subsection. The transceiver receives the data and sends it to the MCU through the SPI module. The MCU then transfers the data to a USB interface chip through a serial non-synchronous link and the aforementioned IC handles the communication with the computer. In the computer, the GUI performs the data processing and stores the received data. Using the GUI, the user can modify the link features such as modulation, data rate and frequency of data collection.

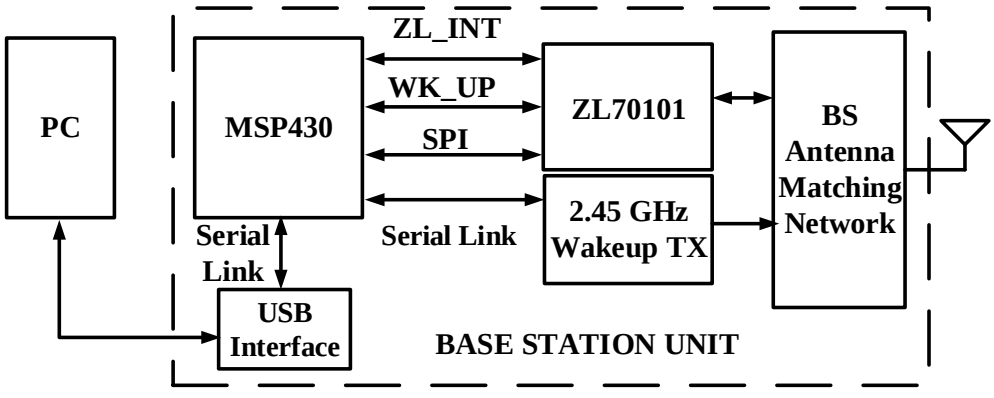

Fig. 9. Block diagram of the base station unit.

When the GUI receives an instruction from the user, the instruction is transmitted to the MCU via USB and the microcontroller sends it to the transceiver using the SPI bus. To start a transmission, the transceiver sends a wake-up signal using the ISM band and the IMD replies using the MICS band. Both, the BS and the IMD units, perform a wireless handshaking using the MICS band and finally, the BS unit transmits the instruction to the IMD where it is processed.

System Design and Implementation

Basic Considerations for MCU-based Low Power Operation

The selected MCU is designed from the outset for low-power operation. Power optimization is achieved through the use of a range of low-power modes (LPM) supported by a versatile clock system [26]. Fig. 10 shows the different MCU operating modes that will be used by the control algorithm along with their corresponding current consumption values for 3V and 2.2V supply voltages. When the MCU operates in active mode (AM), all the internal clocks and enabled modules are active. On the other hand, while operating in a specific LPM, a selected number of clocks are enabled and only the

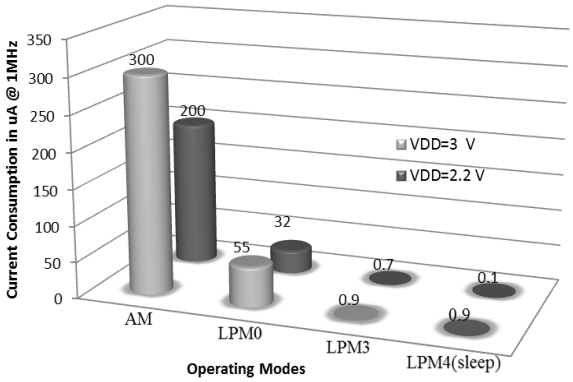

Fig. 10. Different operating modes of the MCU [26].

peripherals driven by the active clocks can be used. For example, during LPM0 the MCU main clock (MCLK) is disabled while the sub-main clock (SMCLK) and the auxiliary clock (ACLK) are active. This allows the operation of high speed peripherals such as SPI and DMA modules with no CPU intervention. Similarly, when the MCU operates in LPM3, only ACLK is active and the MCU is restricted to use only the peripherals performing low frequency tasks such as the op amps, the SAR-ADC and the timer.

Proposed Low-Power-Oriented Control Algorithm

The goal of the algorithm is to switch the MCU between AM, LPM0, and LPM3 using interrupts [27]. Interrupts are generated by hardware or software to respond to an urgent event by executing an interrupt service routine (ISR) [26]. The principle of operation is the following: when the MCU is in a LPM, an interrupt automatically switches the device to AM where the ISR finds the interrupt source and sets a flag to inform the main program what task needs to be performed. The MCU returns to the main program, serves the ISR and goes back into a LPM. This process is repeated each time a new interrupt is asserted.

A basic flow chart of the proposed control algorithm is presented in Fig. 11 where the interrupt sources are the DMA, the timer and the transceiver chip (TX/RX interrupt). The main program initializes the MCU (routine INT_MCU) and sends the MCU to LPM3 where it waits for a wake-up signal to continue. The INIT_MCU routine consists of the following subroutines: Init_McIO, selects the ports that will be used as digital/analog inputs/outputs and enables the external interrupt to be used to assert the

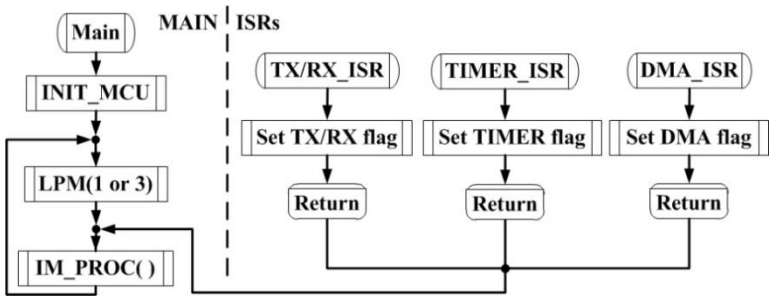

Fig. 11. Basic flow chart of the implemented algorithm.

TX/RX interrupt. InitAnalogPeripherals, initializes the analog peripherals that are used by the IMD: SAR-ADC and the three op amps that compose the IA. This subroutine also sets the control registers of the timer that will be in charge of triggering the ADC and the DMA channels that will transfer information between the RAM and different peripherals. SPIInit, initializes the SPI peripheral by setting the clock frequency/polarity, the port used for the communication and the size of the word that will be transmitted. Finally, MicsInit initializes the transceiver by sending command to set its control registers.

When the wake-up signal is received by the transceiver, the TX/RX interrupt is asserted and the TX/RX_ISR enables the timer and the other interrupts. Then it switches the MCU to LPM3 and waits for the next interrupt to be asserted. The next interrupt to be asserted is from the timer used to start ADC conversions. When this interrupt is asserted, the TIMER_ISR sets a flag and IM_PROC enables the ADC. Then, the MCU goes into LPM0, the ADC sample is sent to the RAM through the DMA1 and the MCU returns to LPM3. This continues until one RAM page (217 samples) has been filled with data and the DMA interrupt is asserted. Then, the DMA_ISR sets a flag to let IM_PROC

know that one memory page has been written and the DMA1 channel destination address is updated in order to write the incoming data into the following memory page.

When a data packet (9 pages) is ready for transmission, IM_PROC enables the SPI module to communicate the MCU with the transceiver and the DMA2 channel sends information from the RAM to the SPI output buffer. When one RAM page has been transmitted to the SPI output buffer the DMA interrupt is asserted again but this time due to the DMA2 channel. The DMA_ISR sets a flag and IM_PROC updates the source address of the DMA2 channel to start reading the next memory page. This happens until the complete data packet is transmitted. Since the RAM can store up to two data packets, while one is transmitted to the BS unit, the other is used to store new physiological samples. This sequence occurs continuously or periodically depending on the settings defined by the user. More details on this regard will be provided in the next section.

The remaining TX/RX interrupt sources are the transmit/receive RF buffers, the SPI bus, a link monitoring register that tracks the communication between the IMD and the BS unit, and another control register that indicates when an instruction command has been completed. When they are asserted, the routine IM_PROC uses the SPI module to read the interrupt vector of the transceiver. In order to serve the different interrupts, the MCU sends instruction commands to the transceiver to perform tasks such as restart the wireless link, read/write data on the TX/RX buffers, or clear the required interrupt vector bit. As a result of the implemented algorithm, the MCU remains in LPM3 most of the time, waiting for the next interrupt to be asserted and, hence, the power consumption of the IMD is optimized.

Power Analysis

The IMD power consumption varies with time depending on the task being performed. By knowing the power consumption and the duration of each task, the IMD average current (I_{AV}) can be computed and its lifetime can be estimated.

Continuous Sampling Mode

Fig. 12 shows a timing diagram of the tasks performed by the IMD while sampling a blood pressure signal with a frequency of 5 Hz. This frequency is used since several physiological signals fall below this bandwidth [23]. In this figure, t_T is the total time needed to collect and transmit a data packet (9 pages of 217 words), t_P is the time needed to write a data packet inside the RAM, t_{TX} is the time required for the RF transmitter to submit the data stored in the RAM to the BS, t_{AS} is the time between adjacent samples, t_C is the ADC conversion time (13 cycles of the 32.758KHz clock that drives the ADC [15]) and t_{AQ} ($1/f_S$) is the acquisition time given by t_{AS} + t_C. For the transceiver with a data rate of 200 Kbps and 16-bit resolution for each sample, the IMD can transmit 12.5 kilo samples per second. Having this transmission rate and an ADC's oversampling rate

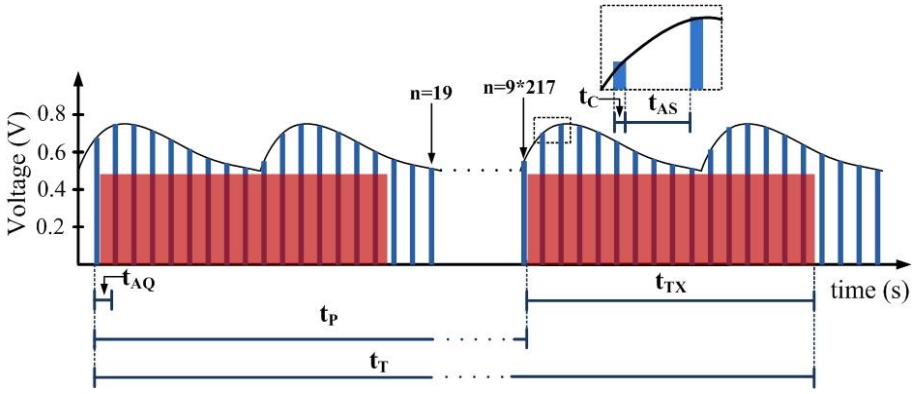

Fig. 12. Timming diagram of the IMD sampling a biological signal in CSM.

of 20 (f_S=100 Hz), the timing parameters in Fig. 9 have the following values: t_C= 13/32758 ≈ 0.4 ms, t_{AS}= (1 / f_S) - t_C = 10 ms – 0.4 ms = 9.6 ms, t_P = 9×217×t_{AQ} = 19.44 s, t_{TX} = 9×217/12.5K = 0.156 s and the total time is t_T = t_P + t_{TX} = 19.596 s. From these numbers, it is possible to observe that the IMD remains in RF transmission mode around 0.8% of the total time needed to collect and transmit a data packet. The scenario where the IMD has the previous timing parameters and sends information to the base station without interruption is defined as continuous sampling mode (CSM). The following equation is used to calculate the average current consumption (I_{AVC}) of the IMD in CSM:

$$I_{AVC} = \frac{217 \times 9(t_C \times I_C + t_{AS} \times I_{AS}) + t_{TX} \times I_{TX}}{t_T} \quad (2.3)$$

where I_C is the current consumption during t_C, I_{AS} is the current consumption during t_{AS} and I_{TX} is the current consumption during t_{TX} with values of 0.65mA, 0.5mA and 6mA respectively. The current values are taken from [15] and [16]. Using **(2.3)**, it is possible to predict an I_{AVC} around 0.549mA. Moreover, selecting a Li/$SoCl_2$ battery from Eagle Pitcher [28] with a capacity of 350mAh, the estimated lifetime of the IMD in CSM can be obtained using the ratio of the battery capacity and I_{AVC}, resulting in approximately 26.5 days. This battery was chosen as the power source due to its small size (6.6 mm x16.5 mm x15.2 mm = 1.66 cc, 4.6 g) and large current capability. The time and current values presented in this subsection are summarized in Table II.

Table II. Summary of the time and current values for different IMD tasks.

Parameter	Time (ms)	Parameter	Current (mA)
$\mathbf{t_C}$	0.4	$\mathbf{I_C}$	0.65
$\mathbf{t_{AS}}$	9.6	$\mathbf{I_{AS}}$	0.5
$\mathbf{t_{TX}}$	156	$\mathbf{I_{TX}}$	6
$\mathbf{t_T}$	19,596	$\mathbf{I_{AVC}}$	0.549

Periodic Sampling Mode

Since the average current is inversely proportional to the lifetime, increasing the lifetime of the IMD can be achieved by decreasing I_{AV}. In order to extend the lifetime, the IMD average current consumption can be reduced using a variation of the CSM where only a fixed number of data packets is collected in a given period of time. This is done in the following way: the user defines the number of packages to be collected using the GUI, the IMD operates continuously until the last data packed is submitted to the BS and finally, the MCU switches to sleep mode (LPM4) until a new set of data is required. During sleep mode the microcontroller turns off all the peripherals and waits for a new wake-up signal. This variation of CSM is defined as periodic sampling mode (PSM). Fig. 13 shows the timing diagram of the IMD current in PSM, where t_{AQ}, t_P and t_T refer to the parameters presented in Fig. 12, t_{OFF} is the time in which the circuit remains in sleep mode and I is the current consumption of the IMD depending on the task being performed. Finally, t_{DS} is defined by $t_{ON} + t_{OFF}$ and the frequency of data collection (f_{DS}) is the inverse of t_{DS}.

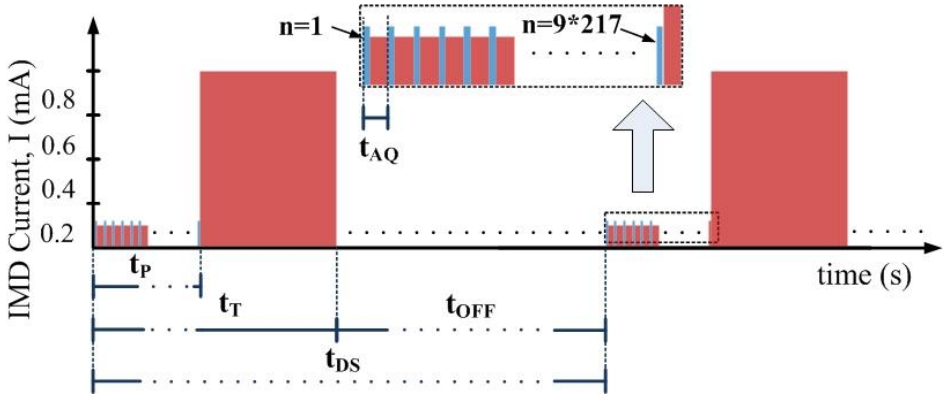

Fig. 13. Timing diagram of the IMD operating in periodid sampling mode (PSM).

The following equation is used to compute the average current during PSM:

$$I_{ACP} = \frac{t_T \times I_{AVC} + t_{OFF} \times I_{OFF}}{t_{DS}} \tag{2.4}$$

where I_{OFF} = 0.9 µA is the current consumption of the MCU during t_{OFF} [15]. Fig. 14 shows a prediction of the lifetime in months and the number of data packets transmitted from the IMD to the BS during one day. This plot is based on equations (2.3) and (2.4), and the timing parameters and battery capacity presented before. A linear relationship

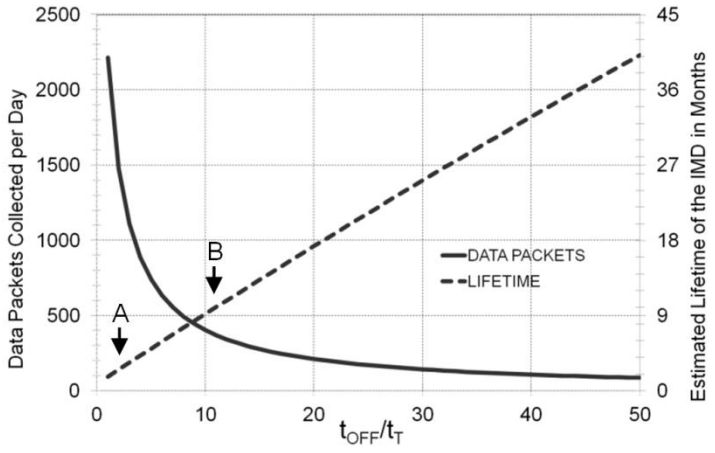

Fig. 14. Lifetime and data packets per day vs. t_{OFF} / t_T for a 350 mAh battery.

between the ratio of t_{OFF} and t_T and the lifetime of the IMD is observed while the amount of collected data decreases and tends to saturate. For example, in points A and B the ratios are 1 and 10 resulting on 1.7 and 9.2 months of lifetime with 2212 and 403 data packets per day respectively. This plot can be used to choose the t_{OFF} / t_T ratio that would fit better with the designer's needs.

In-vitro Measurements and Results

IMD Prototype Implementation

A prototype of the IMD has been implemented in order to demonstrate the operation of the low-power-oriented control algorithm and to corroborate the results obtained from the lifetime estimation presented in the previous section. The fabricated IMD printed circuit board (PCB) is presented in Fig. 15. The 2-layer PCB has a total area of 50.7 cm^2 (7.12 cm x 7.12 cm) and was fabricated with a 0.062" FR4 substrate. The dual-band printed loop antenna (PLA) shown on the left side of the picture was provided by Microsemi and accounts for body losses allowing *in-vitro* testing over free air.

Debug and Testing for *In-vitro* Measurements

The implemented PCB features different debug and testing capabilities in order to allow *in-vitro* measurements before fabricating the final IMD unit with actual implantable dimensions. The main debug resources include a J-TAG receptacle that allows upgrades on the MCU's firmware; a variable R1 resistor used to modify the IA total gain; a set of LEDs used to monitor the link indicating the MICS transmitter or receiver operation, the status of the connection between IMD and BS and if a wake up signal has been received by the IMD; a BNC connector to emulate different biological signals using an

function/arbitrary waveform generator (FAWG) and push buttons to reset or start manually the IMD.

For testing capabilities, the IMD includes test points to monitor different key signals from the IA (gains of the 1st and 2nd stages), MCU (timer output, DAC output, crystal oscillator XT1, etc.), SPI link (CLK, SIMO, SOMI and CS) and the TX/RX (programmable outputs, voltage references, crystal oscillator XT2, etc.). The IMD prototype also includes a set of jumpers to manually enable/disable MCU modules and LEDs in order to measure the current consumption of the IMD in different nodes and with the MCU operating in different power modes.

Board Optimization

The highlighted areas in Fig. 15 included the aforementioned MCU and TX/RX along

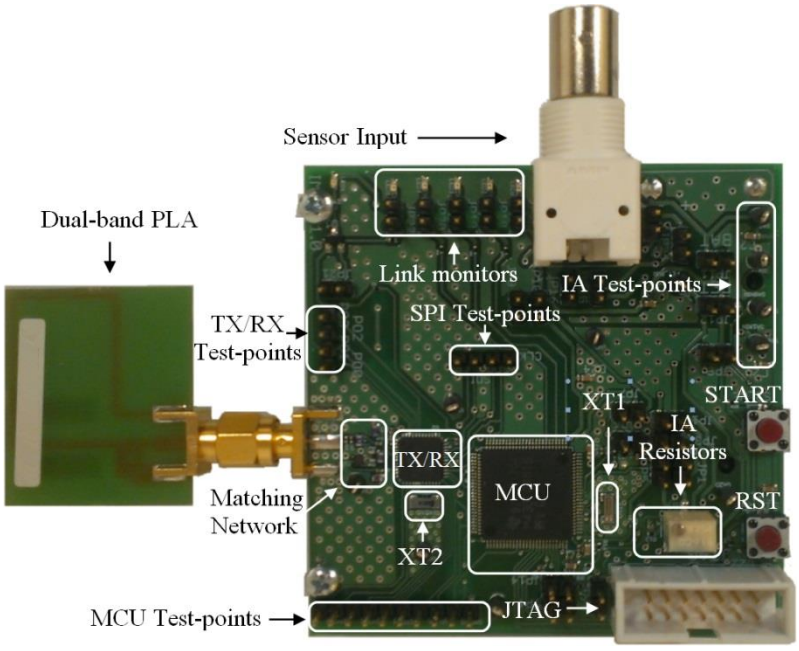

Fig. 15. Fabricated implantable medical device prototype board.

with their external components: bypass capacitors, crystals 1 and 2, IA resistors/capacitors and the matching network elements. Combining all this parts and removing the variable R1 resistor along with all the debug/testing hardware (also highlighted), result in an effective board area of 6.5 cm^2 (12.8% of the original size). Furthermore, if each IC is placed on the top and bottom sides of a PCB, an IMD effective area of 2.7 cm^2 can be achieved.

Link Analysis

This subsection discusses the main factors to be considered while designing a wireless link for implantable applications. The following expression [29] is a simple link budget equation that can be used for typical uplink/downlink calculations:

$$P_{RX}|_{dBm} = P_{TX}|_{dBm} + G_{TX}|_{dB} - L_T|_{dB} + G_{RX}|_{dB} \quad (2.5)$$

where $P_{RX}|_{dBm}$ is the power available at the receiver input terminals, $P_{TX}|_{dBm}$is the signal power available from the transmitter output terminal, $G_{TX}|_{dB}$ is the gain of the transmitter antenna including cable and matching losses, $L_{T|dB}$ $L_T$represents the total of losses between the transmitter output and the receiver input and $G_{RX}|_{dB}$ is the gain of the receiver antenna including only matching losses. Nevertheless, this is not a typical application and some modifications should be considered in order to have accurate results.

First, it is critical to take into account that the propagation path of the presented link happens through two different media: free air and the subjects' body. The total loss between the IMD antenna input and the outside of the subjects' body, including matching network losses is between 40 dB and 45 dB [17]. Also, the MICS standard

requires the antenna gain and the propagation path loss within the body to be combined together when calculating the effective radiated power (ERP) of the IMD transmitter [30]. Therefore, the ERP can be defined as:

$$P_{TX(ERP)}\,|_{dBm} = P_{TX}\,|_{dBm} + G_{TX}\,|_{dB} \tag{2.6}$$

Moreover, the BS and IMD output power levels are restricted to a maximum ERP of -16 dBm in a reference bandwidth of 300 KHz to prevent interference with meteorological aids [17]. Using (2.6) and having a BS antenna gain of -5 dBi including losses, the maximum power transmitted by the BS unit is -11 dBm. For the IMD, the transmitter is programmed to have an output power of -3 dBm and the antenna gain including body and matching losses is -42 dB, resulting in an ERP of -45 dBm. Therefore, since the in-body losses are much more significant than any cable or matching loss at the BS unit, the power transmitted by the IMD is higher than the one transmitted by the BS unit.

The total loss between the transmitter and the receiver $L_T|_{dB}$ consists of the free-space path loss$A_{FSL}|_{dB}$ and a "fading margin" $A_{FADE}|_{dB}$ of 5 dB is added to allow for destructive interference. The free-space path loss depends on the wavelength and the distances as shown in the following equation [29]:

$$A_{FSL}\,|_{dB} = 20\mathrm{Log}\left(\frac{4\pi d}{l}\right) \tag{2.7}$$

Using equations (2.6) and (2.7), the original link budget equation can be defined as:

$$P_{RX}\,|_{dBm} = P_{TX(ERP)}\,|_{dBm} - A_{FSL}\,|_{dB} - A_{FADE}\,|_{dB} + G_{RX}\,|_{dB} \tag{2.8}$$

The minimum detectable signal (MDS) is defined as the minimum $P_{RX}|_{dBm}$ level present at the receiver to perform a successful transmission. Thus, it is possible to compute the MDS using the following equation [29]:

$$MDS|_{dBm} = NF|_{dB} + 10Log(kTB)|_{dB} + 30 + SNR_{MIN}\,|_{dB} \quad (2.9)$$

where $NF|_{dB}$ $N_{IN}|_{dBm}$ $NF|_{dB}$is the noise figure of the receiver, k is the Boltzmann constant, T is the temperature in Kelvin degrees,$N_{IN}|_{dBm}$, B is the bandwidth of interest (B=300 KHz), 30 is added to convert the integrated noise floor to dBm and $P_{RX}|_{dBm}$ $N_{IN}|_{dBm}$ is the minimum signal to noise ratio (SNR) required for a maximum allowed bit error ratio (BER). The NF of the IMD and the BS units operating with a data rate of 200 Kbps using 2FSK modulation in the downlink (BS to IMD) and 400 Kbps with 2FSK in the uplink (IMD to BS) are 5 dB and 9 dB with $P_{RX}|_{dBm}$values of 14 dB and 17 dB respectively [31]. Using (2.9) the MDS levels of the BS and IMD units are found to be -90 dBm and -99 dBm (40.2 μV_{rms} and 14 μV_{rms} with an effective resistance of 1620Ω), respectively.

Measurement Setup and Experimental Results

The implantable WMS *in-vitro* measurement setup is shown in Fig. 16. In this test, a 5 Hz blood pressure signal is emulated using the Agilent 33220A FAWG with a peak-to-peak amplitude of about 1mV and a DC offset of 0.5mV. This signal is injected to the IMD where is amplified, converted to the digital domain and transmitted to the BS unit through the RF channel using the MICS band. The BS unit receives the wireless data and sends it to a computer via USB. In the computer, the GUI stores the data and performs post-processing operations.

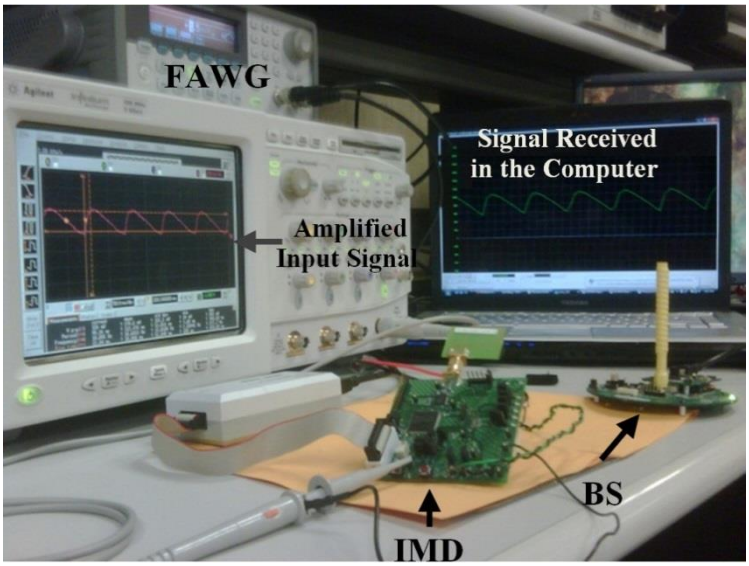

Fig. 16. Measurement setup for *in-vitro* measurements.

In order to verify the operation of the system the IMD and FAWG were placed at a fixed location while the BS unit was moved away from the device to perform transmission measurements in the line of sight. Measurements were taken at each step of 10 cm. The maximum distance of the wireless communication link achieved in the MICS band is 2.1 m in the line of sight. Table III presents the link measurement results for this distance with data rate of 200 Kbps and using the channel located at 403.5 MHz. $P_{RX}|_{dBm}$ and $P_{TX}|_{dBm}$ were taken from the transceiver's measurement registers and the other parameters were calculated using (2.5), (2.6), (2.7) and (2.8). Notice that $P_{RX}|_{dBm}$ $P_{TX(ERP)}|_{dBm}$for the uplink is smaller than the value computed in the previous section (-45dBm). To understand the reason of this difference, let us use equation (2.6), the measured ERP (-49 dBm) and$P_{TX}|_{dBm}$= -3 dBm$P_{TX}|_{dBm}$ = -3dBm, to compute the antenna gain minus losses $G_{TX}|_{dB}$ in the uplink ($G_{RX}|_{dB}$for the downlink). This results in

a value of -46dB, meaning that there are extra losses in the dual-band PLA in comparison with the estimated value. This discrepancy can be due to variations on the matching network components or the length of the PCB traces used to connect the antenna. Nevertheless, the results are still close to the values predicted on the link budget calculations and therefore, the presented method can be used as a start point for designing a WMS for implantable applications.

Table III. Link budget parameters with d=2.1m.

Parameter	**Downlink**	**Uplink**
$\mathbf{P_{TX(ERP)}}$ **|dBm**	-16	-49
$\mathbf{A_{FSL}}$ **|dB**	31	31
$\mathbf{A_{FADE}}$ **|dB**	5	5
$\mathbf{G_{RX}}$ **|dB**	-46	-5
$\mathbf{P_{RX}}$ **|dBm**	-98	-90

Fig. 17 shows a comparison between the amplified signal at the input of the ADC (in the IMD) and the data received at the BS unit for a distance of 2.1 m. Notice that the transmission delay (t_{TX}) is not taken into account since the purpose of this figure is to show the signals in a direct comparison. The sampling frequency of the ADC was 300 Hz and the frequency of the input signal was 10 Hz.

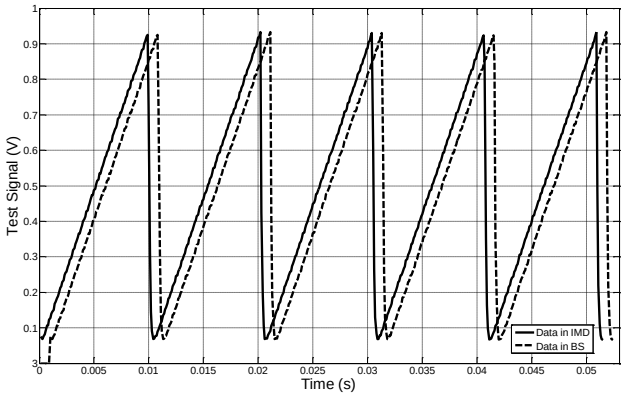

Fig. 17. Signal at the ADC input vs data received at the BS, d=2.1 m.

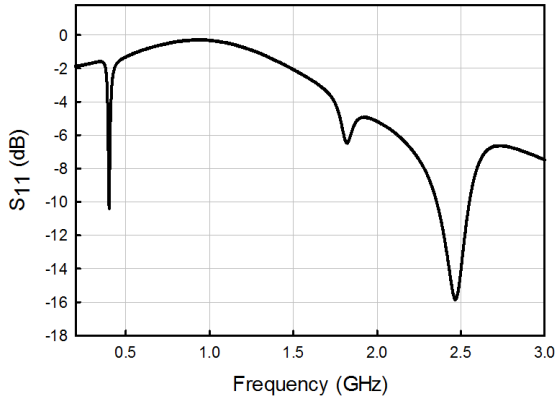

Fig. 18. S11 of the dual-band PLA used in the IMD.

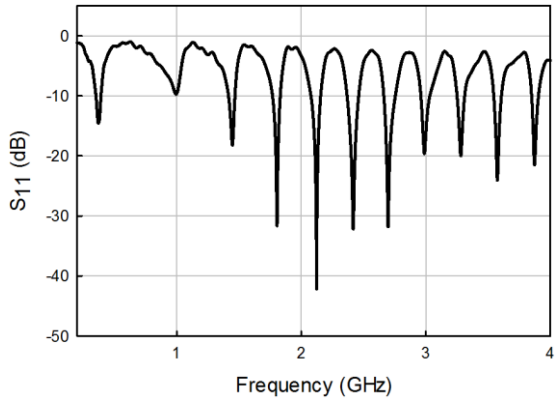

Fig. 19. S11 of the multi-band helical antenna used in the BS.

Fig. 18 and Fig. 19 show the return loss of the IMD's dual-band-PLA and the BS's multi-band helical antenna, respectively. Both antennas were provided by Microsemi and operate in the ISM and MICS bands, as observed on the figures, allowing the use of the ultra-low-power wake-up mechanism described in section B of this chapter.

Finally, power measurements showed an average current value of I_{AVC} = 0.572mA for a 3 V power supply, corresponding closely to the calculations performed in section D. Using this I_{AVC}, the IMD prototype lifetime is 1.7 months operating in continuous mode with a projected 2.7 cm^2 area. This can be compared with 1.5 months and approximately 1.9 cm^2 offered by the commercial implantable blood pressure monitor for small animals from [32].

Summary

This chapter has presented the design, implementation and testing of a WMS prototype for implantable applications meeting FCC standards. Special attention was placed on the realization of the implantable unit in order to obtain the best trade-off between size, cost and power. A thorough explanation of the signal path, starting as an analog waveform from the sensor and reaching the PC as digital information has been presented.

The comprehensive power analysis presented in section D and the link budget study from section E provided results close to the *in-vitro* measurements. Therefore, a similar methodology can be used to predict the lifetime of generic monitory units (invasive or non-invasive) and to make a realistic link analysis from the very beginning of the design stage.

The proof-of-concept IMD prototype includes several testing/debug capabilities and is designed to allow the integration of different sensors to monitor other biological parameters with minimal modifications. Moreover, suggestions for the optimization of the presented IMD and the implementation of the final implantable unit have been discussed.

CHAPTER III

A PORTABLE 12-LEAD ECG WIRELESS MEDICAL SYSTEM FOR CONTINOUS CARDIAC-ACTIVITY MONITORING*

Introduction

Early detection and diagnosis of cardiac diseases allows physicians to identify abnormalities likely to progress and cause permanent damage. Although most arrhythmias don't present a direct risk to the patient, they may lead to the presence of symptoms and become a signal for potential cardiac arrest or stroke [33]. Therefore, the monitoring of these events is important, especially for patients who have suffered a heart attack. Since occurrence and duration of arrhythmias cannot be predicted, it is hard to detect them during routine electrocardiography (ECG) examinations. Thus, the use of wireless medical systems (WMS) intended for continuous cardiac-activity monitoring plays an important role in modern preventive medicine.

Such systems provide patients with the benefits of dedicated equipment for detection, characterization and documentation of the electrical activity of the heart over given periods of time, while allowing them to continue with their daily routine [33]. Nevertheless, the need of continuous and highly accurate monitoring brings limitations on the cost and lifetime of the ambulatory unit [14]. Moreover, the size of the portable unit may affect patients' comfort. Therefore, selecting the appropriate hardware to

*©[2014] IEEE. Reprinted, with permission, from "A Portable 12-Lead ECG Wireless Medical System for Continuous Cardiac-Activity Monitoring," by J. E. Gaxiola-Sosa, N. Mohsin, J. A. Palliyali, R. Tafreshi, and K. Entesari, *2014 IEEE 2nd Middle East Conference on* in *Biomedical Engineering (MECBME)*, presented in Feb., 2014.

guarantee robust operation and implementing a smart software control-algorithm to optimize the power consumption are vital for the development of a WMS [11].

Typically, a WMS consists of an end device (ED), a base station (BS) and a graphical user interface (GUI). In ambulatory electrocardiography applications, the ED is in charge of collecting and transmitting the ECG signals, while the BS acts as gateway between the ED and the GUI. The GUI stores, displays and processes the data, maintaining constant communication with a health center in case of an emergency.

This chapter presents a WMS intended for continuous cardiac-activity monitoring. A standard 12-lead ECG is provided in order to enhance pattern recognition and to enable the comparison of the cardiac vector projections in two orthogonal planes and at different angles. This provides a more accurate analysis in comparison with typical 5-electrode Holter monitors [34]. This chapter is organized as following: section B discusses the ED and BS implementation, section C shows the GUI including the detection algorithm, section D presents experimental results of the system and section E concludes the chapter.

System Overview

A block diagram of the 12-lead ECG WMS, including simplified versions of the ED and BS, is shown in Fig. 20. The ED is based on three off-the-shelf ICs intended for ultra-

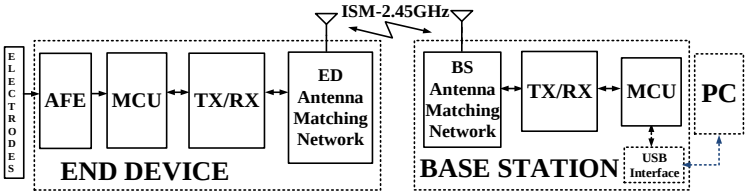

Fig. 20. Block diagram of the wireless medical system.

low-power applications: the ADS1298 [35], an 8-channel low-power analog front-end (AFE) for biopotential measurements; the MSP430FG4618 [15], a mixed-signal microcontroller (MCU); and the CC2500 [36], an ultra-low power 2.45 GHz industrial, scientific and medical (ISM) band transceiver. The BS is composed of similar ICs excluding the AFE and incorporating a universal serial bus (USB) interface. The GUI communicates with the BS using a USB port that generates a virtual communication (COM) port in the PC from which data is retrieved. The basic operating principle of the 12-lead ECG WMS is as follows: *(i)* the BS connects with the PC and waits for a message from the ED; *(ii)* after a given number of ECG samples is stored in the ED, the collected data is sent to the BS which in turn, will transmit it to the PC via USB; *(iii)* the PC receives the ECG data and the GUI processes the information. Tasks *(ii)* and *(iii)* repeat continuously until the monitoring period specified for the patient is over.

End Device

A detailed block diagram of the ED is shown in Fig. 21. The AFE uses 10 electrodes placed on the standard positions to generate 12 leads: six precordial unipolar leads (V1-V6), three limb bipolar leads (I, II, III) and three augmented, unipolar leads (aVR, aVL,

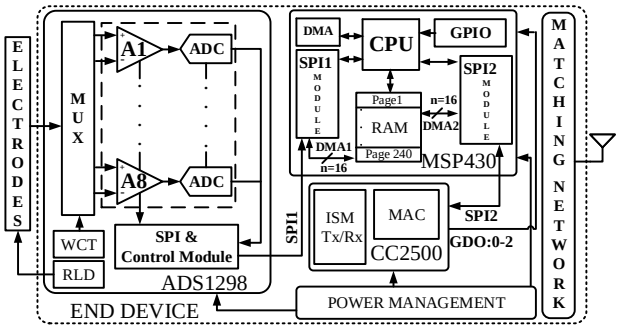

Fig. 21. Block diagram of the end device.

aVF). Bipolar leads are generated by the difference of two electrode voltages while unipolar leads are referenced to the Wilson central terminal (WCT) [35]. The circuit includes 8 channels that consist of a programmable gain amplifier (PGA), internal voltage reference and 24-bit delta-sigma ADC, WCT generator and right leg drive (RLD) loop [8]. Each channel of the AFE provides the difference between two electrodes with a signal to noise ratio (SNR) of 112 dB [33]. Leads I, II, and V1-V6 are computed in the analog domain, while the augmented leads and lead III are computed digitally. The electrode placement and lead derivation are presented in Fig. 22 and Table IV, respectively. The gain of the PGAs is fairly low (6 V/V) since the ADC provides high resolution and shapes the noise taking advantage of the delta-sigma architecture. In order to deal with common mode signals such as the 60/50 Hz noise from the power mains, the internal RLD circuit is used. The RLD operates by sampling the common mode noise between the on-chip gain-setting resistors. The noise is then buffered, inverted, and fed back onto the body through the RL electrode. Because of the low gain, the DC offset from the electrodes doesn't saturate the system and DC removal can be performed by digital filtering. The sampling frequency of the AFE is set to be 500 Hz for the WMS presented in this document.

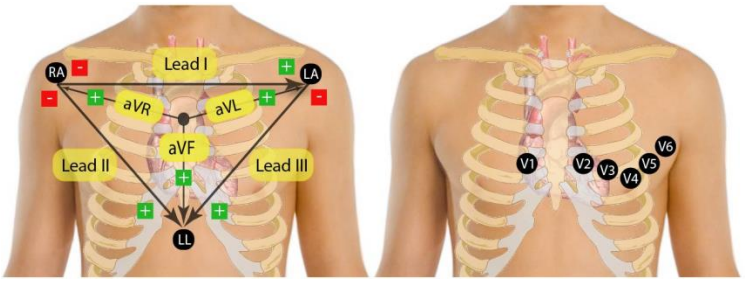

Fig. 22. Typical electrode placement on 12-lead ECG systems. (RL not shown).

Table IV. Lead derivations of the 12-lead ECG WMS.

Lead	**Formula**	**Lead**	**Formula**
V6 (CH1)	*V6-WCT*	**V1(CH8)**	*V1=V1-WCT*
LEADI (CH2)	*LA-RA*	***LEADIII**	*LL-RA-LA=LEADII–LEADI*
LEADII(CH3)	*LL-RA*	***aVR**	*RA-(LA+LL)/2=-(LEADI+LEADII)/2*
V2(CH4)	*V2=V2-WCT*	***aVL**	*LA-(RA+LL)/2=LEADI+LEADII/2*
V3(CH5)	*V3=V3-WCT*	***aVF**	*LL-(RA+RA)/2=LEADII-LEADI/2*
V4(CH6)	*V4=V4-WCT*	***WCT**	*(LA+RA+LL)/3*
V5(CH7)	*V5=V5-WCT*		****Digitally generated leads***

The AFE is controlled by the MCU which sends control commands and receives the sampled data via serial peripheral (SPI) link, SPI1. The received data is stored on the RAM memory of the MCU. The direct memory access (DMA) module uses a transfer channel (DMA1) to send data from the SPI1 buffer to the 8KB RAM with no CPU intervention. The RAM is organized in 240 pages. Each page contains 8 samples (one per channel) of 24-bits and a sample ID is added to verify the consistency of the received data, giving a total of 25 bytes per page. A data packet consists of 120 of these pages. When a data packet is ready for transmission, a second transfer channel of the DMA module (DMA2) sends the information to the output buffer of a second SPI channel (SPI2). Using the SPI2 module, the information is transferred from the MCU to the transceiver with a data rate of 2 mega samples per second. The transceiver codifies

and encrypts the data in order to produce an RF signal with two-level frequency shift keying (FSK) modulation scheme. The signal passes through a matching network and then is radiated by the antenna towards the BS. When the ED receives information from the BS for handshaking, the RF signal is recovered by the transceiver and is sent to the MCU through the SPI2 link described before.

Base Station

The MSP430F5529 experimenter's board is used as base station of the 12-lead ECG WMS. Its design is similar to the ED in the sense that it is based on the same transceiver and that its MCU belongs to the MSP430 family. The main difference is that it doesn't include the AFE chip and incorporates a USB interface. The signal transmitted by the ED is received by the BS antenna and reaches the MCU similarly as explained in the previous sub-section. The MCU communicates with a USB interface that generates a virtual COM port on the PC allowing the BS to act as a communications device class (CDC) device.

ED Control Algorithm

The control algorithm is designed to optimize the power consumption of the ED. The methodology used is similar to the one presented in chapter II. Power optimization is achieved by switching the MCU between an active mode (AM) and three low power modes (LPM) [11]. The MCU will switch from one power mode to another depending on the interrupts generated by hardware or software through the execution of the different tasks. An interrupt service routine (ISR) procures the flow of the main program by performing tasks depending on the asserted interrupt.

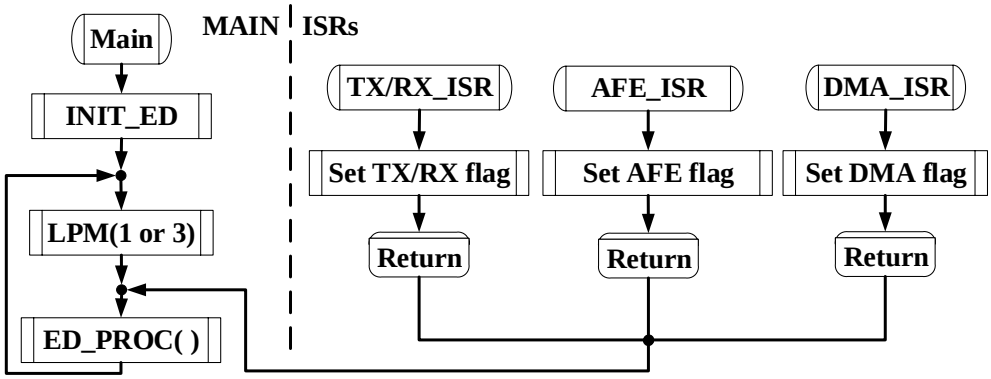

Fig. 23. Basic flow chart of the implemented algorithm.

A basic flow chart of the implemented algorithm is shown in Fig. 23. The subroutine INIT_ED initializes the MCU, AFE and transceiver; and waits for user confirmation (push button) to start sampling and sending data. The DMA and SPI modules are set to operate automatically depending on the amount of samples received. When an interrupt is asserted, the subroutine ED_PROC checks for the interrupt flag and the MCU performs the corresponding task. The main tasks are: updating the destination/origin address of the DMA modules for SPI1 buffer-to-RAM/RAM-to-SPI2 buffer transmission, restarting the wireless link, reading/writing data from/to the TX/RX buffers, and clearing the required interrupt vector bit. All interrupts are generated inside the MCU except for the transceiver and AFE interrupts which are asserted through the MCU input ports. The MCU waits for the next interrupt to be asserted and the cycle continues until the BS requests the ED to return to idle mode. By using the implemented algorithm, the ED remains in a LPM around 70% of the time and hence, its power consumption is optimized.

Graphical User Interface and Detection Algorithm

The GUI was designed with MATLAB SIMULINK® and runs under the ECG detection algorithm presented in [37]. The software extracts the received information and generates the remaining leads as explained in the previous section. Then, the algorithm utilizes parabolic curve fitting, adaptive thresholds, 'area under curve' approach and synchronicity across leads to detect the points of interest of the P, QRS complex and T waveforms as well as the isoelectric line used as reference point for clinical calculations. Based on the detected points, measurements such as QRS complex duration, Q wave width, PR/QT interval, Q/R/S/T wave peak amplitudes and ST/PR deviation can be computed. The detected points of interest and the aforementioned measurements are illustrated in Fig. 24. Using these measurements, ECG abnormalities such as irregular peak-to-peak intervals, irregular T wave, significant Q wave and variation in ST and PR levels can be observed. The detection algorithm featured in the GUI complements the 12-lead ECG WMS and can be used by physicians as start point for diagnosis of several cardiac diseases [9].

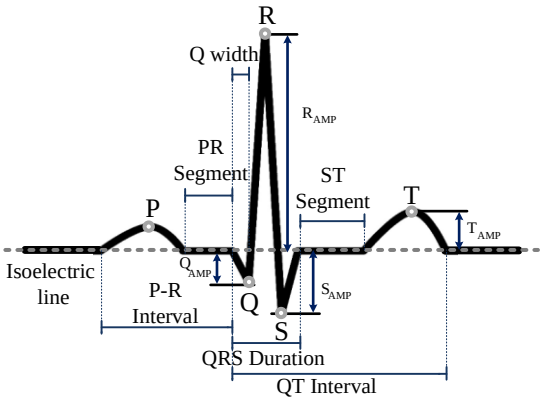

Fig. 24. ECG points of interest and clinical measurements.

Results

End Device Implementation

The ED printed circuit board (PCB) is shown in Fig. 25. It includes the following elements: testing capabilities to upgrade the MCU firmware and verify the proper operation of the AFE; protection circuitry consisting on current limiter resistors and diode clamps on each analog channel; a power management section composed by a negative charge pump and three low-dropout voltage regulators to generate 3.3V (DVDD) and +/- 2.5V (AVDD/AVSS); an RF receptacle that allows the ED to match with transceivers in different RF bands depending on the desired operating range (the transceiver mentioned in section II is used for this implementation); a DA15 connector as input for a 10 electrode cable; and finally the AFE and MCU described in section II. The PCB total area is 66.3 cm2 (79 mm x 84 mm) and it is powered by three AAA batteries placed in a holder located at the bottom of the board, making the ED a completely portable unit.

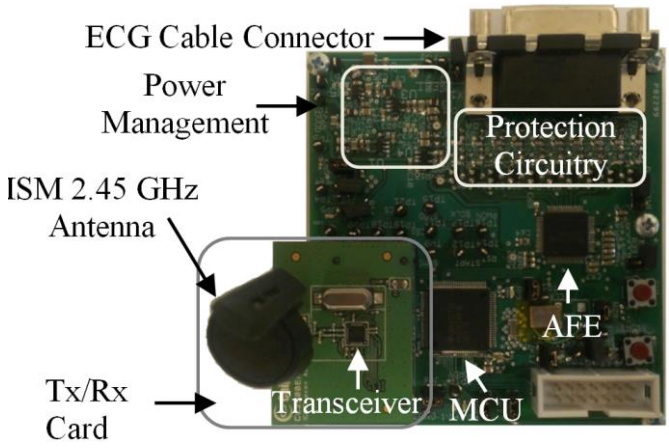

Fig. 25. End device PCB and ISM Tx/Rx daughter card.

The lifetime of the ED can be estimated using the ratio between the typical current consumption of the AFE, MCU and transceiver (5 mA [35], 0.7 mA [15] and 40 mA [36] respectively) over the battery capacity (3000mAh from three AAA batteries), resulting in around 2.6 days. Using the low-power oriented algorithm presented in section II and the power estimation methodology presented in chapter II, the average current consumption of the ED is reduced to around 33mA. This corresponds to a lifetime of approximately 3.7 days, a 40% increment from the estimated lifetime based on typical current consumption values of the AFE, MCU and transceiver.

Detection Algorithm Results

The GUI retrieves data from the BS through the USB port and the embedded ECG detection algorithm computes the key features of the received signals in real time. Based on these measurements, the heart rate can be calculated and a warning can be given if there is any inconsistency in the received waveforms. Fig. 26 displays the GUI presenting the detected ECG signal (lead II) sent from the ED. The analysis panel on the

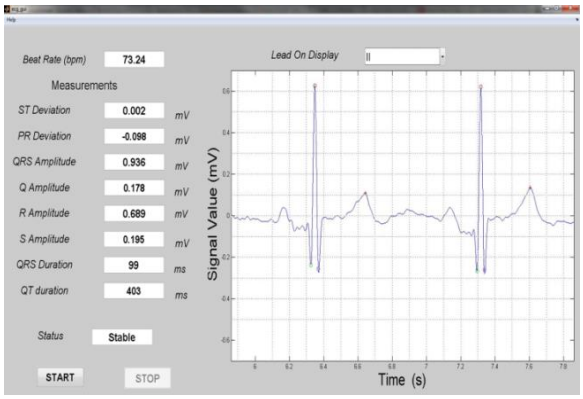

Fig. 26. GUI screenshot presenting the detected ECG signal (lead II).

left side includes the patient's heart rate in beats per minute, different real-time measurements, a status bar and Start/ Stop options to control the GUI operation.

The heart rate is calculated using the number of beats detected within specified period of 5 seconds and is displayed since it is an important parameter for certain cardiac diseases such as arrhythmia. The measurements on the analysis panel are used to indicate the stability of the signals and can be a start point for reliable and fast diagnosis in future analysis. For instance, the presence of ST elevation and hyper acute T wave in certain amount of leads can pinpoint to cardiac problems such as myocardial infarction. Also, appearance of ST elevation in certain regional leads can locate the affected regions of heart. The status bar indicates the regularity determined from the received signals. Finally, full information from the12-leads received by the GUI is available for non-real-time analysis and can be sent to health care providers for further analysis of the patient's heart condition and expediting necessary action.

In-vitro Measurements

Fig. 27 shows the 12-lead ECG WMS measurement setup. The ECG signal is emulated using the Cardiosim II ECG Simulator and is connected to the ED using a 10 electrode shielded ECG cable. Both products were supplied from Biometric Cables. Once the signals are injected to the ED they are amplified, converted to the digital domain and transmitted to the BS unit through the RF channel. The BS receives the information and sends it to the computer via USB where the GUI displays the 12-leads extracted by the ED. This set up allows in-vitro testing and debugging of the WMS for validation before patient trials. In order to verify the operation range of the WMS, the BS was placed at a

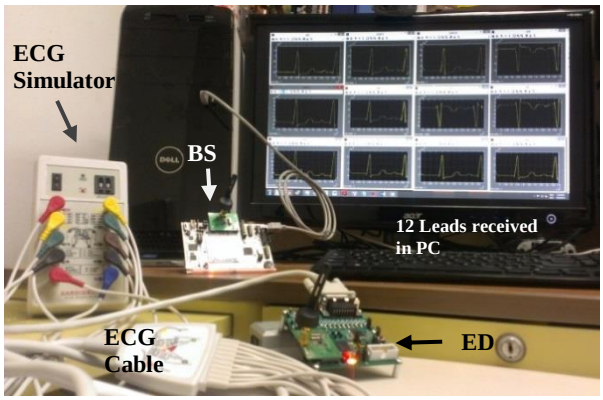

Fig. 27. Measurement setup of the 12-lead ECG WMS.

fixed location while the ED unit, along with the ECG simulator and cable, were moved away. These measurements were made keeping the ED and BS within line of sight, achieving a maximum range of around 35m. While including obstacles, namely walls or furniture between the BS and ED, the maximum link distance decreased to around 27 m. The lifetime (3.7 days) corresponding to the measured current consumption (33 mA) is approximately eight (and two) times better than the one offered by commercial products with similar resolution and range of operation [38, 39]. The measurements are summarized in Table V.

Table V. Summary of measurement results for the presented ECG WMS.

Parameter	**Measured**	**Parameter**	**Measured**
Current Consumption	*33 mA*	**Lifetime**	*88 hours*
Distance(line of sight)	*35 m*	**Distance(obstacles)**	*27 m*

Summary

A 12-lead ECG WMS for continuous cardiac-activity monitoring, including an end device, base station and detection algorithm embedded in a graphical user interface has been presented. The ED was designed to offer portability, high accuracy and long lifetime. The ED control algorithm optimizes the power consumption and allows an increment of 40% lifetime compared with the typical current consumption values of the AFE, MCU and ISM transceiver chips. The basic operation principle of the detection algorithm has been explained. In-vitro testing was successfully performed having line of sight communication between the ED and BS, and including obstacles in the RF path. The system design allows the integration of different RF transceivers and future firmware updates in case a longer range is desired.

CHAPTER IV

A FULLY INTEGRATED ULTRA-LOW-NOISE/LOW-POWER BIOPOTENTIAL AMPLIFIER FOR ECG APPLICATIONS

Introduction

The use of wireless medical systems (WMS) for patient monitoring and medical diagnostic is becoming a common practice in modern medicine [40]. Examples of this kind of systems are electrocardiogram (ECG), electromyogram (EMG) or electroencephalogram (EEG) monitors, used to characterize the electrical behavior of the human heart, muscles and neural system respectively [23]. Modern ECG applications are based on wearable equipment designed to have small size, low power consumption and therefore long lifetime. Typically, an ECG wave has an amplitude of 0.7 mV to 5 mV, thus developing a high sensitivity to thermal and flicker noise, common mode signals and different types of interference (electrical, magnetic, electrostatic or electromagnetic) present within the bandwidth of interest [41]. Therefore, the biopotential amplifier or bioamp is a critical design block of ECG WMS for patient monitoring.

Integrated solutions using approaches based on transistors operating in weak-inversion [42], switching capacitors [43], chopping modulation [44] or current balancing amplifiers [45] have been reported in the literature. The approach in [42] presents a modest thermal noise while consuming less than a micro-watt. Nevertheless, it doesn't deal with the presence of flicker noise thus leading to a relatively high input referred noise. The solution presented in [43] comes at the expense of higher power and the

introduction of parasitic effects from the switched capacitor circuitry [46]. The approach described in [44] offers a good solution for flicker noise reduction at the price of reduced input impedance and needs external capacitors to achieve the desired frequency response. Finally, the use of current balancing amplifiers in [45] leads to a good common mode rejection ratio (CMRR) at the expense of extra power and also requires the inclusion of external components.

This chapter presents a fully integrated ultra-low-noise/low-power differential chopped amplifier with input impedance boosting and low high-pass cut-off frequency. These features combine the strengths of some of the aforementioned approaches while minimizing their weaknesses. The use of a negative capacitance generator (NCG) [47] at the input of the core amplifier compensates the input impedance degradation due to chopping modulation. A T-network composed of MOS-bipolar pseudo-resistors and a transistor operating in triode region is used to achieve a large RC time constant, resulting in higher DC rejection and lower flicker noise corner. Finally, the core amplifier (OTA) is designed with transistors operating in weak inversion to increase the bioamp current efficiency. The chapter organized as following: section B presents a system-level analysis of the amplifier, providing an overview of the building blocks and illustrating the main idea behind this work. Section C describes the implementation of the different blocks as well as relevant design equations. Section D discusses the experimental results of the designed bioamp and compares its performance with similar works presented in literature. Finally, section E concludes the chapter.

System-Level Analysis

Bioamp Architecture

The block diagram of the proposed biopotential amplifier is depicted in Fig. 28. The input signal is originated by ECG electrodes that translate ion-based current from the human body into electron-based current, allowing the detection of a differential voltage between two electrodes (limb leads) or between an electrode and reference voltage (precordial leads) [23]. The generated voltage, the differential electrode offset (DEO) and common mode signals such as 60/50 Hz noise, electrostatic or electromagnetic interference [41] become the bioamp's input voltage, V_{in} add equation.The chopper modulator at the input of the core amplifier transposes V_{in} to the odd harmonics of the chopping frequency f_{chop} , away from the where the OTA's *1/f* noise and systematic offset are located in the frequency spectrum [46]. The chopping signal is provided externally and a non-overlapping clock generator supplies two out-of-phase clock signals to drive the chopper modulators. At this point, V_{in} faces the NCG, a block that allows the use of large input transistors in the OTA (for better thermal noise

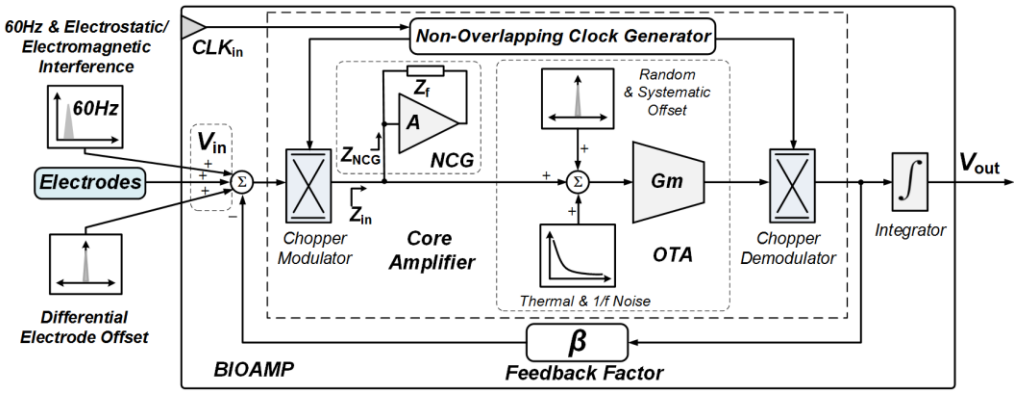

Fig. 28. Block diagram of the biopotential amplifier.

performance) without compromising the effective input impedance of the core amplifier after the inclusion of the chopper modulator. The noise from the NCG block is a common-mode signal for the OTA. Nevertheless, this extra noise won't affect the signal of interest since the CMRR of the OTA by itself depends on transistor matching [48] yielding to a large rejection for common-mode signals . More details on the NCG issues will be discussed on the following sections. Since the noise and offset of the OTA can be considered to be non-correlated, they are represented as two independent signals added to V_{in} at the input of the OTA. Due to the action of the input chopper modulator, the amplification of V_{in} happens at f_{chop}, a region where there is no *1/f* or systematic offset [46]. A chopper demodulator brings the amplified version of V_{in} back to its original frequency location while the low frequency non-idealities of the OTA are modulated to the odd harmonics of f_{chop}. A lossless integrator load along with the OTA's effective transconductance define the low-pass cut-off frequency of the bioamp. This eliminates the need of an anti-aliasing filter for posterior analog to digital conversion and at the same time prevents the fold-over of the chopping spikes at the output generated due to charge injection from the input chopping switches [46].The transfer function resulting from the core amplifier and the feedback factor yields to a band-pass frequency response, providing the necessary AC coupling to remove the DEO component from V_{in}.

The block diagram from Fig. 28 is mapped into the circuit presented in Fig. 29 where the core amplifier includes the chopper modulators and the NCG units. The feedback factor is implemented by the integrated passive elements C_1, R_T and C_2. The rejection of the common-mode components present in V_{in} depends mainly on the

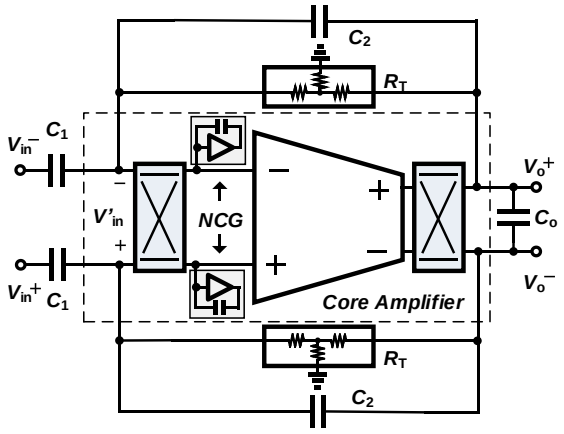

Fig. 29. Schematic diagram of the biopotential amplifier.

mismatch percentage of C_1 and C_2. This percentage is typically low for integrated components. Moreover, CMRR values above 80 dB have been reported for two employing a similar feedback network [42].

Control System Block Diagram and Chopping Modulation

The circuit presented in Fig. 30a displays a single-ended (SE) version of the bioamp from Fig. 29 without the chopping modulators and the NCG block. This circuit is used to obtain the control block diagram on Fig. 30b where the core amplifier and feedback factor present the transfer functions of the transconductance stage and the passive network**.**

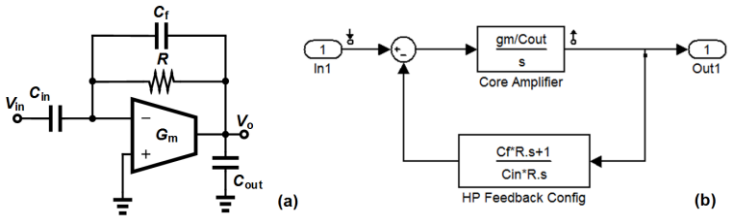

Fig. 30. Single-ended bioamp: a) schematic diagram and b) control system block diagram.

The control block diagram in Fig. 30b works well as a first approximation to determine the required transconductance and passive components for the ideal case. Nevertheless, the offset and noise of the transconductance stage along with the DEO should be taken into account to provide a more accurate model. In Fig. 31a, the SE schematic diagram includes the chopper modulators while Fig. 31b presents a more complete control system block diagram including the noise and offset effects mentioned before to allow us observe the effects of the chopping modulators on these non-idealities.

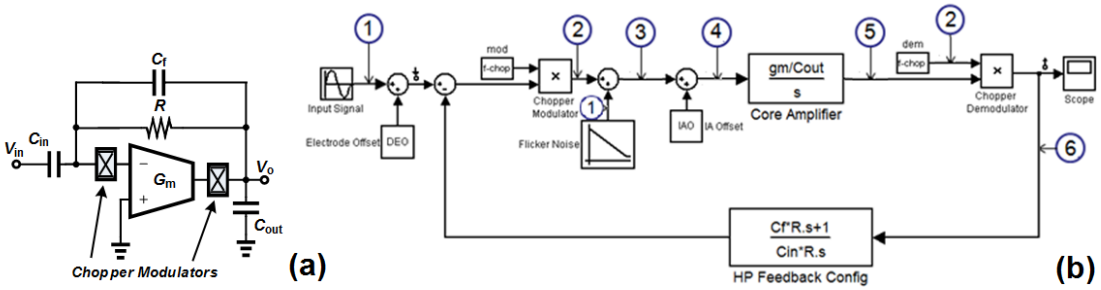

Fig. 31. Single-ended bioamp with choppers: a) schematic diagram and b) control system block diagram including signal and transconductance offset and noise.

Chopper Stabilization Technique: Basic Concepts

The operation of the chopper modulation technique is described in Fig. 32 where the input signal X(f) and an ideal amplifier denoted as AMP with noise components, flicker and thermal, represented by the additive function N(f) are presented. The square wave modulation signal m(t) with frequency f_{chop} shifts the frequency spectrum of X(f) to the odd harmonics of f_{chop} as shown in X(f)⊗m(t). Then, the modulated input signal and N(f) are added together (X(f)⊗m(t)+N(f)) and amplified by AMP. In an ideal case, the

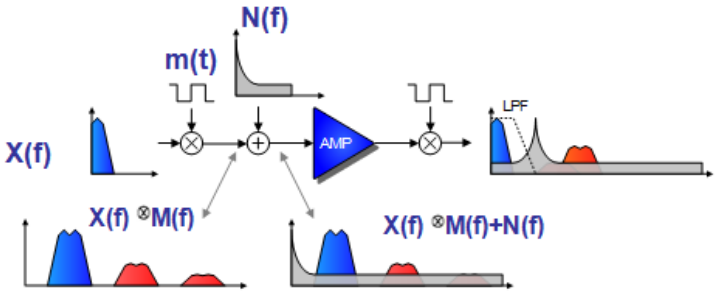

Fig. 32. Operation principle of the chopper modulation technique.

amplifier's gain is constant at all frequencies and there are no limits on the selection of f_{chop} . In practice, the amplifier has a low-pass filter behavior forcing f_{chop} to be located at least at half of the f_{3dB_AMP}, the 3dB frequency of the amplifier, in order to provide linear gain to X(f) now located at f_{chop} . Notice that if X(f) wasn't modulated by m(t) it would be located around N(f) making almost impossible to amplify the signal without being affected by the offset and noise of the amplifier. Therefore by moving the signal from its original low-frequency location to f_{chop}, it is possible to mitigate the effects of 1/f noise and offset. The best results are offered by selecting a higher f_{chop} but as mentioned before, the location of the chopping frequency is set by f_{3dB_AMP}. Therefore, a trade-off between power and noise arises and the designer should choose f_{chop}. More details on this issue are presented later in this chapter. At the output of AMP, the amplified version of X(f)⊗m(t)+N(f) faces the chopper demodulator that brings X(f) back to its original frequency while the 1/f noise is transposed to f_{chop}. For the case where the amplifier gain is not limited in frequency, replicas of the amplified input signal as well as the 1/f noise remain at odd harmonics of *fchop*. These non-wanted signals can be removed by a low-pass filter.

Effects of Chopper Stabilization in the Proposed Bioamp

The block diagram in Fig. 31b includes several numbers located at "points of interest" also displayed in Fig. 33 to observe the behavior signal in the time and frequency domains. Number 1 is the input signal with frequency f_{in} plus the 1/f noise model. Notice that the input signal level is significantly comparable with the level of the noise. Number 2 shows the chopping square signal. Number 3 shows the chopped input signal plus 1/f noise. Number 4 shows number 3 after the addition of the offset of the amplifier (IAO). Number 5 shows the amplified version of number 4. Finally, number 6 shows the filtered output.

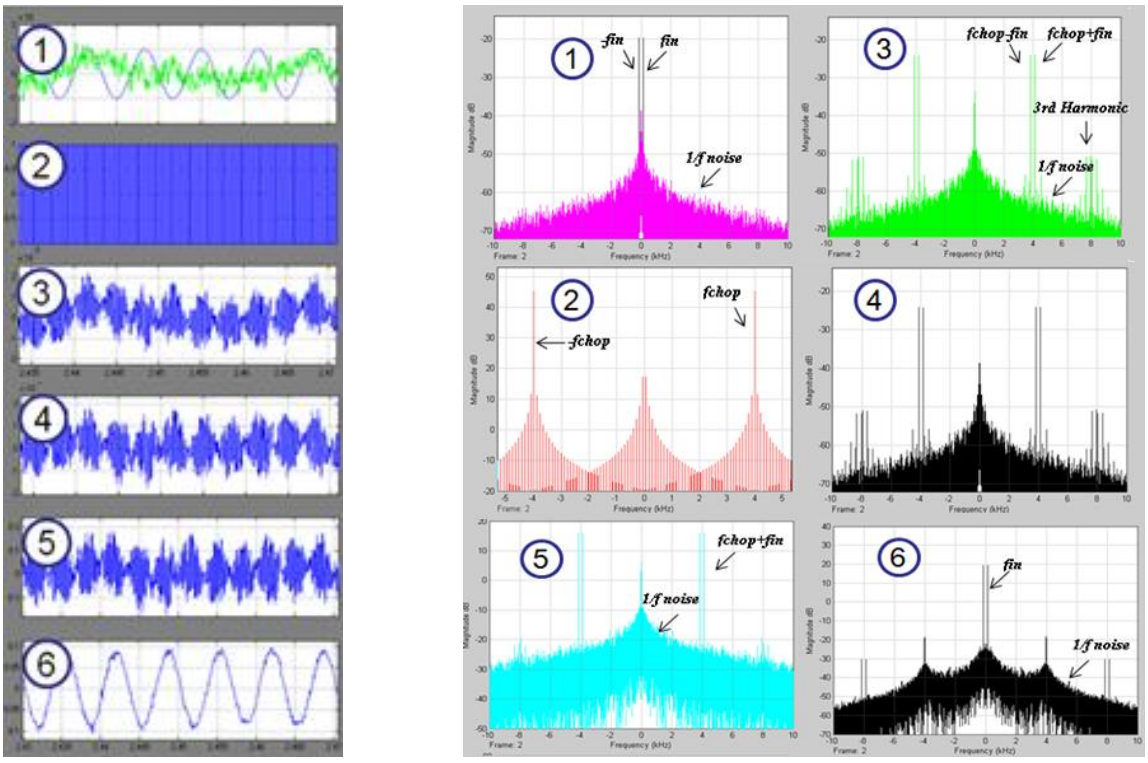

Fig. 33. Transient and frequency response of the block diagram from Fig. 31b.

From these simulations it can be observed that the chopping modulation technique allows an amplifier block to provide a "clean" amplification even with the noise and input signal amplitude levels being similar. Also, this simulation demonstrates how the same amplifier can provide the output low-pass filtering required to remove unwanted spectral content that results from the odd harmonics of *fchop.*

Noise-Power Trade-off Between the Chopping Frequency f_{chop} and the Amplifier's 3dB Frequency f_{3dB_AMP}

In the previous sub-section it was mentioned that in practice, an amplifier has a frequency response with constant gain at up to certain frequency f_{3dB_AMP} where a 20 dB/decade roll-off occurs. It was also mentioned that the signal of interest is amplified at f_{chop} where the effects of offset and 1/f noise are ideally non-existent and that in order to provide linear amplification the gain at f_{chop} should be constant. Therefore, one of the conditions to implement the chopping technique in an amplifier is that $f_{3dB\_AMP} > f_{chop}$.

From the previous analysis it can be inferred that the best 1/f noise and offset rejection would happen for high values of f_{chop}. Taking into account this consideration along with the relationship between f_{3dB_AMP} and f_{chop} for proper operation of the chopping technique, it is possible to conclude that there is a proportional relationship between the power required to design an amplifier with high f_{3dB_AMP} and the amount of 1/f noise (and offset) reduction that can be achieved. Therefore, it is possible to design the OTA block from Fig. 29 with certain f_{3dB_AMP} depending on the noise specifications and the required f_{chop} to achieve that specification.

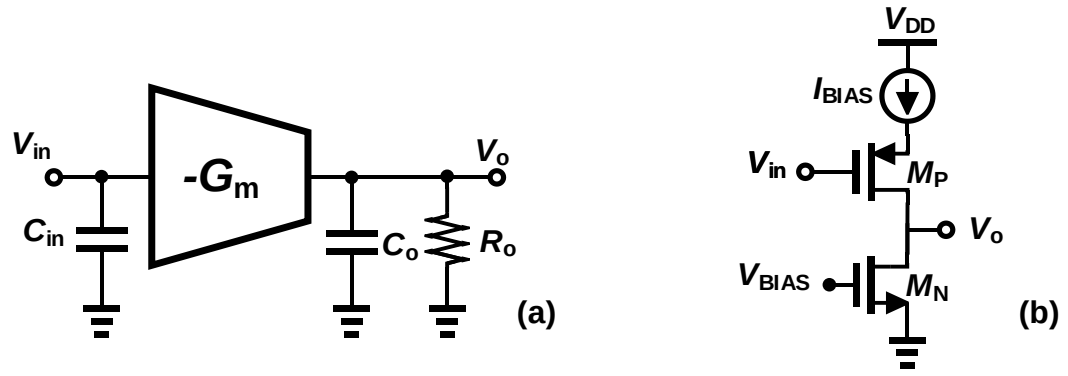

Fig. 34. Schematic diagram of a general transconductance stage: a) block diagram of including equivalent input and output impedances, b) transistor-level diagram.

In order to provide design insight for the OTA block from Fig. 29 power trade-off of a general transconductance stage can be analyzed. The circuits in Fig. 34 shows the block and transistor level diagram of a single-ended PMOS in common source configuration providing a frequency dependent gain defined by

$$\frac{V_o(s)}{V_{in}(s)} = -\frac{A_o}{\frac{s}{\omega_o}+1} = -\frac{G_m R_o}{sR_oC_o+1} = -\frac{g_{mP}}{g_{oN}}\frac{1}{s\frac{C_o}{g_{oN}}+1} \tag{4.1}$$

where A_o, $R_o = \frac{1}{g_{oN}}$ and C_o are DC voltage gain, equivalent output resistance and output capacitance of the transconductance stage respectively. From (4.1) the gain bandwidth product (GBW) can be defined as

$$GBW = A_o\omega_o = \frac{G_m}{C_o} = \frac{g_{mP}}{C_o} \tag{4.2}$$

while the input referred noise of the circuit is given by

$$v_{in}^2 = \frac{8}{3}\frac{kT}{g_{mP}}\left(1+\frac{g_{mN}}{g_{mP}}\right). \tag{4.3}$$

Moreover, the MOS transistor quadratic equation suggests that

$$g_{mP} = \sqrt{2\ k'_p \frac{W_P}{L_P} I_D} = \alpha_P \sqrt{I_{BIAS}} \tag{4.4}$$

$$I_{BIAS} = \frac{g_{mP}^2}{\alpha_P^2} = \frac{g_{mN}^2}{\alpha_N^2} \tag{4.5}$$

$$R_o \approx \frac{1}{g_{oN}} \approx \frac{1}{\lambda I_D} \approx \frac{1}{\lambda I_{BIAS}} \tag{4.6}$$

therefore, it is possible to relate the GBW (and thus the pole location), noise and current consumption of the OTA stage based on the transconductance $G_m = g_{mP}$.

Input Impedance of the Core Amplifier

Fig. 35a depicts the interaction between the chopping modulator and C_{in} representing the equivalent impedance Z_{in} after the modulator. Z_{in} is mainly composed of C_{gs1}, the gate-to-source capacitor of the OTA input transistors, and Z_{NCG}, this is shown in (4.7).

$$Z_{in} = \frac{1}{sC_{in}} \approx \frac{1}{sC_{gs}} // Z_{NCG} \tag{4.7}$$

The switching transistors of the chopping modulator along with C_{in}, create a parasitic switched-capacitor (SC) resistor R_p [44] at the input of the core amplifier, effectively reducing its input impedance. The circuit in Fig. 35b is used to illustrate this effect while presenting the single-ended (SE) version of the bioamp including R_{in}, the equivalent SE input parasitic resistance defined by (4.8).

$$R_{in} = \frac{R_p}{2} = \frac{1}{4C_{in}f_{chop}} \tag{4.8}$$

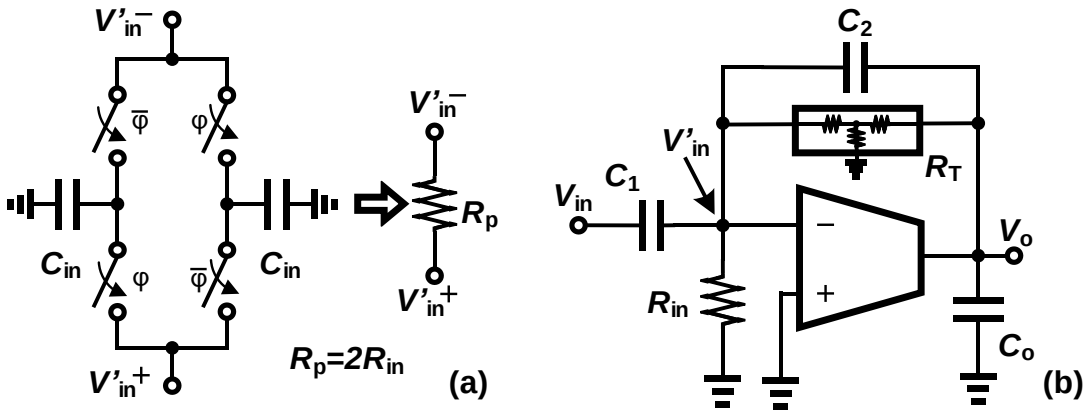

Fig. 35. a) SC circuit generating R_p, b) SE representation of the bioamp including the parasitig input resistance R_{in}.

Assuming that the OTA has a finite gain, the bioamp transfer function including the effect of R_{in} is found to be:

$$\frac{V_o(s)}{V_{in}(s)} = -\frac{C_1}{C_2}\frac{sC_2(R_T // R_{in} A_o)}{[sC_2(R_T // R_{in} A_o)+1]}\frac{1}{\left[s\frac{C_o C_1}{G_m C_2}+1\right]} = -\frac{C_1}{C_2}\frac{s/\omega_{HP}}{[s/\omega_{HP}+1]}\frac{1}{[s/\omega_{LP}+1]} \quad (4.9)$$

Using (4.9) it is possible to study the impact of R_{in} in the bioamp operation but first the expected behavior should be defined. This can be done by making R_{in} infinite, yielding to a mid-band gain given by the ratio of C_1 and C_2 and high/low-pass cut-off frequencies equal to $\omega_{HP}=1/C_2R_T$ and $\omega_{LP}=G_mC_2/C_1C_o$ respectively. For a gain of 40 dB with $f_{HP}\approx 0.05$ Hz and $f_{LP}\approx 160$ Hz, the values of C_1, C_2, C_o, R_T, and G_m are considered to be 20pF, 200fF, 20pF, 16 TΩ and 2μA/V respectively. The transfer function in (4.9) was evaluated for C_{in} values from 0.1pF to 5 pF with f_{chop} set to 4 kHz. The results are

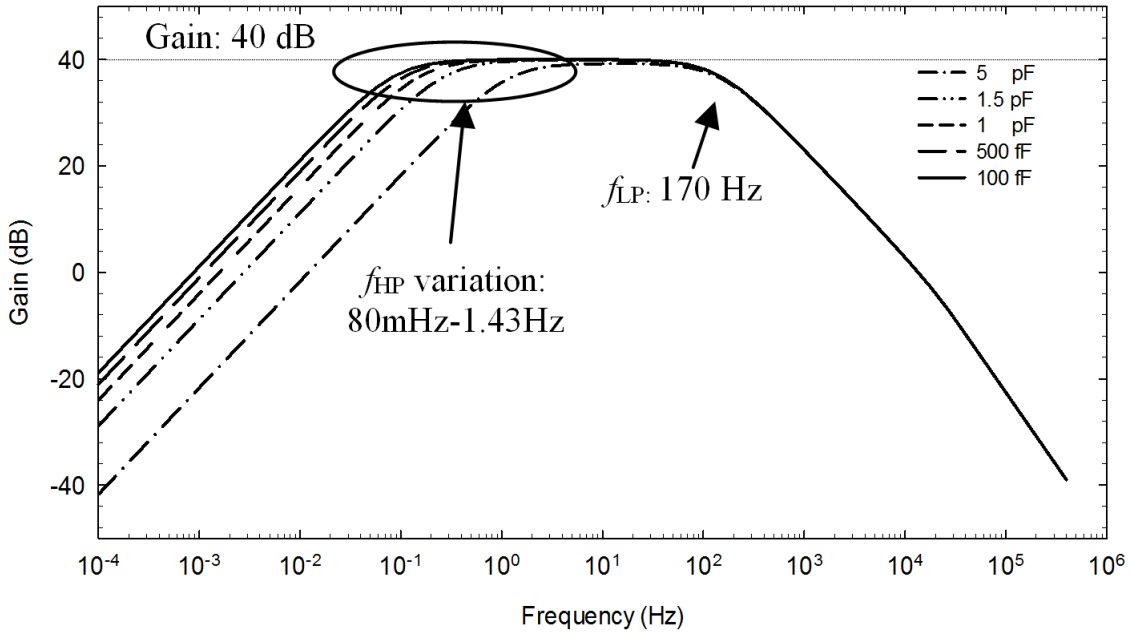

Fig. 36. Frequency response of the SE bioamp for different values of C_{in}.

presented in Fig. 36 and show that ω_{HP} is significantly dependent on C_{in}. Therefore, C_{in} should be as small as possible in order to obtain a low ω_{HP}. Notice that if C_{in} solely depended on C_{gs1}, the OTA thermal noise optimization would be restricted for the bioamp to operate properly. Nevertheless, looking back to (4.7), a way to reduce C_{in} is to make Z_{NCG} a negative capacitance added to C_{gs1}. This task is performed by the NCG block from Fig. 28, where a gain stage with an impedance Z_f connected in positive feedback takes advantage of the Miller effect [47] to obtain an equivalent Z_{NCG} defined by (4.10).

$$Z_{NCG} = \frac{Z_f}{1 - A(s)} = \frac{1}{sC_f}\frac{1}{[1 - A(s)]} \tag{4.10}$$

Limitations for Stable Operation

Fig. 37 presents the block diagram of a system with frequency response given by $A(s)$ with a block with behavior described by β connected in positive feedback. The transfer function of the system is given by

$$P(s) = \frac{x_o(s)}{x_{in}(s)} = \frac{A(s)}{1 - \beta A(s)} = \frac{1}{\beta}\frac{T(s)}{1 - T(s)} \tag{4.11}$$

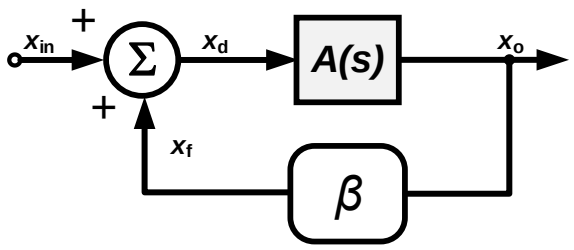

Fig. 37. Block diagram of a system connected in positive feedback.

This equation implies that since if the loop gain is already in phase with the input when $|T(j\omega)|$ is equal or larger to 1, the magnitude of $P(s)$ goes to infinity and then, the circuit can amplify its own noise until it eventually oscillates. In other words, if $|T(j\omega_1)| \geq 1$ and $\angle T(j\omega_1) = 0^o$, the circuit may oscillate at a frequency ω_1. Compared with a system connected in negative feedback, in this case there is no need of extra 180^o for the circuit to meet the oscillation condition; therefore a system connected in positive feedback is very susceptible to sustained oscillation.

After understanding the oscillation criterion for a system in positive feedback it is possible to analyze the stability of the NCG block from Fig. 28. Since the circuit is to be used as NCG, the stability of its input impedance,$Z_{NCG}(s)$, is examined instead of its transfer function. The NCG amplifier is modelled as a frequency-dependent transconductance stage and is presented in

Fig. 38a and Fig. 38b where Z_{in-OTA}, Z_f, G_{m-NCG}, R_o and C_o are the input capacitance of the core amplifier OTA from Fig. 28, the feedback impedance that defines the negative capacitor, the transconductance of the NCG-OTA and the output capacitance/resistance of the NCG-OTA.

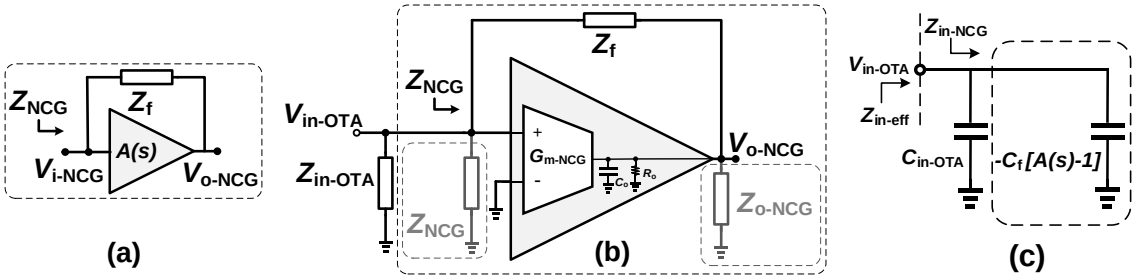

Fig. 38. NCG block: a) simple representation, b) detailed schematic diagram.

Replacing A by A(s) in (4.10) yields to

$$Z_{NCG}(s) = \frac{1}{sC_f}\frac{1}{\left(1 - A(s)\right)} = \frac{1}{sC_f}\frac{1}{\left(1 - \frac{G_{m-NCG}R_o}{sR_oC_o + 1}\right)} = \frac{1}{sC_f}\frac{1}{\left(1 - \frac{A}{\frac{s}{\omega_o} + 1}\right)} \tag{4.12}$$

$$= \frac{1}{sC_f}\frac{\frac{s}{\omega_o} + 1}{\frac{s}{\omega_o} + (1 - A)}$$

and the phase of the denominator will approach to zero when A = 1 . Also, when $A \geq 1$ the system would include a pole located at the right-half plane in the imaginary axis, resulting in an exponentially increasing response. Therefore, the NCG circuit by itself is not stable. Fortunately, the NCG is to be connected in parallel with $Z_{in-OTA} = \frac{1}{sC_{in-OTA}}$ resulting in the circuit presented in

Fig. 38c. The resulting input impedance of the OTA would be

$$Z_{in-OTA}(s) = \frac{1}{sC_{in-OTA} + sC_f\left(1 - A(s)\right)} \tag{4.13}$$

$$= \frac{\frac{s}{\omega_o} + 1}{s^2\left[\frac{C_{in-OTA}}{\omega_o} + \frac{C_f}{\omega_o}\right] + s[C_{in-OTA} + C_f(1 - A)]}$$

where the stability condition can be found looking at the values that would yield to a right-half pole, this is

$$C_{in-OTA} > C_f(A - 1)\,. \tag{4.14}$$

This equation demonstrates that the reduction of C_{in-OTA} reaches a limit where the input impedance can become unstable or completely negative, a condition that should be avoided. Since the value of C_{in-OTA} is dominated by the gate to source capacitance, even though it can be estimated by simulation, the best practice would be to include a capacitor bank for C_f targeting for a cancellation of less than the total value of C_{in-OTA} to avoid stability issues.

Limitations for Effective Input Impedance Boosting

The expression in (4.12) suggests that the effective value of the negative capacitance depends on the 3dB frequency of the NCG amplifier ($\omega_o = 2\pi f_o = 1/R_o C_{o-Eff}$ where $C_{o-Eff} = C_o + C_f (1 - 1/A)$) because the DC gain A will start decreasing after f_o. Notice that for low values of A , the output capacitance of the NCG amplifier will also be affected by the feedback capacitor, effectively reducing ω_o. Since the goal of adding the NCG block is to minimize the input capacitance of the OTA in order to increase the effective input impedance degraded after the inclusion of the chopper modulators, as shown in (4.9), the negative capacitance should operate properly at the chopping frequency. Therefore in order to effectively boost the input impedance of the OTA the NCG amplifier pole should be higher than the chopping frequency. This is shown in the following equation

$$f_o > f_{chop}. \tag{4.15}$$

Component Selection

From (4.12) it is also possible to conclude that different values for A and C_f can result in the same negative capacitance. For instance, to generate -100fF capacitor, the values of

A and C_f can be: 2 and 100fF, 3 and 50fF or 5 and 25fF. From this example the trade-off between the power of the NCG amplifier and the area and accuracy of the feedback capacitor can be observed. The relationship between current consumption and transconductance presented in (4.4) can be used to estimate the power burned by the NCG amplifier for different gains. Using the current as basic variable along with different gain and feedback capacitance values it is possible to find an optimum value for these variables to generate a given negative capacitor. This is shown in Fig. 39 where the X-axis is the gain of the NCG amp, the Y-axis shows the value of the feedback capacitor and the Z axis presents the equivalent negative capacitor value.

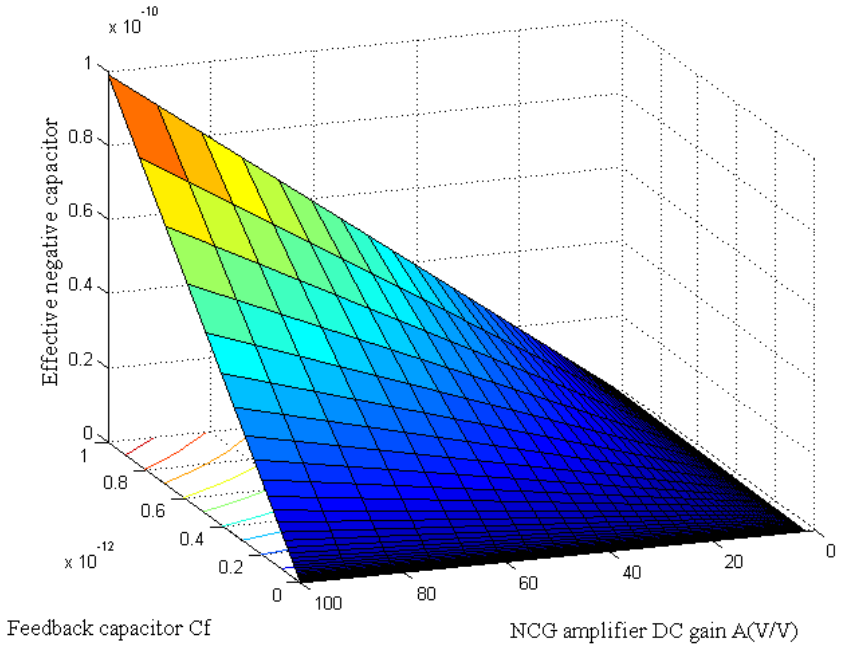

Fig. 39. Design trade-off for NCG amplifier gain, feedback capacitor Cf and effective negative capacitance.

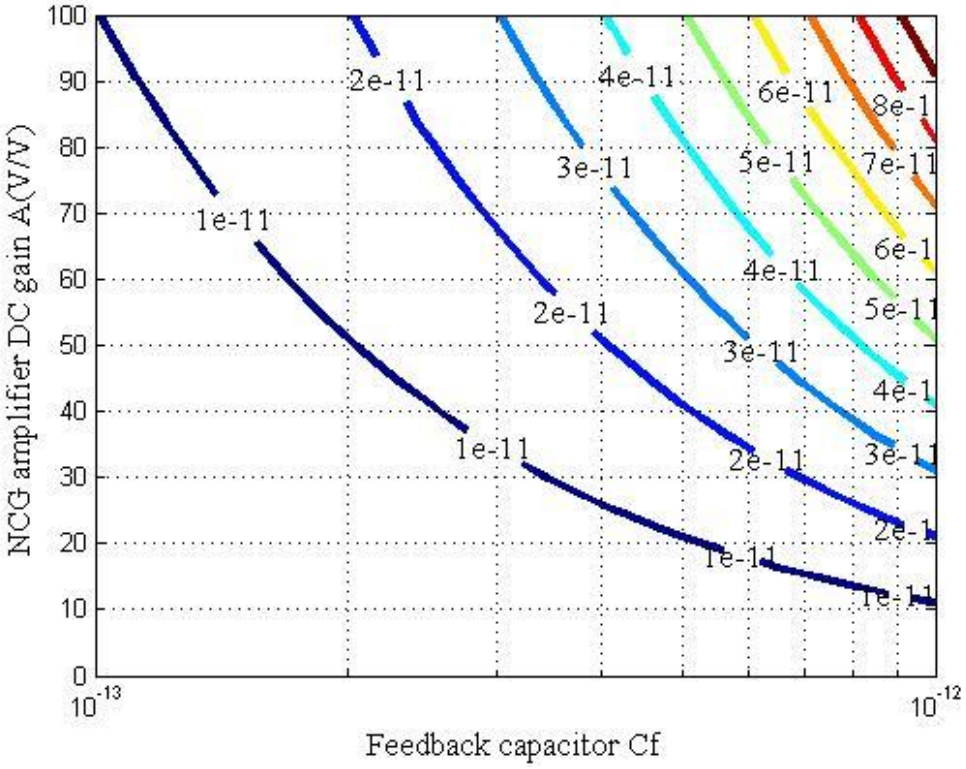

Fig. 40. Feedback capacitor Cf-NCG amplifier gain plane with different effective negative capacitance results.

Depending on the power or area limitations, the best set of feedback capacitor and gain values to generate the effective negative capacitor can be selected from the different contours presented in Fig. 40.

Design Considerations

The discussion presented on the previous subsections can be summarized in three critical design considerations in order to implement a functional bioamp based on the proposed architecture. First, f_{chop} should be smaller than the 3dB frequency of the OTA and larger than its *1/f* corner in order to have linear and *1/f* noise-free amplification [46]. Second, $C_{in\text{-}OTA}$ should be small enough to avoid the effects of R_P on the overall frequency response of the bioamp without compromising its noise performance. This can be done using the NCG block where the cutoff frequency of the amplifier f_o should be larger than f_{chop} . Finally, on-chip passive components should be used for the feedback network to ensure proper rejection of the common-mode components of V_{in}.

Circuit Implementation

Core Amplifier

Fig. 41 shows the implementation of the OTA used in the bioamp. The circuit is designed to optimize the noise performance for a given power consumption while

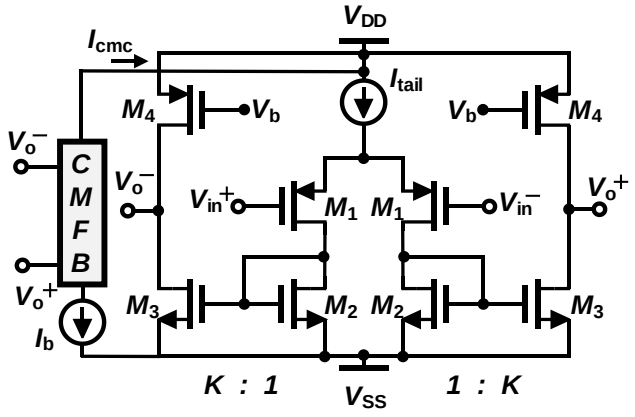

Fig. 41. Transistor-level implementation of the OTA used in the core amplifier.

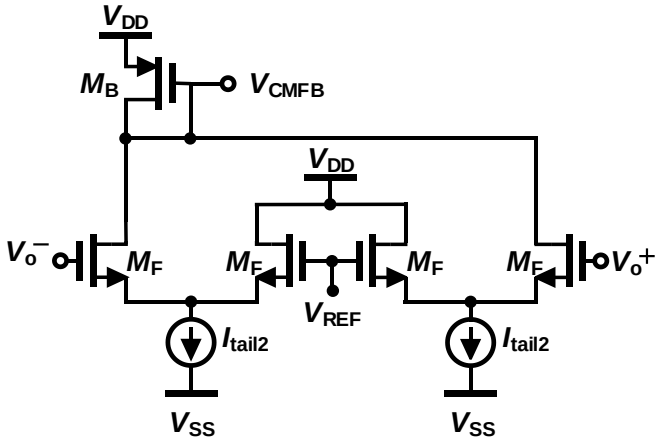

Fig. 42. Common-mode feedback circuit for the OTA shown in Fig. 41.

keeping the bandwidth large enough for proper chopping operation. A two-differential pair common-mode voltage sensor is used to realize the CMFB block and its schematic diagram is shown in Fig. 42. The input-referred noise of the OTA circuit is given by (4.16) and the frequency dependent transconductance is presented in (4.17), where *K* is the mirroring factor between *M2* and *M3*, and ω_D/ω_{ND} are the OTA's dominant/non-dominant poles defined in (4.18).

$$v_{in}^2 = \frac{16}{3}\frac{kT}{g_{m1}}\left(1 + \frac{g_{m2}}{g_{m1}} + \frac{g_{m3} + g_{m4}}{K^2 g_{m1}}\right) \tag{4.16}$$

$$G_m = K\,\frac{g_{m1}}{\left(1 + \frac{s}{\omega_D}\right)\left(1 + \frac{s}{\omega_{ND}}\right)} \tag{4.17}$$

$$\omega_D = \frac{g_{o3} + g_{o4}}{C_{o3} + C_{o4}} \qquad \omega_{ND} = \frac{g_{m2}}{C_{gs2}(1 + K)} \tag{4.18}$$

Using the EKV model [49] or the "one equation all-regions" (also known as ACM) model [50] [51] it is possible to size MOS transistors operating in weak inversion with extremely small bias currents, which is the scenario for the proposed amplifier. The circuit is designed to obtain the transconductance proposed in section B.3 given by

$$g_m = \frac{kI_D}{U_T}\frac{2}{1+\sqrt{1+4\cdot \mathrm{IC}}} \tag{4.19}$$

where I_D is the drain current, k is the sub-threshold slope factor (approximately 0.7 [42]) and equivalent to $1/n$ from the ACM model and $U_T$is the thermal voltage (26 mV at room temperature). The last term, IC, is known as the inversion coefficient given by the ratio between the drain current and the moderate inversion characteristic current as shown in (4.21) where the carrier's mobility, gate-oxide capacitance and the transistor's width/length are denoted by μ, C_{ox} and W/L respectively.

$$IC = \frac{I_D}{I_S} = I_D\frac{k}{2\mu C_{ox}U_T^2}\frac{L}{W} \tag{4.20}$$

Therefore, using the EKV or ACM models the inversion level of each transistor can be set by the designer by choosing the sizing ration for a given drain current I_D. For IC values below 0.1 the transistor operates in weak inversion. When IC is located between 0.1 and 10 the transistor operate in moderate inversion while IC values greater than 10 indicate strong inversion operation.

The input transistors (*M1)* are sized to operate in weak inversion, with IC $\approx$ 0.04, in order to obtain a large transconductance while using a low bias current, thus providing the best trade-off between noise and power. Notice that due to the addition of the NCG block the size of *M1* does not affect the frequency response of the bioamp. Factor *K*

from (4.17) is set to one and transistors are sized such that ω_{ND}doesn't affect the stability of the OTA while large lengths were used for *M2/M3* in order to ensure strong inversion operation of the current mirrors for the desired bias current [42]. Finally, the PMOS load *M4* is designed to have a transconductance similar as *M3* in order to obtain the required OTA open-loop gain. Transistors *M1* to *M4* are sized using the equations presented before and the resulting sizing ratios, biasing currents and inversion coefficients are summarized in Table VI.

The simulated frequency response of the OTA is presented in Fig. 43, where the DC gain is around 60 dB (1000 V/V), the dominant pole is located at 4.2 kHz and the gain-bandwidth product is 4.2 MHz. Therefore, for a closed loop gain of 40 dB or 100V/V, the pole moves up to 42 KHz, with constant DC gain up to 10 kHz thus allowing the use of chopping frequencies up this value.

Table VI. Transistor sizing ratios and operating conditions.

Transistor	**W/L (µm)**	**Id (µA)**	**Inversion Coefficient**	**Gm/Id (V^{-1})**
M1	80/2.4	0.160	0.045	25.80
M2, M3	20/240	0.160	11.04	6.97
M4	14/100	0.160	10.75	7.05
M5	5/2.5	-	-	-
M6	80/0.6	-	-	-
M7	7.2/0.6	-	-	-
M8	4/2.4	0.05	0.17	23.41
M9	12/7	0.05	0.27	21.99

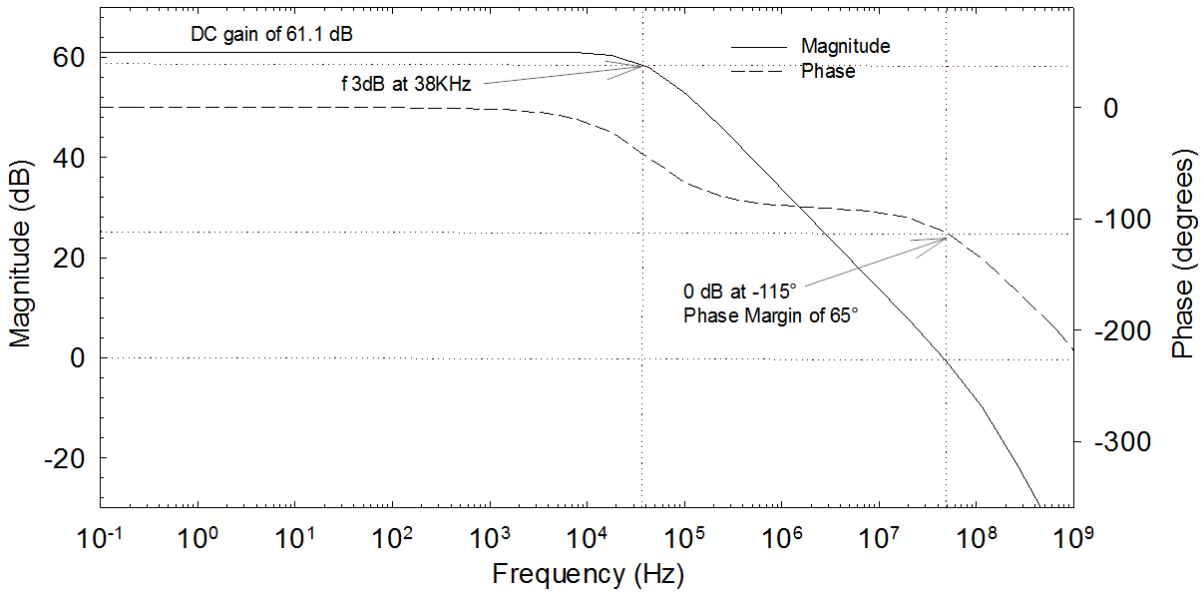

Fig. 43. Frequency Response of the OTA.

High Resistance Implementation (T-network)

Fig. 44 presents the schematic diagram of R_T where R_a, R_b and R_g are connected in *T*-configuration in order to multiply the effective resistance between V_a and V_b [52]. Assuming that either V_a and V_b is connected to a virtual ground (the OTA input terminals for this case) the effective resistance seen across the *T*-network is given by (4.21).

$$R_T = R_a + R_b + \frac{R_a R_b}{R_g} \tag{4.21}$$

The circuit in Fig. 44 also shows the transistor-level realization of R_T where R_a, and R_b are implemented by the MOS-Bipololar PMOS elements [53] generated by

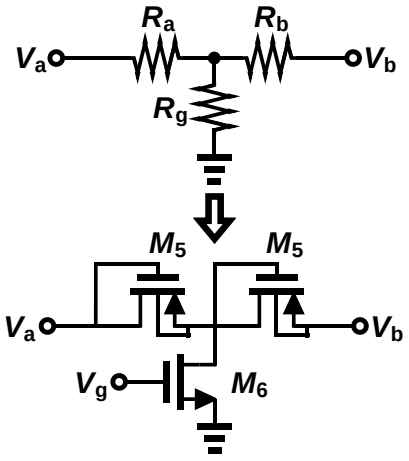

Fig. 44. Schematic diagram and transistor level implementation of R_T.

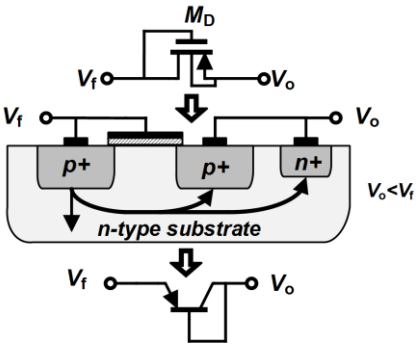

Fig. 45. Principle of operation of the MOS-Biopolar resistive elements.

diode-connected transistors. The operation of these elements transistors is depicted in Fig. 45. For $V_o < V_f$ the p+/n junction is forward biased and the device act as a bipolar transistor with two collectors. Small voltage variations through these elements result invery small current through the transistors producing resistance values in the range of 10^{11} Ω [42]. Resistor R_g is implemented with a transistor operating on the linear region designed to have small resistive value in the order of few hundreds of Ohms to obtain the desired RC constant. Transistor *M6* is sized using equation (4.22).

$$R_g = \frac{L}{\mu C_{ox} W (V_{GS} - V_T - V_{DS})} \tag{4.22}$$

The voltage versus current plot of R_T is presented in Fig. 46 where the effective resistance is in the range of 1TΩ. The sizes of the transistors (M5 and M6) are shown in Table VI.

Chopper Modulator

Fig. 47 shows the double-balanced passive mixer used to implement the chopper modulator. This topology is selected because it doesn't consume power, requires small area and doesn't add significant noise to the design [54]. The modulator should be driven by non-overlapping clock signals to prevent noise leakage with a duty-cycle around 50% to ensure proper modulation [55]. The transistors are sized to obtain a small ON-

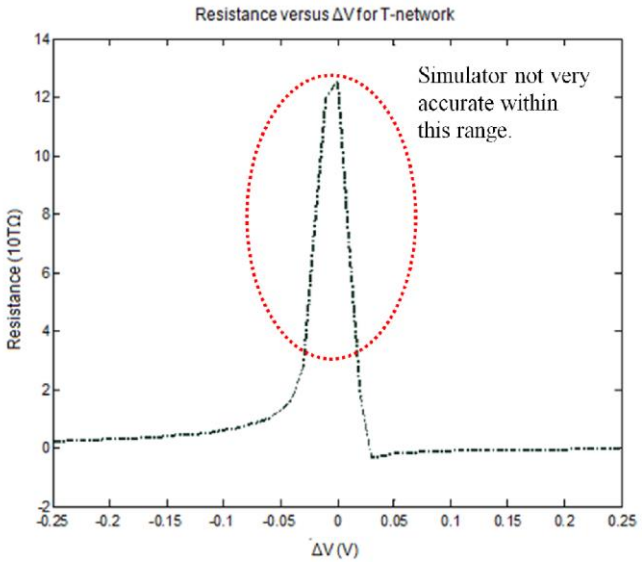

Fig. 46. Pseudo Resistor I vs V characteristics.

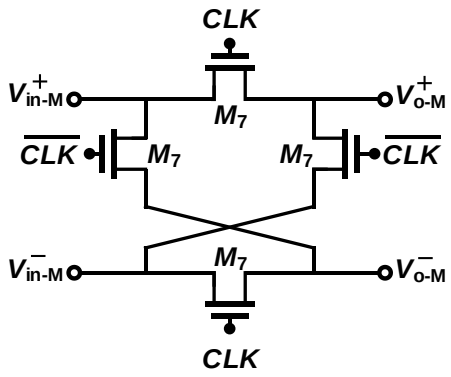

Fig. 47. Transistor-level diagram of the chopper modulator.

resistance (< 1 kΩ) while trying to keep small parasitic capacitances. This, along with the use of a differential topology and low f_{chop} value (4 kHz) effectively minimizes the effects of charge injection and current feed-through inherently present in any switching circuit [46].

Negative Capacitance Generator

Fig. 48 depicts the amplifier stage used to implement the NCG block. The DC gain and input referred noise for the amplifier are presented in (4.23) and (4.24). Although the noise generated by the NCG blocks will appears a common-mode signal for the OTA resulting in a negligible effect in the bioamp noise, *M8* and *M9* are also sized to minimize the input-referred noise using the EKV and ACM model equations presented before. Based on the low-power nature of the circuit and knowing that the input capacitance of the OTA is in the range of hundreds of fF the amplifier gain is selected to be 2 V/V in order to make Z_{NCG}=*-1/*C_f.

$$A = \frac{1}{2}\frac{g_{m8}}{g_{m9}} \tag{4.23}$$

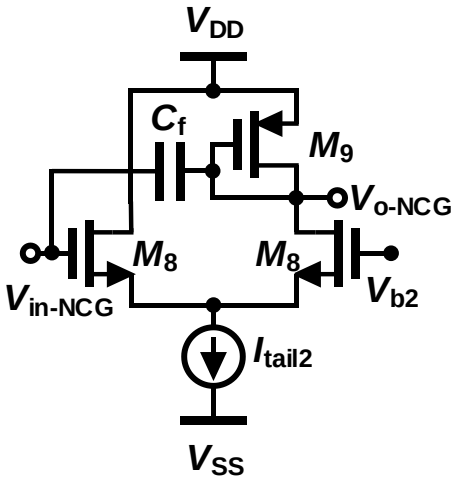

Fig. 48. Transistor-level implementation of the NCG.

$$v_{in}^2 = \frac{16}{3}\frac{kT}{g_{m8}}\left(1+\frac{1}{2}\frac{g_{m9}}{g_{m8}}\right) \tag{4.24}$$

The following figures presents simulation results of the gain of the NCG amplifier along with the magnitude, phase and effective capacitance looking into the input of the NCG circuit for different values of the feedback capacitor C_f . The results in Fig. 49 show that depending on the feedback capacitor value, the effective 3dB frequency of the NCG amplifier will be reduced corroborating the prediction made in section B.3. Similarly, the zero introduced by the feedback capacitor provides a direct path from the input to the output of the amplifier for large feedback capacitor values. The reduction on the amplifier's bandwidth is reflected in the magnitude of Z_{NCG} presented in Fig. 50 where the dominant pole of the amplifier, as shown in (4.13), becomes a left-hand plane zero (due to the positive feedback configuration) for the effective input impedance thus limiting the operating range of the negative capacitor.

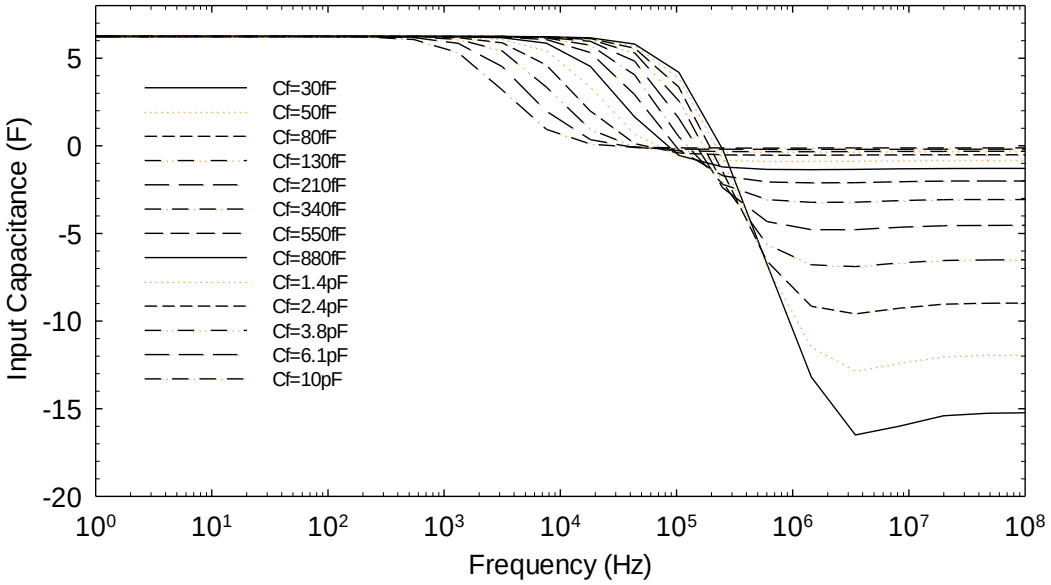

Fig. 49. Frequency response of the NCG amplifier for different Cf values.

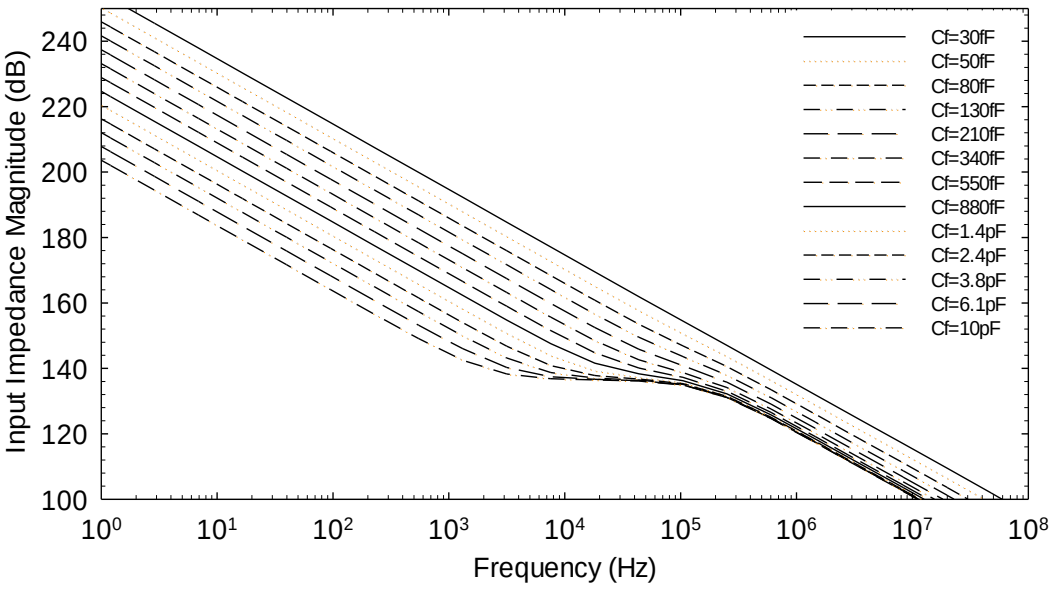

Fig. 50. Magnitude of the impedance looking into the input of the NCG circuit.

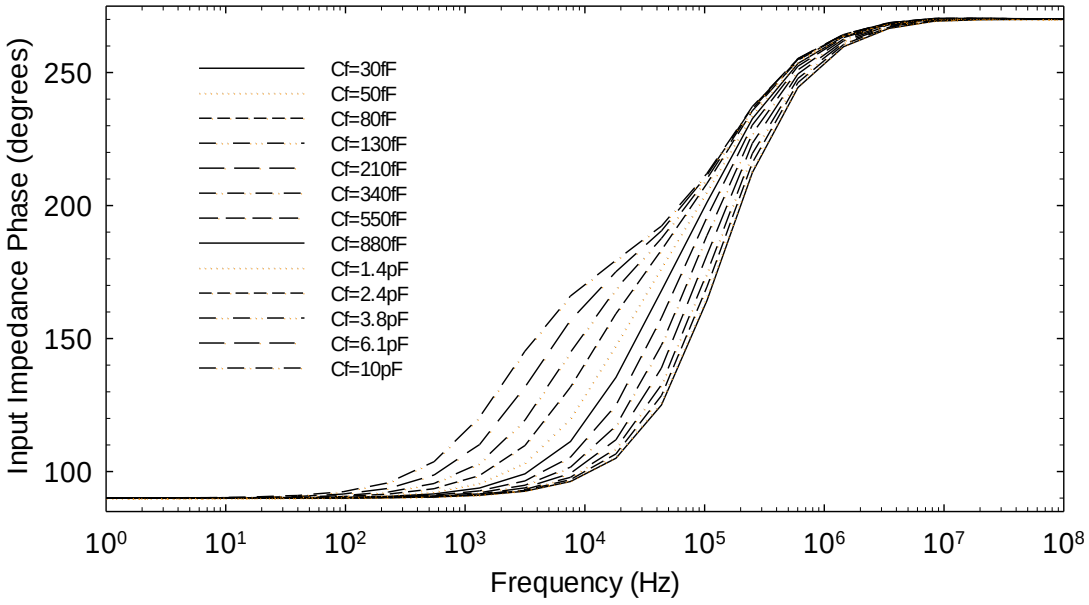

Fig. 51. Phase of the impedance looking into the input of the NCG circuit.

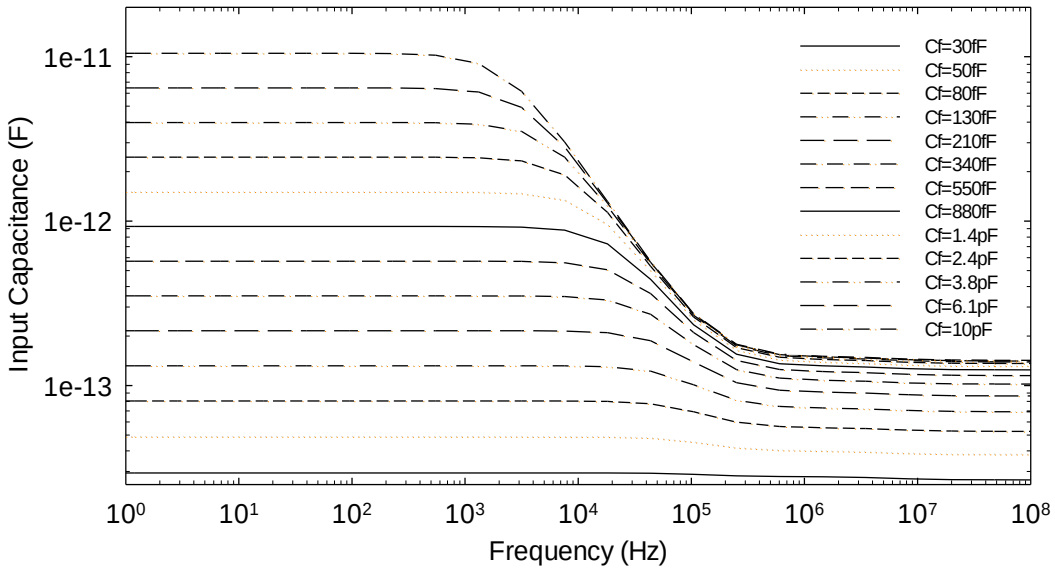

Fig. 52. Effective capacitance looking into the input of the NCG circuit.

Similarly, in Fig. 51 it can be observed that the phase of Z_{NCG} starts moving up from 90 degrees at the effective cutoff frequency of the NCG amplifier.

Finally, the magnitude and phase behavior of Z_{NCG} is summarized in Fig. 52 where the effective negative capacitance value starts dropping at the cut-off frequency of the NCG amplifier.

These results successfully match with the analysis presented in section B.3 allowing its use for other applications of negative capacitance generator circuits.

Non-overlapping Clock Generator

The non-overlapping clock generator used in this work is presented in Fig. 53.As shown in the schematic diagram, the circuit consists of two NAND gates and seven inverters. These logic gates are designed to minimize parasitic capacitance and thus minimize the delay while providing the desired 50% duty-cycle. The transient response of the designed non-overlapping clock generator is presented in Fig. 54.

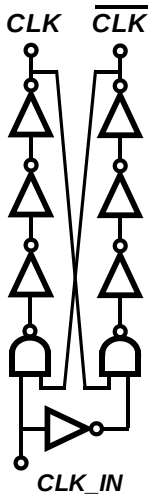

Fig. 53. Schematic diagram of the non-overlapping clock generator.

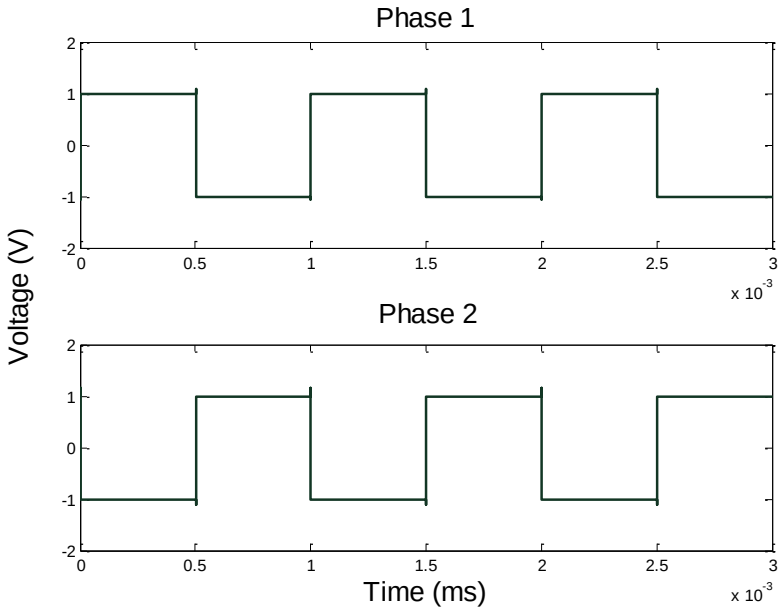

Fig. 54. Transient response of the non-overlapping clock generator.

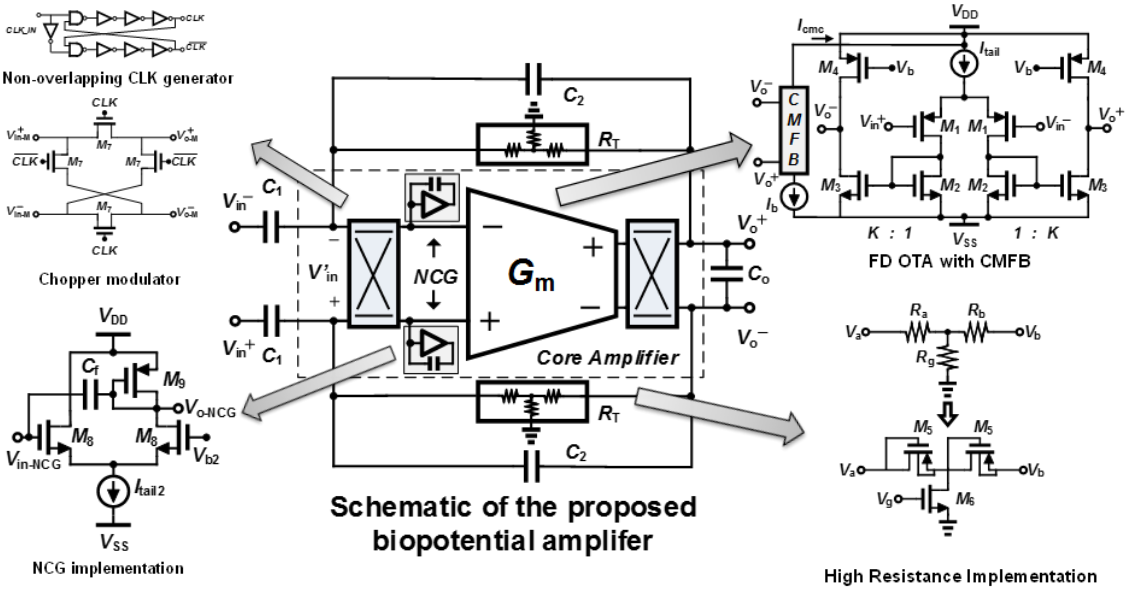

Fig. 55. Complete diagram of the biopotential amplifier including transistor-level schematics of each design block.

Complete Schematic and Transistor-level Diagram

This section concludes with a summary of the different blocks implementing the biopotential amplifier. The diagram in Fig. 55 presents the complete schematic of the bioamp along with the transistor-level implementation of each design block including the fully differential OTA, chopper modulators, non-overlapping clock generator, high resistance implementation and the negative capacitance generator implementation.

Experimental Results and Discussion

The proposed bioamp has been fabricated in the ON Semiconductor 0.5µm, three-metal, two-poly CMOS process. Fig. 56a shows the die microphotograph with active, effective (active + passive) and total areas of 91 μm^2, 360 μm^2 and 2.25 mm^2 respectively. The test PCB is shown in Fig. 56b and includes an off-chip ultra-low-noise SE to differential converter and a highly-linear post-amplifier (PA) in order to characterize the frequency response and to increase sensitivity of the vector signal analyzer (VSA) for the noise measurements.

Circuit Characterization

The measured frequency response of the circuit is presented in Fig. 57 showing a band-pass gain of 40.1 dB with $f_{HP} \approx 0.24$ Hz and $f_{LP} \approx 170$ Hz using C_1 of 200 fF with C_2 and C_o of 20 pF. The location of ω_{LP} and ω_{HP} can be adjusted by varying C_o and C_2, allowing the use of the proposed architecture for acquisition of other biopotential signals such as

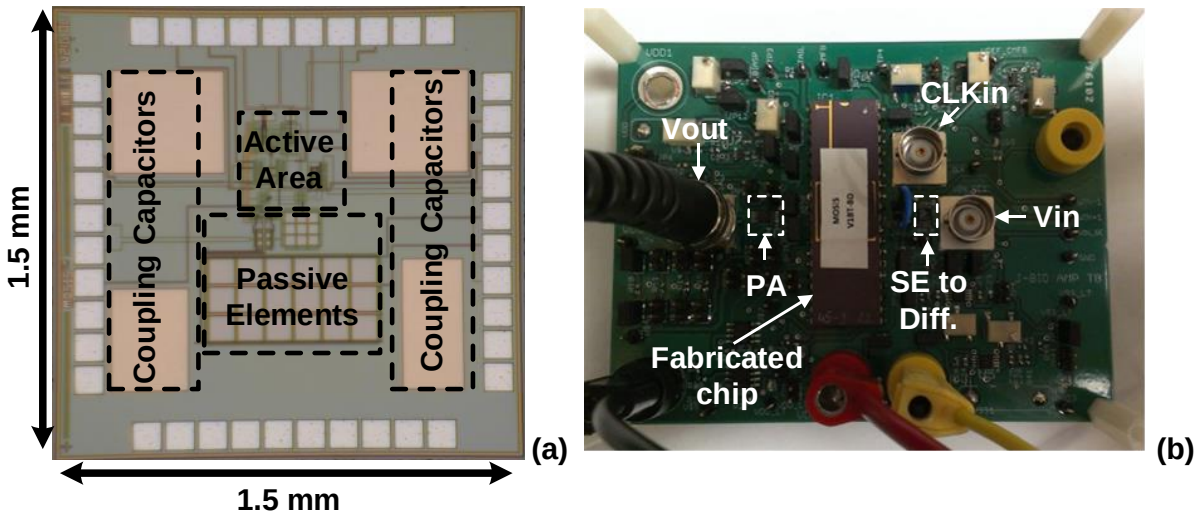

Fig. 56. a) Microphotograph of the fabricated circuit, b) Test PCB.

EMG or EEG. The measured CMRR has a minimum value of 84.3 dB (at 60 Hz) in the band of interest. The HP89410A VSA was used to measure input-referred voltage noise power spectral density of the bioamp, presented in Fig. 58.The thermal noise level of the bioamp is 53V/√Hz and the 1/f corner frequency after chopping was reduced from 2.3 kHz to 3.2 Hz, using f_{chop} of 4 kHz. A bank of capacitors was used to implement C_f, giving the best results for a value of 0.9 pF. The bioamp is biased with tail currents of I_{tail}= I_b 320 nA, while the NCG and clock-generator blocks consume approximately 340nA, resulting in a power consumption of 2.6µW from a dual 1V power supply.

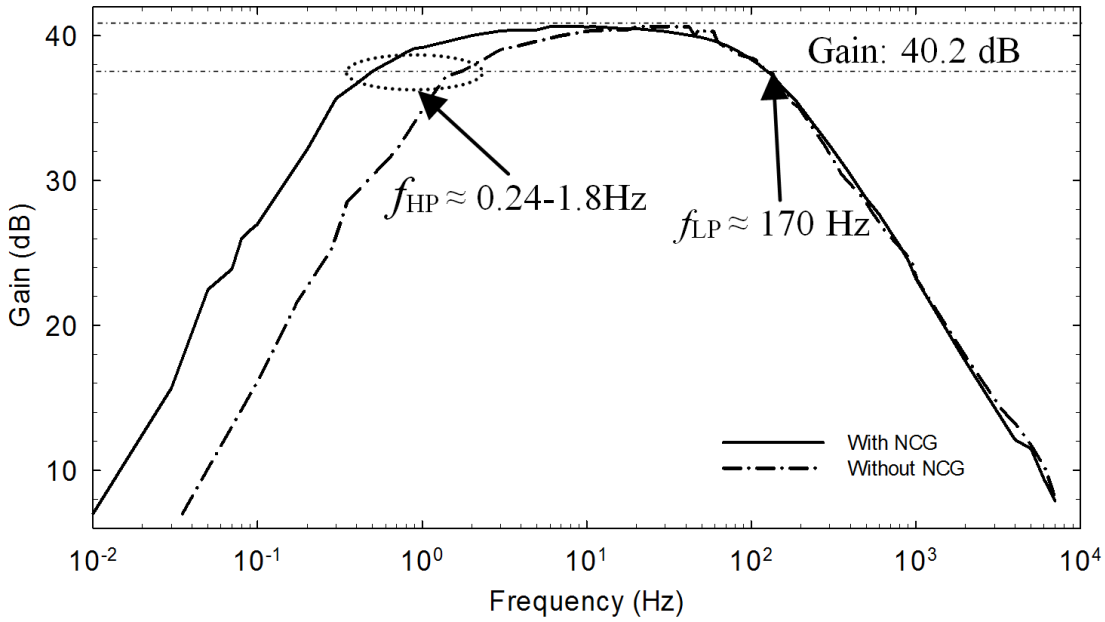

Fig. 57. Frequency response of the biopotential amplifier.

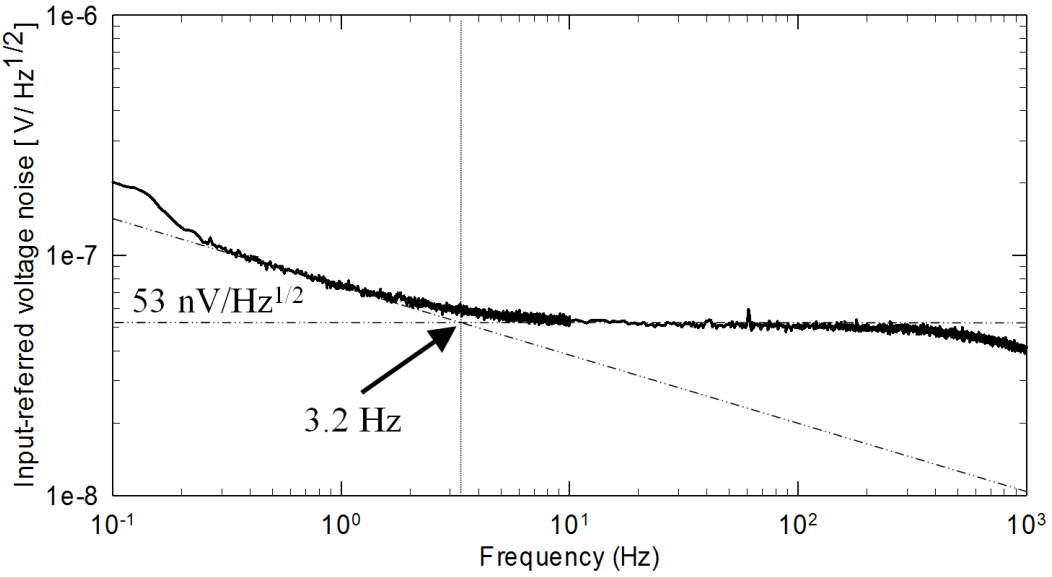

Fig. 58. Measured input-referred voltage noise PSD of the bioamp.

In-vitro Test

Fig. 59 presents the ECG lead I (left arm, right arm) of a 28 year-old male subject taken from an ECG data base and generated using the Agilent 33220A function/arbitrary waveform generator (FAWG). The signal presents an input-referred R wave peak amplitude of 4.3 mV, QRS complex duration of 80 ms with regular P and T waves and a heart rate of approximately 94 bpm. The obtained trace demonstrates that the non-desired components of V_{in} are successfully rejected by the bioamp. In order to test the DEO rejection, the same FAWG is used to provide the ECG signal with variable offset, reaching a rejection of +/- 150mV.

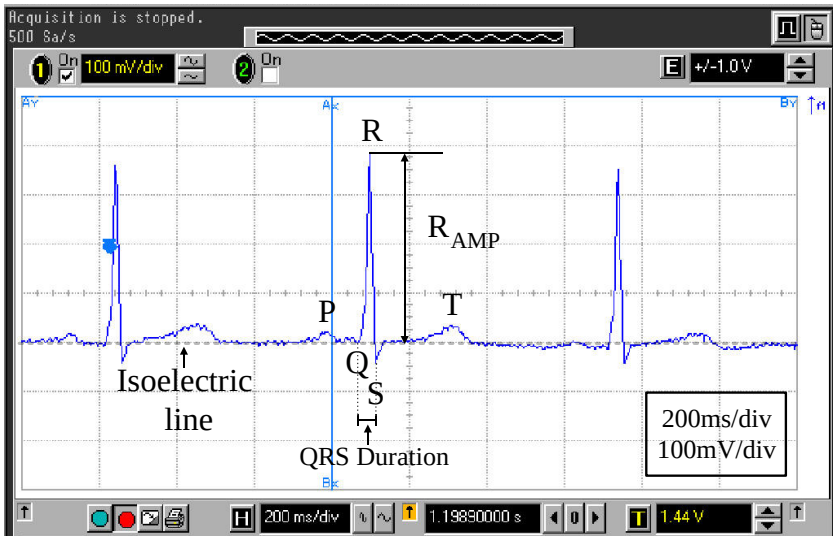

Fig. 59. Transient response of the bioamp showing lead I of a 28 year old male subject (provided with a function generator from a data base).

Discussion

Table VII presents a comparison among the results obtained by the presented bioamp and similar works. The proposed bioamp has a power consumption comparable with other works but achieves a better integrated noise performance (0.68μVrms) between 0.5 Hz and 160 Hz. This is reflected on the calculated noise efficiency factor (NEF) of 2.3, obtained from the low thermal noise resulting from the large input transistors and the reduction of the 1/f noise corner achieved after the inclusion of the chopper modulators. The NCG block does not appear on the thermal or flicker noise calculations, but plays a key role on the bioamp operation allowing the use of the chopper modulators without affecting its AC response.

Table VII. Comparison between the proposed bioamp and other state-of-the art works.

Ref.	**[42]**	**[44]**	**[45]**	**[56]**	**This work**
Gain (dB)	39.8	60	49.54	39.4	40.2
Power (µW)	0.9	3.5	33.3	2.4	2.6
Integrated Input-Ref. Noise (µVrms)	1.6	1.3	1.7	3.07	0.68
Spot noise (nV/√Hz)	21	130	85	60	53
NEF†	4.8	9.4	5	3.09	2.3
CMRR (dB)	>83	>60	>105	>66	>84.3
Bandwidth (Hz)	0.014-30	0.5-100	0.3-170	0.5-1300	0.24-170
External Components	No	Yes	Yes	No	No
Area (mm^2)	0.16	0.30	0.6	0.13	0.36
Design Approach*	PR	CH,PR	CB,CH,DAIC	PR,CS	CH,PR,NC
CMOS process (µm)	1.5	0.18	0.6	0.5	0.5

†Noise efficiency factor. Acronyms used in "*" column. PR: Pseudoresistors; CH: Chopping; CB: Current Balancing; DAIC: Digitally Assisted Interference Cancellation; CS: Current splitting; NC: Negative Capacitance.

Summary

In this chapter, a fully integrated ultra-low-power/low-noise biopotential amplifier has been presented. Measurement results show a pass-band gain of 40.2 dB with a minimum CMRR of 84.3 dB and an input referred noise of 0.68 μVrms, resulting in a NEF of 2.3. Although this work was intended for ECG applications, the proposed architecture allows the integration of the bioamp in EEG/EMG systems with minimum modifications in its feedback network.

CHAPTER V

A VERSATILE AND HIGHLY LINEAR BASEBAND SECTION FOR EXTRAVEHICULAR ACTIVITY (EVA) RADIO RECEIVERS *

Introduction

Extravehicular Activity (EVA) allows astronauts to conduct experiments in the space shuttle's payload bay, to test new equipment in space and to repair satellites in orbit [57]. These tasks demand versatile radio systems with high levels of integration, low power consumption, light weight and small volume. EVA radios typically transmit audio and video information through S-band, a frequency band used by other services such as weather radar and satellite radio. Different transmission protocols and modulation schemes allow simultaneous use of this band at the price of increasing the information traffic with undesired spectral content (blockers).

The presence of blockers, in-band (IBB) or out-of-band (OOBB), degrades the performance of a radio receiver in two different ways: 1) decreasing the sensitivity of the receiver by the intermodulation (IM) products that appear in-band at the base-band output, 2) increasing the in-band noise figure (NF) by degrading the LNA performance and the noise folding effect in the mixer. Therefore, the impact of RF blockers should be taken into account when defining the receiver's frequency planning and while determining the specifications of its individual blocks.

---

*©[2013] IEEE. Reprinted, with permission, from "A CMOS inverse Chebyshev channel selection filter for extravehicular activity (EVA) radio receivers," by J. E. Gaxiola-Sosa, H. Hedayati, L. Pengcheng, and K. Entesari, *2013 IEEE 56th International Midwest Symposium on* in *Circuits and Systems (MWSCAS),*2013, pp. 217-220.

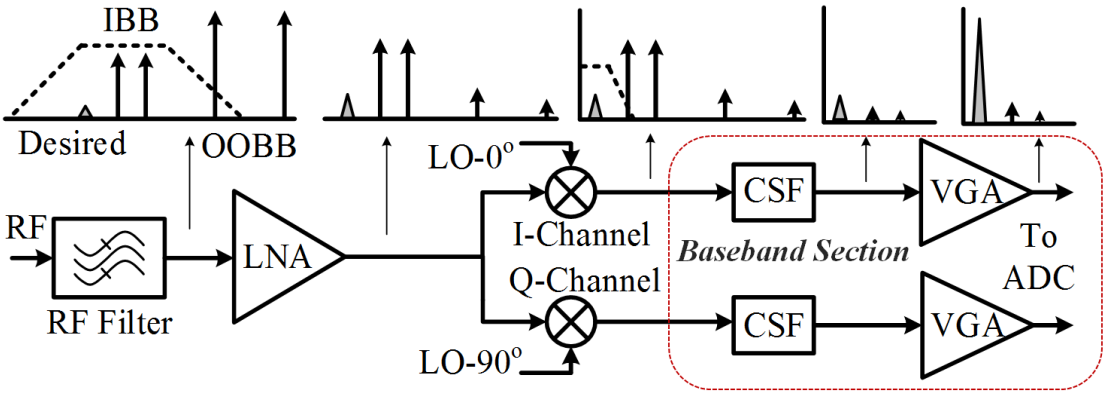

Fig. 60. Block diagram of a direct conversion receiver for EVA radio.

The block diagram of a direct conversion receiver [58] for EVA radio and the frequency spectrum of the desired signal including blockers are presented in Fig. 60. OOBBs are rejected by an RF filter. Furthermore, proper design of the RF section (LNA and mixer) can provide additional poles for out-of-band filtering. After down-conversion, the desired signal is still located within a crowded spectrum that includes in-band blockers at the adjacent channels. The baseband section composed of the channel selection filter (CSF) and variable gain amplifier (VGA) must provide enough rejection to these blockers, guarantee good out-of-channel linearity and amplify the desired signal filtering out any DC component that may saturate the subsequent ADC. With proper adjacent channel rejection, the presence of IM components at the input of VGA is minimized and the overall linearity of the receiver is significantly improved. On the other hand, the need for in-phase and quadrature (I&Q) channels in the baseband section requires good matching between these paths and thus high tolerance to process-voltage-temperature (PVT) variations. Therefore, a filter with high rejection, tuning capabilities

and high linearity is required. Similarly, a VGA with wide output dynamic range, band-pass filter response and accurately defined gain steps is needed.

This chapter presents a 4^{th} order inverse-Chebyshev filter implemented with a leapfrog active-RC network to emulate an LC ladder and a 2-stage VGA with wide dynamic range and DC cancelling. These circuits compose the baseband section of a direct conversion receiver for EVA radio applications. The use of an operational amplifier-based active network in the CSF addresses the linearity issue and the inclusion of a digitally-controlled tuning scheme allows the modification of the frequency response of the I&Q channels while keeping a high rejection and a modest phase response. The VGA includes fully-differential transconductance and transimpedance stages to provide linear variable gain and constant output swing respectively. At the same time, it incorporates a DC cancelling loop to provide rejection to DC and 1/f noise.

This chapter is organized as following: section B presents the system-level analysis of the EVA radio receiver along with relevant equations for the specifications of the CSF and VGA circuits, sections C and D explain the implementation of the CSF and VGA, section E presents the results obtained from the fabricated circuits and section F summarizes this work.

Derivation of CSF/VGA Specifications from EVA Radio Receiver Requirements

The EVA radio receiver requires data rates of 8 Mbps and 100 Kbps for video and voice applications. Based on these data rates, 64QAM and QPSK modulation schemes have been chosen. A 30% imperfection from these modulation techniques results in spectral efficiencies of 4 bps/Hz and 1 bps/Hz [59] which turn into effective bandwidths of 2 MHz and 100 KHz for video and voice transmission respectively. The expected bit error rate (BER) for both modes is 10^{-5} which results in minimum SNR values of 26 dB and 13 dB [59]. The targeted operating ranges for video and voice applications are 1-100 m and 0.001-1 Km. Considering the maximum channel loss and 26 dBm as the transmitter's maximum output power, the sensitivity $P_{in,min}$ of the receiver is found to be in -75 dBm and -96 dBm for video and voice respectively. The noise figure of the receiver for both modes of operation, video and voice, are found to be 10 dB and 12 dB using (5.1).

$$\mathrm{P_{in,min}} = -174\ \mathrm{dBm/Hz} + \mathrm{NF} + 10log(\mathrm{BW}) + \mathrm{SNR_{min}} \tag{5.1}$$

The minimum linearity requirements of the receiver are defined by the maximum input power level P_{sig} in a two-tone test in which the 3rd order IM product P_{int} is within a 6-10 dB margin below the noise floor of the receiver. Therefore, the IIP3 of the entire receiver can be calculated using (5.2) resulting in a minimum value of 15 dBm for both, video and voice modes.

$$\mathrm{IIP3} > \frac{\mathrm{P_{int}} - \mathrm{P_{sig}} + \mathrm{SNR_{min}} + \mathrm{Margin}}{2} \tag{5.2}$$

To achieve the best linearity, a direct-conversion approach has been selected. To overcome the offset and 1/f noise issues inherent with the zero-IF receiver architecture, a DC-free coding approach has been employed [58].

Fig. 61 shows the receiver's frequency planning where the channel bandwidth is 3MHz for video mode. Each channel includes the 2 MHz bandwidth needed for the video data plus 1 MHz to implement the DC-free coding approach mentioned before. Therefore, the lower side of the channel (DC to 500 KHz) does not carry any information. The channel separation is 6 MHz which means that the adjacent channel rejection should be effective at this frequency. The filter cut-off frequencies for video and audio modes are selected to be 2 MHz and 1MHz with a pass-band gain of 0 dB to make sure that the amplitude does not fall more than 3 dB.

Assuming a worst-case scenario where the blocker power is 50 dBm larger than the desired signal [60], the minimum adjacent channel rejection can be defined. The LNA and mixer gain are chosen to be 20 dB and 10 dB with NFs of 4 dB and 15 dB respectively. To satisfy the receiver dynamic range requirements, the maximum VGA gain needs to be 60 dB with IIP3 of 27 dBm. The VGA can achieve such a high IIP3 as a result of the adjacent channel rejection from the CSF. The NF and IIP3 requirements of

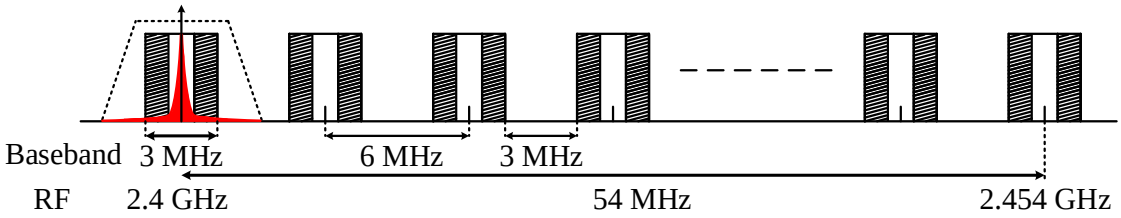

Fig. 61. Frequency planning of the EVA radio.

the CSF and VGA are calculated using the equations presented in [59]. They are found to be 33 dB and 15 dBm, respectively. A summary of the specifications for the EVA radio receiver and the CSF is shown in Table VIII.

Table VIII. Summary of EVA tadio Receiver, CSF and VGA specifications.

Receiver Parameters	**Video**	**Voice**
Data rate	8 Mbps	100 Kbps
Modulation scheme	64 QAM	QPSK
BER	10^{-5}	10^{-5}
Minimum SNR	26 dB	13 dB
Bandwidth	2 MHz	100 KHz
Noise Figure	10 dB	12 dB
Sensitivity	-72 dBm	-96 dBm
Minimum IIP3	-10 dBm	-10 dBm
CSF Parameters	**Video**	**Voice**
Filter cut-off frequency	2 MHz	1 MHz
Adjacent channel rejection	>50 dB	>50 dB
Noise Figure	<33 dB	<33 dB
Minimum IIP3	15 dBm	15 dBm
Pass-band gain	0 dB	0 dB
Maximum ripple in pass-band	Minimum	Minimum
VGA Parameters	**Video**	**Voice**
Noise Figure	<35 dB	<35 dB
Minimum IIP3	10 dBm	10 dBm
Pass-band gain	0 – 30 dB	0 - 60 dB

Chanel Selection Filter

Design Approach

A 4th order inverse Chebyshev approximation is selected to implement the CSF since it provides a smooth pass-band response along with a sharp transition band while keeping a flat group delay [52]. A common way to implement high order filters includes the use of biquads in cascade or the use LC ladder filters. While the use of biquads allows the designer to split the rejection and gain if necessary in different second order stages, it comes at the expense of area and power, and relatively high sensitivity to process variations. On the other hand, LC ladder filters are very stable with process variations and the sensitivity of their shape to these parameters is very small [61]. They can include source resistance as shown in Fig. 62. This approach is common in passive filters at high frequencies, because the matching condition is preserved in both directions. The main disadvantage of this type of filters is the large ratios between the normalized inductors and capacitors of the filter. Typically, the inductors are emulated using capacitors along with impedance inverters or gyrators. Four transconductors and a capacitor are required to emulate a floating inductor. Thus, implementing direct LC ladder filter with gyrators is power hungry, expensive and noisy.

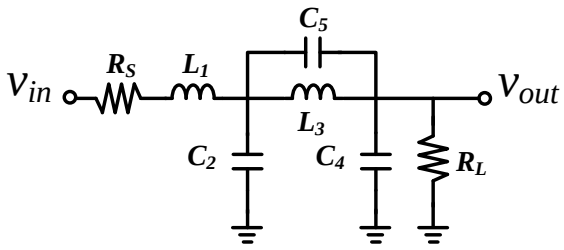

Fig. 62. Doubly terminated LC ladder structure.

Another way to emulate a ladder filter is using a leap-frog architecture [62]. For this architecture, the number of capacitors is the same as the order of the filter, resulting in a power efficient solution for the implementation of high order filters.

The leapfrog signal flow graph (SFG) representation of the LC-ladder from Fig. 62 is shown in Fig. 63 [63] and the transfer functions of each block (t_{Y1}, t_{Z2}, t_{Y3} and t_{Z4}) are defined in (5.3). It includes four poles and one finite transmission zero. The passive realization and the related coefficients of the transfer function are taken from [64]. In order to obtain the desired response using resistors and capacitors, frequency and impedance scaling are performed.

$$t_{Y1} = \frac{1}{sL_1+R_S} \qquad t_{Z2} = -\frac{1}{sC_2} \qquad t_{Y3} = \frac{s^2L_3C_3+1}{sL_3} \quad t_{Z4} = -\frac{1}{sC_4+G_L} \tag{5.3}$$

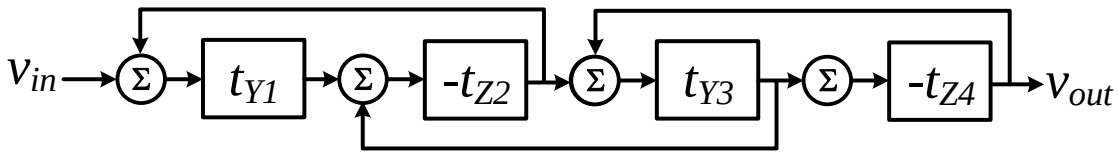

Fig. 63. Leapfrog signal flow graph of the LC prototype from Fig. 62.

Active Implementation of the CSF

The LC ladder presented in Fig. 62 can be implemented emulating the transfer functions in (5.3) and the connections in signal flow graph using active-RC [52, 65], Gm-C [66, 67] or switched-capacitor topologies. Although gm-C implementations consume low power, they suffer from poor linearity. Switched capacitors provide high accuracy and integration but require external circuitry for clocking and dealing with the aliasing issue.

Finally, the use of active-RC elements provides very good linearity and low noise. However, they present higher PVT sensitivity in comparison to SC and consume higher power than gm-C circuits. Using the leapfrog architecture compensates for the sensitivity issue while having a fully differential op amp reduces the power consumption since the filter does not require extra inverters for the implementation of the block transfer functions shown in Fig. 63.

The schematic of the active implementation of the CSF is shown in Fig. 64. This circuit is synthesized from the SFG presented in the previous section and uses four operational amplifiers along with resistors and capacitors in order to implement the desired filter response. Since the inverse Chebyshev coefficients were scaled in frequency to compute the value of the capacitors, changing these capacitors results in frequency tuning. Each capacitor in Fig. 64 consists of a fixed capacitor and a binary weighted capacitor bank (with a 4-bit resolution) connected in parallel for PVT compensation. The value of the fixed capacitor (C_{nF}) provides the highest cutoff frequency. The value of the unit capacitor (C_{nU}) in the capacitor bank is equal to difference between the capacitor value for the lowest cutoff frequency (C_{nT}) and C_{nF} divided by 16. The concept of the capacitor bank implementation is illustrated in Fig. 65. The filter coefficients and the values of C_{nF} , C_{nU} and C_{nT} (from n=1 to n=5) used to implement the different cutoff frequencies are shown in

Table **IX**. The capacitor and resistor values used for impedance and frequency scaling are 6.5 pF and 12 kΩ, respectively.

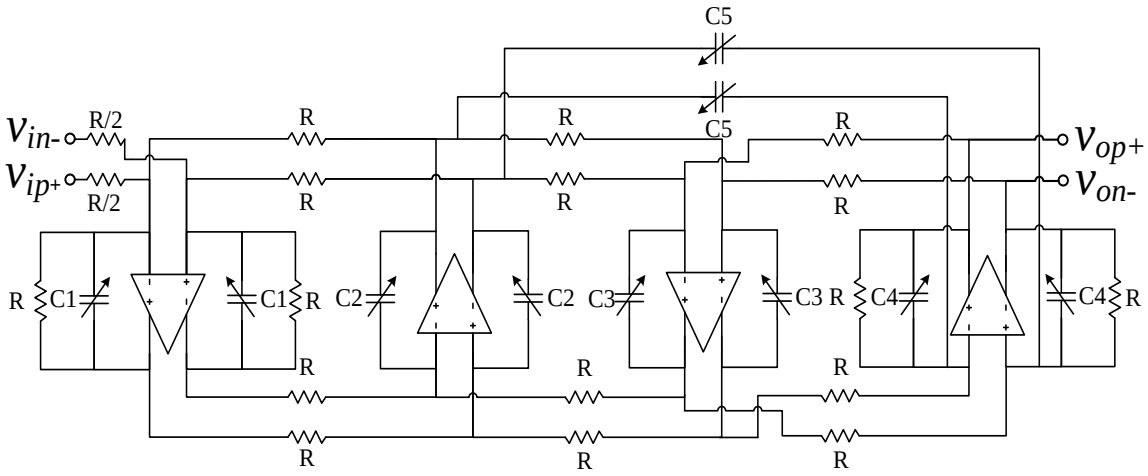

Fig. 64. Active-RC implementation of the signal flow graph from Fig. 63.

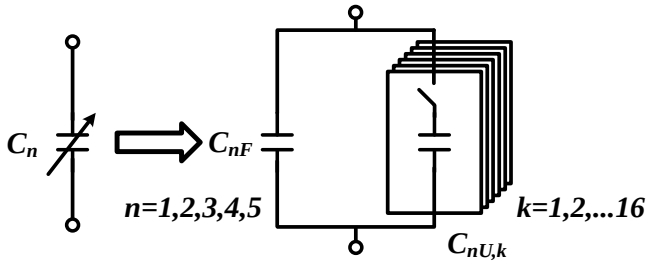

Fig. 65. Schematic diagram of the variable capacitors used for frequency tuning.

Table IX. Filter coefficients and capacitor values after frequency/impedance scaling.

Filter Coefficient	**Capacitor**	C_{nF}	C_{nU}	C_{nT}
0.64094	C1 (pF)	4.165	0.277	8.33
1.51207	C2 (pF)	9.83	0.655	19.66
1.4611	C3 (pF)	9.5	0.633	19
0.58997	C4 (pF)	3.83	0.255	7.66
0.05275	C5(pF)	0.342	0.023	0.684

Operational Amplifier Design and Considerations

The active element showed in Fig. 64 is a two-stage operational amplifier [68] compensated by a miller capacitance (C_m) and its schematic is presented in Fig. 66. The GBW is defined based on the maximum filter bandwidth (2 MHz) and the minimum open loop gain desired at this frequency (40 dB), resulting in a minimum GBW of 200 MHz. The common mode feedback (CMFB) loop is designed to have wider bandwidth than the cutoff frequency of the filter to avoid the effect of the positive feedback of the common mode signal on the main filter loop. Finally, the second stage is designed to have low output impedance in order to drive the resistive loads presented in Fig. 64.

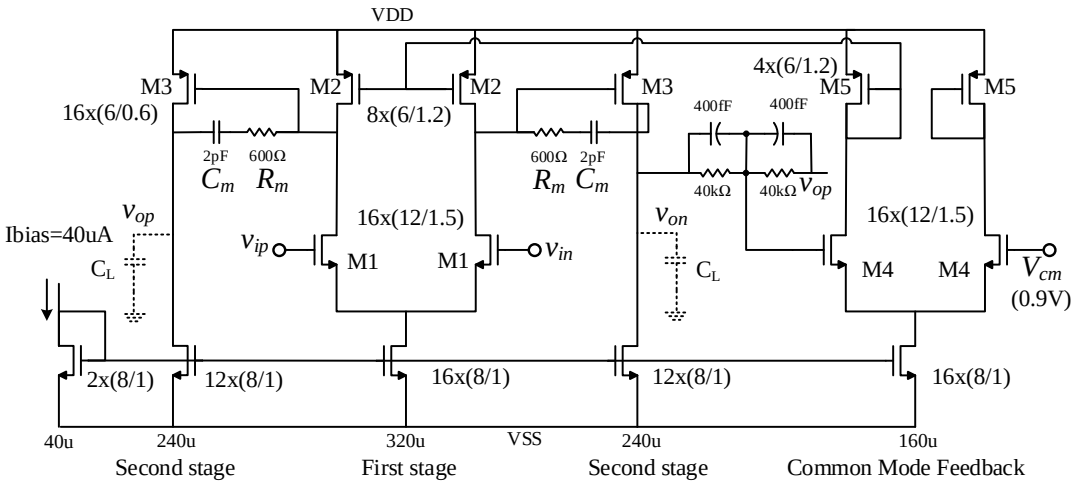

Fig. 66. Schematic diagram of the two-stage miller-compensated operational amplifier used for the active-RC implementation of the CSF.

Fabricated Circuit

The 4th order leapfrog inverse Chebyshev CSF has been implemented in the standard IBM 0.18 µm CMOS process with 6 metal levels. The circuit layout is showed in Fig. 67 and occupies an area of 0.45 x 1.1 mm^2. The passive components were implemented using metal-insulator-metal (MIM) capacitors and polysilicon resistors. The different elements of the system were placed in such a way that good matching can be obtained. In the case of the capacitor banks, the unit capacitors were implemented using four capacitors in series, sacrificing area to "average" possible mismatch errors. Special care was taken for the implementation of the switches on the capacitor bank. Multiple fingers were used to provide a transistor with low on-resistance to avoid contributing parasitic capacitances that may modify the desired cutoff frequency. In the filter layout implementation, standard practices such as common centroid and interdigitation were followed to guarantee the best matching and strength versus PVT variations.

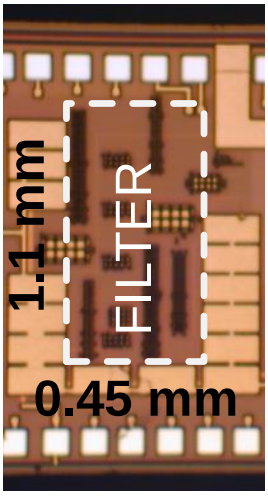

Fig. 67. Microphotograph of the fabricated CSF.

Variable Gain Amplifier

The variable gain amplifier (VGA) is a block able to amplify its input signal by a programmable gain K over a certain bandwidth. In the wireless communication industry, VGAs are commonly used to provide amplification of either intermediate frequency (IF) or radio frequency (RF) signals [69]; they are also frequently used in modern radio receivers to amplify or attenuate incoming signals to properly drive an associated analog-to-digital converter (A/D). For the designed receiver, the total gain should vary between 36 dB and 96 dB while operating in audio mode and between 15 dB and 75 dB while operating in video mode resulting in an effective VGA gain variation of 60 dB. Since the VGA is the last block on the receiver chain, the linearity of the system depends mainly on the VGA while the overall noise figure of the receiver is not very affected by the VGA.

Design Approach

Variations in the gain of an amplifier obtained by either varying the transconductance of a MOS device operated in the saturation region or by varying the load resistance. This is illustrated in Fig. 68. A variation on G_m can be obtaining by modifying the bias current of the MOS device [69]. Since the G_m varies as a function of square root of the bias

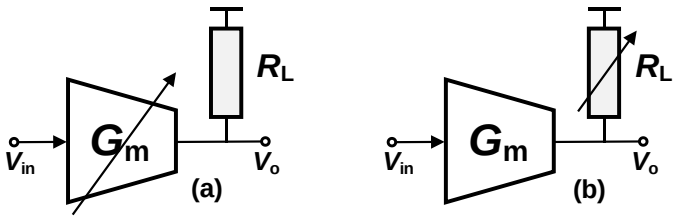

Fig. 68. Basic concept of variable gain based on a) transconductance and b) load variations.

current, this current has to be varied as a square function of the gain variability desired. This entails a lot of power dissipation to obtain gain variation. Another way to obtain G_m variation is by changing the amount of feedback, i.e., by changing the amount of source degeneration [70, 71]; however, in order to reduce the dependence of the total transconductance on the actual G_m of the device and to obtain a linear gain variation, a large G_m is required (such that it can be degenerated). This is translated into high power consumption. Trans-impedance gain variation on the other hand, does not have the drawback of high power consumption at first glance. Assuming a MOS transistor operating in the linear region, only a variation in the gate voltage is sufficient to modulate the channel resistance. Thus, no change in the bias current is necessary to vary the gain, resulting in an attractive way to obtain variation in the gain.

The block diagram of the proposed VGA cell architecture is shown in Fig. 69. It incorporates a VGA cell and a DC offset canceller implemented by a low pass filter

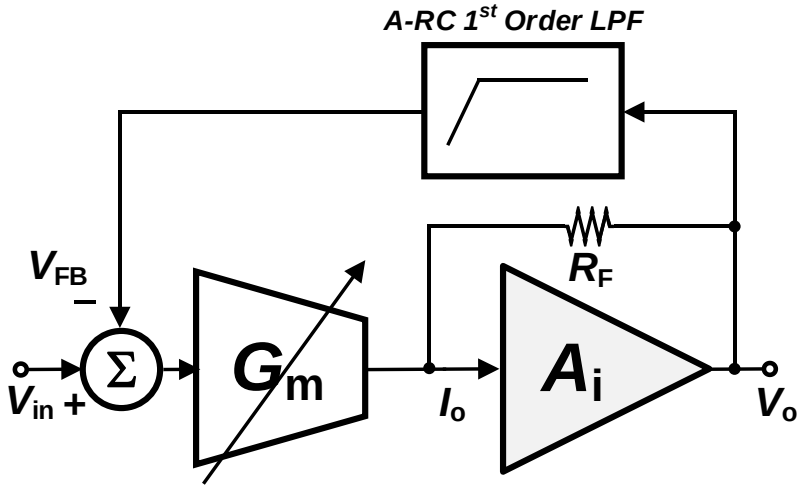

Fig. 69. Block diagram of the proposed VGA.

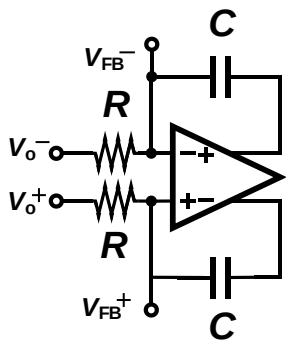

Fig. 70. Low-pass filter implementation using an operational amplifier to multiply the value of the feedback capacitor.

placed in feedback which translates into a high pass filter for the VGA frequency response. The VGA single cell split into two stages. The first is a variable transconductance amplifier with low output swing capability while the second stage is a transimpedance amplifier that provides constant gain and high swing. The circuit operation is described with (5.4).

$$\frac{V_o}{V_{in}} \approx -G_m R_F \tag{5.4}$$

The low pass filter from placed in feedback in Fig. 69 is implemented as shown in Fig. 70. Since the filter is to be used in a feedback loop to effectively provide a high pass behavior for DC cancelling extremely large values of R and C are required to provide a low cutoff frequency. In order to obtain a large time constant while keeping the values suitable for an integrated implementation the feedback signal V_{FB} is taken at the input of the amplifier. By doing this, the value of the capacitance seen by the resistor is equal to the open loop gain of the amplifier times the feedback capacitor based on the

miller effect. After the addition of the feedback network the frequency dependent transfer function is given by (5.5).

$$\frac{V_o}{V_{in}} \approx -G_m R_F(sRC + 1) \tag{5.5}$$

In order to achieve the desired dynamic range, two VGA cells (including the VGA cell and DC canceller) are placed in cascaded and are enabled depending on the gain required by the receiver. For gains between 0 and 30 only one cell is used, for gains between 30 and 60, both cells are used. This is illustrated in Fig. 71.

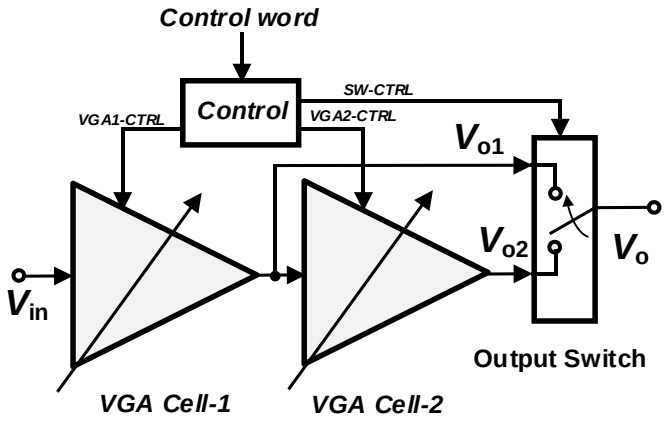

Fig. 71. Block diagram of the complete VGA including two VGA cells and a control block for gain variation.

Transistor-level Implementation

The transistor level implementation of the VGA single cell is presented in Fig. 72. The circuit is designed such that the transconductance is given by 1/ R_S making G_m more independent of the non-linear characteristics of M_{1A}. This achieved by transistor M_{1B} that boosts the impedance seen at the source of M_{1A} as shown in (5.6).

$$G_m = \frac{I_o}{V_{in}} = \frac{1}{\frac{g_{o1A}}{g_{m1A}g_{m1B}} + R_S} \approx \frac{1}{R_S} \tag{5.6}$$

Another way to understand the circuit is by observing that transistors M_{1B} act like current sources and their gate connection provides negative feedback, maintaining the current through M_{1A} constant. Thus the transconductance doesn't depend on M_{1A} anymore. Transistors M_2 provide the bias current for the input stage.

The transimpedance amplifier is implemented by $M_{4B,}$ M_{4A} and R_F where the transimpedance gain is given by

$$R_m = \frac{V_o}{I_o} = \frac{g_F - Kg_{m1B}}{g_F g_{m1B}} \frac{1}{(1+K)} \approx -\frac{1}{g_F} = -R_F \tag{5.7}$$

Transistors M_3 provide the bias current to the output stage while the M_{FB} differential pair is used to add the current from the DC cancelling circuit.

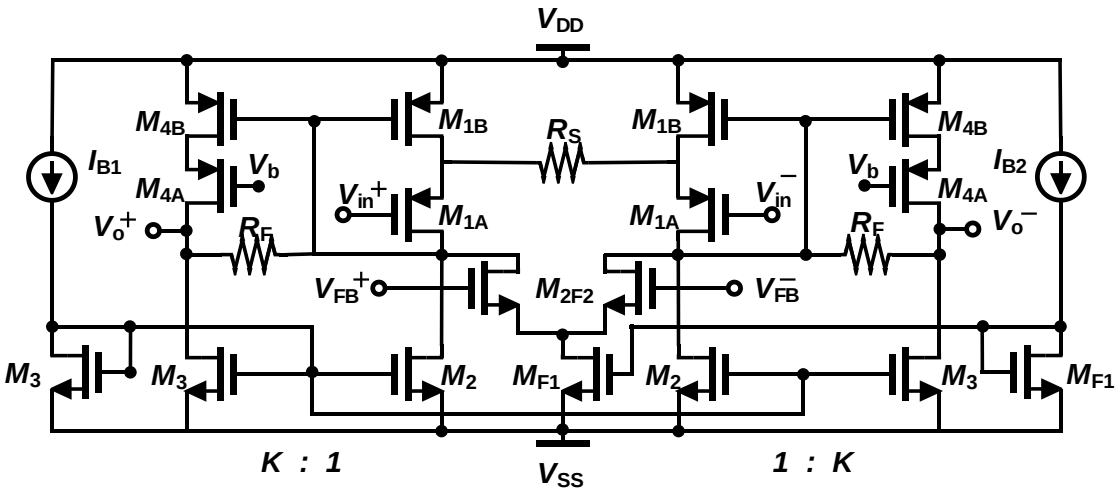

Fig. 72. Transistor-level implementation of the VGA cell.

The sizing ratios of the transistors used on the VGA are presented in **Table X** with bias currents of 60µA and 50µA for I_{B1} and I_{B2} respectively. Finally, the amplifier used in the low-pass filter is similar to the on presented in the previous subsection.

Table X. Transistor sizing ratios.

Transistor	**W/L (µm)**
M1A	300/0.8
M1B	4.2/0.4
M2	3.2/3
MF1	220/2
MF2	220/2
M3	8/3
M4A	130/0.4
M4B	8.2/0.8

Experimental Results

Fabricated Chips

The baseband section of the receiver, including the channel selection filter and the variable gain amplifier (VGA) with ESD protection has been implemented in the standard IBM 0.18 μm CMOS process with 6 metal levels. Fig. 73 shows a micrograph of the chip with a total area of 2.52 mm^2. Different versions of the chip were fabricated including a CSF-only chip, a first version of the CSF-VGA and the one presented on the following figure. All measurements are referred to the last version of the chip.

PCB and Test-bench

In order to characterize the behavior of the channel selection filter and the variable gain amplifier contained in the baseband section, the test PCB presented in Fig. 74 has been fabricated. The PCB includes 3 low drop-out regulators to implement the baseband IC power supply (1.8V), and the supplies (5V, -5V) for the single-ended to differential

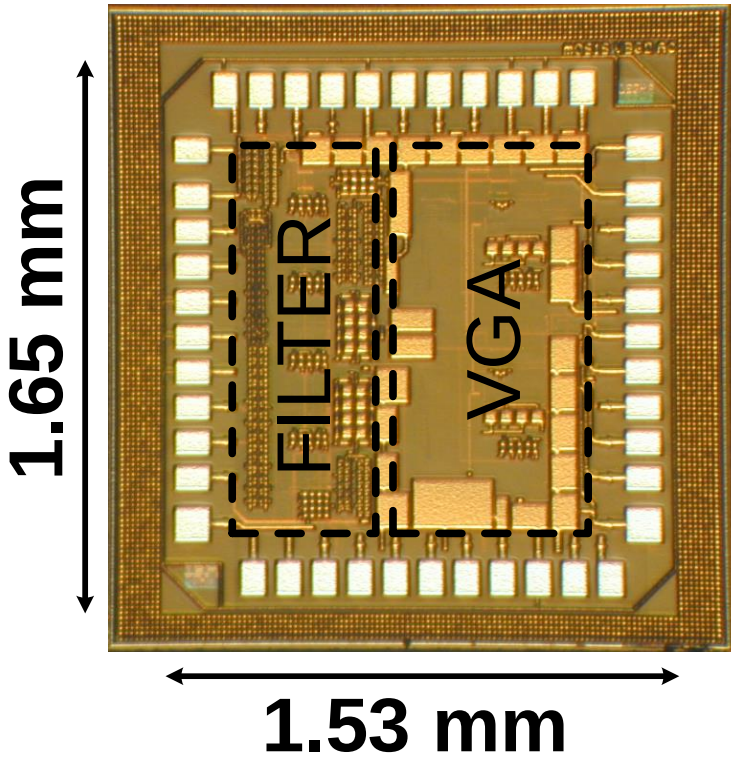

Fig. 73. Micrograph of the fabricated baseband chip.

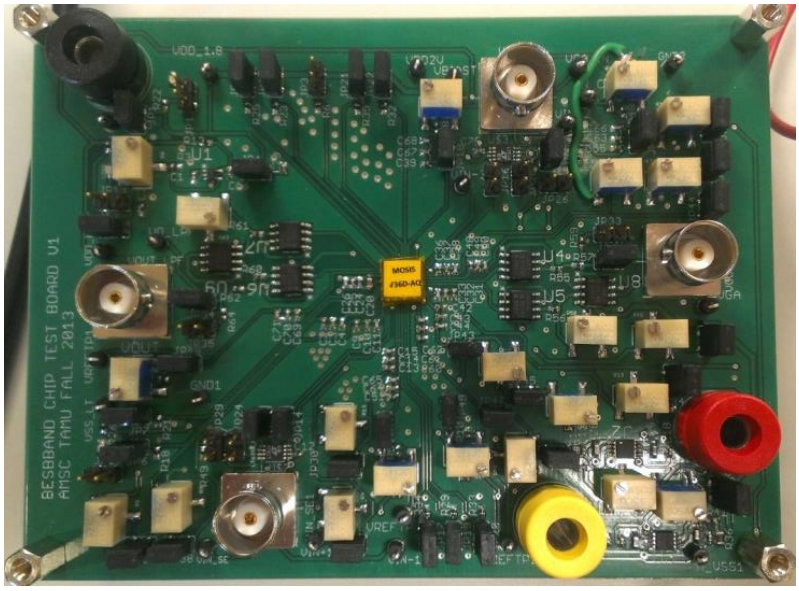

Fig. 74. PCB used to characterize the baseband chip.

resistors can beset to obtain the desired feedback ratio on the LDOs, bias voltage for the and differential to single-ended circuits to be used at the input and output of the circuit, for testing purposes. In order to avoid damaging the chip, jumpers were placed at the output of each LDO and current/voltage bias generator circuits. On this way, variable voltage bias generators, and the estimated resistance that would provide the bias currents for the different blocks of the baseband chip. Finally, a set of pull-down resistors along with jumpers are used as the control bits for the filter frequency and VGA gain variation respectively.

The measurement setup for the single channel baseband chip is shown in Fig. 75. The setup allows the option to test the filter and VGA block working together or as independent blocks. The single ended input can be converted to differential to feed the filter or VGA. A set of on-board jumpers is used to define the control word for the

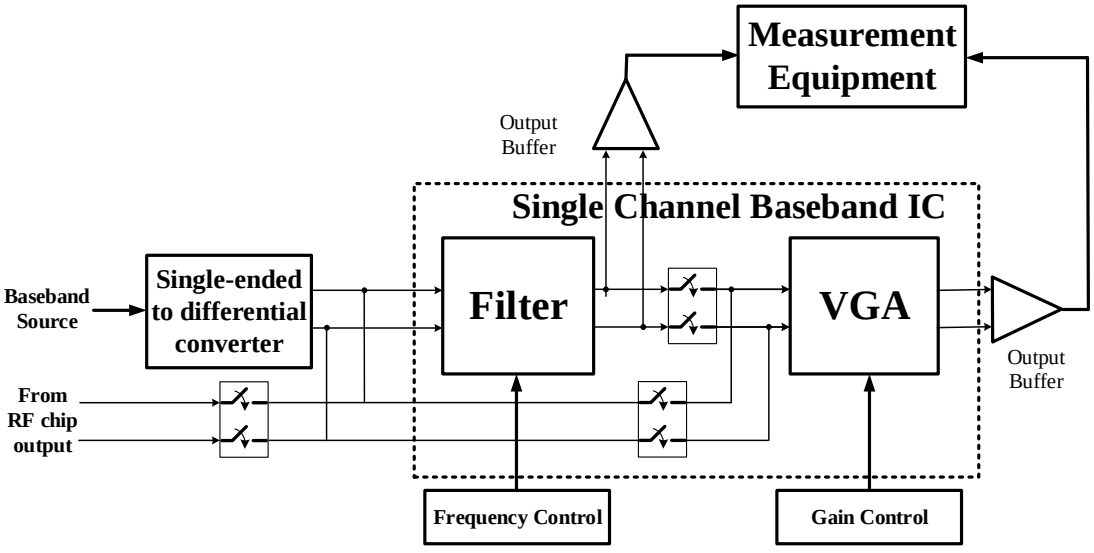

Fig. 75. Baseband chip characterization setup.

frequency of the filter and the gain of the VGA. Finally, commercial highly-linear buffers are added to the differential outputs for single ended conversion and to drive the signal to the measurement equipment.

The next picture shows the test bench built to characterize the baseband chip. The instruments used are: the HP 89410A Vector Signal Analyzer (top left on Fig. 76), Agilent Infinitum Oscilloscope, Agilent 33220A function arbitrary waveform generator (FAWG), and two multi-meters from HP and Fluke.

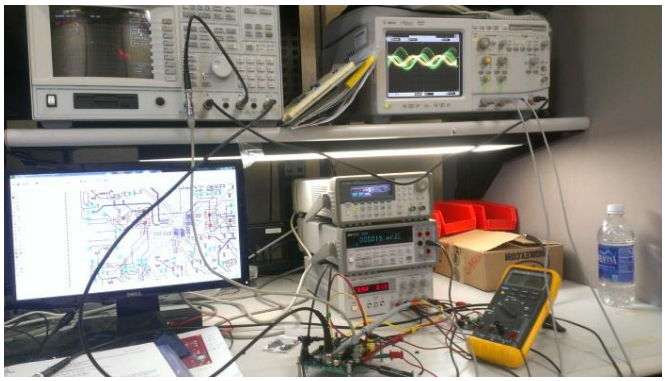

Fig. 76. Test bench used for the characterization of the baseband chip.

The testing procedure was the following:

1. Power supply voltage verification. With all jumpers open, the trimmers on the feedback network of the LDOs were tuned in order to achieve the required output voltages.

2. Bias voltages setup. Resistor dividers were used as bias voltage generators. A fixed resistor and a trimmer composed the divider from 0.1 V to 1.8 V. The trimmers were tuned to achieve the desired values.

3. Bias currents setup. Trimmers connected to VDD or GND were used as source currents for the chip. Since the exact current can't be measured in open circuit, the resistance of the trimmers was tuned to the value used in simulations.

4. DC testing with chip powered. After the supply voltages and bias parameters were set, the circuit was connected and the different voltages and currents were measured in order to verify that the DC operating points were properly set.

5. Transient characterization. The FAWG output was set to a 500 KHz signal with 50mVpp amplitude and an offset of 900mV. This signal was fed to a single-ended to differential generator IC, LT6350, that uses a voltage follower and a unity gain inverter amplifier to generate the differential signals. In order to set the offset of the positive input, a DC offset similar to the one provided by the FAWG was fed to the non-inverting input of the inverter amplifier.

6. AC characterization. The AC responses of the CSF and VGA were obtained using the HP 89410A Vector Signal Analyzer. A diagram of the connections is shown in Fig. 77 , where the device under testing (DUT) is the CSF. The instrument was set to provide an input signal of 100mVpp with an offset of 900mV (with 50 Ohms output impedance). The two channels are used to measure the input and output, and to compare both in order to obtain the frequency response.

7. Noise and linearity. These measurements are explained in detail in the following section.

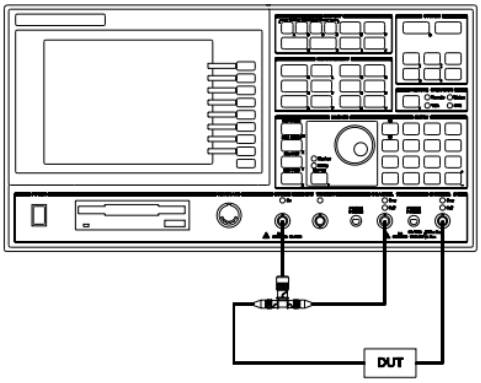

Fig. 77. AC response measurement configuration with the HP89410A vector signal analyzer.

CSF Measurements

DC Operation

The baseband section of the receiver, including the channel selection filter and the variable gain B power supply is generated from the Agilent E3602A, providing the following voltages: +6V, -6V and 0.9V. The filter power supply is generated by the TPS71701, a low noise, high-bandwidth power supply rejection ratio, low-dropout linear regulator. This IC delivers a clean 1.8V supply from the +6V input. A summary of the CSF DC parameters is presented in Table XI.

Table XI. DC bias voltages and current measurements, simulated vs measured results.

Parameter	Simulation	Measurement	Parameter	Simulation	Measurement
VCM	*900mV*	**899.13mV**	**INPUT_DC-**	*900mV*	**903mV**
IB1	*40.1mA*	**39.98uA**	**OUTPUT_DC+**	*900mV*	**905mV**
IB3	*40.05mA*	**39.9uA**	**OUTPUT_DC-**	*900mV*	**904mV**
IB2	*39.98mA*	**40.03uA**	**Current**	*4.03mA*	**4.13mA**
IB4	*40.12mA*	**39.9uA**	**VDD**	*1.8V*	**1.8V**
INPUT_DC+	*900mV*	**902mV**	**Power**	*7.254mW*	**7.434mW**

AC Operation

Fig. 78 shows the frequency responses obtained from the CSF for each control word. The 3dB frequency of the filter as well as the rejection at 6 MHz show good results. The cutoff frequencies varied from 2.29MHz to 1.12MHz with a DC gain of -0.15 dB; and minimum adjacent channel rejection (measured at 6 MHz) of 49.741 dB. The frequency response was measured for each of the different control words (from 0000, to 1111) and the results are summarized in Table XII.

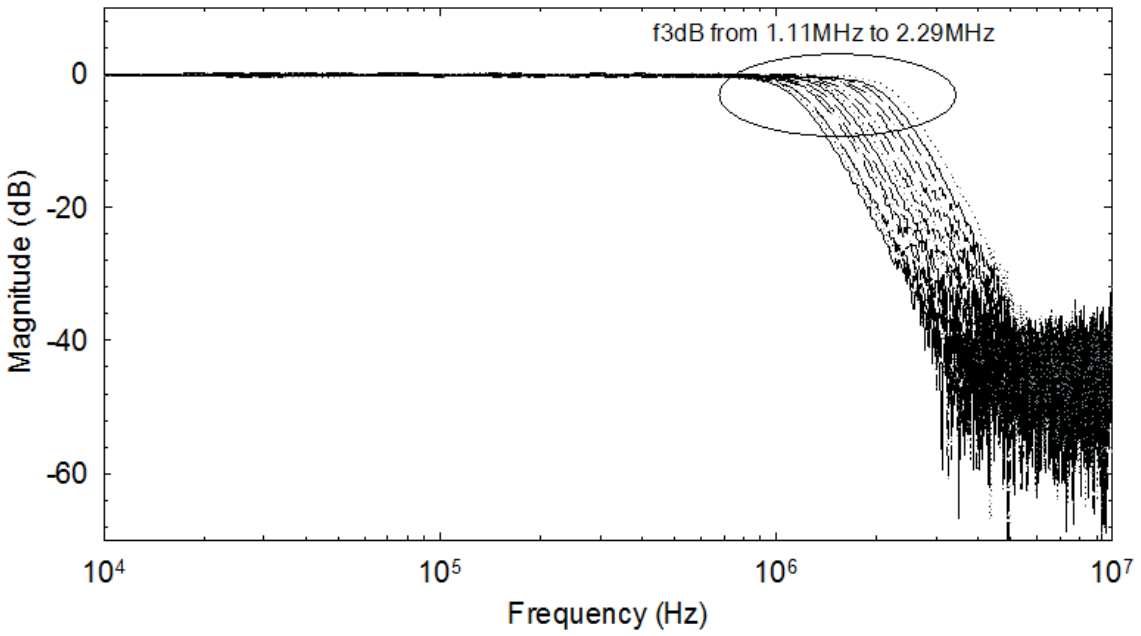

Fig. 78. Frequency response of the CSF for different control words.

Table XII. Simulated and measured cut-off frequencies of the CSF for different control words.

Control word	f_{3dB} **(MHz) simulated**	f_{3dB} **(MHz)**	**Rejection @ *6* MHz**
0000	2.28	2.29	49.741
0001	2.14	2.13	54.717
0010	2.01	1.99	51.586
0011	1.91	1.87	51.714
0100	1.8	1.78	52.64
0101	1.71	1.68	55.071
0110	1.63	1.61	54.166
0111	1.56	1.53	52.197
1000	1.48	1.46	52.808
1001	1.42	1.39	57.051
1010	1.36	1.34	54.22
1011	1.32	1.29	51.43
1100	1.27	1.23	55.597
1101	1.22	1.22	53.99
1110	1.17	1.17	53.73
1111	1.10	1.12	63.379

Linearity

In order to measure the linearity of the system, a two-tone test with blockers of -6 dBm located at the 6 MHz and 11 MHz is performed using the Rohde & Schwarz FSEB spectrum analyzer. The resulting IM3 product (at 1MHz) has a power of –70.45 dBm. The output 6MHz tone has a power of -58.3 dBm, expected from the 50 dB rejection showed by the CSF at this frequency. Since the gain of the CSF is around 0 dB for the IM3 product frequency (1MHz) the input refered IM3 has a power of -70.45 dBm. Therefore, the IIP3 is computed as IIP3=IM3/2-F1, resulting in a 29.225 dBm IIP3. The two tone test measurements are shown in Fig. 79.

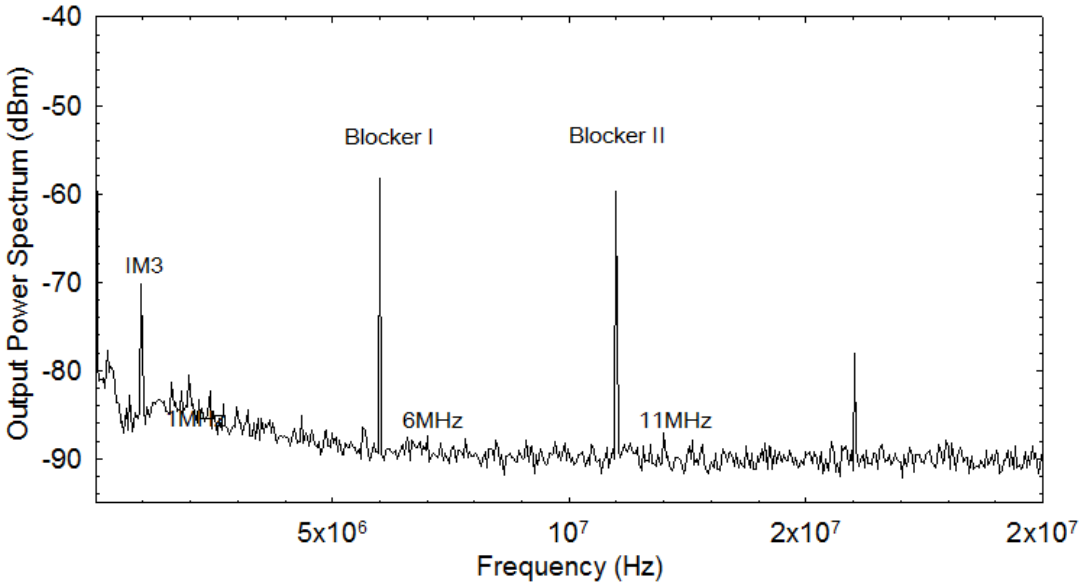

Fig. 79. Output power spectrum of the CSF.

Noise Figure

In order to measure the noise figure, the input is terminated with a 50 Ohm resistor and a bias-T is used to provide the input DC voltage (0.9) for the CSF to operate properly. Since the single ended input is connected to a single ended to differential circuit (LT6350) the main source of noise is dominated by this circuit. Therefore if the observed Noise Figure (NF) of the LT6350 and the CSF is smaller than the desried value (-33 dB), the CSF NF would fulfill the requirements for the entire receiver to operate properly. The measured output spectrum density is -142.64 dBm/Hz (6dB are added due to the input gain of the single ended to differential converter) at 1MHz. Since the noise floor is -174 dBm/Hz and the gain is 0 dBm the resulting noise figure is the difference between figure is the difference between the measured output spectrum density and the noise floor, 25.354 dB.

Summary of Results

Table XIII presents a summary of the different measurements presented in this section.

Table XIII. Summary of results (CSF).

Parameters	Specification	Post-Layout	Measurements
Adjacent channel rejection	>50 dB	>50 dB	>49.74 dB
f_{3dB}	1-2 MHz	1.1-2.28 MHz	1.12-2.29 MHz
IIP3	>15 dBm	38 dBm	29.225 dBm
Pass-band gain	0 dB	-0.07 dB	-0.15 dB
Current consumption	Minimum	4.03 mA	4.133 mA
Noise Figure	<33 dB	30.2 dB	31.35 dB
Power Supply	1.8 V		
Area	0.45x1.1 mm^2		
Technology	0.18 µm IBM CMOS		

VGA Measurements

DC Operation

The PCB power supply is generated from the Agilent E3602A, providing the following voltages: +6V, -6V and 0.9V. The VGA power supply is generated by the TPS71701, a low noise, high-bandwidth power supply rejection ratio, low-dropout linear regulator. This IC delivers a clean 1.8V supply from the +6V input. A summary of the CSF DC parameters is presented in Table XIV.

Table XIV. DC bias voltages and current measurements. simulated vs measured results.

Parameter	Simulation	Measurement	Parameter	Simulation	Measurement
VCMV	*900mV*	**900.13mV**	**VREF**	*900mV*	**902mV**
IBOA2	*40.12uA*	40.05uA	**VBIAST**	*400mV*	**401.17mV**
IB12	*59.92uA*	59.9uA	**IBCM2**	*28.55K*	40.3 uA
IBOA1	*39.98uA*	40.03uA	**IB_2**	*21.27K*	49.9uA
IB11	*59.82uA*	60.2uA	**IBCM1**	*29.25K*	40.4 uA
INPUT_CM	*900mV*	**900mV**	**IB_1**	*21.27K*	49.9uA
INPUT_DC+	*900mV*	**902mV**	**OUTPUT_DC+**	*900mV*	**910mV**
INTPUT_DC-	*900mV*	**901mV**	**OUTPUT_DC-**	*900mV*	**908mV**

AC Operation

The AC response of the VGA was obtained using the HP 89410A Vector Signal Analyzer. The setup is similar to the one presented in Fig. 77. Fig. 80 shows the VGA frequency response for the '11111' control word. The gain setting is 0 dB and extra 6 dB appear in the pass-band due to the gain of the single ended to differential converter at the input. The high pass cutoff frequency is around 90 KHz while the low-pass cutoff is around 6MHz. The gain variation is showed with the VGA operating along with the CSF since those are the measurements important for the actual receiver.

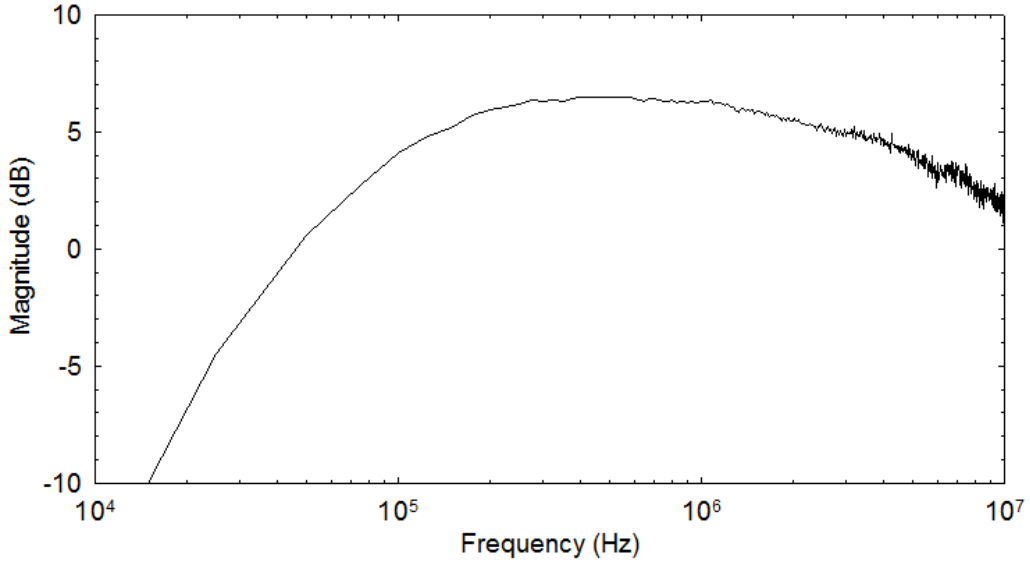

Fig. 80. Frequency response of the VGA for the '1111'control word.

Linearity

In order to measure the linearity of the system, a two-tone test with blockers of -16 dBm located at the 6 MHz (F1) and 11 MHz (F2) is performed using the Rohde & Schwarz FSEB spectrum analyzer. The resulting IM3 product (at 1MHz) has a power of –67.21 dBm. The output 6MHz tone has a power of -19.94 dBm. The inpurt referred IM3 and F1 power values are -73.21 dBm and -16 dBm. The IIP3 is computed as IIP3=IM3/2-F1, resulting in a 12.605 dBm IIP3. The two tone test measurements are shown in Fig. 81.

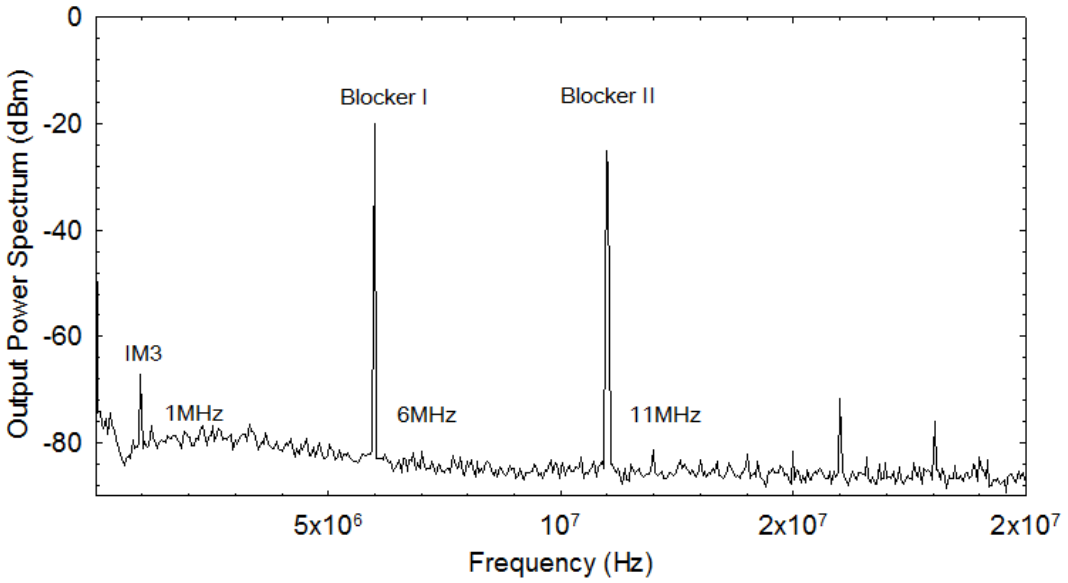

Fig. 81. Output power spectrum of the VGA.

Noise Figure

The NF is measured in a similar way than the explained in the filter calculations, resulting in a value of 38.48 dB.

Summary of Results

Table XV presents a summary of the different measurements presented in this section. As the table shows, the measured results are similar to the expected values.

Table XV. Summary of results (VGA).

Parameters	Specification	Post-Layout	Measurements
Gain	0-60 dB	0-60 dB	-0.13-59.5 dB
IIP3	>10 dBm	14 dBm	12.605 dBm
Current consumption	Minimum	6.22 mA	6.29 mA
Noise Figure	<35 dB	32.2 dB	32.8 dB
Power Supply	1.8 V		
Area	0.7x1.1 mm^2		
Technology	0.18 µm IBM CMOS		

Complete Baseband Section (CSF+VGA) Measurements

DC Operation

The values showed in the previous sections, Table XI and Table XIV present the DC operation points for these two blocks.

AC Operation

The AC response of the CSF+VGA was obtained using the HP 89410A Vector Signal Analyzer. The setup is similar to the one presented on Fig. 75. Fig. 82 shows the VGA frequency response for the '11111', '11011', '11000', and '10100' control words. The remaining gain settings (higher than 30 dB) were not tested with the HP89410 because to the saturation on channel 2 would not lead to accurate frequency response plots. Instead, gains higher than 30 dB were measured with the Spectrum Analyzer.

Fig. **83** shows a plot of the measured gain values vs the gain control word for the circuit.

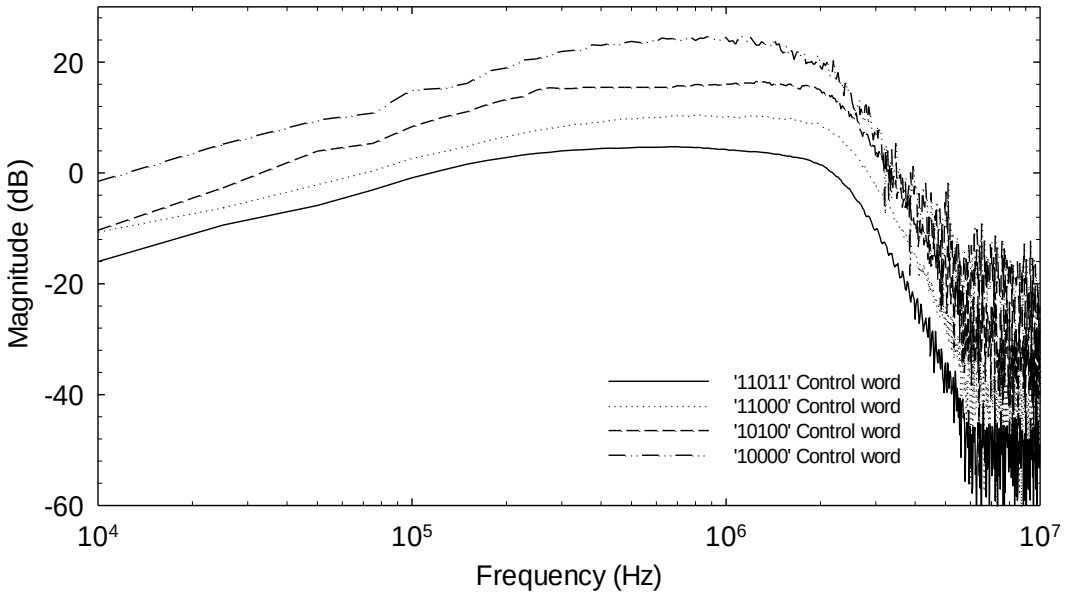

Fig. 82. Frequency response of the baseband section (CSF+VGA) for different control words.

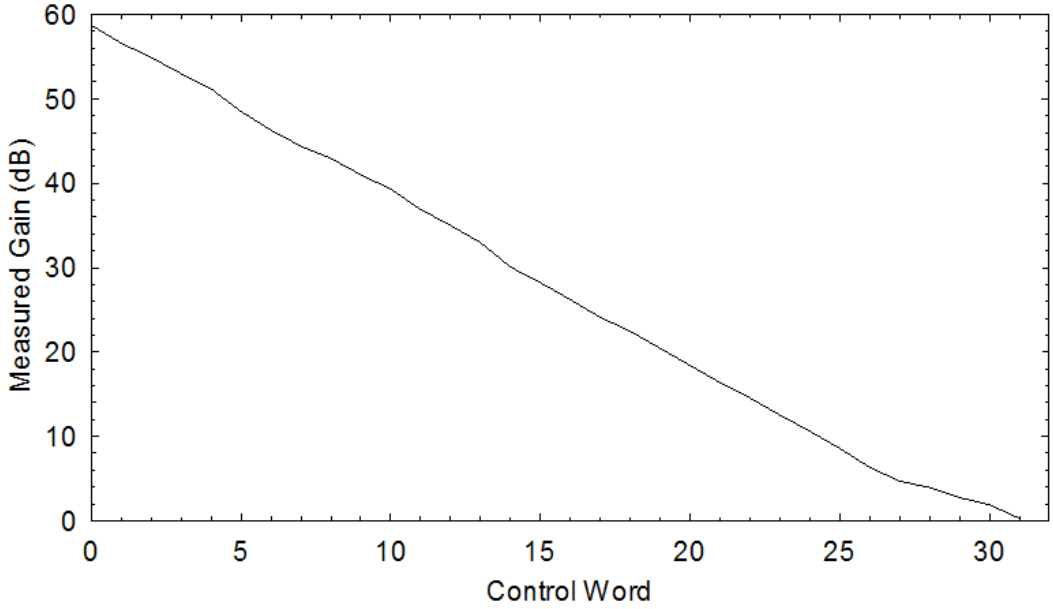

Fig. 83. Gain control word vs measured gain of the baseband section.

Linearity

The IIP3 is measured in a similar way than the explained in the filter and VGA-only calculations, resulting in a value of 27.1 dB.

Noise Figure

The NF is measured in a similar way than the explained in the filter calculations, resulting in a value of 33.48 dB.

Summary of Results

Table XVI presents a summary of the different measurements presented in this section. As the table shows, the measured results are similar to the expected values except for the NF, which is a little higher than the specification.

Table XVI. Summary of results (CSF+VGA).

Parameters	**Specification**	**Post-Layout**	
Adjacent channel rejection	>50 dB	>50 dB	>49.72 dB
f_{3dB}	1-2 MHz	1.1-2.28 MHz	1.12-2.29 MHz
IIP3	>15 dBm	30.91 dBm	27.1 dBm
Pass-band gain	0-60 dB	-0.07-59 dB	-0.13-59.5 dB
Current consumption	Minimum	10.25 mA	10.42 mA
Noise Figure	<33 dB	32.2 dB	33.25 dB
Power Supply	1.8 V		
Area	1..45x1.4 mm^2		
Technology	0.18 µm IBM CMOS		

Summary

This chapter has presented the measurement results of the baseband section chip including the CSF, VGA and CSF+VGA. The measurements show that the baseband chip meets the specifications required to operate in the EVA Radio Receiver.

CHAPTER VI

CONCLUSION

This dissertation has discussed the main challenges and solutions for the implementation of wireless medical circuit and systems for implantable and wearable applications. To WMS for blood pressure monitoring of small laboratory animals (implantable) and cardiac-activity (12-lead electrocardiogram) of patients with chronic diseases (wearable) were described. The main design methodology and power estimation based on a power consumption vs. lifetime analysis was included for the two systems with measured results closed to the expected values. The systems were using *in-vitro* conditions showing successful operation for the desired range.

This dissertation has also presented two transistor-level implementations of a biopotential amplifier and the baseband section of a wireless receiver, consisting of a channel selection filter (CSF) and a variable gain amplifier (VGA). The proposed amplifier achieved results comparable with state of the art designs thus providing a good solution for low-noise/low-power applications. The filter and VGA presented in the last chapter included frequency and gain tuning and a DC-cancellation loop is added to avoid saturation on the sub-sequent analog-to-digital converter block. The presented WMS can integrate the proposed biopotential amplifier and baseband section with small modifications depending on the target signal while using the low-power-oriented algorithm to obtain further power optimization.

REFERENCES

[1] G. Anderson, *Chronic care: making the case for ongoing care*, Princeton, NJ: Robert Wood Johnson Foundation, 2010. [E-book] Available: *www.rwjf.org/pr/product.jsp?id=50968* [Accessed: November 12, 2013].

[2] D. Scheller-Kreinsen, M. Blumel, and R. Busse. "Chronic disease management in Europe," *Eurohealth*, vol.15, no.1, pp.1-5, Jan. 2009.

[3] D. Yach, C. Hawkes, C. Gould, and K. J. Hofman, "The global burden of chronic diseases: Overcoming impediments to prevention and control," *Journal of the American Medical Association,* vol. 291, pp. 2616-2622, Jun. 2004.

[4] Centers for Disease Control and Prevention, *The Power of Prevention. Chronic disease… the public health challenge of the 21st century*. Atlanta, GA, 2009.

[5] R. Busse, M. Blümel, D. Scheller-Kreinsen, and A. Zentner, *Tackling Chronic Disease in Europe Strategies, Interventions and Challenges*. Berlin: World Health Organization, 2010.

[6] J. H. Choi and D. K. Kim, "Health-Care Devices Using Radio Frequency Technology," in *CMOS Biomicrosystems,* K . Iniewski, New York: John Wiley & Sons, Inc., 2011, pp. 93-117.

[7] A. Dittmar, F. Axisa, G. Delhomme, and C. Gehin, "New concepts and technologies in home care and ambulatory monitoring," *Studies in Health Technology and Informatics*, vol. 108, pp. 9-35, 2004.

[8] G. Harsanyi, *Sensors in Biomedical Applications: Fundamentals, Technology and Applications*. New York: CRC Press LLC, 2000.

[9] J. E. Gaxiola-Sosa and K. Entesari, "Design and implementation of a wireless medical system prototype for implantable applications," *Analog Integrated Circuits and Signal Processing (accepted),* Apr. 2014.

[10] J. E. Gaxiola-Sosa, N. Mohsin, J. A. Palliyali, R. Tafreshi, and K. Entesari, "A Portable 12-Lead ECG Wireless Medical System for Continuous Cardiac-Activity Monitoring," presented at the *2014 IEEE 2nd Middle East Conference on Biomedical Engineering (MECBME),* Doha, Qatar, 2014.

[11] J. E. Gaxiola-Sosa and K. Entesari, "A wireless medical system prototype for implantable applications," in *2013 IEEE Fourth Latin American Symposium on Circuits and Systems (LASCAS),* 2013, pp. 1-4.

[12] J. E. Gaxiola-Sosa, J. Coulon, E. Sanchez-Sinencio and K. Entesari, "A Fully Integrated Ultra-Low-Noise/Low-Power Biopotential Amplifier for ECG Applications," submitted to the *IEEE Journal of Solid-State Circuits,* Apr. 2014.

[13] J. E. Gaxiola-Sosa, H. Hedayati, L. Pengcheng, and K. Entesari, "A CMOS inverse Chebyshev channel selection filter for extravehicular activity (EVA) radio receivers," in *2013 IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS),* 2013, pp. 217-220.

[14] P. Gerrish, E. Herrmann, L. Tyler, and K. Walsh, "Challenges and constraints in designing implantable medical ICs," *IEEE Transactions on Device and Materials Reliability,* vol. 5, pp. 435-444, Sept. 2005.

[15] Texas-Instruments, "MSP430x4xx Family User's Guide," SLAU056G datasheet, 2007 [Revised 2013].

[16] P. D. Bradley, "An ultra low power, high performance Medical Implant Communication System (MICS) transceiver for implantable devices," in *IEEE Biomedical Circuits and Systems Conference, 2006, BioCAS 2006,* pp. 158-161.

[17] Federal Communications Commission, *FCC Rules and Regulations 47 CFR Part 95, Subparts E (95.601-95.673) and I (95.1201-95.1219) Personal Radio Services.* Washington, DC, Nov. 2002.

[18] R. Pallas-Areny and J. G. Webster, "AC instrumentation amplifier for bioimpedance measurements," *IEEE Transactions on Biomedical Engineering,* vol. 40, pp. 830-833, Aug. 1993.

[19] Y. Chih-Jen, C. Wen-Yaw, and C. Mely Chen, "Micro-power low-offset instrumentation amplifier IC design for biomedical system applications," *IEEE Transactions on Circuits and Systems I: Regular Papers* vol. 51, pp. 691-699, Apr. 2004.

[20] M. A. Smither, D. R. Pugh, and L. M. Woolard, "C.M.R.R. analysis of the 3-op-amp instrumentation amplifier," *Electronics Letters,* vol. 13, p. 594, 1977.

[21] R. Schaumann and M. E. Van Valkenburg, *Design of Analog Filters*. New York: Oxford University Press, 2001.

[22] F. Maloberti, *Data Converters*. Dordrecht, The Neteherlands: Springer, 2008.

[23] J. G. Webster, *Medical Instrumentation: Application and Design,* 3rd ed. New York: Wiley, 1998.

[24] R. F. Yazicioglu, C. Van Hoof, and R. Puers, *Biopotential Readout Circuits for Portable Acquisition Systems*. New York: Springer Science + Business Media B.V. , 2009.

[25] Kyocera Corporation, "RF SAW filter," SF16-043C5UU01 datasheet, 2008.

[26] J. Davies, *MSP430 Microcontroller Basics*. Oxford, UK: Elservier, 2008.

[27] Texas-Instruments, "MSP430 Software Coding Techniques," Appl. Note SLAA294A, 2007.

[28] Eagle-Picher-Medical-Power, "Implantable Medical Batteries Catalog,", 2009.

[29] Q. Gu, *RF System Design of Transceivers for Wireless Communications*. New York: Springer, 2005.

[30] International Telecommunication Union, *Recomendation ITU-R SA.1346*. Geneva, Switzerland: Headquarters, 1998.

[31] Microsemi Corporation, "Medical implantable RF transceiver," ZL70101 datasheet, May 2012.

[32] Data-Science-International, "PAC-12 PhysioTel Transmitter," datasheet, Jan. 2012.

[33] P. R. Kowey and P. Z. Kokovic, "Cardiology patient pages. Ambulatory electrocardiographic recording," *Circulation*, pp. 108:e31-e33, 2003.

[34] S. D. Sharp, J. W. Mason, and B. Bray, "Comparison of ST depression recorded by Holter monitors and 12-lead ECGs during coronary angiography and exercise testing," *Journal of Electrocardiology*, vol. 25, pp. 323-31, Oct. 1992.

[35] Texas-Instruments, "ADS129xx Low-Power, 8-Channel, 24-Bit Analog Front-End for Biopotential Measurements," SBAS459J datasheet, Jan. 2014.

[36] Texas-Instruments, "CC2500 Low-Cost Low-Power 2.4 GHz RF Transceiver," SWRS040C datasheet, May, 2009.

[37] A. J. Palliyali, R. Tafreshi, N. Mohsin, and L. Tafreshi, "A Comprehensive Algorithm for the Analysis of ECG Waveforms," in *ASME 2012 International Mechanical Engineering Congress & Exposition*, Houston, TX, pp.477-481.

[38] Telemed Solutions Inc, "TM-12 PC-Based Wireless 12-Lead EKG," product brochure, Chino, CA, 2013.

[39] Great Lakes Neurotechnologies LLC, "BioRadioTM 150 Wireless Biomedical Monitor," product user guide, Valley View, OH, 2011.

[40] S. R. Steinhubl, E. D. Muse, and E. J. Topol, "Can mobile health technologies transform health care?," *Journal of the American Medical Association,* vol. 310, pp. 2395-6, Dec. 2013.

[41] A. C. Metting van Rijn, A. Peper, and C. A. Grimbergen, "High-quality recording of bioelectric events," *Medical and Biological Engineering and Computing,* vol. 28, pp. 389-397, Sept. 1990.

[42] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE Journal of Solid-State Circuits,* vol. 38, pp. 958-965, Jun. 2003.

[43] M. Degrauwe, E. Vittoz, and I. Verbauwhede, "A Micropower CMOS-Instrumentation Amplifier," *IEEE Journal of Solid-State Circuits,* vol. 20, pp. 805-807, Jun. 1985.

[44] N. Verma, A. Shoeb, J. Bohorquez, J. Dawson, J. Guttag, and A. P. Chandrakasan, "A Micro-Power EEG Acquisition SoC With Integrated Feature Extraction Processor for a Chronic Seizure Detection System," *IEEE Journal of Solid-State Circuits,* vol. 45, pp. 804-816, Apr. 2010.

[45] R. F. Yazicioglu, K. Sunyoung, T. Torfs, K. Hyejung, and C. Van Hoof, "A 30 µW Analog Signal Processor ASIC for Portable Biopotential Signal Monitoring " *IEEE Journal of Solid-State Circuits,* vol. 46, pp. 209-223, Jan. 2011.

[46] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization," *Proceedings of the IEEE,* vol. 84, pp. 1584-1614, Nov. 1996.

[47] D. J. Comer, D. T. Comer, J. B. Perkins, K. D. Clark, and A. P. C. Genz, "Bandwidth Extension of High-Gain CMOS Stages Using Active Negative Capacitance," in *13th IEEE International Conference on Electronics, Circuits and Systems(ICECS), 2006.*, pp. 628-631.

[48] B. Razavi, *Design of analog CMOS integrated circuits*. Boston, MA: McGraw-Hill, 2001.

[49] C. Enz, F. Krummenacher, and E. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *Analog Integrated Circuits and Signal Processing*, vol. 8, pp. 83-114, Jun. 1995.

[50] A. I. A. Cunha, M. C. Schneider, and C. Galup-Montoro, "An MOS transistor model for analog circuit design," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 1510-1519, Oct. 1998.

[51] M. C. Schneider and C. Galup-Montoro, *CMOS Analog Design Using All-Region MOSFET Modeling*. Cambridge, UK: Cambridge University Press, 2010.

[52] H. Amir-Aslanzadeh, E. J. Pankratz, and E. Sanchez-Sinencio, "A 1-V +31 dBm IIP3, Reconfigurable, Continuously Tunable, Power-Adjustable Active-RC LPF," *IEEE Journal of Solid-State Circuits*, vol. 44, pp. 495-508, Feb. 2009.

[53] T. Delbruck and C. A. Mead, "Adaptive photoreceptor with wide dynamic range," in *1994 IEEE International Symposium on Circuits and Systems (ISCAS), 1994*, pp. 339-342 vol.4.

[54] Z. Sining and M. C. F. Chang, "A CMOS passive mixer with low flicker noise for low-power direct-conversion receiver," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 1084-1093, May 2005.

[55] K. Jordy, "Low-power amplifier chopper stabilization for a digital-to-analog converter," M.S. thesis, Massachusetts Institue of Technology, Cambridge, MA, 2008.

[56] Q. Chengliang, J. Parramon, and E. Sanchez-Sinencio, "A Micropower Low-Noise Neural Recording Front-End Circuit for Epileptic Seizure Detection," *IEEE Journal of Solid-State Circuits,* vol. 46, pp. 1392-1405, Jun. 2011.

[57] National Aeronautics and Space Administration, *Extravehicular Activity (EVA): Astronauts Walk In Space,* Washington, DC: Office of Headquarters Operation, 2009.

[58] B. Razavi, "Design considerations for direct-conversion receivers," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing,* vol. 44, pp. 428-435, Jun. 1997.

[59] Q. Gu, *RF System Design of Transceivers for Wireless Communications*, New York: Springer, 2005.

[60] P. J. Stephanou, J. P. Black, and A. L. Benjamin, "Miniaturized multi-band filter banks for Extravehicular radio (EVA) Applications," in *IEEE Radio Frequency Integrated Circuits Symposium, 2008. RFIC*, 2008, pp. 171-174.

[61] G. Szentirmai, "Electronic filter design handbook," *Proceedings of the IEEE,* vol. 70, pp. 317-317, Mar. 1982.

[62] A. C. M. De Queiroz, L. P. Caloba, and E. Sanchez-Sinencio, "Signal flow graph OTA-C integrated filters," in *IEEE International Symposium on Circuits and Systems, 1988.* , 1988, pp. 2165-2168 vol.3.

[63] R. Schaumann, *Design of analog filters*. New York: Oxford University Press, 2001.

[64] A. C. M. de Queiroz, "Chebyshev Filters," in *Wiley Encyclopedia of Electrical and Electronics Engineering*, New York: John Wiley & Sons, Inc., 2001.

[65] A. Yoshizawa and Y. Tsividis, "Anti-blocker design techniques for MOSFET-C filters for direct conversion receivers," *IEEE Journal of Solid-State Circuits,* vol. 37, pp. 357-364, Mar. 2002.

[66] L. Tien-Yu, H. Chung-Chih, and M. Ismail, "A wide tuning range Gm-C filter for multi-mode CMOS direct-conversion wireless receivers," *IEEE Journal of Solid-State Circuits,* vol. 44, pp. 2515-2524, Sept. 2009.

[67] L. Tien-Yu and H. Chung-Chih, "Multimode Gm-C Channel Selection Filter for Mobile Applications in 1-V Supply Voltage," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 55, pp. 314-318, Apr. 2008.

[68] P. R. Gray, *Analysis and design of analog integrated circuits*. Hoboken, NJ: John Wiley & Sons, 2008.

[69] X. Jianhong, I. Mehr, and J. Silva-Martinez, "A High Dynamic Range CMOS Variable Gain Amplifier for Mobile DTV Tuner," *IEEE Journal of Solid-State Circuits,* vol. 42, pp. 292-301, Feb. 2007.

[70] N. Van Helleputte and G. Gielen, "A 70 pJ/Pulse Analog Front-End in 130 nm CMOS for UWB Impulse Radio Receivers," *IEEE Journal of Solid-State Circuits,* vol. 44, pp. 1862-1871, Jul. 2009.

[71] J. J. F. Rijns, "CMOS low-distortion high-frequency variable-gain amplifier," *IEEE Journal of Solid-State Circuits,* vol. 31, pp. 1029-1034, Jul. 1996.