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System-level design tool for switched capacitor DC-DC energy scavenging converters

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Abstract

This thesis deals with the system modelling and design of a Switched Capacitor DC-DC (SC DC-DC) nano-power converter in Complementary Metal Oxide Semiconductor (CMOS) technology for energy harvesting applications.

First of all, after a critical evaluation on the whole Integrated Circuit (IC) system structure, a Python script has been created in order to accurately analyse any system analytical behaviours before instantiating and running the Cadence usual simulations.

The code is an upgrade with respect to a pre-existing one ([1]): several comparisons are listed and explained to show the differences between the two, as well as stressing on our new dedicated features.

In order to validate the model on the code, then, a feasibility study has been performed with a 180 nm United Microelectronics Corporation (UMC) technology process in the Cadence Virtuoso design suite. Good results let us state its reliability in being used both for the most of SC DC-DC architectures pre-design analysis and post-design verification: a full design space exploration shows how to use the script.

Finally, the SC DC-DC circuit D for bluetooth applications that we present uses the Taiwan Semiconductor Manufacturing Company (TSMC) 55 nm technology process and its design has been mostly realized by Luca Intaschi, during his PhD, and Francesco Dalena from Dialog Semiconductor in Livorno. The circuit D converter is meant to be part of a sensor node (that needs to survive in total absence of battery recharge) supplied by a Thermo Electric Generator (TEG) which guarantees a very low input voltage to the system of about $0.2 - 0.25$ V. Our work on it has focused on looking for an upgrade in order to increase its Power Conversion Efficiency (PCE). A new design which is able to properly work has been simulated and we provide some insight and constraints for future following upgrades.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

In emergent applications such as implantable/wearable biomedical devices and wireless sensor networks, the analog and digital modules in modern mixed-signal system on chips are designed to consume extremely low power. Energy harvesting is an attractive way to provide power supply to such systems in order to avoid inconvenient battery replacement. However, size limitation restricts the amount of harvested power: special requirements for those applications are, in fact, small size, long operating life and low cost. Examples of an energy scavenging application can be found in wireless sensor nodes for fitness activities: their data do not change very often and so they can be intermittently transmitted, guaranteeing low duty cycles and directly linked low operating frequencies.

Efficient DC-DC up-conversion at such low power ranges (for battery charging) is extremely challenging: DC-DC converters are the main circuits that are responsible of generating multiple voltage levels for different loads since they are widely used to harvest energy from DC sources and yield high PCE.

Three main types of DC-DC converters exist: the Low Drop Out (LDO) regulator, Switched Inductor (SI) and Switched Capacitor (SC) ones.

The LDOregulator is not a good solution for small, low power devices because its PCE is dependent on the voltage drop across its input and output. Although the SI are widely used to harvest energy from DC sources and yield high PCE, they require a bulky off-chip inductor which makes chip integration difficult. Therefore, the SC converter remains the best solution for simple and complete on-chip integration, and are favored for applications which require small form factors and high PCE.

However, at low power levels, the SC converter PCE has been constrained by overheads of clock generation and level-conversion to drive the switch capacitors. As a result, efficient SC converter operation has been limited to the μW range.

This thesis deals with the design of a nano-power integrated DC-DC converter featuring low output power of 1-10 μW and high PCE despite the low input voltages (about 0.2 to 0.25 V) available from a TEG.

A TEG is an energy source able to convert thermal energy into electric power

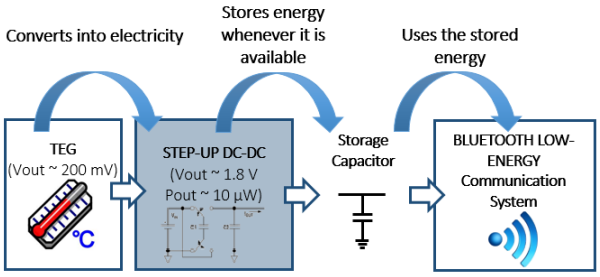

Figure 1.1: Design specifications

from very low temperature drops (for example, a Micropelt generators of 4 cm x 4 cm provides 50 mV/K) to be delivered at a low voltage. This voltage must be boosted significantly so that the power can be used as a standard electrical system power supply.

Here the DC DC converter steps up the TEG output voltage and charges a large external storage capacitor. This capacitor provides energy to a low energy bluetooth communication system, operating at very low duty cycle.

Due to the critical behaviours and strict constraints of those kind of systems, great care has been put into analysing the second block of Figure 1.1. All power losses, such as those of the oscillator and of the charge pump driving circuits, are taken into account.

Fundamental issues encountered in this work are due to switch resistances that rapidly increase for low driving voltages. In addition, for a big voltage conversion ratio, a large number of cascaded stages are needed, decreasing system PCE. Finally, at such low voltages, clock and driver circuitry are significant contributors to the total power consumption.

Structure of the thesis In Chapter 2, after a brief historical introduction, we will present the whole behavioural analysis and characterization of switched capacitors topologies, their limitations and features and the other blocks needed for the complete circuit. The chapter concludes with a brief survey of the software tools used in the analysis.

In Chapter 3 we describe, with a strong emphasis on our design strategy, some of the main difficulties the designer must address when dealing with such a project. In the first part of the design process we define the specifications, and analyse several design choices by developing a dedicated system modelling tool. In this way we rapidly explore a vast design space and evaluate different architectures at a high level of abstraction, gaining important insights into system level design trade offs. Then, we proceed with the usual circuit level design.

In Chapter 4 we explain how the first part of our work is validated using a circuit simulation. Then we show the validity of our system-level modelling tool through comparisons with a complete SC DC-DC converter designed and

fabricated with the TSMC 55 nm CMOS process. We conclude the chapter by comparing results from circuit simulations and the system-level modelling tool ones for each functional block needed in the complete circuit.

In Chapter 5 we explore a design improvement to increase PCE. This last part of the thesis is based upon work performed in the Dialog Semiconductor design center in Livorno, using their 55 process.

Finally, in Chapter 6, a brief discussion of our system-level modelling tool and design is reported, together with insight into possible future developments.

Chapter 2

Switched capacitor DC-DC converters

2.1 Main types of DC-DC converters

Integrated DC-DC power converters are ubiquitous circuits that extract energy from a DC voltage generator at the input and provide it at the output at a different DC voltage level.

One of the main figures of merit is the Power Conversion Efficiency PCE, i.e. the ratio of the power provided at the output to the total power absorbed by the converter.

In the introduction we have mentioned tree main ways to convert voltages in an IC.

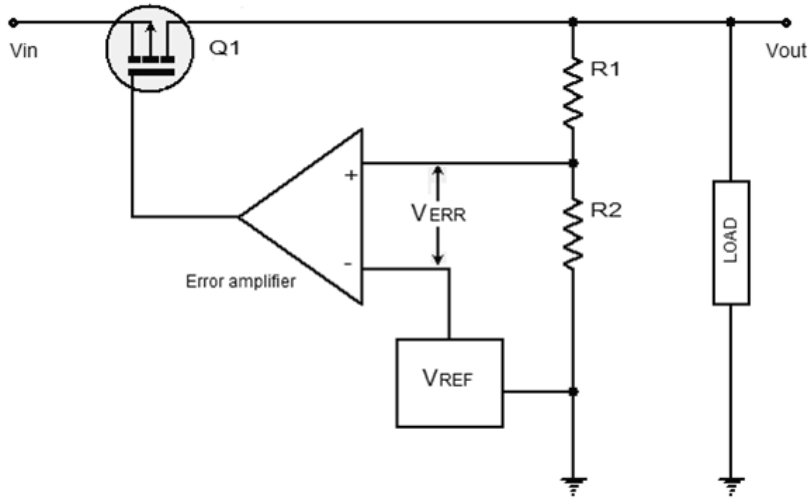

Figure 2.1: LDO voltage regulator schematic.

The LDO regulator is a simple voltage converter and it was presented for the

first time in 1977 by Robert Dobkin who implemented it with a power FET and a differential error amplifier [3]. In simple words dropout voltage is the voltage dropped by the regulator circuitry alone for its working[1].

In Figure 2.1 there is a schematic of a typical LDO voltage regulator. The working principle of LDO regulator is not so different from linear voltage regulator. The essential components of an LDO voltage regulator are a reference voltage source, error amplifier and series pass element (BJT or MOSFET). The voltage drop across the series pass element is controlled by the error amplifiers output in order to control the output voltage. For example, suppose the load current decreases and, as results, the output voltage tends to increase. This increase in output voltage will increase the error voltage (V_{ERR}). The output of the error amplifier will increase, making the series pass element (P-Channel MOSFET) less conducting, which results in the reduction of the output voltage. The output voltage is brought back to the original level:

$$V_{out} = (1 + \frac{R_1}{R_2})V_{ref} \tag{2.1}$$

There are many advantages of implementing al LDO: there are no noisy switches, total area is small (as it does need neither inductors nor transformers), and the circuit itself is very simple. Its use has been overcome by other converters because it dissipates power across the regulation device in order to work . In fact, it is important to keep thermal considerations in mind when using it. Having high current and/or a wide differential between input and output voltage could lead to large power dissipation. Additionally, PCE will suffer as the differential widens. Depending on the package, excessive power dissipation could damage the LDO or causes it to go into thermal shutdown.

[1]For example, an LM2941 LDO voltage regulator has a dropout voltage of only around 0.5 V, which means that in order to get 5 V at the output you need to input only 5.5 V where an ordinary 7805 linear voltage regulator has a dropout voltage of around 2 V. This means that, in order to get 5 V at the output of 7805 you need to input at least 7 V.

Switching converters ideally consist only of reactive elements and switches, and therefore they should have a very limited active power consumption.

They can be base on inductors or on switched capacitors (see Figure 2.2 and Figure 2.3).

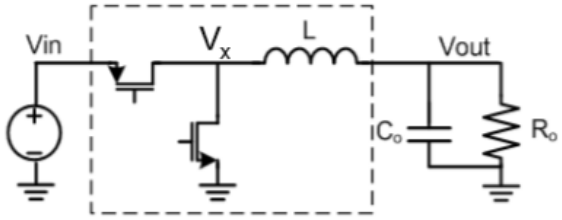

Figure 2.2: Step down converter.

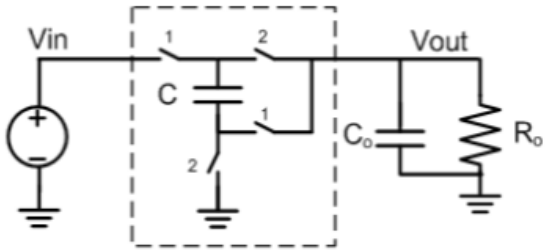

Figure 2.3: A simple switched capacitor converter (conversion ratio of 1/2).

DC-DC conversion by means of capacitors differs fundamentally from an inductive DC-DC converter. The latter have been dominant in the IC power management field for years. However, inductors cause large electro-magnetic interference and cannot be integrated. SC DC-DC converters, storing their energy on capacitors, become more and more interesting in recent years, because they seems to avoid most of the drawbacks of the inductor counterparts.

One of the first differences between them is that in inductor-based converters the conversion ratio is set by the duty cycle of the frequency wave which drives the charge pump while in capacitor ones it is due to the topology of the circuit.

Furthermore, lossless conversion can only be achieved at very high switching frequencies or by a converter with an infinitely large amount of capacitance. In practice, a properly designed capacitive DC-DC converter faces only a small PCE penalty for violating these requirements.

Considering our application, and the strong advantage provided by complete integration, we are focused on SC DC-DC converters.

DC-DC converters have always been very common in industry: they have

typically provided fixed-ratio conversion (such as a simple doubling, halving or inverting of the voltage). They are used to provide the programming voltage for flash and other reprogrammable memories and to generate the voltages required by the serial communication standard RS232. There also exist discrete-capacitor SC converter ICs providing conversion for Light Emitting Diode (LED) lighting promising applications.

In recent years, commercial SC converters have appeared in the market.

- the TPS60311 chip from Texas Instrument (TI) is a single-cell (0.9 V to 1.8 V) to 3.3 V converter for consumer products witch supports regulation through the use of two conversion ratios and by varying switching frequency, allowing for precise regulation for IC applications. Additionally, the chip supports an extremely-low standby power (2μA), allowing its use in ultra-low-power applications, such as wireless sensor nodes.

- The LM3352 chip from National Semiconductor is a 200 mA buck/boost DC-DC converter chip. It employs an external-capacitor design using three flying capacitors which supports multiple conversion ratios and full output regulation. These products push SC converters into the space occupied by regulated inductor-based converters. Improvements in Printed Circuit Board (PCB) area utilization can be made by moving the capacitors on-chip.

- The MAX203E RS232 transceiver IC from Maxim uses internal capacitors to generate a 10 V supply from a single-polarity 5 V input. However, only a minute amount of power is available from this part. This research aims to improve the power density and flexibility of on-chip SC DC-DC power converters

2.2 Switched capacitor DC-DC converter principles and terminology

Since in a SC DC-DC converter we have only switches and capacitors we can easily imagine an elementary converters as a kind of black box with an arbitrary number of ports connected with a control block (Figure 2.4).

The first block is responsible for the conversion between the DC input and output voltage while the second one reads the output and modifies the converter operation.

The closed control loop is not always implemented: in some applications it is required because the output voltage is typically very sensitive to operation variation like load, frequency, output current, input voltage and temperature.

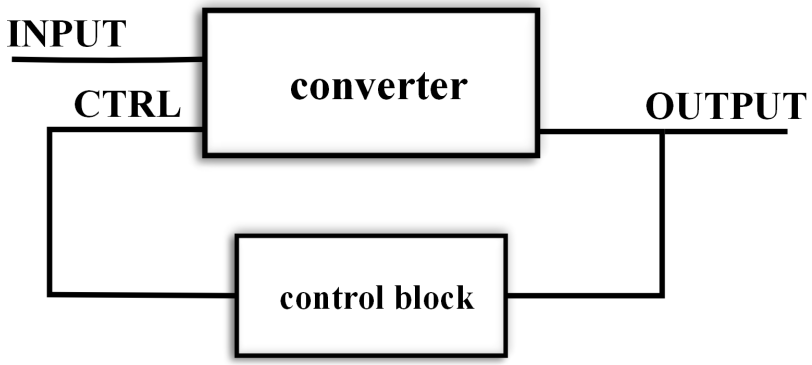

Figure 2.4: Simplified scheme of our IC.

2.2.1 The control block

Design of low-voltage and efficient energy-harvesting circuits is becoming increasingly important, particularly for autonomous systems.

In the case of thermoelectric of photovoltaic harvesting the energy source can have a very low voltage, and it can widely vary during operation.

Therefore, the design of a low input-voltage (low-V_{IN}) up-converter is critical for self-powered systems.

In this paragraph we would like to mention some of the proposed control strategies.

Output voltage and phase regulation Chen et al. ([8]) have proposed the method shown in Figure 2.5. It is applied to a fully integrated inductorless DC-DC converter for micropower energy harvesting with a 1.2 μW bandgap-refereced output controlled. It contains a modified four-phase charge pump and a 3x voltage boost; it is able to work with a minimum input voltage of 270 mV.

The control block mainly control the rising edge of Latch_1, derived from the system clock. As soon as it is revealed, a scaled output of the CP ($V_{DIV} \cdot V_{out}$) is compared with the bandgap reference voltage to gate the pump clock. Defining β the divide ratio of the voltage divider then V_{out} is regulated to V_{ref}/β thanks to the feedback loop. The comparison result is latched on the falling edge of Latch_2 until next comparison. The scaled output voltage V_{DIV} and the bandgap reference voltage V_{REF} are fed to the input nFET pair of the latch comparator. When V_{out} rises from zero during start-up, both V_{ref} and V_{DIV} are low, and the latch comparator cannot resolve in time before the falling edge of Latch_2. Therefore, an XOR operator is used to gate the comparator output. When the differential output of the comparator fails to swing to the opposite rails, the comparison result is bypassed, and the pump is kept enabled. This ensures correct pump control for a wide range of V_{out}, even when itself is very low.

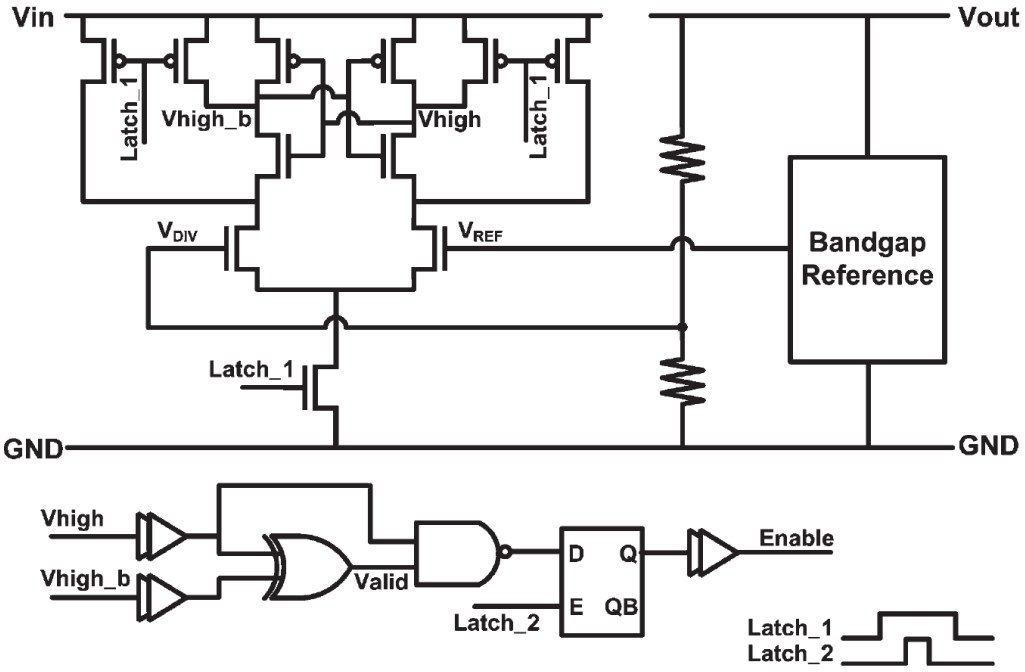

Figure 2.5: Example of output voltage based phase regulation.

Architecture variarion An other work ([10]) deals with some camouflages to keep the system as stable as possible by operating various architecture changes.

It regards a fully integrated low voltage charge pump for thermoelectric energy harvesting which has a dual-mode architecture. After a low start-up voltage in start-up mode with low PCE, it is able to high them up in normal operation mode after some changes in charge fluxes across the structure.

The proposed dual-mode 10-stage charge pump, in fact, combines a 5-stage Dickson charge pump and 10-stage CMOS one. The simplified schematic in Figure 2.6 show how M1 and M2 form Dickson charge pump and are used to charge C_{OUT} at the start-up as shown in (a). At operation mode, the CMOS switches (M3-M6) are driven with high amplitude clock and on-resistance decreases as shown in (b). The first half stages of the CMOS charge pump is constructed from the nMOS transistors (M3, M4) and the back half stages are constructed from pMOS ones (M5, M6).

This scheme ensures the maximum overdrive voltage can be provided to each transistor when gate is driven by high voltage clocks as ϕ. The transistors M1 and M2 are stil functional but most of the current flows through the CMOS switch (M3, M4) because the on-resistance is much smaller than that of diode connected MOSFETs (M1, M2). As a result, the CMOS charge pump improves thePCE while Dickson one achieves low voltage start-up.

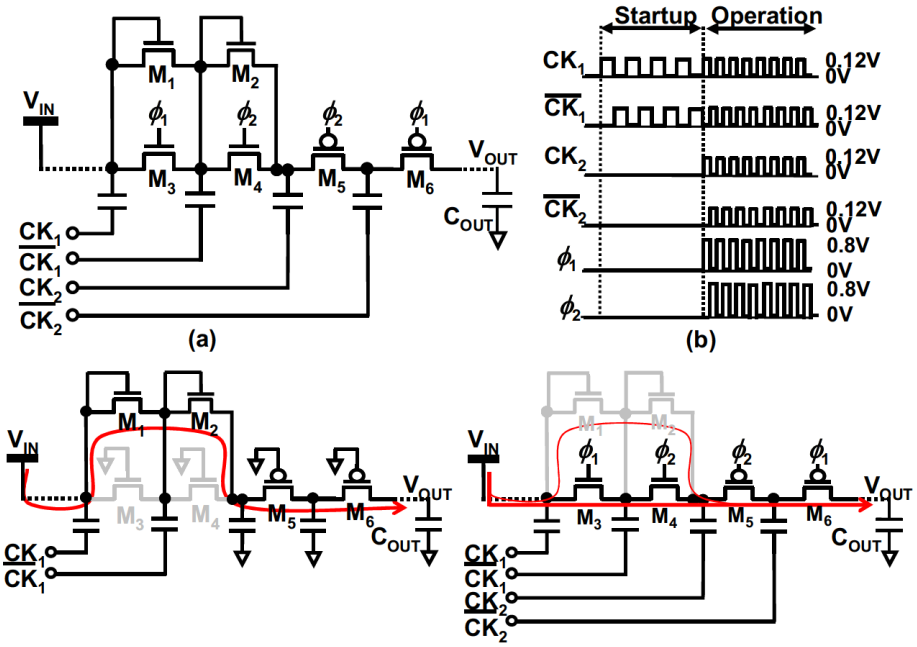

Figure 2.6: Simplified circuit schematic (a) and operation sequences (b) of the dual-mode charge pump. Start-up mode and operation mode on the bottom.

2.2.2 The conversion block

Starting our study on the conversion block we can reconsider Figure 2.3 (it is a basilar step-down converter with a VCR of 1/2) and provide some nomenclature to better analyse and deal with this kind of circuit.

Based on how switches are controlled by clock phases, it is possible to obtain different *topologies* of the same circuit and, as a consequence, a different output voltage (due to the periodic of changes in their structures, SC DC-DC are also called Variable Structure Systems (VSS)).

A converter consst of a varyng number of sub-converters (*stages*) to expand the conversion ratio range: *multi-ratio* converter is a single-stage SC that can implement one or several topologies. It is also possible that a converter stage implements a number of parallel copies of the topology called *interleaved phases*. A *phase* is one of the n non overlapping splits in a switching period $(\phi_1 \dots \phi_n)$. It is by switching through those phases that the converter performs different conversions.

Each converter block i has an ideal $iVCR$ which is the maximum reached ratio of output to input voltage and it is associated with a certain topology. It is called *ideal* because it is met only if the reached PCE η is 100%:

$$i\text{VCR} = \frac{V_{out}}{V_{in}} \tag{2.2}$$

It should be clearer now how the designer has a large range of possible imple-

mentations to achieve a given conversion ratio.

In each SC DC-DC converter there are two different kind of capacitors: *flying*, (C), qhich have a varying common voltage, and bypass, C_O, also called *output buffer*, that have a quasi-constant common mode voltage.

To transfer charge between input and output port, capacitors have to be charged and discharged. Let us consider the simple buck converter shown in Figure 2.3, during phase ϕ_1, C is connected between input generator and output, while during ϕ_2 is in parallel with C_O: with no loads C_O keeps the whole voltage drop to obtain:

$$V_{in} = V_C + V_{C_O} = 2V_{out} \tag{2.3}$$

The voltage drop between input and output ports (needed by the continuous charging and discharging of the capacitors) is proportional to the output current, therefore each converter can be directly represented with the model shown in Figure 2.7; an ideal transformer with a turns ratio equal to iVCR and an output resistance R_{eq}.

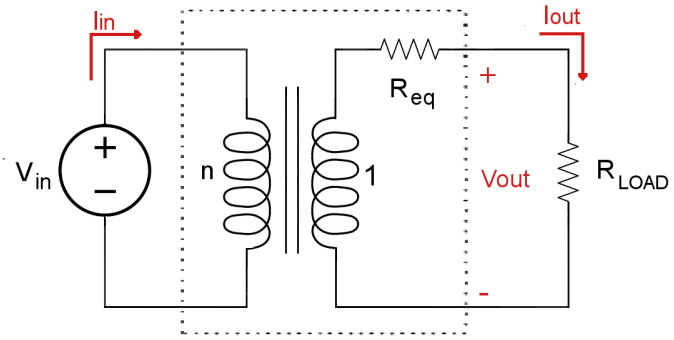

Figure 2.7: Idealized SCC converter model.

Since the ideal transformer has no energy consumption we have

$$I_{in} = -\frac{1}{i\text{VCR}} \cdot I_{out}, \tag{2.4}$$

R_{eq} is a low-frequency equivalent impedance. It determines the open-loop output voltage and sets the maximum converter power.

As it is clearly explained in [1], two working asymptotic limits can be distinguished for R_{eq}, and they are function of the switching frequency:

- *Slow Switching Limit (SSL)*: it is assumed that, because of the slow frequency operation, the switches and all the other interconnections are ideal and have no impact on the R_{eq}, while capacitors are ideally impulsively transferring charge letting the current flow between input and output, being the most relevant contribute to internal power dissipation.

- *Fast Switching Limit (FSL)* : at a high rate frequency we cannot assume switches and interconnects as ideal, so we need to take them into account with their own associated impedances and those losses are going to be prevalent, with respect to the capacitor ones, in the calculation of charge pump power losses.

2.3 SC DC-DC analysis

To explore the complex behaviour of an SC DC-DC converter we would like to start from a particular architecture and go into the details of any its characteristics.

Figure 2.3 shows the Series-Parallel converter, with an ideal conversion ratio of 1/3.

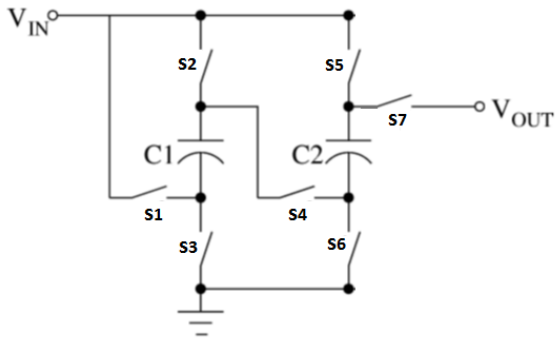

Figure 2.8: A series-parallel converter with VCR = 1/3.

It is convenient to take into account a medium model of analysis in steady-state: first of all, we assume that switches and capacitors are ideal, without considering Equivalent Series Resistance (ESR) or gate-drive or bottom plate contributions. .

The output resistance of the SC DC-DC converter is set once the charge flows q_c and and q_r across each capacitor and switch in a clock period. If we define

$$q_{out} = \frac{I_{out}}{f_s}, \tag{2.5}$$

where I_{out} is the load current and f_s the switching frequency, they can be expressed as the product between q_{out} and a constant vector:

$$\begin{aligned} q_c^j &= a_c^j \cdot q_{out} \\ q_r^j &= a_r^j \cdot q_{out}. \end{aligned} \tag{2.6}$$

a_c^j and a_r^j are charge vectors that can simply be uniquely and directly computed by inspection using the Kirchoff Current Law (KCL) in each topological phase

because they represent charge flow into the circuit components (switch or capacitance, as soon as the first is closed or the second one is charged to initiate each phase of the circuit) normalized with respect to the output charge flow.

To give a first simple example let us determine a_c and a_r for the circuit in 2.3. The two different configurations of the converter, related to the operation phases ϕ_1 and ϕ_2, are shown in Figure 2.9.

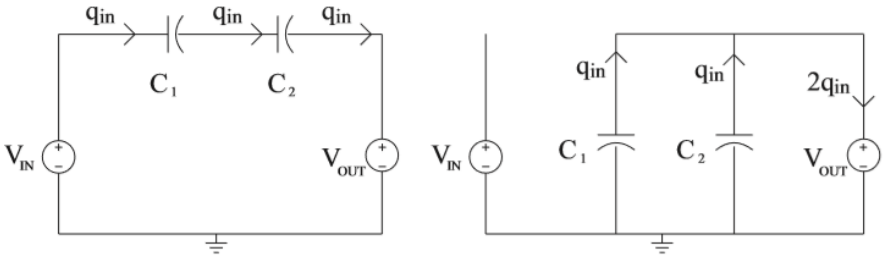

Figure 2.9: Circuit topology of the converter in Figure 2.3 for phase 1 (left) and phase 2 (right).

To determine a_c we neglect the impedance of each switch: V_{in} is connected with the rest of the circuit only during ϕ_1 and this let us define q_{in} as the input charge.

We can then apply current continuity and observe that the total charge variation on each capacitor in the whole clock period must be zero.

Therefore we have:

$$\begin{aligned} q_1^1 &= q_2^1 = q_{in} \\ q_1^2 &= -q_1^1 = -q_{in} \\ q_2^2 &= -q_2^1 = -q_{in} \\ q_{out}^1 &= q_{in} \\ q_{out}^2 &= -q_1^2 - q_2^2 = 2q_{in}. \end{aligned} \tag{2.7}$$

We can now obtain:

$$\begin{aligned} q_{out} &= q_{out}^1 + q_{out}^2 = 3q_{in}, \\ q_{in} &= \frac{q_{out}}{3}. \end{aligned} \tag{2.8}$$

By substituting this equation into (2.7) we obtain

$$a_c = \begin{bmatrix} a_{c1}^1 \\ a_{c2}^1 \end{bmatrix} = - \begin{bmatrix} a_{c1}^2 \\ a_{c2}^2 \end{bmatrix} = \begin{bmatrix} 1/3 \\ 1/3 \end{bmatrix}. \tag{2.9}$$

To deal with switches, as a counterpart, vector a_r is obtained considering their positions and states in both phases as well. This is very easy to do since we

already know how charge flows in the circuit [2].

$$a_r^1 = \begin{bmatrix} a_{r1}^1 \\ a_{r2}^1 \\ a_{r3}^1 \\ a_{r4}^1 \\ a_{r5}^1 \\ a_{r6}^1 \\ a_{r7}^1 \end{bmatrix} = \begin{bmatrix} 0 \\ -1/3 \\ -1/3 \\ 0 \\ -1/3 \\ -1/3 \\ 0 \end{bmatrix}, a_r^2 = \begin{bmatrix} a_{r1}^2 \\ a_{r2}^2 \\ a_{r3}^2 \\ a_{r4}^2 \\ a_{r5}^2 \\ a_{r6}^2 \\ a_{r7}^2 \end{bmatrix} = \begin{bmatrix} 1/3 \\ 0 \\ 0 \\ 1/3 \\ 0 \\ 0 \\ 1/3 \end{bmatrix} \tag{2.10}$$

In [1] and [2] there is an analysis of those two vectors and we will briefly explain it considering to have only two phases (as just previously done considering that, for instance, in (2.6), we have assumed j = 1,2) for our implementation since the multiphase case simply makes things complexer and it is not needed for our application.

2.3.1 Slow Switching Limit

First of all, for a full analysis, including input and output charge fluxes it is mandatory and this is why we need to define the two so-called *charge multipliers vectors* as

$$a^1 = \begin{bmatrix} a_{out}^1 \\ a_c^1 \\ a_{in}^1 \end{bmatrix}, a^2 = \begin{bmatrix} a_{out}^2 \\ a_c^2 \\ a_{in}^2 \end{bmatrix},$$

where $q_{in} = a_{in} q_{out} = (a_{in}^1 + a_{in}^2) q_{out}$ and, for charge conservation, $a_{out}^2 + a_{out}^1 = 1$.

Those are the only needed contributions to state output impedance under SSL condition: it is known from Tellegen theorem that, in each network, any vector of branch voltages that satisfied Kirchoff Voltage Law (KVL) is orthogonal to any vector of branch current (or, equivalently, charge flows) that satisfied KCL. In fact, applying it on each phase ϕ_j of steady-state periodic operation (once we have short-circuited the input and connected the output to an independent voltage source), if we call v^j the voltage drops between capacitors and voltage references it is guaranteed that

$$a^j v^j = 0.$$

Thinking now of calculating R_{eq} as the ratio of output voltage to output current we can write the total losses when the input generator is off as

$$v_{out}(a_{out}^1 + a_{out}^2) + \sum_i q_i \Delta v_i = 0. \tag{2.11}$$

The term with the sum (where $\Delta v_i = v_{c,i}^1 - v_{c,i}^2$) stands for power losses due to the capacitances while the first one is simply the energy given by the output

[2] During phase 1 swithces s2, s3, s5 and s6 are on while s1, s4 and s7 are off and vice-versa for phase 2. Negative values state that switch i blocks a negative current.

voltage generator. If we divide (2.11) by $f_s \cdot q_{out}^2$, then substitute $\Delta v_i = \frac{q_i}{C_i}$ and use the definition of $a_{c,i} = \frac{q_{in}}{qout}$ we obtain

$$R_{eq} = R_{SSL} = -\frac{v_{out}}{i_{out}} = \sum_i \frac{(a_{c,i})^2}{C_i f_s}. \tag{2.12}$$

2.3.2 Fast Switching Limit

This case is complementary to the previous one. Capacitors can be considered ideal and the only dominating impedances in each converter are the switches ones: their crossing-currents are almost constant and this is why we consider the charge flows through each one with the two switches charge flow vectors a_r^1 and a_r^2 just obtained in previous sections. Ripple on capacitors can be ignored.

Switch i has a duty cycle D_i with $i = 1, 2$ and a_r does not depend on it so, when a switch is closed:

$$i_{r,i} = \frac{a_{r,i} q_{out} f_s}{D_i} = i_{out} \frac{a_{r,i}}{D_i}. \tag{2.13}$$

because we have considered that $q_{r,i} = a_{r,i} q_{out}$ and $q_{out} = \frac{i_{out}}{f_s}$.

$$P_{fsl} = \sum_i D_i R_i \frac{a_{r,i}}{D_i} i_{out}, \tag{2.14}$$

where P_{fsl} is the total circuit loss where R_i is the resistance of switch i and so, dividing (2.14) by i_{out}^2 we obtain

$$R_{eq} = R_{FSL} = \frac{P_{fsl}}{i_{out}^2} = \sum_i \frac{R_i (a_{r,i}^2)}{D_i}. \tag{2.15}$$

We have demonstrated how this analysis leads the output impedance of an SC DC-DC converter to be interpreted in a dual way, in different limits. In fact, based on which one of the two limits we are dealing with, it is possible to ignore at all the switched capacitive nature for the resistive side, and all the resistances for the capacitive one.

Anyway both approaches have to be unified if we want to give a general and complete analysis. Since two limits are complementary, a reasonably accurate approximation is obtained considering

$$R_{eq} = \sqrt{R_{SSL}^2 + R_{FSL}^2}. \tag{2.16}$$

2.4 SC DC-DC converter structures

Since a large variety of DC-DC exists we will give a brief overview of some of the most common structures, highlighting their pros and cons.

The main differences among different structures are:

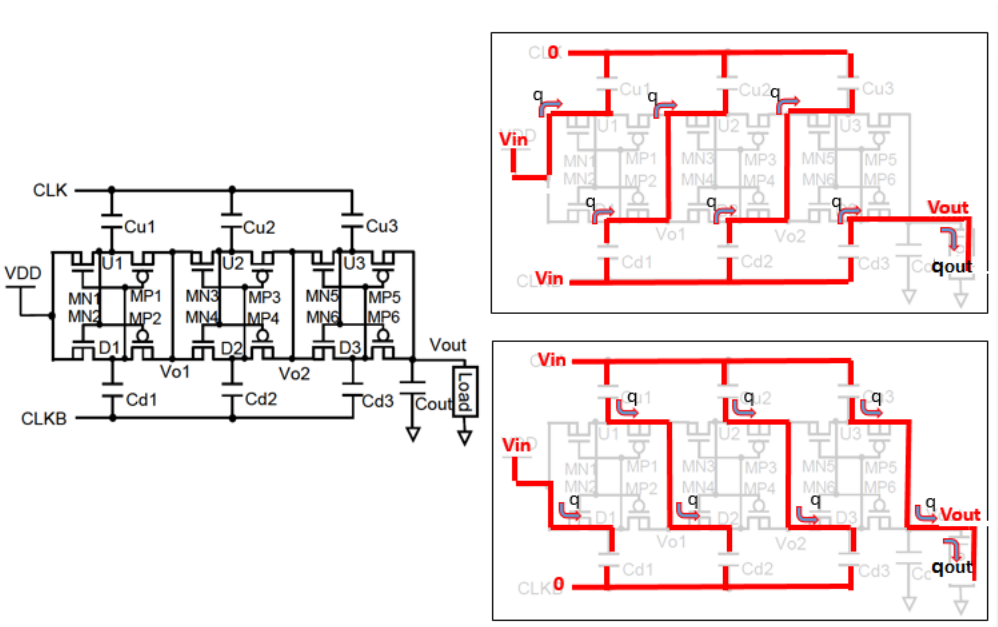

Figure 2.10: Chen architecture and its two phase configurations.

- conversion ratios,
- number of switches and capacitors needed,
- maximum voltage drops on switches and capacitors .

Based on our application and technology various circuit architectures can yield different PCE.

Let us do the analysis with a general iVCR of n/m, even if for our work we are considering only integer ones (m=1).

2.4.1 Up Converters

In the following we discuss some architecture which could be chosen for the final design.

Chen The first up converter configuration that we want to present is a non-standard one, fully explained by Chen [3] et al. in [5]: you can find is representation in Figure 2.10. Using a cross coupled switches driven by output of phase clocks, it is simple to see that, when CLK is high, MN2 and MP1 are turned on and D1 is charged to V_{DD}, while, with the CLK changing to low, MN1 and MP2 are on and so U1 is now charged at V_{DD}. Since D1 is driven by Cd1 and boosted from V_{DD} to $2V_{DD}$, it directly charges node Vo1. On the next half cycle U1 is

[3] We are calling it "Chen" then.

now pumped to $2V_{DD}$ doing the same as D1 has done before: charging Vo1 at $2V_{DD}$, which will be so always charged at $2V_{DD}$. Replicating this reasoning for the following stages it is clear how we can obtain an open-loop output (called $Vout_{nom}$ in the code [4]) voltage of

$$Vout_{nom} = V_{in}\dot{(}1 + k)$$

and each of the inter-stage voltage can be pumped to a fixed DC value. Charge fluxes in the SC DC-DC converter during each clock phase are shown on the right of the same Figure 2.10. Naming q_1 the amount of input charge which comes from the thermoelectric generator V_{in} during the first phase (assuming it is equal to the other phase q_2 since the structure is symmetrical and they have to flow across identical devices for the same time), the total amount of the charge fluxing to the output load in a clock period is equal to the sum of the two ones

$$q_{out} = q_1 + q_2 = 2q$$

This q is flowing both in switches and capacitors, and, according to a number of k stages, with $N = Vout/Vin = 1+k$, the charge multipliers vectors are resumed in being equal to

$$\begin{aligned} a_c[i] &= \tfrac{q_c}{q_{out}} = \tfrac{q}{q_{out}} = 0.5, \\ a_r[i] &= \tfrac{q_r}{q_{out}} = \tfrac{q}{q_{out}} = 0.5, \end{aligned} \tag{2.17}$$

for every i in

- nsw = number of switches = $4 \cdot (N - 1)$,
- $ncap$ = number of capacitors = $2 \cdot (N - 1)$.

Dickson The Dickson charge pump is very well known and is characterized by the use of two opposite-phase flying ladders (the Ladder topology explanation follows below).

It needs (n-1) capacitors and (n+4) switches to have a conversion ratio of n. In the case of n = 2 it reduces to simple Doubler architecture.

Figure 2.11 shows a n = 6 architecture and the corresponding charge multipliers are found by inspection:

$$\begin{aligned} a_r &= \left[3, 3, 3, 3, 3, 3, 2, 2, 1, 1\right]^T, \\ a_c &= \left[3, 1, 1, 1, 1\right]^T \end{aligned} \tag{2.18}$$

For a general architecture with n = k charge multipliers can be calculated by the formula:

$$\begin{aligned} a_r &= \left[\lfloor \tfrac{k}{2} \rfloor, \ldots, 2, 2, 1, 1\right]^T, \\ a_c &= \left[\lfloor \tfrac{k}{2} \rfloor, \lfloor \tfrac{k}{2} \rfloor, \lfloor \tfrac{k-1}{2} \rfloor, \lfloor \tfrac{k-1}{2} \rfloor, \ldots, 1, 1, 1, 1\right]^T \end{aligned} \tag{2.19}$$

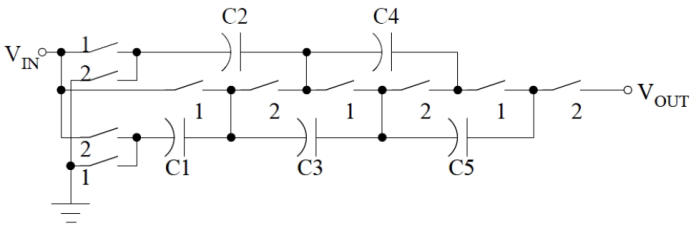

Figure 2.11: Dickson charge pump with n = 6.

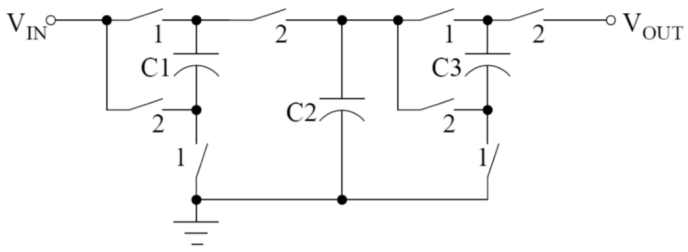

Figure 2.12: Doubler charge pump with n = 4.

Doubler Doubler topology consists of several base cells, which can be cascaded to duplicate multiple times the input voltage.

Two capacitors and four switches are needed for each cell and it is possible to realize conversion ratio n equal to 2^k where $k \in$N is the number of stages.

Figure 2.12 shows a two-stages (k = 2, n = 4) doubler architecture and its charge multipliers are:

$$\begin{aligned} a_r &= \left[8, 8, 4, 4, 2, 2, 1, 1\right]^T, \\ a_c &= \left[1, 1, 1\right]^T \end{aligned} \tag{2.20}$$

.

The general formula to calculate charge multipliers for a general $n = 2^k$ Doubler converter is:

$$\begin{aligned} a_r &= \left[2^{n-1}, 2^{n-2}, 2^{n-2}, \ldots, 2, 2, 1, 1\right]^T, \\ a_c &= \left[2^{n-1}, 2^{n-1}, 2^{n-1}, 2^{n-1}, 2^{n-2}, \ldots, 1, 1, 1, 1\right]^T \end{aligned} \tag{2.21}$$

Fibonacci This converter architecture is named after the well known Fibonacci's series. If F is the Fibonacci function where F_k is the respective k-th element in the series ($F = \{1, 1, 2, 3, 5, 8, 13, \ldots\}$), observing the circuit in Figure 2.13, which shows a n = 5 ratio, its charge multipliers are:

[4] Vin, in this case, is both our V_{DD} and the maximum amplitude of the clock signal.

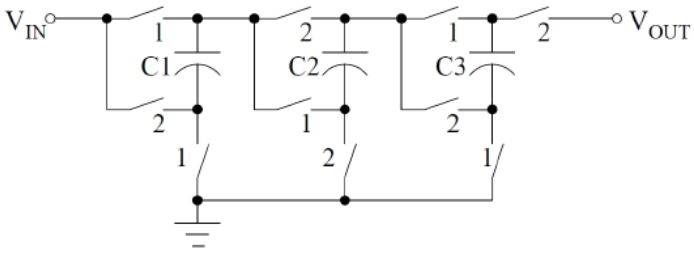

Figure 2.13: Fibonacci charge pump with n = 5.

$$\begin{aligned} a_r &= \left[3,2,2,2,2,2,2,1,1,1\right]^T, \\ a_c &= \left[2,1,1\right]^T. \end{aligned} \tag{2.22}$$

To calculate them for a general k you have to use the formula:

$$\begin{aligned} a_r &= \left[F_{k+1},F_k,F_k,F_k,\ldots,1,1,1\right]^T, \\ a_c &= \left[F_k,\ldots,2,1,1\right]^T. \end{aligned} \tag{2.23}$$

Comparison To briefly summarize up converters parameters you can have a look at Table 2.1 :

	ratio	switches	capacitors
Dickson	n	n-1	n + 4
Doubler	2^k	2k - 1	4k
Fibonacci	F_{k+2}	3k + 1	k

Table 2.1: Up converters parameters comparison.

2.4.2 Down Converters

In the following we provide a brief description of the architectures mostly used for scaling down voltage converters.

Ladder Ladder topology is the most famous one because of its simplicity in both behavior and realization. For a down-conversion factor of 1/n it is composed by (2n - 3) flying capacitors and 2n switches. It can be easily seen as composed with two branches:

- the first one (made by C_{fly1} and C_{fly2}) that connects input and output terminals and where capacitors voltage drops maintain nodes voltages at integer multiples of the input one

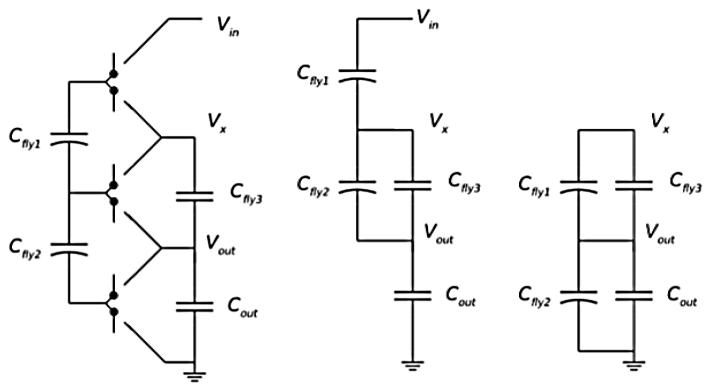

Figure 2.14: Ladder architecture, both operation phases

- the second one carries charge from the previous capacitors without changing their voltages.

For the circuit in Figure 2.14, where n = 3, charge multipliers are easily found:

$$\begin{aligned} a_r &= \left[2,2,1,1,1,1\right]^T, \\ a_c &= \left[2,1,1\right]^T. \end{aligned} \tag{2.24}$$

While, for a general conversion factor of n, the formula to calculate them is:

$$\begin{aligned} a_r &= \left[2,2,1,1,1,\ldots\right]^T, \\ a_c &= \left[(n-1),(n-2),(n-2),\ldots,2,2,1,1\right]^T. \end{aligned} \tag{2.25}$$

Fractional The Fractional Converter is one of converters families where, in most cases, the iVCR is hard to be determined by visual inspection, as well as its charge multipliers. Anyway, by some theorems, they can be synthesized (even if non-methodologically). A $\frac{4}{5}$ fractional converter topology is shown in Figure 2.15.

Comparison The table below summarizes down converters topologies taken into account:

	ratio	switches	capacitors
Ladder	n	n-1	n + 4
Series-Parallel	n	n-1	3n - 2
Fractional	2^k	2k - 1	4k

Table 2.2: Down converters parameters.

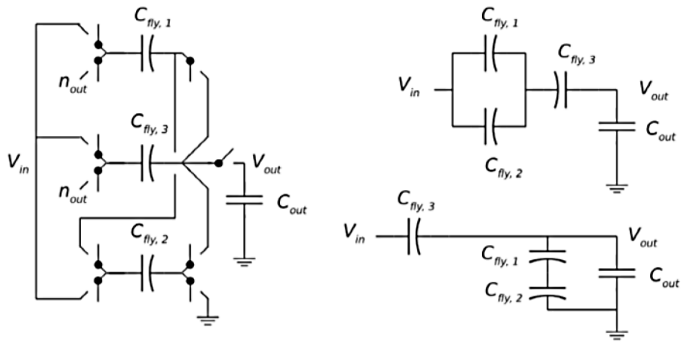

Figure 2.15: Fractional architecture with VCR = 4/5.

2.5 Additional blocks

As previously mentioned, a converter can not work on its own and, starting from the mentioned control block, some more functional blocks are needed.

Frequency generator New technologies and new market requests for smaller sizes and lower power consumption have driven researchers to use on-chip oscillators.

There can be various ways to drive the switching of the capacitors in our charge pump. Frequency generators for this kind of application are usually realized with Voltage Controlled ring Oscillator (VCO), ring oscillators or relaxation ones. Given the small supply voltage, a ring oscillator is more appropriate in our case.

Starting from the base architecture (a ring of simple inverters) our study is focused on improving its behaviour in terms of dissipated power and area occupation.

A more accurate final analysis ends up with a characterization of a current starved ring oscillator; MOS sizes and power losses are reduced in comparison with the classic structure, enabling better output performances .

Buffer chain Since a ring oscillator is not able to drive the whole load made of the MIM capacitors of the charge pump, a chain of buffer is needed.

A simple chain of inverters is enough to drive the output wave of the ring oscillator up to the flying capacitors of the converter block, but then some fine modifications have been done to improve the performance of our system.

2.6 Design and simulation tools

For the realization of those kind of projects the help of new and advanced design and simulation tools is crucial.

2.6.1 Simulator

To schematically design and simulate the whole architecture (block by block for the feasibility study and, then, all blocks together) we have used the Cadence Virtuoso design tool package (Virtuoso Schematic Editor L and ADE L) based on Spectre simulator. The beginning analysis, to check out the Python. code correctness, has been done with the UMC018 library available at our lab in Dipartimento Di Ingegneria Dell' Informazione. After that, we moved to the tsmc55 library owned by Dialog Semiconductor.

2.6.2 Help softwares

Anaconda This is a user-friendly environment used to develop the python script: it encompasses with a console, Spyder, a kernel and some others platforms to run our own project and follows its behaviour and development. It has been very helpful showing all the variables and parameters which we had to deal with in the same window as the growing script; a graphic tool for plotting is also included and it has been used to create some of the graphs you will find in this work.

QTGrace Excellent for graphs fitting and to generate .ps images to be transferred on this thesis: since Cadence images were not well saved we exported them on QTGrace (the Windows version of the famous MAC XMGrace) regenerating the needed graphs.

Crucial parts of the feasibility study has been developed thanks to this software.

Chapter 3

System-level Python design of a DC-DC switched capacitor converter

In any complex electronic design, a system-level simulation can be useful for making the main architectural design choices. One of the main goal of this work is finding an optimization for a SC DC-DC converter which has to be constrained by specific operation settings.

Our strategy has been built on the analysis of the main functions and physical operation of the implemented blocks. Once the behaviour of each block had been critically considered, it was easy to study and write down in Python code semi-analytical expressions for block operation and performance.

Then we can consider the operation of the complete circuit in different circumstances (different process, supply or constraints ...) by performing a design space exploration with the script.

To work with high level designs lets the designer to quickly understand the behaviour of the circuit. To see how everything can change in terms of performance, in fact, it is now enough to change parameters or just the functional description of a block and let the code run; it is very fast compared with the classical circuit simulations that would take definitely longer to be prepared/changed and then run on the ECAD tools.

The Python script attached to this thesis contains three sub files that will be described in the following sections.

Finally, a brief comparison with a pre-existing MATLAB code developed by Seeman et al. ([1]) for those kind of applications is presented, discussing pros and cons with respect to this work.

3.1 Parameters

First of all, it is mandatory to present something more about the project constraints: what we are given, what we need and what we are going to obtain numerically/quantitatively talking.

All of the parameters are stored in four different files (*process_parameters.txt*, *user_parameter.txt*, *external_parameters.txt* [1] and *global_parameters.txt*) which are read at running time from our script.

3.1.1 Process Parameters

The state of the art for Micro Electro Mechanical Systems (MEMS) and harvesting applications is full of emergent processes such as 80 nm, 55 nm or 22 nm.

According to the CMOS technology we have been using (UMC018 or TSMC55) we got to know everything about the process model parameters [2]:

- l_{min} (m): minimum transistor length for both p and n MOS,
- t_{ox} and t_{oxe} (m): nominal and effective oxide thickness,
- n : ideality factor,

and, for both n and p MOS,

- u_0 ($\mathrm{cm^2\,V^{-1}\,s^{-1}}$): charge mobility,
- v_{th0} (V): nominal threshold voltage,
- C_j ($\mathrm{F\,m^{-2}}$) junction capacitance per unit area,
- C_{jsw} and C_{gd0} (both measured in $\mathrm{F\,m^{-1}}$) for the parasitic MOS capacitances.

3.1.2 User Parameters

To develop our project, we need to deal with other (application based) constraints.

Our converter has to work at very low power due to the fact that input/available supply voltage is very low. A reasonable range for V_{in} could be 0.18 - 2.4 V at the running frequency of interest which are included between 1 and 20 MHz.The operating temperature of 25 °C (298 K) is chosen as we are not considering, in this thesis work, to implement the converter in extreme temperature working situation.

Sizing the circuit is up to the designer (current user) too. The user parameter file contains rows for the minimum length and width of n and p MOS of the

[1] We have called them external just because they do not deal with the converter block itself but they are linked to the secondary ones (ring oscillator and buffer chain).

[2] labels are original from the UMC018 library.

charge pump: they have to be filled in with the sizes of the first two (n and p) switches in order to create, then, both switches equivalent resistance (R_{sw}) and capacitance (C_{sw}) vectors to enable the respective evaluation of the R_{FSL} and the power switching dissipation [3] .

In the user parameter file, it is also required to fill in the value of the MIM capacitors of the charge pump, indicated as C_{MIM0} (MIM ones are preferred for this kind of works because they do not have to be referred to ground and they better avoid electromagnetic interferences).

Other two main constraints are mandatory to be known by the user once the final application environment is given:

- $Iout$, which is the output current we need to extract from the converter to drive the future output load,
- established iVCR = N = $\frac{V_{out}}{V_{in}}$, stating how much we want to boost the input voltage, basing on application specifications.

A typical range for I_{out} is few μA, while N depends on the application and the required output voltage performances.

3.1.3 External Parameters

The so-called file contains the minimum widths of n and p MOS for both the just mentioned contour blocks, with the addition of some special parameters needed for their implementation (such as α, called alpha in the code, ΔV_{tn} and ΔV_{tp} for the buffer chain, or V_A and V_B for the final ring oscillator configuration). An explanation of their roles will be given below.

3.1.4 Global Parameters

It contains a list of the well-known global constants which have been used in the code. The following table shows them all.

$$\begin{array}{ll} k & 1.38065 \cdot 10^{23}\,\mathrm{V\,^{\circ}C\,K^{-1}} \\ q & 1.602 \cdot 10^{-19}\,\mathrm{C} \\ \epsilon_0 & 8.85 \cdot 10^{-12}\,\mathrm{F\,cm^{-1}} \\ \epsilon_{si} & 3.9 \\ n_i & 1.45\,\mathrm{C} \end{array} \tag{3.1}$$

[3] It is important to remember that the sizing of transistors can not exceed the minimum process available length, while it is convenient not to exceed in increasing them too much for area occupation reasons.

3.2 Header

This is the longer and denser file. It contains all the functions needed to estimate performances of the whole design.

Since the user has to decide which one of the available architectures to choose for its design, analysis of several ones is included in this file. The code is able to generate all the main starting parameters and collect them all into a single Python class named "architecture".

3.2.1 Charge Pump

The largest part of the analysis on this block is based on the two switching operation limits. Since they are directly linked to the charge multiplier vectors, those are the first in being calculated once the charge pump architecture to be realized (in terms of VCR and architecture constraints) is known. In few iterations, the two vectors a_c and a_r are created and will be ready to be used for later analysis.

They are involved in the calculation of the output resistance of the charge pump, which is responsible of one of the major contribution of power losses in the whole circuit ($Pdiss_{R_{out}}$).

Before analysing the power contributions in the system, all of the switches resistances of the charge pump are calculated too. Since each MOS is operating in sub-threshold region, its resistance had to be found by

$$R = \frac{1}{\frac{\partial I}{\partial V_{DS}}} \tag{3.2}$$

where I is the sub-threshold current expressed by ([6]), considering for simplicity an nMOS,

$$I = k \cdot 2n \cdot \Phi_T^2 \left\{ \left[\log\left(1 + e^{\frac{V_{GB} - V_t - nV_{SB}}{2n \cdot \Phi_T}}\right)\right]^2 - \left[\log\left(1 + e^{\frac{V_{GB} - V_t - nV_{DB}}{2n \cdot \Phi_T}}\right)\right]^2 \right\} \tag{3.3}$$

with

- n, the idealty factor, equal to 1;
- $V_{SB} = 0$ because each MOS bulk is linked to its source node;
- $V_{DB} = V_{DS}$ is approximatively negligible;
- $V_{GB} = V_{GS} = V_{in}$;
- V_t is the threshold voltage of the MOS;
- k is the form factor of each switch given by $C_{ox} \cdot \mu \cdot w/L$.

So, differentiating the 3.3 with respect to V_{DS}, after some approximation and considering those previous points, we obtain

$$R = \frac{1 + e^{\frac{V_{in}-V_t}{2\cdot\Phi_T}}}{k \cdot \Phi_T \cdot \log\left(1 + e^{\frac{V_{in}-V_t}{2\cdot\Phi_T}}\right) \cdot e^{\frac{V_{in}-V_t}{2\cdot\Phi_T}}}. \tag{3.4}$$

A vector R_{sw} of charge pump equivalent MOS resistors is then created: it has nsw elements, where the even ones are occupated by p MOS and the odd ones by the n MOS.

A similar procedure is followed to create equivalent MOS capacitances vector C_{sw} too.

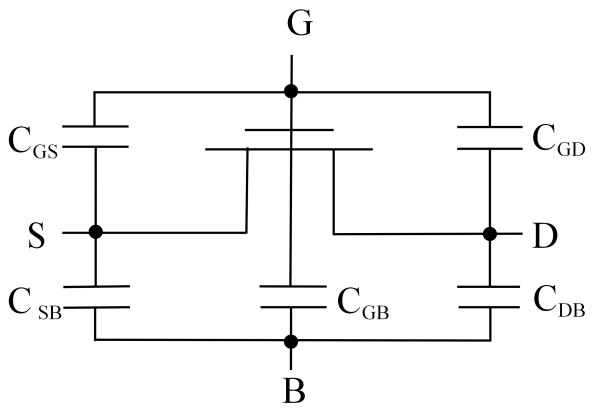

Figure 3.1: Schematic view of MOS parasitic capacitances.

	Cutoff	Triode	Saturation
C_{GB}	$C_{ox}wL$	0	0
C_{GS}	$C_{gd0}w$	$C_{ox}wL/2 + C_{gd0}w$	$2C_{ox}wL/3 + C_{gd0}w$
C_{GD}	$C_{gd0}w$	$C_{ox}wL/2 + C_{gd0}w$	$C_{gd0}w$
C_{SB}	$k(C_{J0}A_S + C_{JSW0}P_S)$	$kj(C_{J0}A_S + C_{JSW0}P_S)$	$k(C_{J0}A_S + C_{JSW0}P_S)$
C_{DB}	$k(C_{J0}A_D + C_{JSW0}P_D)$	$kj(C_{J0}A_D + C_{JSW0}P_D)$	$k(C_{J0}A_D + C_{JSW0}P_D)$

Table 3.1: MOS Parasitic Capacitances Values.

Figure 3.1 shows which are MOS parasitic capacitances and a resume of their general values is given in Table 3.1: C_{JSW0}, C_{J0} and C_{gd0} are taken from the process model parameters file, while A and P are respectively area and semi perimeter of the MOS in account. Each element in C_{sw} vector is then calculated as

$$C_{sw}[i] = C + C_{par} = w[i] \cdot L \cdot C_{ox} + k[i]\big(C_{J0}A_D[i] + C_{JSW0}P_D[i]\big) + C_{gd0}w[i] \tag{3.5}$$

Now we can estimate all of the power losses due to the charge pump.
The PCE of the circuit can be expressed by:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}}$$

where P_{out} is the total power at the output of the converter, P_{in} is the input power amount given by the TEG and P_{loss} is the total power loss in the circuit, which is mainly composed by three contributions:

- charge pump output resistance loss $Pdiss_{R_{out}}$,
- switching power losses (called $Pdiss_{sw}$ in the code) due to the charge pump switch gate and parasitic capacitances,
- losses due to the additional blocks (ring oscillator $Pdiss_{ro}$ and buffer chain $Pdiss_{bc}$).

Starting with the first one, as previously told, the calculation of the two output resistances R_{SSL} in 2.12 and R_{FSL} in 2.3.2 could be easily performed once the charge multipliers are known. The total R_{eq} could be then known and, finally,

$$Pdiss_{R_{out}} = I_{out}^2 \cdot R_{eq} = I_{out}^2 \cdot \sqrt{R_{SSL}^2 + R_{FSL}^2} \tag{3.6}$$

It is considered as a loss because of the fact that, in R_{eq} absence, the total nominal output power of the converter would be $P_{out} = Vout_{nom} \cdot I_{out}$ while it is $P_{out} = V_{out} \cdot I_{out}$, where $V_{out} = Vout_{nom} - I_{out} \cdot R_{eq}$.

The evaluation of switching power losses is performed by a dedicate function too: giving it, as input, the architecture class, after calling $C_\gamma = \sum_i C_{sw}[i]$ with $i \in [0, nsw)$, it returns

$$Pdiss_{sw} = C_\gamma \cdot f_s \cdot V_{in}^2. \tag{3.7}$$

Before estimating the last two loss power contributions, we need to present you their related block behaviours.

3.2.2 Buffer Chain

A buffer chain was needed between the charge pump and the clock frequency generator to let the last one sustain that amount of load.

At the beginning, we have assumed to take into account a standard buffer chain model (illustrated in Figure 3.4). Analysis of this block reveals a cascade of inverters (Figure 3.2), where each inverter behaviour is synthetically summarized, in the following paragraph.

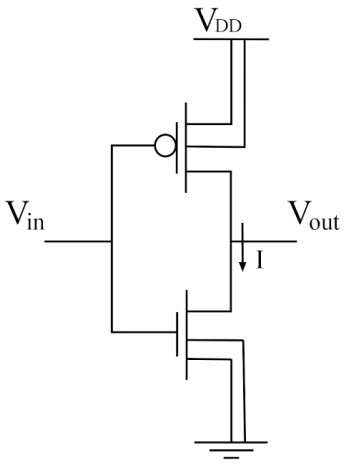

Figure 3.2: Inverter CMOS.

Inverter CMOS As it is well know, the essential behaviour of this block is given by the V_{in} sweep:

- if $V_{in} > V_{tn}$ then the nMOS is ON and pMOS is OFF, so, since no current is flowing through the output[4] , V_{out} become 0;
- if $(V_{in} - V_{DD}) < |Vt_p|$ then the situation is symmetric and V_{out} will be equal to V_{DD}.

Dynamically looking at the inverter behaviour, we could assume a single output capacitance $C_{L_{inv}}$ which includes all the output parasitic and load contributions. The simplest case would be having another inverter as output (Figure 3.3) and it would also be the better one. Assuming as input a clock wave, the calculation of C_L is simply done by the sum of:

- $C_{GS} + C_{GB}$, which have no influence since input varies instantaneously;
- C_{DB}: diffusion capacitances;
- C_W, which could be neglected since it is associated with metal interconnections between two inverters;
- C_{G2}: it summarizes gate/bulk, gate/drain, gate/source contributes but it can be approximated with the simple oxide capacitance ($C_{ox}wL$);
- the sum of the two C_{GD} which mainly stand for the overlap ones since both MOS are most of the time in saturation or cut-off region. Those are the

[4]the load at V_{out} will be a similar structure, luckily another inverter, so to show an input gate capacitance which statically can be seen as an open branch.

only one not referred to ground: Miller effect has to be considered at this point, and it will yield equivalent capacitances equal to two times $C_{OV} \cdot w$.

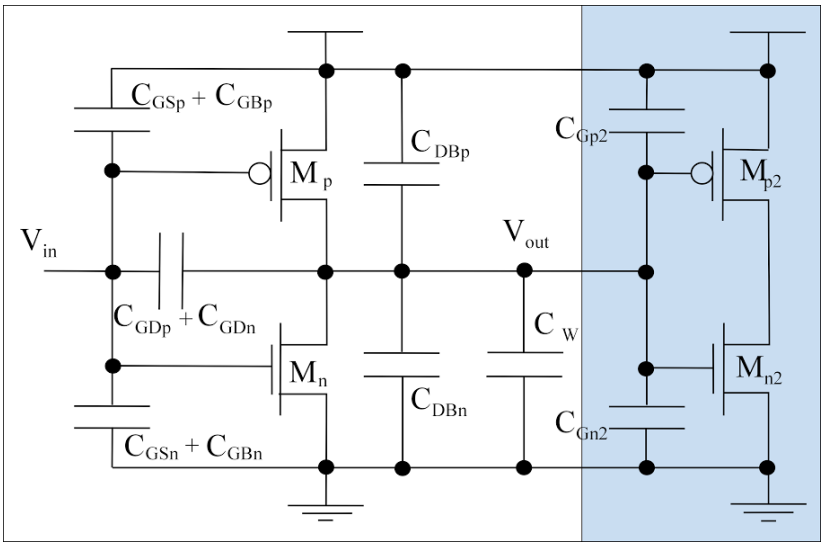

Figure 3.3: Inverter CMOS load and parasitic capacitances.

An approximation of the propagation delay (τ_p) caused by a single inverter could be estimated considering that the system follows an RC model: V_{out} goes from V_{DD} to 0 exponentially within the same time that a first order system would took to reach 50% of the dynamic ($V_{out}(\tau_{phl}) = \frac{V_{dd}}{2}$).

Given I_{Dsat} as the charging current of the load capacitance the propagation time of the transition high-to-low can be calculated by

$$\tau_{phl} \cong \frac{CV_{dd}}{2 \cdot I_{Dsat}}.$$

An average of the two time delays could be considered for estimating the total inverter propagation one $\tau_p = \frac{\tau_{phl}+\tau_{plh}}{2}$.

Power dissipation caused by a single stage inverter had to be now considered as the sum of three contributions:

- static power, about zero and not taken into account for our purposes;
- C_L dynamic power, due to the fact that for input commutations analogue output ones should charge and discharge the output capacitive load;
- short currents dynamic power, which is dissipated when conductive paths between ground and supply exist.

The second mentioned is the main one: during each LH commutation the output capacitor is charged taking energy from the supply:

$$E_{Vdd} = \int_0^\infty V_{Vdd} \cdot I_{Vdd}(t)dt = \int_0^\infty \frac{V^2}{R} e^{-\frac{t}{RC}} dt = CV^2.$$

Half of that one is dissipated in the pMOS (which turns on in saturation region while nMOS is ideally instantaneously turned off) and, thanks to its current $Ip_D = i_{Vdd}(t) = C_L \frac{dV_{out}(t)}{dt}$, C_L is charged at V_{DD} so that

$$E_{C_L} = C_L \int_0^\infty V_{out} dV_{out} = \frac{C_L V_{DD}^2}{2}.$$

During HL phase, supply is not providing energy and C_L is discharged by the nMOS. Total energy losses in a period is given by the sum of n and p MOS loss contributions. It is not related with their equivalent resistances/sizes anyway and the total amount of power dissipation is given by its definition:

$$P_{dyn} = C_L \cdot V_{DD}^2/(2T) = C_L \cdot V_{DD}^2 \cdot f_s/2. \tag{3.8}$$

Design of a buffer of M inverters First of all, some hypothesis are needed to start:

- every i MOS of each inverter in the chain has an $L_{p_i} = L_{n_i} = L_{min}$ so we only have to deal with widths sizing,
- a geometric reason α [5], called *alpha* in the script, is the ratio between widths of cascaded stages : $w_p^{i+1} = \alpha \cdot w_p^i$,
- all of the reactive elements for each inverter i can be represented by a unique load capacitance C_L^i between output node and ground that is made by the gate capacitances of the following stage ($C_L^i = L_{min} C_{ox} \big(w_n^{i+1} + w_p^{i+1}\big)$) increased with all the previously mentioned parasitic ones needed for accuracy,
- input wave has vertical/ideal slopes and we want them to remain at least symmetrical when they reach the chain output node accepting as good $\tau_{plh} = \tau_{phl} \leq 1/8 f_s$,
- a first order model of the i-MOS can be valid, so the rising and falling propagation delays for each buffer are

$$\begin{aligned} \tau_{plh}^i &= \frac{C_L^i}{k_p^i} \frac{1}{-V_{dd} - V_{tp}^i} \Big(\frac{V_{tp}^i}{-V_{dd} - V_{tp}^i} + \gamma \Big) \cong \frac{C_L^i}{k_p^i} \frac{V_{tp}^i}{(-V_{dd} - V_{tp}^i)^2} \\ \tau_{phl}^i &= \frac{C_L^i}{k_n^i} \frac{1}{V_{dd} - V_{tn}^i} \Big(\frac{V_{tn}^i}{V_{dd} - V_{tn}^i} + \gamma \Big) \cong \frac{C_L^i}{k_n^i} \frac{V_{tn}^i}{(V_{dd} - V_{tn}^i)^2}. \end{aligned} \tag{3.9}$$

A procedure to know how many stages of the buffer are needed has been demonstrated considering what has to be known at this analysis point. We need to be given by operating frequency (to find τ_p), charge pump characteristics

[5] optimum α design has been found to reach the minimum dissipation of power, given for $\alpha = 2.7 \cong 3$.

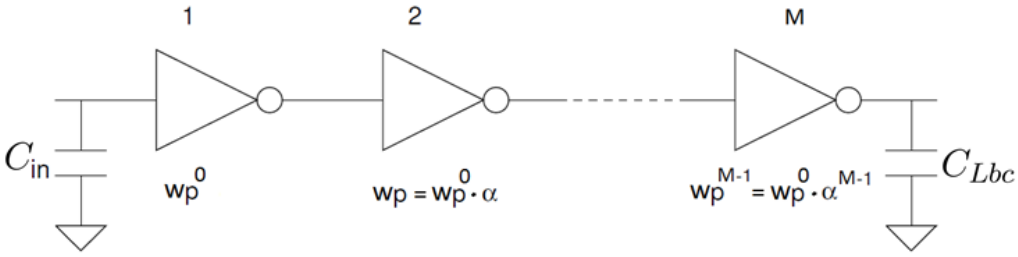

Figure 3.4: Schematic Buffer Chain.

(architecture parameters as N and C_{sw}, to evaluate the final buffer chain load $C_{Lbc} = \sum_{i=0}^{nsw} C_{sw}[i]$) and input buffer sizes (dimensions of the first inverter which give $C_{in} = C_{ox} \cdot L \cdot w_p^0(1+u)$, where w_p^0 is usually equal to the clock generator one and $u \triangleq \frac{w_n^i}{w_p^i}$.

Because of the fact that

$$w_p^0 = w_p^1 \cdot \alpha^{-1} = w_p^2 \cdot \alpha^{-2} = \cdots = w_p^{M-1} \cdot \alpha^{1-M}$$

and, consequently,

$$C^0 = C^1 \cdot \alpha^{-1} = C^2 \cdot \alpha^{-2} = \cdots = C^{M-1} \cdot \alpha^{1-M}$$

we can imagine an equivalent output $C_{Lbc} = L \cdot C_{ox} \cdot w_p^M$. Extrapolating w_p^M from adjusting the first of 3.9 for an $i = M$, we can find the best w_p^{M-1} to be $w_p^M \cdot alpha^{-1}$ and so having the value of C^{M-1} to be able to finally find the searched M by

$$\alpha^{M-1} = \frac{C^{M-1}}{C^0} \rightarrow M = \frac{\log\left[\frac{C^{M-1}}{C^0}\right]}{\log(\alpha)} + 1 \tag{3.10}$$

Everything is now available to establish the power loss in this block. Referring to what has been previously analysed in 3.8 about inverters power losses, and considering the existence of C_{Lbc} one too,

$$\begin{aligned} Pdiss_{bc} &= \sum_i \left[\frac{f_s \cdot V_{dd}^2 \cdot C^i}{2}\right] + \frac{C_{Lbc} \cdot V_{DD}^2 \cdot f_s}{2} = \\ &= \frac{C^{M-1} \cdot V_{DD}^2 \cdot f_s}{2} \cdot \sum_i \frac{1}{alpha^{M-1-i}}, \end{aligned} \tag{3.11}$$

with $i \in [0; M)$.

3.2.3 Ring Oscillator

The ring oscillator is only one of the various way in which one can obtain an on-chip local oscillator.

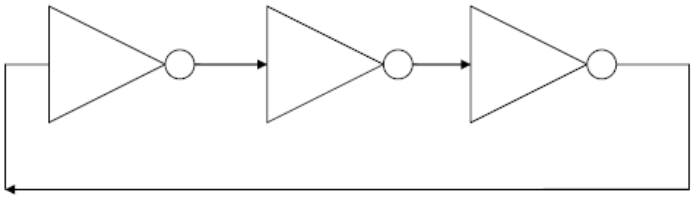

Figure 3.5: 3 stage ring oscillator schematic.

It is an a-stable circuit made by an odd number of inverters in a ring (Figure 3.5). No stable operating zone exists and the circuit, after an initial slow start-up, is oscillating with a period of

$$T_{ro} = 2 \cdot \tau_{ro} \cdot N_{ro} \tag{3.12}$$

where with N_{ro} we indicate the ring elements number while

$$\tau_{ro} = (\tau_{plh} + \tau_{phl})/2 \tag{3.13}$$

is a single cell propagation delay, made by n and p MOS transistors ones. To establish a desired oscillation period, and, consequently, the frequency of the whole system clock $f_s = 1/T_{ro}$, we could deal with both N_{ro} and τ_{ro}.

Once width of each inverter has been established by filling the associated row in the *external_parameters.txt* and the operation frequency is chosen for the given application, a unique $N_{ro} = \frac{1}{2 \cdot f_s \cdot \tau_{ro}}$ which satisfied our purposes exists.

Our analysis started with a simple ring oscillator standard configuration made by a chain of an odd number of identical inverters. Since inverters in the ring are all the same, the load of each stage consist on the following equivalent capacitance C_{Lro} (just explained before).

According to that, the power dissipation due to the ring oscillator is given by

$$Pdiss_{ro} = N_{ro} \cdot \left[\frac{f_s \cdot V_{dd}^2 \cdot C_{Lro}}{2}\right]. \tag{3.14}$$

Current Starved Ring Oscillator It is realized simply adding devices able to control the speed of the previous simple stage inverter by controlling the charging/discharging currents. Both Ma and Mb in Figure 3.6 could act as voltage controlled (respectively Va and Vb ones) current sources: in h $\rightarrow$ l transition and vice-versa the output charge flux control would guarantee a different propagation timing. Since both Ma and Mb act in saturation region, there is a direct quadratic relation between the control voltages and their respective currents (and so τ_{ro}).

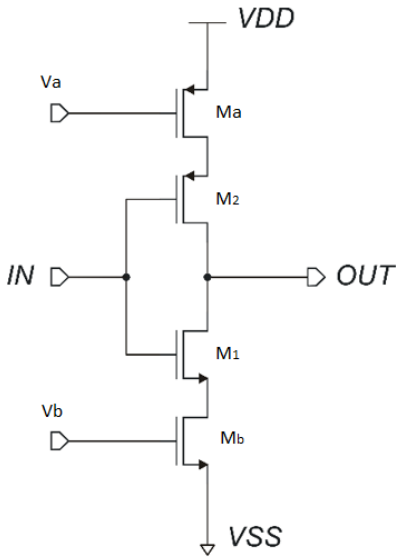

Figure 3.6: Current starved ring oscillator inverter.

3.3 Main file and design exploration contour functions

This file is simply built to interact with the user. First of all, it is responsible for asking which architecture the user wants to choose for the design, and it stores the answer to associate it to the name of the whole class "Architecture" which will be created.

It contains a sequence of commands to prepare the needed parameters and values for design exploration and analysis. At the end we will be told about the PCE, the distribution of power losses as well as area occupation, and there will be several available files and graphs, based on the contour functions we have decided to run at compiling time.

By those last ones, new files will be saved on Desktop and they will contain a list of the most important informations dealing with PCE: it is up to the user which ones have to be taken into account for plotting/analysing, basing on its purposes (with the exception of some of them which return graphs without needing any other user's action).

At this last point it is important to stress that Python code has been implemented both for prior analysis and design exploration and for post design verification.

A very basilar example of how it could be used follows here, but, for more curated and important ones you should refer to the end of Chapter 4.

If our goal is to understand how the system behaves with linearly varying the TEG input voltage V_{in} from a starting point (sp, by default equal to 0.1 V) to an

ending one (ep, by default equal to 0.3 V), having a resolution of nop (number of points, by default equal to 50) per interval $[ep - sp]$, after having run the *main.py* file for a Dickson charge pump, with typing $V_{in}\_sweep(arch, sp, ep, nop)$, Figure 3.7 will appear on the screen. Based on previous analysis we should just have an idea of those final results.

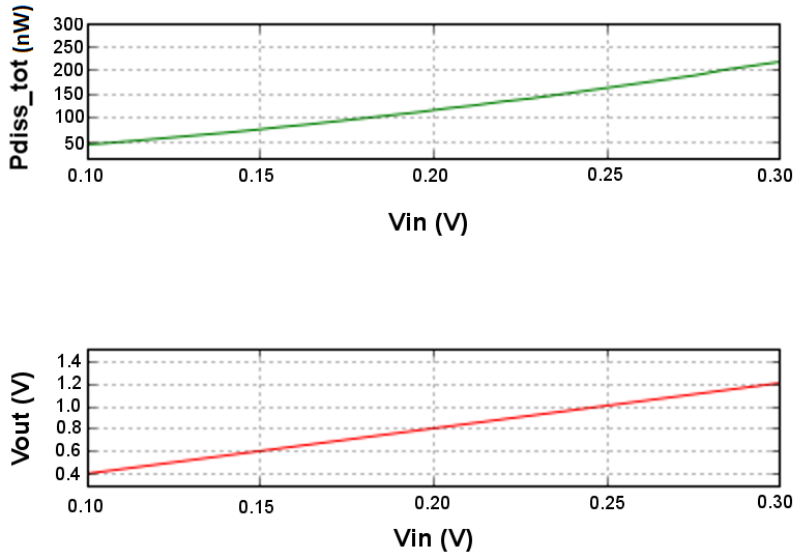

Figure 3.7: An example of what happens with a Vin sweep

We were just aware of the dependence of V_{out} and P_{diss_tot} on V_{in}. The first one is a linear function with the N factor while the second one is a kind of a quadratic one since it encompasses the sum of all the previously calculated P_{diss} : buffer chain, ring oscillator and charge pump one.

We hope that it is more understandable now how this tool could be very useful to have a design space exploration of the performances and behaviours of our system with respect to main parameter variations [6].

3.4 MATLAB Code from Seeman

The Matlab code from [1] gave us the starting idea: after having critically understand its structure we though an upgrade was necessary for our needs.

The MATLAB based script can automate some design methodologies to enable rapid evaluation of SC topologies. These design methodologies are supposed to enable the optimal design of SC converters for many application, from sensor nodes to microprocessors and more. The Seeman automation is focused on:

[6] NB: no any analysis could be performed at all: we have chosen the major important ones for our evaluation.

- choosing the correct topology and finding its charge multipliers with matching components basing on device technologies,
- best sizing of switches and capacitors according to the current requests,
- area, frequency and capacitor area choosing to optimize performances.

Of course it would speed up the design process, giving also several computer-based visualization, but it could not be adopted for our kind of study since

- it has been tested only for step down converters and we need to deal with a step up one;
- it starts from some hypothesis and assumes several things which do not suite well with our work and we will explain you why.

3.4.1 Structure

Seeman's Matlab package encompasses with some functions to specify the idealized topology structure, assign and size devices for each component and evaluate the loss of the converter at a certain operating point.

The *techlib.m* file for technology process choices is given within many parameters of several available design processes such as International Technology Roadmap of Semiconductor (ITRS) 32 and 65 both for oxide capacitors and switches; other parameters dealing with frequency, VCR, and other constraints are known only at compiling time when specific functions are called.

The two files *implement_topology.m* and *generate_topology.m* let the user choose the topology, VCR, technology available structures for switches and capacitances and if area or loss metric is preferred. Thanks to them an ideal sizing of switches and capacitors which will compose the final circuit is made, based on two metrics (M_{SSL} and M_{FSL}, fully explained in the PhD thesis). You can also create a particular topology thanks to the *permute_topology.m* function, which simply cascades more topologies to create a miscellaneous one.

Previous functions are the backbone of the *evaluate_loss.m*: the user is able to state the input voltage, frequency or output voltage [7], output current and available area for switches and capacitors of its final desired circuit. The code will return the main losses in the charge pump and several analysis can be performed.

Two more functions are included in the package: they use the previous ones to create plots which aid in the development of the SC converter.

- *plot_opt_contour.m* plots a PCE contour plot over a two-dimensional space of switching frequency and switch area for a given input voltage and output current,

[7] Seeman code is able to state for you the frequency to run at in case you want a specific output voltage or, if you fix an operative frequency, the corresponding output you will obtain

- *plot_regulation.m* plots the PCE of one or more SC converter topologies as either the input or output voltage is swept across a range while the other is held constant; regulation is performed by varying switching frequency.

Function *optimize_loss.m* is used by the two previous ones for finding the most-efficient operating point for a given input voltage and output current.

3.4.2 Codes comparison

As it is clear, Matlab code from Seeman thesis have been accurately studied before implementing our Python one. Several trials have been done to understand its behaviour and results and, once we have implemented our one and reached similar results, a careful comparison followed to check if they could be exchanged.

What came out was that, of course, Matlab package is really performing for charge pumps analysis in terms of area occupation and power losses imputable to the output equivalent resistance and some other parasitic ones, but, for our kind of work, we need a more complete one: contributions of clock generator and drivers can not be disregarded in power loss analysis if we want to have an idea of the PCE in those kind of IC (meaning their realization at all, not only switched capacitor converter block). Seeman script lacks, in fact, of other important power contributions which does not deal with output resistance and equivalent capacitance of the switches: especially for applications such as harvesting ones the power loss contributions of the clock generator and the buffer chain can equal the charge pump ones, so they need to be computed.

What is more, Matlab package starts with assuming some hypothesis which restrict a lot the design space: for instance the user has not the freedom in making any technology variations (i.e. threshold voltage or mobility of p and n MOS) to better fit its needs, as well as it is not possible to vary the sizing of switches and capacitors in the charge pump once they have been fixed from the script in order to reach the best PCE.

Another important difference between the two codes is that no very low voltages are considered to be at the inputs of the SC DC-DC: MOS sub-threshold region is not taken at all in to account, while, for low voltage applications, it is mandatory to be implemented, or the script is not properly working.

This is may due to the fact that Seeman's model has been implemented to be dedicated to step-down converter analysis, .

Chapter 4

Feasibility Study

Our whole analysis included in the code needs now to be validated with simulation results. It is mandatory to verify that our study on the system has been properly focused and that what we obtained from the Python script can be compared with what we actually get from the simulator.

For this procedure, we have made a strong use of the Cadence Virtuoso design tool with Spectre simulator using the UMC018 CMOS technology library available at the Dipartimento di Ingegneria Dell' Informazione of the University of Pisa.

In this chapter we will present the feasibility study of each block of our design with particular attention on eventual modifications and upgrades needed on the code to better estimate design circuits performances and behaviours.

Particular schematic blocks have been examined:

- a three stages Chen architecture for the charge pump (the same as the one shown in 2.10);
- a single inverter and then a chain of them (in two different Bulk configurations);
- a five stage ring oscillator, simple and current starved one.

Finally, some design space explorations using this tool are performed.

4.1 Charge Pump

Charge pump is of course the crucial block because, unfortunately, little information is available on its realizations for such low power and low voltage applications. The Chapter 3 analysis may be re-visited based on what comes out from Cadence simulations.

The simple three stage Chen architecture is shown in its Virtuoso schematic view editor in 4.1. First of all, the correctness of its open loop behaviour with

$V_{dd} = 0.2\,\mathrm{V}$ and an ideal clock wave (clk) from 0 to V_{dd} at 4 MHz has been checked out.

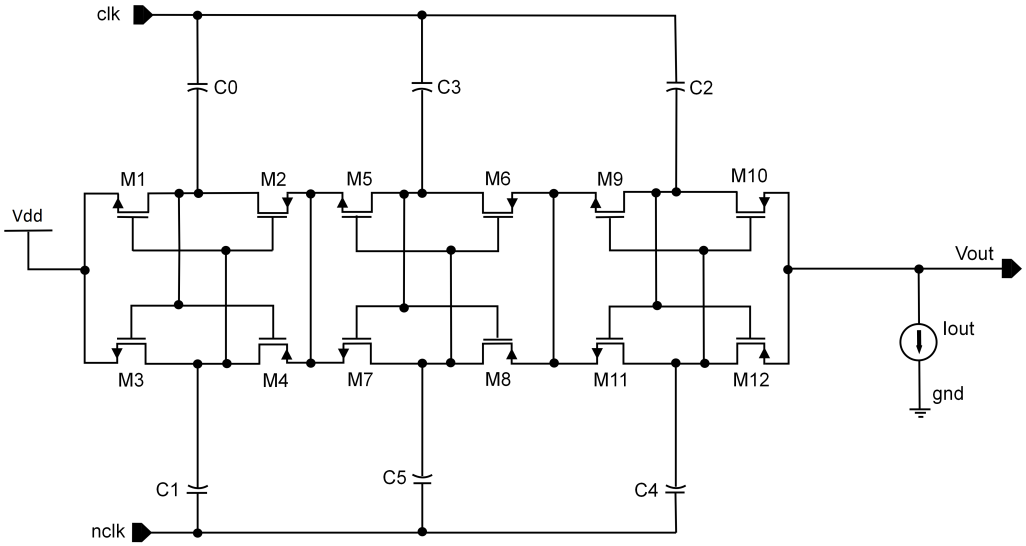

Figure 4.1: Three stages Chen DC-DC schematic view.

In order to do that, we needed to align the files of the Python script parameters with the simulation ones. We have looked for the process parameters available on the software libraries to find the so-called needed ones for the related *process_parameters.txt* file.

All the lengths in the circuit have then been sized as the minimum ones. About the widths, several trials have been done with the Python code before building up the simulation in order to obtain future reasonable results on it. Thanks to the initial analytical study helped by the script, we were able to briefly know the amount of the output equivalent resistance of the three stage charge pump and so establish which kind of widths and constraints (i.e. output current and frequency) needed to be used in Cadence simulation to obtain certain results.

Finding the nominal output voltage (what has been previously called $Vout_{nom} = V_{dd} \cdot (1 + k)$) was easy and the simulation in Figure 4.2 confirms the expected open loop behaviour of the charge pump ($Vout_{nom} = 0.2 \cdot (1+3) = 0.8$ V).

What happens with a certain output current requested to the charge pump is shown after enabling at $t^* = 15$ ms a current source ($I_0 = 10$ nA shown in 4.1) connected between node V_{out} and ground.

With a few calculations (see red squared numerical quantities shown in Figure 4.3) the output resistance of the charge pump simulated by Cadence is directly known:

$$R_{out} = \frac{\Delta V_{out}}{I_{out}} = \frac{113.2\mathrm{mV}}{10\mathrm{nA}} = 11.32\mathrm{M}\Omega$$

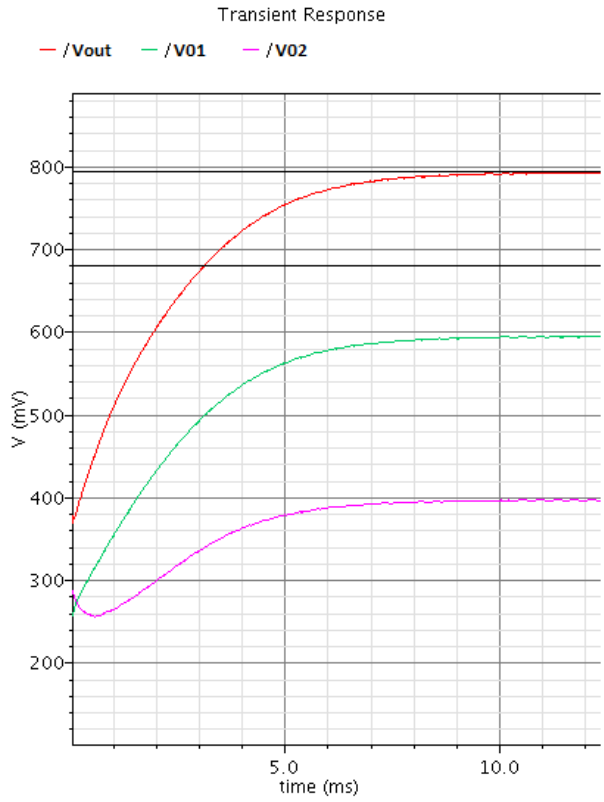

Figure 4.2: Transient simulation of the open loop three stages charge pump.

According to the Python code, it was initially around 42.5 MΩ [1] .

This result was not as good as desired. The charge pump is the main block and we wanted its model to be as precise and curated as possible.

Since the way to calculate charge multipliers and both R_{fsl} and R_{ssl} is correct, some problems should have occurred in the equivalent resistances (R_j) and capacitances (C_j) model of the switches. Taking into account the first ones, this error could be imputable to some parameters, as the mobility, which are included in the impedance calculus:

$$R_j = \frac{1 + e^{\frac{V_{in} - Vtj}{2 \cdot \Phi_T}}}{kj \cdot \Phi_T \cdot \log\left(1 + e^{\frac{V_{in} - Vtj}{2 \cdot \Phi_T}}\right) \cdot e^{\frac{V_{in} - Vtj}{2 \cdot \Phi_T}}}.$$

The model library of UMC018 gives us general parameters and we took that ones to be included in the *process_parameters.txt*:

- μ_j: mobility of holes and electrons

[1] calculated as the square root of $R_{fsl} + R_{ssl} = \sum_i \frac{R_i (a_{r,i}^2)}{D_i} + \sum_i \frac{(a_{c,i})^2}{C_i f_s}$.

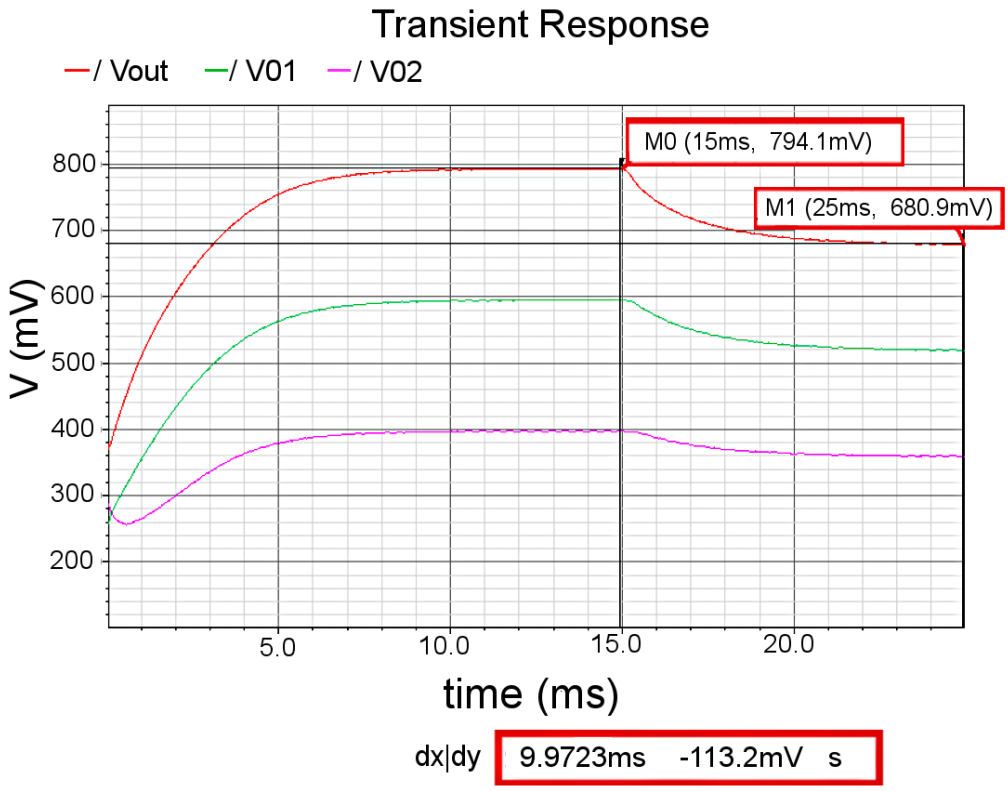

Figure 4.3: Transient simulation of the three stages charge pump with an output current of 10 nA turned on at $t = 15$ms.

- Vt_j: voltage threshold of p and n MOS
- n : ideal factor

According to them, the equivalent resistance could change a lot and an accurate fitting has been performed analysing a single n and p MOS on its own. Sweep simulations to find the two transfer characteristics have been run simply connecting each MOS in a similar voltage configuration as the charge pump one.

After having extracted the tabular values of the curves from Cadence as *.csv* files and re-plotted them on QT-Grace software, we started a curve fitting plotting our modelled trans-characteristics (see Equation 3.3) and changed the previous three "crucial" parameters in order to obtain the superposition with the Cadence one.

Figure 4.4 contains a sequence example of the realized steps. Adjusting then those parameters on the related file, a second trial has been performed in order to improve the results.

The Python code returns now an output resistance of 10.1 MΩ and a deeper analysis of the results is reported in the Table 4.1.

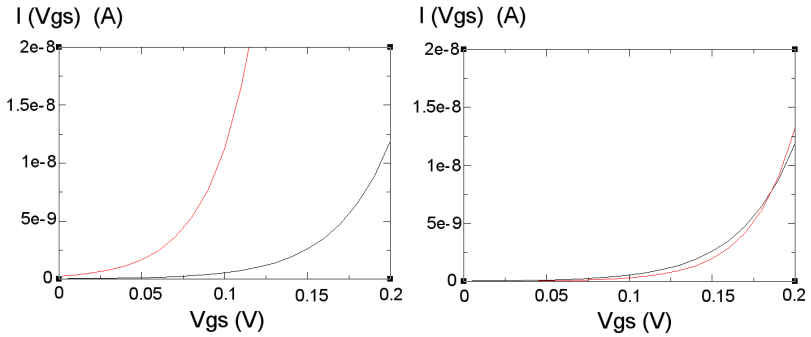

Figure 4.4: QT-Grace transcatacteristic: pre (on the left) and post (on the right) fitting. Red curves show the analytical results while the black ones are Cadence results.

	Rn (Ω)	Rp (Ω)	R_{FSL} (Ω)	R_{SSL} (Ω)
Circuit	6 M	0.2 M	11.30 M	7.5 K
Model	5.4 M	0.3 M	9.98 M	7.5 K

Table 4.1: Charge pump equivalent resistance results comparison.

This could just be an acceptable starting point to state that a good model has been created to simulate the charge pump switches behaviour; expected results come out to be definitely better than previous ones having a look at each output resistance contribution.

Dealing with switch equivalent capacitances, it is important to note here that, since first results of Python equivalent capacitances would not be that acceptable (and, consequently, a bad estimation of the power losses due to them would be incorrect) even with the modification on the model parameters, a calculation of all the parasitic capacitance for the switches has been included in the 3.5 in order to be as much accurate as possible.

For the comparison with what comes out from the simulator, then, we have calculated the equivalent capacitances of charge pump MOS observing the transient simulation results of a single charge pump MOS. By measuring

$$C_j = \frac{I_j}{dV_j/dt},$$

a verification of what turned out with Python code can follow directly by practical results in Table 4.2.

The feasibility study could now be continued.

The power loss contribution of the charge pump fits well what comes out from the simulator both regarding switching loss (according to 3.7: $Pdiss_{sw} = 0.6{\cdot}10^{-7}$ W) and output resistance (according to 3.6, with an output current of I_{out} =10 nA : $Pdiss_{Rout} = 5\mu$W).

	C_n (F)	C_p (F)
Circuit	4e-14	2e-13
Model	3e-14	3e-13

Table 4.2: Charge pump capacitance results comparison.

Having a good model for our charge pump, the buffer chain has to be sized in order to let the clock wave sustain its heavy load calculated as $C_{Lbc} = \sum_{nsw} C_{sw}[i] \cong$ 1.28 pF.

4.2 Buffer Chain

This block analysis, according to what has been presented in Chapter 3, has to start with the study of a single inverter (schematic view on the left of Figure 4.5).

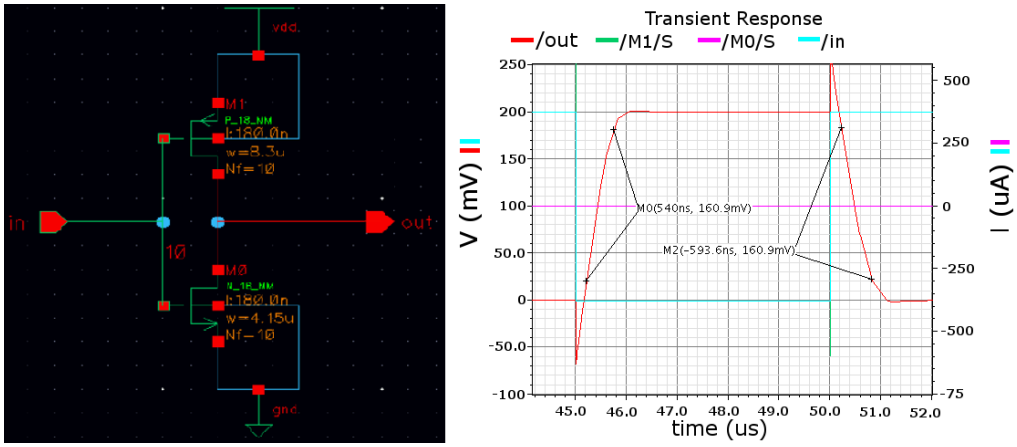

Figure 4.5: Single standard inverter schematic and transient simulation.

Its feasibility study is pretty simple. After having aligned Cadence transistor sizes with the *external_parameters.txt* file ones and having stated a 0.5 duty cycle input clock wave with a period of $T = \frac{1}{f_s} = 10$us, comparison measurements on MOS delay times coming out both from model and circuit simulations (see Figure 4.5) are resumed in Table 4.3.

	$\tau_n = \tau_{hl}$ (μs)	$\tau_p = \tau_{lh}$ (μs)
Circuit	593	540
Model	582	524

Table 4.3: Single standard inverter results comparison.

Inverter performance improvements Thanks to the Cadence simulations, connecting together bulks and gates of each inverter MOS turned out to be a good choice in terms of output waves performances and speed (rising and falling times) as well as power losses, since the whole behaviour of the buffer chain can be improved. This new configuration is also called DTMOS and takes advantages of the Body effect: the threshold voltage of a MOS depends on the fourth MOS terminal and a huge time loss is due to the charging of the parasitic inner capacitances. We have decided to improve our Python code in order to let the user use the standard buffer chain configuration or this last one as the preferred one for its design. The main change between the two architectures has been modelled with a variation of the threshold voltage of the two inverter MOS.

We have inserted in the *external_parameters.txt* file two dedicated rows for instantiating ΔVt_n and ΔVt_p for the new calculations of the output parameters and power losses.

The study on those two has been specific for the current technology (UMC018) and it has to be repeated every changes of it, in order to maintain the correctness and reliability of Python results. It has been not as detailed as the previous one done for the charge pump MOS V_t and μ but by simply sweeping V_t values and putting attention on the various τ until they were about to be equal to the Cadence simulation ones.

Comparing those results with the previous ones in 4.3 should give the reader the idea of the improved performance as we were expecting: rising and falling times are about 4/5 times lower than before.

We can state now that the model of the inverter is correct enough to see if the buffer chain system modelling performs as well. Its feasibility study can go on by imposing (in simulation) the same amount of load as the charge pump one (C_{Lbc}, calculated at the end of previous section).

According to the current frequency of $f_s = 0.1$ MHz, the C_{Lbc} would represent an impedance equal to $Z_{Lbc} = \frac{1}{j \cdot w \cdot C_{Lbc}} = 1.24$ MΩ ($w = 2\pi f_s$).

From the Python code results, having as first inverter the same one as the last simulations, we should need a number of inverters equal to $M = 5$ to drive correctly the charge pump. We have instantiated a simulation on Cadence with a five stage buffer chain and an input clock at 0.1 MHz with a dynamic of 0.2 V to see if it could work with a load equal to the charge pump one: you can see the results in Figure 4.6 and Figure 4.7 and we can say that the feasibility study is satisfactory.

4.3 Ring Oscillator

Once the buffer chain analysis has been done it can be easily followed by the test of the last block of our IC in terms of comparison between code analysis and simulation results.

Leaving the inverter CMOS configuration where Gate is shorted with Bulk, we

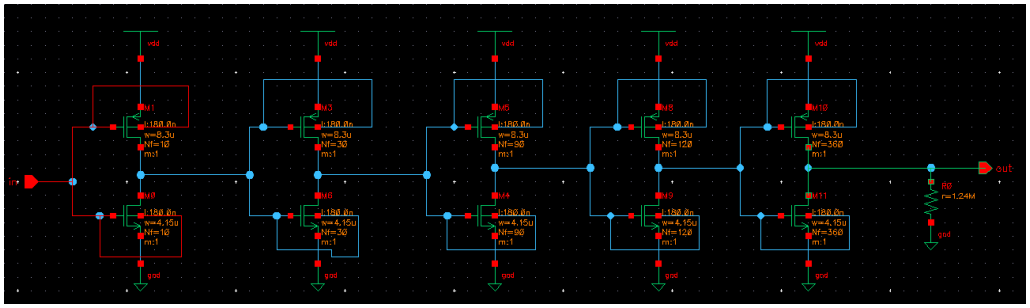

Figure 4.6: Schematic view of a 5 stages buffer chain and a load equal to the charge pump one.

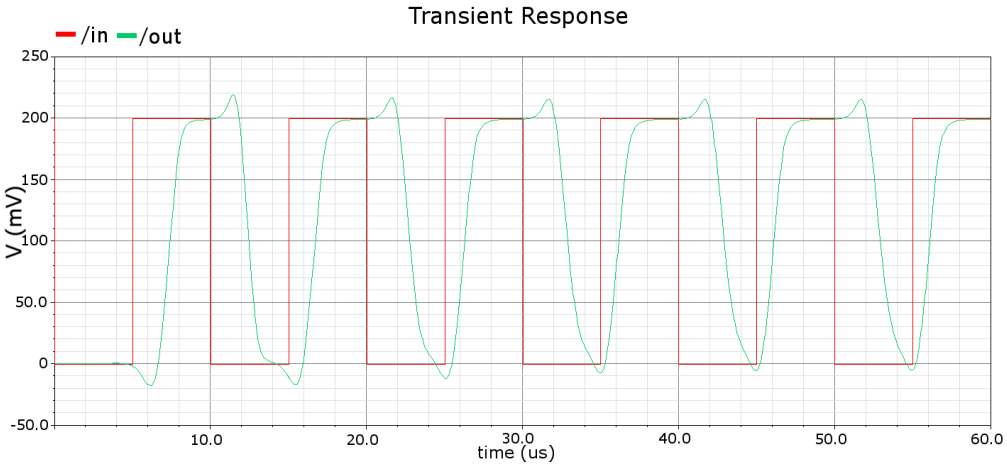

Figure 4.7: Input and output waves of a 5 stages buffer chain and a load equal to the charge pump one.

started from the design of a standard $N_{ro} = 5$ stages ring oscillator (its schematic view is shown in Figure 4.8)

The system will oscillate with a precise period/frequency which depends on MOS sizing and voltage supply. The transient simulation showed below (Figure 4.9) gave us, with a V_{dd} of 0.2 V, an approximate square wave of a period $T = 13.96\,\mu s$ (so we can state each single inverter stadium has an average delay time, measured directly on the curves or calculating by the formula $\tau_{ro} = \frac{T}{2 \cdot N_{ro}}$, of 1.39 µs).

As previously described, τ on Python code is calculated as $\frac{C_{Lro} V_{dd}}{x I_{sat}}$ where:

- I_{sat} is the saturation current in sub threshold region of p and n MOS (known from the Python code once the system is sized, which has to be compared with the simulation output);
- C_{Lro} is the total capacitive load of each inverter (the same contributions of the just calculated buffer chain ones);

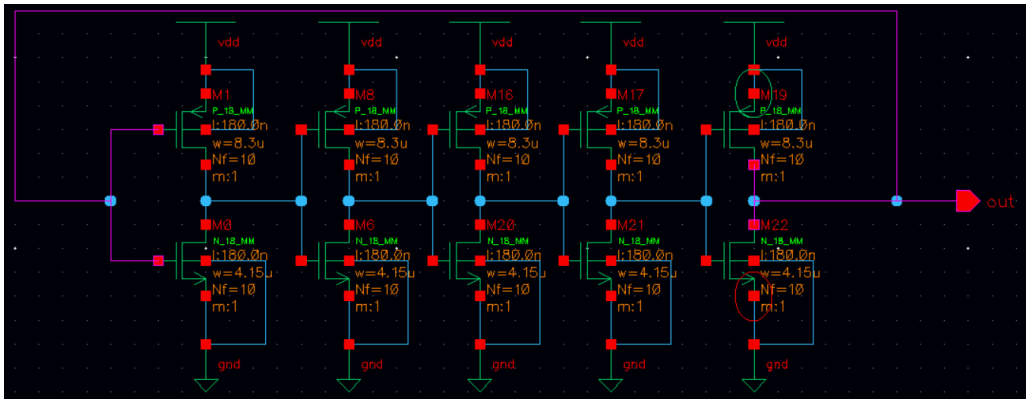

Figure 4.8: Five states ring oscillator schematic view.

- x is a correction parameter which depends on the technology process (usually it is around 2 and, having now stated the other needed parameters for the τ calculation , we could include the best x value in the Python script, after having done a sweep on it to fit the best we could with Cadence τ_{ro}: we will consider $x = 1.9$).

The first line of Table 4.4 shows what we obtained from the transient simulations for each ring stadium [2].

	T (μs)	τ_{ro} (μs)	$\overline{I_{sat}}$ (nA)	C_{Lro} (pF)
Circuit	13.96	1.31	37.75	0.401
Model	13.35	1.33	33.72	0.399

Table 4.4: Ring oscillator results comparison.

Simulations showed an Ip_{sat} (in the middle of its peak) of 39.38 nA and an In_{sat} of 36.12 nA respectively in p and n MOS. Since during the two transitions low-high and high-low in a Δt of 1 µs the voltage drop is about 132 mV we can estimate a $C_{Lro} = \frac{\overline{I_{sat}}}{\Delta V/\Delta t} = 0.401$ pF

[2] $\overline{I_{sat}}$ is the arithmetic average of Ip_{sat} and In_{sat}.

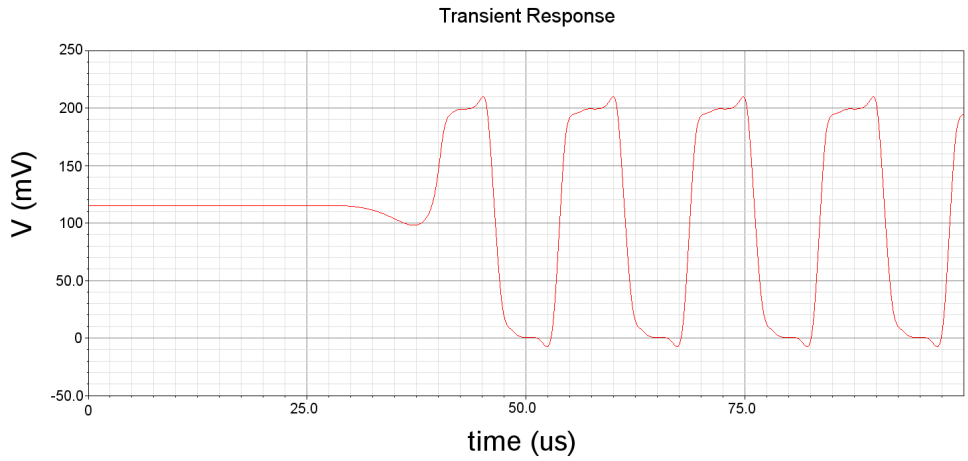

Figure 4.9: Ring oscillator MOS transient simulation.

Our script can be used to model any kind of ring oscillator with this basilar architecture. In fact, dealing with power dissipation, the most important contribution (as it has just been shown with 3.14) is given by the dynamic power, which only depends on the values of C_{Lro} and V_{dd}.

We have explained in the previous chapter how current starved architecture for those kind of applications, where speed and control are very important, is preferred to the simple one. The final Python script contains parameters and functions for a design of this last architecture, and a feasibility study needs to be performed as well in order to validate its correctness.

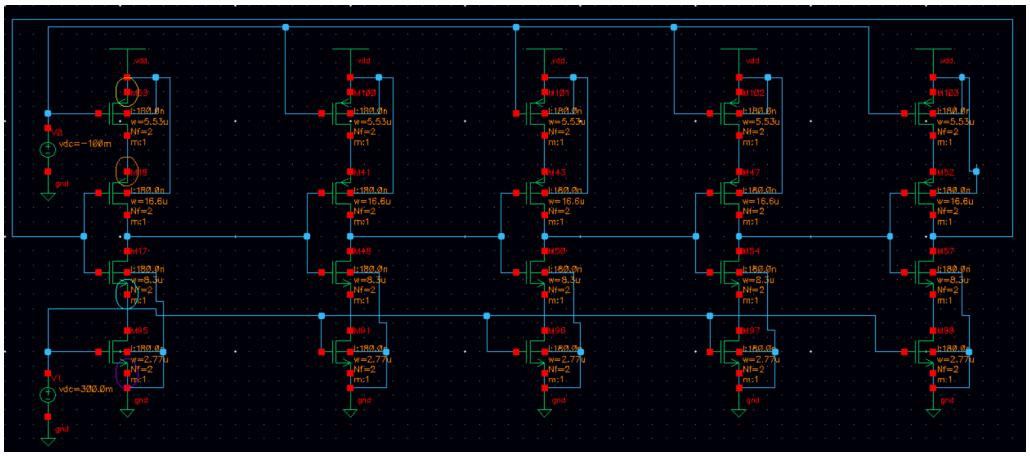

Figure 4.10: Current starved ring oscillator schematic view.

The real optimization in using this kind of architecture, even if it could be not be appreciated because of the addition of two MOS per inverter stage and

an increase of area occupation, is given by the possibility to considerably reduce each MOS width obtaining the same output frequency. In fact output charging/discharging current is imposed by M_A and M_B because of their reduced w sizes which, also by tuning V_A and V_B, decide the driving currents and state the oscillation period.

Considering the saturation region of M_A and M_B gives

$$\begin{aligned} I_A &= k_A V_T^2 \big[ln(1 + e^{\frac{V_A - V_{dd} - V_{t_A}}{2V_T}}) \big]^2, \\ I_B &= k_B V_T^2 \big[ln(1 + e^{\frac{V_B - V_{t_B}}{2V_T}}) \big]^2; \end{aligned} \tag{4.1}$$

the current for each ring oscillator inverter stage is approximately equal to an average of those two.

Initially, no C_{Lro} variation has been taken into account since we thought it was good enough to assume the load of each stage inverter remains almost constant despite the devices addition. In fact the major contribution to each stage load capacitance should remain the initial M_1 and M_2 while M_A and M_B should not count much.

Simulations on Cadence showed us how this hypothesis was not so solid and we should analyse better the contributions to the load capacitance given by the added MOS.

In Figure 4.11 there is shown a first model for the C_{Lro} in which M_A and M_B drain-source capacitances could be considered in this way:

$$C_{Lro} = C_{gd_{ro}} + (C_{gs_{ro}} || C_{ds_x}) \tag{4.2}$$

This formula is linked with what happens to the inner current of each inverter. The more it is imposed by M_1 and M_2, the more their C_{gs} are going to prevail on the C_{ds_x}, and vice-versa. Unfortunately, having a look at the simulation results on Cadence, both C_{ds_x} were not the missed contribution that we were looking for.

A second order more accurate equivalent model was then created.

Several trials have been done to see what was happening on the system with imposing different currents with respect

- to equal V_A and V_B varying w_a and w_b,
- to equal w_a and w_b varying V_A and V_B.

It turned out that the load capacitance of each stage does not remain constant as we expected to, but it grows up and lows down depending on the amount of imposed current (so depending on V_A and V_B voltages as well as w_a and w_b variations). The main contribution in the C_{Lro} variation was not due to the added M_A and M_B (as we were going to investigate) but due to the pre-existing M_1 and M_2, whose behaviour has critically changed according to the new configuration.

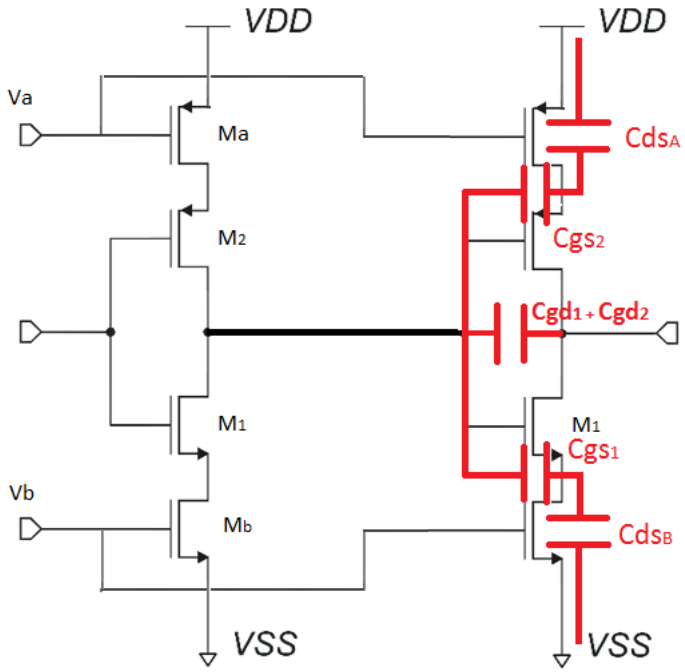

Figure 4.11: Current starved ring oscillator load capacitance contributes.

We have built a model able to describe those second order contributions which deeply consider oxide capacitance variation too for the inner MOS, starting from this notice. Oxide capacitance of each MOS has, in series, the depletion region capacitance C_d, which is usually considered to be constant, but in this case it is mandatory to consider its contribution, that we have called C_q, which is in some way proportional to the transferred charge through the gate capacitance. According to those contributions we can write a model for a new oxide capacitance :

$$C'_{ox} = C_{ox}||(C_d + C_q) = \frac{C_{ox} \cdot (C_d + K \cdot I^{\gamma})}{C_{ox} + C_d + K \cdot I^{\gamma}}. \tag{4.3}$$

This last one expression summarizes up the idea that there is one capacitance contribution which starts to count the most with the increase of the current and that can be, on the other hand, overcome for very slow currents (as described in 4.4), guaranteeing the usual values for C_{ox} (and subsequently for C_{gs} and C_{Lro}).

To determine a final expression to compare results from model and simulations, an investigation on the two parameters K and C_d has been done both for n and p MOS.

Anyway, before that, it was important to state that the real current in each inverter of the ring oscillator is given by a kind of parallel between the two main ones:

- $I_{M1} = I_{M2}$: imposed by the inner MOS,

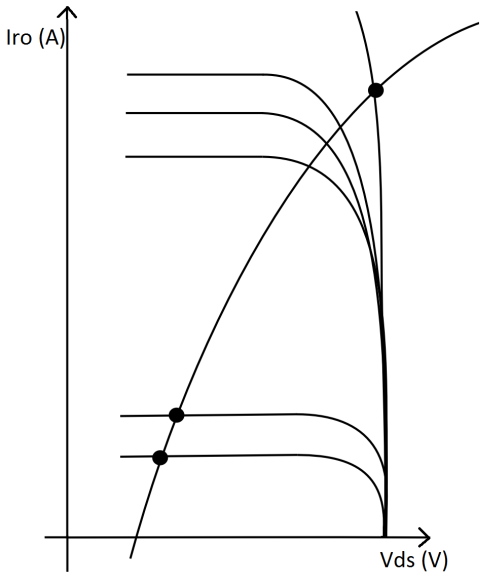

Figure 4.12: VCO ring oscillator current decision.

- $I_{MA} = I_{MB}$: imposed by the peripheral ones, which should actually behave as the real current sources because imposing the minimum current.

To make this statement stronger, the picture in Figure 4.12 can give you a demonstration of why this idea could really work.

Once it was clear which couple of MOS current was dominating on the other, we proceeded in getting to know about the parameters C_d, K and γ.

A parametric fitting analysis on a simple nMOS [3] with a minimum L and an certain w, imposing dc V_{GS} and V_{DS} (in the operative ranges of the ring oscillator MOS one, for example V_{GS} =10 mV and a V_{DS} = 100 mV) while adding a sinusoidal V_g on the gate with a frequency $\widehat{f}$ = 1 MHz and an amplitude of 20 mV. In this way, we knew that, imposing different V_{GS} on that MOS, gate capacitance C_{GS} was going to change as well: packaging off the measurements on circuit simulations based on a sweep of I_D (given by a sweep of V_{gs}) let us obtain the results plotted in Figure 4.13 provided that

$$C_{GS} = \frac{dI}{dV} \cdot \frac{1}{2\pi\widehat{f}}$$

[3] exactly the same specular one has followed for the p MOS, but we show only its final results in order not to be so repetitive

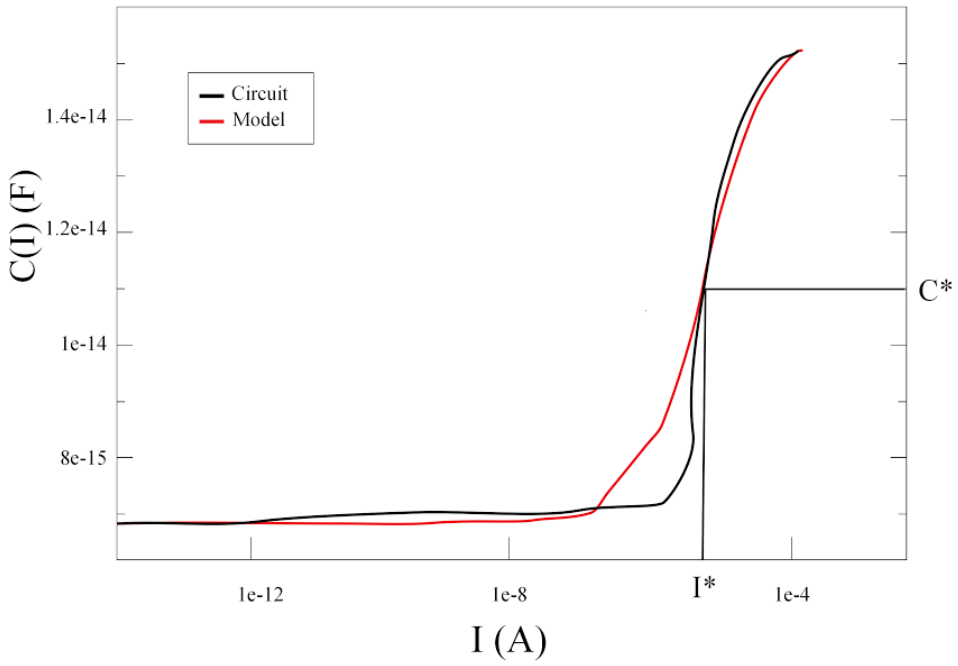

Figure 4.13: Simulation results of nMOS C_{GS}(I): black line is extracted from circuit simulations while the red one is our model fitting.

Cadence circuit simulation results show us that our model could be consider a good one since we were expecting exactly the same behaviour based on the two limits imposed on the 4.3:

$$\begin{aligned} \lim_{I\to+\infty}\left[C'_{ox}\right] &= \lim_{I\to+\infty}\left[\frac{C_{ox}\cdot(C_d+K\cdot I^{\gamma})}{C_{ox}+C_d+K\cdot I^{\gamma}}\right] = C_{ox}, \\ \lim_{I\to 0}\left[C'_{ox}\right] &= \lim_{I\to 0}\left[\frac{C_{ox}\cdot(C_d+K\cdot I^{\gamma})}{C_{ox}+C_d+K\cdot I^{\gamma}}\right] = C_{ox}||C_d. \end{aligned} \tag{4.4}$$

Unifying analytical and graphical results for both p and n MOS, we are able to obtain the desired parameters (Table 4.5 summarize all them up)[4]:

- C_{ox} from the first equation in 4.4,
- C_d from the second one,
- K from 4.3, having set the previous unknowns and used the two C^* and I^*_D in 4.13.

[4]Since the results without the parameter γ were just fine in terms of simulation graphs and analytical ones fitting, we did not explore its variation and took its value equal to 1.

	C_{ox} (F)	C_d (F)	K (F/Am^2)
n MOS	0.0129	0.0102	$2 \cdot 10^3$
p MOS	0.0128	0.0143	$1.25 \cdot 10^3$

Table 4.5: Ring oscillator parameters.

It is possible now to complete the Python code calculation of the C_{Lro} with the sum of the two contributes of $C_{gs} = C'_{ox} \cdot w \cdot L$ of p and n MOS, disregarding any previous additional ones.

Now an analysis of the current starved VCO ring oscillator can be performed regarding the needed number of stages and its power dissipation. According to 3.14, once we have assured on the code to have the correct values for C_{Lro}, if we try to design a VCO with a particular sizing (the same as previous one, see Figure 4.10), $V_A = -100$ mV and V_B =300 mV, for a frequency of 1 MHz, Python code returns a $N_{ro} = 5$, which is exactly what we needed to design on Cadence to have a clock wave of that amount of frequency.

Those last results confirm the precision and correctness, as well as the reliability, of the ring oscillator block on the Python model.

4.4 Design space explorations

A good validation of the Python code has been done. We want now to verify how one can take advantages of using this script to do a reliable design space exploration and have an idea of the whole system behaviour without having to use slow (according to this kind of huge circuit simulations) software design suites.

Once the system constraints are given, this tool gives the user the possibility to know how to change project parameters and variables in order to reach the best compromise in terms of PCE.

Architecture Since the tool is based on the topology, the first thing to choose and provide to the script is the type of architecture to be chosen. Then, the tool is going to return all of the needed power losses.

Below, in Table 4.6, one can find the behaviour (in terms of power dissipations) of all the architectures that our Python script can deal with.

These explorations have been done once the user has decided the sizing (for every block) and other main parameters such as:

- input voltage $V_{in} = 0.2$V;
- $N = 5$ stages;
- @1 MHz clock frequency;
- with an I_{out} =10 nA;

- using $C_{MIM} = 50$ pF;
- UMC018 technology process;
- room temperature equal to 298 K.

		Dickson	Ladder	SeriesParallel	Doubler	Chen
$Pdiss_{Rout}$	(μW)	4.58	9.21	2.75	5.12	2.29
$Pdiss_{sw}$	(μW)	0.92	1.15	1.38	0.91	0.73
$Pdiss_{ro}$	(μW)	0.13	0.13	0.13	0.13	0.13
$Pdiss_{bc}$	(μW)	0.95	1.74	0.84	0.95	0.73
PCE	(%)	45.2	6.2	54.7	40.7	66.4

Table 4.6: Architectures comparison in terms of power losses and PCE.

This table gives the opportunity to do several comparison between topologies and considerations on the results.

First of all, as you can see, the major contribution to power dissipations in those kind of systems (confirming what we have been told in [1]) is due to the output resistance. Surely, at the beginning of your design study, when one has to decide which will be your architecture, having the opportunity to choose, you have to put attention on the amount of its equivalent output resistance.

This is one of the main reasons of why we have chosen the Chen one (of course, varying some parameters as sizing, better results in terms of PCE can be achieved also for the other architectures, anyway, for our constraints, the best compromise has been found for Chen charge pump topology).

The buffer chain power loss is related to the type of architecture too: the more amount of load the chain has to drive, the bigger it has to be and so the more it is dissipating.

Then, according to the other contributions of dissipated power, it is well seen that the one due to the ring oscillator, once we have decided its MOS sizing and the control voltages (V_A and V_B), as well as the operating frequency, remains constant (as it has to). Of course, it is not a contribution that we have to take into account at the starting point of your design exploration because one can take care of it later. We have included its values in the table just to show you that its amount can not be disregarded at all in PCE analysis: this confirms our expectations and it is the added value of this Python script with respect to Matlab package ([1]).

Widths Once it is known that the major loss in the circuit is due to the equivalent output resistance of the charge pump, the designer can go on by sizing it in order to improve the PCE performances.

Considering what it is told by the literature there is the possibility to reach efficiencies of about 80 %: we will show you how this is hard to obtain for a complete system as the one that our model considers.

We have done a sweep of the MOS widths [5] for a Chen architecture with the same constraints considered in the previous paragraph: results are shown in 4.14.

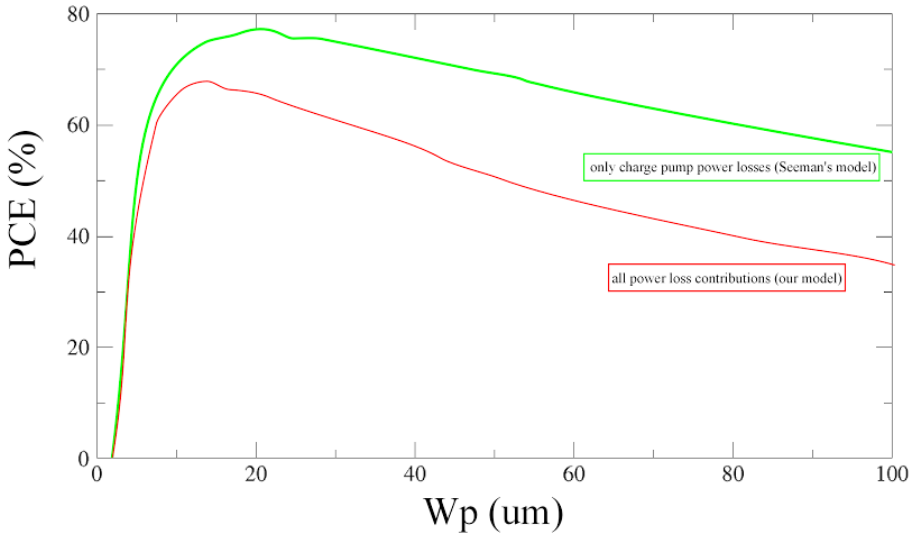

Figure 4.14: Efficiency versus width size.

As you can see an optimum sizing can be found, as well as, by little varying that, the system sits down, since it is not able to sustain the imposed amount of output current (which is a constraint of our project): the voltage drop on the output impedance due to that current makes the output voltage become negative and the system fails.

The green line shows the ideal PCE (with the only contributions of the charge pump losses) and confirms that a better estimations in terms of SC DC-DC performances can be done without considering buffer chain and ring oscillator contributions as it is also considered in Seeman's model ([1]).

Frequency Once we decide which kind of charge pump architecture fits better for our constraints and application, and once we have sized it to reach its best performance in terms of output resistance power losses, we can evaluate the sensitivity of our system to some parameters.

[5] p MOS ones, maintaining constant the ratio between that and the n MOS, so having a proportional sweep of the n MOS widths too.

A frequency sweep is shown in Figures 4.15 [6] and 4.16.

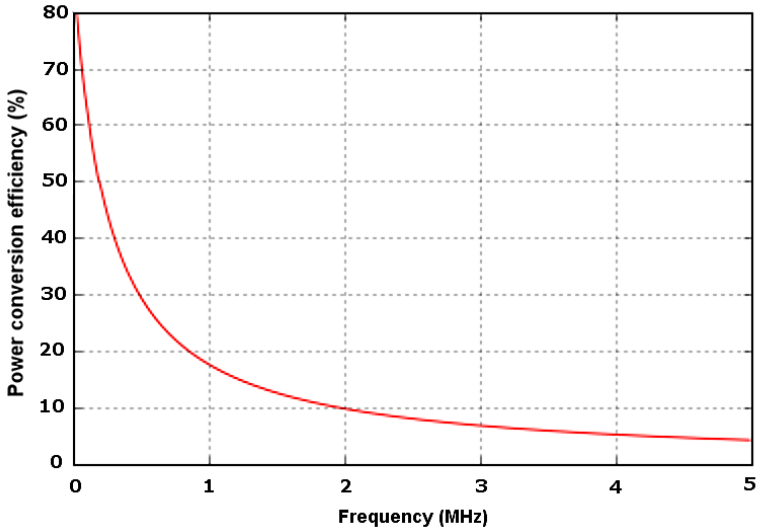

Figure 4.15: Frequency sweep: PCE behaviour.

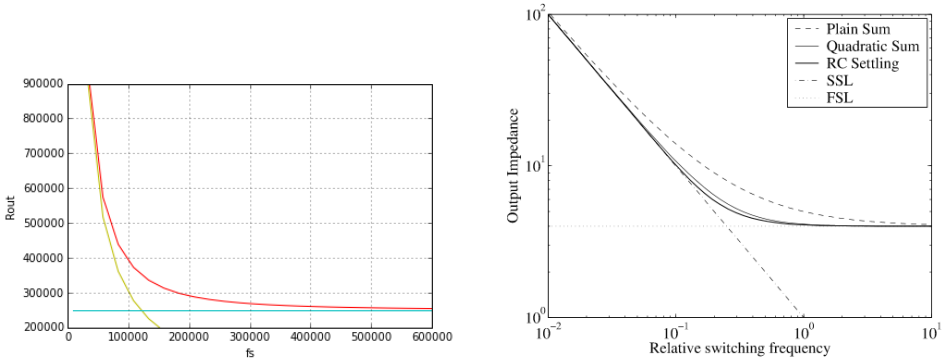

Figure 4.16: Output impedance contributions according to a frequency sweep: comparison with the Seeman theory.

The second one confirms the validity of the two switching limits (fully explained in Chapter 2): with lowering down the frequency the R_{ssl}, the yellow line, starts to count the most, but, increasing it up, the major contribution is given by the blu R_{fsl}, which is constant with it. Red line is the total amount of output resistance, given by the square root of the sum of their squares.

Its behaviour can be seen as one of the main reasons why, with higher frequencies, the power loss due to the charge pump output impedance starts to count the less with respect to the others.

[6] We are considering the real PCE taking into account all the IC losses as it was our goal to.

Since all of thee power losses are proportionally linked to the frequency, the more you grow it up the more you are going to dissipate if you do not want to do any other system variations.

The sum of all them determines the PCE of the system shown in red in Figure 4.15.

Thanks to the new model one can see what happen when other parameters are changing as well as the frequency, to do a better space exploration of the whole system.

Below you can find, respectively,

- in Figure 4.17 a PCE frequency sweep according to different sizing;
- in Figure 4.18 a PCE frequency variation according to different temperatures.

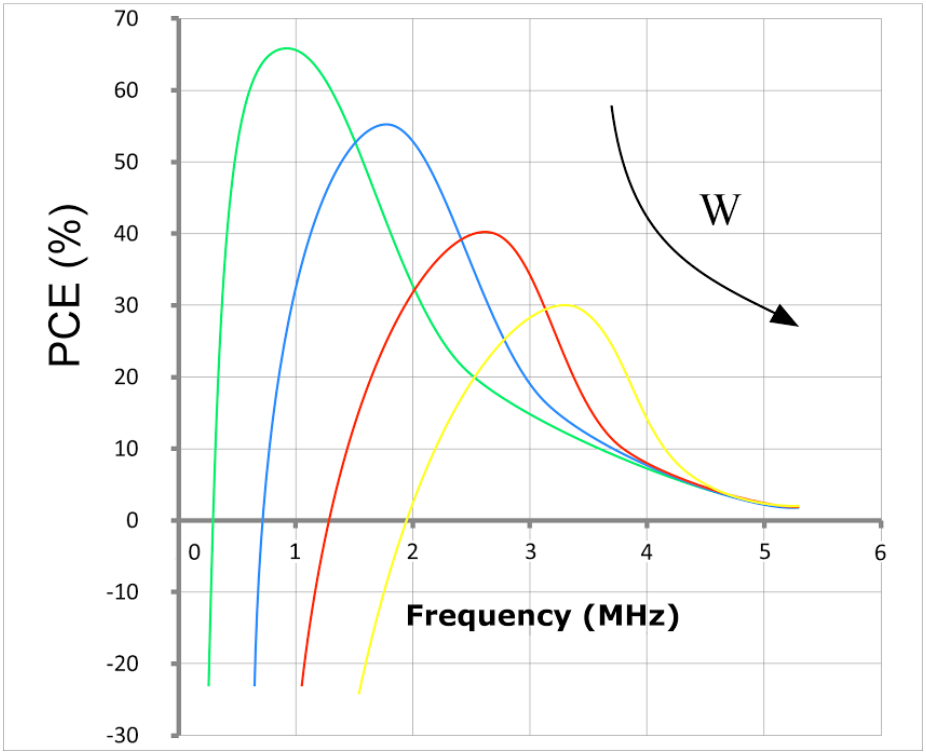

Figure 4.17: Frequency sweep of the PCE with different sizing.

It should be clear that, doing a pre-design exploration with this Python package, you can go on varying more than one parameter at the same time to reach the best efficiently-speaking compromise .

Process All of the previous analysis have been done with the library UMC018. Performances and other considerations change having another technology process.

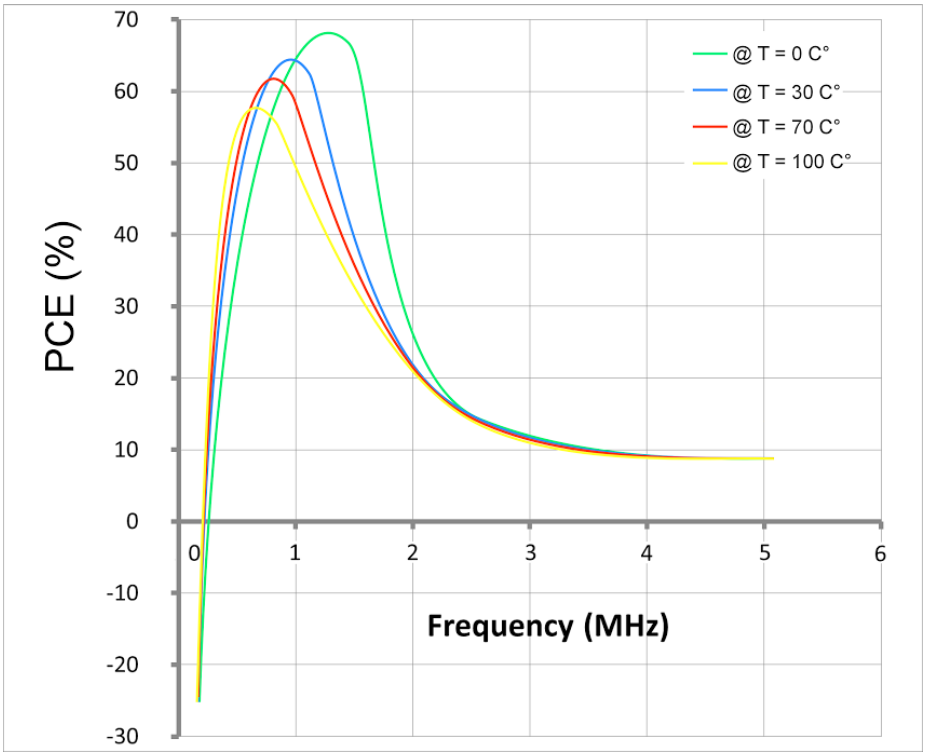

Figure 4.18: Frequency sweep of the PCE with different temperatures.

What follows in the next Chapter 5, for example, is a design with the TSMC55 of Den Bosh Dialog Semiconductor: you will see how different considerations have to be done according to the behaviour of this analogue system.

Chapter 5

Electrical test and design

This chapter deals with a SC DC-DC standard converter, circuit S, which has the same constraints we have considered and has been designed by Luca Intaschi during his PhD in collaboration with Dialog Semiconductor [7].

First of all, after having presented circuit S design, another validation of our system level simulation tool has been performed for its single blocks.

Then we have analysed circuit D, which is an upgrade of S, showing its advantages in terms of PCE. We finally focused on a more accurate and critical analysis of D design to see if any upgrades could have been realized in order to improve its power performances.

At the end, we propose our solution with some starting points for future studies.

5.1 Circuit design

The project of Luca Intaschi has focused on the realization of a SC DC-DC converter in 55 nm CMOS technology. The system has been realized for energy harvesting applications.

A block diagram of S converter is included in Figure 5.1.

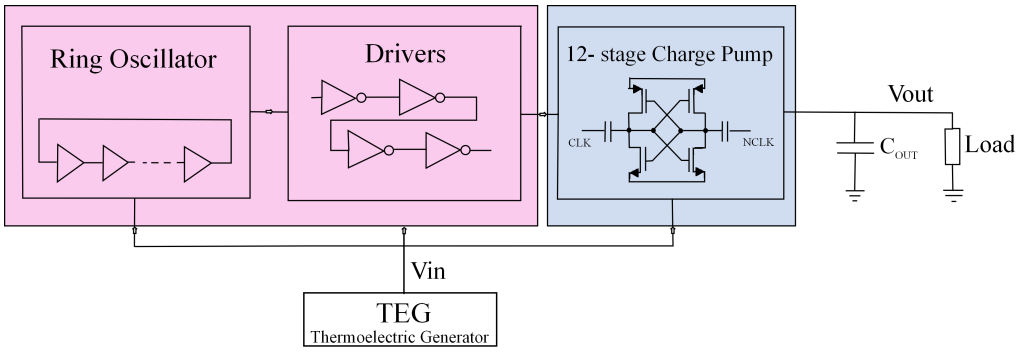

Figure 5.1: S converter schematic block.

An input voltage coming from a TEG of few hundreds of mV needs to be boosted up to a low energy bluetooth operating system voltages. To do that, a SC DC-DC in Chen architecture is designed for operating in low-power mode at low input voltage.

The heart of the converter, highlighted in blu in Figure 5.1, is a 12-stage charge pump (input voltages are very low and every MOS in its stage needs to operate in sub threshold region as described in Chapter 3) and is driven by two-phase split clock signals from a local oscillator (pink part of the same Figure 5.1).

Charge pump inner stages are different from the ones in our previous study and the main differences are shown in Figure 5.2.

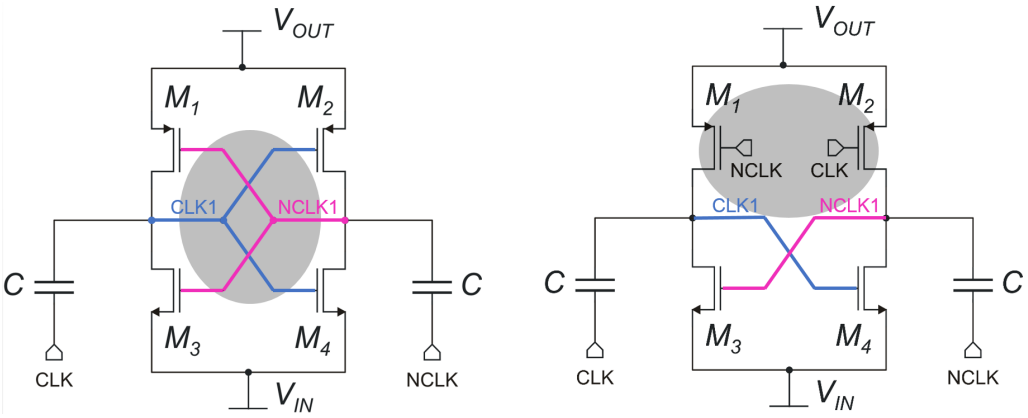

Figure 5.2: Charge pump single stage, two different clock driving configurations.

In the circuit on the left of Figure 5.2, the regular clock signals for n and p MOS are taken from exactly the same current stage (this is the configuration we have dealt with in Chapter 4). In contrast, in the circuit on the right, improved performances in terms of speed are obtained by driving the pMOS with clock wave from the previous stage. Letting those last ones having a higher on voltage ensures size reduction.

With the same output current conditions, this configuration will indicatively reduce the output drop (and so the output losses) due to the reduction of the converter equivalent output resistance R_{eq}.

Ring oscillator is a very important block since the energy comes directly from the TEG source and flows through the charge pump starting from there. Very strong drivers are needed to charge and discharge conversion and parasitic capacitances too.

Dealing then with the two additional blocks, ring oscillator inverters and the first buffer chain ones are simple inverters while other ones (represented as the second line in Figure 5.1) are boosted. These boosted inverters include two charge pumps each, able to increase the base voltage coming from the TEG generator (Figure 5.3), guaranteeing a clock for the p and n MOS of the following inverter

which has a greater dynamic. Increasing the V_{gs} of those last ones lets the designer shrink their sizes and reduce the power consumption coming from this stage (of course you have to take into account the power losses due to the two little charge pump too, but, anyway, at the end it is possible to obtain a higher whole design PCE).

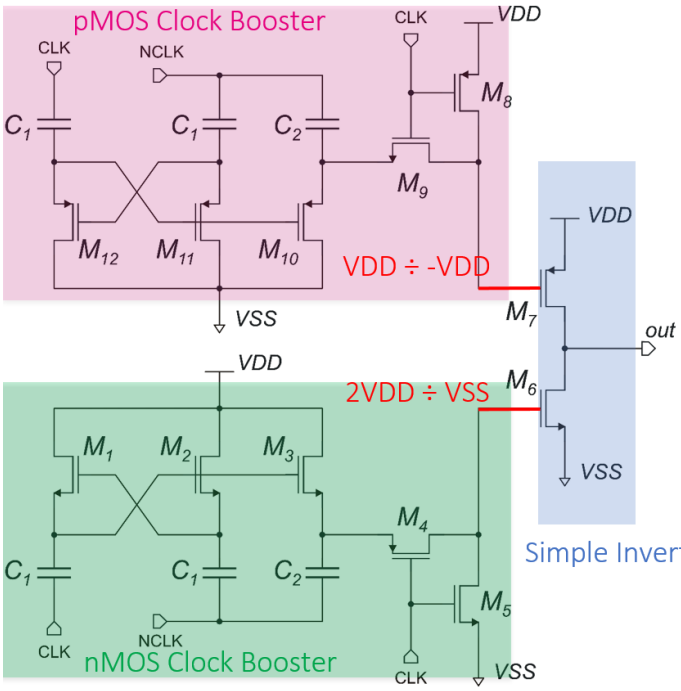

Figure 5.3: Boosted driver configuration.

S converter has been taped out and fabricated on silicon exhibiting the following performances at room temperature:

Output Voltage	1.82 V
Output Power	15.47 μW
PCE	36.9%
Frequency	4 MHz

Table 5.1: S performances at I_{out} = 8.5 μA, T=27 °C and V_{teg} = 200 mV.

Model validation This new charge pump configuration is not easy to model with our script since the charge multipliers of this configurations are not instantiated in the code.

Anyway, the code is very easily rearrangable for ones needs, and, by simply adding the new charge multiplier calculus, it is possible to estimate the R_{eq} also

in this case. It will not be that precise, because equivalent resistance equations (see 3.4) of each stage are still considering every MOS V_{gs} equal to V_{in}, while one should consider that, stage by stage, pMOS switches are driven by a higher input voltage, and so V_{in} should change every stage for every pMOS). At the end, R_{FSL} turns not out to be so precise in contrast with the R_{SSL} which is still well-estimated since the MIM capacitor (as well as equivalent MOS capacitances) remains the same as before (and a good estimation of the load that the buffer chain has to drive can still be correctly performed).

Our model returns an equivalent output resistance of 91.6 KΩ that is not so good in comparison with the real one shown in circuit simulations of 68.2 KΩ.

We have preferred to go on with our study instead of taking more care of this point: the model should give a designer just a hint and a guide line to estimate architecture parameter values, otherwise the complexness of it would reach the simulator one and no convenience would be provided in line with the simplicity in realization.

Dealing with the buffer chain, since its load (C_{Lbc}, given by the charge pump) can be accurately evaluated, it is possible to do a precise estimation of the needed number of stages and, subsequently, the power losses related to it.

What is new in S and D design with respect to our model is the presence of the double chain (one for clk and the other for nclk) and the boosted inverters instead of one single simple inverter chain.

By the automated model, to drive the total amount of C_{Lbc} (divided by two in order to consider just one clock chain) the needed number of inverters turned out to be equal to 10, which can be comparable with Luca's design of four simple inverters and three boosted ones. Model simulation returns a $Pdiss_{bc} \cong 23.6\mu$W against the 20.1 μW calculated by the circuit one.

According to circuit simulations, in fact, they show out that a bigger power loss comes out from the boosted inverters with respect to a single inverter (because of the presence of the two little charge pumps which drive each of them). Anyway, since the number of the inverters are decreased, there is an effective advantage in considering S buffer chain configuration instead of the classical one.

Finally, dealing with the ring oscillator, it has been confirmed that our Python script can be used to estimate a good average power loss of it. According to the same sizing and an input voltage of $V_{in} = 0.2$ V, in fact, requiring a clock frequency of 4MHz, the model returns a $Pdiss_{ro} = 81.9$ nW, which is comparable with the circuit 91.6 nW one.

Comparison between circuit and model simulations are shown in the Table below (5.2).

	Charge pump	Buffer chain	Ring oscillator
Circuit	15.47 μW	40.09 μW	91.6 nW
Model	13.85 μW	47.2 μW	81.9 nW

Table 5.2: Circuit S: comparison between circuit and model simulations of the power loss contributions @ f_s = 4 MHz, I_{out}= 8.5 μA, V_{in} = 200 mV.

5.1.1 D converter new design

Circuit D is an upgrade with respect to circuit S.

The improvements in the design are:

- the local ring oscillator is a VCO as the one described in Chapters 3 and 4;
- a simple control logic is added at the output of the charge pump to have the possibility to select which of the charge pump output to use as system output.

Another circuitry for the drivers needs to be designed since they are consuming too much power (as Table 5.2 confirms)[1].

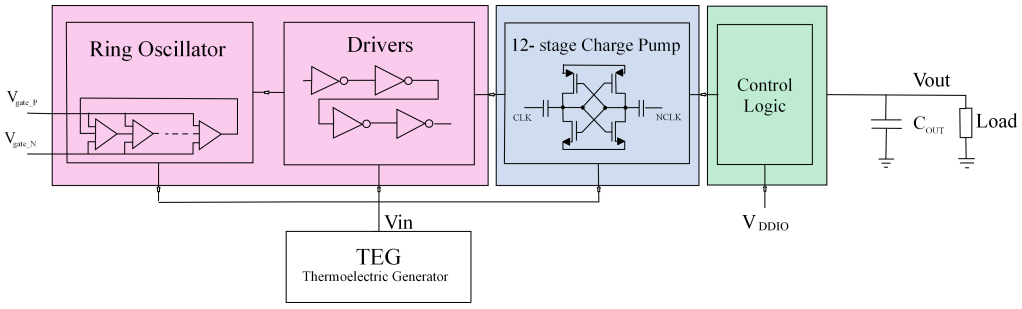

Figure 5.4: D converter schematic block.

Dealing with the VCO ring oscillator, it represents a huge development in terms of frequency regulation: frequency can be decreased a lot, letting the PCE of the whole system increase proportionally with the decreasing of the power losses.

Its performances have been confirmed by our Python script, with control voltages $V_{control\_VCO1_p}$ and $V_{control\_VCO1_n}$ (which correspond to the V_A and V_B in the *external_parameters.txt* file) respectively equal to 30 mV and 220 mV.

To generate an operating frequency of 4 MHz, the number of necessary stages for the VCO in Python script turned out to be around N_{ro} = 5.3 $\cong$ 5, in line with what Luca has found out to be necessary, working on Cadence Virtuoso.

[1] We will discuss on this in the following Section 5.2.

The estimation of power losses according to this block are also good: the model returns a power dissipation $Pdiss_{ro}$ equal to 90.85 nW, which is well comparable with the circuit one of 96.22 nW.

On the right of Figure 5.4 you can see how, thanks to this upgrade, with the same environmental constraints (input voltage and output current), circuit D is able to reach very higher power conversion efficiencies with respect to S.

The details of block losses are resumed in Table 5.3: for S converter f_s = 19.23 MHz is the lower limit to let it properly work, while the D circuit is able to reach a minimum clock frequency of 3.9 MHz).

This logic is realized with a simple analog multiplexer driven by three control signals (c1, c2 and c3) which allows the user to select as converter output one of the last 8 stages of the charge pump. An example of how it can be used is shown on the left of Figure 5.5: on the upper part there is the timing behaviour of the three control signals, while at the bottom the variation of the output voltage is performed according to it.

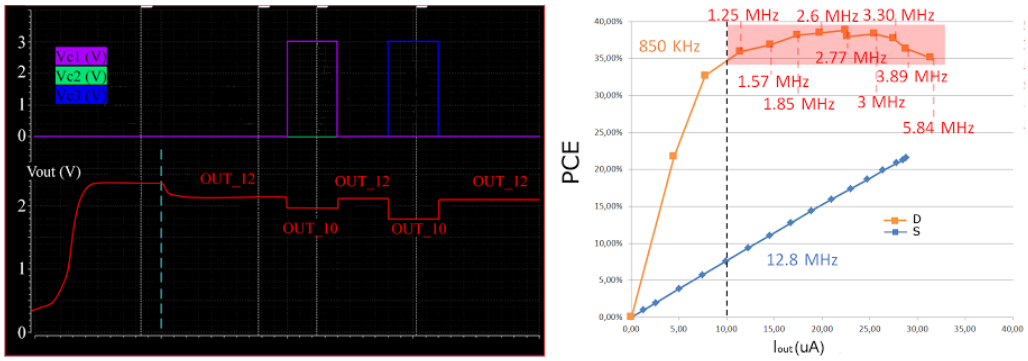

Figure 5.5: Circuit D simulations. On the right: how the output logic works. On the left: D improved performances results with respect to S.

	Charge Pump	Buffer Chain	Ring Oscillator	Power Efficiency
Circuit S	55.34 μW	4.831 μW	412.18 nW	31.46 %
Circuit D	38.2 μW	1.508 μW	96.22 nW	44.11 %

Table 5.3: Comparison in terms of power losses between old circuit S and new D one with V_{in} = 250 mV and I_{out}= 20 μA .

The control logic of Figure 5.6 is added at the end of the charge pump. It is not imputable on system performances growth, but it can be useful for future usages and applications for the chip if its following stages would need an intermediate voltage between V_{teg} and $(1+k)V_{teg}$ (with k = 12).

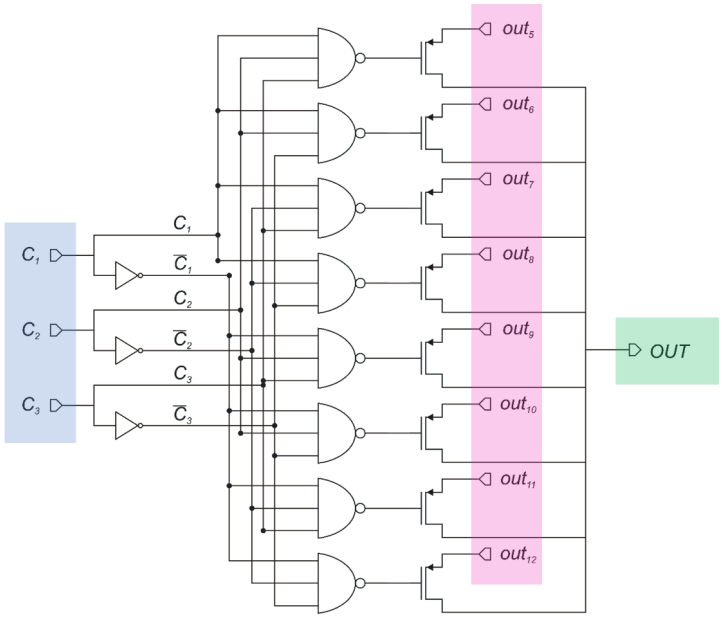

Figure 5.6: D converter control logic schematic.

5.2 Upgrades

Our goal, during the internship at Dialog Semiconductor, has focused on investigating the circuit D, with particular attention to the boosted drivers of the buffer chain, to improve PCE.

The choice of focusing our attention on this block has been made since simulations showed out (see Table 5.3 to prove it) that the power losses due to that block are predominant.

Boosted driver inverters consume a lot of power since they are still very big; therefore, strong modification leading to loss reduction contribute turn out to be very important.

Having a look at the two little charge pumps (previous Figure 5.3) which drive the boosted inverters in the last stages of the buffer chain, we noticed that, of course, they increase the voltage dynamics of the boosted inverter n and p MOS, but not to complete satisfaction.

As shown in Figure 5.7, in sub threshold region, the more one increases the input voltage, the largest is the current and, as a direct consequence, the more one can reduce MOS sizes and the related losses.

Having $2V_{teg}$ instead of V_{teg} was a good choice, but further upgrades could be done, i.g., with having an input of the boosted driver which goes from 0 to 1 V, and, why not, from -1 to 1 V.

Up to now, no differential behaviour of the charge pump was taken into account, but some considerations on why we should choose this approach need now

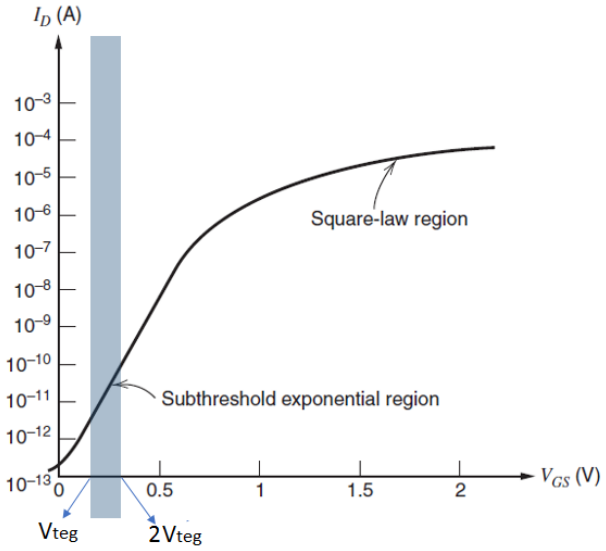

Figure 5.7: MOS transcharacteristic.

to be done.

5.2.1 Differential charge pump

Dealing with the boosted inverter, the speed and driving of the pMOS turned out to be the major trade off. Increasing the single-ended dynamic of the clock made the nMOS stronger, but, as a counterpart, slowed the pMOS commutation down, since in the sweep the lower voltage which turned on the pMOS was still 0. The major drawback could have driven to a decrease in functioning correctness because of the asymmetry between up and down clock commutation.

The possibility of having a differential design for the whole circuit has been taken into account (shown in Figure 5.8) since the TEG generator is floating.

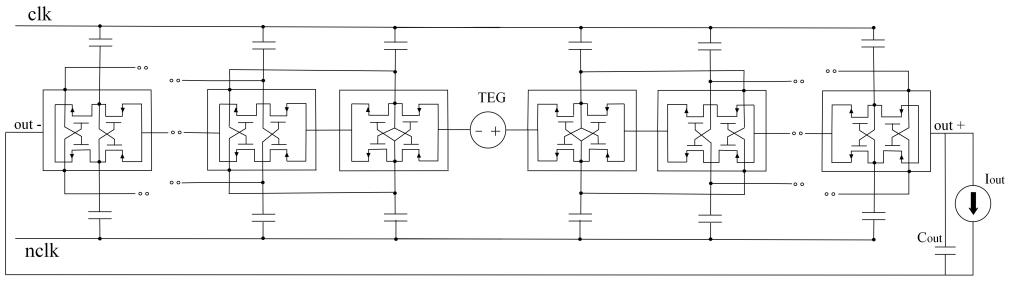

Figure 5.8: 12 stage differential charge pump architecture.

Starting from the very beginning of the IC, our system clock is now a square wave between +100 mV and -100 mV.

Since we did not want to modify all the system architecture in order to do this change, the major nominal voltage reached in the system, if was previously imposed by the 12 stages charge pump at an open loop value around 2.4 V $\cong V_{teg}\cdot$ 12 (decreased around to 1.8 V in I_{out} presence because of the output resistance of the charge pump), now it will hardly reach 1 V. From now on, we will call OUT+ = 1 V and OUT- = -1 V, indicating the major positive output voltage of the converter and the minor negative one, respectively.

5.2.2 Voltage Controlled Differential Level Shifter design

The availability on the chip of those two voltages let us use them to generate the increased clock levels for the boosted inverters. The main challenge has been to find a way to realize such a high dynamic clock wave starting from the ring oscillator output one between +0.1 V and -0.1 V.

In fact, it should be easy to understand that, since V+ and V- come from the charge pump output which has been sized to sustain an output current of a certain maximum value (i.e. 6 μA), not so much power could be requested by other eventual added blocks (if we want to connect them to it) or the whole system is unequivocally going to sit.

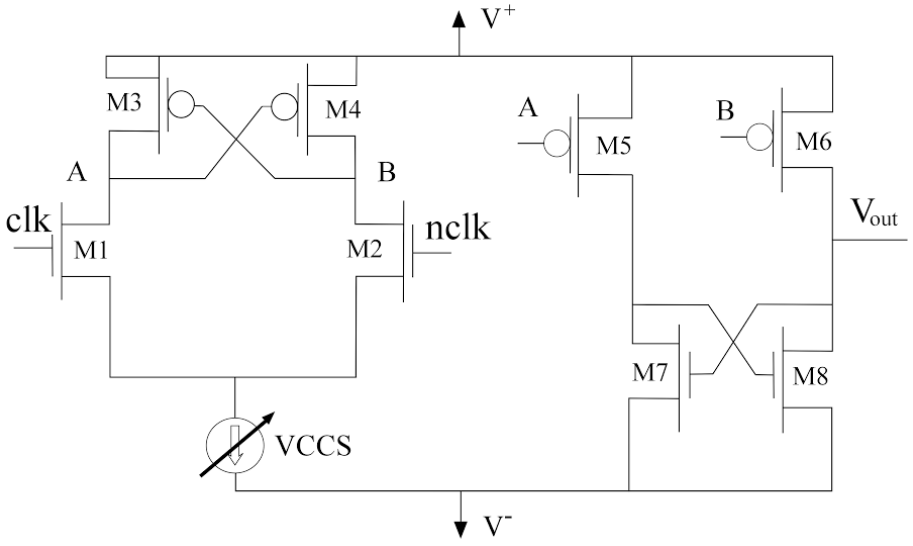

Figure 5.9: Voltage controlled level shifter.

A voltage controlled level shifter (shown in Figure 5.9) has been designed in order to respond to our needs: taking *clk* and *nclk* from the two chains coming from the VCO ring oscillator, we inserted two positive feedback by M_3, M_4, M_7 and M_8, to let nodes A and B sweep from $V+$ to a voltage around 0.2 V [2]. It

[2]NB: V+ and V- will be then connected with $OUT+$ and $OUT-$.

would be possible, then, to throw off balance M_5 and M_6 and the output V_{out} could reach the expectations of switching between $V+$ and $V-$.

V_{out} is meant to drive just one very strong boosted inverter which is connected between +0.1 V and -0.1 V and is able to give to the differential charge pump the correct clock wave.

Dealing with the differential level shifter, after having considered a basilar circuit without the current generator (VCSS in Figure 5.9) at the bottom, this last one turned out to be necessary. Without it, in fact, the voltage drop (clk to V-) as well as M_1 and M_2 were not strong enough to turn on and off alternatively without having on one of them for the major part of the period (T $= 1/f_s = 250$ ns).

We have obtained the desired output only by pumping current at the bottom of the first block with an ideal voltage controlled current source able to generate current pulses of about 20 μA for every 6 ns clock rising and falling edge. In this way A and B correctly switched up and down enabling the correct V_{out} behaviour as the boosted clock signal of our interest (see Figure 5.10, where vcmnd is the voltage command of VCCS).

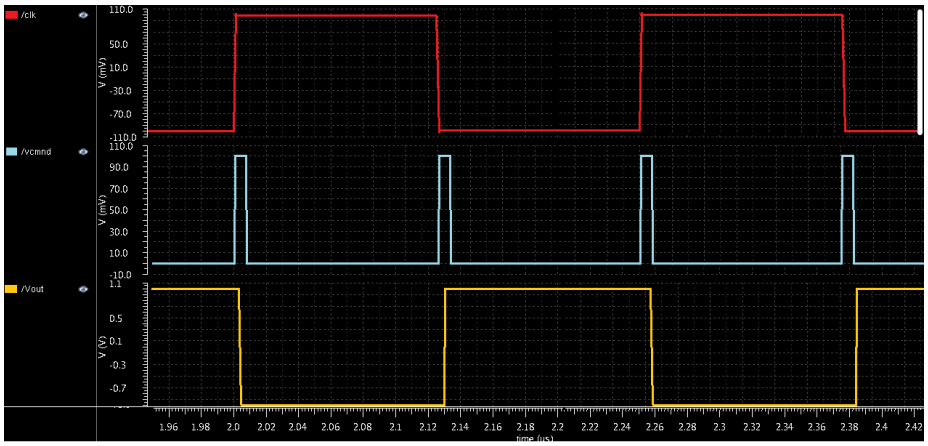

Figure 5.10: Voltage control signal (vcmnd) needed to drive the differential level shifter.

This block itself, ideally supplied, is not consuming so much, but the main challenges deal with some issues:

- a real voltage controlled current source which let it work properly has to be found,
- everything has to be integrated in the whole circuit (as shown in Figure 5.13).

Both points have been taken into account and they are briefly resumed here.

Voltage controlled current source design The realization of a real system which could replace the ideal voltage controlled current source has been analysed:

the challenge has been generating an impulsive amount of current which lasted the less it could every rising and falling edge of the basic clock.

Its needed basilar behaviour can be summarized in the following steps:

- as soon as the input clock *clk* goes from high to low we need to provide a pulse (vc) from V- able to switch on a simple low Vt nMOS (M_{cg1}) transistor attached by its Drain below the level shifter;
- we need to realize a voltage control signal (vcd) on each rising edge of the clock too, so the same structure (which drives another identical current source lowVt nMOS, Mcg2) is replicated using the nclk as input;
- signals vc and vcd are able to switch on the two current generators (Mcg1 and Mcg2, respectively, sized to pump the correct amount of current from the upper block) of the differential level shifter and so obtain the desired output voltage Vout.

If we put attention on the amount of the current flowing in the two branches of the charge pump, we can see that they are bigger than the needed one of about 20 μA (even if we have sized the two current generators to pump that amount). By plotting the behaviour of the two current generators we realize that both of them pump currents even if they are not switched on by their respective control voltages, so the real current flowing into the ON-MOS (M6 or M7 of the differential level shifter) will be greater than expected .

This is due to Mcg1 and Mcg2 Cds parasitic effects: even if one of those switches is turned OFF, a drain current still exists. It is a real help for the whole behaviour of our circuit because it allows us to reduce the current generators sizes since they do not need to pump on their own all the needed current (Figure 5.11).

We are leaving the problem of finding this block open for future studies according to the fact that it is not so easy to be solved.

Some trials have been done to see if any slope detector can satisfy our needs, according to the fact that the main difficulties in its realization are:

- having an input signal voltage dynamics between -100 ad +100 mV and voltage supplies not greater than OUT+ and OUT-;
- being fast in revealing the slope of the clock and produce very short-lasting signals;
- not decreasing PCE too much: we think that reasonable advantages can be produced if the whole new D design is increasing about 5% the previous one.

Figure 5.11: Parasitic currents in the current generators at the bottom of the differential level shifter.

Whole new system behavior Considering, at the end, to maintain an ideal block (named after a question mark in Figure 5.13) as the current source of our level shifter, according to the fact that we could have richen a larger PCE thanks to the differential version of the charge pump, we proceed simulating all the blocks together.

A resume of how we proceeded is listed here.

- We set a $V_{in} = V_{TEG} = 250$ mV;
- we instantiated the VCO ring oscillator and the buffer chain from the previous circuit D;
- we left the ideal voltage controlled current source at the bottom of the differential level shifter;
- we added, for the start-up , two ideal dc voltage supplies of 1 V (V+) and -1 V (V-) and, as load, an only capacitor ($C_{out} = 100$ pF), requesting different values of I_{out};
- once the output of the charge pump has reached the correct level we connected it to the supplies of the level shifter (V+ and V-) so to have a self-driven system.

According to the figures (5.15 and 5.14) and the tables (5.4 and 5.5) below it will be clear how this configuration is not having the desired performances.

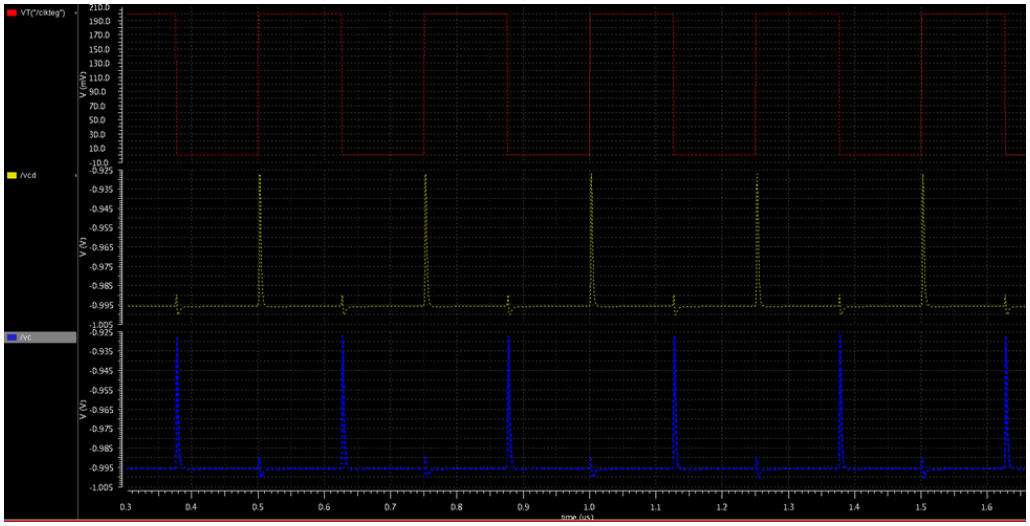

Figure 5.12: Behaviour of the voltage controlled current source driving voltages.

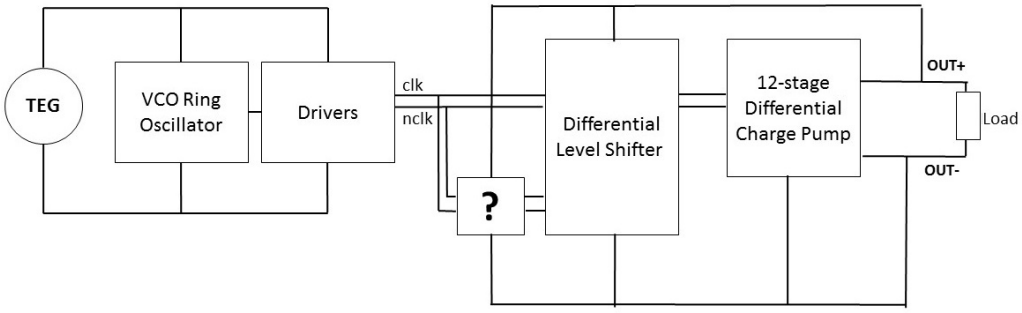

Figure 5.13: Whole ideal system schematic blocks.

While, for low currents, it seems to be more efficient in terms of power conversion, it can hardly sustain currents larger than 2.8 - 3 μA, so we can sadly state that it cannot be taken into account for those kind of applications.

Figure 5.14: 4 MHz transient simulation of the old converter D.

Iout (μA)	Vout (V)	Pout (μW)	η (%)
1	2.41	2.41	17.5
2	2.36	4.73	29.87
3	2.32	6.96	38.8

Table 5.4: Old D circuit performances.

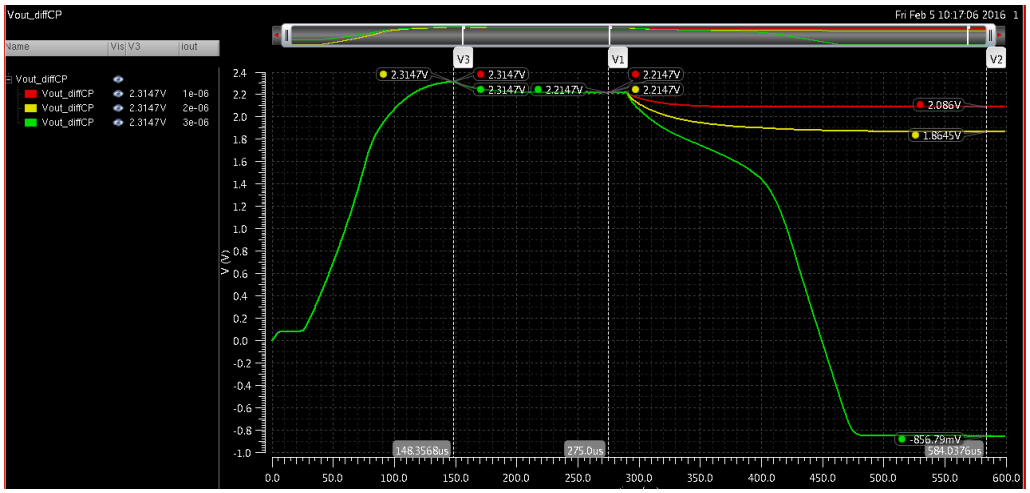

Figure 5.15: 4 MHz transient simulation of the proposed new converter D.

Iout (μA)	Vout (V)	Pout (μW)	η (%)
1	2.08	2.08	19.04
2	1.856	3.73	31.04
3	-0.85	2.57	X

Table 5.5: New D circuit performances.

Chapter 6

Conclusions

Cons Unfortunately we have to leave this last aspect non-accomplished at all because of timing issues, but we have presented the problems and constraints one should consider to go on with the studies.

Dealing with the model simulator, of course there are some aspects that cannot be taken into account (as particular circuit adjustments, i.g. Figure 5.2 one) since it is just a model and not a real circuit simulator.

Pros On the other hand, our Python system's level model enables quick design and application space investigation for SC DC-DC converters. The PCE of a converter can be estimated in very little time, and a design space parameter exploration can be rapidly iterated to achieve the best solution for a given application.

However, as many approximations are used in the analysis, device-level circuit simulation (e.g. SPICE) are necessary for a more-precise estimate of PCE, as we have seen in Chapter 5 according to S and D converters.

Our new system-level model is definitely more precise than the Seeman one for energy harvesting applications. First of all the sub-threshold MOS region has been considered according to the low available voltage input. What is more, we have shown (i.g., in Table 5.3) how much important are the power loss contributions of the additional driving blocks with respect to the single converter one and how much they can decrease PCE.

The feasibility study has succeed the realization of the script and several validations of our model with respect to a real implemented design has been done thanks to the circuit simulations using Cadence Virtuoso both with the UMC018 process and TSMC55 one during the internship with Luca Intaschi and Francesco Dalena at Dialog Semiconductor.

We have demonstrated how the model is quickly re-arrangeable for new or different charge pump architectures and for various design choices.

A design experience has been done in order to decrease PCE in a real IC and go deeper in the design of that project.

Appendix A

Acronyms

CMOS	Complementary Metal Oxide Semiconductor i
FSL	Fast Switching Limit 12
FSL	Fast Switching Limit 12
IC	Integrated Circuit i
ITRS	International Technology Roadmap of Semiconductor .. 36
KCL	Kirchoff Current Law 12
KVL	Kirchoff Voltage Law 14
LDO	Low Drop Out 1
LED	Light Emitting Diode 7
MEMS	Micro Electro Mechanical Systems 24
PCB	Printed Circuit Board 7
PCE	Power Conversion Efficiency i
SC DC-DC	Switched Capacitor DC-DC i
SC	Switched Capacitor 1
SCC	Switched Capacitor Converter iii
SI	Switched Inductor 1
SSL	Slow Switching Limit 11
TEG	Thermo Electric Generator i
TI	Texas Instrument 7
TSMC	Taiwan Semiconductor Manufacturing Company i
UMC	United Microelectronics Corporation i
VCO	Voltage Controlled ring Oscillator 21
VCR	Voltage Conversion Ratio iii
VSS	Variable Structure Systems 10

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