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A Continuous-Time Delta-Sigma Modulator for Ultra-Low-Power Radios

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List of acronyms

AA	Anti-alias
ADC	Analog-to-digital converter
CIFB	Cascaded integrator feedback
CT	Continuous-time
DAC	Digital-to-analog converter
DEM	Dynamic-element matching
DLL	Delay-locked loop
DSCR	Dual switched-capacitor-resistor
DSM	ΔΣ modulator
DT	Discrete-time
DWA	Data weighted averaging
GBW	Gain bandwidth
IBN	In-band noise
ISI	Inter-symbol interference
LSB	Least significant bit
NRZ	Nonreturn-to-zero
NTF	Noise transfer function
OBG	Out-of-band gain
OSR	Oversampling ratio
RF	Radio frequency
RZ	Return-to-zero
SAB	Single amplifier Biquad
SAR	Successive approximation register
SC	Switched-capacitor
SNR	Signal-to-noise ratio
SNDR	Signal-to-noise-and-distortion ratio

SQNR	Signal-to-quantization noise ratio
STF	Signal transfer function
ULP	Ultra-low-power

List of symbols

α	Starting time instant of a DAC pulse
β	Ending time instant of a DAC pulse
dQ	Charge error
Δ	Quantization step
e_q	Jitter charge error sequence
f_{bw}	Signal bandwidth
f_s	Sampling frequency
H_{CT}	Continuous-time feedback transfer function
H_{DT}	Discrete-time feedback transfer function
G_{CT}	Continuous-time forward transfer function
G_{DT}	Discrete-time forward transfer function
L	Loop filter order
N	Number of bits in the quantizer
N_q	Quantization noise
NTF	Noise transfer function
OSR	Oversampling ratio
Q	Charge
STF	Signal transfer function
t_d	Loop delay
t_d	Jitter timing error
T_s	Sampling period
τ	Time constant
τ_d	Normalized loop delay

Introduction

The increasing need of digital signal processing for telecommunication and multimedia applications, implemented in complementary metal-oxide semiconductor (CMOS) technology, creates the necessity for high-resolution analog-to-digital converters (ADCs). Based on the sampling frequency, ADCs are of two types: Nyquist-rate converters and oversampling converters. Oversampling converters are preferred for low-bandwidth applications such as audio and instrumentation because they provide inherently high resolution when coupled with proper noise shaping. This allows to push noise out of signal band, thus increasing the signal-to-noise ratio (SNR). Continuous time delta-sigma ADCs are becoming more popular than discrete-time ADCs primarily because of inherent anti-aliasing filtering, reduced settling time and low-power consumption

In this thesis, a 2nd-order 4-bits continuous-time (CT) delta-sigma modulator (DSM) for radio applications is designed. It employs a 2nd-order loop filter with a single operational amplifier. Implemented in a 65-nanometer CMOS technology, the modulator runs on a 0.8-V supply and achieves a SNR of 70dB over a 500-kHz signal bandwidth. The modulator operates with an oversampling ratio (OSR) of 16 and a sampling frequency of 16MHz.

In the first chapter the principles of ΔΣ modulators are analysed, introducing the differences between discrete-time (DT) modulators and continuous-time (CT) modulators. In the next chapter the techniques to design a ΔΣ modulators for

ultra-low-power radios are presented. The third chapter talks over the design of the operational amplifier, which appears inside the loop filter. In the fourth chapter the performance of the complete ΔΣ modulator, which employs a flash quantizer, is shown. Finally, in the last chapter, a performance analysis is carried out replacing the flash quantizer with an asynchronous SAR quantizer. The analysis shows that a further reduction of the quantizer power consumption of about 40% is possible. The conjunction of this replacement with the power-saving technique implemented in the loop filter appears effective.

1. ΔΣ modulators: principles of operation and architecture

In this chapter, the need for oversampling data converters will be discussed. Delta modulation and delta-sigma modulation will be described and compared. Important design aspects of CT DSMs such as discrete to continuous-time conversion, selection of the feedback pulses and anti-alias (AA) filtering is covered as well.

1.1 FEATURES

DSMs employ a combination two important concepts: oversampling and noise shaping.

1.1.1 OVERSAMPLING

In signal processing, oversampling is the process of sampling a signal with a sampling frequency significantly higher than the Nyquist rate. Theoretically, a bandwidth-limited signal can be perfectly reconstructed if sampled above the Nyquist rate, which is twice the highest frequency in the signal.

$$\text{OSR} = \frac{fs}{2fbw} \tag{1.1}$$

Oversampling improves resolution, reduces noise and helps to avoid aliasing and phase distortion by relaxing anti-aliasing filter performance requirements.

Oversampling can make it easier to realize analog anti-aliasing filters. Without oversampling, it is very difficult to implement filters with the sharp cut-off

necessary to maximize use of the available bandwidth without exceeding the Nyquist limit. By increasing the bandwidth of the sampled signal, design constraints for the anti-aliasing filter may be relaxed [1]. Once sampled, the signal can be digitally filtered and down sampled to the desired sampling frequency. In practice, oversampling is implemented in order to achieve cheaper higher-resolution A/D and D/A conversion. If multiple samples are taken of the same quantity with uncorrelated noise added to each sample, then averaging N samples reduces the noise power by a factor of 1/N. Oversampling by a factor of 4, the signal-to-noise ratio in terms of power improves by factor of 4 which corresponds to a factor of 2 improvement in terms of voltage. Certain kinds of A/D converters known as delta-sigma converters produce disproportionately more quantization noise in the upper portion of their output spectrum. By running these converters at some multiple of the target sampling rate, and low-pass filtering the oversampled signal down to half the target sampling rate, a final result with less noise (over the entire band of the converter) can be obtained. Delta-sigma converters use a technique called noise shaping to move the quantization noise to the higher frequencies.

1.1.2 NOISE SHAPING

Oversampling can become more effective if the In-band noise (IBN) is further reduced by noise shaping. The quantization noise is shaped by an appropriate high-pass filter function. The combination of oversampling and noise shaping is more effective compared to oversampling alone. The performance can be further

improved by using a higher order filter; but the noise shaping does not reduce the total noise power in the Nyquist interval. Integrating the noise from 0 to $f_s/2$ would still yield the same power as for oversampling alone. In this way, the In-band noise is reduced and more noise is pushed towards higher frequencies.

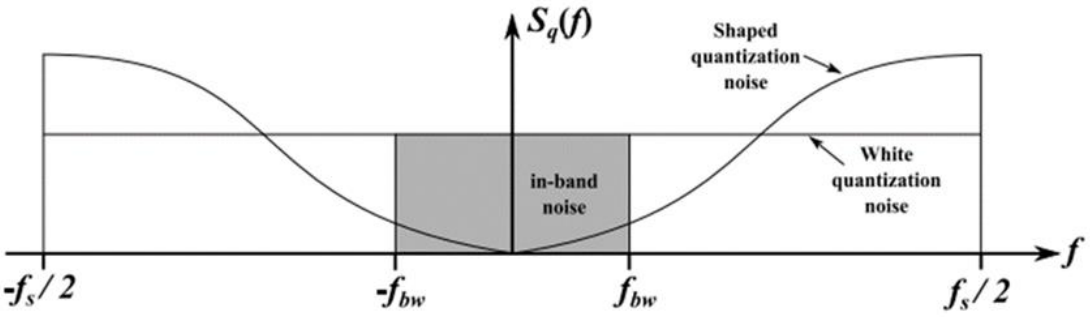

Fig. 1.1: Quantization noise spectra with oversampling and noise shaping [4].

To full exploit the benefit provided by oversampling and noise shaping, a sharp low-pass digital filter is required after the ADC to filter out the noise outside the band of interest. Furthermore, the sampling rate at the output of the ADC must be reduced to the Nyquist rate by discarding the unnecessary samples. Usually, filtering and decimation are combined into one filter called decimation filter.

1.2 Δ AND ΔΣ MODULATOR

ΔΣ modulation (DSM) is inspired by Δ modulation (DM). If quantization were linear, the following would be a sufficient derivation of the equivalence of DM and DSM:

1) Start with a block diagram of a Δ modulator/demodulator.

2) The linearity property of integration makes it possible to move the integrator, which reconstructs the analog signal in the demodulator section, in front of the Δ-modulator.

3) Again, the linearity property of the integration allows the two integrators to be combined and a ΔΣ modulator/demodulator block diagram is obtained.

However, the quantizer is not homogeneous, and so this explanation is flawed. It is true that ΔΣ is inspired by Δ-modulation, but the two are distinct in operation. From the first block diagram in Fig. 1.2, the integrator in the feedback path can be removed if the feedback is taken directly from the input of the low-pass filter. In other words, DSM and DM swap the position of the integrator and quantizer.

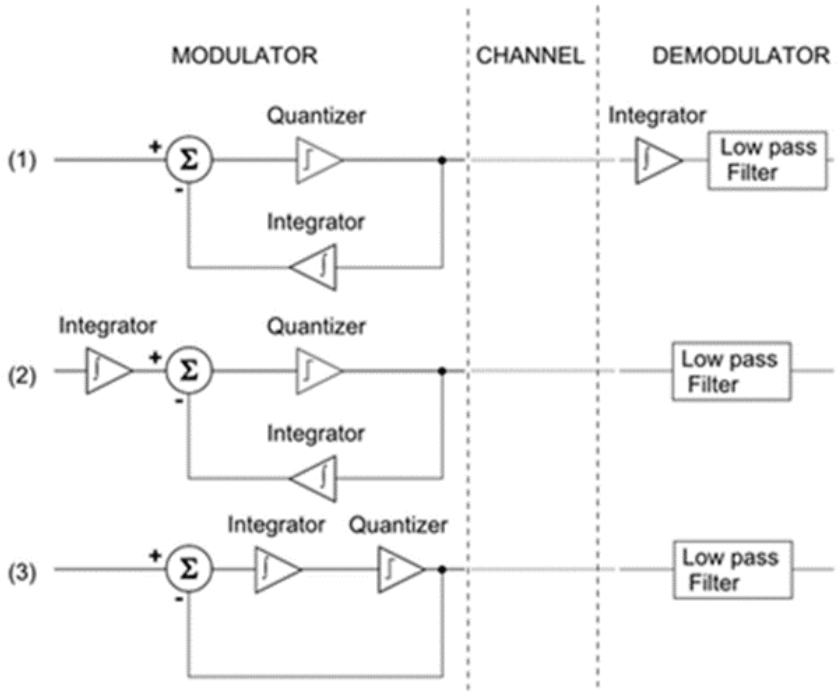

Fig. 1.2: Derivation of ΔΣ- from Δ-modulator [29].

The net effect is a simpler implementation that has the added benefit of shaping the quantization noise away from signals of interest (i.e., signals of interest are low-pass filtered while quantization noise is high-pass filtered). This effect becomes more dramatic with increased oversampling, which allows quantization noise to be somewhat programmable.

On the other hand, Δ-modulation shapes both noise and signal equally. Additionally, the quantizer used in DM has a small output representing a small step up and down the quantized approximation of the input while the quantizer used in DSM must take values outside of the range of the input signal, as shown in Fig. 1.3.

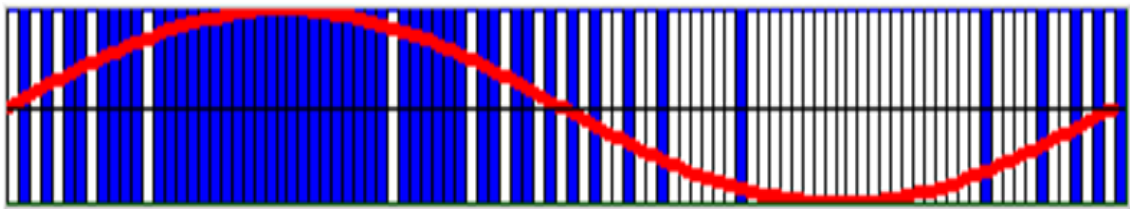

Fig. 1.3: Example of DSM of 100 samples of one period a sine wave. 1-bit samples overlaid with sine wave where logic high (+Vcc) represented by blue and logic low (-Vcc) represented by white [28].

In general, ΔΣ has some advantages versus Δ modulation. The whole structure is simpler:

1) Only one integrator is needed;

2) The demodulator can be a simple linear filter (e.g., RC or LC filter) to reconstruct the signal;

3) The quantizer can have full-scale outputs.

The quantized value is the integral of the difference signal, which makes it less sensitive to the rate of change of the signal.

In conclusion, the major difference between these two techniques lies in the positioning of the integrator within the modulator loop. While the Δ modulator places the integrator into the feedback path, the ΔΣ modulator integrates the signal prior the quantization process. Consequently, the Δ modulator generates a differentiated (or high-pass filtered) version of the input signal while the ΔΣ modulator, by differentiating and integrating in the forward path, passes the signal essentially unchanged through the system. Therefore, the output of the ΔΣ modulator contains a precise, albeit quantization noise corrupted, replica of the input signal. Since the negative feedback inherently differentiates the quantization error sequence, the corresponding noise spectrum is high-pass filtered, with little quantization noise overlapping the low frequency signal spectrum. This spectral discrimination between signal and noise, also referred to as noise shaping, is a unique property of ΔΣ modulators. Depending on the relative signal bandwidth, this feature enables an extremely wide dynamic range and explains the popularity of the ΔΣ approach in the field of high-resolution data conversion.

1.3 TOPOLOGIES OF ΔΣ MODULATORS

Both DT and CT ΔΣ modulators share the same building blocks. The characteristics of the loop filter distinguish one from the other. DT architecture uses a discrete-time loop filter, typically implemented with switched-capacitor

circuits. On the other hand, CT implementation employs a continuous-time loop filter, which may be implemented with g_m-C, active RC, LC, or other filtering elements.

1.3.1 DISCRETE-TIME IMPLEMENTATION

Mathematic analysis of this architecture can result too difficult due to non-linearity of quantizer. It is possible to make it as a linear model, consisting of additive quantization noise $N_q$and a unity gain block and, furthermore, the DAC can be represented with a short circuit if it is ideal. By performing linear analysis, the output Y is a linear combination of the input X and the quantization noise N_q:

$$Y(z) = STF(z) \cdot X(z) + NTF(z) \cdot N_q(z) \tag{1.2}$$

where the noise transfer function (NTF) is given by

$$NTF(z) = \frac{1}{1 + H_{DT}(z)} \tag{1.3}$$

and the signal transfer function (STF)

$$STF(z) = \frac{G_{DT}(z)}{1 + H_{DT}(z)} = G_{DT}(z)NTF(z) \tag{1.4}$$

It can be concluded that the feedback transfer function $H_{DT}(z)$ must be large to reduce the NTF in the band of interest and the forward transfer function $G_{DT}(z)$ must be large as well to make the STF unitary.

Since the loop-filter coefficients in a DT switched-capacitor loop filter are set by capacitor ratios, the clock rate of a DT implementation is essentially arbitrary, up to some specified maximum. The only restriction is that the clock, that sets the f_s value, should be at least equal to twice the maximum signal frequency

multiplied by the OSR. In other words, the clock should be adequate to the input signal.

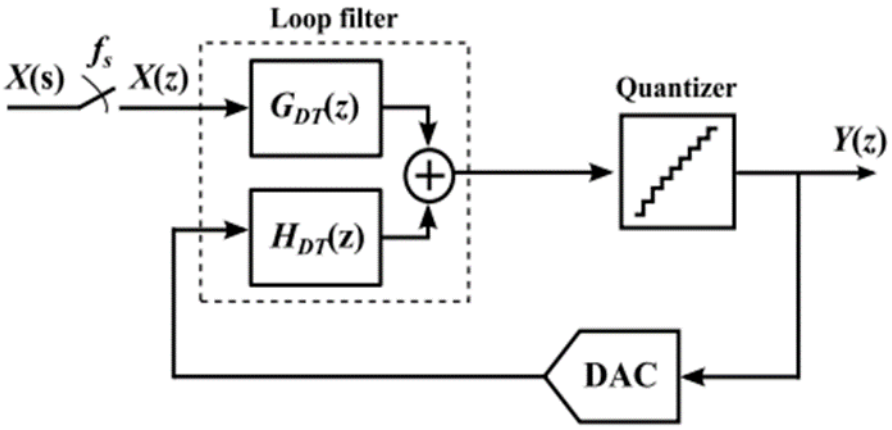

Fig. 1.4: General DT DSM [4].

Although the linear model is simple and intuitive, it fails to predict the stability behaviour of DSMs due to the fact that the gain of the quantizer is signal dependent.

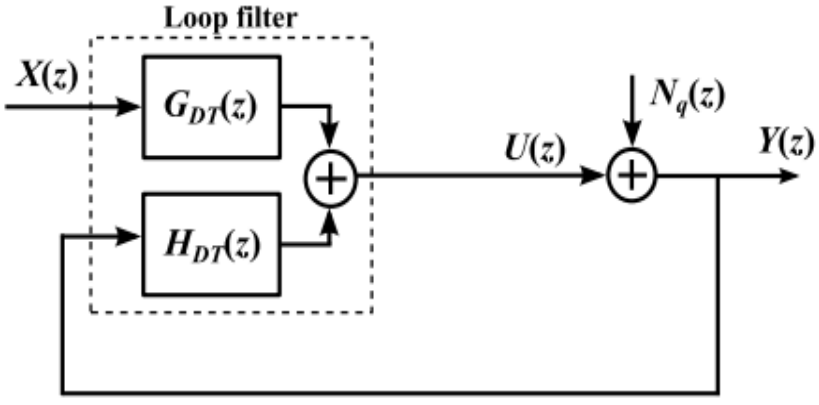

Fig. 1.5: DT linear model [4].

The sigma-delta modulation is based on a negative feedback loop in which a low

quality quantization is performed at a high sampling frequency, and a big amount of the quantization noise is moved into a superior area of the input signal frequency band. Whatever order of modulator's loop filter goes up, noise shaping would be better and SNR would be higher. SNR in output of sigma-delta modulator is dependent on density of output quantization noise. Whatever density of output quantization noise is lower, SNR would be higher. Location of loop filter's zeros and poles in first and second order of sigma-delta modulator are fixed. But, in high order loop filter, by changing the location of zeros and poles, the density of output quantization noise will be changed. The stability requirement also restricts the possible choice of the NTF, especially for higher order loop filter. For a loop filter with an order L, the NTFs are:

$$NTF(z) = (1 - z^{-1})^{L} \tag{1.5}$$

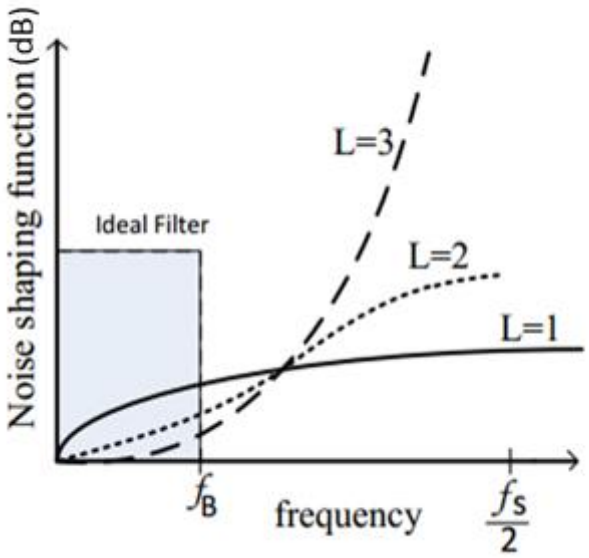

Fig. 1.6: Comparing noise shaping in NTF of first, second and third order of sigma-delta modulator.

To ensure stable operation, the NTF can be optimized through the commonly used Schreier's toolbox in Matlab; in this way, the poles are shifted away from the origin.

1.3.2 CONTINUOUS-TIME IMPLEMENTATION

The earliest implementations of ΔΣ modulators ADCs used CT loop filters but, after the advent of switched-capacitor (SC) circuits, the majority of ΔΣ ADCs have been constructed with SC loop filters. SC filters became popular to their good accuracy and good linearity, in contrast with CT filters. Despite these disadvantages, ΔΣ ADCs employing CT elements in their loop filters are gaining interest due to two important reasons:

1) CT modulators possess inherent anti-aliasing, that simplifies system design by eliminating the anti-alias filter, which typically must precede other ADCs;

2) For low-voltage application, the resistance of the switches in DT DSMs is increased due to the lower overdrive voltage. This issue is avoided in CT DSMs since the loop filter does not require any switches.

1.3.3 CT LINEAR MODEL

The quantizer is a strongly-nonlinear circuit in an otherwise linear system, which makes the behavior of DSMs very complicated to investigate analytically.

However, the basic idea of ΔΣ modulation is easy enough to state: the analog input signal is modulated into a digital word sequence whose spectrum approximates that of the analog input well in a narrow frequency range, but which is otherwise noisy. This noise arises from the quantization of the analog

signal, and the loop filter “shapes” the quantization noise away from the narrow (desired) frequency range.

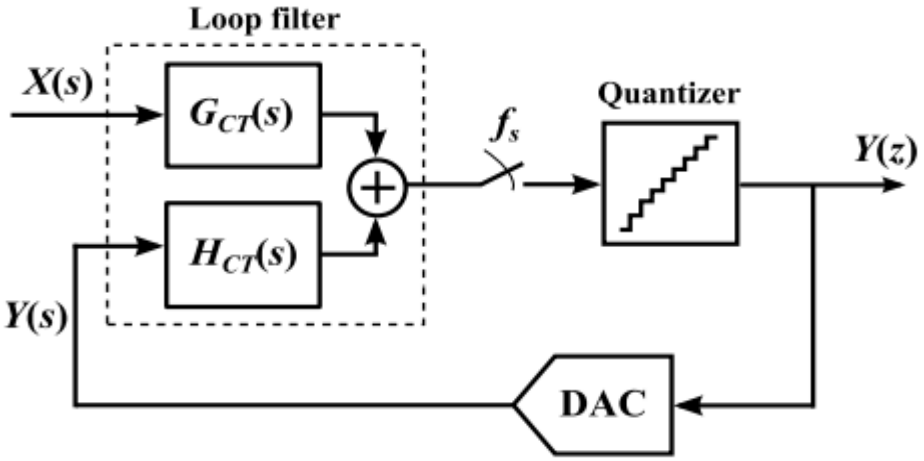

Fig. 1.7: General CT DSM model [4].

An intuitive qualitative understanding of how this happens can be had by linearizing the circuit as shown in Figure 1.8. The quantizer is replaced by an adder and we pretend that the quantization noise is “generated” by an input e, which is independent of the circuit input $X(s)$. It is as though the quantizer knows exactly the right value to add to its input that gives an output value which falls exactly at one of the discrete output levels.

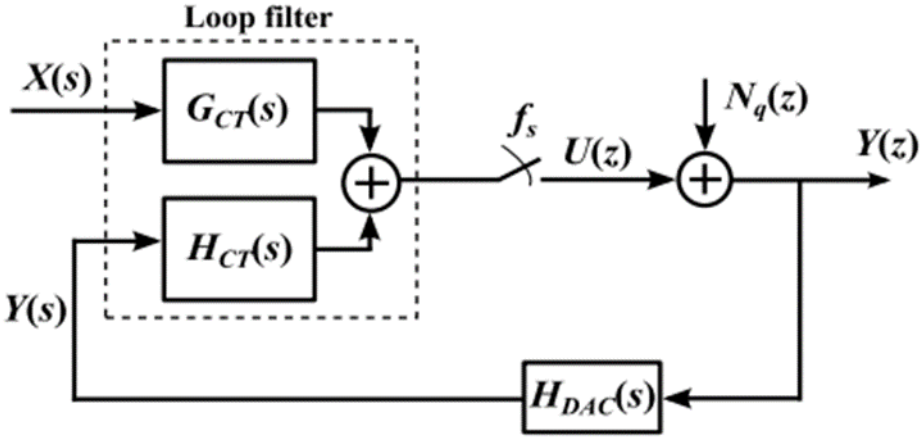

Fig. 1.8: CT DSM linear model [4].

The CT input signal is pre-filtered by the forward transfer function $G_{CT}(s)$ before it is sampled, improving the AA filtering present in CT DSM. The shorthand for the signal after filtering and sampling is given by:

$$[G_{CT}(s)X(s)]^* = \sum_{-\infty}^{\infty} G_{CT}(s + j2k\pi)X(s + j2k\pi) \quad (1.6)$$

The output $Y(z)$ may now be written:

$$Y(z) = NTF(z)[G_{CT}(s)X(s)]^* + NTF(z)N_q(z) =$$

$$= [G_{CT}(s)NTF(e^{sT_s})X(s)]^* + NTF(z)N_q(z) \quad (1.7)$$

where NTF(z) is the same in the equation (1.3) and $z = e^{sT_s}$ with a sampling period of T_s. The CT STF is defined as:

$$STF(s) = G_{CT}(s)\text{NTF}(e^{sT_s}) \quad (1.8)$$

In other words, the input and output spectra are in greatest agreement at frequencies where the gain of H (z) and that of $G_{CT}(s)$, are both large. The NTF (z) is the same as for the DT DSM and is given by (1.5) and z = e^{sTs}, where T_s is the sampling period. As for DT DSMs, the STF depends on the NTF; this effect improves the AA filtering in CT DSMs.

1.4 DISCRETE TO CONTINUOUS TIME CONVERSION

This conversion method uses a mathematical transformation to find a CT-DSM that implements the NTF designed in discrete-time domain. DT modulator has a CT equivalent, which can be found through a transformation between the DT and CT domains. This transformation between DT and CT is called the impulse-invariant transformation because we require the open-loop impulse responses to be the same at sampling instants. The input to the CT open-loop diagram is the

output bit y(n). This is a discrete-time quantity; it only ever changes at sampling instants.

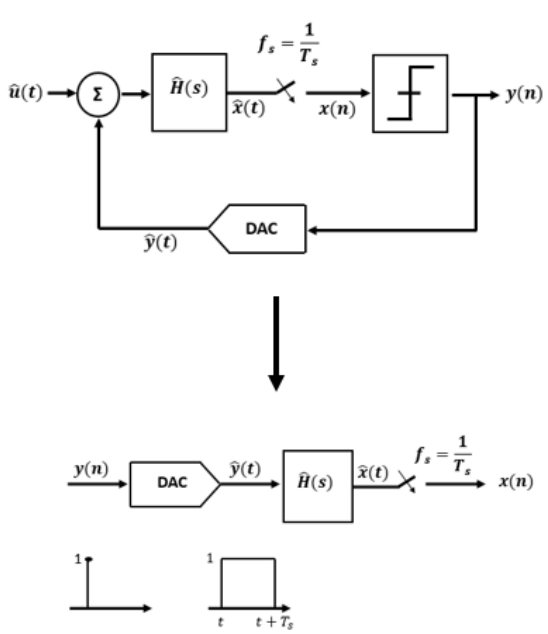

Fig. 1.9a: Open loop CT DSM.

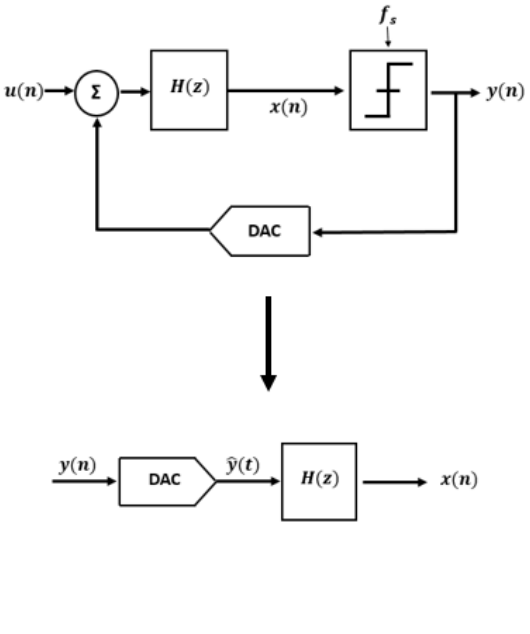

Fig. 1.9b: Open loop DT DSM

The DAC may be thought of as a discrete-to-continuous converter: it takes a sample y(n) and produces some kind of continuous pulse $\hat{y}(t)$, depicted in Figure 1.9a as a full-period rectangular pulse. This pulse is filtered by the loop filter $\hat{H}(s)$, then sampled, where it becomes the discrete-time output of the open-loop system x(n) (as well as being the input to the quantizer). In the DT open-loop diagram, the signals never leave the DT domain.

Note that for both CT and DT loops, the input and output of the open-loop diagrams are both DT quantities. Two DSMs are equivalent when their quantizer inputs are the same at sampling instants; for the CT and DT modulators, this means:

$$x(n) = \hat{x}(t)\Big|_{t = nTs} \tag{1.9}$$

This would be satisfied if the impulse responses of the open-loop diagrams in Figures 1.6a and b were equal at sampling times. This leads to the condition:

$$Z^{-1}\{ H_{DT}(z) \} = L^{-1} \{ H_{CT}(s)\, H_{DAC}(s) \} \Big|_{t = nTs} \tag{1.10}$$

where Z and L indicate the Z and the Laplace transform operators, respectively.

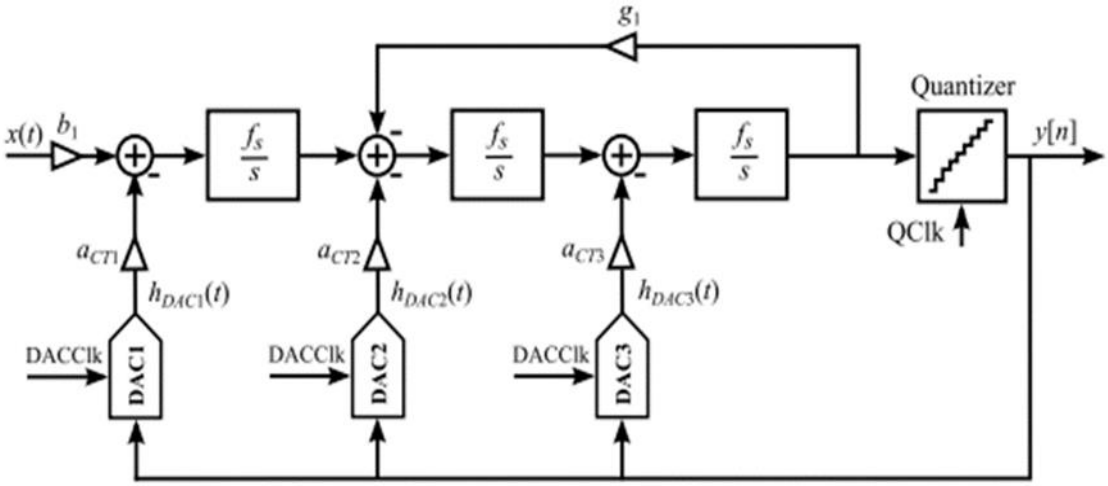

Fig. 1.10: A 3rd-order CT CIFB DSM [4].

The basic architecture of CT CIFB (Cascade of Integrators in Feedback) loop filter in Fig. 1.10 is the same as for the DT loop filter. In CT version the transfer function of integrators is given by I (s) = f_s / s. It is possible to obtain the CT feedback coefficients a_{CT1}-a_{CT3} from DT feedback coefficients a_{DT1}-a_{DT3} by solving (1.4) for DAC pulses h_{DAC1}(t) - h_{DAC3}(t). The CT coefficients are related to the ratio of RC time-constants to the sampling period.

1.5 DAC RECTANGULAR FEEDBACK PULSES

Applications in the communications market are continuously demanding higher bandwidth and resolution, and many works have already proved that CT delta-sigma modulators are a good choice to achieve it. One of the more important drawbacks is their sensitivity to clock jitter. In order to overcome this problem, rectangular pulses have been proposed, being the most commonly used feedback signals.

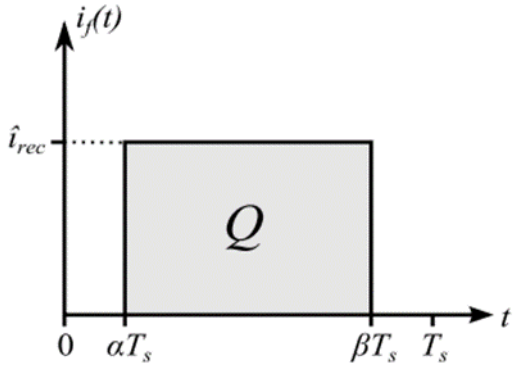

Fig. 1.11: General rectangular pulse [4].

A general rectangular pulse, contained within one sampling period, T_s, is shown in Fig. 1.11, where $\hat{\imath}_{rec}$ is the DAC peak current and Q is the amount of charge transferred during one sampling period . The rectangular feedback DAC pulse can be described in the time domain by the following relationship:

$$h_{rec}(t) = u(t - \alpha T_s) - u(t - \beta T_s) \tag{1.11}$$

By applying the Laplace transform:

$$H_{rec}(s) = \hat{\imath}_{rec} \frac{e^{-\alpha T_s} - e^{-\beta T_s}}{s} \tag{1.12}$$

Replacing this transfer function in (1.10), it is possible to get the value of the feedback coefficients for a general rectangular feedback pulses.

1.5.1 RETURN-TO-ZERO FEEDBACK

$\beta - \alpha < 1$ is the characteristic of this kind of feedback pulse, which is referred to as return-to-zero as the DAC current return to zero at βT_s.

The most commonly used RZ feedback pulse is with $\beta - \alpha = 0.5$, therefore the pulse has a duty cycle of 0.5.

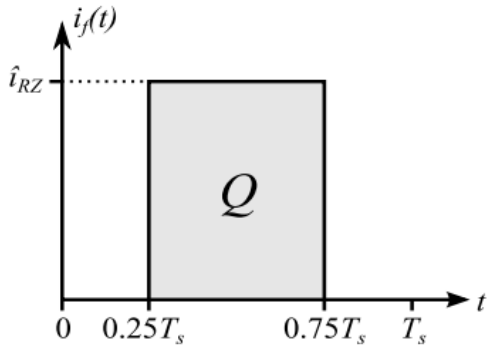

Fig. 1.12: RZ pulse [4].

1.5.2 NONRETURN-TO-ZERO FEEDBACK

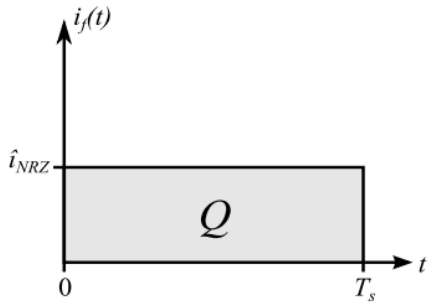

Fig. 1.13: NRZ pulse [4].

The DAC current is high during the completely sampling period, therefore this rectangular pulse is obtained if $\alpha = 0$ and β=1. It can be noted from the Fig. 1.13 that the peak current for NRZ case is reduced by half compared to the RZ case, since the transferred charge Q for two equivalent modulators, respectively employing NRZ and RZ feedback, is the same, therefore the current in RZ case must be double to transfer the same charge in $T_s/2$. This means that the CT feedback coefficients are in the following relationship:

$$a_{CT1,RZ} = 2a_{CT1,NRZ} \tag{1.13}$$

The low peak current in NRZ feedback allows to have relaxed integrator amplifier slew-rate requirements.

2. Design of a ΔΣM for ultra-low-power radios

2.1 MOTIVATION

The application of delta-sigma modulation data converter is getting extended rapidly to new emerging applications such as wired and wireless communications, which have expanded into many areas of our life. One of the great advantages of delta-sigma modulation data converter is that the accuracy requirements for its analog circuitry are greatly relaxed thanks to oversampling and noise shaping. This popularity comes from its inherent high resolution and low power characteristics. In fact, in today's modern world, one of the most critical challenge is the power consumption. Size and power consumption are two critical features in portable battery-powered applications. Otherwise, acceptable components can be designed out of portable systems based on deficiencies in these two features alone. Everybody desires smaller, more compact mobile phones, MP3 players, personal digital assistants (PDAs), and digital cameras, with increased time between battery charges or replacement. For semiconductor manufacturers, this translates into a requirement for lower power ICs with high performance and the same features in ever-smaller packages. A good level of portability can be realised by addressing the design issues of the

radio frequency (RF) transceiver, which is the most critical component in ultra-low-power (ULP) wireless applications. To achieve low power operation, the transceiver should only be activated when sending/receiving data.

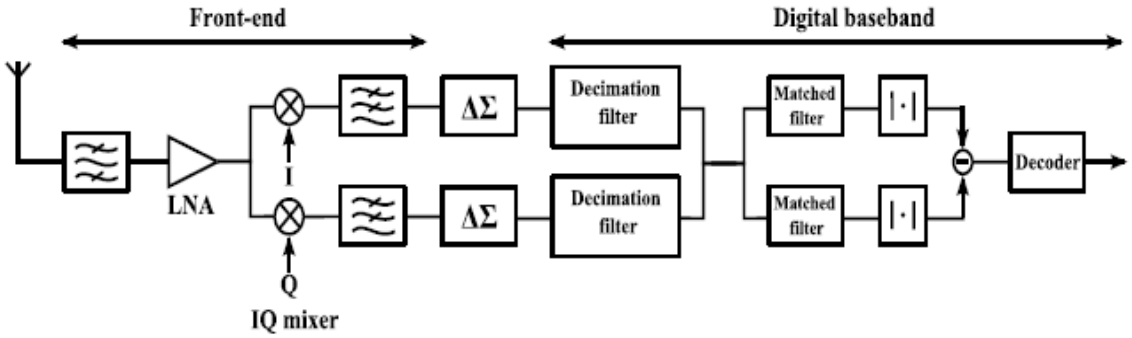

Fig. 2.1: Receiver chain [37].

The architecture of the receiver chain, shown in Fig. 2.1, consists of a direct conversion front-end followed by the ΔΣ ADCs and the digital baseband. The chosen modulation is frequency shift keying, for which transmitters can be realized with high efficiency and low spurious emissions. To minimize the size of the radio transceiver it should be realized as a single chip in nanometer complementary CMOS technology. A direct-conversion architecture is employed, which has benefits in power consumption but problems with dc-offsets and 1/f noise. Matched filters with dc-notches can be used for demodulation, eliminating dc-offsets and suppressing 1/f noise. The target frequency band is 2.45-GHz, and since this is a popular band for wireless communication systems, immunity to interfering signals is critical. Therefore, continuous-time delta–sigma ADCs are used, providing an attractive dynamic-range/power trade-off and inherent anti-alias filtering. To further improve

linearity, the ADCs are preceded by mixers with passive output filtering. High selectivity is obtained by sharp filtering in the digital domain, and by using a low phase noise LC-oscillator for the local oscillator. A decoder is used to increase the receiver sensitivity, and to reduce the power consumption.

Power consumption is an important limitation to analog-to-digital converters, since it limits the average data rate and the distance between receiver and transmitter. This is mainly due to the minimum transmitted energy per information bit needed to obtain reliable communication over a certain distance. But the ADC is also a mandatory component in an RF transceiver.

The low-power characteristic of the DSM is due to its operation based on a negative feedback system, which combines two the important concepts: oversampling and noise shaping.

Traditionally DSMs have been implemented with discrete-time (DT) circuits, implemented using switched-capacitor while in recent years, they have been used in communications chips where inherent anti-aliasing provide by the continuous-time (CT) architecture is very useful. Delta-sigma ADCs are oversampling ADCs that sample the signal at much higher rates than a Nyquist rate. For a signal with maximum bandwidth, f_b, the Nyquist theorem states that input must be sampled at a rate > $2f_b$. The ratio of sampling frequency (f_s) to twice the signal bandwidth ($2f_b$) is called the oversampling ratio (OSR). In a discrete-time delta-sigma ADC, sampling of the input signal $x(t)$ occurs prior to the loop filter (Fig. 2.2). The loop filter $H(z)$ is discrete time, implemented using switched-capacitor

integrators. The quantizer generally is low resolution, somewhere from 1 to 5 bits. The loop filter shapes the quantization noise out of the baseband to higher frequencies.

The feedback digital-to-analog converter (DAC) is also discrete-time implemented with switched-capacitor techniques. The loop filter does not shape errors in the feedback DAC, requiring the DAC to be as good as the overall ADC. The output of the quantizer is low-pass filtered by a decimation filter, which outputs the data at the rate of $F_{DR.}$

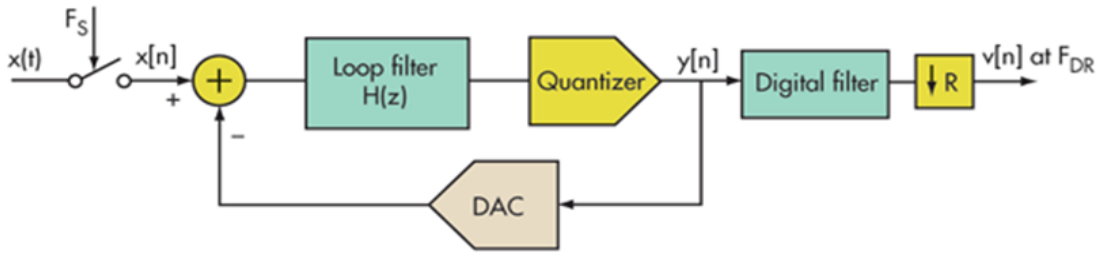

Fig. 2.2: DT DSM [28].

In a continuous-time delta-sigma ADC, the principle of noise shaping and oversampling remains the same as its discrete-time counterpart. The key difference is where the sampling operation takes place. In the continuous-time design, input sampling takes place just before the quantizer.

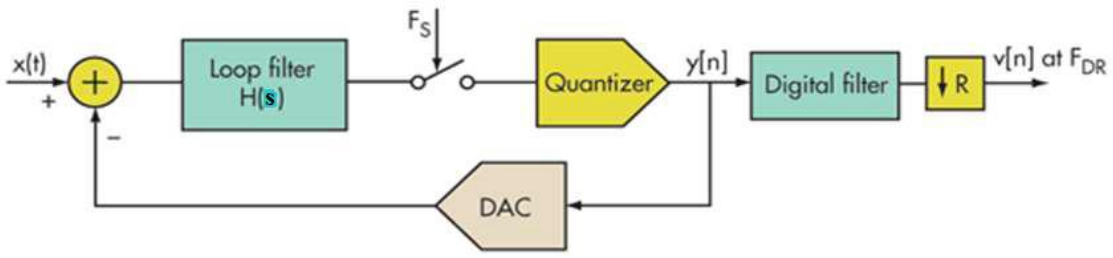

Fig. 2.3: CT DSM [28].

CT DSMs have received increasing attention due to the following reasons: 1) Relaxed amplifier requirements compared to DT DSMs resulting in low power consumption. 2) Implicit anti alias (AA) filtering which is especially beneficial in radio applications. The loop filter is usually the largest power consumer in a CT DSM due to the use of operational amplifiers. In this dissertation, the loop filter will be implemented with fewer operational amplifiers while still maintaining the desired resolution. An attempt has also been made to decrease the power consumption in the quantizer. Furthermore, the high clock jitter sensitivity usually associated with CT DSMs has also been considered.

In a DSM, the loop filter is the block with more power consumption due to the presence of the operational amplifiers, which implement the integrators. It is usually designed by using CIFB structure, where the number of integrators is determinate by the order of the loop filter. In this thesis, a second-order fully-differential loop filter has been implemented.

2.2 CONVENTIONAL SAB POWER SAVING TECHNIQUES FOR THE LOOP FILTER

The loop filter is the main block of a CT ΔΣ modulator. It dissipates a significant amount of the total energy and occupies a major portion of the modulator die area. There are two types of commonly used continuous-time active integrators to realize a loop filter: R-C integrators and Gm-C integrators. Active-RC based loop filters have the widest dynamic range, but they consume more power due to the larger number of active blocks. On the other hand, passive networks do not

consume power, but they introduce an attenuation factor for the in-band signals, which amplifies the internal electronic noise, and non-idealities of the loop filter blocks referred to the modulator input.

As an alternative, Single Amplifier Biquad (SAB) networks, which are a combination of active and passive filters and use just one operational amplifier instead of two, can be used in the modulator loop filter to reduce the power consumption, to simplify design process and to reduce distortions. SAB-based loop filters have all the benefits of both active and passive filters.

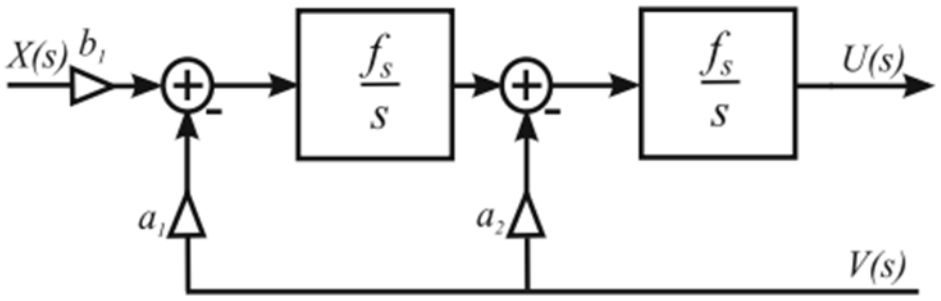

Fig. 2.4: Block diagrams of a 2nd-order CIFB loop filter [4].

2.2.1 REQUIREMENTS OF SAB

The input signal must be applied to the virtual ground of the operational amplifier; otherwise, the front-end DAC signal cannot be subtracted from the input signal. If this feature is not verified, SAB network cannot be used in the ADC front-end to reduce the power consumption of the most power hungry part of the ADC. Another requirement is related to SAB network transfer function about first-order Laplace term in the denominator. This term creates a leakage effect in the modulator final performance by shifting the NTF optimized zeros

from the imaginary axis to the left half plane. Fortunately, this undesired effect can be attenuated by choosing suitable values for resistors.

Finally, when either of these SAB techniques are applied, they require high gain bandwidth (GBW) amplifiers. The high GBW amplifiers reduce the accumulated delay in the loop filter from the ADC front-end to the input of the quantizer block that can cause modulator instability.

2.3 SINGLE-AMPLIFIER LOOP FILTER

The feedback transfer function of a 2nd-order loop filter implemented with the CIFB structure shown in Fig. 2.4, from $V(s)$ to $U(s)$is given by,

$$H(s) = -\frac{a_1 + a_2 T_s s}{(T_s s)^2} \tag{2.1}$$

where poles are at the origin.

The aim is to get an active network consisting of one active element and a 2nd-order passive RC network, which implements the same transfer function as in (2.1). The same result in not achievable with conventional 2nd-order, like a well-known Sallen-key filter, since its transfer function is different from the above one.

The 4-terminal RC network, in Fig. 2.5, can be characterized by its short circuit admittances.

The transfer function of this network, assuming that the operational amplifier is ideal, is:

$$H(s) = \frac{V_3}{V_1} = -\frac{y_{12}}{y_{32}} \tag{2.2}$$

where

$$y_{12}(s) = \frac{I_1}{V_2}\Big|_{V_1,\, V_3=0}, \quad y_{32} = \frac{I_3}{V_2}\Big|_{V_1,\, V_3=0} \tag{2.3}$$

are the short circuit admittances.

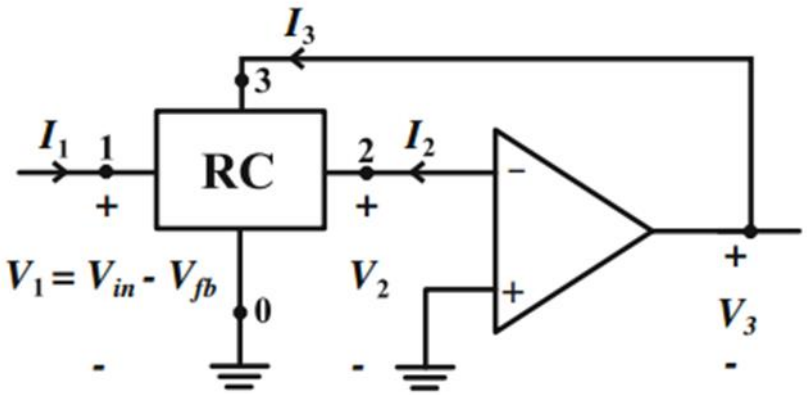

Fig. 2.5: General Single-Amplifier Network [7].

2.3.1 LOOP FILTER IMPLEMENTATION

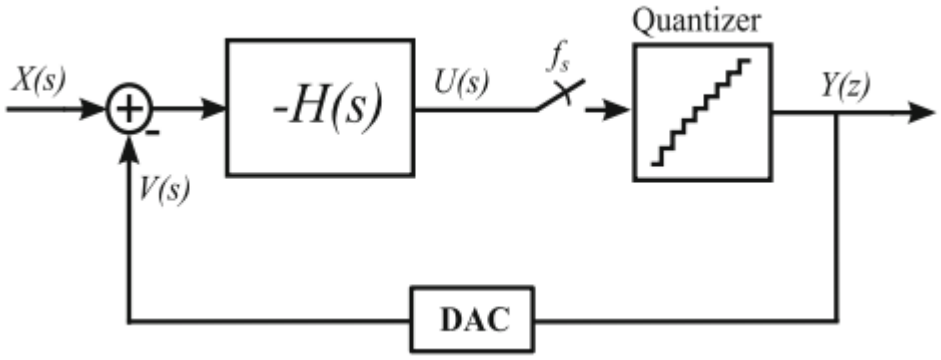

Fig. 2.6: CT DSM Modulator [4].

The task is to synthesize the RC network to get the same transfer function in (2.1), because, when the loop filter is used in DSM, the input signal to the RC network is given by the difference between the input signal to the modulator and

the feedback signal. Thus, the implementation of additional operation is also necessary.

2.3.2 SYNTHESIS OF THE RC NETWORK

The denominator in (2.1) contains the term $(T_s s)^2$, which is the transfer function of a second order differentiator. This means that the term $(T_s s)^2$ must be present in one of the short circuit admittances. Starting from a 1st-order RC network, which gives a transfer function

$$D(s) = \frac{V_R}{V_2} = \frac{R_1 Cs}{1+R_1 Cs} \tag{2.4}$$

It is possible to get the short circuit admittance y_{32} adding a capacitance C, which contributes a second differentiator.

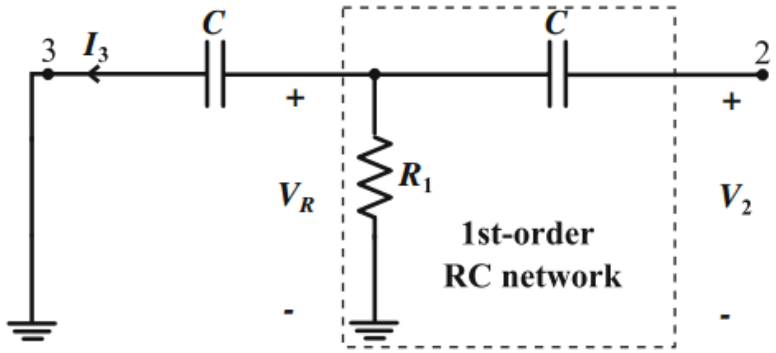

Fig. 2.7: RC network implementing $y_{32}(s)$ [7].

The short-circuit admittance y_{32} of the above circuit is given by:

$$y_{32} = \frac{I_3}{V_2} = -\frac{(R_1 Cs)^2}{R_1(1+2R_1 Cs)} \tag{2.5}$$

where the numerator implements the 2nd-order differentiator, which, in the complete transfer function $H(s)$, will end up in the denominator. The numerator

of (2.5) ends up in the denominator of (2.1), but it is undesired, thus it needs to be cancelled by $y_{12}(s)$. It is possible modifying the RC network.

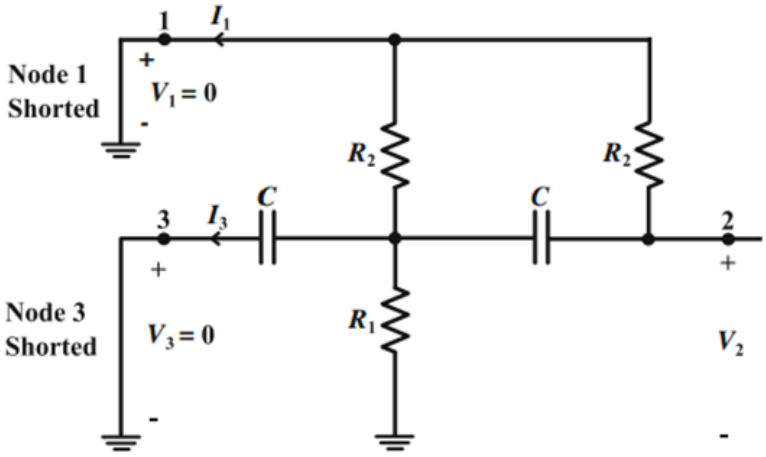

Fig. 2.8: Modified RC network that implements both $y_{12}(s)$ and $y_{32}(s)$ [7].

The short-circuit admittance $y_{12}(s)$ of the modified RC network is

$$y_{12}(s) = -\frac{\frac{R_1}{R_2^2}(R_1+R_2+3R_1R_2Cs)}{\frac{R_2}{R_1}(R_1+R_2+2R_1R_2Cs)} \tag{2.6}$$

Substituting (2.6) and (2.5) into (2.2), the final transfer function of the single amplifier network will be:

$$H(s) = -\frac{R_1}{R_2^2}\frac{R_1+R_2+3R_1R_2Cs}{(R_1Cs)^2} \tag{2.7}$$

It is convenient to use a single R for all resistors and defining, then, defining $R_1 = n_1R$ and $R_2 = n_2R$. The value of R is determined according to noise and power consumption requirements, while n_1 *and* n_2 are used to implement the desired loop filter coefficients. Substituting the new definition for two resistors into (2.7),

$$H(s) = -\frac{\frac{1}{n_2^2}\left(1+\frac{n_2}{n_1}\right)+\frac{3}{n_2}sRC}{(sRC)^2} \tag{2.8}$$

where the time constant RC equals the sampling period T_s and n_1 and n_2 can be calculated by the comparison between numerators of (2.8) and (2.1).

$$\begin{cases} a_1 = \frac{1}{n_2^2}\left(1+\frac{n_2}{n_1}\right) \\ a_2 = \frac{3}{n_2} \end{cases} \qquad \begin{cases} n_1 = \frac{3a_2}{9a_1 - a_2^2} \\ n_2 = \frac{3}{a_2} \end{cases} \tag{2.9}$$

2.3.3 IMPLEMENTATION OF THE ADDITION OPERATOR

Until now, the voltage V_{in} and V_{fb} were considered like only voltage source but, in pratical, they are two separate voltages and, therefore, they need to be applied to the RC network separately. Thus, the RC network needs to be transformed like in Fig. 2.9. In the right sub-circuit, the transformation is linear because the resistor is connected to the virtual ground of the operational amplifier; for this reason, V_{in} and V_{fb} can be applied in parallel without changing the transfer function of the loop filter. The situation for the left-sub-circuit is different, since its transformation is not linear, being not connected to a virtual ground. In the new left sub-circuit n_1R is represented by the parallel $n_2R \,||\, KR$, whence

$$K = \frac{n_1 n_2}{n_1 + n_2} \tag{2.10}$$

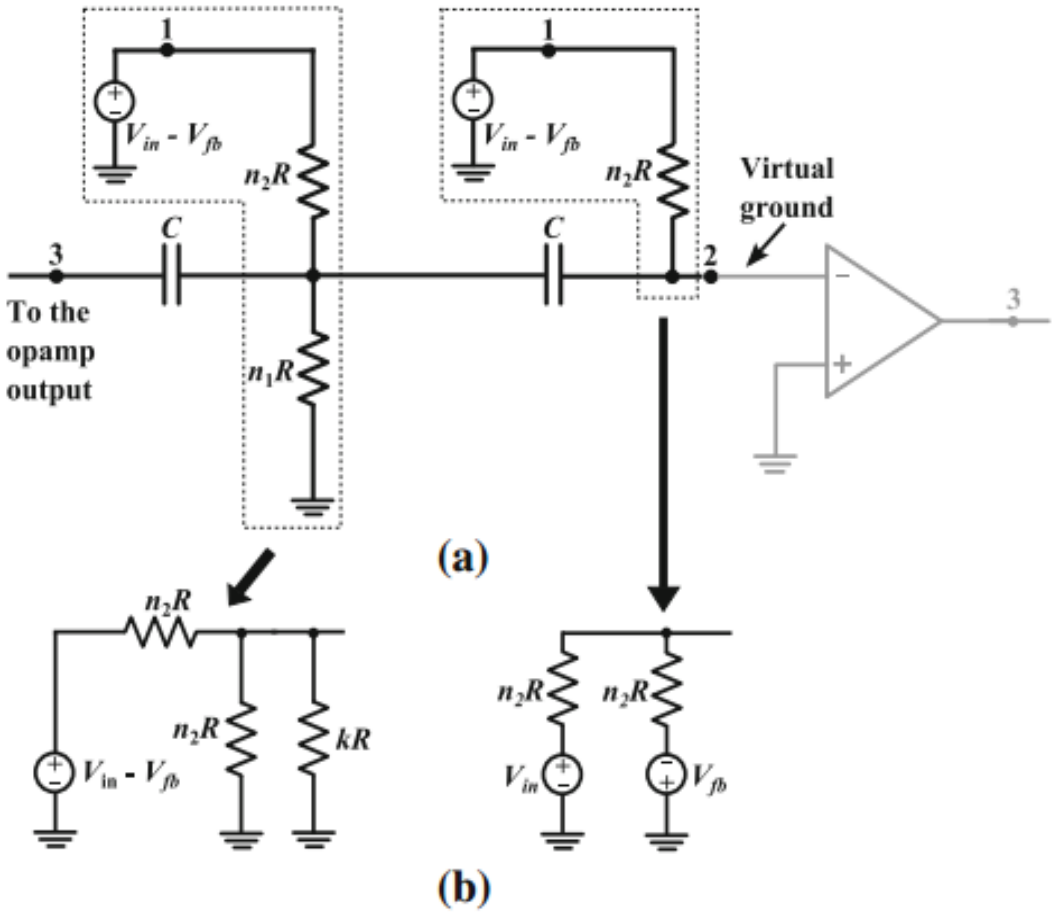

Fig. 2.9: a Loop filter with voltage $Vin - Vfb$ provided. **b** Transformations of the two sub-circuits [7].

2.3.4 FURTHER TRANSFORMATION OF THE LEFT SUB-CIRCUIT

This sub-circuit has a suitable Thévenin equivalent, as shown in Fig. 2.10, which separates the two voltage signals as desired.

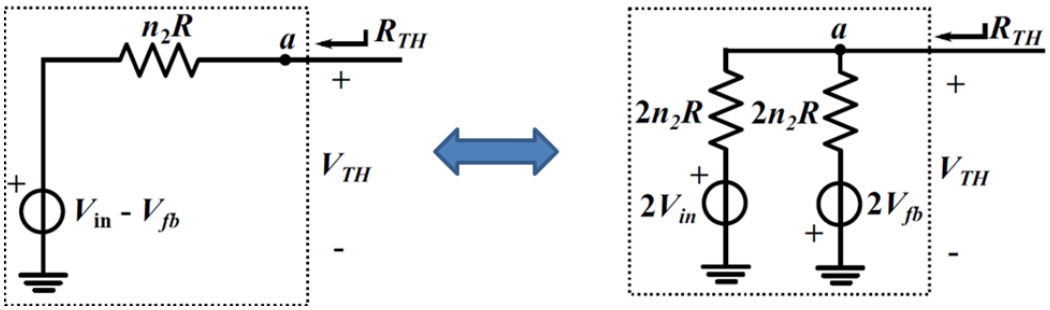

Fig. 2.10: A straightforward way of transforming the right sub circuit [12].

This transformation is problematic since now the multipliers in front of V_{in} and V_{fb}, must be implemented. Furthermore, twice as large resistors are required, resulting in different feedback DACs for left and right sub circuits. In order to avoid these problems, add a resistor n_2R between node a and ground. This resistor should not affect the overall transfer function.

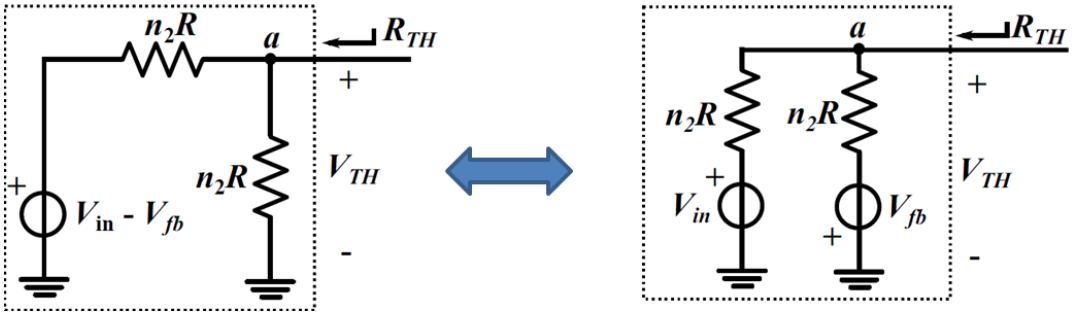

Fig. 2.11: Transformation using Thévenin equivalent [12].

The transformation does not result in any multipliers and the resistors of n_2R are the same for both sub-circuits.

The semi-final loop filter after all transformation in shown in Fig. 2.12. The two resistors connected to the feedback signal V_{fb}, are split into several parallel unit resistors when multi-bit DACs are used.

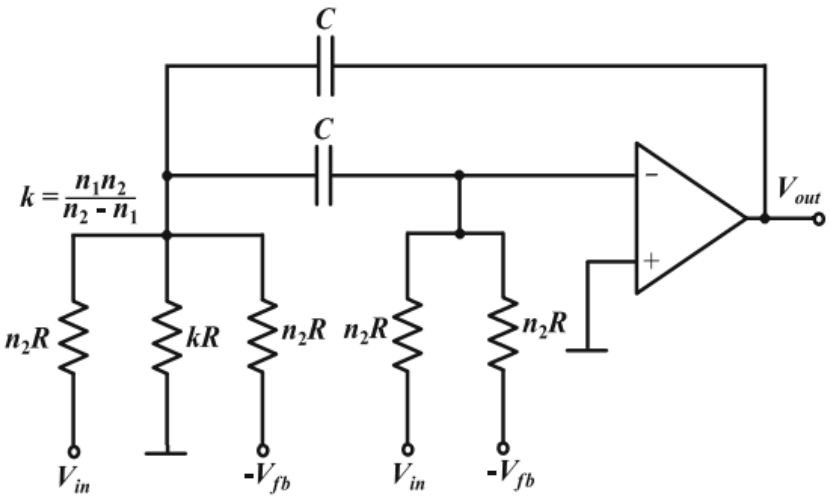

Fig.12: Semi-final loop filter [7].

2.4 STF AND ANTI-ALIASING

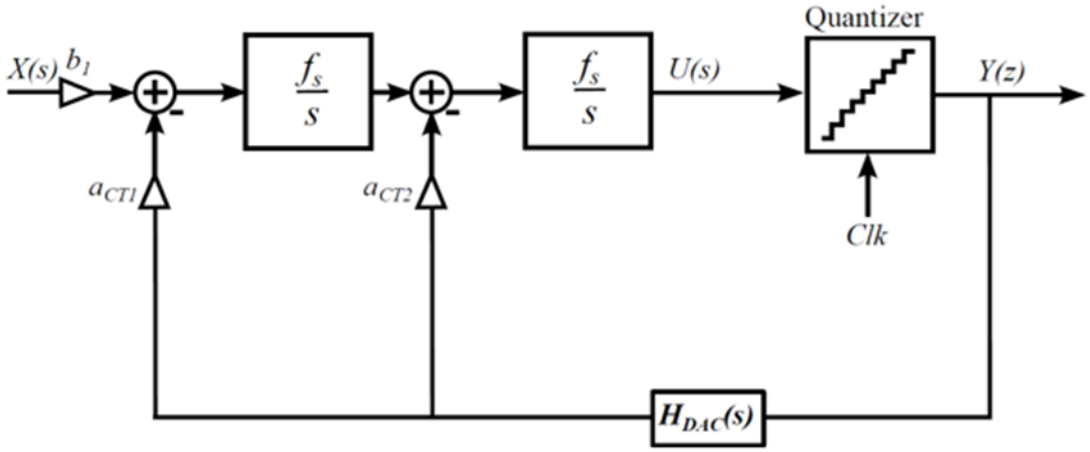

Fig. 2.13: ΔΣ modulator with a2nd order CIFB loop filter [4].

Considering the following design case,

- ✓ Continuous time ΔΣ-modulator
- ✓ 2nd order loop filter
- ✓ 4-bit quantizer
- ✓ NRZ pulses DACs
- ✓ Sampling frequency f_s = 16 MHz
- ✓ Bandwidth f_{bw} = 500 kHz
- ✓ OSR = $f_s/2f_{bw}$ = 16

when NRZ DACs are used, α = 0 and β = 1.

$$NRZ = \begin{cases} a_{CT1} = 1 \\ a_{CT2} = 1{,}5 \end{cases} \quad (2.11)$$

This results into the following CT feedback path transfer function:

$$H_{CT}(s) = -\frac{1+1.5sT_s}{(sT_s)^2} \quad (2.12)$$

In Fig. 2.13, the forward coefficient b_1 is 1 which yields the following double integrating forward path CT transfer function:

$$G_{CT}(s) = \frac{b_1}{(sT_S)^2} = \frac{1}{(sT_S)^2} \tag{2.13}$$

The forward transfer function $G_{CT}(s)$ affects the STF in different way in the CIFB architecture, in Fig. 2.13, and in SAB loop filter. In the first case, the forward path transfer function $G_{CT}(s)$ and the feedback path transfer function $H_{CT}(s)$ are determined, respectively, by (2.13) and (2.12),

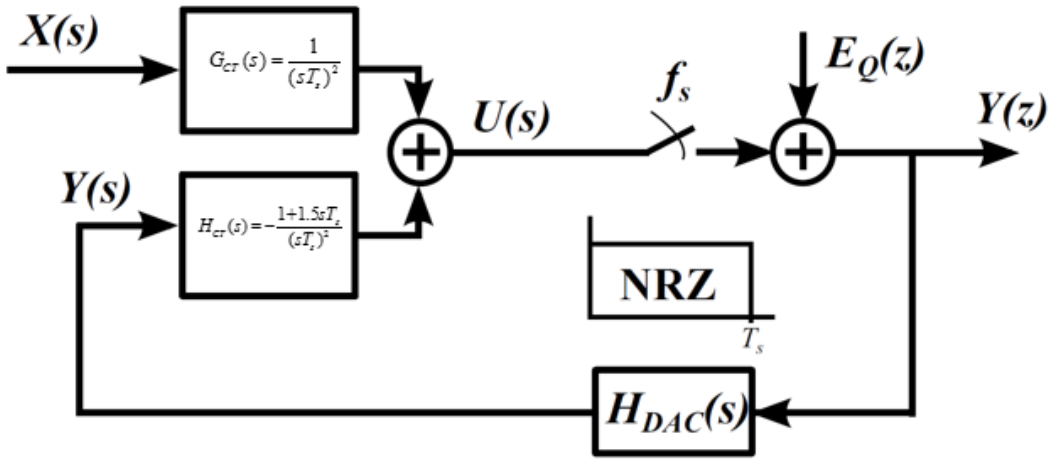

Fig. 2.14: GH-model of the loop filter [4].

where

$$NTF = (1 - z^{-1})^2 \tag{2.14}$$

$$STF = G_{CT}(s)NTF(e^{sT_S}) \tag{2.15}$$

The choice of a low sampling frequency (16 MHz) is due to the design of the NTF considering an OSR = 16. It achieves an SQNR of 70 dB, which gives 10dB margin for noise and distortion, where targeted SNR is minimum of 60 dB.

The SAB loop filter, instead, can be regarded as a direct implementation of the desired feedback transfer function in (2.1), as in Fig. 2.15. In this case, $G_{CT}(s) = H_{CT}(s)$, which is always a double integrating function, but with a zero (2.12).

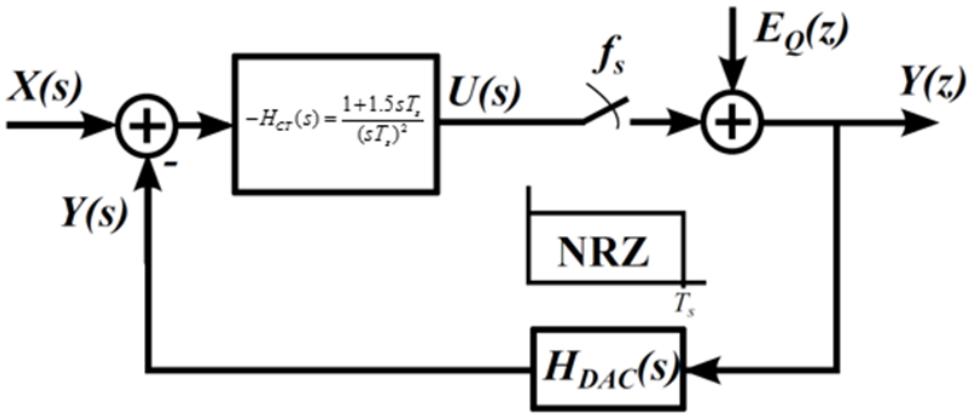

Fig. 2.15: ΔΣ modulator with a 2nd-order SAB loop filter [12].

The NTF and the STF are obtained in the following way:

$$NTF = (1 - z^{-1})^2 \tag{2.16}$$

$$STF = H_{CT}(s)NTF(e^{sT_s}) \tag{2.17}$$

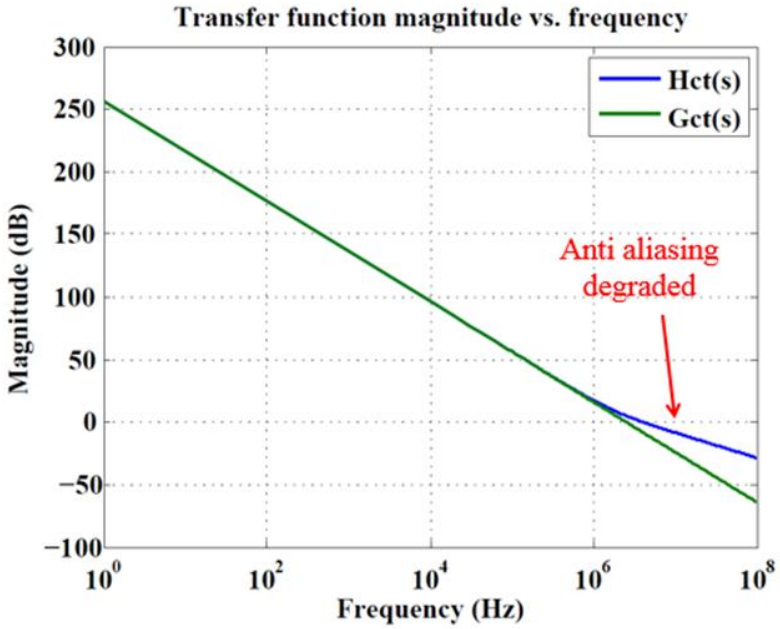

Fig. 2.16: Comparison between transfer function of 2nd-order CIFB and SAB loop filter [12].

$G_{CT}(s)$ is an ideal double integrating transfer function, while $H_{CT}(s)$ is a double integrating transfer function with one zero. A modulator with $H_{CT}(s)$ as loop filter will have a worse anti-aliasing performance.

If the STF pre-filtered by $G_{CT}(s)$, (2.15), and the other one prefiltered by $H_{CT}(s)$, (2.17), are plotted, it is evident that the attenuation for the STF pre-filtered by $H_{CT}(s)$ is degraded compared to the STF pre-filtered by $G_{CT}(s)$. Before plotting them, calculating their equations is necessary:

$$|STF_1(j2\pi f)| = \left|G_{CT}(s = j2\pi f)NTF\left(e^{j2\pi f T_s}\right)\right| = \left|b_1\left(\frac{1-e^{-j2\pi f T_s}}{j2\pi f T_s}\right)^2\right| =$$

$$= b_1\left(\frac{\sin\left(\pi\frac{f}{f_s}\right)}{\pi\frac{f}{f_s}}\right)^2 \tag{2.18}$$

$$|STF_2(j2\pi f)| = \left|H_{CT}(s = j2\pi f)NTF(e^{j2\pi f T_s})\right|$$

$$= \left|-\frac{(a_{CT1} + a_{CT2} s T_s)(1 - e^{-j2\pi f T_s})}{(sT_s)^2}\right|$$

$$= \sqrt{\left(a^2{}_{CT1} + \left(2a_{CT2}\pi\frac{f}{f_s}\right)^2\right)}\left(\frac{\sin\left(\pi\frac{f}{f_s}\right)}{\pi\frac{f}{f_s}}\right)^2 \tag{2.19}$$

where STF_1 and STF_2 are respectively the STF pre-filtered by $G_{CT}(s)$ and the STF pre-filtered by $H_{CT}(s)$.

The DC gain of the STFs can be obtained as:

$$\lim_{f\to 0}|STF_1(j2\pi f)| = b_1 \tag{2.20}$$

$$\lim_{f\to 0}|STF_2(j2\pi f)| = a_{CT1} \tag{2.21}$$

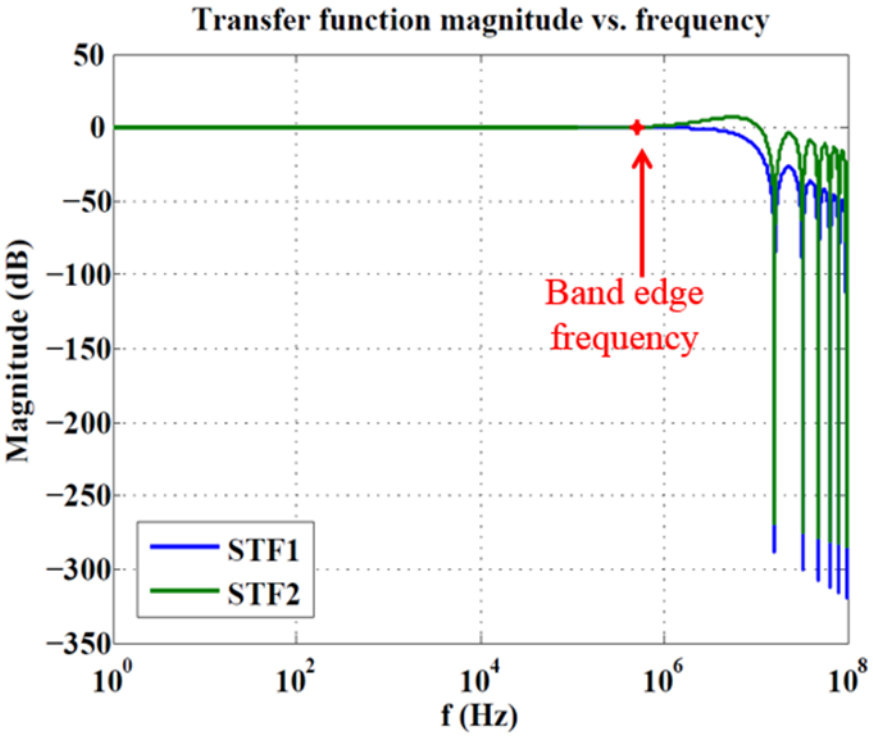

Fig. 2.17: STF_1 and STF_2 [12].

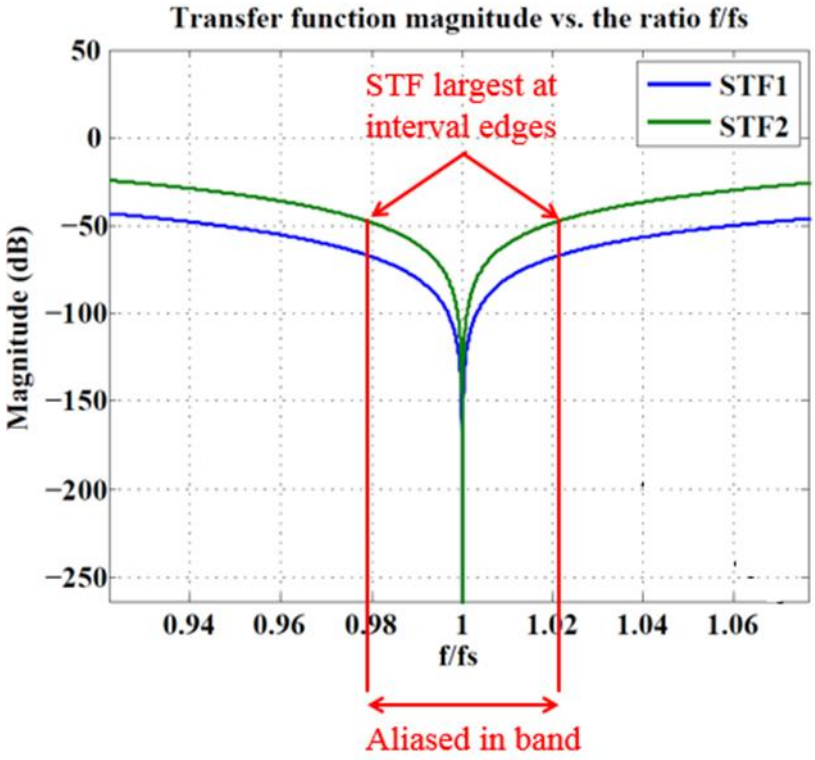

Fig. 2.18: The plot zoomed at the first aliasing zone [12].

The STF is 1 in band always for the STF_1 and, only for NRZ feedback pulse case, for the STF_2, since for RZ feedback pulse, $a_{CT1} = 2$, as expressed in (1.13).
Out of-band STF2 shows peaking and the magnitude is larger than 0 dB for some frequencies. All the components inside the frequency intervals
$nf_s - f_{bw} \leq f \leq nf_s + f_{bw}$, with $n = 1,2,3, ...$, are folded in band. n represents the number of the aliasing zone. Due to the term in front of the sinc function, the attenuation around nf_s for STF_2 is degraded compared to STF_1.

It is possible to suppress the aliasing applying an input signal inside any of the aliasing zones. In a CT ΔΣ modulator an attenuated version of this signal will be aliased in band. The attenuation of the aliased signal in dB is defined as the aliasing suppression. This is the same as the magnitude of the STF in the aliasing zones since the signal is first attenuated by the STF before it is sampled and thereby aliased.

$$AA = 20log_{10}|STF(j2\pi f)|, \qquad nf_s - f_{bw} \leq f \leq nf_s + f_{bw} \tag{2.22}$$

Aliasing suppression is worst at the edges of the aliasing zones $nf_s \pm f_{bw}$. Calculating AA for STF_1 and $STF2_2$:

$$AA_1 = 20log_{10}|STF_1(j2\pi(nf_s \pm f_{bw}))| =$$
$$= 40log_{10}\left(\sqrt{b_1}sinc\left(1 \pm \frac{1}{2nOSR}\right)\right) \tag{2.23}$$

$$AA_2 = 20log_{10}\left|STF_2\left(j2\pi(nf_s \pm f_{bw})\right)\right| =$$

$$= 10log_{10}\left(a^2{}_{CT1} + 4a^2{}_{CT2}\pi^2\left(1 \pm \frac{1}{2nOSR}\right)^2\right) +$$

$$+ 40log_{10}\left(sinc\left(1 \pm \frac{1}{2nOSR}\right)\right) \quad (2.24)$$

where, using the relation $OSR = f_s/2f_{bw}$, the frequency ratio f/f_s at the edges is found as:

$$\frac{f}{f_s} = \frac{nf_s \pm f_{bw}}{f_s} = \frac{2nf_{bw}OSR \pm f_{bw}}{2nf_{bw}OSR} = 1 \pm \frac{1}{2nOSR} \quad (2.25)$$

The magnitude of the STF at the edges of the aliasing zones for $n > 1$ is always less than at the edges of the aliasing zone for $n = 1$. This is also seen from the expression in (2.25), which is largest for $n = 1$. For the aliasing zone edges, which are equally spaced around any minima $f = nf_s$, the magnitude of the STF at the left edge is always slightly larger than for the right edge. It is possible to conclude that the worst possible aliasing suppression occurs at the left edge of aliasing zone 1, at $f = f_s - f_{bw}$, where the frequency ratio is given by:

$$\frac{f}{f_s} = 1 - \frac{1}{2OSR} \quad (2.26)$$

As expected, looking at equations (2.23) and (2.24), the aliasing suppression of STF_2 is significantly worse than for STF_1, being, for NRZ case, $b_1 = 1$, $a_{CT1} = 1, a_{CT2} = 1.5$.

Seeing (2.13), for the NRZ case, the aliasing suppression is better compared to the RZ case. Thus, if $a_{CT1} > 1$, the suppression is degraded, since noise is amplified by the STF

The STF and aliasing suppression for a general L[th]-order CT ΔΣ-modulator are given by:

$$|STF(j2\pi f)| = b_1 sinc^L\left(\frac{f}{f_s}\right) \tag{2.27}$$

$$AA = 20Llog_{10}\left(\sqrt[L]{b_1}sinc\left(1-\frac{1}{2OSR}\right)\right) \tag{2.28}$$

It can be concluded that the aliasing suppression improves with increasing loop filter order and increasing OSR.

The anti-aliasing filter can be removed in a CT modulator, since it provides an inherent antialiasing filtering. In [21] the anti-aliasing performance was measured by applying a large signal around the sampling frequency and checking at which frequency the aliased and filtered version of the signal will appear, sweeping the frequency from $f_s - f_{bw}$ to $f_s + f_{bw}$. The anti-aliasing suppression was calculated as the ratio between the input signal amplitude and the amplitude of the aliased signal.

2.5 CONTROLLING STF

The STF is set by the G_{CT} (s) and the NTF, while the NTF is set by H_{CT} (s). Therefore, the NTF and STF can be designed independently. This is true only considering the case in Fig. 2.14.

If the transfer function of the loop filter is given by (2.1), the STF cannot be controlled independently of the NTF, which will completely determine the behaviour of the STF. This can make STF in band larger than 1, which reduces the maximum input signal range to the modulator. Furthermore, the anti-

aliasing is degraded. The value of the STF depends on the kind of the feedback. In NRZ feedback case, where $a_{CT1} = 1$ and $a_{CT2} = 1.5$, the STF in band is $|STF(0)| = 1$, as desired. For delay RZ-feedback, $a_{CT1} = 2$ and $a_{CT2} = 3$, therefore $|STF(0)| = 2$.

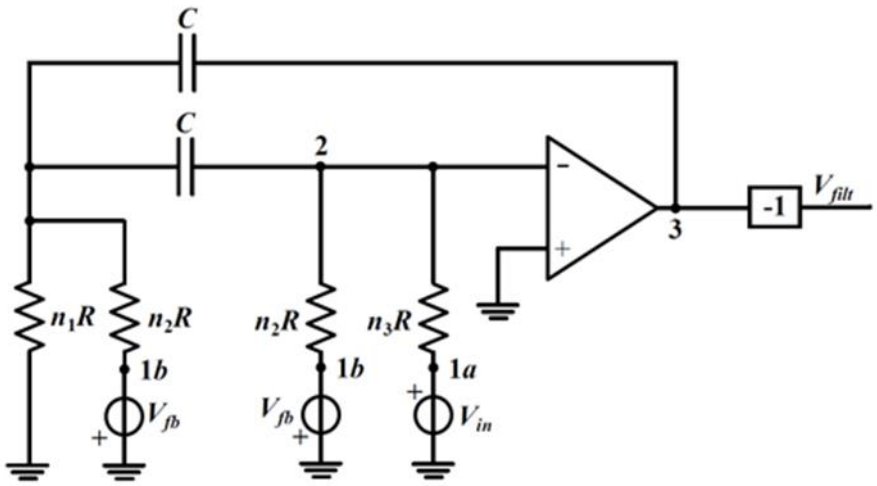

Fig. 2.19: Modified loop filter.

```
clear all
L = 2;                                  % Order of the loop filter
opt = 0;                                % Flag for NTF optimization:
                                        % If 0: No optimization of the NTF; If 1: Optimize the NTF
means = 1;                              % Number of means (Number of times to average the fft)
Nfft = 2^13;                            % Number of fft points
len = means * Nfft;                     % Total length of the data
skip = 1;                               % Number of points to skip in order to avoid initial transients

Fbw = 500e3;                            % Input signal bandwidth

Fs = 16e6;                              % Sampling frequency
f = (Fs / Nfft) * (0 : Nfft / 2 - 1);
OSR = Fs / (2 * Fbw);                   % Oversampling ratio
fbw_bin = round(Nfft / (2 * OSR));      % Band edge frequency bin
N = 4;                                  % Number of bits in the quantizer
nQlev = 2^N;                            % Number of quantizer levels

Hinf =4;                                % Maximum gain of the NTF, which sets the agressivity
                                        % of the loop filter
VrefDac = nQlev - 1;                    % Reference voltage (Defined here as the maximum voltage
                                        % level the DAC can output)


nperiods = 13;                          % Number of periods of the input signal < fbw_bin
fin = (nperiods / Nfft);                % Normalized input signal frequency, Fs = 1 Hz
t = 0 : len - 1;                        % Time vector, Nfft seconds = simulation time, valid for a normalized
                                        % sampling frequency Fs = 1Hz


AdBFS = -3.022;
Ampl = VrefDac * 10^(AdBFS / 20);
input = Ampl * sin(2 * pi * fin * t);
NTF = synthesizeNTF(L, OSR, opt, Hinf)
output = simulateDSM(input, NTF, nQlev);

alpha = 0 * ones(1,L);
beta = 1 * ones(1,L);
[a, g, b, c] = realizeNTF(NTF, 'CIFB')
aDT = a;
aCT = dt2ct_cifb(alpha, beta, aDT)
```

Fig. 2.20: Matlab script.

It is possible to modify the loop filter in order to gain control of the STF and make it unity in band for all possible feedback pulses.

In both case, a_{CT1} and a_{CT2} are got by a script in Matlab (Fig. 2.20).

In the loop filter in Fig. 2.19, V_{in} is only injected at virtual ground. Additional resistor and parameter n_3 are used to control the STF. V_{filt} must be inverted in order to achieve negative feedback. Using superposition to analyse the circuit, the transfer function for the new passive RC-network is found:

$$V_{filt}(s) = \frac{\frac{1}{n_3}\left(\frac{1}{n_2}+\frac{1}{n_1}\right)+\frac{2}{n_3}sRC}{(sRC)^2}V_{in} - \frac{\frac{1}{n_2}\left(\frac{1}{n_2}+\frac{1}{n_1}\right)+\frac{3}{n_2}sRC}{(sRC)^2}V_{fb} \qquad (2.29)$$

In the right half of the expression, $n_1$and $n_2$are chosen to implement the desired feedback coefficients, instead the parameter n_3 is adjusted to make the first coefficient, in the first half of the expression, equal to 1 in order to make the STF unity in band.

The STF function is determinate by the forward path transfer function $G_{CT}(s)$.

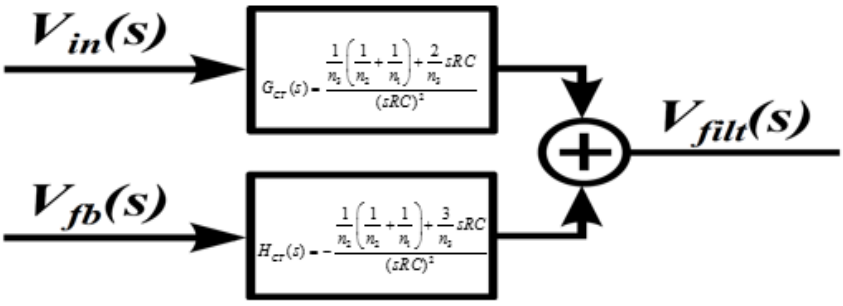

Fig. 2.21: Graphical representation.

Therefore, $G_{CT}(s)$can be written as the equation (2.1)

$$G_{CT}(s) = \frac{b_1+b_2sRC}{(sRC)^2} \qquad (2.30)$$

where

$$b_1 = \frac{1}{n_3}\left(\frac{1}{n_2} + \frac{1}{n_1}\right), \qquad b_2 = \frac{2}{n_3} \tag{2.31}$$

The magnitude of the STF is found as:

$$|STF(j2\pi f)| = \sqrt{\left(b_1^2 + \left(2b_2\pi\frac{f}{f_s}\right)^2\right)}\left(\frac{\sin\left(\pi\frac{f}{f_s}\right)}{\pi\frac{f}{f_s}}\right)^2 \tag{2.32}$$

Further simplifications are possible since $G_{CT}(s)$ has the same form as $H(s)$ in (2.1), injecting the feedback signal at virtual ground as well and changing the expression of the feedback coefficients. Simplified loop filter is shown above:

Using the superposition to calculate the transfer function, either resistor n_3R will be connected to node 1 and resistor n_2R to ground or vice versa.

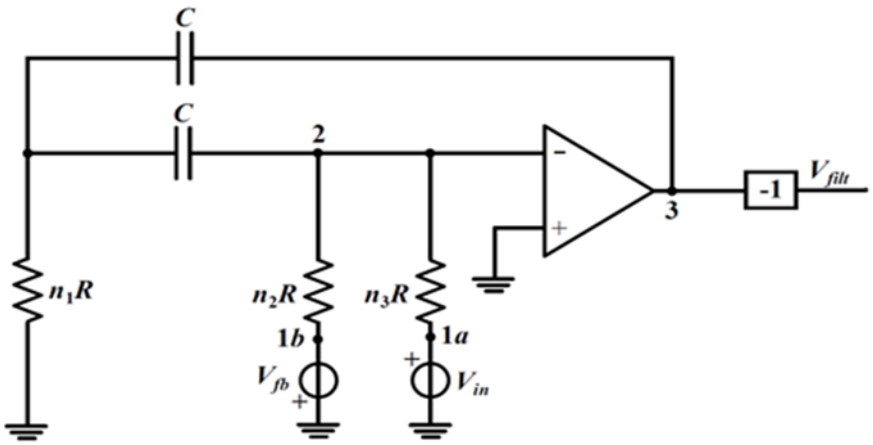

Fig. 2.22: Final loop filter.

The output voltage is found:

$$V_{filt} = \frac{\frac{1}{n_1n_3} + \frac{2}{n_3}sRC}{(sRC)^2}V_{in} - \frac{\frac{1}{n_1n_2} + \frac{2}{n_2}sRC}{(sRC)^2}Vfb \tag{2.33}$$

$$\begin{cases} a_{CT1} = \frac{1}{n_1 n_2} \\ a_{CT2} = \frac{2}{n_2} \end{cases} \begin{cases} n_1 = \frac{a_{CT2}}{2a_{CT1}} \\ n_2 = \frac{2}{a_{CT2}} \end{cases}, \Rightarrow \begin{cases} b_1 = \frac{1}{n_1 n_3} \\ b_2 = \frac{2}{n_3} \end{cases} \quad (2.34)$$

Setting b_1 to 1 to make STF unity in band and solving for n_3 yields:

$$\frac{1}{n_1 n_3} = 1 \quad \Rightarrow \quad n_3 = \frac{1}{n_1} \quad (2.35)$$

The loop gain of the loop filter in Fig. (2.22) is higher than the one in Fig. (2.19), due to less resistive loading on the amplifier by feedback network. This leads to lower DC-gain and GBW requirements, which, being finite, alter the loop filter transfer function and imply an NTF with degraded quantization noise suppression. It is important that the loop gain is as large as possible, because it determines how the ideal loop filter transfer function is approximated [7].

2.6 CHOICE OF R VALUE

Having high value of R allows to achieve higher loop gain. But this value is limited by various design constraints, such as thermal noise and resistor area. The first limitation was checked with a simulation on the overall performance of the modulator, with an ideal operational amplifier (OPAMP) and ideal ADC and DAC. The amplifier model consists of a transconductance G_m, output capacitance c_o, input capacitance c_i and output resistance r_o, set to 130KΩ, which is a typical value obtained by a common source output stage. While for the ADC and DAC was used two scripts in VerilogA. The modulator was designed for a maximum differential input signal of $200mV$, which was used in simulations as well.

The simulation consisted in representing the signal-noise ratio (SNR), sweeping different values of the transconductance G_m, from $100\mu\frac{A}{V}$ to $2000\mu\frac{A}{V}$, for different values of R, from $10k\Omega$ to $30K\Omega$, including thermal noise of resistors in the simulations. An ocean script, on Cadence, whose data was stored in a file for each value of R, was used to allow data to be read from MATLAB and, therefore, to plot the graph SNR vs. G_m.

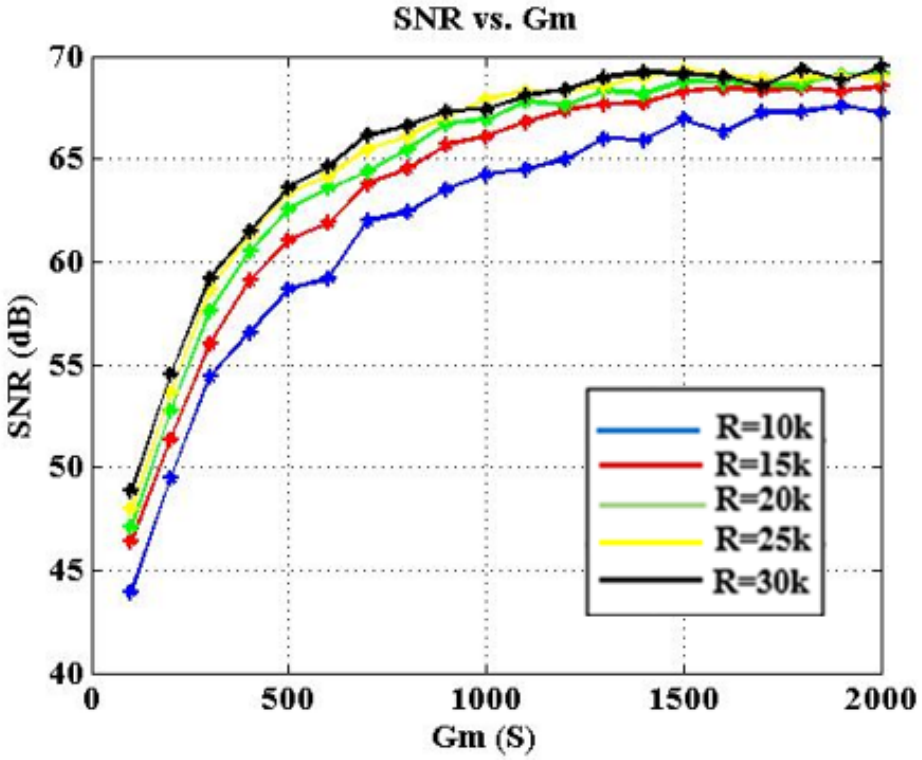

Fig. 2.23: SNR vs. G_m.

The graph in Fig. 2.23 shows that the performance of the modulator, about the SNR, is worse for lower value of R. This confirms how said above, about the fact that the loop gain decreases when the R decreases, like in Fig. (2.19), where more resistive loading load the feedback network. It is possible to conclude that,

to have at least a SNR of 65dB, the g_m of the OPAMP must be at least $1600\mu\frac{A}{V}$, therefore the OPAMP gain, given by $g_m R_{out}$, should be bigger than 46dB.

The design constraint about the resistor area become an issue in a unit cell in a 4-bit resistive DAC, whose resistance value is bigger 15 times than R, having the DAC 15 resistors in parallel.

Considering both of these two limitations, R was set to $30k\Omega$; being the sampling period $T_s = RC$, calculating C results immediate, which is equal to $2pF$.

2.7 FINITE GBW EFFECTS

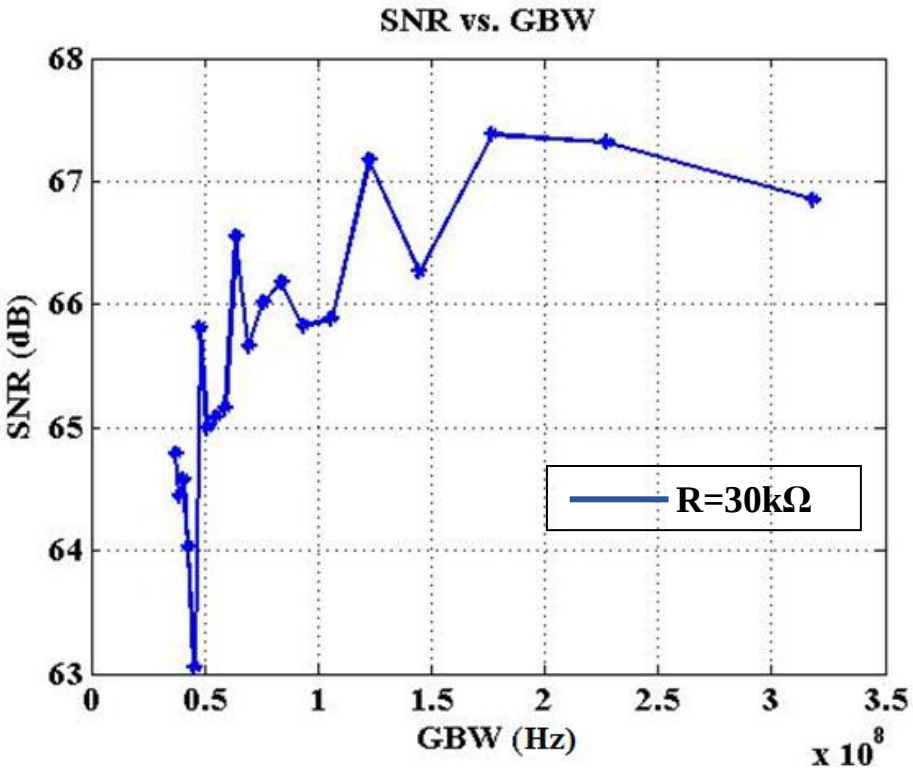

Fig. 2.24: SNR vs GBW.

To achieve an acceptable performance, a higher gain bandwidth (GBW) is required. In fact, due to the additional pole introduced by the finite GBW, the maximum value of the ideal loop gain is never reached [7]. The real loop gain, with finite DC-gain and GBW, differs from the ideal one for a deviation already at low frequencies, and intermediate frequencies as well.

This deviation involves a worsening of the quantization noise suppression.

After choosing the proper value of R, that provides an acceptable SNR and does not take up too much area, the second step is to determine, for the selected R, the minimum value of GBW that allows to achieve a good SNR. To meet this need, the SNR graph, sweeping different values of load capacitor C_l from $1pF$ to $8.6pF$, with a step of $0.4pF$, was plotted considering $GBW = C_l/g_m$, and using the ocean script.

The graph in Fig. 2.24 shows that, to reach a SNR of 65dB, a GBW of 70MHz is required.

3. Operational Amplifier design.

The operational amplifier in fully differential configuration was implemented using an operational transconductance amplifier (OTA) with a positive feed-forward and feedback compensation. An important disadvantage of a fully differential structure is the need of a common-mode feedback (CMFB) circuit. The CMFB circuit goals are: 1) to fix the common-mode voltage V_{CM} at different high impedance nodes and 2) to suppress the common-mode signal components overall band of differential operation. The CMFB loop has to be designed carefully to avoid potential stability problems and high DC gain is required to stabilize the common mode output. High bandwidth is another important requirement to be respected as well, since new communication standards offer higher data rates, resulting in increasing channel bandwidth [13]. The circuit was designed to consume a power of $44\mu W$ with a supply voltage of $800mV$.

3.1 ACHIEVING REQUIREMENTS

Two different structures of OTA are possible to reach an enough high DC gain. The first one is based on cascading stages, which requires compensation technique to increase the phase margin, but, at the same time, allows to obtain a large loop gain with improved linearity, and the second one consist in transistors stacking, which limits the voltage supply. In this thesis, the first structure was implemented.

The Miller compensation technique is one of the several compensation techniques, consisting to reduce the first pole's frequency and increasing the one of the second pole, in fact it is called also pole spitting. Thus, altering the transfer function response in this way, it is possible to reach stability. But, the shift towards lower frequencies of the dominant pole, is in contrast with the GBW requirement. Another issue of the Miller compensation is due to the introduction of right-half-plane (RHP) zero. This singularity is very undesirable, since it boosts the magnitude while decreasing the phase.

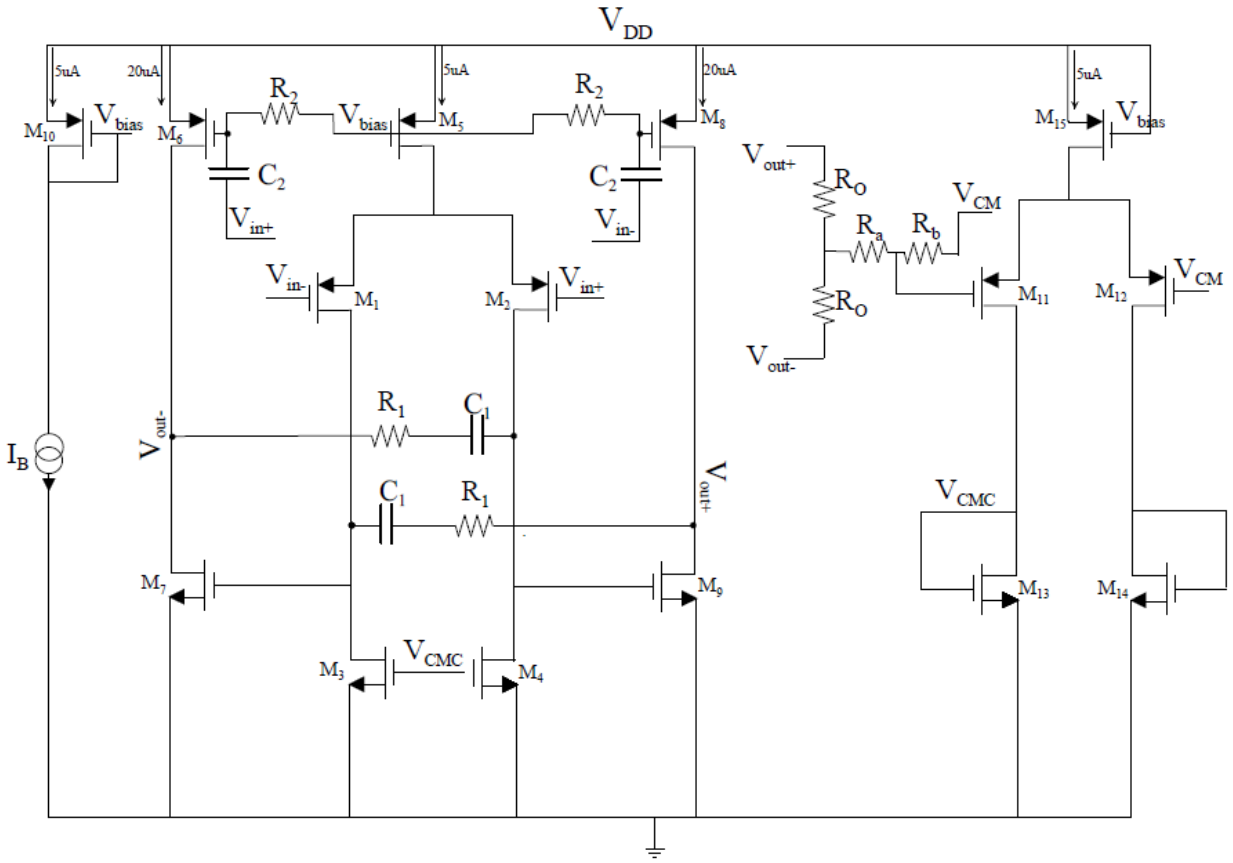

Fig. 3.1: Schematic of the OTA with common mode feedback.

Counteracting these negative effects of the Miller compensation, positive feed-forward and feedback paths are used in the above circuit. The feed-forward path via C_2 results in a left-half-plane zero (LHP) instead of RHP of the Miller compensation. This path acts only on the transfer function, increasing the phase margin as desired with tuning the resistance R_2. The positive feedback, enabled through C_1, consents to increase the BW_{3dB} in the transfer function and to boost the phase margin in the loop gain plot. This feedback acts as an anti pole-split [15], that causes the two loop poles to attract, and eventually become imaginary with increasing values of C_1. In this case, the GBW is not improved and the phase margin is reduced. If the capacitance continues to grow, the poles may also appear in RHP. However, the closed loop poles of the integrator can still be in the LHP, since the LHP zero and the feedback via the integration capacitor moves the closed-loop poles into the LHP [14].

3.2 SIZING

The MOSFETs were sized in such a way as to respect the requirement about the power consumption, considering the total current of the circuit of $55\mu A$. The current was divided in the different branches, starting from a bias current of $5\mu A$, so as to flow $5\mu A$ in the first stage, $20\mu A$ in the second stage and other $5\mu A$ in the common mode feedback stage.

All transistors work in saturation region, and all n-MOSFETs in sub-threshold region to achieve two important requirements:

1) It was necessary to increase the g_m of the output stage n-MOSFETs to achieve maximum linearity in the input- output characteristic (Fig. 3.2).

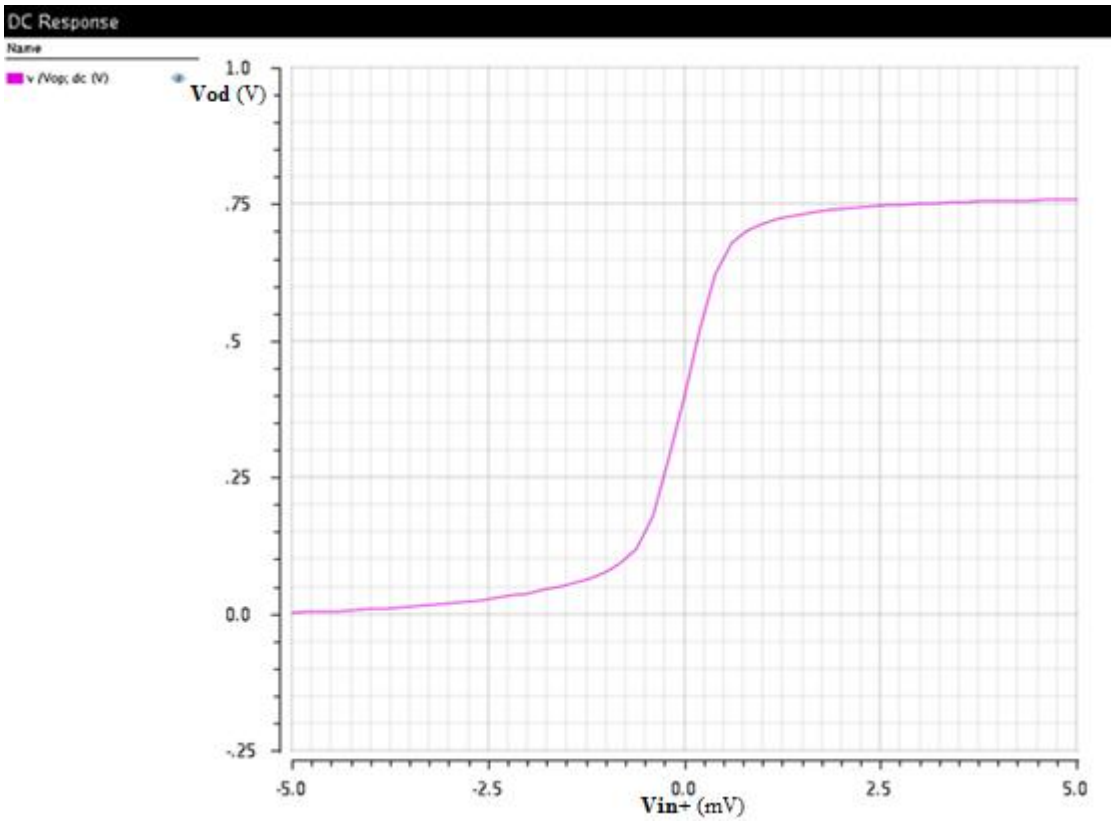

Fig. 3.2: Input-output characteristic.

2) Boosting the g_m of the n-MOSFETs of the common mode feedback stage, it is possible to increase the CMFB loop gain, important to stabilize the common mode output, for different process corner. The worst case is found in the Fast-Slow (FS) process corner, where the NMOS devices are fast and the PMOS are slow, and the output results lower than the typical corner of less 10%.

Consequently, the n-MOSFETs of the first stage will be in sub-threshold region, having to maintain the output voltage at the common mode of 400mV. The other MOSFETs were sized so as to flow the respective currents in the different branches and to have the correct operating point.

MOSFETs	W(µm)	L(µm)	N.F.	N.D. in //
M_1	2.4	0.7	2	4
M_3	18.17	2	1	1
M_5	0.7	0.7	2	4
M_6	7	0.7	2	2
M_7	30	0.7	2	4
M_{10}	3.2	0.7	2	1
M_{11}	6.6	0.7	2	1
M_{13}	27	3.3	1	1
M_{15}	3.3	0.7	2	1

Table 3.1: MOSFETs size

The table above shows the values of width, length, number of fingers and number of devices in parallel for each active component.

3.2.1 AC ANALYSIS IN OPEN LOOP

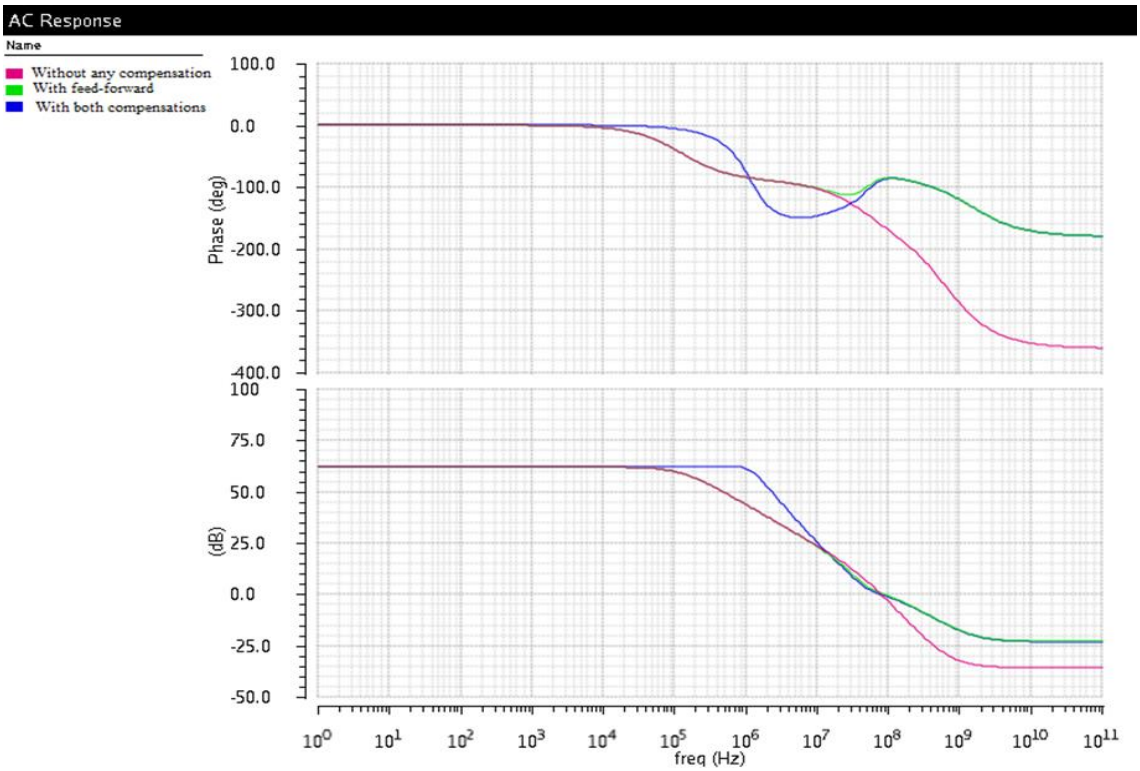

Fig. 3.3: Gain and phase of the differential mode.

The two resistances R_o of $90K\Omega$ allow to reach an enough high gain in the transfer function of $62dB$. The value of these resistances is important to be satisfactory to make the amplifier linear. The resistance R_2 and the capacitance C_2 were sized in such a way that the feed-forward path performs the frequency compensation, and stabilizes the amplifier by bending the root locus into the LHP. Therefore, a pole and a zero, respectively before the unity gain frequency f_0 equal to $81.3MHz$, got from the circuit without any compensation, were placed. Introducing these two roots, the f_0 results shifted towards $90.8MHz$, at which the phase margin φ is equal to 95.49°, instead of 18.95° without the feed-forward path.

The positive feedback, enabled by R_1 and C_1, results a pole-zero cancellation, therefore, the dominant pole frequency appear shifted to the higher frequencies. In this OPAMP the cut-off frequency appears at $1.4MHz$, instead of $126.2KHz$ obtained just with feed-forward. It is important to notice that BW_{3dB} is much larger as much as the load capacitor is smaller [13], which represents the parasitic capacitance at the input of the flash ADC. The capacitance was estimated to $200fF$[7].

A phase margin of 92.2° was obtained considering the contribution of both the feedback and the feed-forward paths.

3.2.2 STABILITY ANALYSIS IN OPEN LOOP

As mentioned above, the feed-forward path does not contribute to phase compensation of the loop gain. The positive feedback, instead, acts on boosting the phase margin of the loop gain.

This increasing is due to the pole splitting of the feedback, which results negative for the calculation of the loop gain; therefore, its behaviour is the same of the Miller compensation.

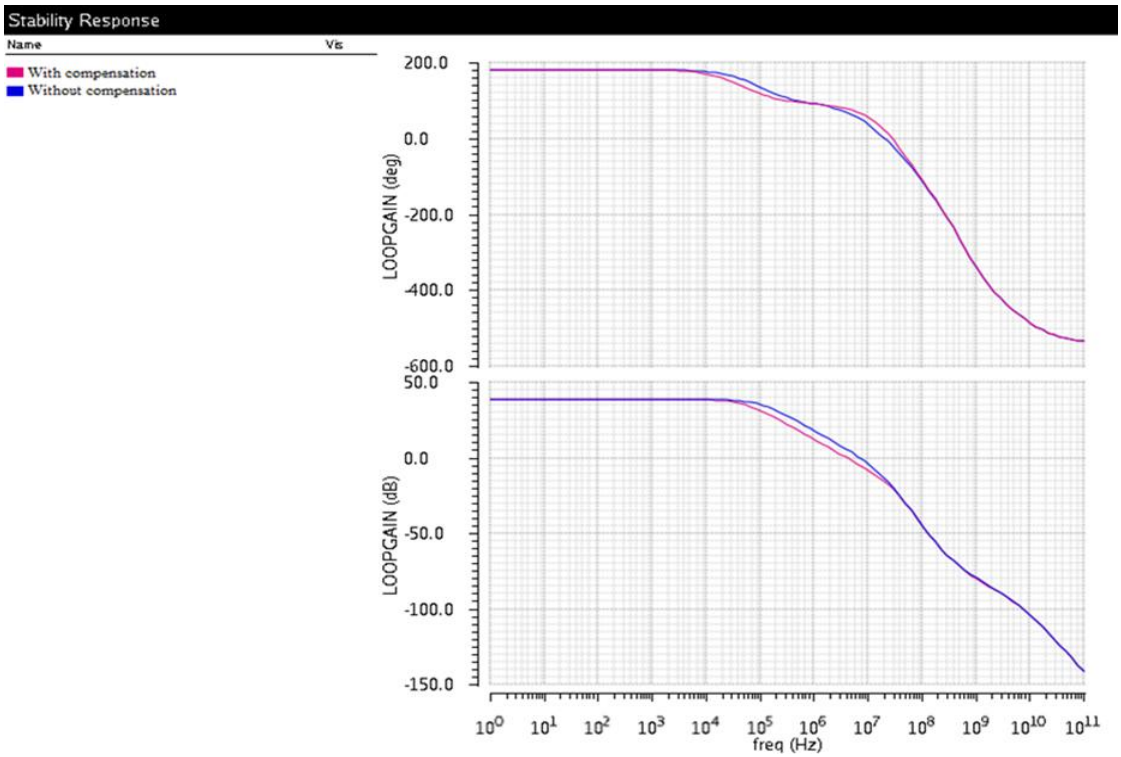

Fig. 3.4: Loop gain.

The plot in Fig. 3.4 shows that the phase margin without the feedback positive is already enough to meet the stability conditions, in fact its value is of 51.86°, but the issue is continuing to satisfy these conditions when the OPAMP appears in the closed loop. It is good to introduce the feedback path, thanks to which the

phase margin grow up until 76.4°. To make this kind of analysis, a differential probe, called cmdmprobe, has to be used. When the analysis common mode loop stability is carried out, CMDM should be set as 1 in the cmdmprobe property.

The two resistances R_a and R_b play a very important role with regard to the stability of the common mode, because they allow finding a trade-off between the gain and the phase margin. In fact, tuning the ratio between these two components, increasing the gain and decreasing the phase margin, or vice versa, is possible.

PASSIVE COMPONENTS	VALUES
R_2	$10K$
C_2	$325f$
R_1	$200k$
C_1	$50f$
R_a	$4.6K$
R_b	$5.4K$
R_o	$90K$

Table 2: Passive components values.

3.3 OPAMP IN CLOSED LOOP

Once that the OPAMP appears inside the negative feedback of the integrator, closed loop stability analysis is followed to ensure the two feedback loops in the

system are stable. Last, transient simulation is performed to see the differential and common mode responses.

3.3.1 STABILITY ANALYSIS

The loop of the common mode feedback and the loop of the integrator were opened at the same time to check if the conditions stability were respected. First of all, the stability with criterion bode has been studied, and afterwards with the Nyquist criterion.

The plot in Fig. 3.5 shows a phase margin of 50° and a gain of 38dB, that is the best achievable. It is no longer possible tuning the ratio between the two resistance R_a and R_b, since now the phase margin has reached the limit acceptable to the conditions of stability.

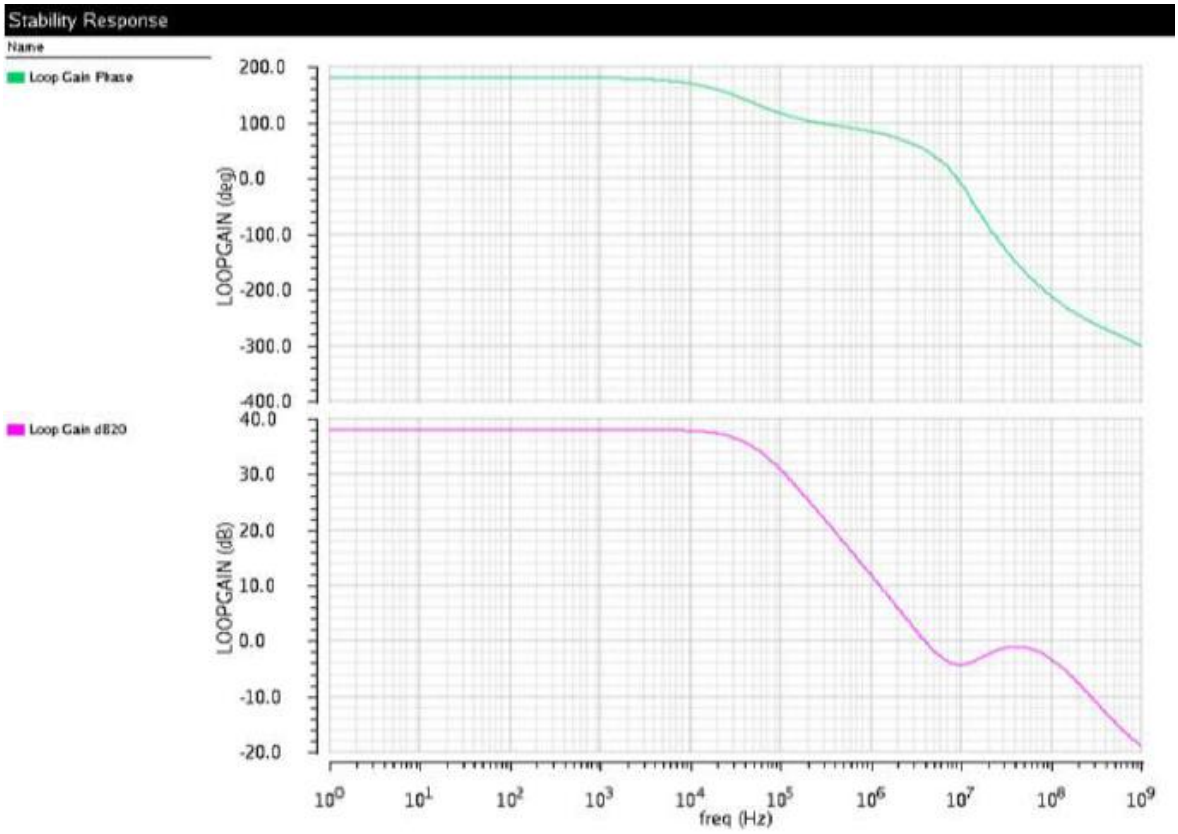

Fig. 3.5: Common-mode loop gain of the loop filter.

Now, the differential stability of the negative feedback of the integrator has to be checked (Fig. 3.6). For differential loop stability, CMDM should be set as -1 in the cmdmprobe property. The loop gain plot converges to zero at DC, due to the capacitive feedback of the filter. It can be inferred from the graph that the phase margin is equal to 82.6°, value that would ensure stability. But, for greater safety, also the Nyquist diagram was plotted.

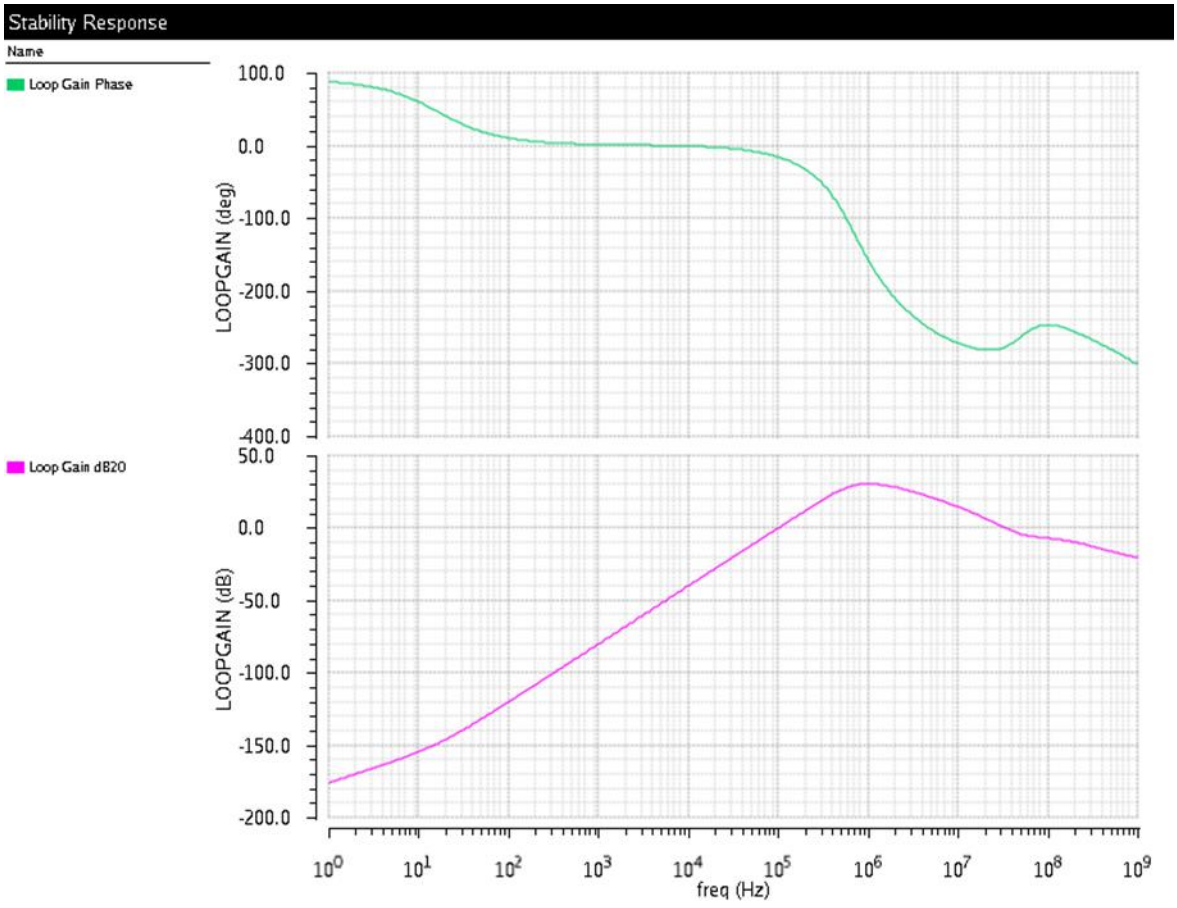

Fig. 3.6: Differential mode stability of the loop filter.

The differential mode is stable even by the Nyquist diagram, in which the point $1 + j0$ is not included in the curve.

It can be said, surely, that the loop filter is stable as regards both the common mode and the differential mode.

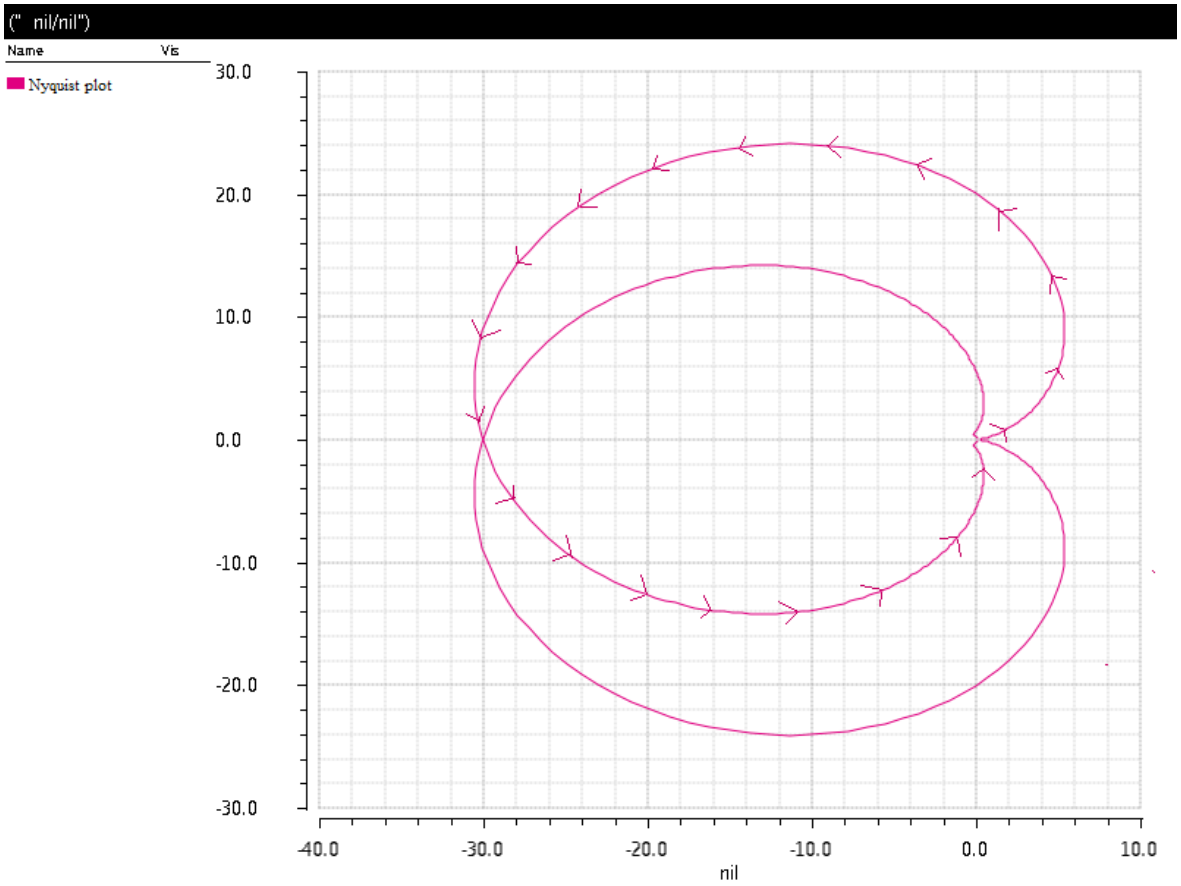

Fig. 3.7: Nyquist plot of differential stability of the loop filter.

3.3.2 DIFFERENTIAL/COMMON MODE TRANSIENT RESPONSE

Transient simulations are performed to test differential mode and common mode responses when the OPAMP results inside the loop filter. 50µV differential mode pulse and 100mV common mode pulse with 1fs rise/fall times and 1ms pulse width are simulated, resulting waveforms are plotted in Fig. 3.8 and Fig. 3.9, respectively. For differential mode response, as shown in Fig. 3.8, there is a

overshoot and undershoot about 7.5mV. The under damping maybe caused by less phase margin when configured to unity-gain.

For common mode response, as shown in Fig. 3.9, the common mode disturbance at the input is attenuated with respect to the case of differential transient response, in fact the amplitude of the overshoot and undershoot in about 3.6mV.

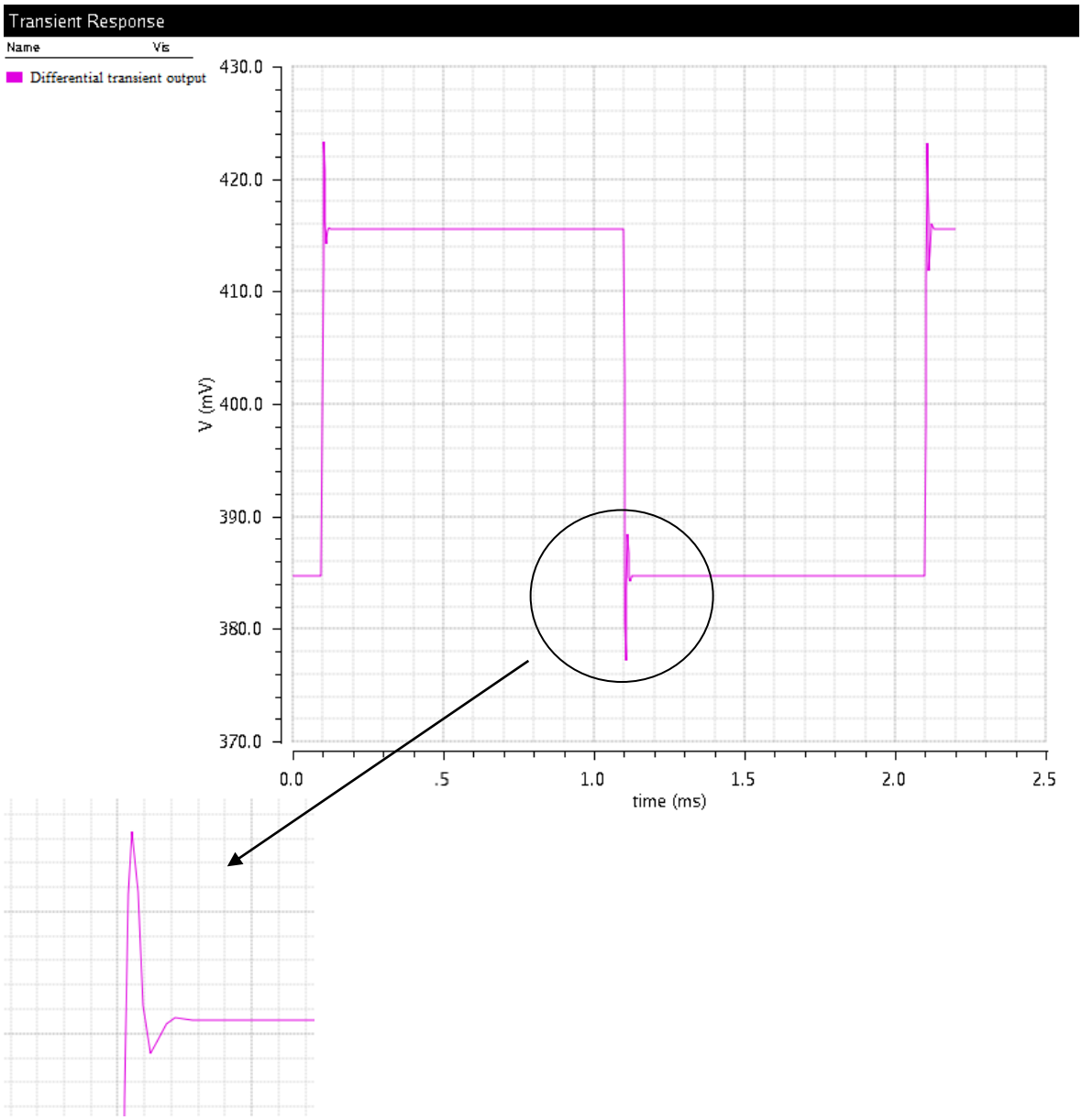

Fig. 3.8: Differential transient output of the loop filter.

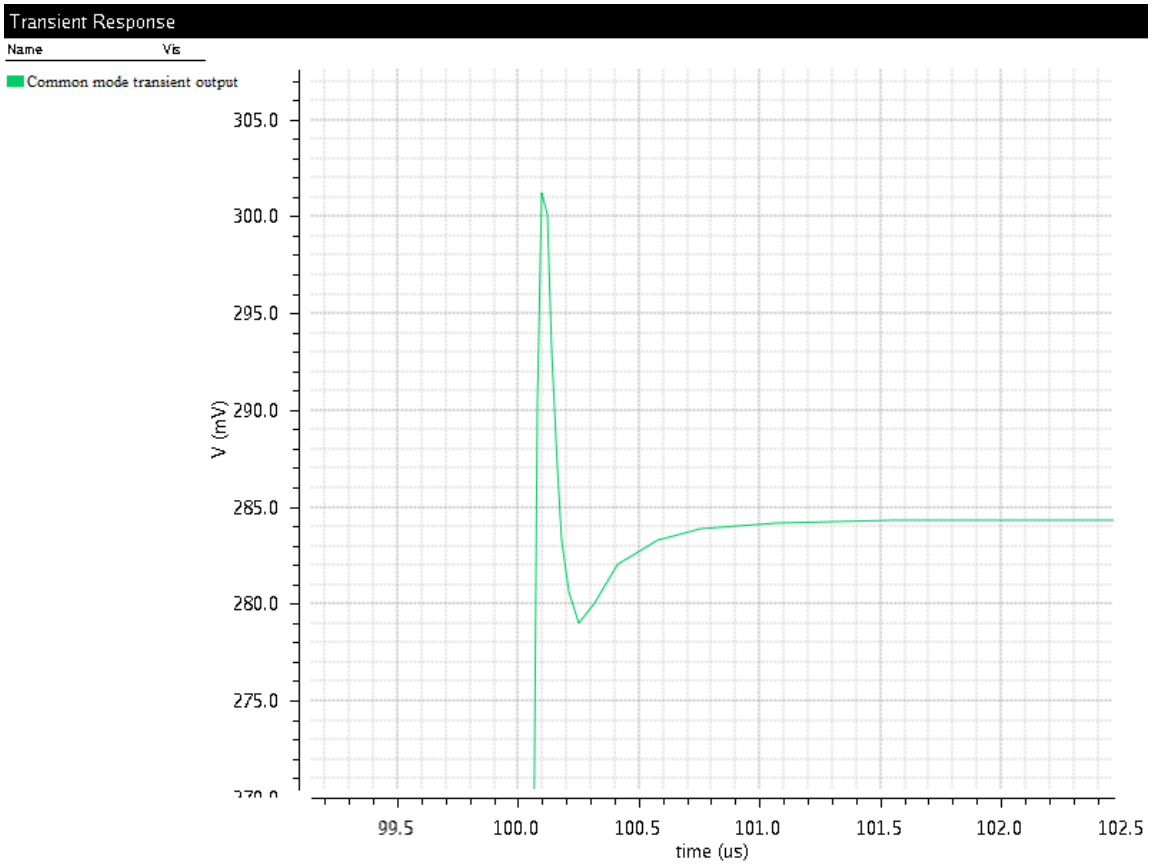

Fig. 3.9: Common mode transient output of the loop filter.

3.4 OPAMP LAYOUT

A careful design of the OPAMP layout, with common centroid structures and the use of dummy elements, was implemented. Layout dimensions are 58,63 µm of length and 49,45 µm of width.

Post layout simulation result is shown in Fig. 3.11.

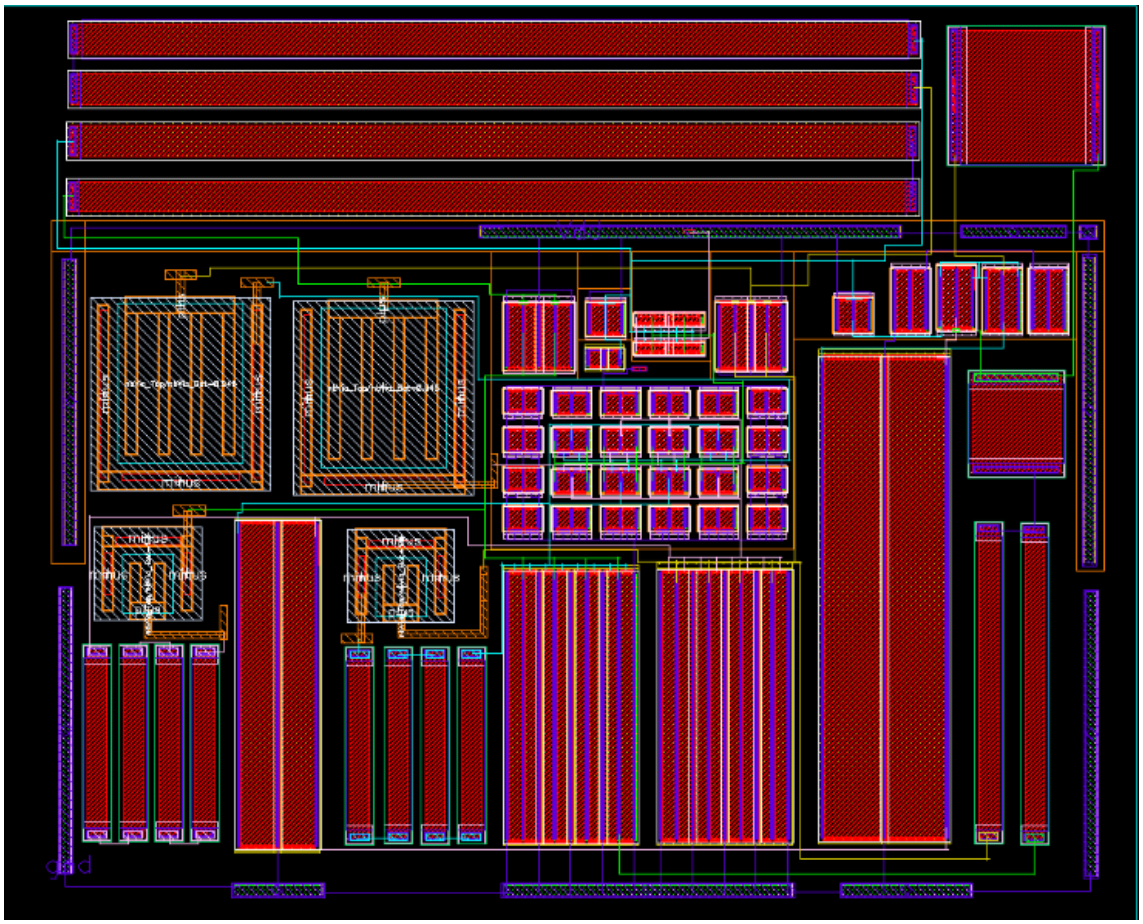

Fig. 3.10: OPAMP layout.

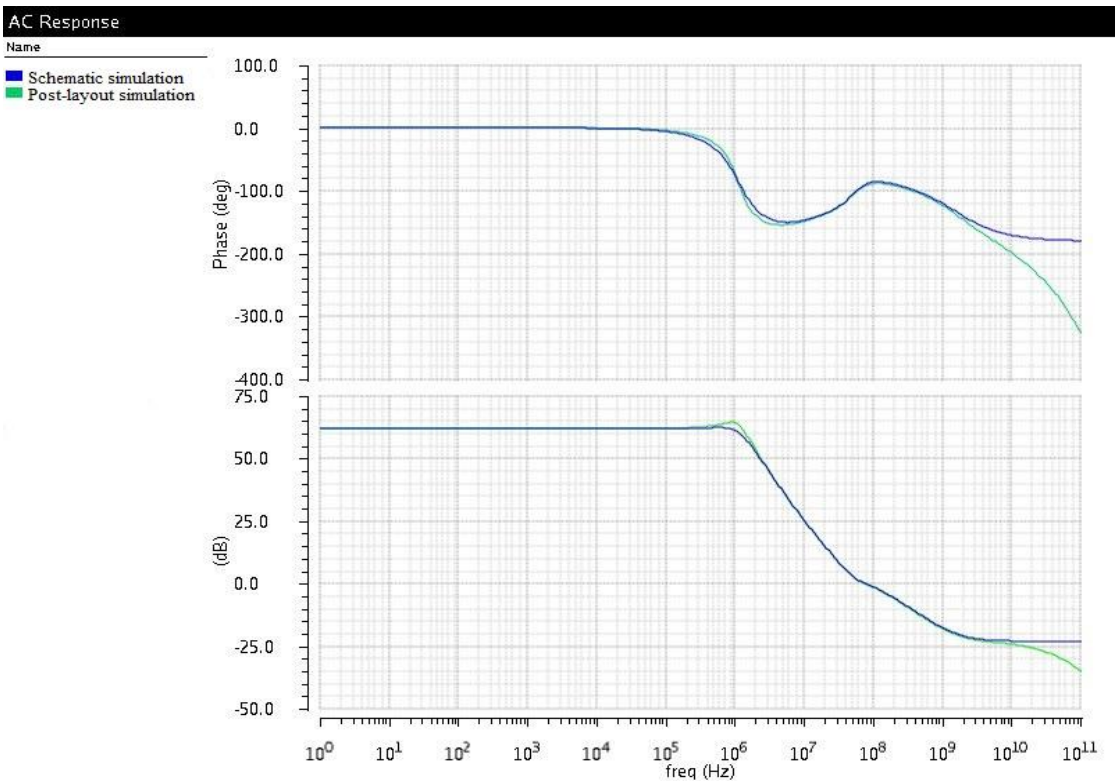

Fig. 3.11: Post-layout simulation: gain and phase of differential mode.

4. Performance estimation of the complete ΔΣ modulator.

The DAC and the ADC also influence the performances of the modulator. In this chapter, the modulator uses a flash ADC.

The feedback DAC is a critical component in a ΔΣ modulator, due to its non-idealities, such as mismatch error, which causes distortions in the DAC output when multi-bit DACs are employed, and timing errors, which includes excess loop delay and clock jitter. Instead, the requirements on the flash ADC are low since any errors injected in the ADC such as clock jitter, DC offset, thermal noise, and distortion are shaped by the loop. The only requirement should be a low input capacitance, which allows minimizing the capacitive loading and loss in GBW of the loop filter.

4.1 DISTORTIONS

If the ΔΣ modulator employs a single-bit DAC, which is linear and does not require precision matching, the only issue is caused by inter-symbol interference (ISI), a form of distortion of a signal in which one symbol interferes with subsequent symbols.

This happens due to the NRZ pulse transition, which has a limited rise and fall time, therefore, the effective DAC feedback level will depend on whether or not

there is an output transition from one level to the opposite level. In fact, in case of a transition, the effective DAC feedback level will be less than that without transition. Being the distortion signal dependent, depends on the preceding symbol and will result in harmonic distortion components and intermodulation products. As shown in Fig. 4.1, there are errors caused by the absence of rising and falling edges. This interference results in a compression of out-of-band gain (OBG). A solution to reduce the effects of limited rise and fall times is to use RZ pulses, but it is more sensitive to clock jitter and may not provide sufficient feedback level especially at high sampling frequency. Thus, a multi-bit quantizer can be employed for reducing clock jitter and alleviating the problem of the limited OBG, which results in less quantization noise in-band, being more precise. The quantizer is a latched comparator, whose output drives differential pair digital-to-analog converters. However, the dynamic range improvement of a multi-bit quantizer is not quite realized due to the high linearity requirement of feedback DAC.

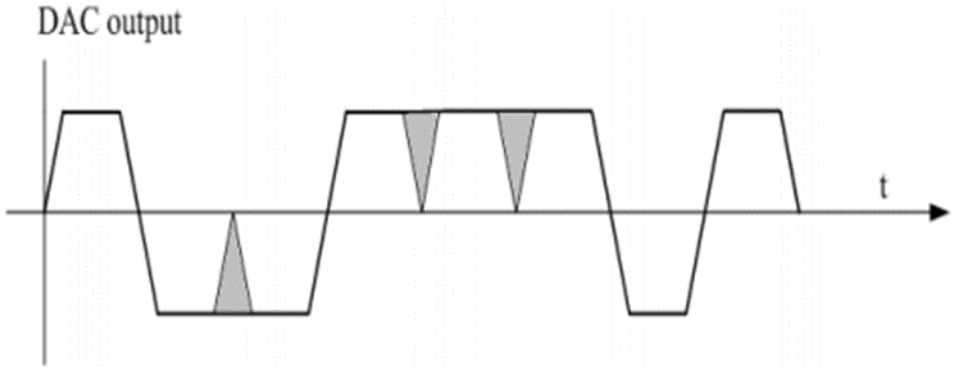

Fig. 4.1: Distortion due to limited rise and fall times using NRZ pulse [19].

The non-linearity in a multi-bit feedback DAC increases the noise floor in the signal output spectrum of the modulator and reduces the dynamic range. This noise added is due to the mismatch error introduced by the uneven spacing of DAC levels. Due to the non-linearity effect, this ΔΣ modulator uses a resistor string DAC rather than a current steering DAC, because resistors show better matching accuracy than transistors, as the output of a differential current-steering DAC may be asymmetric if, for example, the two transistors in the differential switch pair inject a different amount of charge. The choice of resistive DAC allows to reach the desired performance.

Certain noise shaping techniques have been used to reduce this non-linearity, the purpose of which is to push also the non-linearity noise to higher frequency, where is then removed by the decimation filter. But before that, a dynamic-element matching (DEM) must be used; the most efficient is data-weighted averaging (DWA) [19].

4.1.1 DATA-WEIGHTED AVERAGING

The overall resolution of a multi-bit ΔΣ modulator is limited by the effective resolution of the feedback DAC. Decreasing the mismatch between the elements of the DAC, which gives rise to a noise term in the overall ADC transfer function that is not shaped, data-weighted averaging technique, is implemented.

The method uses just one index, in common with all the input codes updated by the addition of the new input code to the content of the index register. Fig. 4.2

depicts 15 unity elements arranged as a wheel to outline the rotation in the selection of elements.

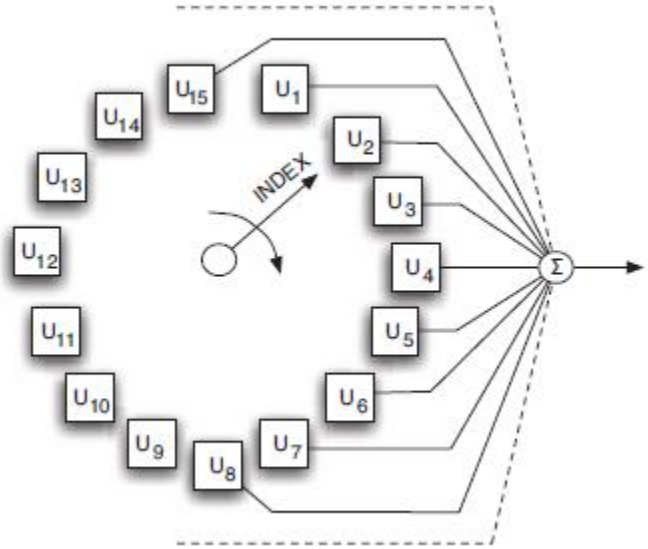

Fig. 4.2: Data weighted algorithm section of 15 unity elements [22].

The advantage of the DWA method is that the rotation cycle is fast thanks to the update of the only index every clock period. The same sequence of input data used in Fig. 4.3a gives rise to the element usage and the corresponding waveforms of Fig. 4.3b. The DWA method works well for 7 or more elements [22].

The average value of all the elements, such that each time a complete cycle is made around the wheel, corresponds to the ideal element value. In this case, the accumulated error must equal zero, while the accumulated error at any point along the wheel is a finite value. This results in a first-order mismatch error

shaping, which is sufficient if mismatch among the DAC elements is less than 5% [27].

First-order DEM approaches can be susceptible to tonal problems; resolving this issue, a randomly reversal of the direction of the rotation about the wheel technique is used. The introduction of the random reversal technique produces a rise in the noise floor of the DAC, which can be reduced retaining the last position visited in each rotation direction and returning to that position as a starting point [27].

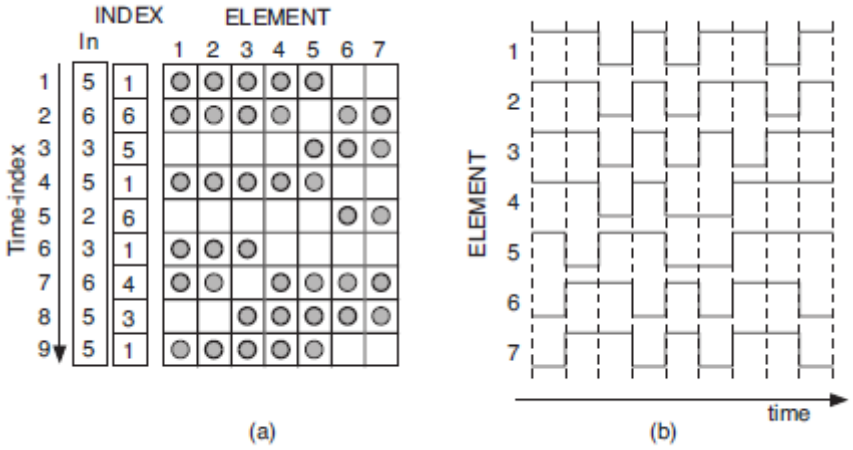

Fig. 4.3: (a) DWA index and usage of 7-elements for a given sequence of input data. (b) Elements waveforms.

4.2 EXCESS LOOP DELAY

A real quantizer does not make a decision instantaneously, being a regenerative circuit with finite regeneration gain, where the finite transistor switching times causes a delay between the quantizer clock and the DAC waveforms. This delay contributes to the excess loop delay, which includes also delay in the feedback

network, such as dynamic element matching circuits or delay in the loop filter due to integrator with finite GBW. A quantizer input close to zero level, will generally take longer to resolve. Furthermore, DAC has a nonzero switching time.

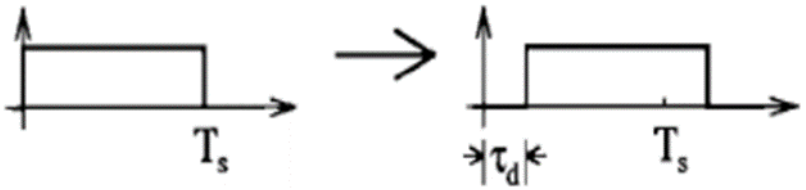

Fig. 4.4: Excess loop delay in NRZ DAC pulse.

If the loop delay causes the DAC pulse to extend beyond the sampling period, T_s, then the modulator order increases by one [16] from L to L+1, which may eventually make a CT ΔΣ modulator unstable. A large loop delay is required to push the RZ pulse into the next sampling period, like illustrated in Fig. 4.5.

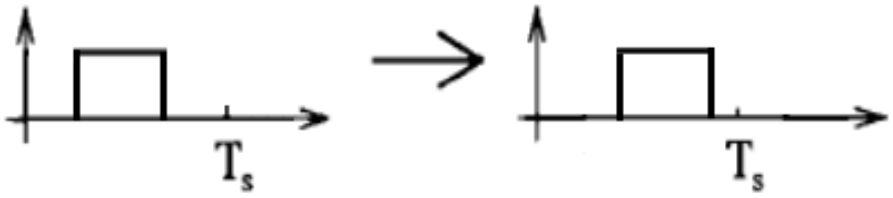

Fig. 4.5: Excess loop delay in RZ DAC pulse.

This characteristic makes the RZ feedback pulse less sensitive to loop delay compared to NRZ feedback. Placing an RZ pulse, of duration $T_s/2$, exactly in the

middle of the sampling period, results in a $T_s/4$ delay between the quantizer and the output of the DAC and in a $T_s/4$ delay margin until the next sampling period.

Different studies show that loop delay results in coefficient mismatch which affects the NTF and boosts the quantization noise [17], but knowing which of the feedback paths in a CT ΔΣ modulator is most sensitive to loop delay is of the great importance. The first feedback path is the least sensitive to loop delay, while the following feedback path are increasingly more sensitive. Therefore, in this thesis, the last feedback path was considering to achieve the desired performance.

The uncertainty of the delay from the flash ADC output to the DAC input is often removed by clocking the DACs with a delayed clock, to allow the digital signal to settle before rising edge of the DAC clock.

4.2.1 LOOP DELAY COMPENSATION

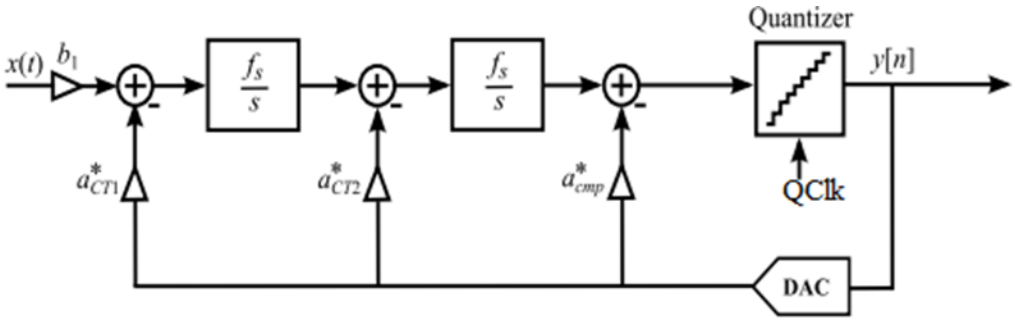

Fig. 4.6: Additional path for loop delay compensation of a 2nd order CIFB DSM [4].

A certain amount of loop delay, much larger than the worst-case delay, is required to ensure that the DAC is update just when the quantizer has finished the conversion of the current sample; this is one of several delay compensation

methods. It also results in an advantage for controlling loop delay, both being dependent on signal and process variations.

As shown above, the introduction of a loop delay t_d can shift the DAC pulse into the next sampling period, increasing the order of the modulator; therefore, a direct path around the quantizer is required, to avoid that the ΔΣ modulator become unstable. The new path requires the addition of a DAC and a summing operation, as the Fig. 4.6 illustrates.

To achieve full compensation, a compensating coefficient a_{cmp} has to be determined and, at the same time, the other two coefficients, a_{CT1} and a_{CT2}, respectively equal to 1 and 1,5 in the case without any loop delay, must be tuned rightly, like in the following way,

$$\begin{cases} a^*_{CT1} = a_{CT1} \\ a^*_{CT2} = a_{CT1}\tau_d + a_{CT2} \\ a_{cmp} = \frac{a_{CT1}\tau^2_d}{2} + a_{CT2}\tau_d \end{cases} \tag{4.1}$$

where τ_d is the normalized loop delay given by:

$$\tau_d = \frac{t_d}{T_s} \tag{4.2}$$

From the plot of the compensating coefficient [4], in Fig. 4.7, for different values of τ_d, determining loop delay is possible. The choice is based on the way, which allows optimizing the value of the compensating coefficient. In fact, choosing $a_{cmp} = 1$, the loop compensation DAC realized in VerilogA, during the simulations with flash ADC, will be the same to the DAC in the SAR quantizer, after the replacing.

Thus, using $\tau_d = 0.56$, the loop delay t_d is equal to $0.56T_s$. Starting from the value of τ_d, ${a^*}_{CT1}$ and ${a^*}_{CT2}$ can be now calculated by the system in (4.1), from which ${a^*}_{CT1} = 1$ and ${a^*}_{CT2} = 2$. Obviously, as shown in (2.9), n_1 and n_2 will change their values as well and, as a result, n_3 (2.31).

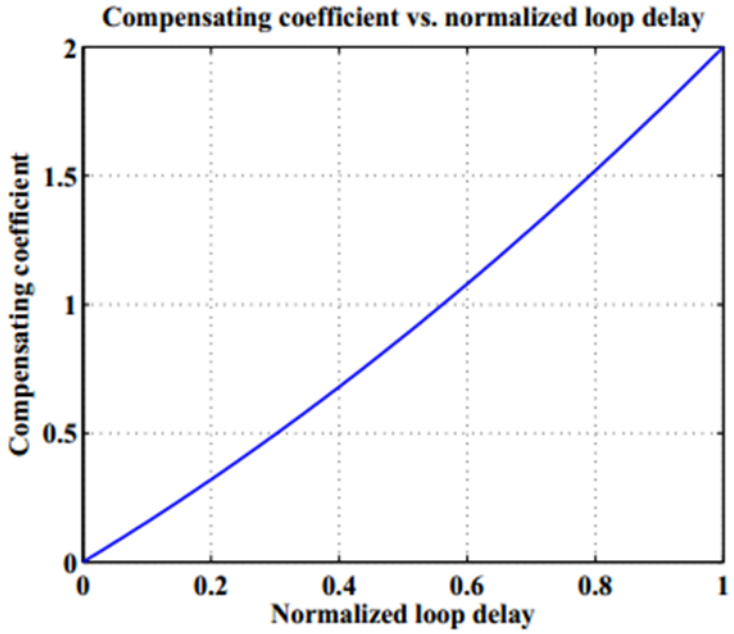

Fig. 4.7: Compensating coefficient vs. normalized loop delay [4].

4.3 CLOCK JITTER

Jitter is the timing variations of a set of signal edges from their ideal values. Clock jitter is typically caused by noise or other disturbances in the system. Contributing factors include thermal noise, power supply variations, loading conditions, device noise, and interference coupled from nearby circuits.

Clock jitter influences the sampling instant of the flash quantizer, as well as the width of the feedback DAC pulse. Noise due to the modulation of the

feedback DAC pulse-width is the dominant cause of jitter noise [23], [24]. This is quite credible whereas the error due to the variation of the sampling instant of the quantizer is noise shaped due to the high loop gain. Hence, the in-band noise power should not be dominated by this noise. However, the error in the DAC feedback pulse-width adds directly at the input of the modulator and is not noise shaped.

As mentioned above, multi-bit quantizer is less sensitive to clock jitter than the single bit one. Another advantage results in the possibility to choose a more aggressive NTF, which decreases the IBN (in-band noise).

4.3.1 JITTER ERROR SOURCES IN DT AND CT ΔΣ MODULATOR

The two most critical errors resulting from clock jitter are generated at the input and in the feedback DAC; these are respectively sampling jitter errors and DAC jitter errors.

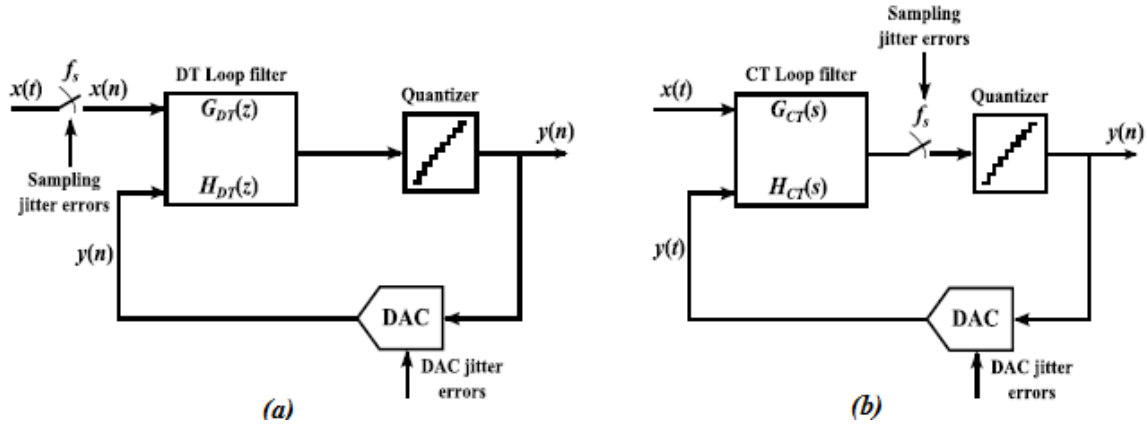

Fig. 4.8: (*a*) Jitter error sources in DT DSM and ***(b)*** in CT DSM [4].

In the DT DSM in Fig. 4.8*a*, the CT signal at the input is sampled at wrong time instants, due to the jittered clock. This results in amplitude errors that are injected directly at the input. In the CT DSM, in Fig. 4.8*b*, all errors before the quantizer are suppressed by NTF, therefore also sampling jitter errors can be neglected.

Any timing variations affecting the clock that controls the DAC will modify the starting and ending points of the feedback pulses. In a DT DSM the shape of a typical feedback pulse is exponential, since the capacitors in SC circuits are discharged through switches with finite on-resistances. As shown in Fig. 4.9*a*, the charge lost due to an error is tiny, being most of the charge transferred during the beginning of the sampling period. In a CT DSM, for the commonly used rectangular pulses, more charge is lost due to the rectangular shape which results in high sensitivity to clock jitter.

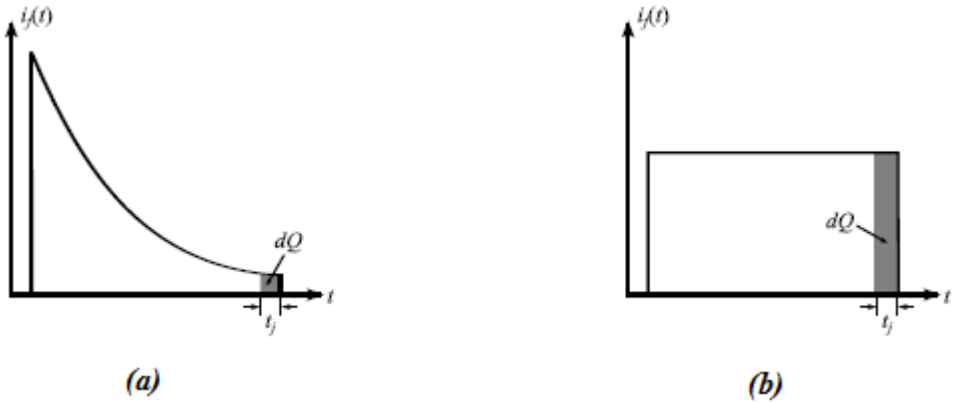

Fig. 4.9: (*a*) Jittered DT DAC pulse, **(*b*)** Jittered CT DAC pulse [4].

Finally, CT DSMs are more sensitive to clock jitter than DT DSMs, since the sampling jitter errors at the input only affect the signal while the DAC jitter errors affect the sum of the signal and the quantization noise.

4.3.2 CLOCK JITTER AS ADDITIVE AMPLITUDE ERRORS

Jitter in the feedback DAC can be modelled as an additive amplitude error sequence that produces the same charge error as the timing variations due to clock jitter [4]. Considering the 3rd-order CT DSM in Fig. 4.10, and referring the errors back to the input and then multiplying by the STF, which is ideally unity in band, is deducted that the first DAC is most critical. In fact, the DAC errors $e_2[n]$ and $e_3[n]$ are noise shaped when referred back to the input since they are preceded by at least one integrator.

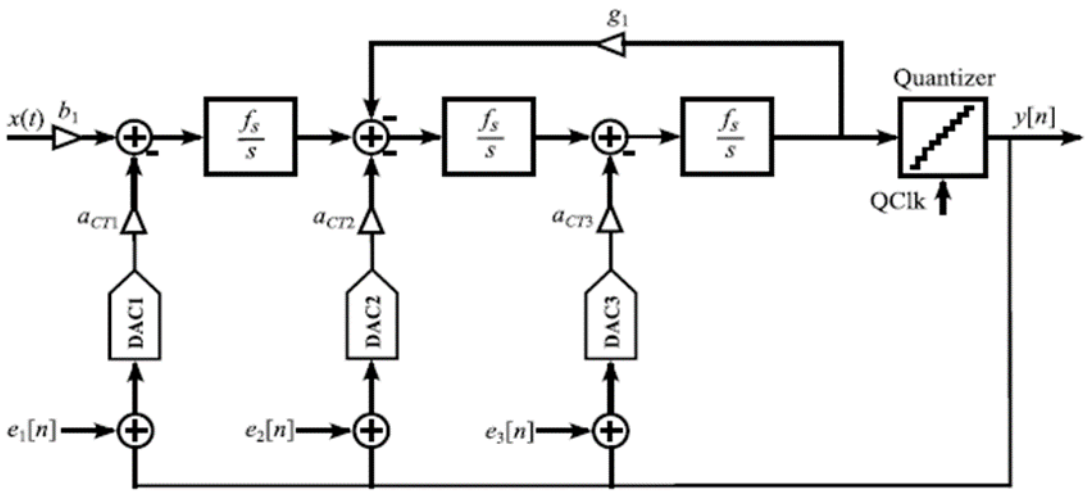

Fig. 4.10: Modelling clock jitter as additive amplitude errors [4].

4.3.3 JITTER SENSITIVITY OF RECTANGULAR PULSE

The charge errors due to clock jitter are generated only during the transitions of the DAC output signal. The peak values of the DAC outputs are determined by the feedback coefficient $a_{CT,NRZ}$ or $a_{CT,RZ}$ and the quantization step Δ which equals the DAC reference voltage. The NRZ DAC output switches between

$a_{CT,NRZ}\Delta$ and $-a_{CT,NRZ}\Delta$, while the RZ DAC output transitions between $\pm a_{CT,RZ}\Delta$ and 0. As shown in (1.13), $a_{CT,RZ} = 2a_{CT,NRZ}$, therefore the height of the transitions is the same in both cases, if the duty cycle of the RZ pulse is equal to 0,5. Consequently, the charge error affecting one edge of the RZ and NRZ pulses is also the same and is given by:

$$dQ = 2a_{CT,NRZ}\Delta t_j \tag{4.2}$$

The number of transitions between RZ and NRZ is different, in fact the RZ pulse transitions two times during every clock period even when the input data does not change, increasing the power of the charge error compared to the NRZ DAC which transitions only when the input data changes. Therefore, RZ feedback is more sensitive to clock jitter than NRZ feedback.

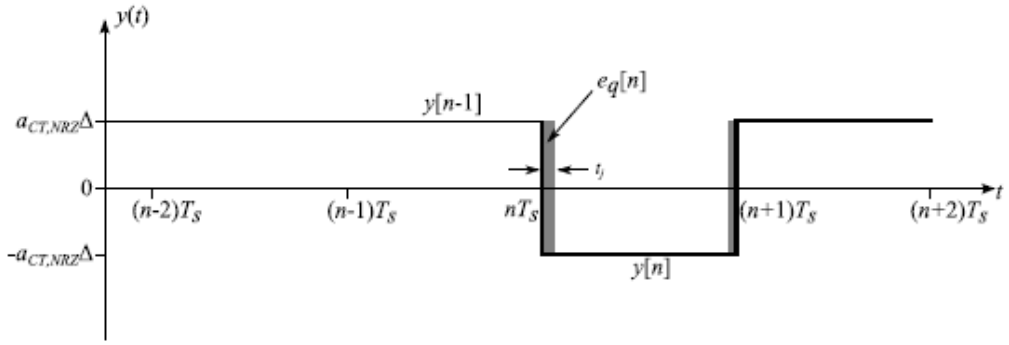

Fig. 4.9: NRZ pulse affected by clock jitter [4].

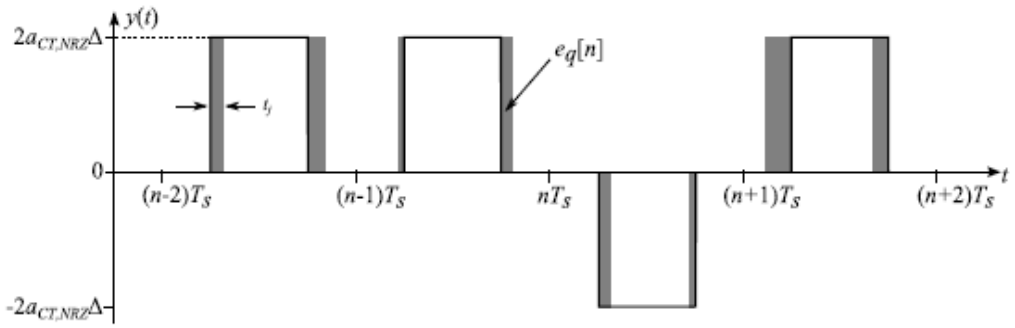

Fig. 4.11: RZ pulses affected by clock jitter [4].

4.4 REDUCING THE EFFECTS OF CLOCK JITTER

A way to improve the jitter performance in CT DSMs is to use multi-bit feedback. As mentioned above in 4.1, multi-bit feedback degrades linearity of the DACs due to mismatch. The NRZ waveform transitions only by one least significant bit (LSB) at most, which reduces the charge errors compared to the single-bit case. Furthermore, increasing number of bits it is possible to reduce clock jitter errors, since every bit yields approximately 6 dB of jitter suppression [4]. The RZ pulses also benefit from multi-bit feedback but less than NRZ pulses, since the transitions are signal dependent and are usually larger than 1 LSB.

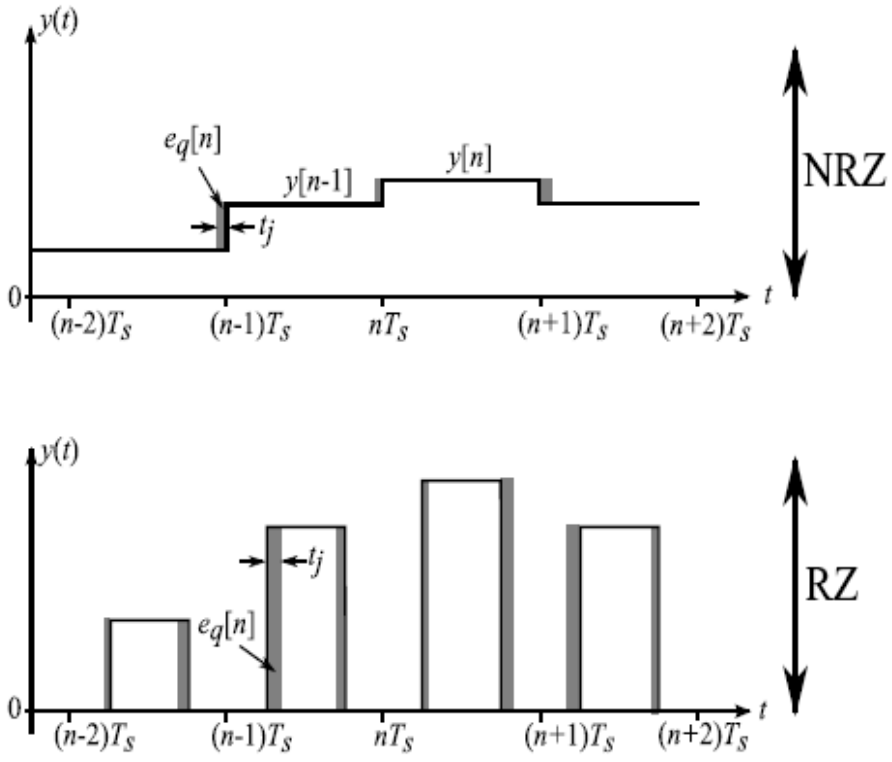

Fig. 4.12: Jittered NRZ and RZ multi-bit pulses [4].

4.5 SWITCHED-RESISTOR DAC

The DAC was implemented using switched-resistor cells [21], connected in parallel to build a multi-bit NRZ DAC. Each of them receives at the input one of the thermometer coded output bits from the flash ADC.

When the output bit is 1, all switches CP1 result closed and all switches CP2 result open. This configuration connects positive and negative DAC references to the positive and negative terminals of the OPAMP inside the loop filter. When the output bit is equal to zero, the situation is just the opposite, in fact the switches CP2 are closed and the switches CP1 are open; in this way, the desired inversion will be created, as the positive DAC reference in now lead into the negative terminal of the OPAMP, and the negative DAC reference into the positive one.

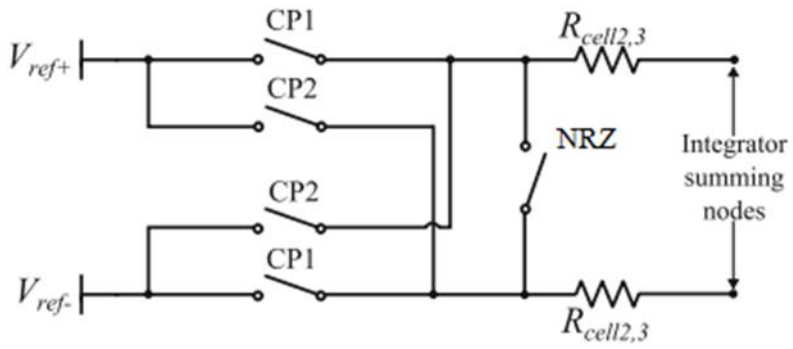

Fig. 4.13: Switched-resistor NRZ DAC cell.

A resistive multi-bit DAC was chosen, as it produces lower thermal noise than the current-steering DAC. In fact, a resistor is less noisy than a MOS transistor working in the active region for the same current, assuming a channel noise factor of unity. The resistive DAC has a low output impedance, which in a multi-

bit implementation may cause distortion due to the code dependent output impedance in a differential implementation, whose linearity is retained by DWA technique.

4.6 FLASH ANALOG-TO-DIGITAL CONVERTER

Among the different parts of a low power electronic system, the highest power consumers are still analog and mixed-signal blocks. An analog-to-digital converter (ADC) is such a block, and one having a fundamental importance due to the required interface between the analog and digital domains.

To achieve very high sampling rates, a 4-bit flash ADC is employed as the quantizer of the DSM. A resistor ladder is used to generate the threshold voltages. The ADC requires 2^N-1 comparators, where N is the number of bits. All comparators convert their bits simultaneously during once clock cycle; it is a parallel conversion.

The output of the flash ADC is represented by a thermometer code. For this reason a VerilogA block, which converts the ADC output in binary code is employed.

4.6.1 ADVANTAGES AND DISVANTAGES

The advantage of this architecture is its conversion speed, but for large number of bits the architectural complexity increases exponentially and the mismatch in comparators and resistors hard to handle.

The flash architecture is not the most power-efficient quantizer. The common use of flash quantizer in CT-ΔΣ modulators is explained by desire to avoid the excess-loop-delay issue owing to its fast speed [30].

In the next chapter, performances with a successive-approximation (SAR) quantizer will be studied.

4.7 PERFORMANCE IN TERMS OF SNR

The targeted SNR is 60 dB over a 500 kHz bandwidth. The most appropriate way to increase the SNR DSMs is to increase the OSR [4]. To achieve the targeted SNR, while keeping the sampling frequency as low as possible, a 4-bit quantizer was used. This choice together with a 2nd-order loop filter resulted in a sampling frequency of 16 MHz and an OSR of 16.

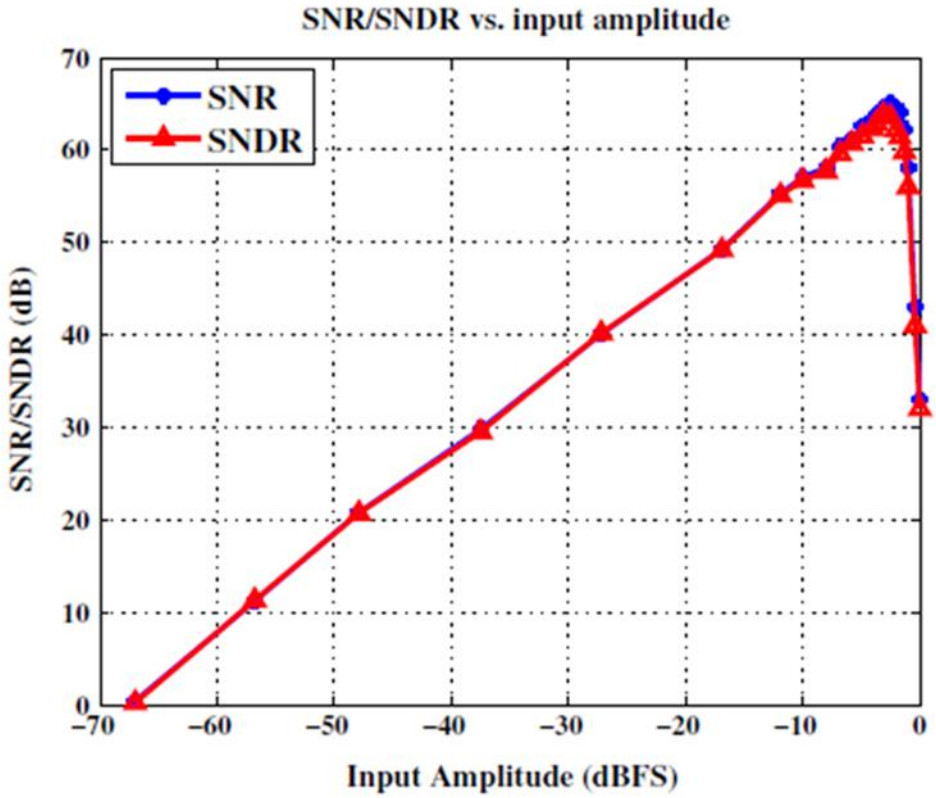

Fig. 4.14: Measured SNR and SNRD [7].

The Fig. 4.14 shows the plot of SNR and SNDR (signal-to-noise distortion ratio) vs. the input amplitude.

To calculate the SNR of the ΔΣ modulator, a process of outputting data from Cadence to Matlab was used. The data from Cadence must be written to a file and after Matlab can import the data from the written file.

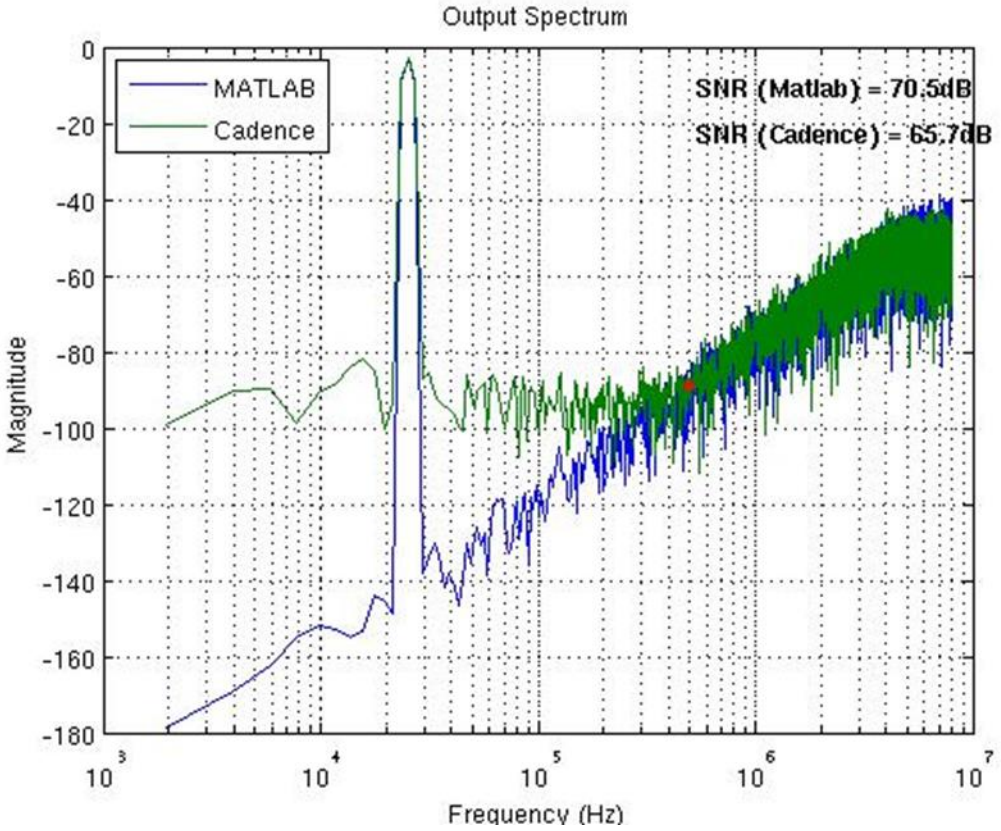

Fig. 4.15: Output spectrum of the modulator employing flash quantizer.

In Fig. 4.15, a comparison between output spectrum from Matlab and the one from Cadence, is shown, for an input signal amplitude of $-3dBFS$, 8192 point FFT with a Hann window. The difference between the noise floor in Matlab and the one in Cadence is evident. This is because including thermal noise in Matlab simulation was not possible. The modulator achieves a maximum SNR of 65.7

dB for an input signal of -2.5 dBFS, and a maximum SNDR of 64 dB for an input signal of -3 dBFS (Fig. 4.14). The circuit consumes $76\mu W$ [7]. The well-known figure-of-merit, $FOM = P_{Tot}/(2^{ENOB}2f_b)$, $ENOB = (SNDR - 1{,}76)/6{,}02$, yields a FOM of 59 fJ / conv.

A post-layout simulation of the overall ΔΣ modulator with the flash quantizer was carried out (Fig. 4.16). It employs just the OPAMP layout.

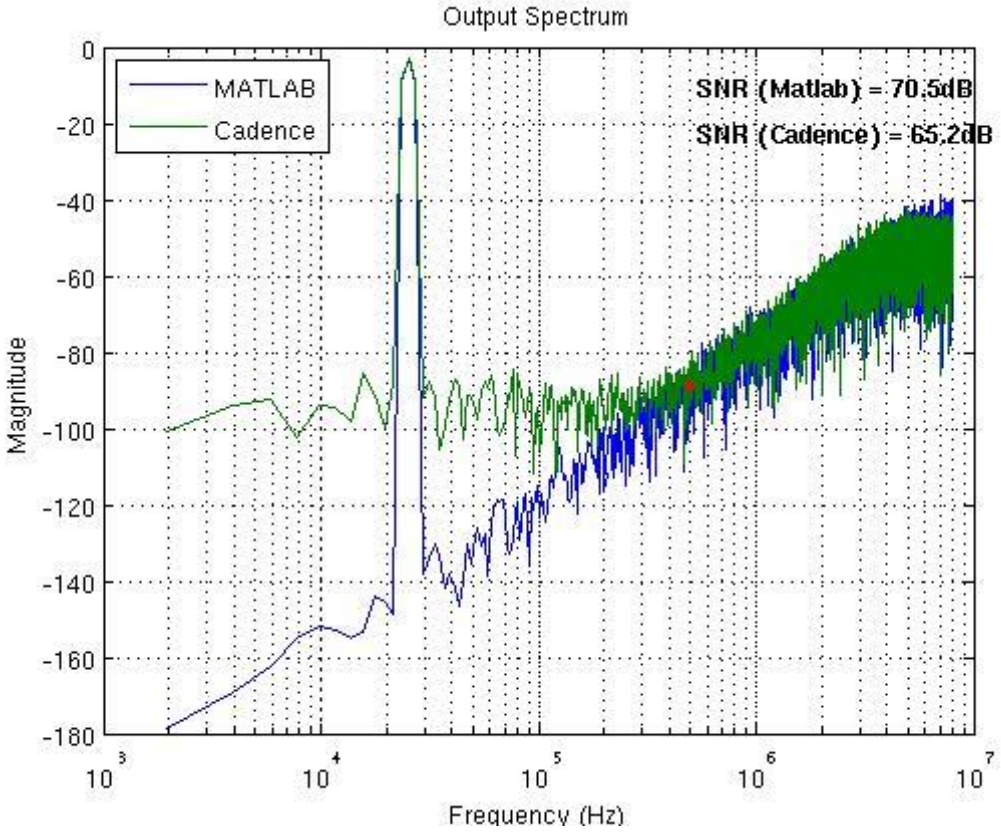

Fig. 4.16: Post-layout output spectrum of modulator employing flash-quantizer.

5. DSM modulator employing a SAR ADC

As shown in the previous chapter, for reducing the quantization error and relaxing the jitter requirement, the multi-bit quantizer can be employed in DSMs. But, for a large number of bits, the power consumption can become an issue especially if the flash architecture is used to implement the quantizer. In this chapter a low-power 2nd-order CT DSM with a 4-bit quantizer implemented with the successive approximation register (SAR) architecture is presented. It is more power efficient than the flash architecture.

5.1 BENEFITS OF SAR QUANTIZER

Replacing the flash quantizer in a DSM, with a SAR quantizer it is possible to save power and area. This is achievable since for an N-bit quantizer, only one comparator, clocked with a higher frequency than the sampling frequency, replaces 2^N comparators in the flash quantizer. In fact, compared with an N-bit flash quantizer, a SAR quantizer needs to be clocked N times faster to achieve similar throughput [30]. This results in an N- fold power consumption increase for a single comparator. Assuming that the quantizer power is proportional to the comparator power and the number of comparators, the ratio between the SAR quantizer power and the flash quantizer power will be $N/2^N$. This means that for

the same throughput, the SAR quantizer consumes less power. This ratio becomes more significant as the number of bits increases.

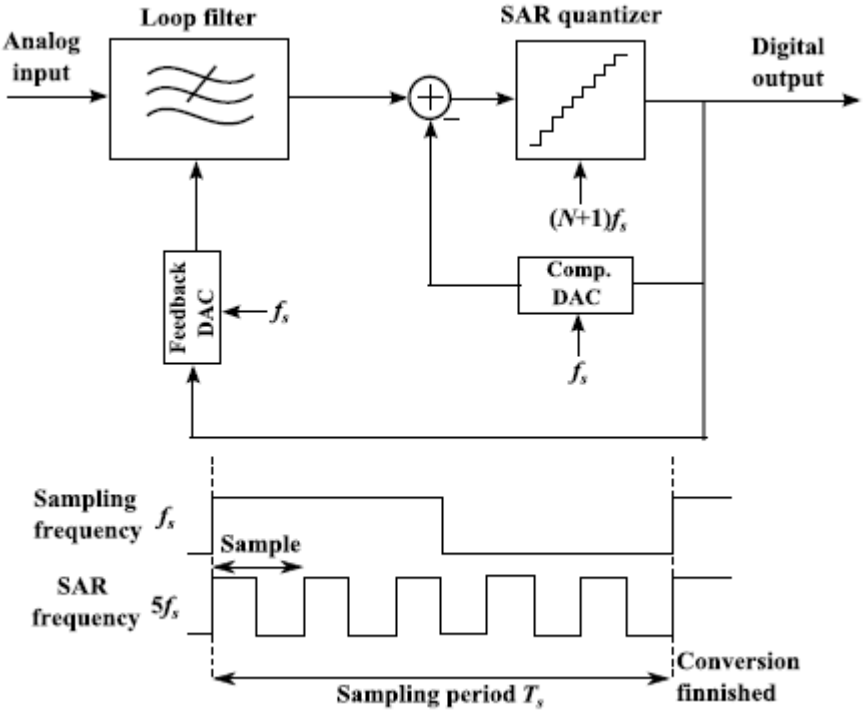

Fig. 5.1: Block and timing diagram of a CT DSM with a SAR quantizer [4].

Since successive approximation analog-to-digital conversion causes a delay proportional to the number of bits and the clock frequency, the quantizer needs to be clocked at a higher frequency to keep the conversion time less than one sampling period. The loop delay compensation DAC and the summing operation have been realised using switched capacitor techniques, while the main DAC is current-mode and uses the NRZ pulse scheme, like in the CT DSM with the flash quantizer. The delay of the SAR quantizer has to be contained within one

sampling period as it is not possible to fully compensate for larger loop delays. If the clock frequency for the SAR quantizer is chosen to more than (N + 1) f_s, the loop delay will not exceed one sampling period as shown in the timing diagram in Fig. 6.1 for N = 4. The issue is the generation of the clock, which requires additional power and area and a delay-locked loop (DLL) for synchronization [4]. To avoid the generation of the high frequency clock, asynchronous control was adopted in this work [4].

5.2 CIRCUIT IMPLEMENTATION

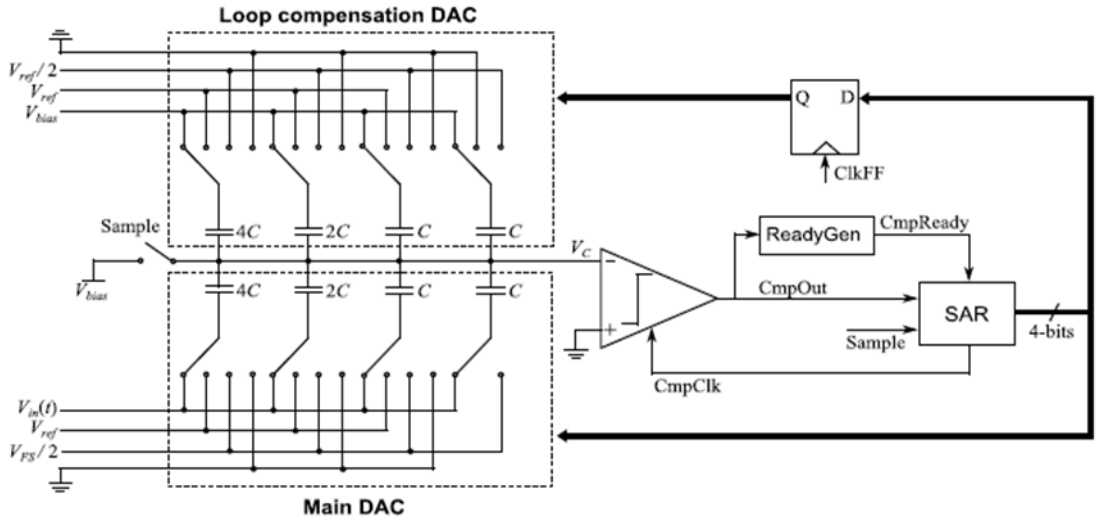

Fig. 5.2: Asynchronous SAR quantizer.

The 4-bits successive approximation register analog-to-digital converter (SAR ADC) has three major analog parts: an input-sampling circuit, a digital-to-analog converter (DAC) and a comparator. The input-sampling circuit is merged with the DAC. When it comes to power dissipation, both comparator and SAR logic

circuits of a SAR ADC benefit from CMOS technology scaling. This is, however, not always the case for the DAC. The size of the capacitors in the DAC is a function of several parameters; the smallest capacitor of the DAC, which is referred to as the unit capacitor, has a lower limit set by the technology. It should be sufficiently larger than the parasitic capacitances of transistors and wirings. The total capacitance must satisfy the thermal noise requirements, often expressed in the form of kT/C noise [31]. The unit capacitor of each DAC is 50fF.

The loop delay compensation DAC has been realized using the SC technique and embedded together with the main DAC. The compensation DAC can be identical to the main DAC, since the compensation coefficient in 4.2.1 was set to 1.

The compensation digital-to-analog converter (CDAC), which affects the system performance of speed and linearity, occupies the most area in successive approximation register (SAR) analog-to-digital converter (ADC). A tri-level charge redistribution technique is proposed to save the silicon cost and power as well. Both the main and the compensation DAC employ the tri-level charge redistribution technique to reduce the power consumption and improve the settling time [34].

Charge sharing between the capacitors in the main and the compensation DAC implements the required summing operation in the quantizer [4]. All capacitors have binary weighted values, i.e., C, 2C, 2^{n-1}C. The last two capacitors having the

value C are connected so that the total capacitance of the n+1 capacitors is 2C. During the conversion phase, it can be shown that after charge sharing, the following voltage is present at the input of the comparator

$$V_C = \frac{1}{2}(-(V_{IN} - V_{CDAC}) + V_{MDAC}) \quad (5.1)$$

where V_{MDAC} and V_{CDAC} are, respectively, the voltages from the main and the compensation DACs. The SAR quantizer determines the output bits by the comparison between $V_{IN} - V_{CDAC}$ and V_{MDAC}. Charge sharing results in power savings as the implementation of the active summation amplifier is avoided.

5.2.1 THE TRI-LEVEL CHARGE REDISTRIBUITION

During the sampling phase, the input signal is sampled on the capacitor array of the main DAC just as for the conventional charge redistribution. During the determination of the first bit, the bottom plates of all capacitors are switched to $V_{ref}/2$ instead of V_{ref}, which consumes less energy from the reference, being the middle point between V_{ref} and ground. Instead the top plates are floating and settle to V_{BIAS}-V_{IN}+$V_{ref}/2$. The input signal is also compared with $V_{ref}/2$. The voltage stored on the effective series capacitor of the array, which is equal to C, keeps being zero. So this step does not consume any switching energy.

If the input is larger than $V_{ref}/2$, 2^NC will be switched from $V_{ref}/2$ to V_{ref} so that the input can be compared with $3/4V_{ref}$. The energy drawn from V_{ref} in this up-transition step is [34]

$$E = \frac{1}{2} C V_{ref}^2 \tag{5.2}$$

If the input is smaller than $V_{ref}/2$, $2^N C$ will be switched from $V_{ref}/2$ to ground so that the input can be compared with $1/4V_{ref}$. In this down transition step there is no capacitor connected to V_{ref} and therefore no energy drawn from V_{ref}.

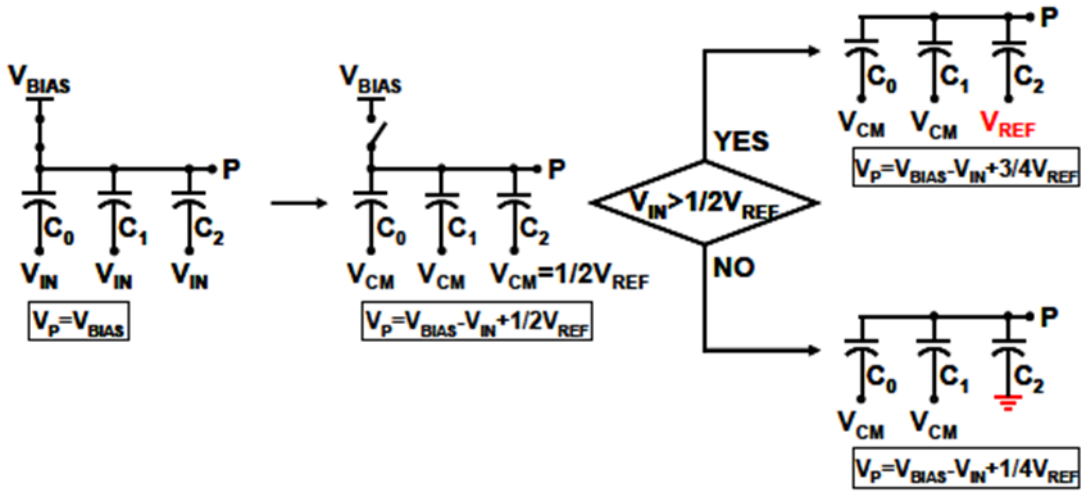

Fig. 5.3: Tri-Level Charge Redistribution DAC.

It is obvious that the tri-level DAC consumes much smaller switching energy drawn from Vref than the conventional DAC on average [34].

C_2 is switched to V_{ref} or ground based on the first bit decision. If the input signal is larger than $1/2V_{ref}$, the MSB is equal to 1 and C_2 is switched to V_{ref}, which makes the next digital estimate become $3/4V_{ref}$. The input voltage is then compared with $3/4V_{ref}$. The next comparator result determines the second bit. If the input is larger than $3/4V_{ref}$, the second bit will be 1 anc C_1 will be switched to V_{ref}. With the settling of C_1, the next digital estimate becomes $7/8V_{ref}$. If the input

is smaller than $3/4V_{ref}$, the second MSB will be 0 and C_1 will be switched to ground, settling the next digital estimate $5/8V_{ref}$. The similar process is followed for the remaining bit. The tri-level based DAC has intrinsically one more bit resolution than the conventional DAC. At the end of the conversion interval, all the capacitors are connected to V_{IN}, *Sample* is connected to ground, and the converter is ready for another cycle.

Another advantage of the tri-level charge redistribution is the reduction of the total capacitance by half, which also results in energy savings (5.2) compared to the conventional approach assuming the same unit capacitance. Furthermore, the settling time is also improved since the capacitors are either switched in the same direction or one at the time.

The tri-level based DAC adds an additional error with respect to the conventional charge redistribution DAC, due to the precision by which $V_{REF}/2$ is calculated. This resulting non linearity noise can be neglected because it is shaped by the modulator, being the DAC placed after the integrating loop filter.

5.3 TIMING OF THE SAR OPERATION

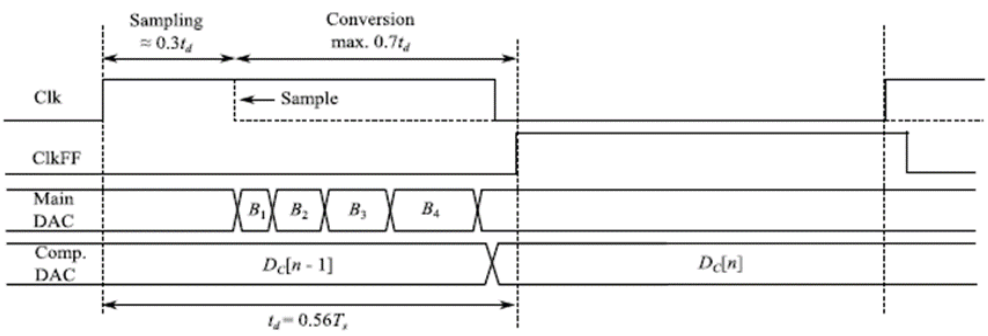

Fig. 5.4: Timing diagram.

During the sampling phase, the main DAC samples the input signal V_{IN} while the loop compensation DAC holds the previous value $D_C[n-1]$. After the sampling phase, the conversion phase starts and the four bits B_1-B_4 are successively determined. Since the operation is asynchronous, the duration of each bit is determined by the delays in the comparator, SAR-register and the control logic. The first bits are resolved quickly as the comparator handles the largest signal. Naturally, the LSB takes the longest time for the comparator to resolve. When the last bit has been determined, the conversion is finished and the compensation DAC is updated. The sampling phase occupies around 30% (10.5ns) of the loop delay while the remaining 70% (24.5ns) are left for the conversion phase.

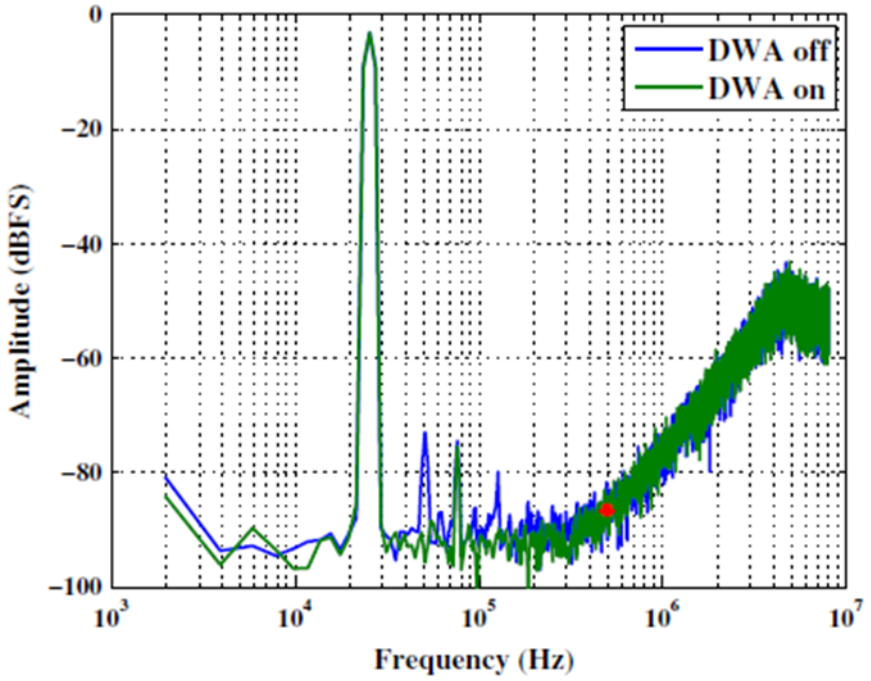

Fig. 5.5: Output spectrum for a -3dBFS input signal [7].

One consequence of restricting the implemented loop delay to 0.56Ts is that there is not much time left for the DWA after all the time margins. Therefore,

DWA was omitted in this design; this was possible since, from previous implementations, it became evident that the DAC mismatch did not affect the performance significantly (Fig. 5.5). If the DWA algorithm is inactivated, a 2nd-order harmonic at -73 dBFS and a 5th-order harmonic at -80 dBFS appear in the spectrum. This shows that the DWA algorithm successfully mitigates for the mismatch errors in the DAC unit elements.

5.4 DYNAMIC COMPARATOR AND READY GENERATION

The comparator is crucial for the overall power consumption. The two-stage dynamic comparator, in Fig. 5.6, is used. The first stage is a differential amplifier, which suppresses the noise from the second stage. The second stage is a positive feedback latch. When the clock is low, the comparator compares the inputs and when the clock is high the comparator is reset. Since there is no static biasing, only dynamic power is consumed which makes the comparator energy efficient. To further reduce the power consumption, high-Vt devices have been used.

Since the implemented logic in this ADC is asynchronous, a ready-indication from the comparator is used to control the timing of the state-machine. As shown in Fig. 5.6, the two outputs of the latch (OUTP and OUTN) are pre-charged low. As soon as the comparator has taken a decision, one of the two outputs will go high. A logical NOR operation detects this low-to-high transition and generates

an active-low ready-indication as shown in Fig. 5.6. A combination of high- and low- transistors is used in the NOR-gate to ensure that the output is valid before the ready-signal.

The *Ready* signal is generated by monitoring the two comparator outputs and deciding which output goes high as shown in Fig. 5.6. When the comparator has taken a decision, one of the outputs will go high and the NOR gate will detect this by generating an active-low ready indication.

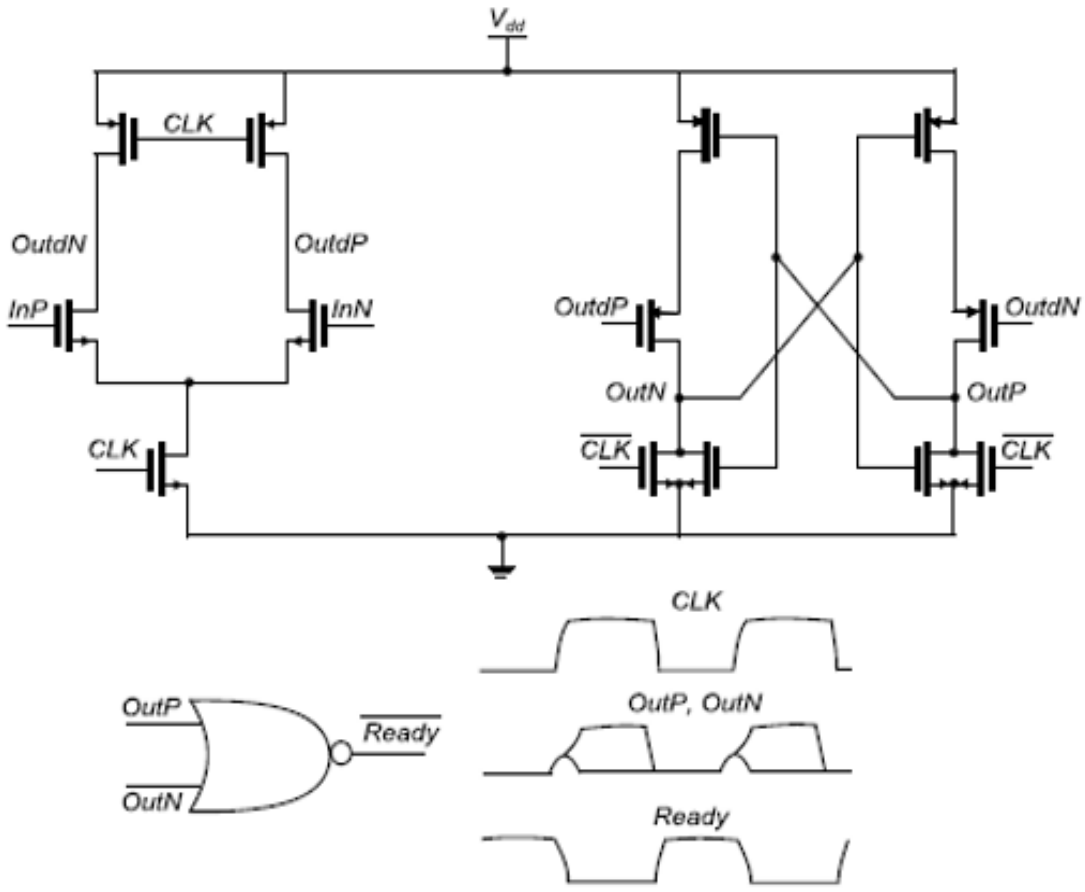

Fig. 5.6: Comparator and ready signal generation [4].

5.5 SAR

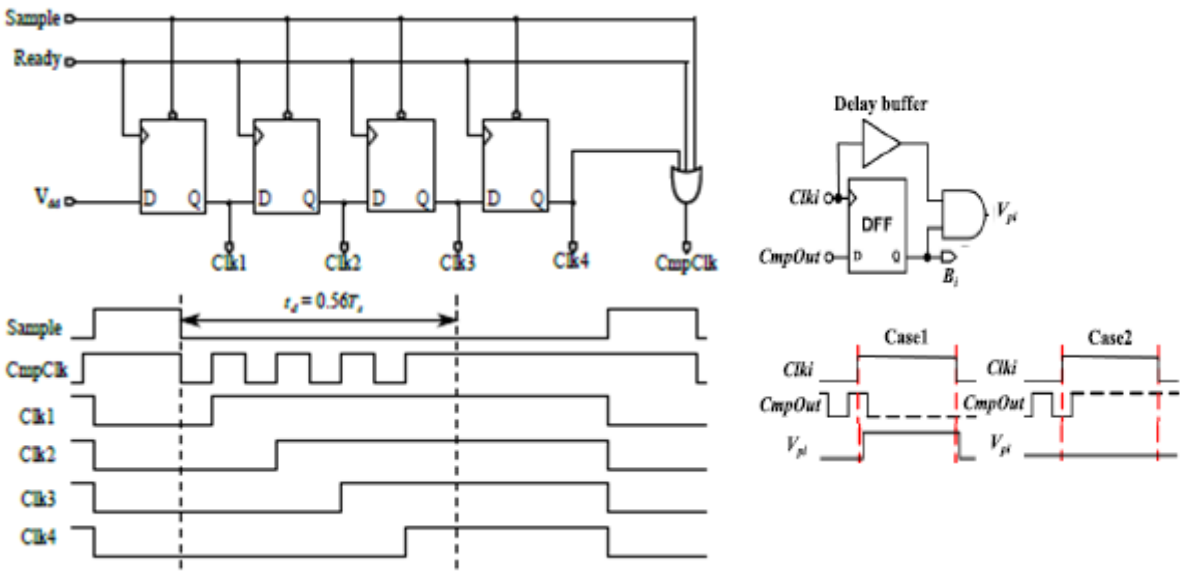

Fig. 5.7: SAR logic and timing diagrams [39].

In Fig. 5.7 the asynchronous SAR register together with the timing diagram is shown. The signals *Clk1* - *Clk4* are generated successively and used by the DAC control logic. A three-input OR-gate generates the asynchronous clock to the comparator.

When the sampling phase is over, or when a comparison has been detected, the OR-gate causes *CmpClk* to transition from low to high to reset the comparator. Furthermore, *Clk4* is the last signal generated and is also used to reset the comparator at the end of conversion. The flip-flop is used to sample the comparator output at the rising edge of *Clki*. If the comparator output is high, the relevant capacitor is switched from Vref /2 to Vref while for a low comparator output, the capacitor is switched to ground. The delay buffer is used to ensure

that Clki triggers the AND-gate after the output of the flip-flop has stabilized. In this way unnecessary transitions are avoided.

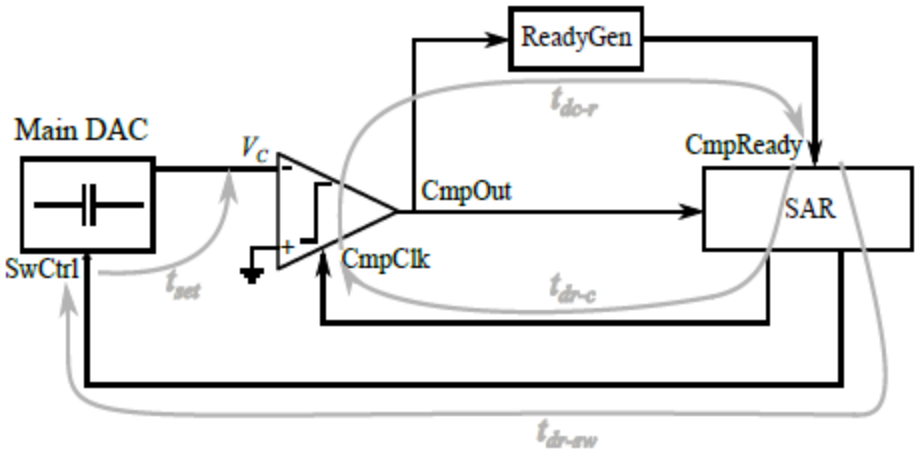

Fig. 5.8: Block diagram illustrating the asynchronous operation [39].

Looking at the Fig. 5.8, it is simple understanding better the asynchronous operation in the SAR quantizer. As soon as the sampling phase is over, *CmpClk* will transition from high to low indicating that the comparator can start the comparison. After a comparator delay, one of the outputs goes high (in this case OutP) and *Ready* is generated. The delay from *CmpClk* to *Ready* is denoted as $t_{dc\text{-}r}$. The rising edge of *Ready* triggers two parallel processes:

1) *CmpClk* is pulled down after a delay of $t_{dr\text{-}c}$ to reset the comparator and indicate that the conversion is finished. Next, *CmpClk* pulls down *Ready* after a delay of $t_{dc\text{-}r}$. This process repeats until the end of the conversion period. It is

assumed for simplicity that $t_{dr\text{-}c}$ and $t_{dc\text{-}r}$ are symmetrical for both rising and falling edges. Both delays determine the pulse widths of *CmpClk* and *Ready*.

2) The logic of the SAR register is updated to set the determined bit, which in turn changes the position of the switch controlling the relevant capacitor in the main DAC. The delay from *Ready* to the switches is denoted by $t_{r\text{-}sw}$ and is dominated by the delay of the flip-flops. When the switches change position, the main DAC settles to a stable value after the time t_{set}.

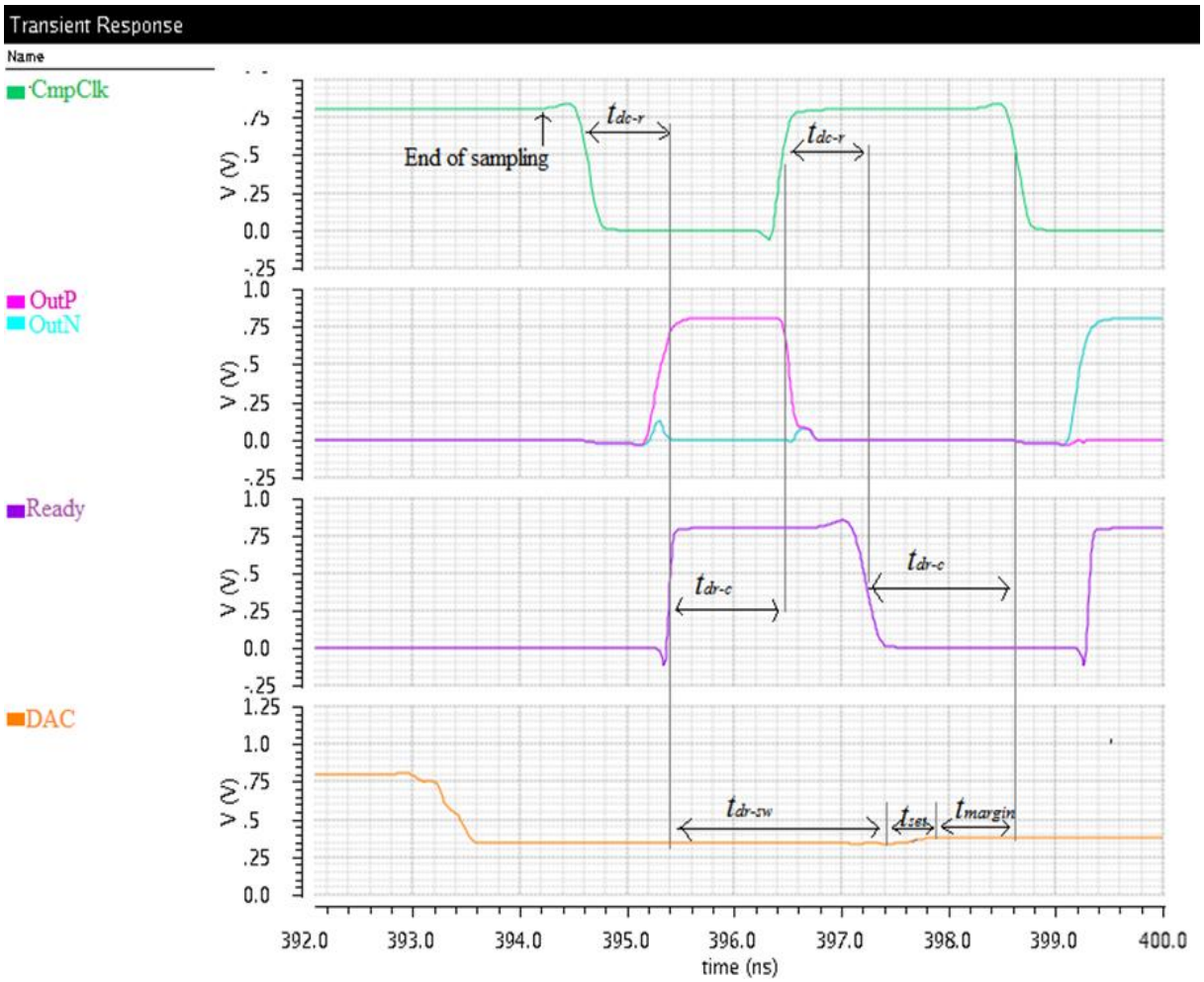

Fig. 5.9: Simulated internal signals of the SAR quantizer.

Correct operation is ensured only if the second process has finished before the next falling edge of *CmpClk*, which marks the beginning of the next conversion. Therefore, the following condition must be fulfilled:

$$2t_{dr-c} + t_{dc-r} > t_{dr-rw} + t_{set} \tag{5.3}$$

The delays $t_{dr\text{-}c}$ and $t_{dc\text{-}r}$ can be increased to fulfil (5.3) by inserting delay lines with devices using larger than minimum lengths. Since asynchronous operation completely relies on delays, it is important to simulate the SAR quantizer over process variations to ensure that all timing requirements are met.

5.6 PERFORMANCE

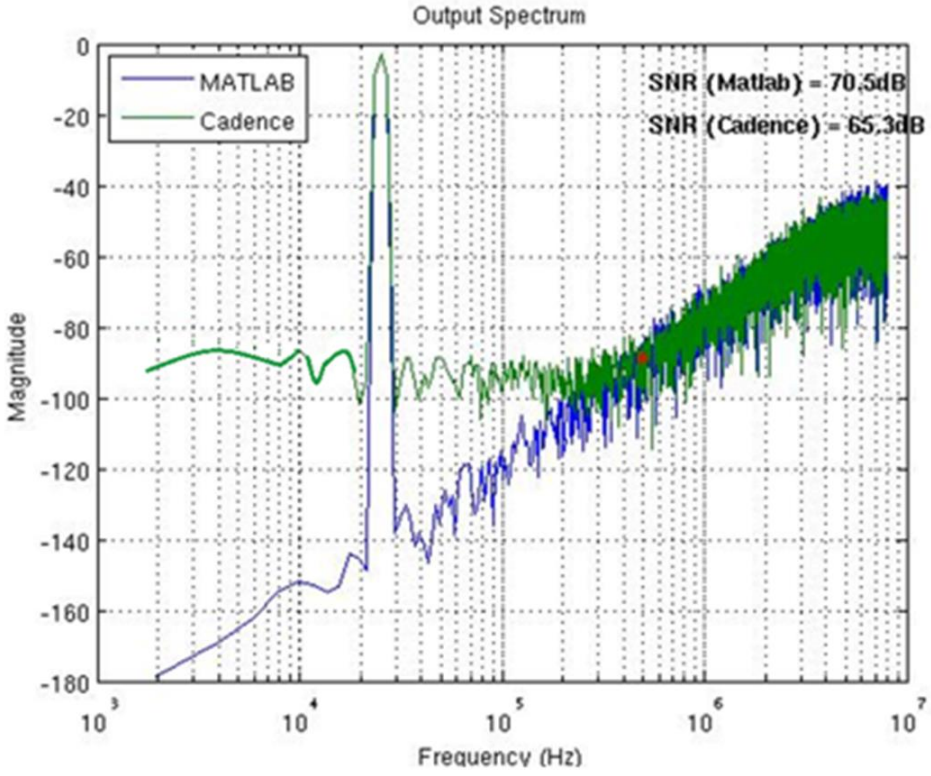

Fig. 5.10: Output spectrum of modulator employing SAR quantizer.

By employing the SAR architecture, the quantizer power consumption was reduced by 40% [4] compared to the flash quantizer, employing in the previous modulator. The simulated output spectrum of the DSM including thermal noise is shown in Fig. 5.10 for an input signal amplitude of -3 dBFS. The simulated SNDR was 65 dB over a 500 kHz bandwidth. This results in a figure of merit of 47 fJ/conv., considering the total power equal to $69\mu W$.

Conclusions

This thesis has presented a 2nd-order loop filter using a single operational amplifier, for reducing power consumption of the overall modulator. The usage of the single operational amplifier loop filter has resulted in a DSM with a performance that is well within the system requirements of the ULP radio. Other amplifier architectures could also be investigated and optimized to further reduce the power consumption. Furthermore, the reduction of the quantizer power consumption is also of interest and has been accomplished by replacing the commonly used flash quantizer with an asynchronous SAR quantizer.

Reference	**Process** (μm)	**Supply Voltage** (V)	**BW** (MHz)	**SNDR** (dB)	**Power** (mV)	**FOM** (fJ/Conv)
[39]	0.18	1	0.024	92	0.352	210
[40]	0.04	1.2	1.92	80	1.91	64
[45]	0.18	1.8	0.024	91	0.09	65
[46]	0.18	1.8	0.024	89	0.122	110
[43]	0.090	1.2	1	62	0.89	433
[42]	0.065	0.8	0.02	91	0.23	198
This modulator	0.065	0.8	0.5	65	0.069	47

Table 1: Performances of the proposed DSM compared with previous work.

The main goal of the loop filter is to reduce the power consumption while still achieving a 2nd-order shaping of the quantization noise. . The concept has been implemented in a 65nm CMOS 2nd-order 4-bit CT ΔΣ modulator, achieving a peak SNDR of 65 dB over a 500 kHz bandwidth while consuming 76 μW, when

the CT DSM employs the flash quantizer and 69 μW in the case in which the flash quantizer is replaced by an asynchronous SAR quantizer.

A performance summary and comparison with other relevant DSMs is shown in Table 1.

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