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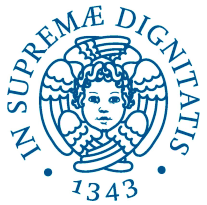

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Development of a high bandwidth PET data acquisition system based on last generation FPGA architecture

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LAUREA MAGISTRALE IN FISICA

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Abstract

Positron Emission tomography (PET) is a nuclear medical imaging technique which allows non-invasive quantitative assessment of biochemical and functional processes. Its purpose is to determine the distribution of radioactive tracers, chosen depending on the tissues and organs of interest, injected the patient body. The physical principle behind the PET is the detection of the two photons generated by electron positron annihilation due to a β^+ decay. The PET is one of the most useful tools to investigate the biology for cancer and cardiac disorders, and to perform molecular imaging. Its best feature is sensitivity: it is the most sensitive technique for medical molecular imaging. This thesis aims at proposing a method for improve the count rate performance of the IRIS PET scanner, a new preclinical system developed on the Department of Physics at the University of Pisa. The IRIS scanner is a data acquisition system based on FPGA (Field Programmable Gate Array) developed with an high modularity and flexibility. It is composed by 16 detectors, 16 data acquisition boards (DAQ) and 1 motherboard.
As of today, the detectors are able to count $0.8{\cdot}10^6$ single events per second, while the DAQ boards are able to transfer to the motherboard the data produced by 0.8 10^6 counts per second and the motherboard is able to transfer to the Host-PC the data produced by $1.1{\cdot}10^6$ counts per second. Thus, the maximum rate of photons that could be detected is $0.8{\cdot}10^6$ photons per second. For a PET scanner, this maximum rate is very important because place limits on the sensitivity and on the *Noise Equivalent Count Rate* (NECR) of the system and its performance when a tracer with a high activity is used. The bottleneck is given by the detectors and by the link between the DAQ boards and the motherboard. Research for improve the detectors are planned, thus my study has been focused on improve the link between the DAQ boards and

the motherboard and the link between motherboard and Host-PC.
In order to upgrade the first link, a new protocol for the data transfer has been investigate. This upgrade would be poorly invasive because does not require hardware changes. To implement this new protocol some firmware components have been developed. After a complete simulation, these components were integrated in the DAQ and the motherboard firmwares. Several tests were made for verify the data integrity and the data transfer performance.
In order to upgrade the link between the motherboard and the Host-PC, the performance of a new family of FPGA was investigate. The main characteristic of this FPGA family is the integration of an Hard Processor System (HPS) in it. The combination of FPGA and HPS is very powerful because it allows to implement custom logic in the former and use the latter for high level control. High-throughput data paths between the HPS and FPGA fabric provide interconnect performance otherwise infeasible with dual-chip solutions.
The board used for test the performance of this new platform is the general purpose prototyping board Arrow SoCkit.
A separated set of firmware components has been developed to implement the communication interface between the FPGA and the HPS. Also, a separated set of driver has been developed to control these components through the HPS.
Several test was made for verify the data transfer speed. The HPS-FPGA bridge was tested with a loop-back through two 64 bits FIFOs components. Eventually, a Ethernet test has been conducted to measure the data transfer speed between the HPS and the Host PC.
The results obtained are: a 30% performance improvement on the link between the DAQ boards and the motherboard without any hardware changes; a potential 200% performance improvement reachable with the change of the FPGA family. The maximum count rate reachable with the firmware change is 1.1 Mcps, while the maximum count rate reachable with the change of the FPGA can potentially becomes 3.5 Mcps.
Currently, with the implementation of the new firmware the bottleneck becomes the FPGA-Host link, but when a data acquisition system based on the new FPGA family will be developed the bottleneck will become the detectors. Thus, developments to improve the detectors speed will be necessary in the future.

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Introduction

Positron Emission tomography (PET) is a nuclear medical imaging technique, which allows non-invasive quantitative assessment of biochemical and functional processes. Its purpose is to determine the distribution of radioactive tracers, chosen depending on the tissues and organs of interest, injected the patient body. The physical principle behind the PET is the detection of the two photons generated by electron positron annihilation due to a β^+ decay.

The PET is one of the most useful tools to investigate the biological nature of cancer and heart/cardiac deseases and to perform molecular imaging. In particular, it is the most sensitive technique for medical molecular imaging.

PET systems are constantly under development. The first system was able to produce images with resolution as low as 1/2 cm, where modern systems reach a resolution of few millimeter. The *state of the art* in nuclear instrumentation is the PET/CT, which combines a PET scanner and a CT scanner in a single device. The current main technological challenges consist of increasing the detection efficiency, reducing the dead time of the systems and managing all data produced. Therefore, hardware research is fundamental in order to reduce the dead time and increase the throughput of data acquisition system.

IRIS PET scanner is a new preclinical system developed on the Department of Physics at the University of Pisa. The IRIS scanner is a data acquisition

system based on FPGA (Field Programmable Gate Array) developed with an high modularity and flexibility. It is composed by 16 detectors, 16 data acquisition boards (DAQ) and 1 motherboard.

This thesis work reported aims to propose a method for improve the IRIS data acquisition system. The fundamental physics of PET imaging systems, in terms of acquisition system design, are reported in the first chapter. In particular, the physics of positron emission and annihilation, and the effect of positron range and photon non-colinearity in coincidence detection on spatial resolution, are described. Furthermore, detector technologies suitable for detecting 511 keV annihilation photons are introduced and the geometries for typical PET scanner configurations are discussed.
In the second chapter, the *state of the art* of PET scanners is explored. Special attention is paid to the technological solutions and characteristics of previous PET scanners. The conceptual design solution of the IRIS data acquisition system is discussed. Various characteristics and performance are analysed.
The third and the fourth chapters describe my studies for implement hardware upgrade on the IRIS data acquisition system. The first upgrade presented will be at the firmware level. This upgrade would be poorly invasive because does not require hardware changes. The second upgrade presented will be at the hardware level. This one can bring forth a new generation of PET data acquisition systems in which both characteristics of FPGA and hard processor (CPU) are exploited. Some tests will be reported in order to verify the potentiality of these new tools.

Eventually, results and proposal on further research will be discussed.

CHAPTER 1

Positron Emission Tomography (PET)

Positron Emission Tomography (PET) is an imaging technique based on studying the spatial distribution of a radioactive tracer. It uses the β^+ decay of specifics radioactive tracers bound to metabolic molecules injected, in the patient body. Since these molecules diffuse in patient body, according to specific physiological processes, PET is able to provide information on metabolic function of tissues and organs.
When a β^+ decay generates an e^+, this quickly annihilates, producing two 511 KeV photons . Annihilation photons are emitted with an angle of 180°, hence it is possible to trace a straight line between the two emitting points (detection points) in order to localize the photons source. The detection is usually made by scintillators coupled with position-sensitive photomultiplier tubes (PSPMT).
The kinetic of the β^+ decay, the intrinsically stochastic nature of photons and the equipment accuracy impose some limits on the imaging PET technique. These limits affect the spatial resolution attainable with PET and can be thought as a blurring of the reconstructed images.
In the following chapter will be presented the theoretical aspects and some of the limits of the PET technique.

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1.1 Physics of PET

Positron Emission Tomography (PET) is one of the most widespread medical imaging techniques. The technique is based on studying the spatial distribution of radioactive tracers injected into a biological tissue. Some of the most frequently used radiotracers are listed below, with their main decay properties [4] (table 1.1). All these nuclides produce positrons by β^+ decay with a minimum β^+ *Branching Fraction* of 89% [5].

Nuclide	$E_{e^+}^{max}$ [MeV]	$T^{1/2}$ [min]	Average $Range_{e^+}$ [mm]
11C	0,959	20,4	1,1
13N	1,197	9,96	1,5
15O	1,738	2,03	2,5
18F	0,633	119,8	0,6
68Ga	1,898	68,3	2,9
82Rb	3,40	1,25	5,9

Table 1.1: Radioactive tracer with its decay properties [4].

1.1.1 β^+ decay

The β^+ decay process is shown in equation (1.1). In this process, a proton from a radionuclide is converted into a neutron, by releasing a positron and

an electron neutrino.

$$ {}^{A}_{Z}X \rightarrow {}^{A}_{Z-1}Y + e^{+} + \nu_e \tag{1.1} $$

Lifetimes τ of β^+ unstable nuclide vary between a few ms and 10^{16} years. They strongly depend on both the energy E that is released ($\frac{1}{\tau} \propto E^5$) and on the nuclear properties of mother and daughter nuclides [8]. β^+ decay is a two particles decay, the kinetic energy of the atom Y is negligible, thus the all energy is mainly shared between the positron and the neutrino. Positron, and neutrino, have a kinetic energy that follows a continuous distribution of energy, figure 1.1, from zero to an upper limit, the endpoint energy.

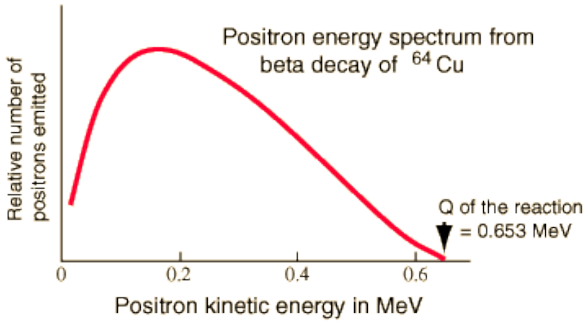

Figure 1.1: The energy spectrum for an electron in a β decay [16].

After the emission, the positron starts to lose its kinetic energy by interacting with the surrounding matter. This occurs mainly by ionisation events with other atoms and scattering. This energy loss continues until the positron reaches thermal energy and finally annihilates with an electron[1]. When that happens electromagnetic, radiation is given off, in the form of two photons emission[2][11]. The energy of these two photons is $0.511 MeV$ and the directions of emission are close to 180° to each other (figure 1.2). In fact, photons

[1] A metastable intermediate species called positronium may be formed by the positron and electron combination. Positronium is a hydrogen-like element composed by a positron and an electron that revolve around their combined centre of mass. It has a mean life of around 10^{-7} seconds.

[2] Also three photons can be emitted but with $< 1\%$ probability.

are emitted in opposite directions to conserve momentum, which is near zero before the annihilation. This effect places a fundamental lower limit to spatial resolution of positron emission tomography and will be studied in section 1.3.2.

Another limit to spatial resolution comes from the finite distance travelled by the positron before annihilation (positron range). This aspect will be examined below.

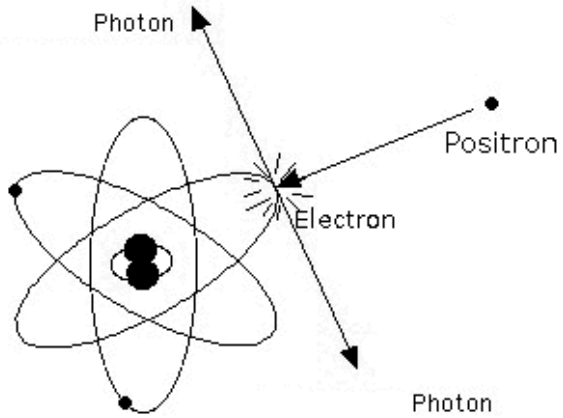

Figure 1.2: Schematic diagram of a positron electron annihilation.

Positron range

Positron range is defined as finite distance travelled by a positron before annihilation. Its path is extremely tortuous as shown in figure 1.3. All the deflections shown in figure 1.3 are mainly due to the following types of collision:

- *Inelastic collision: excitation and ionization*
- *Multiple Coulomb elastic scattering from the nucleus*
- *Hard elastic collision*

Interactions with atomic electrons are present too, but their effect is negligible. Estimating the positron range is possible by simulating positron

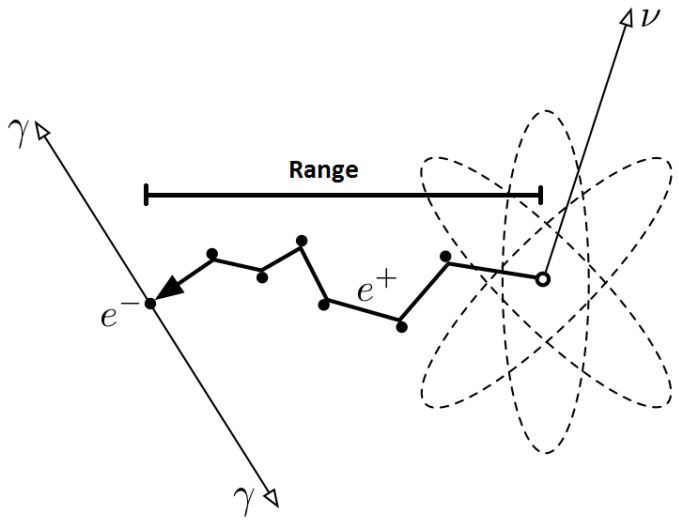

Figure 1.3: Schematic diagram of a positron range in β^+ decay.

trajectories with a Monte Carlo simulation and by constructing their annihilation point distribution (figure 1.4 [24]). Annihilation point distributions (positive side) can be fitted well to the sum of two exponential functions of the form equation 1.2 with the parameters C, k_1 and k_2 given in table 1.2 [24].

$$P(x) = Ce^{-k_1 x} + (1 - C)e^{-k_2 x} \tag{1.2}$$

With this distribution, it is possible to calculate the FWHM that is used to estimate the positron range. Having the range distribution it is possible to apply image reconstruction corrections with an improvement in the spacial resolution.

	^{18}F	^{11}C	^{13}N	^{15}O
C	0,516	0,488	0,426	0,379
$k_1(mm^{-1})$	0,379	0,238	0,202	0,181
$k_2(mm^{-1})$	0,031	0,018	0,014	0,009

Table 1.2: Best fit parameters of equation 1.2 [24].

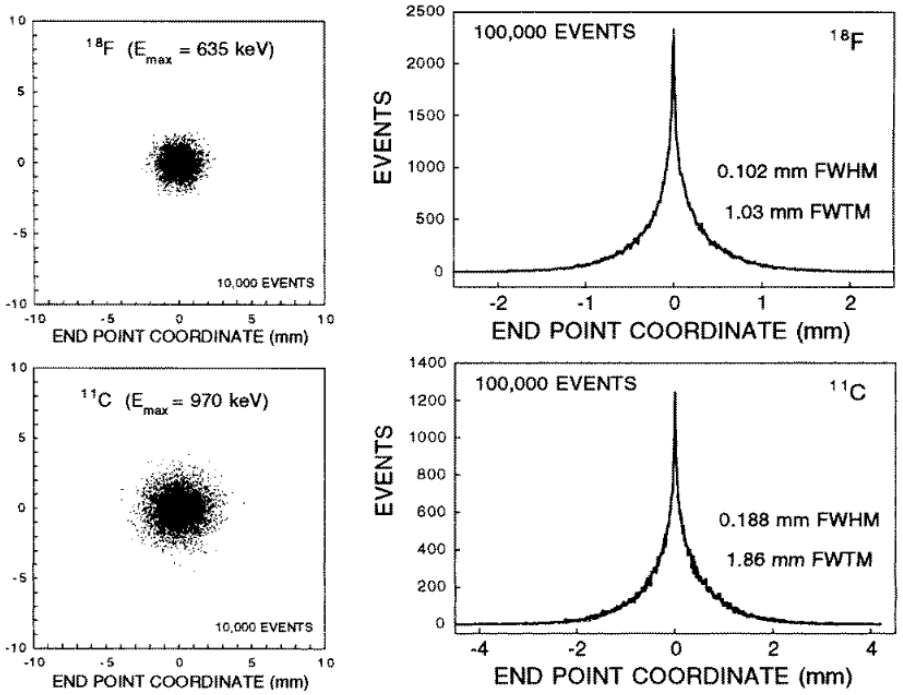

Figure 1.4: Left: simulated distribution of positron annihilation coordinates in water projected onto a plane for ^{18}F and ^{11}C sources. Right: histogram of the positron annihilation coordinates projected on the x axis[24].

1.1.2 Photon-matter interaction

Depending on their energy, photons interact with matter according to four main mechanisms[3]:

- *Rayleigh scattering: coherent interaction between a photon and an atom;*
- *photoelectric effect: interaction between a photon and an orbital electron;*
- *Compton effect: incoherent interaction between a photon and an orbital electron;*
- *pair production: photons conversion in electrons and a positrons.*

[3]There are also others mechanisms of interaction, like triplet production and photonuclear reactions, but they require energies greater than ∼10 MeV.

The cross-section of these four mechanisms depends on the photon energy (figure 1.5). Thus, it is possible define four energy ranges in which only one mechanism can be identified as dominant. For energies less than 50 KeV, the Rayleigh scattering is the main mechanism; between 50 KeV and 100 KeV, the photoelectric effect dominates; at energies above 100 KeV and less than 2 MeV, the Compton effect dominates; at last with energies greater than 2 MeV, the main mechanism is the pair production[1].

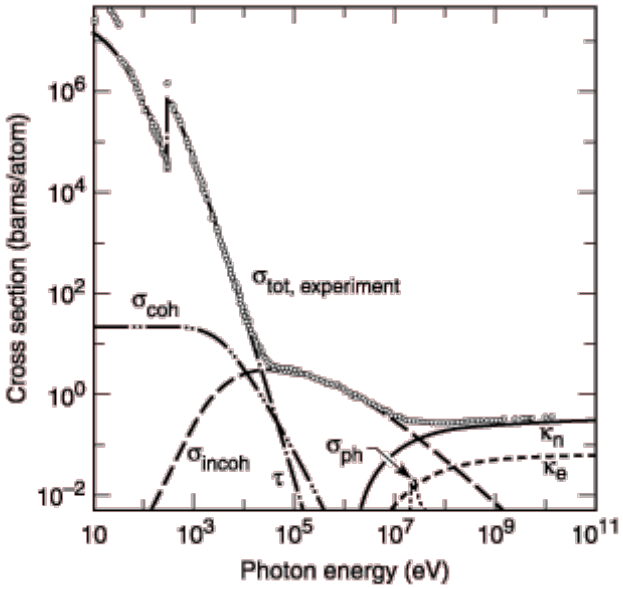

Figure 1.5: Total photon cross section σ_{TOT} in Carbon, as a function of energy, showing the contributions of different processes: τ, atomic photoeffect (electron ejection, photon absorption); σ_{COH}, coherent scattering (Rayleigh scattering); σ_{INCOH}, incoherent scattering (Compton scattering); K_n, pair production, nuclear field; K_e, pair production, electron field; σ_{ph}, photonuclear absorption [17].

All the previous mechanism are microscopic effects that influence at same time the two macroscopic effects: attenuation and scattering of photons. The attenuation is the gradual loss of intensity of the photons beam and takes the form of a mono-exponential function:

$$I(x) = I_0 e^{-\mu x} \tag{1.3}$$

where I_0 is the initial intensity of the beam, $I(x)$ is the intensity of the beam after it passed through a material of thickness x and μ is the linear

attenuation coefficient corresponding to specific material.
Differently, photons scattering happens when photons deviate from their initial straight trajectory with, sometimes, a change of their initial energy. The deviation from the initial trajectory can affect the spatial resolution. However, since scattering affect the photon energy, it can be detected and can be corrected (section 1.3.2).

1.2 PET scanners

PET scanners are typically constructed as a cylindrical array of detectors arranged in full or partial rings typically enough to accommodate small animals or body parts (figure 1.6).

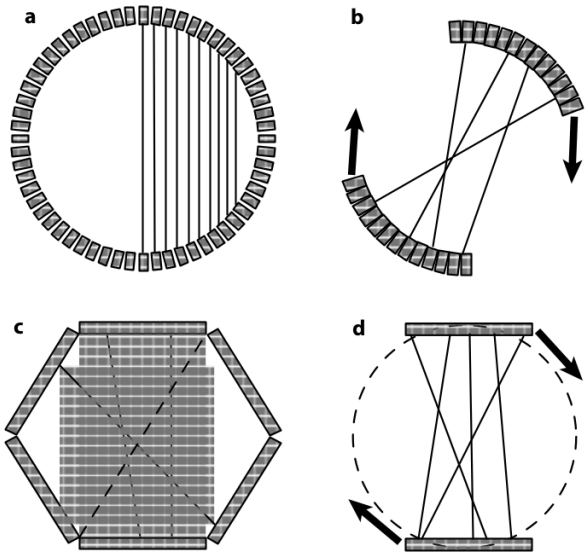

Figure 1.6: Common PET scanner architecture: (a) full-ring circular system, (b) partial-ring system with continuous rotation, (c) full-ring of flat detectors system (typically 6–8) and (d) flat detectors system with "step-and-shoot" rotation (geometry used for gamma camera PET and some other prototype systems using multi-wire proportional counters). LORs not measured indicated by the dashed line. [3].

A PET scan is based on the detection in coincidence of the two 511 KeV annihilation photons that originate from the β^+ emitting sources. A coincidence is detected when two photons arrive to two opposites detectors in

a defined time window. Typically, the time window changes from a few ns to 20 ns depending on the type of detector.
The line that connects the two detectors is referred to as *line of response* or LOR (figure 1.7). The annihilation point occurred somewhere along this line. To reconstruct a complete image, a large number of LORs is needed at different angles.

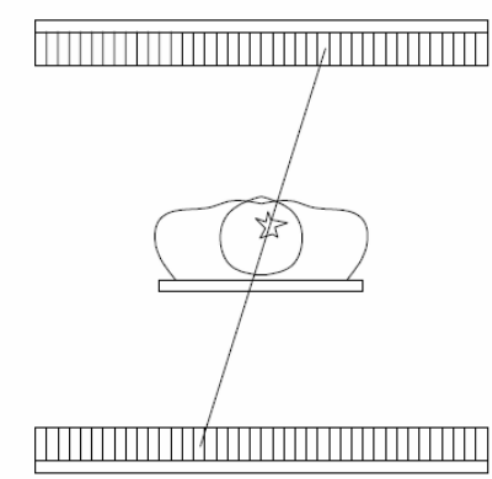

Figure 1.7: Line of response in a PET scanner.

Detectors must have a very high efficiency for detecting annihilation photons and, also, must give precise information on the location of the interaction. They must have also the ability to discriminate events in a short time interval and must determine their energy.
To comply with all these requirements common detectors use scintillators coupled with a photomultiplier tube.

1.2.1 Detectors

Scintillators

Scintillators are transparent materials that emit light in the visible region when they absorb radiation energy. Scintillators have four main properties which are crucial for their application in PET[15]:

- *stopping power at 511 KeV,*

- *scintillation efficiency ,*
- *scintillation rise and decay time,*
- *energy resolution.*

The stopping power of the detector determines the mean distance between the photon entrance and its stops after the complete deposition of its energy. It depends on the density and effective atomic number (Z_{eff}) of the detector material. The stopping power of a scintillator is the major factor in the choice of a scintillator.

Scintillation efficiency η is defined as:

$$\eta = \frac{Energy\ \ of\ \ scintillation\ \ light}{Energy\ \ deposit} \tag{1.4}$$

It is a measure of the light output in relationship with the energy deposited in crystals.
The scintillation decay starts after a photon interacts with an atom of the detector material, and the atom is excited to a higher energy level, which later decays to the ground state, emitting visible light. This decay time is the time required for scintillation emission to decrease to $1/e$ of its maximum. It varies with the material of the detector. The shorter the decay time, the higher the efficiency of the detector at high count rates.
The intrinsic energy resolution is affected by inhomogeneities in the crystal structure of the detector and random variations in the production of light in it. A good energy resolution is needed to efficiently reject events that scattered in the patient before entering the detector.
Table 1.3 lists some proprieties of the most commonly used scintillator materials.
The light emitted by scintillators is then detected by photomultiplier tubes. The scintillators crystal can be of two type: continuous and pixellated. Depending on its type, the scintillators light can be read by photomultiplier with two different scheme: the direct scheme or the light sharing scheme.

Photomultiplier tubes

Photo-multiplier tubes represent the oldest and most reliable technique to measure and detect low levels of scintillation light. Figure 1.8 shows its basic scheme.

Material	NaI(Tl)	BGO	LSO	YAP:Ce
Density (g/cm^3)	3.76	7.13	7.4	5.37
Light Yield %NaI(Tl)	100	15	75	55
Effective Z	51	74	66	33
Decay time (ns)	230	300	40	27
Photoelectric fraction at 511 KeV	18 %	44%	34 %	4.4 %
Fluorescence GMFP[a] (mm)	0.32 - 0.44	0.68 - 0.93	0.41 - 0.56	0.13 - 0.17
Electron range at mean deposited energy (mm)	0.43	0.18	0.19	0.07
GMFP at 511 KeV (mm)	2.85	1.04	1.15	2.18
Peak wavelength (nm)	410	480	420	370
Energy resolution (%)	9, 4	26, 6	10, 5	4, 4

[a]Gamma Mean Free Path.

Table 1.3: Properties of some scintillator materials [32][26][18][27][19].

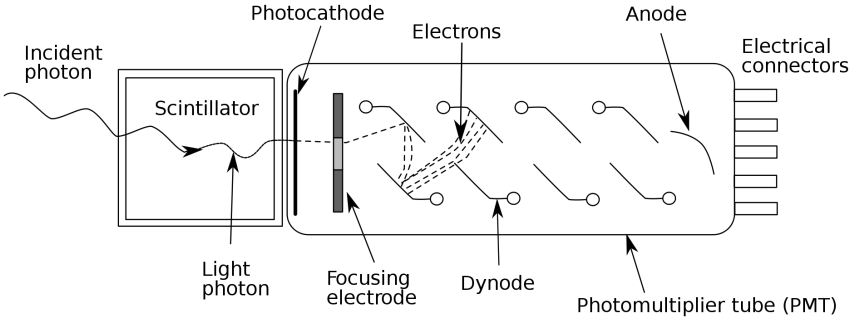

Figure 1.8: Scintillator and photomultiplier tubes schematization in individually coupling.

A vacuum enclosure with a thin photo-cathode layer at the input window is placed at the front of the device. The material of the input window limits the spectral sensitivity in a short wavelength region. The photo-cathode is normally made of a deposited photoemissive semiconductor. When an incoming scintillation photon deposits its energy inside the photo-cathode, it triggers the release of photo-electrons. These are accelerated and focused onto the first dynode where they are multiplied by emission of secondary electrons. This process is repeated at each dynode. Eventually, secondary electrons emitted from the last dynode are collected by the anode. Ideally, the current amplification of a photomultiplier tube having the number of dynode stages n and average secondary emission ratio m per stage will be $G = m^n$.
The high gain obtained with this technique leads to a very good SNR[4] ratio for low light levels.

Read-out

Three basic configurations of read-out exist depending on the scintillator crystal.
For a continuous crystal, the detector consists of one crystal and one position-sensitive PMT. In this configuration, the scintillation light diffuses and reflects throughout the crystal and generates different signals in the PMT (figure 1.9a). The position of the photon interaction is individuated by an appropriate weighted mean of the individual PMT signals.
This weighted-mean position calculation can be also useful when pixellated crystals are used. In this configuration, the light created in one pixel is confined in it and collected on a smaller area on the PMT plane (figure 1.9b). This is an efficient technique for reducing the number of electronic processing channels required because the pixels can be read from a lower number of PMT. Also, with this weighted-mean calculation, the detector intrinsic spatial resolution will be finer than the PMT anode readout pitch and on the order of the crystal pixel size.
At last, with pixellated crystals an individual read out can be used (figure 1.9c). In this case, all light created in one crystal is focused on one PMT. As for the previous configuration, the detector spatial resolution is determined by the crystal width.

[4]Signal to Noise Ratio

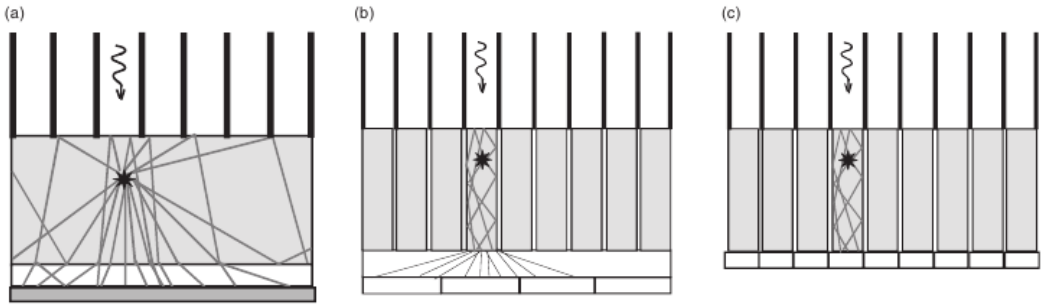

Figure 1.9: Possible read out schemes of crystals from PMT in detectors.

1.3 Theoretical limits of PET scanner

1.3.1 Coincidences

In PET imaging, data acquisition consists on detecting coincidences generated by annihilation photons. Due to the instrumentations limits, real coincidences are affected by undesirable false coincidences. Coincidences can be of the following four types:

- *true coincidences,*
- *random coincidences,*
- *scattered event,*
- *multiple event.*

A true coincidence results from the detection of two photons originating from a single positron-electron annihilation. A random coincidence is detected when two unrelated photons hit opposing detectors close enough to be recorded within the coincidence timing window. Because they are unrelated, they do not carry any spatial information about the activity distribution. Random coincidences produce an undesired background in the reconstructed image. Another type of noise comes from scattered coincidences. A scattered coincidence is a true coincidence where one, or both, annihilation photons are deviated from their initial trajectory by Compton scattering before they interact with the detector. At last, multiple coincidences are detected when three, or more, photons hit the detector within the coincidence timing window. In figure 1.10 all these types of coincidences are shown.

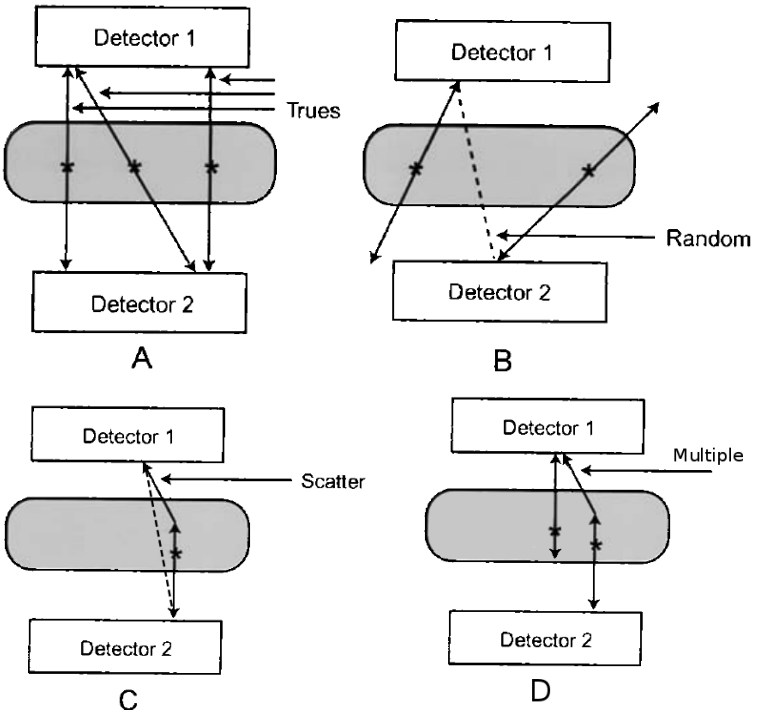

Figure 1.10: Type of coincidences detected: (A) True coincidence events, (B) Random coincidence events, (C) Scattered coincidence events, (D) Multiple coincidence events[22]. For the B and C the LOR measured is the dotted line.

All the previous type of noise sources, can be corrected. Correction for scatter is probably the most difficult correction that is required in PET, mainly because a scattered event is indistinguishable from a true event except on the basis of energy. When an annihilation photon undergoes a Compton interaction in the body and scatters, it will lose some of its energy in the process. If PET detectors only accepted events with an energy of 511 KeV, all scattered events could be eliminated. But this would require a detector with extremely good energy resolution. An additional difficulty in separating scattered events from primary events is caused by the fact that a significant fraction of the primary 511 KeV photons will only deposit a portion of the energy in the detector volume. Although these events are true events, they are detected in the same energy range as scattered events. Thus, if the system would only accept events in a narrow energy window at approximately 511 KeV, the overall detection efficiency of the system would be very poor. Therefore, to maintain a reasonable detection efficiency, most PET systems operate with a relatively large energy window between 350 KeV to 650 KeV,

which also results in the detection of a certain amount of scattered photons. Energy discrimination is most efficient in rejecting low energy, large angle scatter, photons.
For correcting the randoms rate in a particular LOR, the delayed coincidence channel method is used. Here timing signals from one detector are delayed by a time significantly greater that the coincidence resolving time of the system. Therefore, there will be not true coincidences in the delayed coincidence channel, the number of coincidences found is a good estimate of the number of random coincidences. The estimate from the delayed channel may be subtracted from the LOR, or stored as a separate sinogram for later processing. Eventually, to correct the multiple coincidences is the most simple correction. Since the multiple coincidences are distinguishable, they will be discarded.

1.3.2 Spatial resolution

We define spatial resolution the minimum distance at which it is possible distinguish two close point sources in a measurement process. Several factors contribute to the worsening of the spatial resolution in PET imaging. There is not analytical expression to determine the spacial resolution of a PET system given its geometry. However, an attempt to give an early estimation can be found in [25].
It considers four main physical aspects: detector size, positron range, non-collinearity and parallax.
Its simplest form is:

$$R = \sqrt{R_{det}^2 + R_{non-coll}^2 + R_{range}^2 + R_{par}^2 + R_b^2} \tag{1.5}$$

where:

- R_{det} is the intrinsic spacial resolution of the detectors used in the scanner. It is related to the detector size d and is given by $d/2$ on the scanner axis at midposition between two detectors.

- $R_{non-coll}$ is related to the small residual momentum of positron at the end of its range. The two annihilation photons are not emitted exactly at 180° after annihilation process (figure 1.11). The maximum deviation from 180° is $0,25°$ (i.e., $0,5°$ FWHM)[22]. If d is the distance

in cm between two detectors, then this contribution ($R_{non-coll}$) can be calculated as follows:

$$R_a \approx 0,5^\circ \cdot \frac{d}{4} = 0,0022 \cdot d \tag{1.6}$$

- R_{range} is related to the positron range. As explained in section 1.1.1, the site of β^+ emission differs from the site of annihilation. Coincidence detection is related to the location of annihilation and not to the location of β^+ emission. This contribution is determined from the full width at half maximum (FWHM) of the positron annihilation point distribution[24].

- R_{par} is related to the various depth in which the interaction of annihilation photon on crystal could happens. This contribution can be calculated as follows:

$$R_{par} = \alpha \frac{r}{\sqrt{r^2 + R^2}} \tag{1.7}$$

  where r is the distance between center and annihilation point, R is the radius of the ring and α depends by the thickness of detectors. Is important to underline that, as shown in equation 1.7, parallax error is a function of distance between center and annihilation point, thus has a different value in each annihilation point.

- R_b is related to the coupling between scintillators and photodetectors. It is 1 in case on individual read out. It is greater in the others cases.

1.3.3 Dead time

When a photon is absorbed in the crystal and thus interacts, in the PMT an electric pulse is generated. Dedicated analogic and digital electronics are then triggered to process this pulse so as to determining its energy and fine timing. The total time required to complete these steps is defined as the dead time τ. During this time the detection system is unable to process a second event, which will be lost. The loss count increases at high count rates and depends on the acquisition electronics.

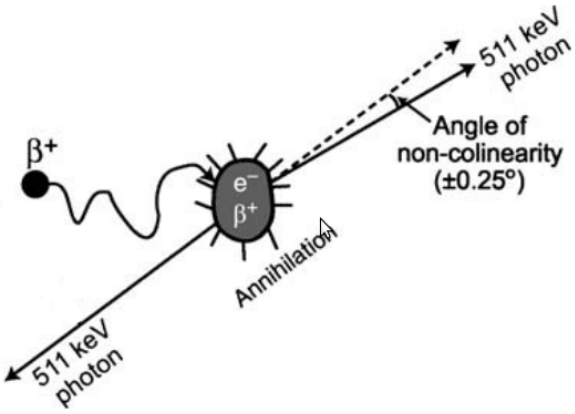

Figure 1.11: Non-collinearity in photons annihilation.

Dead time is a characteristic of any counting system. There are two type of it:*nonparalysable* and *paralysable*.
In the nonparalysable case, when the system is busy, further events have no effect. In the paralysable case, when the system is busy, further events force the system to remains busy for a further amount of time τ.
The relationship between the measured count rate m, the real count rate n, and the dead time resulting from a single event τ is given by the equation 1.8 in nonparalysable system and by the equation 1.9 in paralysable system[21].

$$m = \frac{n}{1 - n\tau} \tag{1.8}$$

$$m = ne^{-n\tau} \tag{1.9}$$

The differences between this two models are shown in figure 1.12. The maximum count rates is $1/\tau$ in nonparalysable model and $1/e\tau$ in paralysable model, so a paralysable system is more affected by the dead time.
It is important to underline that paralyzable and nonparalysable models represent theoretical models, real detector behaviour is likely to fall somewhere in between. It is obvious that the dead time can be reduced by using detectors with shorter scintillation decay time and faster electronics components in the PET scanners. Any improvement of dead time can give a sensible improvement on scanner performances.

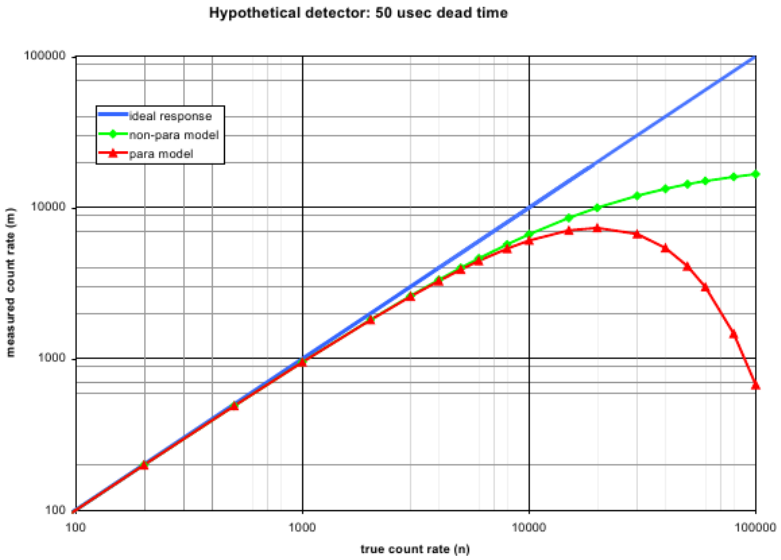

Figure 1.12: Systems performance at high count rates.

1.3.4 Noise Equivalent Count Rate

The image noise is the random variation in pixel counts across the image. It can be reduced by increasing the total counts in the image. More counts can be obtained by imaging for a longer period, injecting more radio tracer, or improving the detection efficiency of the scanner. All these factors are limited by various conditions, e.g., too much more activity cannot be administered because of increased radiation dose to the patient. Imaging for a longer period may be uncomfortable to the patient. The detection efficiency may be limited by the design of the scanner.
A good measure of the signal to noise ratio is provided by the *noise equivalent count rate* (NECR). It is given by:

$$NECR = \frac{T^2}{T + R + S} \tag{1.10}$$

where T, R, and S are the true, random, and scatter coincidence count rates, respectively.
NECR can be used as measure of performance of a PET acquisition system under different operating conditions. A larger NECR indicates a higher ratio of good events to the overall detected events with the same scanning time, which include randoms and scatters. The parameters that affect the measurement of NECR include injected dose, scan time post-injection, patient weight

and scanner design. All these factors impact NECR through their influence on the measured random, true and scatter events.

Also, recent studies have demonstrated that improve the system dead time can increase considerably the NECR. The NECR can be increased up to a 30% when the dead time is dropped by 50%. Moreover, the peak NECR of a faster dead time system is appearing at a much higher dose level[20].

CHAPTER 2

Acquisition system

New progress in PET instrumentation could improve the image resolution and could reduce the amount of radiotracer used. The increase of the detection efficiency, the reduction of the system dead time, and the easy management of all data produced are still the main technological challenges of this powerful technique.
In the following chapter, the PET scanners state of the art is described. Furthermore, IRIS data acquisition system and its possible improvements are disscussed.

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2.1 State of the Art in Acquisition system for PET

One of the most used preclinical nuclear instrumentation is the PET/CT, which combines a PET scanner and a CT scanner in a single device.
The success of these instruments is given by the simple co-registration of images from different equipments. Prior to the introduction of PET/CT, essentially all multimodality imaging systems were based on software fusion techniques. To circumvent the problems given by the co-registration PET/CT integrated system has been developed by several manufacturers. In a PET/CT system both units are mounted on a common support with the CT unit in the front and the PET unit in the back next to the CT unit (figure 2.1).
The PET/CT has another advantage: it provides a fast, low-noise attenuation correction of PET emission data. This attenuation correction is fundamental for the improvement of PET image quality.
Data acquisition in PET/CT is performed in two steps: first the CT scan and then the PET scan. The CT scan takes about 1 minute. The typical time for the entire protocol for PET scan is about 30 minutes.
The PET/CT images are very complementary in preclinical situations. A very small tumor is well detected by PET but can be missed by CT. On the other hand, a large tumor with minimal functional deviation may be seen on a CT image, but may not be detected by PET. In both situations, PET/CT would localize the tumor accurately.

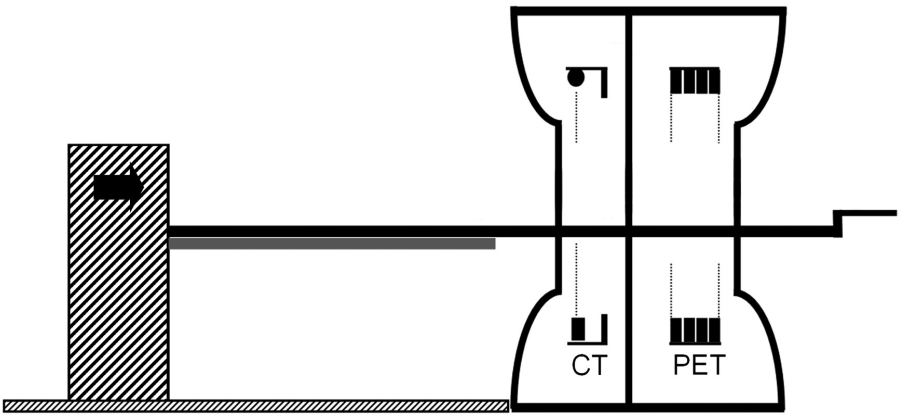

Figure 2.1: PET/CT scanner.

In the past, several preclinical PET scanners were available. Few example are: the microPET FOCUS 220, the ECAT HRRT, the ClearPET, the rPET-1 the Inveon and the NanoPET/CT. The microPET FOCUS 220, manufactured by CTI-Concorde Microsystems LLC, (Knoxville, TN), consists of 168 LSO blocks, which are organized in 4 rings and composed by a matrix of 12 $\times$ 12 crystals with dimensions of 1.5 mm $\times$ 1.5 mm $\times$ 10 mm[23]. The ECAT HRRT, manufactured by Siemens Medical Solutions, Inc. Compared (Berlin, Germany), is a PET scanner made of 8 detector heads, each consisting of 72 $\times$ 104 dual-layer 2.1 mm $\times$ 2.1 mm $\times$ (10 + 10) mm LSO-LYSO crystals[12]. The ClearPET, manufactured by Raytest GmbH (Mannheim, Germany), is composed by a rotating full ring of detectors[9]. It use pixelated crystals made of a LYSO and LuYAP phoswich matrix with two layers. The rPET-1, manufactured by SEDECAL, S.A. (Madrid, Spain), has two rotating, planar block detectors[9]. It use pixelated crystals made of a mixed lutetium silicate (MLS). The Inveon, manufactured by Siemens Medical Solutions, Inc. Compared (Berlin, Germany), consists of 64 detector blocks organized in rings[14]. Each detector module consists of a 20 $\times$ 20 array of LSO crystals of size 1.5 mm $\times$ 1.5 mm $\times$ 10 mm. The NanoPET/CT, manufactured by Mediso Ltd. (Bioscan Inc.), consists of 12 detector modules organized in one ring[31]. Each detector module consists of a 39 $\times$ 81 array of LSO:Ce crystals of size 1.12 mm $\times$ 1.12 mm $\times$ 13 mm.

The main characteristics of all these scanners are summarized in Table 2.1.

	HRRT	microPET	ClearPET	rPET-1	Inveon	NanoPET
Crystal Material	LSO/ LYSO	LYSO	LYSO/ LuYAP	MLS	LSO	LSO:Ce
Crystal Size (mm^3)	2.1 x 2.1 x (10 + 10)	1.5 x 1.5 x 10	2 x 2 x 10	1.4 x 1.4 x 12	1.5 x 1.5 x 10	1.12 x 1.12 x 13
Transverse FOV (mm)	31.2	24.2	144	45.6	10.0	12.3
Axial FOV (mm)	25.35	7.6	110	45.6	12.7	9.48
Slice thick. (mm)	1.22	0.80	1.15	0.77	0.8	0.3

Table 2.1: Comparison between for six scanners[23][12][9][14][31].

More recently the IRIS PET data acquisition system has been developed. It is a new preclinical system developed in the Department of Physics at the University of Pisa. One of the differences between this system and the four scanners previously mentioned is that the IRIS system can be used in two different configurations, with and without gantry rotation. Thus, the IRIS has not a fixed geometry for its detectors (table 2.2). This characteristic gives more flexibility to the system.

System	Geometry	Rotation
HRRT	ring of flat detectors	no
microPET	full ring	no
ClearPET	full ring	yes
rPET-1	planar	yes
Inveon	full ring	no
NanoPET	full ring	yes
IRIS	ring of flat detectors	yes or no

Table 2.2: Geometry differences between PET scanners.

Another interesting comparison is related to the acquisition platforms. For the acquisition platforms two main strategy can be followed:

1. use general purpose hardware (cheapest solution)
2. use custom hardware that allows to obtain better performance (expensive solution)

A summary of the acquisition platforms for the above system is reported in table 2.3.

System	Acquisition platform	Performance	Cost
HRRT	ASIC	excellent	high
microPET	CPU	normal	low
ClearPET	CPU	normal	low
rPET-1	CPU	normal	low
Inveon	ASIC	excellent	high
NanoPET	CPU	normal	low
IRIS	FPGA	very good	medium

Table 2.3: Acquisition platform differences between PET scanners.

System	NECR Peak (Mcps)	Activity (MBq)
HRRT	1.7	96.2
microPET	0.8	170.2
ClearPET	0.07	0.51
rPET-1	0.03	1.35
Inveon	1.67	131
NanoPET	0.43	36
IRIS	0.43	13

Table 2.4: NECR differences between PET scanners[23][12][9][14][31].

Eventually, a comparison from the point of view of the NECR can be done. The NECR peaks are measured following the recommendations of the National Electrical Manufacturers Association (NEMA) NU 4-2008 standard. In table 2.4 a comparison of different systems is reported. From the analysis of the NECR peaks and the activity, it is possible to observe that HRRT, Inveon and microPET systems show the betters values in terms of NECR, as well as the higher activity compared with the other systems listed.

2.2 The IRIS data acquisition system

The main features of the IRIS data acquisition system are an high modularity and flexibility. Some of the main advantages of of the IRIS scanner are:

- *Sensitivity = 9.8 % [250 KeV - 750 KeV],*
- *Spatial resolution = 1.1 mm,*
- *Axial FOV = 94 mm,*
- *Trans-axial FOV = 80 mm,*
- *Energy resolution = 14 %,*
- *Timing resolution = 1.4 ns.*

A simplified schematic diagram of the IRIS system components is reported in figure 2.2. The main components of the system are:

- *radiation detectors,*
- *front-end electronics,*
- *data acquisition modules,*
- *motherboard,*
- *Host-PC.*

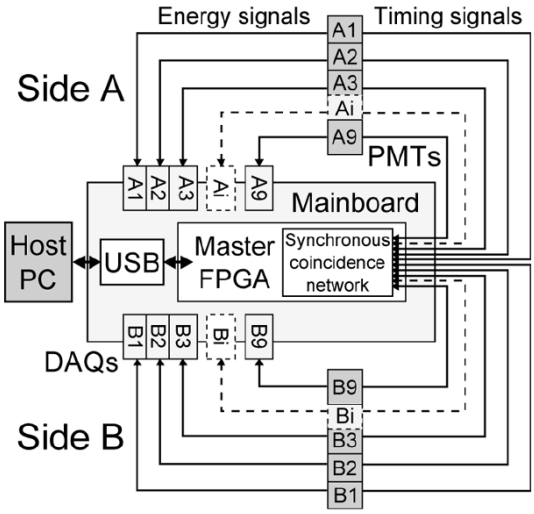

Figure 2.2: Simplified schematic diagram of the IRIS data acquisition system[30].

Each of these components will be described in the following section.

2.2.1 Radiation detectors

LYSO crystal

The LYSO crystal matrix consists of 27 × 26 single crystals. The size of any crystals is 1.6 mm × 1.6 mm × 12 mm and the pitch is 1.68 mm (figure 2.3). As previously reported, LYSO crystals have excellent characteristics for medical imaging applications. The disadvantage of LYSO is a high background count rate from the decay of ^{176}Lu. In fact, the ^{176}Lu isotope has an half-life of $3.6 \cdot 10^{10}$ years and decays emitting: one electron with energy of about 420 KeV and three photons with energies of about 88, 202 and 307 KeV.

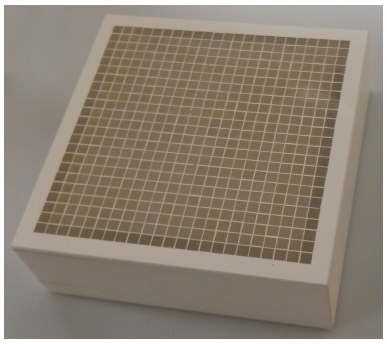

Figure 2.3: LYSO crystal matrix.

Photomultiplier tubes

The used photomultiplier tubes are Hamamatsu model H8500. These photomultiplier tubes have 64 (8 × 8 matrix) anodes (fig 2.4). Each anode has a size of 5.8 mm × 5.8 mm. The size of the effective area is 49 mm × 49 mm. The entrance window is made of borosilicate glass (thickness 1.5 mm). This photomultiplier has 12 stages of dynodes and 64 outputs.

2.2.2 Front-end electronics

The front-end electronics is composed of three different components:

- *symmetric charge divisor,*
- *pulse shape preamplifier,*

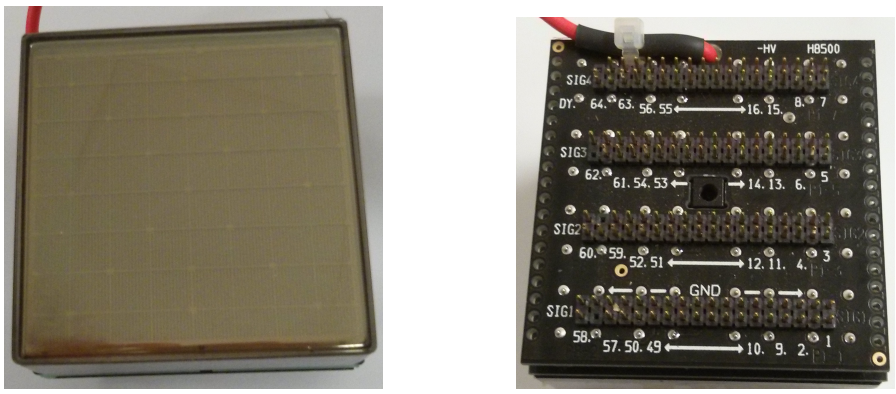

Figure 2.4: The photomultiplier tubes H8500. (Right) The front side of the photomultiplier; (left) the back side of the photomultiplier.

- *constant fraction discriminator.*

Symmetric Charge Divisor (SCD)

The symmetric charge divisor consists of a resistive network (figure 2.5). The SCD reduces the 64 outputs of each PMT in 8 + 8 signals. Therefore, each signal is divided in two by a matrix of equal resistors. This type of charge division involves a degradation of the signals due to the voltage drop caused by each resistors. For this reason, the signals are amplified before going in the pulse shape preamplifier.

Pulse Shape Preamplifier (PSP)

The 16 signals enter a passive resistive chain that further reduces the number of signal to 2 + 2 (S_a, S_b for the X side and S_c, S_d for the Y side). Later these are filtered with a low-pass filter. Finally, these signals are sent to the data acquisition board.
This type of coding is know as Anger coding, the position of interaction of a photon is calculated with the formulas[7]:

$$X_{int} = \frac{S_a - S_b}{S_a + S_b} \qquad Y_{int} = \frac{S_c - S_d}{S_c + S_d} \tag{2.1}$$

Figure 2.6 shows a picture of the board here the PSP and the Constant Fraction Discriminator (CFD) are implemented.

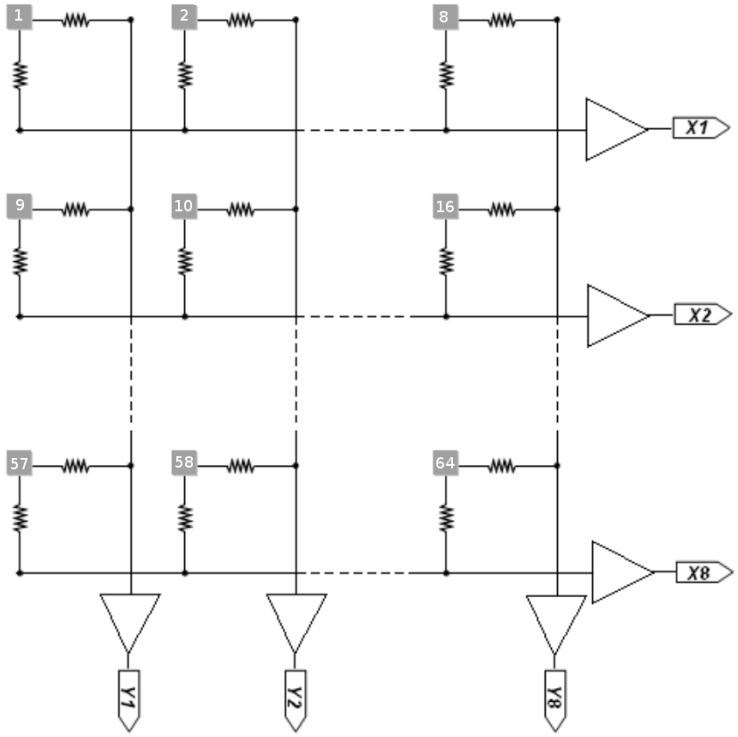

Figure 2.5: The symmetric charge division resistive network.

Constant Fraction Discriminator (CFD)

The last dynode output of the PMT is forwarded directly to CFD. The CFD is one of the components that contributes more to the total system dead time, thus being a critical stage in the overall performance characteristics. A schematic of the circuit is presented in figure 2.7. The last dynode signal is used in three different lines. The first one is attenuated by a fraction λ of its own peak[1]. The second line is delayed of 3 ns. These first two are sent to a comparator. The last line arrives to another comparator without any changes. The second input of this second comparator is an arm threshold. In sum, the CFD produces a digital trigger when the last dynode signal is higher then the arm threshold. This trigger stays high for the time in which

[1]The fraction is usually chosen depending on the PMT output properties. In IRIS system this fraction is set to 14%

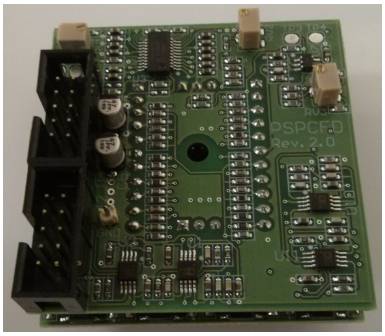

Figure 2.6: Picture of the Pulse Shape Preamplifier (PSP) and Constant Fraction Discriminator (CFD) board.

the last dynode signal is higher then a constant fraction of itself. Eventually, the digital trigger is sent to the motherboard in a differential way in order to reduce the noise.

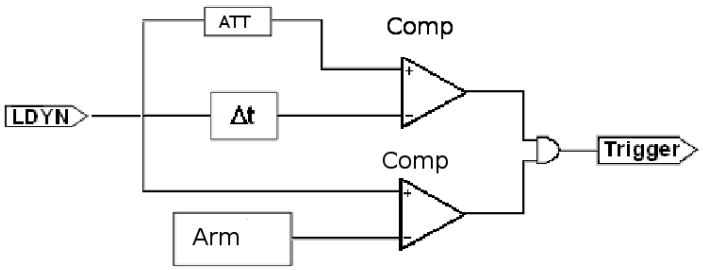

Figure 2.7: Schematic architecture of the Constant Fraction Discriminator (CFD).

2.2.3 Data Acquisition (DAQ)

When the motherboard detects a coincidence event, it triggers the Daq board to starts the event acquisition. Each DAQ board mounts a Cyclone II FPGA (Altera Corp. San Jose CA), which manages the events acquisition. A picture of the DAQ board is showed in figure 2.8. When a trigger is sent to the DAQ board, its FPGA enables four 12 bits ADCs that convert the 4 anger signals in digital signals. While the ADCs are converting the DAQ does not accept further triggers. The 4 digital coordinates are sent to the

motherboard with additional information. The data packet consists of five 16-bits words, thus the coincidence event size is 20 bytes. The structure of one data packet is showed in table 2.5.
The data link between the DAQ boards and the motherboard is obtained with two 16-bits wide parallel buses. The measured bandwidth of this link is 8 MB/s per bus[29]. The communication protocol used for the packet transmission is presented in section 3.1.1.

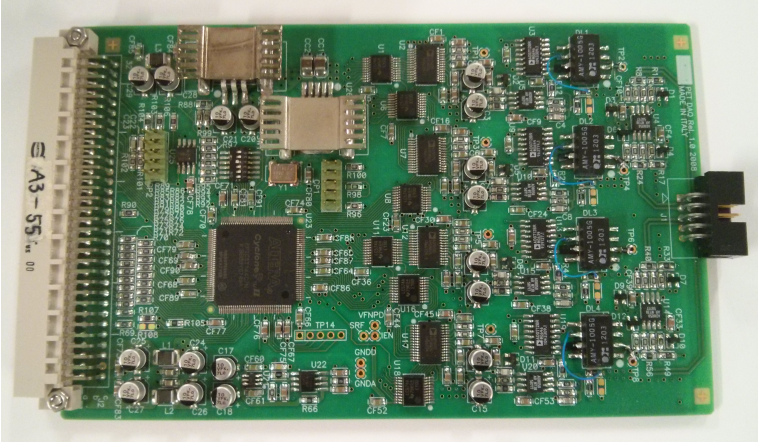

Figure 2.8: The DAQ module.

Data Packet																
Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	c	DAQ and event markers											
1	0	0	0	c	XA											
2	0	0	1	c	XB											
3	0	1	0	c	YA											
4	0	1	0	c	YB											

Table 2.5: Structure of one data packet. Bits 15, 14 and 13 are control bits. Bits labelled with c are programmables bits.

2.2.4 Motherboard

The motherboard mounts a Stratix III FPGA (Altera Corp. San Jose CA). It is the main FPGA that manage the acquisition. The Stratix III is a high-end model that provides high memory sources, high I/O pin count

and high performance. The main processing tasks carried out by this FPGA consist of data transfer, coincidence network and event tracking. The data link between motherboard and Host PC is based on an USB 2.0 controller. The maximum value of the USB 2.0 controller bandwidth is 60 MB/s. The real bandwidth in IRIS data acquisition system is 21 MB/s[29]. Figure 2.9 shows a picture of the motherboard.

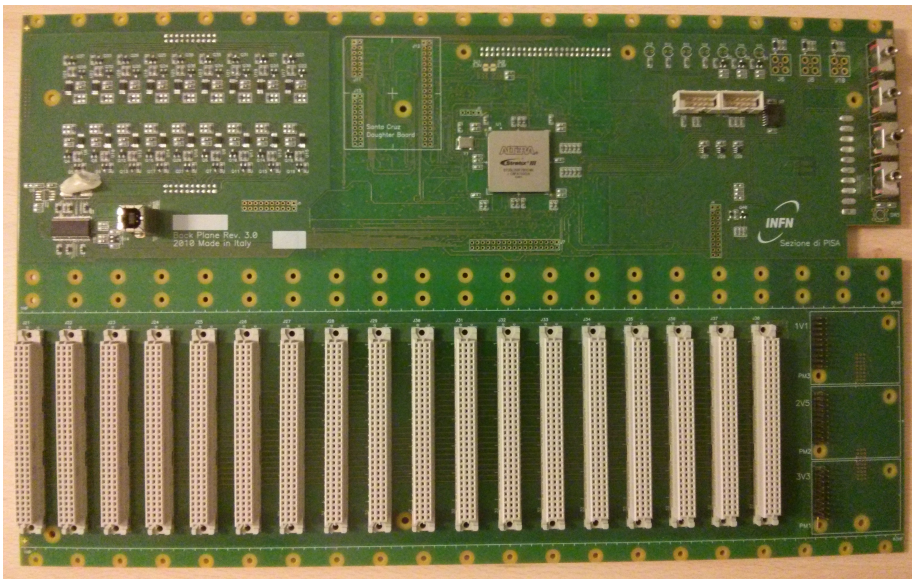

Figure 2.9: IRIS motherboard.

2.3 Features and possible improvement of the IRIS system

In an ideal system, the count rate of the system should increase linearly with increasing activity in the field of view. However, there are a number of components in the detection chain that will limit the count rate capabilities of the system. Mainly, the count rate capability depends on its overall dead time of the system.
Identify the component that principally contributes to the overall dead time is essential for an improvement of the count rate capability of the system.
The IRIS data acquisition system can be considered as composed by two sub-system. The first one is the mixed analogic digital front-end. This sub-system is composed by the detectors and the front-end electronics. The second

sub-system is the digital back-end. It is composed by DAQ, motherboard and Host PC. Each sub-system has different limitations.

2.3.1 Analogic digital front-end

Detectors

The temporal characteristics of the detectors that could limit the acquisition performance are:

- *the decay time of the scintillator*
- *the transit time of the PMT*

The decay time of the scintillator is 40 ns, while the transit time of the PMT is 6 ns. Both are paralysable dead time, but it is clear that the transit time of the PMT is negligible.

Front-end electronics

In order to perform a characterization of the front-end electronics an important parameter is the dead time. The front-end (section 2.2.2) has a paralysable dead time. A measurement of this dead time has been performed in [13] and the result are briefly present in figure 2.10. The dead time τ of the front-end electronics is (129 $\pm$ 13) ns.

The overall behaviour of the analogical sub-system is well represented by the paralysable model. Its overall dead time is given by the dead time of the front-end. As discussed in the previous chapter, for a paralysable system, the observed count rate is given by[21]:

$$m = ne^{-n\tau} \tag{2.2}$$

2.3.2 Digital back-end

DAQ boards

The dead time of the DAQ boards is due to the finite time needed to convert an analogic signal to a digital signal. Since the DAQ boards can

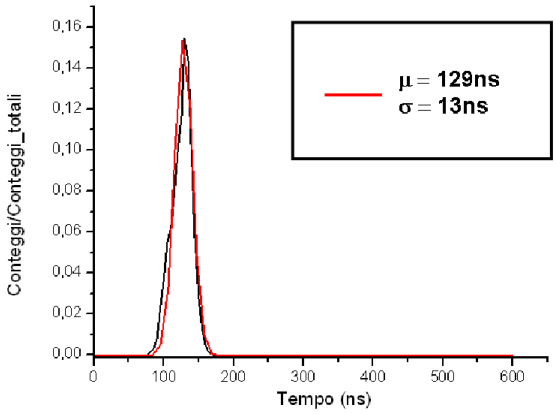

Figure 2.10: Dead time distribution measurement of the front-end electronics[13].

ignore a trigger when the ADCs are performing an acquisition, this dead time is a nonparalysable one.
The main part of the DAQ dead time is due to the ADCs performance. So an estimation of it is given by the internal conversion delay and the maximum output delay of the ADCs. These are about 30 ns + 20 ns. In this case, the form that the count per second takes is[21]:

$$m = \frac{n}{1 - n\tau} \tag{2.3}$$

Link DAQ-Motherboard

The link DAQ-Motherboard has an important limitation, it as a limited throughput. The throughput is the rate of successful data delivery over a communication channel. The units of throughput are the reciprocal of the unit for propagation delay, so it can be used to measure device performance. The maximum data throughput is measured in bits per second. A typical measurement method is to transfer data from one system to another and measure the time required to complete the transfer. The throughput is then calculated by dividing the file size by the time is second. The results is typically less than the maximum theoretical data throughput due to latency of the system.
As previously mentioned, the throughput between DAQ and motherboard is about 8 MB/s per bus.
Thus, it can transfer approximately $0.8 \cdot 10^6$ event per second. In this case,

the form that the count per second takes is:

$$m = \begin{cases} n & \text{if} \quad n < R_{max} \\ R_{max} & \text{if} \quad n > R_{max} \end{cases} \tag{2.4}$$

Link Motherboard-Host

The link Motherboard-Host has the same limitation of the link DAQ-Motherboard, it has a limited throughput. In this case, this throughput is about 21 MB/s[29].
Thus, the link between motherboard and Host PC can transfer approximately $1.1 \cdot 10^6$ event per second. Also for this link, the form that the count per second takes is given by the equation 2.4.

The overall throughput of the previous links is about $0.8 \cdot 10^6$ event per second.

2.3.3 Overall features

In order to quantify the overall limits of the system, acquisitions with different activity have been performed. The result of this acquisition is shown in figure 2.11. As discussed previously, different dead times involve different behaviour of the system. With a comparison between the figure 1.12 and the equations 2.2, 2.3 and 2.4, it is clear that the behaviour shown is given by paralysable dead time.
The sub-system that has a paralysable dead time is the analogical part of the IRIS scanner.

Possibles improvement

As a whole, limits of the IRIS data acquisition system can be summarised as follow (table 2.6).

All the above performances contribute to the NECR of the system. From the table 2.4, it is evident that the NECR is the Achilles heel of the IRIS

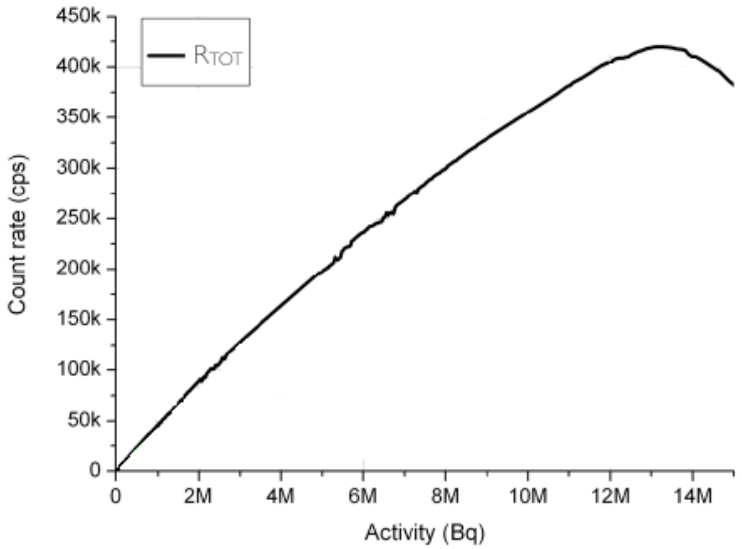

Figure 2.11: Coincidences measured with the IRIS system on varying of the activity.

Analogical part	
Number of detector	Maximum count rate (Mcps)
16	0.43

Digital part		
Link	Maximum count rate transfer (Mcps)	Maximum data transfer (MB/s)
DAQ-Motherboard	0.4[a]	16
Motherboard-Host PC	1.1	21

[a]In each bus.

Table 2.6: Limits of the IRIS data acquisition system.

scanner. Thus, improve the count performances is essential.
From the point of view of the hardware electronics, it is clear that the bottleneck is due to the the front-end.
For this reason, in order to improve the performance of the IRIS system the first step is to improve the front-end dead time. This work is already planned. At a later stage, could be essential improve the communication between DAQ

and motherboard and the link between motherboard and Host PC.
Therefore, this thesis work aims to propose a method to improve the DAQ-moterboard link and the motherboard-Host PC link.
This method will be thoroughly presented in the following chapters.

CHAPTER 3

Methods

In the previous chapter, an analysis of the limits of the acquisition systems currently used for IRIS has been done. Research efforts should focus primarily on enhancing the photon detection and the reconstruction methods. Hardware developments could help improving the dead time and increase the throughput of data acquisition system.
In this chapter, a few methods to implement hardware upgrade on the IRIS data acquisition system are presented. A first upgrade is performed at the firmware level. This upgrade aims to improve the DAQ-Motherboard data transferring. A second upgrade is performed at the hardware level. This upgrade aims to improve the motherboard-Host PC communication. In particular, the hardware upgrade allows significant improvements leading to a new generation of PET in which both FPGA and hard processor characteristics (advantages, properties, qualities, features) are maximized.

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3.1 Improving the DAQ-motherboard communication

This section starts with a discussion of the current communication protocol between the motherboard and a DAQ board. In the second part, the new communication protocol is proposed. The main difference between the two protocols is that the first one is asynchronous, while the new one is synchronous. In particular, the proposed protocol does not require any hardware changes, nevertheless it can considerably improve the bandwidth between the motherboard and DAQ boards.

3.1.1 Asynchronous bus

The current communication protocol between the motherboard and the DAQ boards uses a bus made of 16 data lines controlled by four signals per DAQ. The control signals are:

- *read request,*

- *read acknowledge,*
- *data ready,*
- *read reject.*

Signal directions are listed in table 3.1. All these signals are used by two finite state machines, one in the motherboard and the other in the DAQ board. Also, in the DAQ board, a single clock FIFO is implemented for temporary data storage.

Signal	read request	read acknowledge	data ready	read reject
Direction	MB ⇒ DAQ	DAQ ⇒ MB	DAQ ⇒ MB	DAQ ⇒ MB

Table 3.1: Signals direction in asynchronous communication protocol.

The communication protocol is controlled by one VHDL component, the DAQFETCH, and follows this sequence:

1. the data ready signal is asserted, i.e., there are data available in DAQ board
2. the motherboard requests data by asserting the read request signal
3. the DAQ board drives the data on the bus
4. the DAQ board informs the motherboard that data is on the bus by asserting the read acknowledge signal
5. the motherboard reads data and turns off the read request signal
6. the DAQ board stops driving the bus and turns off the read acknowledge signal.

In each step, an internal synchronization must be performed. Each of them request at least 30 ns. To transfer a single packet (five 16 bits words) 20 signals must be sent, thus at least 600 ns are lost for the synchronization. Assuming that the words can be transferred continuously is possible to estimate the bandwidth as:

$$\frac{10 \quad byte}{600 \quad ns} = 16 \quad MB/s \tag{3.1}$$

A simulation of this protocol is shown in figure 3.1. As it can be noted, the words are not transferred continuously. For this reason, the maximum transfer speed is about 8 MB/s[29].

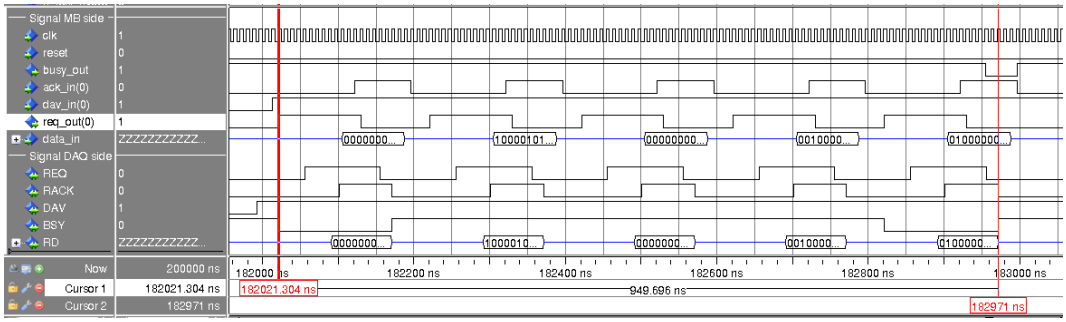

Figure 3.1: Simulation of the asynchronous communication protocol using ModelSim-Altera Edition 10.1d.

3.1.2 Synchronous bus

The new interface between the motherboard and the DAQ boards uses synchronous bus made of 16 lines. As in the asynchronous interface, four signals per DAQ are used to control the data transfer:

- *read request,*
- *read clock,*
- *data ready,*
- *output enable.*

The read clock is continuously sends by the motherboard to any DAQ boards.
Signals direction are listed in table 3.2. All these signals are controlled by two finite state machines, as in the asynchronous interface. A simplified scheme of the VHDL component developed to implement this type of communication is shown in figure 3.2. A difference between the asynchronous and the synchronous protocols is that the FIFO that is implemented in the DAQ board becomes a dual clock FIFO, i.e., the input and the output operate a two different clocks.

Signal	read request	read clock	data ready	output enable
Direction	MB ⇒ DAQ	MB ⇒ DAQ	DAQ ⇒ MB	MB ⇒ DAQ

Table 3.2: Signals direction in synchronous communication protocol.

The communication protocol follows this sequence:

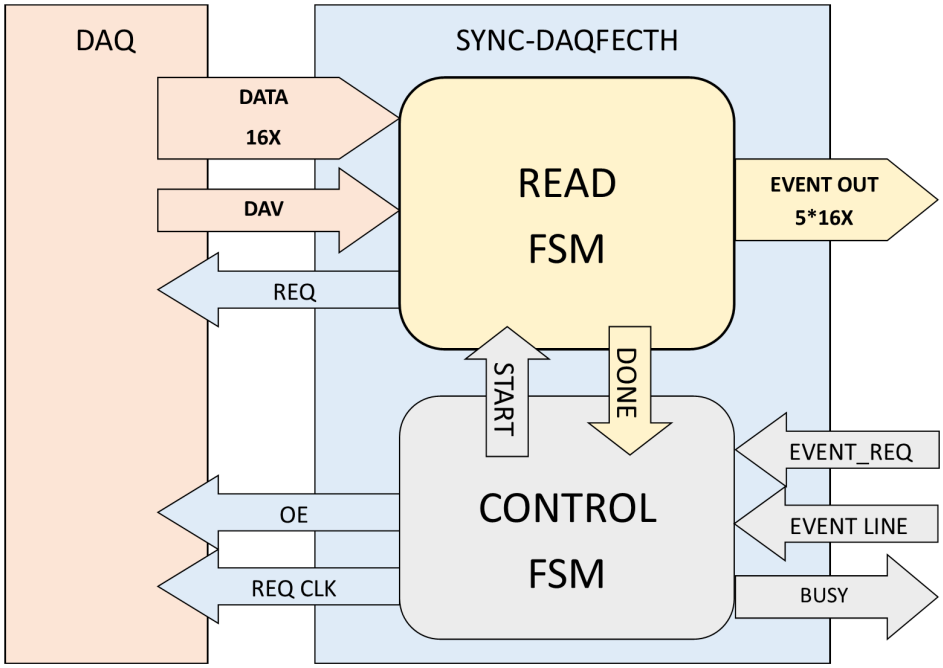

Figure 3.2: Simplified scheme of the component developed for implement a synchronous communication protocol.

1. the data ready signal is asserted, i.e., there are data available in a DAQ board
2. the motherboard asserts the output enable signal
3. the motherboard requests data by one pulse of read request signal, simultaneously the DAQ board drives the data on the bus and the motherboard reads it
4. the motherboard turns off the output enable signal

With this protocol the internal synchronization is not necessary, hence, no synchronization delay are needed. It is very important to underline that with this protocol it is possible to perform a data transmission in bursts. The third step can be repeated as many times as needed to transfer several words in short burst. The burst length reduce the control overhead and at its limit, the data transfer speed becomes $\sim clk_{freq} \cdot bits$. This is the characteristic that will increment considerably the data transfer velocity.

3.2 Improving the motherboard-Host PC communication

In this section a method to implement a SoC acquisition system for PET is illustrated. In particular, the features and the performances of the SoC are shown. The current SoC prototype is based on the SoCkit commercial board (Arrow Electronics Inc., Englewood, USA).

3.2.1 The prototype board

The Arrow SoCkit (figure 3.3) is a general purpose prototyping board with the following features:

- *A FPGA Cyclone V SoC with dual ARM Cortex® – A9 processor,*
- *MicroSD memory card,*
- *Gigabit Ethernet interfaces,*
- *Altera high-speed mezzanine connector (HSMC),*
- *Two low-power DDR3 memory banks.*

The FPGA is a Cyclone V SX SoC with a dual core ARM-based HPS. Its features are:

- *3.125 Gbps transceivers,*
- *150 GMACS,*
- *100 GFLOPS digital signal processing (DSP).*

The Hard Processor System (HPS) ia an ARM Cortex®-A9 with multiport memory controller shared with the FPGA. The combination of the FPGA and the HPS is very powerful because it allows to implement custom logic in the former and use the latter for high level control and for communication with the Host PC. High-throughput data paths between the HPS and the FPGA fabric provide over 125 Gbps peak bandwidth with integrated data coherency between the processors and the FPGA.

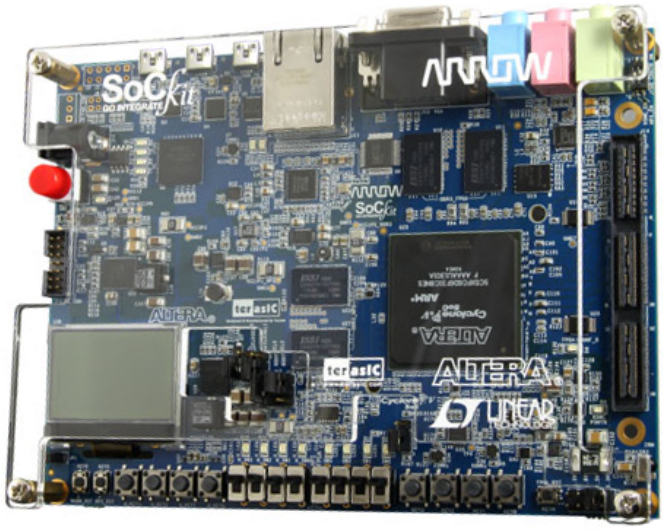

Figure 3.3: Prototyping board Arrow SoCkit.

3.2.2 Hard Processor System

The ARM Cortex-A9 MPCore processor operates at 800 MHz and supports symmetric and asymmetric multiprocessing.

The HPS has been setup with an embedded Linux based on the Yocto Source Package. The Yocto Source Package installer provided by Altera allows to compile a custom Linux bootloader, kernel and root filesystem. After building the bootloader, the kernel and the root filesystem, it is possible to make a SD-Card that automatic performs the follow operation a boot time:

- *start a Linux system*
- *load device driver,*
- *configure the FPGA,*
- *start user applications,*
- *configure the Ethernet interface.*

The HPS can boot from multiple sources, including the FPGA fabric and the flash memory. In contrast, the FPGA must be configured through either the HPS or an externally supported device.

In order to implement the device driver, the FPGA-HPS bridge must be configured. The Qsys project contains all the information to configure the HPC connection with the FPGA. The current Qsys configuration is based on the Golden Hardware Reference Design, which is a template project that is distribuited with the SoCkit. There are a number of basic Qsys components that are required by the HPS for standard operation: the on-chip memory, the system id peripheral and the Avalon Master Bridge. Two additional component FIFOs have been added to stream data between the HPS and the FPGA. The FIFOs are connected through the high bandwidth bridge. The slow control of the two FIFOs is made through the "lightweight", i.e., slow, bridge (see 3.2.3).

3.2.3 HPS-FPGA bridge

The HPS-FPGA interface contains the following components:

- *FPGA-to-HPS bridge,*
- *HPS-to-FPGA bridge,*
- *Lightweight HPS-to-FPGA bridge.*

This nomenclature underline the master in the communication between the FPGA and the HPS, i.e., it indicates the component that operates the flow control.
The first two bridge have a data width of 32, 64, and 128 bits. If the interface has 32-bit or 128-bit, the bridge performs data width conversion to the fixed 64-bit interface within the HPS.

The lightweight HPS-to-FPGA bridge provides a lower-performance interface to the FPGA fabric. This interface is useful for accessing the control and status registers of soft peripherals. The bridge master exposed to the FPGA fabric has a fixed data width of 32 bits. The slave interface of the bridge in the HPS logic has a fixed data width of 32 bits.

3.2.4 HSMC interface

The Altera High Speed Mezzanine Card (HSMC) specification defines the electrical and mechanical properties of a high speed mezzanine card

adapter interface for FPGA-based motherboards. This specification allows for the design of interoperable motherboards and add-on cards by different manufacturers that can interoperate and utilize the high-performance I/O features found in new generation FPGA devices. The connector is based on the Samtec 0.5 *mm* pitch, surface-mount QTH/QSH family of connectors. Compatible versions with this specification vary from 132 to 192 physical pins. It is both low-cost and high performance. The HSMC interface supports two basic types of signaling standards: LVTTL and LVDS.

3.3 Test

3.3.1 Synchronous bus

The first test for the synchronous communication protocol was be performed by simulation. The developed components consist of a modified version of the DAQFETCH VHDL component and the DAQ top component. These two have been integrated in the DAQ and the motherboard firmwares, respectively. With this strategy, it is possible to switch from the asynchronous protocol to the synchronous protocol (and vice versa) by changing a VHDL parameter.
The main characteristic of the new protocol is the possibility to perform data transmission in bursts. The new firmware version transfers five 16-bit words per sequence. The number of words transferred per sequence is fixed and limited to the words present in one packet. Data integrity control is performed by additional component in the motherboard firmware.
The *read clock* used in the simulation test vary between 10 MHz to 50 MHz. In figure 3.4, a test with the *read clock* running at 50 MHz is shown.

A comparison between the asynchronous and the synchronous communication protocol performance is present in table 3.3.

The time required to transfer a single packet is roughly 250 ns. Therefore, the maximum transfer speed is close 40 MB/s.

The synchronous protocol has been validated on the IRIS scanner, as detailed in the following.

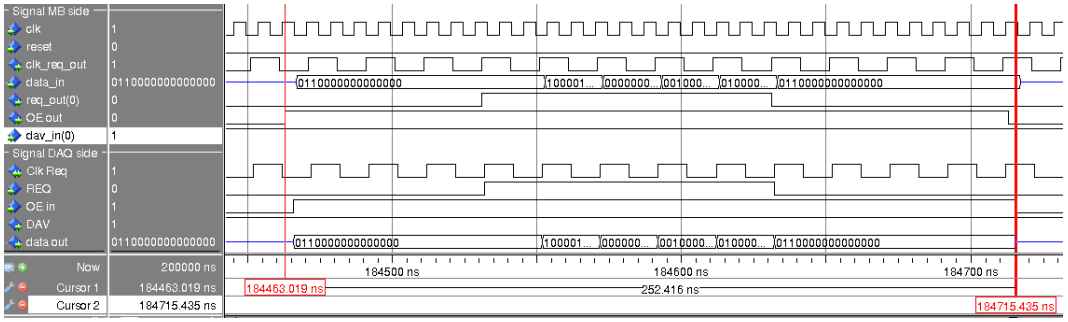

Figure 3.4: Simulation of the synchronous communication protocol using ModelSim-Altera Edition 10.1d.

Protocol	Clock MHz	Transfer delay ns	Transfer speed MB/s
Asynchronous	-	949	10.5
Synchronous	10	1040	9.8
Synchronous	30	310	32.2
Synchronous	50	252	39.7

Table 3.3: Comparison between the asynchronous and the synchronous communication protocol performance in simulation. The read clock used vary between 10 MHz to 50 MHz. The transfer delay is referred to one packet (five 16-bit words).

3.3.2 Data packet transfer time

This test has the purpose to measure the time taken to transfer a data packet. We refer to this time as *packet delay time*. The measurement has been done with a Tektronix logic analyser (figure 3.5). It is based on Microsoft Windows PC platform,it has up to 16 single ended probes and it performs up to 200 MHz state acquisition.

The packet delay time is related to the throughput of the system. Starting from the packet delay time (δt_{packet}) the throughput (T) can be calculated as:

$$T \sim \frac{packet_{size}}{\Delta t_{packet} + \Delta t^{I}_{packet}} \tag{3.2}$$

where ($packet_{size}$) is 10 byte and Δt^{I}_{packet} is the time between two packets. Figure 3.6 shows the measured packet delay time for the asynchronous protocol.

Figure 3.5: Logic Analyser (Tektronix).

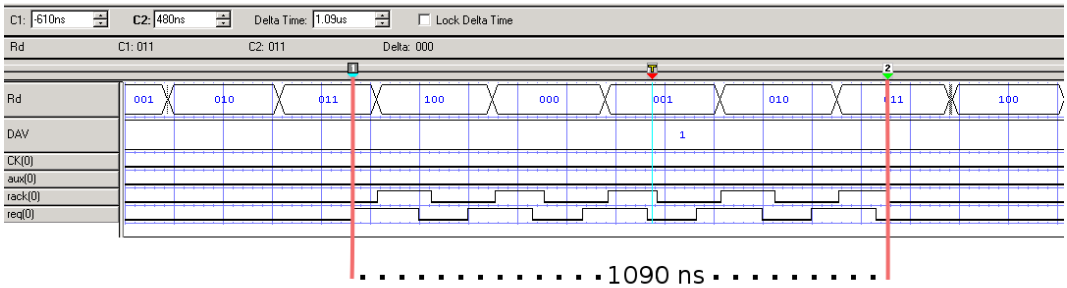

Figure 3.6: Measurement of the packet delay time with the asynchronous protocol. The RD signal is composed by the bits 15, 14 and 13 of the packet words.

Every single word has a transmission overhead. For a packet complete transmission the sequence presented in 3.1.1 is performed five times.

The same test was performed for the synchronous protocol. Clocks vary from 10 MHz to 30 MHz. Figures 3.7 and 3.8 show the packet delay time obtained for such frequencies.
In this case, there is a communication overhead is present only once every five words. This is because packets are transmitted in short bursts of five words. For the complete transmission of one packet the sequence presented in section 3.1.2 is performed only once, with the third step repeated five times.

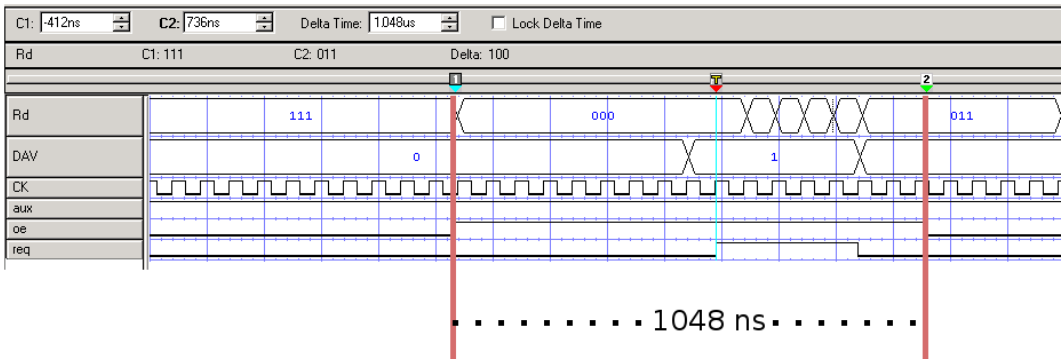

Figure 3.7: Measurement of the packet delay time with the synchronous protocol. The read clock is 10 MHz. The RD signal is composed by the bits 15, 14 and 13 of the packet words.

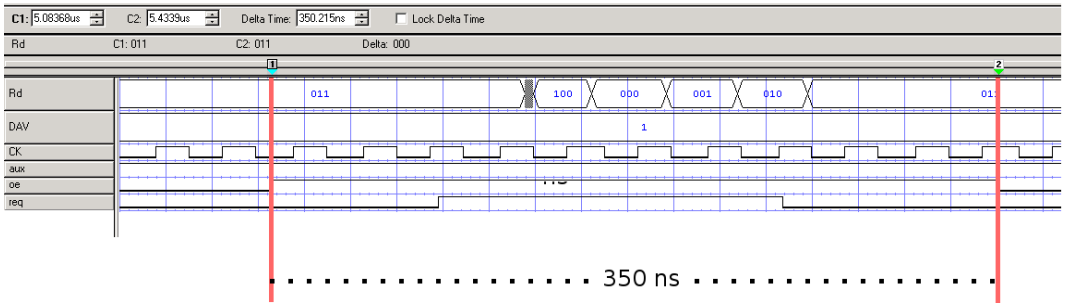

Figure 3.8: Measurement of the packet delay time with the synchronous protocol. The read clock is 30 MHz. The RD signal is composed by the bits 15, 14 and 13 of the packet words.

3.3.3 System throughput in a complete acquisition

This third test has been conducted with the purpose of measuring the system throughput in a complete acquisition. As explained in the section 2.3, the maximum data throughput is measured in bits per second and a typical measurement method is to transfer data from one system to another and to measure the time required to complete the transfer. For this purpose, the IRIS data acquisition software has been used. The size of the acquisition output files are divided by the acquisition times.

The maximum used read clock is 13 MHz. With this clock the limits of the implemented USB 2.0 controller are reached (21 MB/s [29]). Using a

higher clock rate the communication fails after a few second. This happens because of a malfunction of the USB subsystem when the bus is higher than 21 MB/s [29]. We left the debug of this malfunctions for further investigation.

3.3.4 Data integrity

This fourth test has been conducted with the purpose to verify the data integrity. As in the previous test, the Tektronix logic analyser has been used. In figure 3.9 the transmission with the new protocol of one data packet is showed.

The transition between two words has a short period of time in which is not stable. In order to understand what happens during the transition

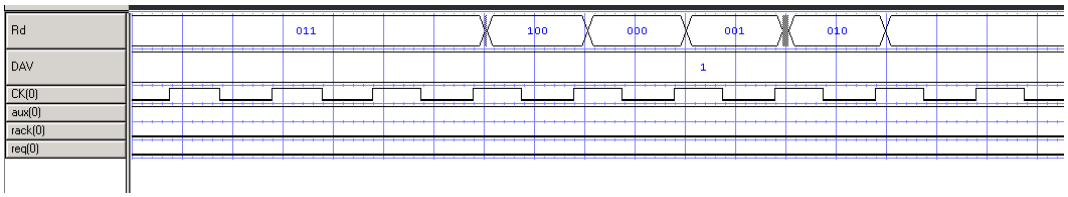

Figure 3.9: Some instabilities in the transmission of one data packet with a read clock of 30 MHz. The RD signal is composed by the bits 15, 14 and 13 of the packet words.

between two words, it could be useful to zoom in the transition (figure 3.10). In this case, the word in the bus changes from *001* to *010*. In the transition from *001* to *010* two bits are changing. In this change, for a little interval of time, the word *011* appear. This kind of problems are due to:

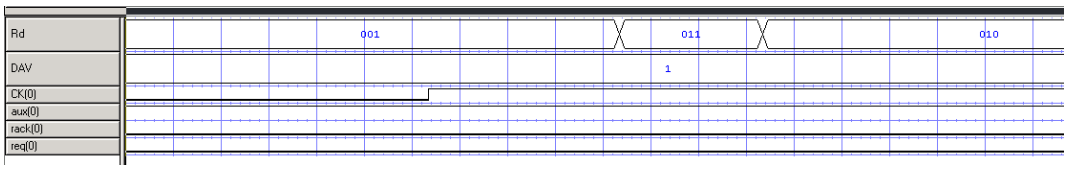

Figure 3.10: Zoom of one instability in the transmission of one data packet with a read clock of 30 MHz showed in figure 3.9. The RD signal is composed by the bits 15, 14 and 13 of the packet words.

- *the characteristics of the flip-flop,*
- *the race condition,*
- *the skew of the bus.*

Three parameters characterise a flip-flop:

- *Setup time:the time interval in which the signal must be stable before the clock edge.*
- *Hold time: the time interval in which the signal must be stable after the clock edge.*
- *Clock-to-output delay: the propagation delay required for the input to show up at the output after the sampling edge of the clock signal.*

If any setup or hold time violation occurs the output may change to an unwanted state, this make the correspondent data to be corrupted[1].
The clock-to-output delay is related with the race condition. A critical race occurs when the order in which internal variables are changed alter the output.
The skew of the bus is the variation of the propagation delay between different lines.
For these last two, for a brief period, the output may change to an unwanted state before settling back to the designed state.
In the case analysed, the race condition is guaranteed by the constraint given to the FPGA project. Also the skew of the bus[2] can be compensate with the constraint given to the FPGA project. Only for the setup or hold time violation require a more detailed study.

[1]Data corruption refers to errors in computer data that occur during writing, reading, storage, transmission, or processing, which introduce unintended changes to the original data.

[2]Measured by the motherboard and DAQ boards constructor.

Mean Time Between Failures (MTBF)

Because of the stochastic nature of the occurrence of a timing violation and resolution time, analysis of the metastable condition is characterized by a statistical average. We use the average time interval between two synchronization failures to express the reliability of the design. It is known as *mean time between synchronization failures* (MTBF) and is the main quantity used in metastability timing analysis. MTBF depends on many factors. It is possible derive the MTBF by calculating the average rate of synchronization failures, AF, which is the reciprocal of MTBF. AF is defined as the average number of synchronization failures occurring in a 1-second interval. It is determined by two factors:

- *the average rate at which an FF enters the metastable state* R_{meta},
- *the probability that an FF cannot resolve the metastable condition within* T_r.

R_{meta} is determined by the formula:

$$R_{meta} = w \cdot f_{clk} \cdot f_d \tag{3.3}$$

In this formula, w is the susceptible time window, which is a constant determined by the electrical characteristics of the FF. It can be interpreted as a metastability susceptible time interval associated with the triggering edge of the clock signal. For current device technology, the typical value of w is from few picoseconds to a fraction of a nanosecond. The f_{clk} parameter is the frequency of the clock signal. The f_d parameter is the rate of change in input data, which is defined as the number of input changes per second.

The resolution time $P(T_r)$ is the probability that the metastability condition persists beyond T_r, after the clock edge. It can be interpreted as the probability that the metastability cannot be resolved within T_r seconds.
It is characterized by a probability distribution function:

$$P(T_r) = e^{\frac{-T_r}{\tau}} \tag{3.4}$$

where τ is the decay time constant and is determined by the electrical characteristics of the FF. A typical value of today's device technology is around a fraction of a nanosecond.

Thus, the average number of synchronization failures per second is:

$$AF = R_{meta} \cdot P(T_r) \tag{3.5}$$

For a given T_r, the MTBF becomes:

$$MTBF(T_r) = \frac{1}{AF} = \frac{e^{\frac{T_r}{\tau}}}{w \cdot f_{clk} \cdot f_d} \tag{3.6}$$

Using the susceptible time window and the resolution time given by the FPGA manufacturer, the MTBF of our architectures can be estimate.
The susceptible time windows of our FPGA is 100 *ps* and the decay time constant of the resolution time has the same value. Thus, in both the architectures used, due to the number of FF used and the low clock rate implemented, the MTBF is several centuries.

3.3.5 HPS-FPGA bridge

A loop-back test-bench has been implemented to test the HPS-FPGA bridges. In this test-bench data has been send forth and back between the HPS and the FPGA through two FIFOs components. A simplified diagram of the test-bench is shown in figure 3.11.

In order to use the FIFOs from the HPS, a custom driver must be developed using a set of libraries provided by Altera: the Hardware Library API and the System on Chip Abstraction Layer (Socal). In these libraries there are all the functions for write or read a word in a specific memory address. A Python script has been written to test the driver. The script operates an integrity check of the data in the loop-back.

Two tests were performed. In the first one a data width of 32 bits was used, in the second one a data width of 64 bits was used.

The purpose of the test was to measure the data transfer speed between the HPS and the FPGA.

3.3.6 Ethernet

An Ethernet test has been conducted to measure the data transfer speed between the HPS and the Host PC. In this test, the SoCkit was connected to

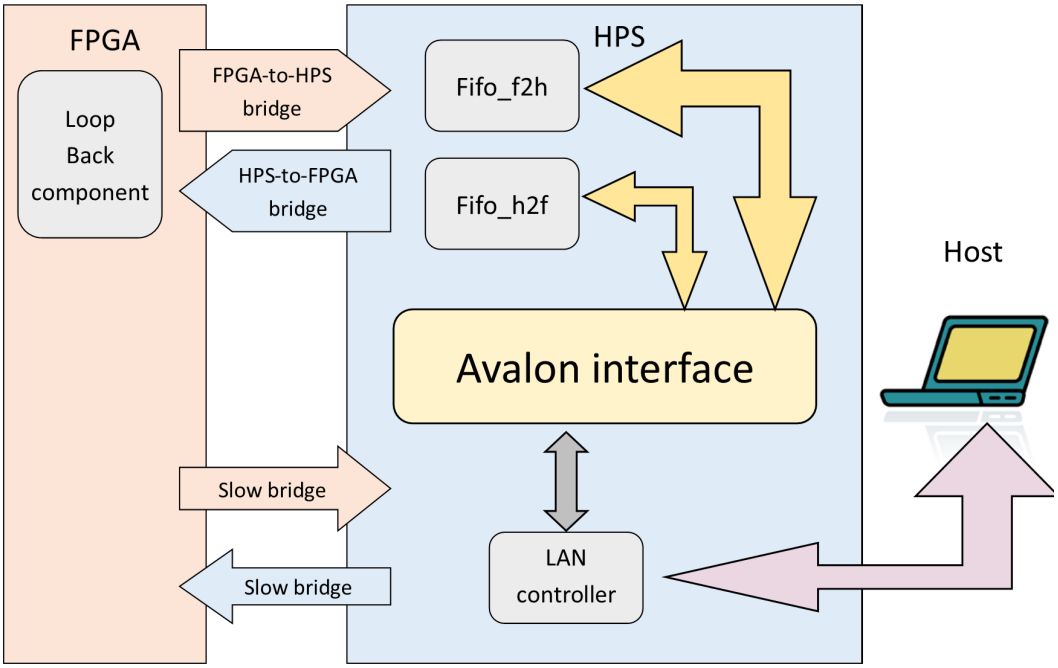

Figure 3.11: Simplified diagram of the test-bench used for the bridge test.

a PC with the Gigabit Ethernet interface. To measure the transfer speed two protocol were used: HTTP and FTP.
The HTTP is the HyperText Transfer Protocol and is mainly used for the transmission of internet pages. The FTP is the File Transfer Protocol and is mainly used for the transmission of files.
Fou our purpose, the main difference between this two protocol are:

- *Transfers with HTTP include a set of headers. FTP does not send such headers. When sending small files, the headers can be a significant part of the amount of actual data transferred. HTTP headers contain info about things such as last modified date, character encoding, server name and version and more,*

- *HTTP provides meta-data with files, Content-Type, which clients use but FTP has no such thing. The meta data can thus be used by clients to interpret the contents accordingly.*

3.3.7 HSMC (LVDS standards)

A separated set of VHDL components has been developed to implement the communication interface between the FPGA and a ADC Board through the HSMC port. The implementation is based on the Altera megafunction for low-voltage differential signaling (LVDS). This megafunction has two different variations: LVDS_TX for the transmitter and LVDS_RX for the receiver. With the latter, it is also possible to implement a serializer and a deserializer.

A test-bench was developed to work with the LVDS_RX component. In this test-bench the finite state machine reads commands from the HPS and when needed reads data thought the HSMC connector from the ADC board. The test-bench includes:

- *Memory banks,*
- *FIFO data transfer finite state machine,*
- *Synchronization registers.*

These components accomplish the following tasks: memory banks keep the configuration commands and the status; the finite state machine controls the two FIFOs; the synchronization registers allow deserialized signals to cross clock boundaries without incurring in metastability problems. The finite state machine can be instructed to "read N words" from LVDS_RX, "write the status" or "reset".
The main states in finite state machine are:

- *State 1: Inizialization,*
- *State 2: Ready,*
- *State 3: Read command,*
- *State 4: Write status,*
- *State 5: Read from HSMC,*
- *State 6: Done.*

An simplified state diagram for the finite state machine is represented in figure 3.12. In order to reduce the simulation complexity, the HPS has been replaced with a component that implements only the basic interfacing signals.

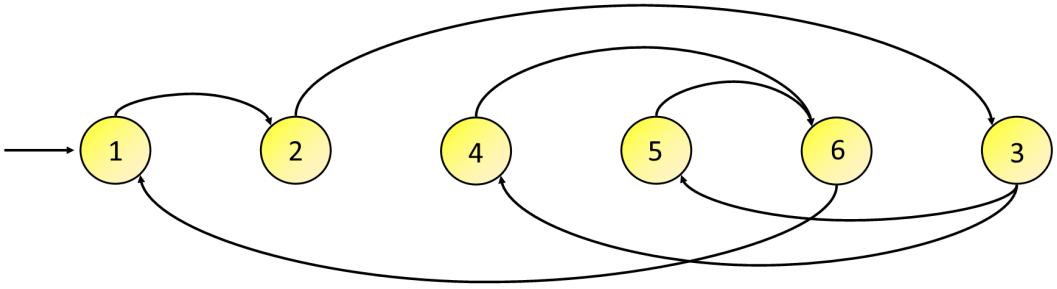

Figure 3.12: An simplified state diagram for the finite state machine. State 1: Inizialization; State 2: Ready; State 3: Read command; State 4: Write status; State 5: Read from HSMC; State 6: Done.

In this component there are only two FIFOs and a finite state machine that continuously writes command registers in the output FIFO. The components behind the HSMC interface were replaced with a simplified component. The logic at the other side of the HSMC has been emulated with a FIFO, a counter that fills the FIFO, and a LVDS_TX to serialize and send the FIFO output. The LVDS clock runs at 600 MHz and the data bus had 2 lines. A serializer factor of 8 was implemented by which 16 bits word was sent in our bus. The finite state machine was configured to transfer short burst of five words.

CHAPTER 4

Results and discussion

This chapter collects and discusses the main results obtained during this thesis work. Two of them are stand out from the others. The first oneconsists in the improvement of the IRIS data acquisition system with an upgrade at the firmware level. The second one consists in the validation of a new possible acquisition system based on a System-on-Chip.

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4.1 DAQ-motherboard communication

4.1.1 Data packet transfer time

The first useful parameter measured is the packet delay time. A comparison between the packet delay time obtained in the simulation and the packet delay time measured is presented in table 4.1. In any case the packet delay time measured is longer than the packet delay time simulated.

Protocol	Read Clock (MHz)	Packet delay time simulated (ns)	Packet delay time real (ns)
Asynchronous	-	949	1090
Synchronous	10	1040	1148
Synchronous	13	854	931
Synchronous	30	310	350

Table 4.1: Delay time for the transmission of one data packet.

The real packet delay time in the synchronous protocol with a 10 MHz clock is comparable with the real packet delay time in the asynchronous protocol. On the other hand, with a little increment in the clock the packet delay time difference becomes considerable. With the result shown up the reachable performance improvement could be substantial.

The second quantity measured is the time between two packets. The measurement obtained are listed in table 4.2. In this case, with any clock the

difference between the two protocols is significant, at least a difference of the 30% is present.

Protocol	Read Clock (MHz)	Time between two packets (ns)
Asynchronous	-	120
Synchronous	10	83
Synchronous	13	65
Synchronous	30	31

Table 4.2: Delay time for the transmission of one data packet.

This measurement confirms the potential improvement achievable with the synchronous protocol. In fact, using these results in the equation 3.2, the maximum system throughputs expected is 52.4 MB/s (table 4.3). The

Protocol	Read Clock (MHz)	Packet delay time (ns)	Time between packet (ns)	Throughput extrapolated (MB/s)
Asynchronous	-	1090	120	16.5
Synchronous	10	1048	83	17.7
Synchronous	13	901	65	20.7
Synchronous	30	350	31	52.4

Table 4.3: Comparison between the system throughput extrapolated from the one packet delay time and the system throughput measured in one complete acquisition.

system throughputs reported in the table 4.3 are referred at our system that has two bus.
In any case the synchronous protocol is expected to be faster than the asynchronous protocol.

4.1.2 System throughput for a complete acquisition

In order to quantify the real improvement of the IRIS data acquisition system, the system throughput was measured. A comparison between the

throughput calculated using the total delay time[1] obtained in the previous test and the throughput measured for the two protocol is presented in table 4.4.

Protocol	Read Clock (MHz)	Throughput extrapolated (MB/s)	Throughput measured (MB/s)
Asynchronous	-	16.5	16.36
Synchronous	10	17.7	17.38
Synchronous	13	20.7	20.71
Synchronous	30	52.4	-

Table 4.4: Comparison between the system throughput extrapolated from the one packet delay time and the system throughput measured in one complete acquisition.

The extrapolated throughput is higher than the measured one for any clock speed. However the difference is less than the 2%. These differences are due to the approximation made in the equation 3.2.

Forasmuch as the information of one coincidence is stored in 20 bytes (sec. 2.2.3), the measured throughputs converted in Mcps are presented in table 4.5.

Protocol	Read Clock (MHz)	Throughput (MB/s)	Throughput[a] (Mcps)
Asynchronous	-	16.36	0.409
Synchronous	10	17.38	0.435
Synchronous	13	20.71	0.502
Synchronous	30	-	-

[a]In each bus.

Table 4.5: System throughput in one complete acquisition.

The maximum throughput reached is 0.502 $Mcps$ per bus that is about the 30% higher than the maximum throughput reached with the previous

[1]The total delay time is given by the sum of the packet delay time and the time between two packet.

architecture.

4.2 Motherboard-Host PC communication

4.2.1 HPS-FPGA bridge

The results of the first transfer speed test between the HPS and the FPGA are shown in figure 4.1.

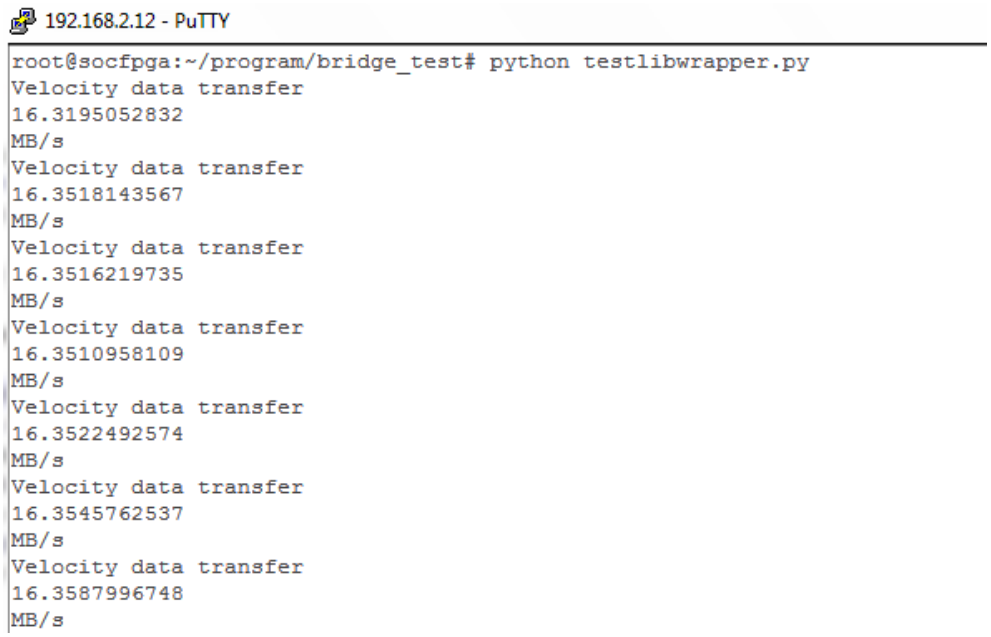

Figure 4.1: Result of the bridge speed test using a data width of 32 bits.

The speed value was approximately 16 MB/s in writing and the same speed in reading. A higher maximum speed value was expected.
In the connection between the HPS and the FPGA was used a data width of 32 bits for the input and 32 bits for the output. A second test with double data width was performed. The results obtained with this second test are shown in figure 4.2. In this case the maximum speed value was approximately 36 MB/s.
Even this, this speed is lower than the maximum bandwidth. A possible way to improve this result is to use a bus width of 128 bits. Another way it is to

Figure 4.2: Result of the bridge speed test using a data width of 64 bits.

use both the ARM core. Eventually, an optimization of the custom driver can be performed.

4.2.2 Ethernet

The results of the Ethernet tests are shown in figures 4.3 and 4.4 and summaries in table 4.6.

Protocol	Mean speed MB/s	Peak speedMB/s
http	10	12
ftp	50	78

Table 4.6: Result of Ethernet speed test.

The http protocol allows data transfer running as speed varying between 8 MB/s and 12 MB/s (figure 4.3) while with the ftp protocol we have speed result values varying between 40 MB/s and 60 MB/s with a peak of 78 MB/s (figure 4.4).
The FTP protocol showed to be faster than the HTTP protocol.

```
root@socfpga:~/program/hps_fifo_test_1_write# wget http://192.168.2.13/cyclone_w
eb-13.1.0.162.qdz -O /dev/null
--2014-01-11 05:15:41--  http://192.168.2.13/cyclone_web-13.1.0.162.qdz
Connecting to 192.168.2.13:80... ^C
root@socfpga:~/program/hps_fifo_test_1_write# wget http://192.168.2.13:8000/cycl
one_web-13.1.0.162.qdz -O /dev/null
--2014-01-11 05:16:04--  http://192.168.2.13:8000/cyclone_web-13.1.0.162.qdz
Connecting to 192.168.2.13:8000... connected.
HTTP request sent, awaiting response... 200 OK
Length: 575075159 (548M) [application/octet-stream]
Saving to: '/dev/null'

45% [================>                    ] 260,644,864 11.4MB/s  eta 30s
```

Figure 4.3: Data transfer speed test between the HPS and the Host PC with http protocol.

```
root@socfpga:~/program/hps_fifo_test_1_write# wget ftp://192.168.2.13:21/cyclone
_web-13.1.0.162.qdz -O /dev/null
--2014-01-11 06:01:00--  ftp://192.168.2.13/cyclone_web-13.1.0.162.qdz
           => '/dev/null'
Connecting to 192.168.2.13:21... connected.
Logging in as anonymous ... Logged in!
==> SYST ... done.    ==> PWD ... done.
==> TYPE I ... done.  ==> CWD not needed.
==> SIZE cyclone_web-13.1.0.162.qdz ... 575075159
==> PASV ... done.    ==> RETR cyclone_web-13.1.0.162.qdz ... done.
Length: 575075159 (548M) (unauthoritative)

86% [==================================>      ] 498,016,256 51.8MB/s  eta 1s
```

Figure 4.4: Data transfer speed test between the HPS and the Host PC with ftp protocol.

Since, the nominal maximum speed for the Ethernet protocol is 125 MB/s, both protocol showed to have a lower maximum speed.

4.2.3 HSMC

The results of the Ethernet test bench are shown in figures 4.5.

The speed of data transfer was approximately 75 MB/s (260 ns are needed for transfer 160 bit). A considerable increment of this speed can be easily attained using a higher bus width. Also it is excessive perform the alignment control in each transition. It takes approximately 50 ns. Moreover, it is important to underline that the clock used for data transfer was 600 MHz, this value is very high. Produce a custom link between two different hardware that support clock higher than 100 MHz could be very difficult and expensive. Thus the right strategy to improve the speed of data transfer is to reduce

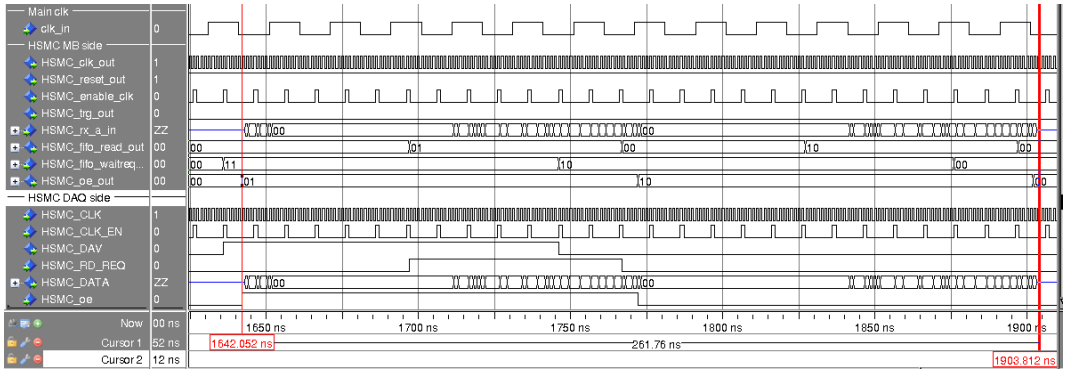

Figure 4.5: Test performed of verify the functioning of the Altera megafunction LVDS_TX/RX and, accordingly, the integrity and data transmission speed.

serializer factor and reduce the clock.

In conclusion, with this test it has been possible to understand and verify the functioning of the Altera megafunction LVDS_TX/RX and, accordingly, the integrity and data transmission speed.

Combining all the improving obtained in each sub-system, a potential 200% performance improvement is reachable with the change of the FPGA family, i.e., the maximum count rate reachable will be 3.5 Mcps.

Conclusion

The objective of this was to improve the IRIS data acquisition system by upgrading its firmware and proposing architectural alternatives that make use of the most recent available technologies. The work that has been carried out includes the following major results:

1. a new data communication protocol between the DAQ boards and motherboard has been developed and tested, the new protocol increases the acquisition bandwidth by 30% at the bus level,
2. a new acquisition architecture based on the last generation low-cost SoC/FPGA (Altera Cyclone V) has been proposed,
3. an operating system and a set of applications for the proposed SoC has been built and tested,
4. a preliminary FPGA-to-HPS communication firmware has been developed in order to demonstrate the feasibility of a SoC acquisition system,
5. the performances achievable with the new SoC based acquisition system have been characterized.

The first result alone allows to immediately improve IRIS performances in terms of NECR with no further hardware development costs. This is due to the 30% increase in the maximum coincidence rate that the system can acquire

with the new protocol, and it is true only if the front-end does not become the bottleneck at higher coincidence rates. The remaining results, all related to the new SoC architecture, demonstrate the convenience and the feasibility of a new acquisition system with higher performances and very low development effort. In this work the maximum theoretical bandwidth achievable with the SoC under test has not been reached, and a fine tuned implementation is left as future work. However, the new architecture enables managing the data transfer at the application level, i.e., with http and ftp, and still obtaining counting performance improvements greater than 200% with respect to the old architecture. This paves the way for designing PET acquisition systems adaptable to more complex geometries and stronger requirements than for the IRIS PET.

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