Low-Overhead Built-In Self-Test for Advanced RF Transceiver Architectures

by

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ABSTRACT

Due to high level of integration in RF System on Chip (SOC), the test access points are limited to the baseband and RF inputs/outputs of the system. This limited access poses a big challenge particularly for advanced RF architectures where calibration of internal parameters is necessary and ensure proper operation. Therefore low-overhead built-in Self-Test (BIST) solution for advanced RF transceiver is proposed. In this dissertation. Firstly, comprehensive BIST solution for RF polar transceivers using on-chip resources is presented. In the receiver, phase and gain mismatches degrade sensitivity and error vector magnitude (EVM). In the transmitter, delay skew between the envelope and phase signals and the finite envelope bandwidth can create intermodulation distortion (IMD) that leads to violation of spectral mask requirements. Characterization and calibration of these parameters with analytical model would reduce the test time and cost considerably. Hence, a technique to measure and calibrate impairments of the polar transceiver in the loop-back mode is proposed.

Secondly, robust amplitude measurement technique for RF BIST application and BIST circuits for loop-back connection are discussed. Test techniques using analytical model are explained and BIST circuits are introduced.

Next, a self-compensating built-in self-test solution for RF Phased Array Mismatch is proposed. In the proposed method, a sinusoidal test signal with *unknown* amplitude is applied to the inputs of two adjacent phased array elements and measure the baseband output signal after down-conversion. Mathematical modeling of the circuit impairments and phased array behavior indicates that by using two distinct input amplitudes, both of which can remain *unknown*, it is possible to measure the important parameters of the

phased array, such as gain and phase mismatch. In addition, proposed BIST system is designed and fabricated using IBM 180nm process and a prototype four-element phased-array PCB is also designed and fabricated for verifying the proposed method.

Finally, process independent gain measurement via BIST/DUT co-design is explained. Design methodology how to reduce performance impact significantly is discussed.

Simulation and hardware measurements results for the proposed techniques show that the proposed technique can characterize the targeted impairments accurately.

To My Parents and Family

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CHAPTER 1

INTRODUCTION

1.1 Outline of Dissertation

Continuous demand for RF system-on-chip (SoC) devices has fueled the integration of various RF components, such as power amplifier (PA), low-noise amplifier (LNA), and mixer, together with the baseband, analog, and digital subsystems into a single chip. However, this level of integration, while essential to meet increasing performance/power requirements, brings about challenges in terms of test and calibration of RF devices. Production test process for RF SoCs requires high caliber digital testers equipped with RF enabled instrumentation, increasing the total cost.

Several techniques in the literature aim to reduce the dependence on external RF instrumentation for low cost testing [1-17]. In [1-3], simple test signals such as multi-tone sinusoidal signals, are used to generate output data, where the performance of RF transceiver is predicted using the output data as well as machine learning methods. Another well-known test technique is loop-back based testing. In [4-9], the loop-back configuration is used to characterize both the transmitter and the receiver. In [4, 5], the authors derive the analytical model for the entire loop-back path and use numerical techniques in order to solve transmitter and receiver parameters simultaneously. In [6], authors use similar mathematical models with specialized signals in order to achieve an analytical solution. In [7], transceiver parameters are predicted using statistical learning, and in [8] embedded sensors are used together with statistical learning to improve prediction accuracy. In [9], most transceiver parameters are decoupled to characterize the entire system. While system-level testing and loop-back reduces the go/no-go testing burden significantly, some

parameters, such as linear gain, cannot be decoupled in the loop-back mode no matter what input signal is used due to linear dependencies. This hampers system-level calibration techniques [18] that rely on absolute complex coefficients of the system rather than ratio-metric performance parameters, such as third or fifth order input intercept. Moreover, for RF circuit-level calibration, more fine-grained characterization may be necessary [19, 20]. Hence, robust RF BIST (Built-in Self-Test) methods are needed to measure parameters of individual blocks that can be independently calibrated. It has been shown through extensive hardware experiments that when RF blocks can be characterized in terms of performance, one-shot methods can be used to accurately calibrate devices without the need for iterations at the system level [21].

In this dissertation, RF BIST methods for advanced RF transceiver such as RF polar transceiver and RF phased array are proposed. In addition, robust amplitude and gain measurement for RF BIST application are proposed and discussed.

In chapter 2, a comprehensive BIST solution for RF polar transceiver is proposed. Among the RF transceivers, the polar transceiver architecture is a promising solution for future wireless communication systems in terms of power efficiency. In the polar transmitter, the In-phase/Quadrature (I/Q) signal is converted to polar form and divided into an amplitude component and a phase component. The amplitude component is used as an envelope to modulate the supply voltage of the PA while the phase component modulates the high frequency carrier directly, which leads to a constant amplitude signal at the input of the PA. Since the PA's supply voltage is modulated based on the amplitude of the PA output, it saves power, thus achieving significantly high efficiency [22]. The receiver in the

polar transceiver is typically a traditional IQ receiver which consists of identical in-phase and quadrature paths.

Although polar transceivers provide high efficiency, their performance suffers from unavoidable inherent impairments, namely, gain and phase mismatches in the receiver, differential delay skew between the envelope and phase signals, and limited envelope bandwidth in the transmitter. Additionally, nonlinear behavior of the PA between supply voltage and PA output is still a problem. Hence, accurate measurement and calibration of the above impairments are essential to ensure operational compliance. At the high level, testing of the polar transceiver is same as testing of Cartesian transceiver. A modulated signal is applied to the input of the transmitter and spectral density at several offset frequencies, EVM, and output power are characterized using vector signal analyzers [23]-[24]. For the receiver, an RF modulated signal is applied to the input of the RF receiver and then sensitivity and selectivity can be determined by measuring Signal-to-Noise-Ratio (SNR) or Bit Error Rate (BER). However, such performance-based characterization does not lend to easy calibration since the required parameters are not directly measured. Instead, the system performances are optimized by trial and error, using a search process. For example, regarding the delay skew in the transmitter, the baseband signal is delayed step-by-step fashion until best performance is found [25]. Unfortunately, such an iterative search process for calibration significantly increases test cost since it can take several seconds [25]. This is particularly true for delay skew since the range of possible skew values can be large and this parameter needs to be tuned with acceptable accuracy. As an example, for the GSM-EDGE specification, the tolerable delay skew is 50 ns [23] while the search range

for delay skew is [0-500 ns], requiring at least 7 binary steps to find the optimum skew calibration point [23].

In order to calculate specific internal parameters of polar transceivers, the entire system is modeled and analytical formulations along with a parameter suppression/enhancement algorithm is used [26], [27]. In addition, target parameters in the receiver as well as the transmitter are determined using the loop-back configuration. Since the loop-back signals differ from the RF signal, specialized test signals are determined to de-embed each parameter of interest. This de-embedding is based on analytical derivations that can be computed within several milliseconds using the baseband digital signal processor (DSP). Removal of external RF equipment enables significant test cost reduction. Experimental results confirm that the gain and phase mismatches in the receiver, delay skew and the AM bandwidth in the transmitter can be determined with low-cost implementation.

In Chapter 3, a technique for robust amplitude measurement is proposed. RF amplitude measurement has been the focus of significant prior work. Generally an RF-to-DC or RF-IF conversion is used for the measurement and a single sinusoidal RF generator is used to generate the input signal. Most research in this domain has focused on the measurement side via the use of peak or power detectors [10-15]. Two kinds of RF detectors are widely used to measure RF circuit performance. The RF root mean square (RMS) detector relies on the quadratic relationship between the RF input and RF output of the device under test (DUT) [10-13]. The output of the detector is a DC voltage proportional to the amplitude of the detector's input signal. Hence, two identical detectors should be placed at the input and output of the DUT in order to accurately measure the DUT gain. Another popular detector

is an RF envelope detector [14, 15] that relies on a simple rectifier and low-pass filter. If the input is a simple sinusoidal waveform, the detector will yield the amplitude of the signal. Unfortunately, detectors are subject to the same process variations as the DUT, with their gain and DC offsets differing quite widely over process corners.

Gain measurement can be made relative to the input/output amplitudes. Hence, it does not necessarily require the knowledge of absolute signal amplitudes. However, such detectors cannot be used for the measurement of the absolute amplitude of the signal. Existing RF power/amplitude measurement techniques require an initial characterization phase involving RF instrumentation. However, the behavior of these circuits also drifts with in-field wearout, use, and environmental conditions. Hence, a robust, self-calibrating BIST circuit is necessary to enable RF power/amplitude measurements not only during initial production phase, but also in the field as the circuit is subjected to different conditions.

In Chapter 4, BIST system for loopback connection is proposed. The RF transceiver contains two paths with complimentary operation, namely a transmitter and a receiver, which can be placed in a loop-back configuration. Naturally, loop-back based testing of RF transceivers has attracted a lot of attention [5]–[8]. Hence BIST hardware support components are designed and analyzed in terms of area overhead, performance impact, and accuracy.

In Chapter 5, BIST for RF phased array is introduced and discussed. It is progressively more difficult to improve spectral efficiency using pure time and frequency domain methods. Recently, utilization of the spatial dimension to improve spectral efficiency has attracted much attention. The spatial dimension can be used by directing the RF beam

according to the signal frequency. An RF phased array is a special case of a system that uses the spatial dimension. Contrary to a fixed directional antenna system, the phased array enables controlling the beam direction electronically. Phased arrays provide high signal-to-noise ratio (SNR) and directivity [28], [29] and have been used in communication systems for space and military applications [30], car radars, and high-speed point-to-point systems [31], [32].

Since the primary function of the phased array is to shift the phase of the incoming signal, this parameter is of utmost importance. Unfortunately, due to increasing process variations during fabrication, it is increasingly more difficult to match the phases of the elements perfectly. Even a few degrees of error can be detrimental to the phased array operation. Hence, it is absolutely imperative that the phase mismatch of the elements is calibrated, which requires a measurement/calibration approach that involves high frequency signals. Traditionally, measurement of phase and gain mismatch requires the use of an RF network analyzer. Using this equipment, the amplitude and phase of S-parameters are measured and the mismatches are calculated. While a network analyzer is a common piece of test bench equipment, it is an expensive enhancement to the automatic test equipment (ATE). Furthermore, if an RF mixer is integrated on the phased array path in an effort to bring down the measurement signal frequency, the frequency of the RF input signal is different than the frequency of the baseband signal. In such a down-conversion system, it is not easy to define an absolute phase shift between the input and the output signal, and the phase mismatch between phased array elements still needs to be measured and calibrated. High performance synchronized instrumentation, which can simultaneously

generate and analyze signals, is required to measure the phase shift of signals with different frequencies. An instrument that includes this capability increases the cost of the ATE.

Built-in self-test (BIST) is an alternative to lower the test cost by shifting some of the burden to the chip. BIST also brings about the added benefit of in-field calibration, as the use and environmental conditions shift the parameters of the phased array. The additional circuits for test purposes should not affect the performance of the existing RF circuits. This can be enabled by the use of RF couplers rather than RF switches to enable the BIST operation. More importantly, since the BIST circuit is integrated with the circuit under test (CUT), its parameters are also unknown. The test technique should not rely on the knowledge of these parameters. In addition, the test results using the BIST technique should still provide high accuracy compared with the traditional technique using expensive RF equipment.

Various methods to test the phased arrays exist in literature. In [33], [34], the performance of the phased array is tested using an artificial wave front. The wave is generated by feeding the RF inputs to each receiver path via power splitters as well as adjustable phase shifters. The external phase shifters are adjusted until maximum power is reached. At this point, the phase mismatch in the external phase shifters matches the phase mismatch of the phased array. Hence, the phased array phase mismatch is measured in a trial-and-error search manner. This technique is not desirable for high volume production due to the high cost and long test time. In [35], RF signals with a fixed phase are applied to the inputs of two elements, and the output baseband signal is captured for different settings of the phase generators. In this method, the baseband waveforms are measured in time domain using an oscilloscope. However, the phase difference is manually measured

in the time domain, which is not appropriate for a BIST operation. In [36], [37], the BIST method for a phased array RFIC is proposed. The BIST test signal is coupled to all the antenna ports using a 20 dB coupler and a pair of full receivers is integrated on-chip to measure the amplitude and phase of the injected signal, thus determining the channel vector response. In this technique, the output signal is a DC value, since the frequency of the RF test signal is same as the frequency of the receiver local oscillator (LO). However, the circuits in the phased array may include a DC offset, which is unknown, and hence degrade the accuracy of the measurement. This technique also requires large area overhead because two full receivers and an external RF source need to be embedded on the. Moreover, since signals are not combined until the end of the full receiver paths, any mismatch in the receiver paths degrades the accuracy of the measurement.

In [38], the authors propose a test solution for multi-input, multi-output RF systems (MIMO), which have similar parameters to the phased arrays. However, since the intended application is production test, all test signals are assumed to have known amplitude/phase relations and the capture and analysis are done via external equipment. Hence, a new BIST method and the associated circuitry are proposed in order to measure the phase mismatch of the phased array using signals with unknown amplitudes.

In Chapter 6, a technique on process independent gain measurement is proposed via BIST/DUT co-design. RF detectors are subject to the same process variations as the DUT, with their gain and DC offsets differing quite widely over process corners. Gain measurement can be made relative to the input/output amplitudes. Hence, the knowledge of absolute signal amplitudes is not required. However, we cannot assume that the parameters of the detector circuit are known. Even for two identical detectors [10], [11],

[19], within-die mismatch for active devices generates unpredictable DC offsets, which introduces errors in measurements.

Another major issue with RF BIST is the impact on DUT performance due to the additional BIST circuit. Even when BIST can generate accurate results with low area overhead, it is frowned upon by designers due to the parasitics introduced by the BIST circuit that alters the DUT performance. This is particularly troublesome when contact-based BIST is used (e.g. driving the input and sensing the output directly). In [39], the authors show that the performance degradation due to BIST for an LNA is about 1dB for gain, and can be up to 8dB for S11. In this chapter, a BIST solution that is robust with respect to process variations is proposed to determine the gain of an RF DUT.

CHAPTER 2

A COMPREHENSIVE BIST SOLUTION FOR POLAR TRANSCEIVERS USING ON-CHIP RESOURCES

Most communications systems use variable amplitude signals, which necessitate the use of linear PAs with low efficiency. The discrepancy between the output signal level and the supply voltage, which is dissipated as heat, causes the loss in efficiency. This leads to poor battery life and increases heat around the PA, causing reliability concerns. As a solution to this problem, the RF polar transceiver architecture has been proposed.

2.1 Polar Transceiver Overview

2.1.1 Overview of the Polar Transceiver

In polar transmitters, the baseband DSP converts the baseband *I(t)* and *Q(t)* data to polar form, as in Eqn. (2.1) and modulates the carrier with this information, as in Eqn. (2.2). From a modulated signal perspective, this polar-modulated RF signal is mathematically equivalent to the Cartesian modulated RF signal, shown in Eqn. (2.3). Hence, the polar-modulated signal can be received and down converted using a traditional Cartesian receiver.

$$A(t) = \sqrt{I(t)^2 + Q(t)^2} \quad \varphi(t) = \tan^{-1}\left(\frac{Q(t)}{I(t)}\right) \tag{2.1}$$

$$V_{RF}(t) = A(t) \cdot \cos(\omega_c t + \varphi(t)) \tag{2.2}$$

$$V_{RF}(t) = I(t) \cdot \cos(\omega_c t) + Q(t) \cdot \sin(\omega_c t) \tag{2.3}$$

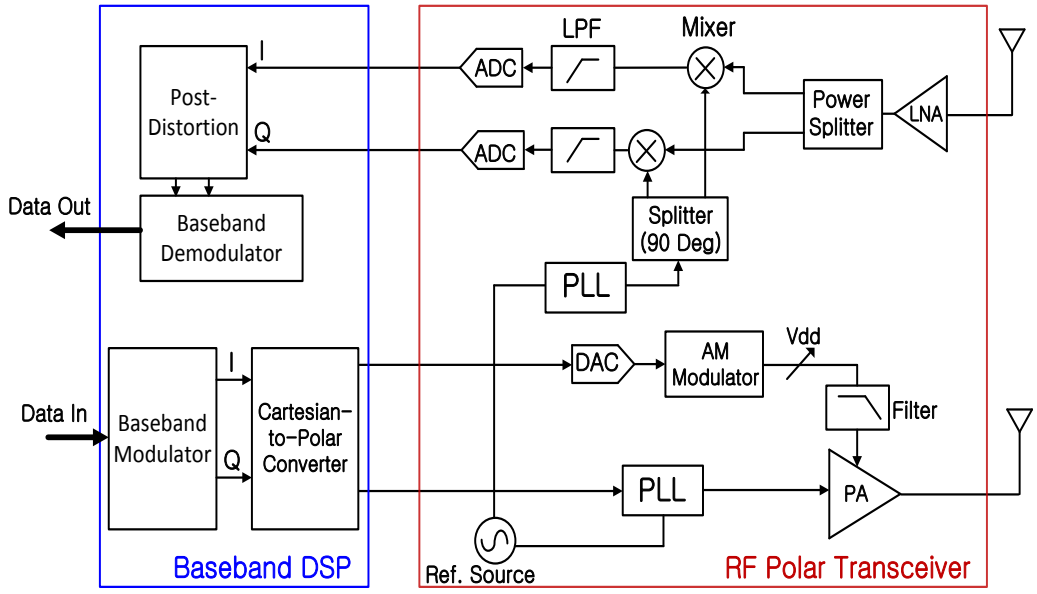


Fig. 2.1. Polar Transceiver Architecture.

Fig. 2.1 shows a typical RF polar transceiver architecture which consists of polar transmitter and IQ receiver. In the transmitter of Fig.2.1, the IQ signal information is converted into a constant amplitude high frequency carrier which is modulated with the phase of the baseband signal, and a low frequency envelope signal which is equal to the magnitude of the original complex IQ signal. The envelope signal is used to modulate the supply of the PA, while the phase modulation is conducted within a phase-locked loop (PLL). The envelope and phase components of the signal are divided into two completely different paths and they must arrive at the PA where they are mixed at exactly the same time. The receiver is implemented using the LNA, mixers, low pass filters, and PLL. Because the receiver includes I and Q paths, in-phase and quadrature component of the RF input signal are recovered at the receiver output.

2.1.2 RF Impairments in the Polar Transceiver

Ideally, the transmitter has to send RF modulated signal which satisfies spectral mask and EVM requirements with high efficiency while the receiver needs to recover in-phase and quadrature components from the RF input signal. Impairments due to the non-linear nature of the underlying devices as well as process variations cause distortion in the transmitted and received signals.

In the transmitter, delay skew between the envelope path and the phase path is detrimental to the operation of the transceiver [40]. As an example, a 100 ns delay skew alone can cause the EVM-EDGE polar transmitter to fail its spectrum mask specifications [23]. In addition to delay skew, a low pass filter (LPF) is located in the envelope path in order to prevent leakage from the supply modulator [25] and it has limited bandwidth (BW). This BW limitation of the envelope signal causes distortion of the RF signal at PA output because the envelope signal may have a high BW compared to filter bandwidth. Nonlinearity of PA with respect to the supply voltage also results in additional distortion. Among these three sources, the delay skew is the most significant contributor to distortion and must be compensated for the transmitter to function. [23], [25]. Envelope bandwidth may also be calibrated by tuning filter components [41], hence suppressing its contribution to the signal distortion. PA non-linearity needs to be characterized and may be compensated using advanced techniques of pre-distortion [42] or post production tuning [43].

In the receiver, process variations cause gain mismatch as well as phase mismatch, which degrade the quality of the received signal [5], [44]. These two impairments can be compensated using post-distortion [43]. More importantly, receiver impairments need to be characterized and calibrated prior to transmitter characterization in the loop-back mode.

There is currently no published work to characterize and de-embed both the transmitter and receiver impairments in the loop-back mode.

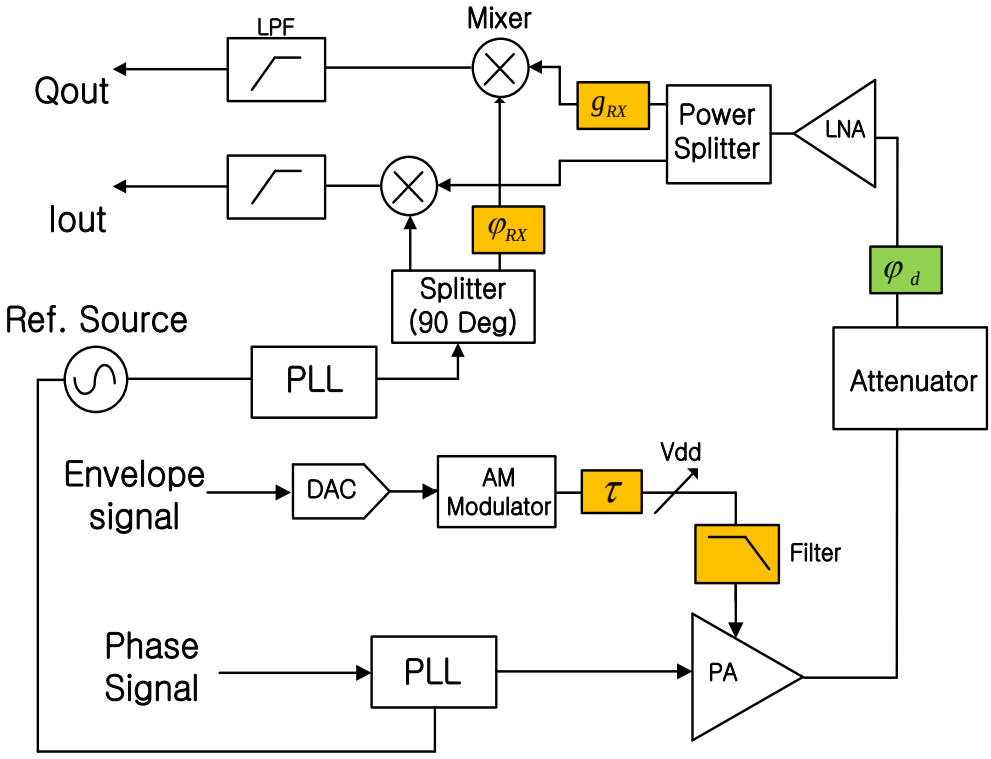


Fig. 2.2. Polar Transceiver with the Impairments in the Loop-Back Mode.

2.2 Test Methodology

In order to develop a technique to measure the target parameters of the transmitter and the receiver, first the transceiver in the loop-back mode needs to be configured. As shown in Fig. 2.2, the output of the PA is connected to the input of the low noise amplifier (LNA) through an attenuator. The RF input of the receiver is down converted to the baseband trough the mixer. The down converted signal is digitized through the ADC and the signal is converted to frequency domain using Fast Fourier Transform (FFT). After taking the FFT, spectral analysis is performed in order to determine the internal parameters. In this chapter,

a BIST solution for the characterization of the entire path is proposed in a step-by step fashion.

2.2.1 Receiver Gain and Phase Mismatch Measurements

Gain and phase mismatches between I and Q channels degrade the performance of the receiver. In order to use digital compensation techniques, gain imbalance needs to be measured within 1% error and phase imbalance needs to be measured within 1^{o} error [45].

The proposed technique uses the baseband output signal of the receiver in the loop-back mode. Even though the polar transceiver uses a variable envelope signal, the baseband parameters can be set such that a single-tone signal will appear at the PA output, transforming the polar transmitter into a single-tone signal generator. Hence, transmitter impairments in terms of delay skew, envelope BW limitation, or PA nonlinearity will not distort this single tone signal and it can be used for receiver characterization. This signal can be obtained by applying a DC signal for the *I(t)* and *Q(t)* input of the polar transmitter, making *A(t)* and *φ(t)* in Eqn. (2.1) constant terms. In the loop-back mode, the receiver outputs are also DC signals, given by Eqn. (2.4) and (2.5).

$$I_{out} = \frac{1}{2} \times A_{in} G_{RX} G(v_{dd1}) \cdot \cos(\varphi(v_{dd1}) + \phi + \varphi_d) + DC_I \tag{2.4}$$

$$Q_{out} = \frac{1}{2} \times A_{in} G_{RX} (1 + g_{RX}) G(v_{dd1}) \cdot \sin(\varphi(v_{dd1}) + \phi + \varphi_d + \varphi_{RX}) + DC_Q \tag{2.5}$$

Where A_{in} is the input of the polar transmitter, GRX is the gain of the receiver, *φ(vdd1)* is the phase of the PA, ϕ is additional delay from RF path and LO path, g_{RX} is gain mismatch, φ_{RX} is phase mismatch between I and Q channel, φd is the delay in the loop-back path, and DC_I and DC_Q are additional DC offsets.

As expressed in Eqns. (2.4) and (2.5), the direct-conversion receivers suffer from the additional DC offsets (DCI and DCQ) because a fraction of the LO signal leaks to the RF port of the mixer due to finite isolation between LO port and RF port. This finite amount of the LO leakage is mixed with the LO signal again, which is called "LO self-mixing". The LO self-mixing generates a DC component which is unknown and combine it with the DC value that is generated by phase and gain mismatches.

From Eqn. (2.4) and Eqn. (2.5), the contribution of the input signal is dependent on amplitude of the input signal. However the DC offset remains constant because LO leakage is not dependent on the amplitude of input signal. In addition, all other DC offsets in the path are a function of process variation, but not a function of the input signal. Hence if two test signals with different amplitudes are used, it is possible to obtain two linearly independent equations to solve for the DC offset term as well as the term related to the input signal. There are multiple ways to generate two different amplitudes at the receiver input. The baseband input amplitude at the transmitter could be changed. However, this would change the supply voltage and also change the phase shift through the PA which would cause uncertainty. Therefore, this simple way of amplitude control is not desirable. An alternate way of generating two different amplitudes is through the loop-back path with a variable attenuator. Of course, in this case, the attenuator through the loop-back path must be treated as an unknown. Hence any knowledge on the input amplitudes, A_1 and A_2 for parameter calculation cannot be assumed. With these two inputs, if the differences of output DC measurements are taken, the DC offset term will disappear as in Eqn. (2.6) and Eqn. (2.7).

$$I_{out,2} - I_{out,1} = \frac{1}{2}\left(A_2 - A_1\right) \cdot G_{RX} G(v_{dd1}) \cdot \cos(\varphi(v_{dd1}) + \phi + \varphi_d) \tag{2.6}$$

$$\begin{aligned} Q_{out,2} - Q_{out,1} = {} & \frac{1}{2}\left(A_2 - A_1\right) \times G_{RX}(1 + g_{RX}) G(v_{dd1}) \\ & \times \sin(\varphi(v_{dd1}) + \phi + \varphi_d + \varphi_{RX}) \end{aligned} \tag{2.7}$$

However, this equation still contains a number of unknowns such as A_1, A_2, $\varphi(v_{dd1})$, ϕ, φd, in addition to the impairment parameters, g_{RX}, and φ_{RX}. In order to decouple the target parameters from the additional unknowns, more information needs to be generated. Note that measurement M_1 and M_2 have non-linear dependency on $\phi_{\text{tot}} = \varphi(v_{dd1}) + \phi + \varphi_d$ as well as φ_{RX}. In order to generate more information, the parameter ϕ_{tot} needs to be adjusted in a predictable manner. Luckily, this can be done using the loop-back path, which is not part of normal operation mode. The loop-back path can be switched between two traces with different lengths without affecting the performance of the transmitter, with a predictable phase difference of $\Delta\varphi_d$. This phase difference depends on the difference in trace length, and can be realized within 0.1% error. Thus Eqns. (2.6) and (2.7) are the difference in I and Q (with two input levels) outputs with one loop-back delay, and Eqns. (2.8) and (2.9) are the difference in I and Q outputs with the same two input levels but different loop-back delay.

$$I_{out,4} - I_{out,3} = \frac{1}{2}\left(A_2 - A_1\right) \cdot G_{RX} G(v_{dd1}) \cdot \cos(\varphi(v_{dd1}) + \phi + \varphi_d + \Delta\varphi_d) \tag{2.8}$$

$$\begin{aligned} Q_{out,4} - Q_{out,3} = {} & \frac{1}{2}\left(A_2 - A_1\right) \times G_{RX}(1 + g_{RX}) G(v_{dd1}) \\ & \times \sin(\varphi(v_{dd1}) + \phi + \varphi_d + \Delta\varphi_d + \varphi_{RX}) \end{aligned} \tag{2.9}$$

With the two input amplitudes set at A_1 and A_2, and the two loop-back delays with a phase difference of $\Delta\varphi_d$, two additional measurements can be obtained if Eqn. (2.8) is

divided by Eqn. (2.6) and Eqn. (2.9) is divided by Eqn. (2.7). The resulting expressions will also be independent of the input signal amplitude which is a quantity that cannot be predicted with high accuracy since it depends on the power amplifier gain and synthesizer output voltage. The results are given by Eqn. (2.10) and Eqn. (2.11) as follows.

$$\begin{aligned}&\varphi(v_{dd1})+\phi+\varphi_d\\&=\tan^{-1}\left(\frac{-(I_{out4}-I_{out3})/(I_{out2}-I_{out1})+\cos(\Delta\varphi_d)}{\sin(\Delta\varphi_d)}\right)\end{aligned} \tag{2.10}$$

$$\begin{aligned}&\varphi(v_{dd1})+\phi+\varphi_d+\varphi_{RX}\\&=\cot^{-1}\left(\frac{(Q_{out4}-Q_{out3})/(Q_{out2}-Q_{out1})-\cos(\Delta\varphi_d)}{\sin(\Delta\varphi_d)}\right)\end{aligned} \tag{2.11}$$

The phase mismatch is determined by subtracting (2.10) from (2.11) and given by (2.12) as follows.

$$\begin{aligned}\varphi_{RX}=&\cot^{-1}\left(\frac{(Q_{out4}-Q_{out3})/(Q_{out2}-Q_{out1})-\cos(\Delta\phi)}{\sin(\Delta\phi)}\right)\\&-\tan^{-1}\left(\frac{-(I_{out4}-I_{out3})/(I_{out2}-I_{out1})+\cos(\Delta\phi)}{\sin(\Delta\phi)}\right)\end{aligned} \tag{2.12}$$

The gain mismatch is computed next by dividing Eqn. (2.7) by Eqn. (2.6) and given by Eqn. (2.13) as follows.

$$g_{RX}=\frac{Q_{out,2}-Q_{out,1}}{I_{out,2}-I_{out,1}}\times\frac{\cos(\varphi(v_{dd1})+\phi+\varphi_d)}{\sin(\varphi(v_{dd1})+\phi+\varphi_d+\varphi_{RX})}-1 \tag{2.13}$$

Note that these computations do not require knowledge of the input amplitude or the loop-back attenuation level. As a result, process variations affecting these parameters will not affect the accuracy of the proposed technique.

2.2.2 Two-Tone Test in the Loop-Back Mode

In order to determine performance of the transmitter, the effect of the delay skew and limited envelop BW should be analyzed. In prior work, it has been shown that these two parameters cause intermodulation distortion (IMD) [27]. Thus, the simple way to analyze these effects is to use a two-tone signal as the input, as in Eqn. (2.14) and analyze the output of the receiver in the loop-back mode. The resulting PA output is represented as in Eqn. (2.15) in polar form where the amplitude signal and the phase signal are given in Eqn. (2.16). Once the transceiver is configured in the loop-back mode, this signal is down converted to baseband at the output of the receiver. It is noted that both amplitude and phase components are still maintained after down conversion in frequency domain as in Eqn. (2.17).

$$V_{RF}(t) = \frac{1}{2}\left(\cos(\omega_c t - \omega_m t) + \cos(\omega_c t + \omega_m t)\right) = \cos(\omega_m t) \cdot \cos(\omega_c t) \tag{2.14}$$

$$V_{RF}(t) = \cos(\omega_m t) \cdot \cos(\omega_c t) = a_y(t) \cdot \cos(\omega_c t + \varphi_y(t)) \tag{2.15}$$

$$a_y(t) = \left|\cos(\omega_m t)\right| \quad \varphi_y(t) = \frac{\pi}{2}\left(1 - c(t)\right) \tag{2.16}$$

$$V_{RX}(t) = \frac{1}{2} G_{RX} a_y(t) \cdot c(t) \tag{2.17}$$

A challenge in modeling this system in the loop-back mode is to maintain phase coherence. As Fig. 2.2 shows, while the two PLLs in the transceiver are synchronized by the same reference source, their phase relation will be random every time a measurement is taken. Therefore it is necessary to include a random phase offset in the receiver LO signal that changes at every step. This additional variable prevents us from using any phase-related information.

In order to analyze the impact of delay skew and BW limitation of the transmitter in the loop-back mode, a time delay, τ, is injected into the envelope signal and express the envelope signal using a Fourier series. The resulting signal at the output of the receiver can be expressed by Eqn. (2.18).

$$\begin{aligned} V_{RX\ \text{with Delay Skew}}(t) &= \frac{1}{2} G_{RX}\, a_y(t+\tau)\cdot c(t) \\ &= \frac{1}{2}\cdot\left(a_0 + \sum_{m=2,4,\cdots,M} a_m \cos(m\omega_m(t+\tau))\right)\cdot\left(\sum_{n=1,3,5,\cdots} c_n \cos(n\omega_m t)\right) \\ &= \frac{G_{RX}}{2}\left(a_0 + a_2\cos(2\omega_m(t+\tau)) + \cdots a_M \cos(M\omega_m(t+\tau))\right) \\ &\quad \times\left(c_1\cos(\omega_m t) + c_3\cos(3\omega_m t) + \cdots\right) \end{aligned} \tag{2.18}$$

Where G_{RX} is gain of the receiver, am is Fourier coefficient of envelope signal, c_m is Fourier coefficient of phase signal, and M is number of harmonics included in envelop signal.

Since the envelope signal, $|\cos(\omega_m t)|$ has sharp discontinuities, the bandwidth of this signal is theoretically infinite. However, the constructed signal has finite frequency components due to the limited bandwidth of reconstruction filter and the supply modulator, which causes IMD. The delay skew between the envelope and the phase signal as well as the PA nonlinearity further increase the IMD levels. The effects of all of these contributors are intertwined and combined in a nonlinear fashion. Thus, they need to be isolated properly in the loop-back mode in order to measure the parameters respectively.

2.2.3 AM/AM and AM/PM Distortion Measurement

The relevant AM/AM and AM/PM distortion for polar transceivers is due to the non-linear relation between the control voltage and PA output. This nonlinearity causes the

violation of spectral mask as well as EVM requirements of the transmitter. Therefore these distortions need to be characterized accurately.

The AM/AM distortion and AM/PM distortion of the PA in the polar transmitter generally are characterized from S-parameter measurements using a vector network analyzer (VNA). The gain and phase of the PA are measured by sweeping supply voltage and measuring amplitude and phase of S21. However, as seen in Fig. 2.2, the PA is integrated in the polar transmitter and the PA input typically is connected to the baseband DSP through the PLL. For measurement using VNA, input and output of the device under test (DUT) should be connected to ports of the VNA. Therefore nonlinearity measurement of the polar transmitter using VNA is not feasible once the PA is integrated into the single chip. In addition, measurement using a high caliber RF instrument such as VNA, is not appropriate for BIST solution.

In order to characterize the PA in the polar transmitter using the proposed BIST solution, the loop-back configuration is desirable, which is already proposed in the previous work. [27] However, in [27], it is assumed that the receiver is ideal, which means that there are no gain and phase mismatches in the receiver. In order to compensate for the gain and phase mismatches of the receiver, the overall signal model must contain this information. With the receiver impairments, the phase and amplitude of the baseband signal at the output of the receiver are given by Eqn. (2.19) and Eqn. (2.20).

$$\begin{aligned}\text{Phase} &= \varphi(v_{dd,n}) + \phi + \varphi_d \\ &= \tan^{-1}\left(\frac{-\dfrac{(Q_{out,n,2} - Q_{out,n,1})}{\left((I_{out,n,2} - I_{out,n,1})(1+g_{RX})\right)} + \cos(\varphi_{RX})}{\sin(\varphi_{RX})}\right)\end{aligned} \tag{2.19}$$

Amplitude

$$= A_{in} G'_{RX} G(v_{dd,n}) = \frac{2 \times \left(I_{out,n,2} - I_{out,n,1} \right)}{\cos(\varphi(v_{dd,n}) + \phi + \varphi_d)} \quad (2.20)$$

$$\left(G'_{RX} = G_{RX} \cos(\varphi_{RF} - \varphi_{LO}) \right)$$

Note that with the two-tone test, the effect of random phase mismatch between the transmitter and receiver PLL is eliminated from the equations. The effect of this phase offset is a part of the term G'_{RX}, which will be treated as an unknown for each separate step. By using comparative analysis, it can be eliminated from calculation. According to Eqn. (2.19), the phase can be calculated from the measured DC values at the receiver output as well as the phase mismatch that is obtained in Eqn. (2.12). Once we calculate the phase, the amplitude of the baseband output can be calculated from Eqn. (2.20). Therefore AM/AM distortion and AM/PM distortion can be characterized in the loop-back mode using the derived equations although the receiver includes phase and gain mismatch.

2.2.4 Delay Skew Measurement in the Loop-Back Mode

For delay skew measurements the three contributors to IMD, namely limited envelope BW, nonlinearity of the receiver, and nonlinearity of the PA, need to be isolated. First the effect of the limited BW should be considered. As indicated in Eqn (2.16), the envelope signal has a square wave component, which makes its BW theoretically infinite. However, signal power diminishes as one moves away from the fundamental tone. If a sufficient number of harmonics are included in the final signal, the distortion caused by the BW limitation can be minimized. In order to enable this, M in Eqn. (2.18) needs to be sufficiently large. At around M >10, the distortion contribution of the BW limitation can be ignored. While the BW of the envelope path is not known yet, it is ensured that M is large by using a low-bandwidth envelope signal.

The second contributor which needs to be isolated is nonlinearity of the receiver. The receiver needs to operate in linear region to eliminate its contributors to the IMD levels. The amplitude of the input signal at the receiver should be sufficiently small to ensure linear operation. Luckily, if the input of the LNA is limited to 3-6 dB below the 1 dB compression point, the IMD generated by the receiver will be negligible. Therefore an attenuator between transmitter output and receiver input is used to ensure that the receiver operates in the linear region.

In addition to the receiver, the PA of the transmitter needs to operate at a voltage where the relation between PA gain and PA supply voltage is mostly linear. Note that this is not possible in the normal mode of operation since the supply voltage is determined by the input stimulus. However, during testing, the test input signals can be set. Hence the PA supply voltage can be maintained at the desired level, which corresponds to around the mid-point of the operation, as shown in Fig. 2.3. When the test signal is set with the abovementioned constraints, the major contributor to IMD at the output of receiver will be the delay skew.

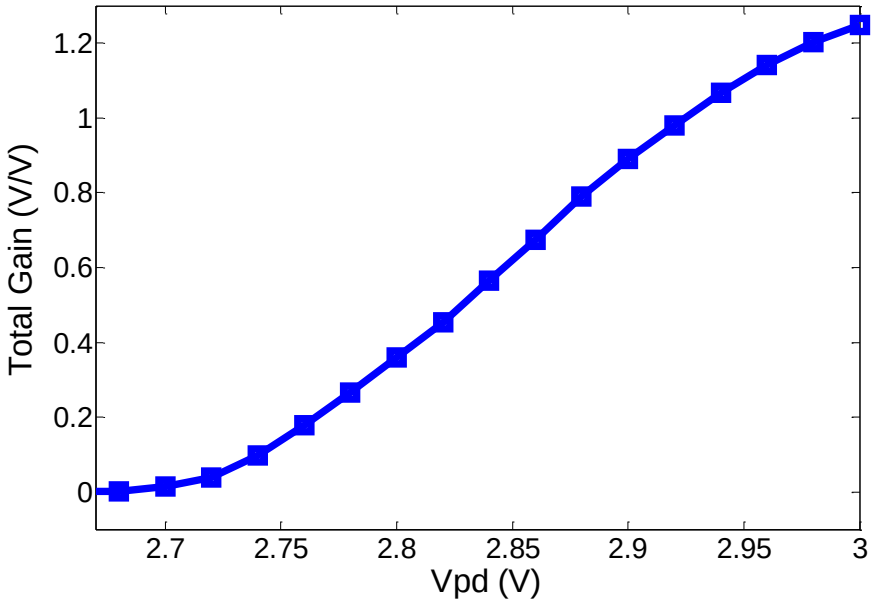


Fig. 2.3. PA Supply Input Versus Receiver Output.

However, determining the primary input signal that satisfies all these constraints is not trivial. The two-tone signal response of the transceiver is given by Eqn. (18). This signal however spans a supply voltage level between zero and maximum. This signal will result in PA to generate IMD and corrupt the information for the delay skew measurements. In order to solve this problem, a DC offset needs to be added to the envelope signal and derive the system response with this new input signal. With the DC offset, the output of the receiver can be expressed as in Eqn. (2.21), where the output amplitude and the DC offset are expressed as in Eqn. (2.22).

$$V_{RX,out}(t) = \left(A_{RX,out} \times \left| \cos(\omega_m (t+\tau)) \right| + \Delta V_{RX,out} \right) c(\omega_m t) \tag{2.21}$$

$$A_{RX,out} = G'_{RX} \times \left(G(v_{dd2}) - G(v_{dd1}) \right) \times A_{in}$$

$$\Delta V_{RX,out} = G'_{RX} \times G(v_{dd1}) \times A_{in}, \quad G'_{RX} = G_{RX} \cos(\varphi_{RF} - \varphi_{LO}) \tag{2.22}$$

In this response, the highest power intermodulation product is the third order intermodulation distortion (IMD3), which can be calculated using Eqn. (2.23).

$$\frac{|IMD_3|}{A_{RX,out}} = \frac{1}{2}\sqrt{a_3^2 + \left(b_3 + \frac{\Delta V_{RX,out} \times c_3}{A_{RX,out}}\right)^2} \tag{2.23}$$

Where a_3 and b_3 are Fourier coefficients, as expressed in (2.24).

$$\begin{aligned} a_3 &= -\frac{2}{\pi}\left[\frac{1-\cos(4\tau)}{4} + \frac{\cos(2\tau)-1}{2}\right] \\ b_3 &= -\frac{2}{\pi}\left[\frac{\sin(2\tau)}{2} - \frac{\sin(4\tau)}{4}\right], \quad c_3 = \frac{-4}{3\pi} \end{aligned} \tag{2.24}$$

It is noted that since $A_{RX,out}$ is also measured, the effect of the unknown gain is eliminated from the IMD3 expression. By using these specified signals, there are no additional unknowns in (2.23) and (2.24). Hence the delay skew can be calculated from the measurement of IMD3.

2.2.5 Envelope BW limitation in the loop-back mode

Once this delay skew is determined, it can be compensated digitally, by leading or lagging the envelope signal, thus minimizing its contribution to IMD. And once the distortion components for delay skew are eliminated, other factors can be measured. To measure the envelope BW, it needs to be emphasized, rather than suppress it. The input signal of Eqn. (2.18) is modified by increasing the bandwidth of the envelope signal. This will spread the harmonics further into the spectrum and reduce the number of harmonics included in the envelope BW. The harmonic contribution of the envelope BW will increase accordingly. The amplitude of the IMD3 with the DC offset voltage at the output of the receiver can be expressed as in Eqn. (2.25) and Eqn. (2.26) according to the number of harmonics (M).

$$\left|IMD_3\right|_{M=2} = \frac{1}{2} \times \left| A_{RX,out} \left[2a_0 c_3 + a_2 (c_1 + c_5) \right] + \Delta V_{RX,out} \times c_3 \right| \tag{2.25}$$

$$\begin{aligned} \left|IMD_3\right|_{M=4} = \frac{1}{2} \times \Big| & A_{RX,out} \left[2a_0 c_3 + a_2 (c_1 + c_5) + a_4 (c_3 + c_7) \right] \\ & + \Delta V_{RX,out} \times c_3 \Big| \end{aligned} \tag{2.26}$$

The direct relation between M and the amplitude of IMD3 at the baseband output of the receiver enables us to generate a lookup table. Thus, once the IMD3 level is measured, the amplitude of IMD3 is compared with the calculated values in the lookup table. From the IMD3 measurement, the number of frequency components that are included in the passband of the filter can be determined. In order to calculate the BW more accurately, this measurement may need to be repeated several times with different baseband signal frequencies and interpolate the results.

2.2.6 BIST Algorithm

The BIST algorithm is based mostly on analytical derivation and carefully crafted test signals. Here, the computational overhead of the algorithm is quite low. Fig. 2.4 shows the flow of the BIST algorithm.

First the system in the loop-back mode is configured by applying the appropriate control signals. Next, the input is set to the single tone signal where the baseband signal frequency is set to the mid-point of the band. Gain and phase imbalance of the receiver are calculated using Eqn. (2.12) and Eqn. (2.13).

Second, AM/AM and AM/PM distortion is characterized in the loop-back mode by sweeping the supply voltage of the PA, measuring the receiver output, and using Eqns. (2.19) and (2.20). Third, the envelope signal amplitude and DC levels is set to the mid-point of the PA operating range and generate the signal at the baseband processor. The

frequency of the baseband signal is set to $f_{bb}/20$ to ensure that at least 10 harmonics are present in the envelope signal after filtering. The envelope/phase skew is calculated as in Eqn. (2.23) and Eqn. (2.24).

Finally, using the calculated skew value, the baseband signal is calibrated and the same measurement is repeated in a binary search fashion between $f_{bb}/3$ and $f_{bb}/20$ until the measured IMD3 levels match with the pre-determined values based on M, as in Eqn. (2.25) and Eqn. (2.26). If a match cannot be found, after 5 iterations, the bandwidth is interpolated between two closest measurements. As shown in Fig 2.5, estimated M (Mest) is given by (2.27)

$$M_{est} = -\frac{IMD_{meas} - IMD(M_i)}{IMD(M_{i+1}) - MD(M_i)} \cdot \left(M_{i+1} - M_i\right) + M_{i+1} \qquad (2.27)$$

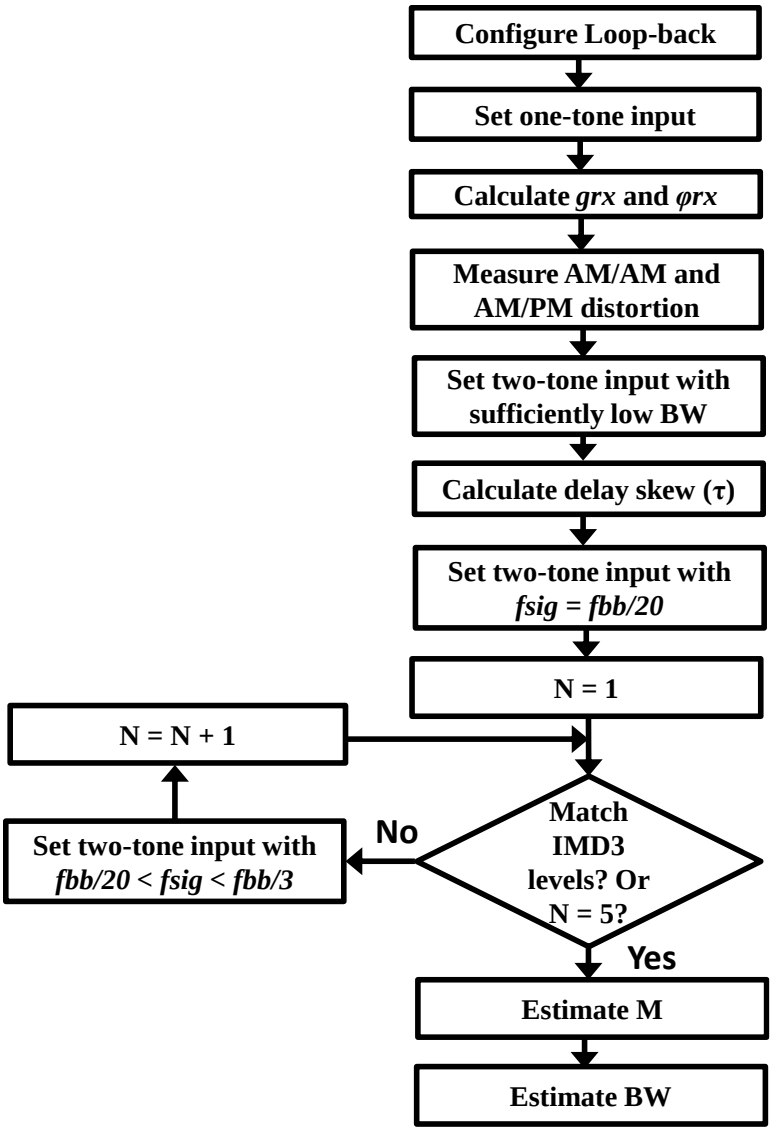


Fig. 2.4. Flow Chart for BIST Algorithm.

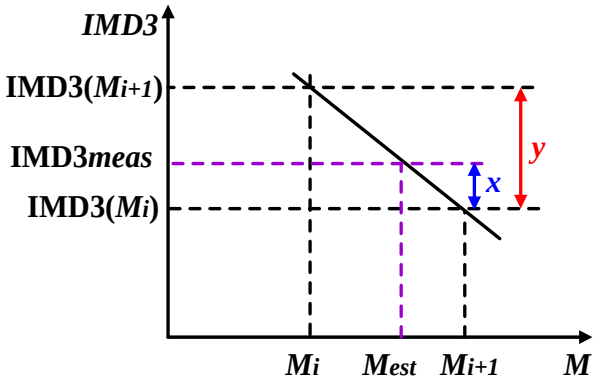


Fig. 2.5. Graph for Estimation of M.

2.3 On-Chip Implementation of the Loop-Back Path

The proposed BIST technique requires minimal hardware support to enable measurements. The hardware components include mainly the loop-back path, which is not part of the design. Note that in all of the derivations, the loop-back path parameters, such as gain, delay, and phase have been treated as unknowns and have been eliminated from the equations using comparative analysis with one exception, namely the phase difference between two loop-back path traces. In this section, the circuit implementation details of the loop-back components are presented and the error is analyzed by this assumption using extracted layout simulations. In the next section, this error is included in the calculations and present accuracy results with the effect of this error.

2.3.1 Loop-Back Path Implementation

As explained III-A, in order to characterize the receiver using the proposed technique, two test signals with different amplitude and another two test signals with different delays are required. Two test signals with different amplitude can be generated by using variable attenuator in the loop-back path. Note that in the derivation, the amplitudes and the relation between them do not need to be known. Hence the effect of process variations is eliminated. The two test signals with different delays can be generated in the loop-back path by switching between two traces with different length. In order to verify a functionality of the proposed concept, loop-back path is designed using 0.18μm IBM 7RF process. Fig. 2. 6 shows the circuit topology for the loop-back path. The proposed loop-back path consists of four single pole double throw (SPDT) switches, two resistors (R_1 and R_2), and two metal lines with different length. The switches are used to select one of two different metal lines as well as one of two different attenuation values.

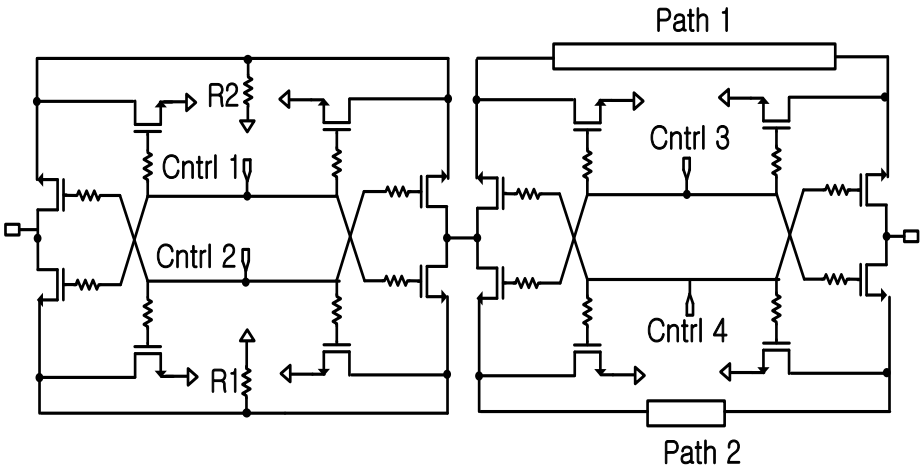


Fig. 2.6. Circuit Topology for Loop-Back Path.

Post-layout Monte-Carlo simulations on the loop-back circuit have been conducted with 50 samples including die-to-die and within-die variations. Table 2.1 shows the delay difference for the nominal circuit as well as the worst-case deviation from the nominal for the 50 Monte-Carlo samples. This data shows that even though process variations severely affect transistor parameters, by designing symmetric switch circuits, and relying on trace differences (which are subject to much lower process variations), the delay difference can be predicted very accurately. Note that the delay difference is the only parameter that is assumed to be known in terms of its absolute value in the entire process. In the next section, the effect of the error that is made in this estimation on the accuracy of the gain and phase mismatch calculations is analyzed. Transmitter parameters do not rely on the estimated delay difference.

Table 2.1. Monte-Carlo Simulation Results for Loop-Back Path

Nominal	**Worst-case**	**Error**
20.32°	20.02 °	0.3°

2.4 Experimental Results

2.4.1 Simulation Results

In order to evaluate the BIST solution for a wide variety of gain and phase mismatches/delay skew/BW scenarios, MATLAB model of the transceiver was implemented in the loop-back mode. RF components of the polar transceiver such as the PA, LNA, attenuator, and mixer are included in the model. Noise and DC offsets which results from LO leakage are also added. In the simulation set-up, all aforementioned impairment parameters are introduced at the same time.

Monte Carlo simulations using the MATLAB model were conducted to inject various impairment parameters, and the proposed technique in the loop-back mode is used to extract the parameters. Fig. 2.7 shows Monte-Carlo simulation results for each parameter and Table II shows the bounds of the injected parameters and RMS error of the extracted parameters in Monte-Carlo simulation. These results indicate that the proposed technique accurately determines the desired parameters.

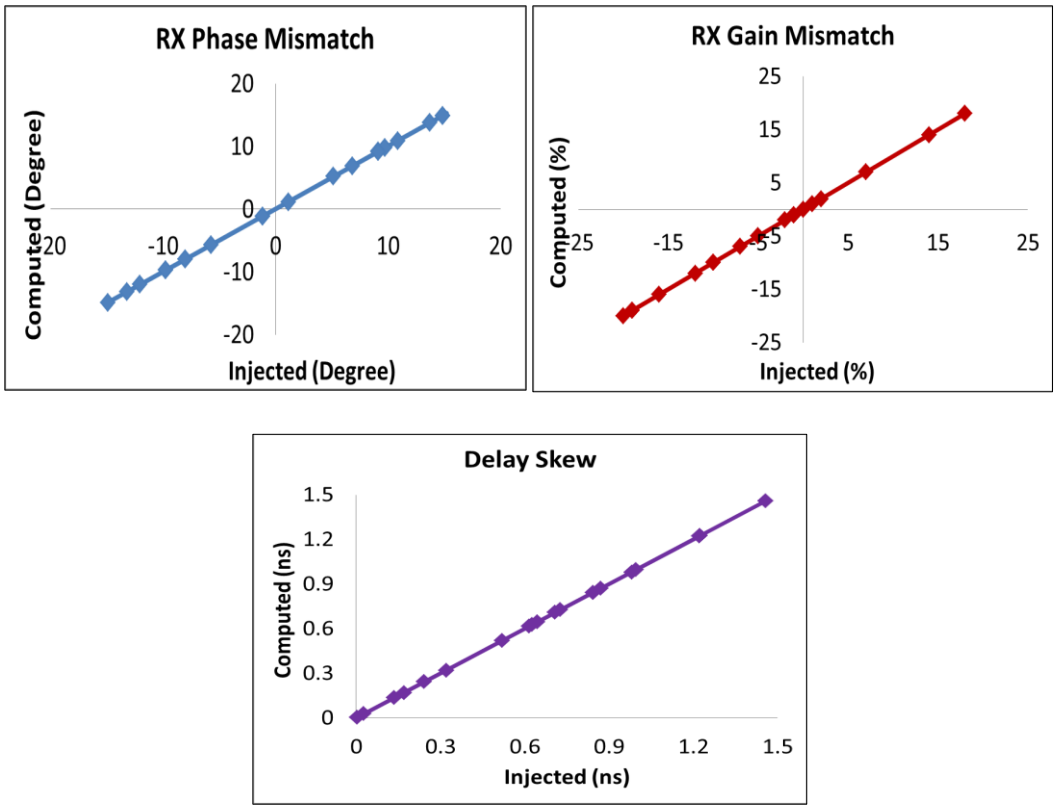


Fig. 2.7. Monte-Carlo Simulation Results.

Table 2.2. Simulation Results for Polar Transceiver Parameters

Parameter	**RMS Error**	**Injection Limit**
Gain Mismatch	0.023 %	[-20%, 20%]
Phase Mismatch	0.015°	[-15°, 15°]
Delay Skew	0.00053 ns	[0ns, 2ns]
M	0	[1, 5]

2.4.2 Hardware Measurements

The polar transceiver was emulated using bench equipment and discrete components. As shown in Fig.2.8, the polar transmitter was implemented using the PA module (Hittite Microwave HMC450QS16G), an arbitrary waveform generator (Agilent Technologies

33250A), and a vector signal generator (Agilent Technologies N5182A). The receiver was formed using discrete components, which consists of LNA (Mini-Circuits ZX60-2522+), RF splitters (Mini-Circuits ZFSC-2-4-S+), 90o RF splitters (Mini-Circuits ZX10Q-2-13-S+), mixers (Mini-Circuits ZFM-15-S+), low pass filters (Mini-Circuits SBLP-117+). The LO signal was generated using analog signal generator (Agilent Technologies N5182A) and the baseband digital signal processing (DSP) unit was built using MATLAB.

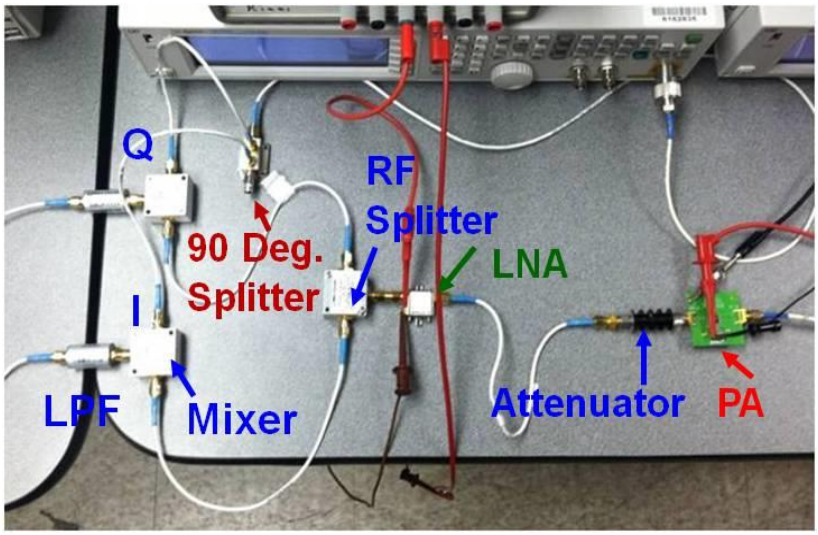


Fig. 2.8. Implemented Polar Transceiver.

The arbitrary waveform generator is used to generate the envelope signal while the vector signal generator is used to generate the phase modulated (PM) signal. Both the envelope and the PM signals should have same clock frequency and be phase locked together in order to extract the delay skew. Additionally, the transmitter and receiver should use same reference clock for coherence. Hence, all equipment should share reference clock to implement complete RF polar transceiver. Fig. 2.9 shows measurement setup with clock synchronization. Synchronization between the envelope and phase generator is ensured by locking the clock of these two pieces of equipment. This clock synchronization enables

that the delay skew remains constant between the envelope path and the phase path. However, phase coherence is not ensured as it will be the case for an IC implementation. In addition, the reference clock source in the receiver also should be same as one in the polar transmitter. Therefore, as seen in Fig.2.9. instruments use same clock source by connecting external 10 MHz output of the vector signal generator to 10 MHz input of the arbitrary waveform generator and 10 MHz input of the vector signal generator to 10 MHz output of the analog signal generator. Fig. 2.10 shows the experimental setup for the polar transceiver characterization, which matches all of the limitation of the IC-based implementation. The overall system works with a carrier frequency of 1 GHz and a baseband frequency of 1 MHz. These values were based on the specifications of the commercial RF components. The technique can be applied to other carrier frequencies.

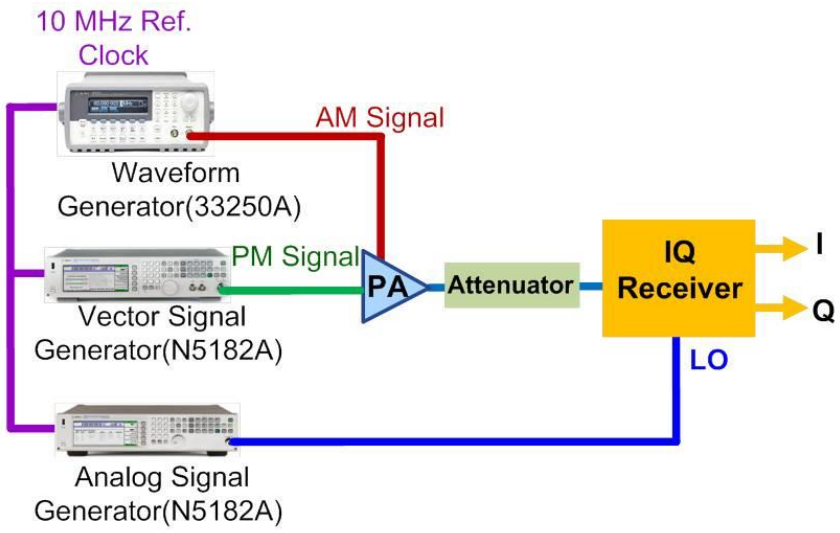


Fig. 2.9. Measurement Setup for Clock Synchronization.

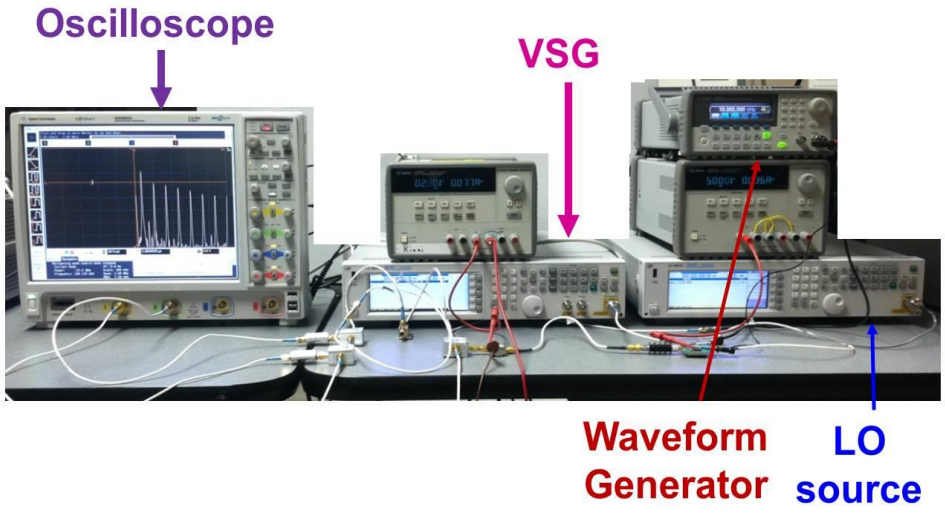


Fig. 2.10. Experimental Setup for Polar Transceiver Characterization.

Measurements for the receiver impairments have been conducted for two different cases. Different phase mismatches were implemented using cables with different lengths. For comparison purpose, impairments of the receiver were measured manually in time domain using the oscilloscope. Table 2.3 shows actual impairments measured from traditional method as well as extracted values from the proposed method. As the results show, analytically computed results from the proposed method are highly accurate compared with values from the traditional manual method. For transmitter characterization, all measurements use the IMD3 information which is obtained by taking the FFT of the baseband signal as shown in Fig. 2.11.

Table 2.3. Measurement Results for Receiver Parameters.

Case	Parameter	Traditional	Proposed	Error
1	Gain MM	-5.4 %	-5.8 %	0.5 %
	Phase MM	-33.9°	-33.5°	0.4°
2	Gain MM	-3.6 %	-3.9 %	0.3 %
	Phase MM	-3.0°	-3.3°	0.4°

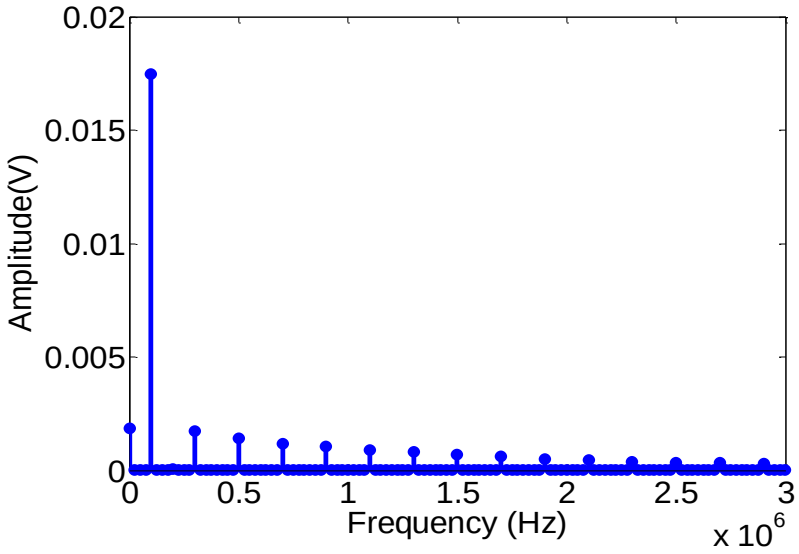


Fig. 2.11. FFT Results of the Output of the Receiver.

In order to verify the accuracy of the proposed delay skew measurement technique, the baseband output response in the time domain is used. The delay skew can be measured manually in time domain in order to compare the proposed technique with traditional method. Fig. 2.12 shows the measured waveform at the receiver output using the oscilloscope. In the waveform, the delay skew can be measured manually because it is expressed as time difference between A and B in Fig. 2.12. Table 2.4 summarizes the comparison of the results. As these results indicate, the proposed technique is able to

measure the delay skews accurately within sub-ns error. Note that compared to [5], the proposed technique provides better accuracy thanks to baseband signal analysis, which can be more accurate than RF signal analysis. As noted earlier, for effective digital calibration, receiver gain mismatch needs to be measured within 1%, phase mismatch needs to be measured within 1° [21], and transmitter delay skew needs to be measured within 50 ns [2]. The proposed test method provides excellent accuracy for these target parameters.

Table 2.4. Measurement Results for Delay Skew

Case	Traditional	Proposed	Error
1	294.2 ns	294.4 ns	0.2 ns
2	453.7 ns	453.8 ns	0.1 ns
3	956.4 ns	955.6 ns	0.8 ns

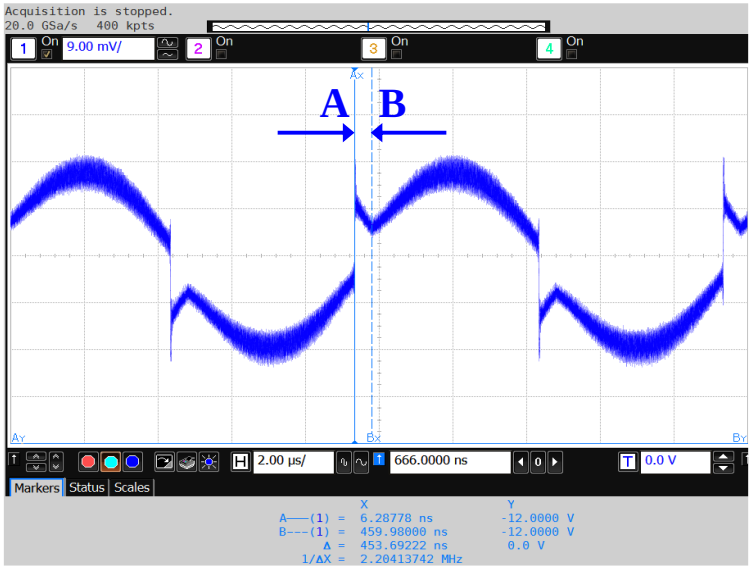


Fig. 2.12. Measurement Results for Verification.

2.4.3 Accuracy of BW measurement

Once the delay skew in the loop-back mode is calculated and compensated, the finite bandwidth in the envelope signal is determined by applying the relatively high bandwidth two-tone signal to the input of the transmitter. Since the other effects such as delay skew and nonlinearity of the transceiver are already minimized, the IMD3 at the output of the receiver is mainly due to the finite envelope BW and the offset voltage. The measured amplitude of IMD3 is compared with the calculated values in the lookup table.

In order to evaluate the BW measurement technique, the envelope path with two different BWs is generated and the algorithm to determine the closest M value for the baseband signal is used. Table V shows the actual BW of the envelope signal, measured IMD3 value, the M value for the closest IMD3 table entry, and estimated BW of the envelope path. Using the algorithm, the BW can be confirmed accurately in less than 5 iterations.

Note that envelope BW measurement requires compensation of delay skew. A potential pitfall in this compensation is frequency-dependent group delay of the envelope filter. The delay skew is measured with one frequency ω_m. This delay is used to calibrate for the effect of skew and calibrated signal is used to measure envelope BW. The envelope BW measurement can have a different frequency than ω_m and in this case there may be a slight variation for the delay through the filter, causing additional IMD that would be attributed to the filter. This variation for a simple RC filter (10 MHz bandwidth) has been analyzed, and the deviation of the delay through the filter has been calculated for the two extreme frequencies (f_m =100 KHz and f_m = 3 MHz) used in delay and BW measurements. It was found that there is a 0.14 ns delay difference through the filter between 100 KHz and 3

MHz baseband input. Then this error was used in the calibration for delay difference and IMD3 component was calculated due to incorrect delay calibration. After that, this error (refer to Table V) was included in the BW calculation and found that it may be cause about 3 % error in the IMD3 calculations. In the experiments, this error does not cause misprediction. It can be safely said that the effect (22μV) is negligible for BW estimation.

Table 2.5. Experimental Results for Envelope BW

	Case 1		**Case 2**	
f_m	100 KHz	3 MHz	100 KHz	3 MHz
Envelope BW	4 MHz	4 MHz	8 MHz	8 MHz
Measured IMD3	1.71 mV	1.77 mV	0.596 mV	0.618 mV
Closed IMD3	1.61 mV	1.61 mV	0.557 mV	0.557 mV
Actual M	2	2	4	4
Estimated M	2	2	4	4
Estimated BW	4 MHz	4 MHz	8 MHz	8 MHz

2.4.4 Accuracy with On-chip loop-back Delay

In order to investigate how on-chip loop-back delay affects the accuracy of the proposed technique, the error in delay difference ($\Delta\varphi_d$) of the worst case from Monte-Carlo

simulation in Table I was taken and it was substituted into Eqn. (12) and Eqn. (13) for gain and phase mismatch computation. The computed values from the worst case are compared with actual values and shown in Table 2.6. As these results show, even with the worst-case delay difference estimation, the gain imbalance can still be determined within 1% error, and the phase imbalance can be determined within 1^{o} error. These error numbers are well within target values for polar transceiver calibration.

Table 2.6. Accuracy with On-Chip Loop-Back Delay

Parameter	**Traditional**	**Proposed**	**Worst Case**
Gain MM	-5.4 %	-5.8 %	-6.0 %
Phase MM	-33.9°	-33.5°	33.28°

2.4.5 Test Time

The proposed technique requires four steps. (a) measurements of gain and phase mismatches between I and Q channel at the receiver (b) voltage sweep at the PA supply input to determine the linear range (c) measurement of delay skew, and (d) measurement of the envelope BW. In order to increase the resolution of the BW measurement, step (d) needs to be repeated multiple times with varying baseband input frequencies. Step (a) and step (b) need several DC measurements and step (c) and step (d) require 1024-point FFT at the output of the receiver. The signal capture time for each step is around 128μs. FFT requires around 1 ms of computation time. Additional computation time for Eqn. (1) through Eqn. (26) is negligible because all of target parameters can be directly obtained based on analytically derived equations. Note that the proposed technique uses same test set-up for all measurement steps. Hence there is no signal source or output switching

overhead. Assuming step (b) takes 15 DC measurements and step (d) is repeated 5 times, the overall test time is less than 50 ms. This overall test time is comparable to one instrument and relay settling time which is generally around 50 ms-100 ms.

2.5 Conclusion

In this chapter, a new BIST solution to measure the internal parameters is proposed for RF polar transceivers, namely gain and phase mismatches, delay skew between the envelope and phase signals, and the finite envelope BW. In order to solve for these parameters using baseband signal analysis, the transceiver in the loop-back mode is configured, the baseband output response of the receiver is observed, and the parameters are extracted using analytically derived equations. Special test signals are developed in the loop-back mode, which enable isolation of the effect of one parameter at a time. First, gain and phase mismatches in the receiver are determined from the measured DC values at the output of the receiver in the loop-back mode. Regarding the transmitter, the delay skew is calculated from the measured IMD3 at the output of the receiver by applying low BW two-tone signal. After compensating for the effect of delay skew, the envelope BW is measured by increasing the BW of two-tone input signal. From the second measurement of IMD3 in the loop-back mode, the finite envelope bandwidth can be estimated by comparing the measured IMD3 with a lookup table that consists of the calculated IMD3 values according to the number of harmonics included in the passband of the reconstruction filter. The loop-back path circuit is designed and its functionality and performance are verified. Based on simulation and hardware measurements, the proposed method determines the critical parameters accurately while eliminating the expensive RF equipment. In addition, the

proposed method enables implementation of BIST and internal calibration for the RF polar transceiver because with complexity, high accuracy, and short test time.

CHAPTER 3

ROBUST AMPLITUDE MEAASUREMENT FOR RF BIST APPLICATION

In this chapter, a new robust BIST solution is proposed to determine amplitude of an RF DUT. The variation issue is solved via (a) analytical modeling of the imperfections in the BIST circuit, and (b) a multi-step measurement procedure with carefully designed input signals. The necessary BIST components have been designed at the transistor level and simulated them over process variations. Experimental results show that the measurement can be attained with high accuracy over process corners. The BIST measurement system have been also constructed using off-the-shelf components, which are inherently subject to process variations, and demonstrated the measurement concept via hardware.

3.1 Proposed Methodology

The configuration of the proposed BIST system is shown in Fig. 3.1. A simple LC oscillator is used to generate the RF test signal and the test signal is amplified and applied to an RF limiter. The limiter generates a square wave with known amplitude. While the RF circuits are band limited, and are expected work with sinusoidal waveforms, it is difficult to generate sinusoidal signals with known amplitudes over process variations. The response of the limiter, on the other hand, is deterministic in terms of the amplitude of the fundamental tone. Its response in terms of the higher order tones is not an issue as will be shown mathematically in this section. Hence, by using the square wave signal, an implicit sine wave can be generated with known amplitude. This square wave test signal is applied to the input of the BIST circuit (measurement system). A self-mixing technique is used for the BIST measurement.

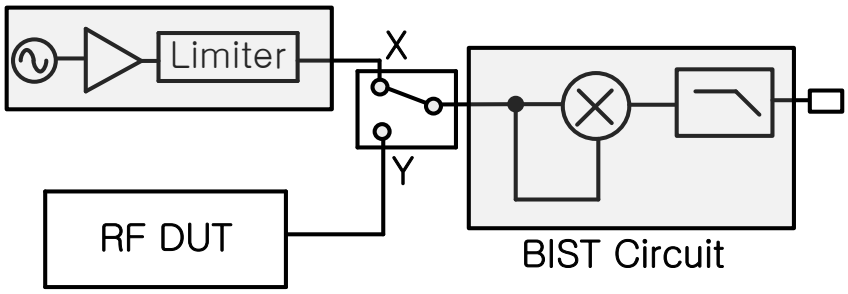


Fig. 3.1. BIST system for an Amplitude Measurement.

The BIST measurement circuitry consists of a mixer and low pass filter (LPF). The test signal (either from the BIST source or from the DUT output) is applied to the input of the BIST measurement system. This signal is divided into two paths before the input of the mixer. Because the RF and LO signals have the same frequency, the IF output of the mixer generates a DC component as well as high frequency component. The LPF removes the unnecessary high frequency component. The measured DC value at the output is determined by four variables: (a) BIST measurement system gain, (b) DUT output amplitude (target variable), (c) path losses, and (d) DC offsets generated in the path. In order to extract the DUT output amplitude, analytical modeling is used for the BIST system response and four consecutive measurements are conducted.

3.1.1 Calibration Phase

During the calibration phase, the signal from the test signal generator is directly connected to the measurement system using switch (SW) connected to node X in Fig. 3.1. The test signal generator consists of an oscillator, amplifier, and limiter. The output of the limiter can be represented as a square wave and is given by Eqn (3.1) as Fourier series:

$$A_{in} = \frac{4}{\pi} A_{BIST} \left[\sin(\omega_{RF} t) + \frac{1}{3} \sin(3\omega_{RF} t) + \frac{1}{5} \sin(5\omega_{RF} t) \right] \qquad (3.1)$$

The square wave is applied to the measurement circuit. Since the mixer used in the measurement circuit performs self-mixing, the signal is multiplied by itself. Therefore, when the mixer operates in the linear region, the IF port of the mixer is given by Eqn (3.2) as follows:

$$V_{o\_mix} = \frac{4}{\pi} A_{BIST} \left[\sin(\omega_{RF}t) + \frac{1}{3}\sin(3\omega_{RF}t) + \frac{1}{5}\sin(5\omega_{RF}t)\right] \times \frac{4}{\pi}\left[\sin(\omega_{RF}t) + \frac{1}{3}\sin(3\omega_{RF}t) + \frac{1}{5}\sin(5\omega_{RF}t)\right] \times G_{BIST}G_{Path} + DC_{Meas} \quad (3.2)$$

Where V_{o_mix} is the signal at the output of the mixer, G_{BIST} is the gain of the BIST measurement system, which includes the conversion gain of the mixer, and insertion loss of the low pass filter. G_{Path} is the total insertion loss of the switch and RF path, and A_{BIST} is the input signal amplitude of the measurement circuit. The crucial point here is that A_{BIST} is known with high accuracy, since it is generated by a limiter. G_{path} and G_{BIST} can be combined into one parameter, since these components do not need to be separated. Because the low pass filter at the IF port of the mixer eliminates high frequency components, only a DC value (V_{o_BIST}) is measured at the BIST output given by Eqn (3.3).

$$V_{o\_BIST} = A'_{BIST}G_{Meas} + DC_{Meas} \quad (3.3)$$

$$A'_{BIST} = A_{BIST}\left[\frac{4}{\pi}\left(1 + \left(\frac{1}{3}\right)^2 + \left(\frac{1}{5}\right)^2\right)\right] \quad (3.4)$$

$$G_{Meas} = \frac{4}{\pi}G_{BIST}G_{Path} \quad (3.5)$$

A'_{BIST} is the BIST signal amplitude which is known, and G_{Meas} is total gain of the measurement circuit. In order to compute $G_{Meas,}$, two measurements with different

amplitudes are needed to isolate DC offset (DC_{meas}) from Eqn (3.3). The measured BIST outputs (M_1 and M_2) are given by Eqn (3.6) and Eqn (3.7) as follows:

$$M_1 = A'_{BIST} G_{Meas} + DC_{Meas} \tag{3.6}$$

$$M_2 = \frac{2}{3} A'_{BIST} G_{Meas} + DC_{Meas} \tag{3.7}$$

The DC offset (DC_{meas}) can be removed by subtracting the second measurement from the first measurement. When subtracting, G_{Meas} is given by Eqn (3.8) as follows:

$$G_{Meas} = \frac{3 \times (M_1 - M_2)}{A'_{BIST}} \tag{3.8}$$

Once G_{BIST} is determined, DC offset is also directly computed from Eqn (3.6) and given by Eqn (3.9) as follows:

$$DC_{Meas} = M_1 - A'_{BIST} G_{Meas} \tag{3.9}$$

3.1.2 Measurement Phase

During the measurement phase, point **Y** of SW in Fig. 3.1 is connected. The output of the DUT is a sinusoidal signal that has amplitude A_{DUT}. It is noted that the amplitude of the input signal of the DUT should be sufficiently small in order to operate DUT in linear region and avoid nonlinearity of the DUT. After the signal is applied to the input of the measurement circuit in the BIST system, the output of the BIST is measured. The output includes the same terms as in Equations (3.6-3.7). The DC output of the measurement circuit is given in Eqn (3.10). Note that there are no additional DC terms due to nonlinearity, since only a sinusoidal signal is multiplied by itself. Finally, the DUT output amplitude can be extracted using Eqn (3.11), since the other terms have already been computed in the calibration phase.

$$M_3 = AG_{Meas}G_{path} + DC_{Meas} \tag{3.10}$$

$$A_{DUT} = \frac{M_3 - DC_{Meas}}{G_{Meas}} \tag{3.11}$$

Since M_3 is a measured value, and DC_{Meas} and G_{Meas} are internal parameters computed during the calibration phase, the amplitude of DUT (A_{DUT}) can be computed. It is important to note that only one RF switch is used in the proposed BIST which has the same loss in the calibration path as in the measurement path. This have been verified premise using transistor level simulations of the BIST system in Fig. 3.1.

3.2 BIST Circuit Implementation

The proposed BIST system is designed and simulated in a 0.18 μm IBM_7RF process with nominal power supply of 1.8V. The BIST system consists of the test signal source and BIST measurement circuitry. Fig. 3.2 shows the entire BIST system. The test signal source is implemented with an LC oscillator, resistors, inverter chain, and RF switch. Fig. 3.3(a) shows the LC oscillator circuit topology, where a spiral inductor is used for the LC resonator. The oscillation frequency is 1.5GHz. The output of the oscillator is amplified by a common-source amplifier and applied to the input of Inverter Chain 1.

It is noted that the output of the inverter chain is a square wave, which has the same amplitude as the supply voltage. A single pole double throw (SPDT) switch is used to connect the test signal to the measurement circuit during calibration as well as measurement phase. Because IIP3 of the switch is 25 dBm and the amplitude of the signals during calibration and measurement phase is much lower than the IIP3, the signals do not suffer from the nonlinearity of the switch. Fig. 3.3(b) shows the switch circuit topology.

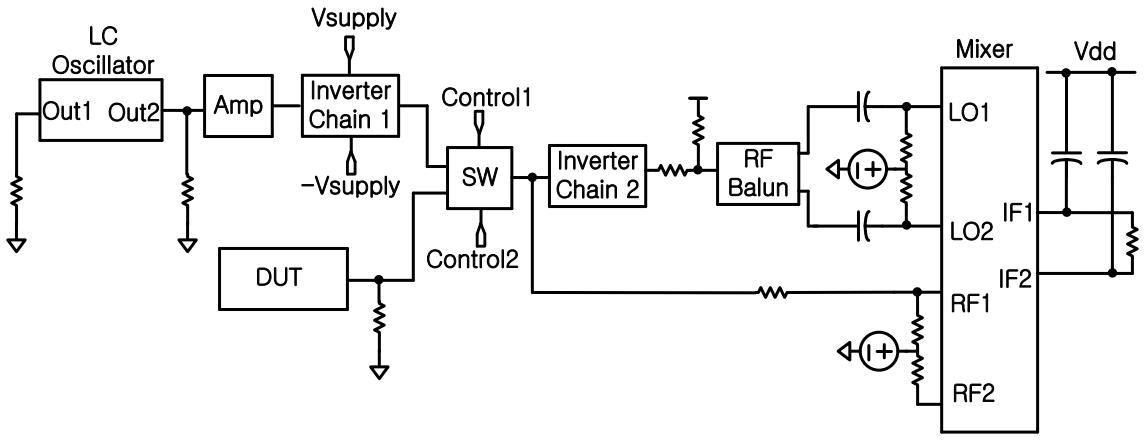
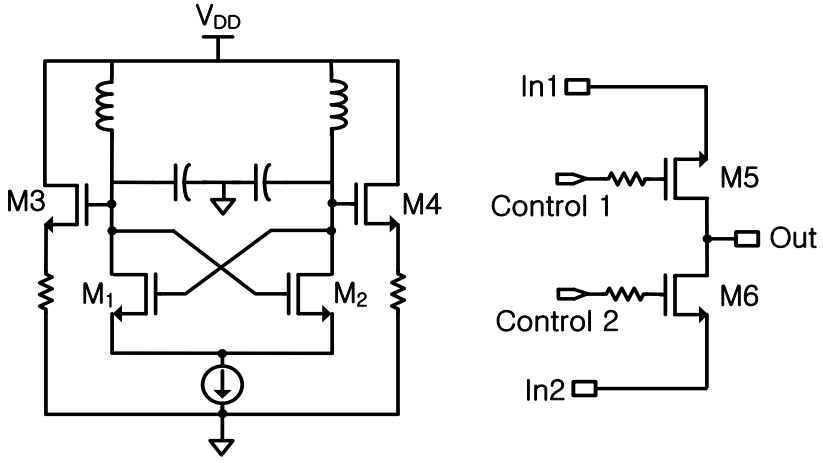


Fig. 3.2. Test Bench for Entire BIST System.

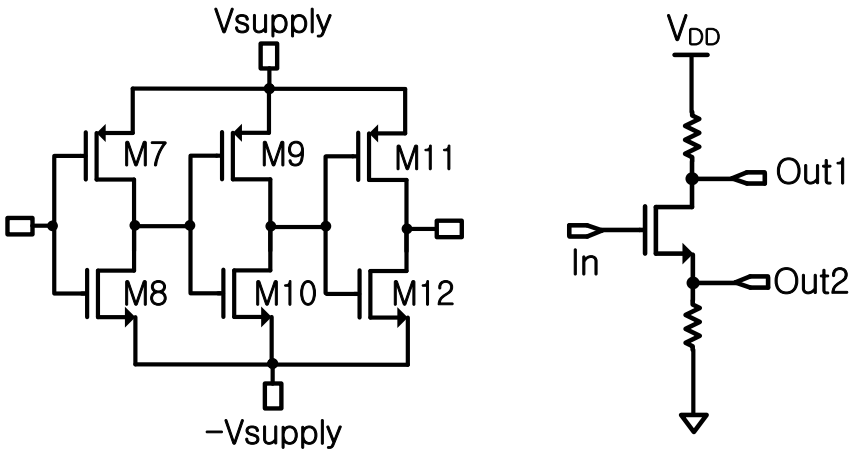


(a) (b)

Fig. 3.3. Circuit Topology of (a) LC Oscillator (b) RF Switch.

The inverter chain used to generate the square wave is shown in Fig. 3.4(a). Two square waves with different amplitudes are generated by adjusting the supply voltage of the inverter chain. In the BIST system, two inverter chains shown in Fig 3.2 is used. In order to keep the conversion gain of the mixer constant, the amplitude of the LO signal should be the same. Therefore, a second inverter chain (Inverter Chain 2) is used to generate an LO signal that has the same amplitude regardless of the amplitude of the DUT output signal.

Since the output of the inverter chain is single-ended, an active balun is designed, shown in Fig. 3.4 (b), to generate differential signals for driving the mixer LO port.



(a) (b)

Fig. 3.4. Circuit Topology of (a) Inverter Chain (b) Active balun.

A Gilbert mixer is designed for the BIST measurement circuitry, as shown in Fig 3.5. The mixer should operate in the linear region because harmonics due to nonlinearity generate extra DC components, which degrades the accuracy of the proposed method. The mixer generally operates in the linear region when the amplitude of the input signal of the mixer is sufficiently small. Therefore, a resistive attenuator is simply added between the mixer and the switch. In addition, in order to avoid impedance mismatch, a 50 ohm resistor is added in shunt at the output of the DUT because the DUT is generally connected to a 50 ohm load for measurement purposes.

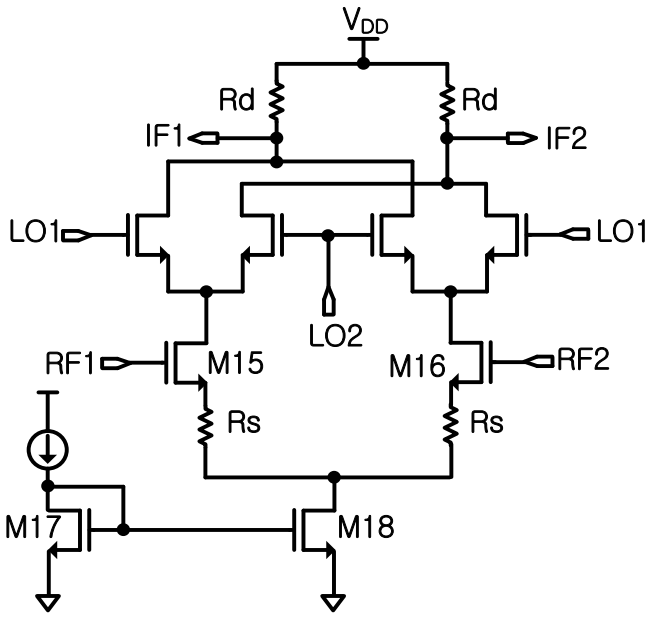


Fig. 3.5. Circuit Topology of Gilbert Cell Mixer.

3.3 Experimental Results

The proposed BIST system is evaluated using both simulations and off-the-shelf components. Simulations are used to show that the proposed technique is robust with respect to process variations, and the hardware experiments are used to demonstrate that the technique can be employed in a practical environment.

3.3.1 Simulation Results

Extensive simulations have been conducted with process variations for the designed circuits. The proposed technique is divided into three sequences. Fig. 3.6 shows the BIST output waveform during each sequence. During the first and second sequences, the measurement circuits are calibrated using two different inverter supply voltages. Once the measurement circuit is calibrated, the amplitude of the DUT is measured during the third sequence. Table 3.1 summarizes the BIST DC output voltages with different supply

voltages, DC offset, and gain of the circuit, G_{Meas}. Table 3.2 compares computed amplitudes of the DUT with actual amplitudes obtained from the simulator.

Table 3.1. BIST Parameter Computation from Simulation

Parameter	**Value**
DC output with Vsupply1	1518.8 mV
DC output with Vsupply2	1512.2 mV
DC offset	1502.3 mV
G_{Meas}	9.4 mV/V

Table 3.2. Output Measurement with BIST from Simulation

Case	**BIST Output**	**DUT output (dBm)**		**Error (dB)**
		Computed	Actual	
1	1516.3 mV	13.5	13.52	0.02
2	1521.2 mV	16.09	16.02	0.07
3	1525.4 mV	17.84	17.95	0.11

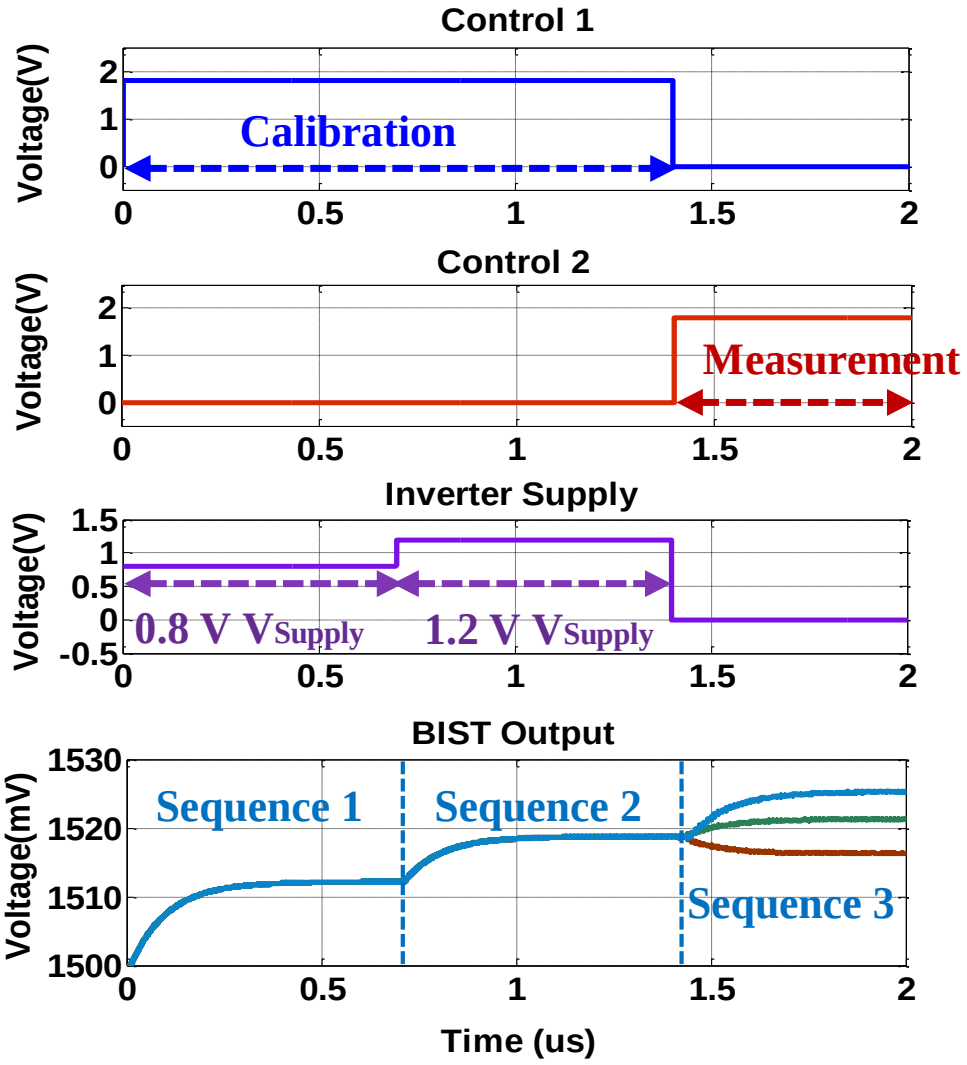


Fig. 3.6. Transient Analysis in Cadence Simulation.

Table 3.3. Monte-Carlo Simulation Results for Output Measurement

Actual	Computed	RMS Error
17.96 dBm	18.01 dBm	1.77 %

The available process design kit is used for Monte-Carlo simulations. As expected, the oscillator output amplitude and the gain of the BIST system vary more than 20%. However, thanks to the self-calibration phase, the major error in the method will stem from

component matching values (which are within 0.1% error) in line mismatch in traces and switch paths. From a 100-sample Monte-Carlo run, the RMS error in predicting the DUT amplitude is 1.77 %, as shown in Table 3.3.

3.3.2 Hardware Measurement Result

For hardware demonstration, a hardware emulation for the BIST circuit is implemented using off-the-shelf components. The circuit is composed of an RF limiter (ZFLM-252-1WL-S+), RF splitter (Mini-Circuits ZFSC-2-4-S+), RF mixer (Mini-Circuits ZFM-15-S+), and low pass filter (Mini-Circuits SBLP-117+). Fig. 3.7 shows the implemented hardware emulation for the BIST circuit. As seen in Fig.3.7, the BIST input signal becomes square wave through the RF limiter and is divided into two paths through the RF splitter.

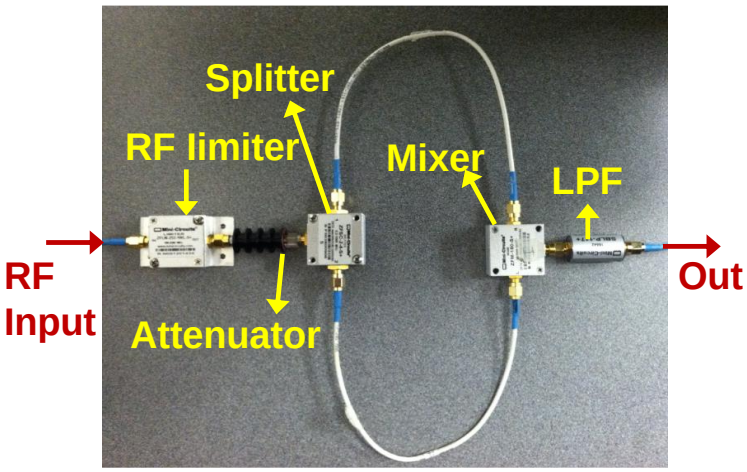


Fig. 3.7. Implemented BIST Circuit for Hardware Experiments.

One is the main path, which is connected to the mixer's RF port, and the other is an auxiliary path connected to the mixer's LO port. Fig. 3.8 shows the measurement setup for the proposed BIST system. A vector signal generator (Agilent N5182A) is used as the primary signal source. However, knowledge of the input signal amplitude is not assumed.

For the hardware experiment, the two test signals are generated by the same source and attenuated using an RF attenuator. The ratio of the amplitudes is set as 1.86. Using the BIST Output measurement results, the BIST system parameters, G_{Meas} and $DC_{Offset,,}$ were computed. Table 3.4 shows the measured DC outputs and the computed parameters

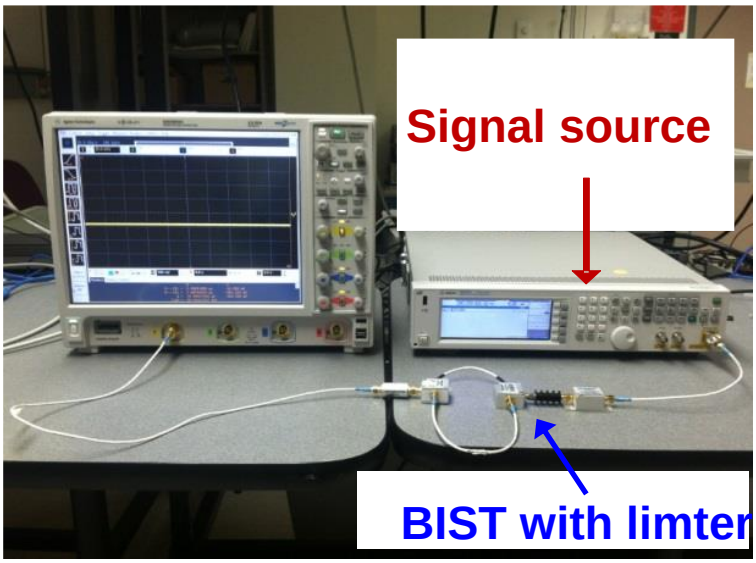


Fig. 3.8. Measurement Setup Experiments.

Table 3.4. BIST Output Measurement and Computed Parameters

Parameter	**Value**
DC output with A_{in1}	-15.81 mV
DC output with A_{in2}	-21.2 mV
G_{BIST}	-145.52 mV/V
DC offset	-65.69 mV

In order to demonstrate the amplitude measurement system, the signal generator as the DUT was used. Measurements have been conducted for 3 different amplitudes. Once the RF test signal is applied to the input of the DUT, the DC output of the BIST circuit is

measured with an oscilloscope. Based on the measurement results, the DUT output signal power was computed and compared with actual power from the signal generator. It is important to note that this experimental set-up is subject to much higher mismatch between the calibration and measurement paths, presented by the traces and switches, compared to an integrated circuit environment. Nevertheless, as the results in Table 3.5 show, the proposed method is highly accurate in computing different power levels.

Table 3.5. Parameter Computation from Hardware Measurements

Case	**BIST Output**	**DUT output (dBm)**		**Error (dB)**
		Computed	Actual	
1	8.3 mV	4.12	4	0.12
2	15.6 mV	4.94	5	0.06
3	25.4 mV	5.93	6	0.07

3.3.3 Test Time and Hardware Overhead

The proposed technique requires four steps. (1) BIST output measurements after applying two test signals with different amplitude to the BIST input (2) calculation of the BIST system's internal parameters, such as BIST circuit gain and DC offset, (3) measurement of the DUT using the BIST system, and (4) calculation of the DUT gain. Steps (1) and (2) require DC measurements (50-100ms each), and Steps (3) and (4) require simple mathematical manipulations. With the control sequences and 3 DC measurements, an IC-based test time is estimated within 500ms.

The proposed BIST circuits have been implemented using 0.18µm IBM 7RF process to verify functionality. Table 3.6 shows the area estimates for the various building blocks of the BIST circuit. Table 3.6 also shows the area estimate of an RF transceiver (RF front-end only) built with a similar technology for comparison purposes [22-24]. The area overhead of the proposed technique is less than 1.2% of the area of an RF front-end. Note that the proposed BIST technique is intended for the entire transceiver. If the gains of individual circuit blocks need to be measured, the same BIST circuit can be re-used with more switches to control the input and output nodes. Since switches are small, enabling multiple gain measurements will result in negligible increase in the area overhead, but will increase the insertion loss within the RF path.

Table 3.6. Area Overhead for RF BIST with IBM 7RF 180nm Process

Circuit	**Area (mm^2)**
Oscillator	0.1
Switch	0.006
Mixer	0.008
Filter	0.002
Total Area (BIST)	0.11
RF Transceiver [46-48]	9
%Overhead	1.2%

3.4 Conclusion

In this chapter, a process-robust technique to measure the output amplitude of an RF DUT using a BIST system is proposed. The BIST system is implemented with a test signal source and BIST measurement circuit. The test signal source is designed using an oscillator, an amplifier, and an RF limiter. The BIST measurement system consists of an RF mixer and low pass filter. The proposed technique consists of two phases: a BIST calibration phase and a DUT measurement phase. During the calibration phase, the internal parameters, such as gain and DC offset of the BIST circuit, are computed and calibrated using analytical equations. After calibration, the DUT is connected to the BIST system and the amplitude of the DUT is measured. The BIST system was designed and simulated in a CMOS 0.18μm IBM 7RF process to verify functionality. The BIST system was also implemented using off-the-shelf components for hardware experiments. Both the simulation and hardware experiments show that the proposed technique accurately determines the gain of an RF transmitter. The BIST system is capable of measuring RF amplitude within 0.1dB error, requires less than 500ms test time, and introduces approximately 0.1mm2 area overhead.

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CHAPTER 4

BIST CIRCUIT FOR LOOPBACK CONNECTION

In this chapter, simple BIST circuitry is proposed to use to place the transceiver in the loop-back mode to initiate the characterization process. The transceiver can be characterized during post production testing and periodically in the field while it is not in use. The computed performance parameters are stored and used for digital calibration.

4.1 Proposed BIST Architecture

4.1.1 BIST circuit for Loop-Back Connection

In order to facilitate the measurements, a loop-back connection that can switch between two phase delays is needed. The precise delays or the delay difference between the paths do not need to be known, the two loop-back paths need to have the same insertion loss, or need to be reasonably matched. Moreover, BIST circuit needs to have a very low insertion loss for the primary path and a respectable attenuation between the PA and the LNA to avoid saturating the receiver. To achieve all of these goals, the loop-back connection with two couplers is designed to sense the PA output and excite the LNA input, a power splitter and a switch is used to select between the loop-back paths, and two metal traces with different lengths is designed to provide the different loop-back phase delays. This BIST circuit, marked as "BIST for Loop-back" in Fig. 4.1 is designed and laid out using 0.18μm IBM 7RF technology and presents with 0.08mm^2 area overhead. The couplers is opted to use for signal connection as opposed to switches (despite slightly larger area), due to very loss insertion loss in the functional path, which is less than 0.17 dB. Another advantage of using the coupler is that in the BIST path, the very low coupling coefficient (-30 dB) provides the necessary attenuation for the PA output. In addition,

Monte-Carlo simulations were conducted and gain mismatch between the two loop-back traces was less than 0.1 dB.

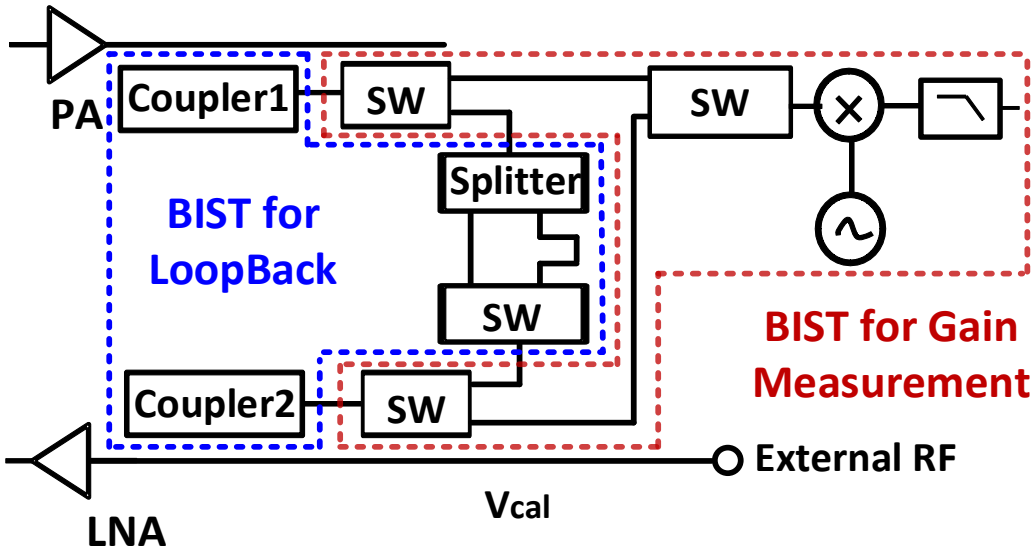


Fig. 4.1. Proposed BIST Circuit in the Loop-Back Mode.

4.1.2 BIST Circuit for Transmitter Gain

In some cases, it may be necessary to measure the linear gain of the transmitter. It is proposed to use the loop-back BIST circuit, which already has the necessary mechanism to sense and inject signals, to measure this gain. The BIST measurement circuit can easily be calibrated during production test with an external source via the LNA input, without any additional pins. There are various detectors proposed earlier for amplitude/power measurement, including envelope detectors [14], [15], and root mean square (RMS) detectors [13]. These existing solutions are not suitable for the requirements, since they require additional steps for measuring and de-embedding the DC offsets. Here, a measurement circuit suitable for low frequency dynamic signals is designed.

4.2 Experimental Experiments

4.2.1 BIST Hardware Demonstration

All of the hardware experiments thus far include the loop-back BIST circuit. The proposed gain measurement BIST circuit has been implemented with discrete components and its accuracy also has been evaluated. This circuit is shown in Fig. 4.2. Note that the gain measurement BIST circuit needs to include the couplers, which is a part of the loop-back BIST circuit. Coupler 1 is located at the output of the transmitter and the coupler 2 is located at the other port which is used for calibration. In the hardware demonstration, an attenuator also needs to be included between the mixer and the RF combiner because the coupler is not designed to have the low coupling coefficient. The low pass filter at the IF port of the mixer eliminates high frequency components, and hence only baseband signal can be captured at the BIST output. Fig.4.3. shows the measurement setup for the BIST circuit. The output of the BIST circuit is baseband sine wave and the amplitude of the signal is used to characterize the BIST gain as well as the output of the transmitter.

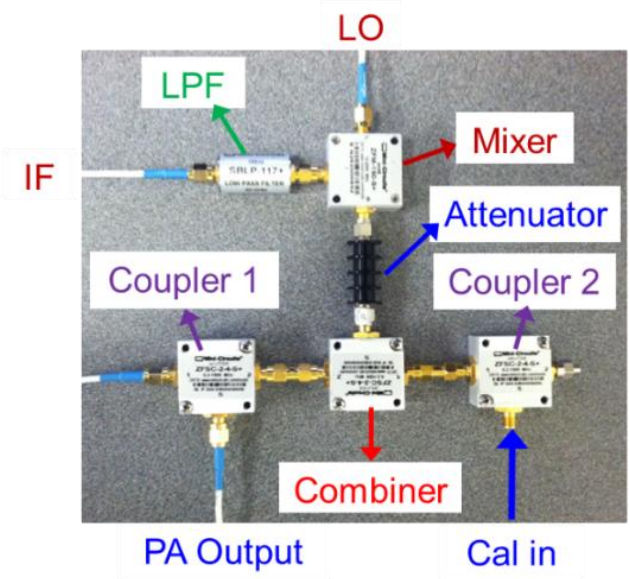


Fig. 4.2. Hardware Demonstration for the Proposed BIST Circuit.

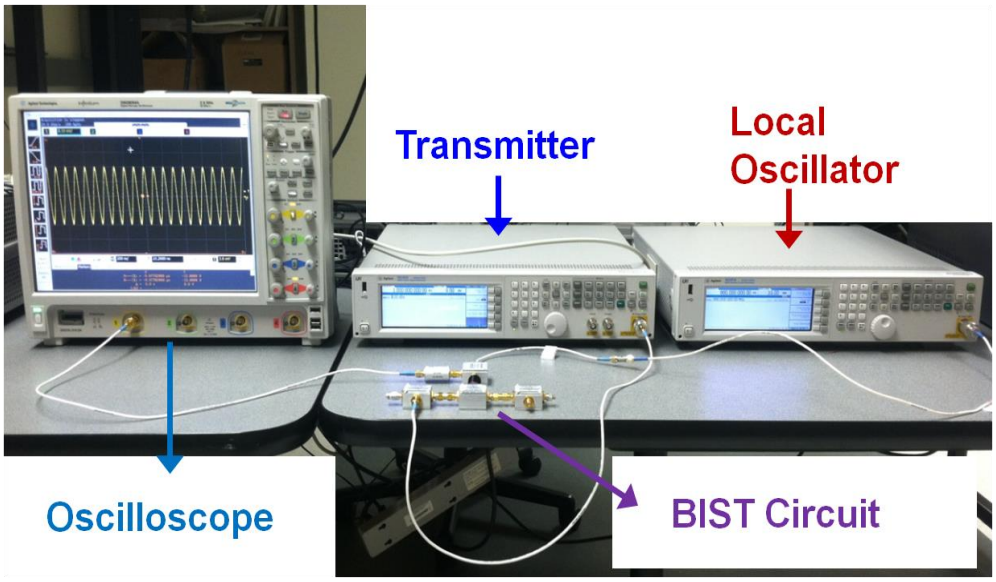


Fig. 4.3. Experimental Setup for the Proposed BIST Circuit.

In the first phase, a single sinusoidal source is applied to the input of the BIST circuit. This step will determine the gain (or loss) of the overall BIST loop, including couplers, switches, and traces. After calibration, this information is used to determine the PA output power. Table V compares the computed power with the actual power. As seen in Table 4.1, the computed power using the technique is highly accurate. Particularly, despite mismatch in components, the transmitter power (or gain) can be measured within 0.1dB error.

Table 4.1. BIST Circuit Measurement Results

Injected Power (dBm)	0	5	10	15
Computed Power (dBm)	-0.045	4.92	9.93	14.99

4.2.2 Area Overhead

The hardware overhead of the BIST circuits have also evaluated. The BIST approach requires no additional pins. The area of each of the BIST circuit components is given in Table 4.2. Compared to RF transceivers (excluding any digital processing) manufactured with the same technology and working in the same band of operation, the total area of both BIST circuit is less than $0.18mm^2$, corresponding to 2% of the area of the transceiver. Hence, with this small additional area, most important parameters of the transceiver can be characterized without any RF instrumentation, and more importantly re-characterized in the field.

4.3 Conclusion

In this chapter, a complimentary BIST circuit to measure the transmitter gain is designed. The accuracy of the technique is verified with hardware measurements. The measured parameters can be used for pre- or post-distortion to calibrate the transceiver, both at production time and in the field.

Table 4.2. Area Overhead Estimate for Loop-Back BIST with 180nm process

Block	**Circuit**	**Area (mm^2)**
BIST for Loop-back	Couplers	0.08
	Splitter	0.0025
	Switch	0.0014
BIST for Gain Measurement	Oscillator	0.088
	Mixer	0.0054
	Switches	0.0042
	Filter	0.002
Total Area (BIST)		0.18
RF Transceiver [46-48]		9
%Overhead	%Overhead	>2 %

CHAPTER 5

ACCURATE ON-CHIP RF PHASED ARRAY CHARACTERIZATION WITH ONLY DC MEASUREMENTS

In this chapter, a new BIST method and the associated circuitry to measure the phase mismatch of the phased array using signals with unknown amplitudes. The basic principles of the proposed BIST method are as follows:

- No absolute measurements are needed or intended.
- The parameters of the BIST circuit are not assumed to be known.
- Signals are combined at the immediate output of the CUT to avoid accuracy degradation due to BIST mismatches.
- Frequency or amplitude of the BIST signals do not have to be precise.
- Path loss due to the RF couplers and switches do not have to be known.

A theoretical framework for a BIST method has been developed with these principles. The accuracy of this technique has been verified with a large number of post-layout simulations. For hardware demonstration, a four-element RF phased array has been built on a PCB and this experimental circuit also has been used for hardware measurements. Both simulations and hardware measurements confirm that the proposed technique can be used to measure the path-to-path phase mismatches with sub-degree error.

5.1 Phased Array : Overview and Challenge

A phased array system (shown in Fig. 5.1) is composed of multiple elements which are spaced with a physical distance. Each element includes a phase shifter used for the electronic beam forming and a variable gain amplifier to match the path gains and increase the signal strength. If the RF wave arrives at the antennas at a specific incident angle, the

wave actually arrives at each element at different time instances. The difference of arrival times between adjacent elements is given by Eqn (5.1).

$$\Delta\varphi = \frac{2\pi d\cos\theta}{\lambda} \qquad (5.1)$$

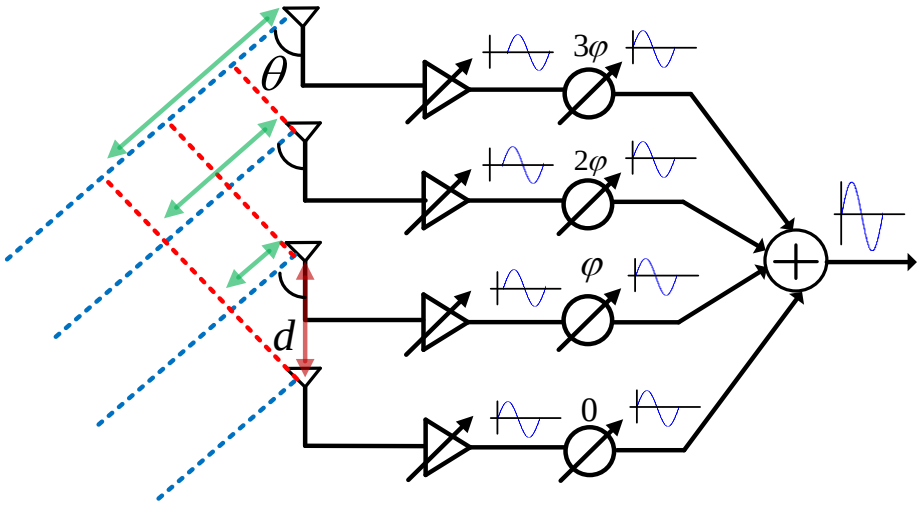


Fig. 5.1. Block Diagram of Phased Array Receiver.

Here, d is the physical distance between adjacent elements, θ is an incident angle, and λ is the wavelength of the received RF input signal. Phase shifters in the phased array adjust the phase between elements in order to coherently combine the elements' output signals, which leads to an RF output with higher power than a single element. In addition, interference signals arriving in the array with different incident angles are nulled according to the array pattern [34]. However, if output signals from each element are not summed coherently, the desired signal will be significantly attenuated,, while the undesired signals will be amplified, thus degrading the SNR. Therefore, the phase mismatch between the elements is the most important parameter for the phased array. A few degrees of phase error may result in 10 dB or more degradation in SNR [36].

Various types of phase shifters are used in phased array applications [49]-[53]. The first technique utilizes an all-pass network with variable resonant circuits [49], [50]. In this technique, the phase is changed by adjusting the capacitance or the inductance of the resonant circuits. A varactor diode is implemented using a FET transistor, and the diode capacitance is changed by varying the transistor's gate voltage. The second technique, called a distributed-type (DT) phase shifter, uses transmission lines with distributed loads [51]. The phase in this type of phase shifter can be changed by switching or tuning the distributed loads along with the transmission lines. An LC lumped circuit can replace the transmission lines to reduce area. Another technique is to use a reflective-type variable phase shifter, which is composed of a transistor, an active circulator, and an LC network [52].

All of the above techniques generally use variable LC circuits, which adopt MOS varactors for variable capacitance and transistors for variable inductance. These components are particularly sensitive to process variations and the resulting phase can deviate significantly from the desired value. Unfortunately, a phase error that is on the order of a few degrees significantly degrades SNR. However, since controllable devices are used on the phased array, the phase mismatch can be calibrated. This requires high accuracy measurement of the phase mismatch between paths. For low cost testing and calibration, a technique to accurately measure the phase mismatch for phased arrays without using expensive RF equipment is needed. In addition, the new technique needs to be suitable for a BIST solution in the sense that the knowledge of BIST circuit parameters cannot be relied on, such as absolute signal amplitudes and gains in the BIST path. The desired accuracy of the BIST measurement and calibration should be within 1° for state-of-the-art performance.

5.2 Proposed Method

In the prior work [17], the method to determine the gain and phase mismatch for RF phased array is proposed. In this chapter, BIST test signal source as well as BIST measurement system implement is implemented on-chip. And the BIST system is also fabricated with IBM 180 nm process. In addition, process-robust BIST input circuit is proposed and designed.

In the proposed technique, a single-tone RF sinusoidal stimulus whose amplitude and phase does not need to be known is generated, and DC signal analysis is used for ease of on-chip implementation. Fig. 5.2 shows the block diagram of the proposed technique. The BIST method is based on the observation that the system performance is primarily determined by the mismatches between the elements while the absolute values of element parameters (gain, phase) are not at issue. Hence, all measurements can be made relative to one another. Relative measurements greatly simplify the BIST design. On the input side, the BIST circuit includes a waveform generator, a power splitter, a number of switches, and couplers to control the primary circuit input. On the output side, the output of the phased array is applied to the input of the BIST circuit through an RF switch.

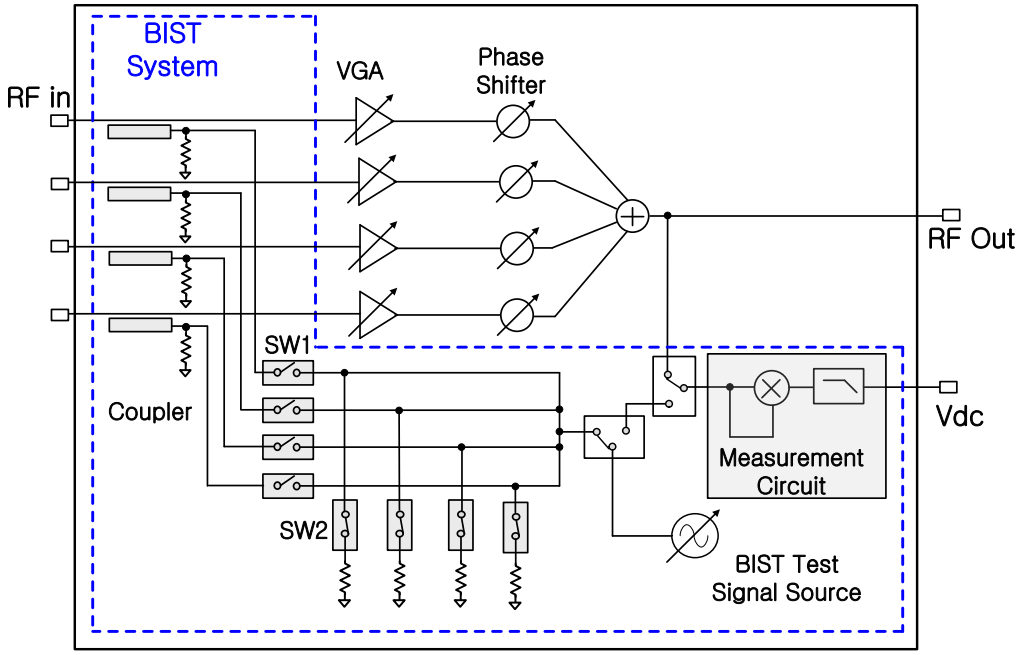


Fig. 5.2. Block Diagram of Proposed BIST for Phased Array.

It is noted that the output of the phased array is divided into two paths through an RF splitter, and one of the outputs is connected to the RF port of the mixer while the other path is connected to the LO port of the mixer. Since the same output signal is used at both mixer ports, an additional LO signal source is not necessary. The amplitude of the LO signal needs to sufficiently drive the LO port of the mixer. The output path down-converts the high frequency signal to a DC signal, and the low pass filter (LPF) removes high frequency components to enable on-chip measurement and analysis. The resulting DC output is digitized by an existing ADC, which usually has 8-10 bit resolution. It is important to note that all mismatches contributing to the phase of each path, not just the phase shifters, are included in the self-test path in a manner identical to the normal operation mode.

The proposed technique consists of three phases. The first phase (Phase I) compensates for the internal parameters of BIST circuit such as DC offset. The Phase 1 is conducted by applying a sinusoidal signal to the input of the BIST measurement circuit. The output signal

of the BIST measurement circuit are saved in memory and used to compute gain and phase difference of the phased array. In the second phase (Phase II), the gain of each path is determined by applying the BIST signal sequentially to each path and measuring the output signal of the BIST measurement circuit. During the third phase (Phase III), the BIST test signal is applied simultaneously to two adjacent elements in the phased array for the measurement of phase difference. During the Phase III, amplitude of test signal which is applied to two inputs of phased array must be same as the amplitude of test signal during Phase II. In order to do that, all ports at the output of the divider should be terminated to same resistor regardless of status of switch. In Fig. 5.2, when test signal is applied to two inputs of the phased array, the other two paths at the output of the divider should be terminated to 50 ohm since impedance of the coupler is also 50 ohm at operating frequency. Hence parallel switches are added with 50 ohm resistor at the outputs of the divider. It is noted that all parameters need to be computed from only DC values measured at the output of the BIST measurement circuit, since a self-mixing technique is used for the BIST circuit. However, the measured DC value includes not only the target parameters but also DC offset due to LO leakage. Since all terms are at the same (DC) frequency, they must be separated from each other.

In order to compute the parameters from only DC outputs of the BIST circuit, a mathematical model is analytically developed in this chapter. The splitter and RF switches can be implemented on-chip (for in-field calibration) or on the load board (for production testing and calibration) in order to lower the cost and achieve a stable test setup. Output signals at the baseband can be analyzed by the DSP to compute target parameters such as gain and phase shift in RF phased arrays.

5.2.1 Phased I : BIST Self-Loop

In Phase I, a sinusoidal test signal which is generated in BIST test signal source is applied to the BIST circuit and the output of the BIST circuit includes only DC values because self-mixing technique is used. However, the DC value at the output of BIST measurement circuits includes gain of the BIST measurement circuit as well as the DC offset due to LO leakage. The DC offset needs to be separated from the gain of BIST measurement circuits using two measurements of the BIST system, in which the input signals are sinusoidal signals that have different amplitude. In Phase I, the BIST test signal source with two different amplitudes is directly connected to the BIST measurement circuits and then the responses at the intermediate frequency (IF) port of the mixer are given by Eqn. (5.1) and Eqn. (5.2) respectively as follows.

$$A_1 G_{SW} \cos(\omega_c t) \times A_{LO} \cos(\omega_c t - \theta)\, G_{Mixer} + DC_{Meas} \qquad (5.1)$$

$$A_2\, G_{SW} \cos(\omega_c t) \times A_{LO} \cos(\omega_c t - \theta)\, G_{Mixer} + DC_{Meas} \qquad (5.2)$$

Because output responses of the mixer in Eqn. (5.1) and Eqn. (5.2) include high frequency components which are eliminated through LPF. After the LPF, the output responses at BIST measurement circuits are given by Eqn. (5.3) and Eqn. (5.4) as follows.

$$M_1 = A_1 G_{SW} G_{BIST} + DC_{Meas} \qquad (5.3)$$

$$M_2 = A_2 G_{SW} G_{BIST} + DC_{Meas} \qquad (5.4)$$

Where GBIST is the gain of the BIST measurement circuit that includes conversion gain of the mixer, and insertion loss of the low pass filter. GSW is the total insertion loss of the switches, and A is the input signal amplitude.

The DC offset (DC_{Meas}) can be removed by subtracting the second measurement (M_2) from the first measurement (M_1). The result from the subtraction is given by Eqn (5.5).

This term is the compensation term for the BIST circuit and will be used to calculate the parameters of the DUT.

$$M_2 - M_1 = (A_2 - A_1)G_{SW}G_{BIST} \quad (5.5)$$

5.2.2 Phase II: Gain Measurement

During Phase II, the BIST test signal is applied to the input of LNA. After two test signals that have the same amplitude as in Phase I are applied to the input of the LNA, the output responses of the mixer in BIST measurement circuits are given by Eqn (5.6) and (5.7) as follows.

$$A_1 G_{LNA} G_{SW} \cos(\omega_c t) \times A_{LO} \cos(\omega_c t - \theta)\, G_{Mixer} + DC_{Meas} \quad (5.6)$$

$$A_2 G_{LNA} G_{SW} \cos(\omega_c t) \times A_{LO} \cos(\omega_c t - \theta)\, G_{Mixer} + DC_{Meas} \quad (5.7)$$

Similar to Eqn. (5.3) and Eqn. (5.4) in 5.2.1, output responses of the BIST measurement circuits after LPF are given by Eqn. (5.8) and Eqn. (5.9) respectively as follows.

$$M_3 = A_1 G_{LNA} G_{SW} G_{BIST} + DC_{Meas} \quad (5.8)$$

$$M_4 = A_2 G_{LNA} G_{SW} G_{BIST} + DC_{Meas} \quad (5.9)$$

where G_{path} is a gain of each path in the phased array. The DC offset (DC_{Meas}) in the measurement step also can be removed by subtracting the fourth measurement (M_4) from the third measurement (M_3) and the subtraction result is given by Eqn. (5.10).

$$M_4 - M_3 = (A_2 - A_1)G_{LNA}G_{SW}G_{BIST} \quad (5.10)$$

In Eqn (5.10), it is noted that $(A_2 - A_1)G_{SW}G_{BIST}$ is already determined during phase I. Therefore, gain of each path is determined by simply dividing Eqn. (5.10) by Eqn. (5.5) and is given by Eqn. (5.11) as follows.

$$G_{LNA} = (M_4 - M_3)/(M_2 - M_1) \quad (5.11)$$

5.2.3 Phase III: Phase Mismatch Calculation

Once the gain of each path is computed, phase difference between adjacent can be determined. In order to determine the phase difference, the same two test signals as in previous phases are applied to the inputs of two adjacent paths of the phased array. The output responses of the mixer are given by Eqn. (5.12) and Eqn (5.13) as follows.

$$A_1 G_{comb\_i} G_{SW} \cos(\omega_c t) \times A_{LO} \cos(\omega_c t - \theta)\, G_{Mixer} + DC_{Meas} \qquad (5.12)$$

$$A_2 G_{comb\_i} G_{SW} \cos(\omega_c t) \times A_{LO} \cos(\omega_c t - \theta)\, G_{Mixer} + DC_{Meas} \qquad (5.13)$$

Where G_{comb_i} is the gain of two adjacent paths when a test signal is applied to the two paths.

After the low pass filter the measured DC values at the output of the BIST measurement circuit are given by Eqn (5.14) and (5.15).

$$M_5 = A_1 G_{comb\_i} G_{SW} G_{BIST} + DC_{Meas} \qquad (5.14)$$

$$M_6 = A_2 G_{comb\_i} G_{SW} G_{BIST} + DC_{Meas} \qquad (5.15)$$

After subtracting Eqn (5.15) from Eqn (5.14), DC offset in Phase III is eliminated and the result is given by Eqn (5.16) as follows

$$M_6 - M_5 = (A_2 - A_1) G_{comb\_i} G_{SW} G_{BIST} \qquad (5.16)$$

Once the DC offset is removed, G_{comb_i} is computed by dividing (5.16) by (5.5) and given by Eqn (5.17) as follows.

$$\Delta\varphi_i = cos^{-1}\left[\frac{1}{2}\left(\frac{A_{comb\_i}^2 - (A_i^2 + A_{i+1}^2)}{A_i \times A_{i+1}}\right)\right]$$

$$= cos^{-1}\left[\frac{1}{2}\left(\frac{\left(A_1 G_{comb\_i}\right)^2 - \left[\left(A_1 G_{path\_i}\right)^2 + \left(A_1 G_{path\, i+1}\right)^2\right]}{A_1 G_{path\_i} \times A_1 G_{path\, i+1}}\right)\right]$$

$$= cos^{-1}\left[\frac{1}{2}\left(\frac{\left(G_{comb\_i}\right)^2 - \left[\left(G_{path\_i}\right)^2 + \left(G_{path\,i+1}\right)^2\right]}{G_{path\_i} \times G_{path\,i+1}}\right)\right] \qquad (5.17)$$

Eqn (5.17) includes three variables, $G_{comb\_i}, G_{path\_i}, G_{path\_i+1}$ which are already determined in Phases I, II, and III. It is noted that the phase difference can be determined with only measured DC values at the output of the BIST measurement circuits. Namely, the precise amplitude of the test signal and ratio of the test signal amplitudes are not necessary for the phase difference measurement. Furthermore, phase mismatch is computed only using DC measurements from Phases I, II, and III.

5.3 BIST Circuit Implementation

5.3.1 BIST Circuitry Design

The proposed BIST system is designed and simulated in a 0.18 μm IBM_7RF process with nominal power supply of 1.8V. The BIST system consists of the test signal source and BIST measurement circuitry. Fig. 5.3 shows the entire BIST system. The test signal source is implemented with an LC oscillator and RF switches. Fig. 5.4(a) shows the LC oscillator circuit topology, where a spiral inductor is used for the LC resonator. The oscillation frequency is 1 GHz. The amplitude of the signal is controlled via the control input.(I_{bias}).

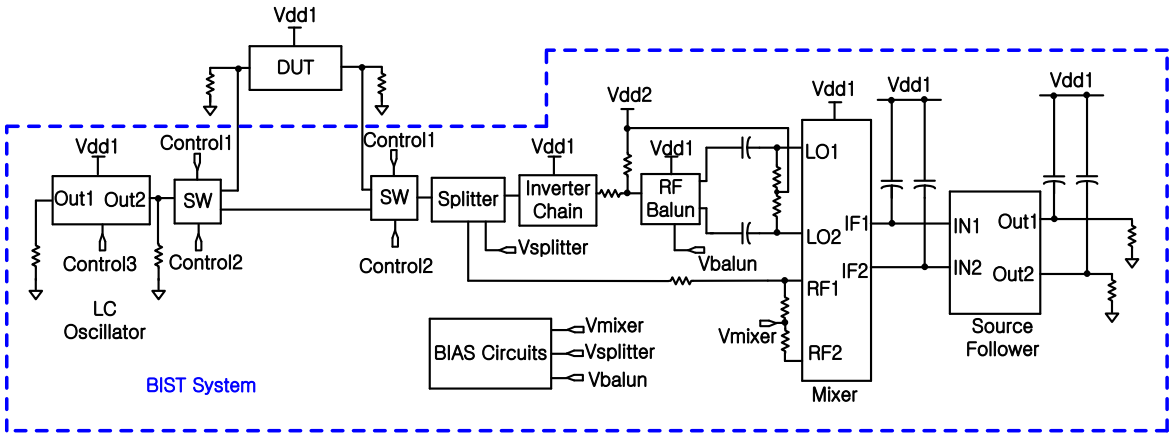
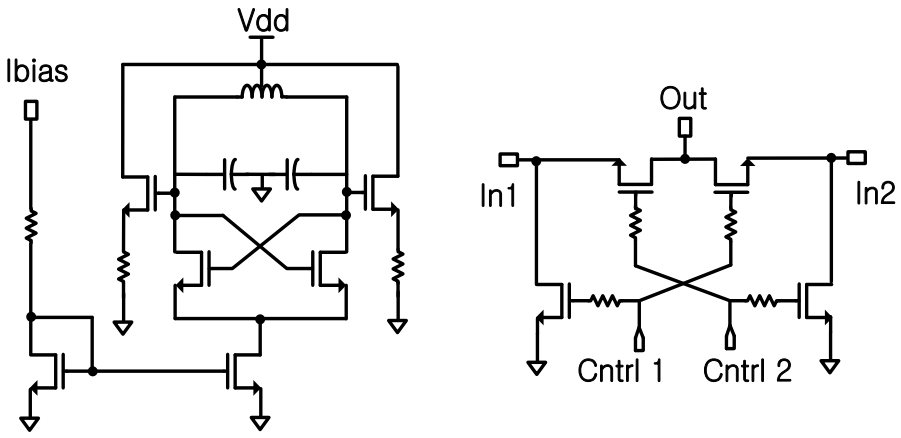


Fig. 5.3. Block Diagram of Proposed BIST system.

The BIST method only requires that the two input signals have distinctly but the exact relation between them does not need to be known. This relaxation greatly simplifies the BIST design, as the exact value of the control signal and the output signal amplitudes do not need to be determined. In addition, although the LC oscillator is in an open-loop, and its frequency varies with respect to process variations, there is no frequency mismatch thanks to self-mixing.



(a) (b)

Fig. 5.4. Circuit Topology of (a) LC Oscillator (b) RF Switch.

Fig. 5.4 (b) shows topology of single-pole double-throw (SPDT) RF switch circuit topology. In order to improve isolation, parallel switches are added to each path. The BIST measurement circuit consists of a splitter, inverter chain, balun, and mixer. Because the proposed BIST measurement circuitry use self-mixing technique, the input of the BIST measurement circuits should be divided into two path. Active splitter is used to convert single-ended signal to differential signal. Fig. 5.5 (a) shows topology of the active splitter used in the proposed BIST measurement circuit. In order to keep the conversion gain of the mixer constant, the amplitude of the LO signal should be the same for all RF BIST input signal amplitudes. Therefore, an inverter chain shown in Fig. 5(b) is used to generate an LO signal that has the same amplitude regardless of the amplitude of the DUT output.

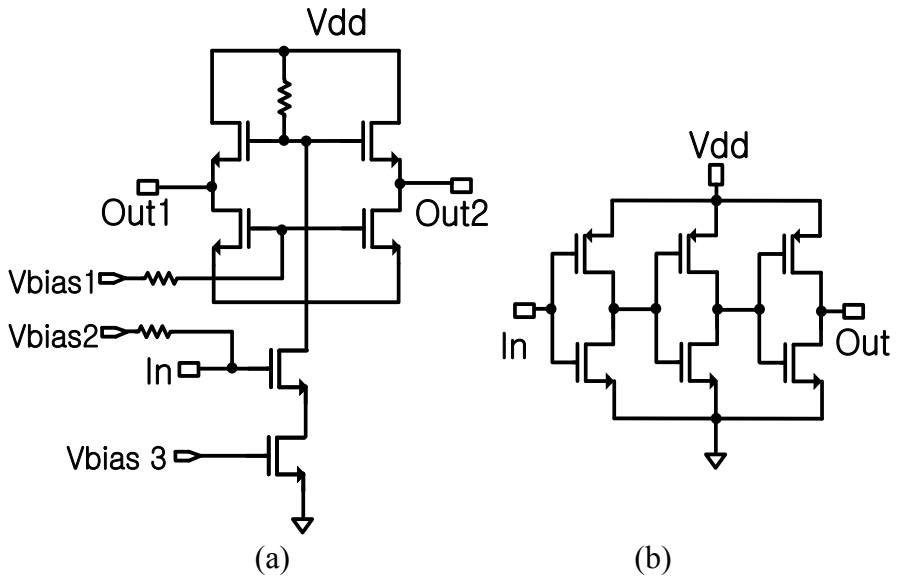
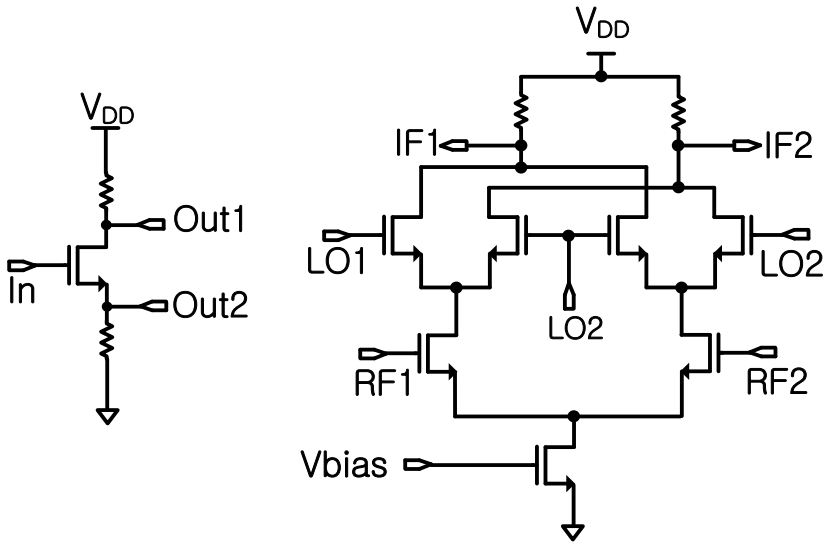


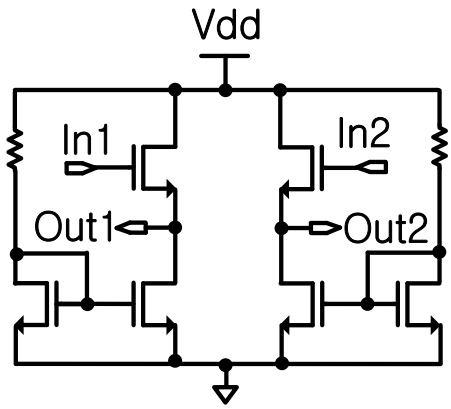
Fig. 5.5. Circuit Topology of (a) Active Splitter (b) Inverter Chain.



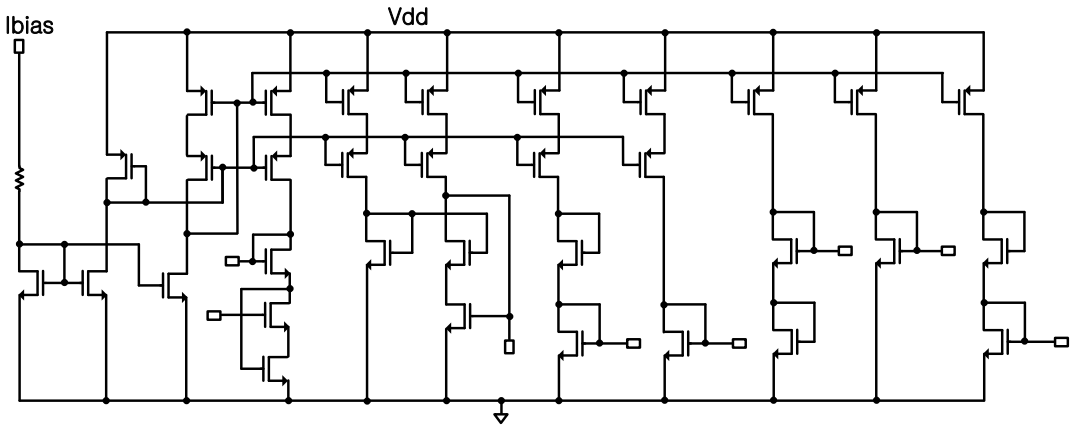
(a) (b)

Fig. 5.6. Circuit Topology of (a) Active Balun (b) Gilbert Cell Mixer.

Since the output of the inverter chain is single-ended, an active balun, shown in Fig. 6(a), is used to generate differential signals for driving the mixer LO port. A Gilbert mixer is designed for the BIST measurement circuitry, as shown in Fig.5 6 (b). The mixer operates in the linear region because harmonics due to nonlinearity generate extra DC components, which would degrade the accuracy of the proposed method. The mixer generally operates in the linear region when the amplitude of the input signal of the mixer is sufficiently small. Therefore, a resistive attenuator is introduced between the mixer and the switch.



(a)



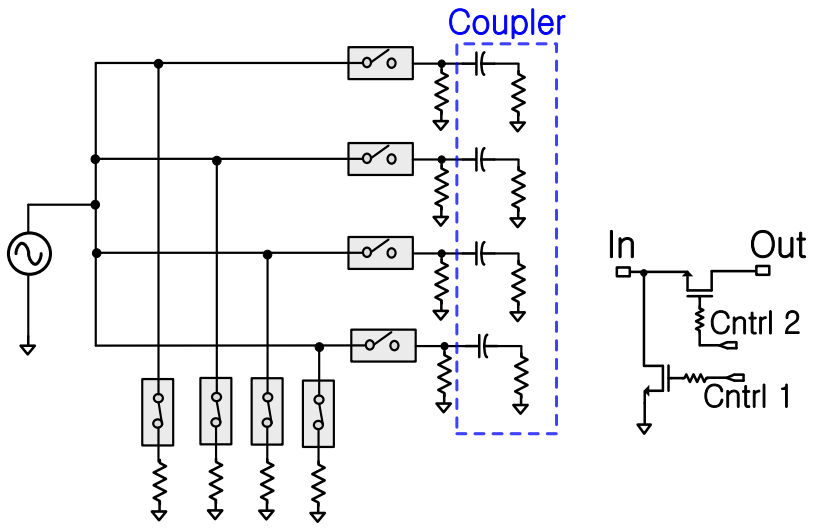
(b)

Fig. 5.7. Circuit Topology of (a) Source Follower (b) Biasing Circuits.

Finally, a buffer as shown in Fig. 5.7 (a) is designed and added at the IF output of the mixer. Finally biasing circuit is designed in order to provide proper bias voltages to each sub circuits in BIST measurement system. Fig. 5.7 (b) shows topology of biasing circuits. The biasing circuits generate multiple bias voltages and they are used to operate the splitter, balun, Gilbert cell mixer, and source follower.

5.3.2 Design of BIST input

It is noted that BIST circuit should not affect performance of the phased array during a normal mode while it should determine gain and phase mismatch accurately during the test mode. In order to satisfy the requirement, simple BIST input circuit is designed in this chapter. In the proposed design coupler, RF switch, and 50 ohm resistors are used. In order to keep same amplitude of test signal at the input of the phased array during the test mode, load impedance of the BIST test signal source should be same regardless of status of RF switches. Hence, parallel switch is added along with 50 ohm to each path of the phased array. When BIST test signal is applied to one or two paths of the phased array, other paths should be terminated to 50 ohm through parallel switch. Therefore, output impedance of BIST test signal source is always same for any kind of switch combination during test mode. Finally, capacitive coupler can be used in order to inject small part of the test signal to each path of the phased array. The capacitive coupler is simple and it does not affect performance of the phased array during the normal mode. Fig. 5.8(a) shows BIST input circuit which includes equivalent circuit of the capacitive coupler and Fig. 8(b) shows topology of single-pole single-throw (SPST) RF switch used in BIST input circuits.



(a) (b)

Fig. 5.8. Circuit Topology of (a) BIST Input Circuits (b) SPST RF switch.

5.4 Experimental Results

The proposed BIST system is evaluated using both simulations and off-the-shelf components. Simulations are used to show that the proposed technique is robust with respect to process variations, and the hardware experiments are used to demonstrate that the technique can be employed in a practical environment.

5.4.1 Simulation Results

Extensive simulations with process variations are conducted for the designed circuits. The proposed technique is divided into four sequences. Fig. 5.9 shows the BIST output waveform during each sequence. During the first and second sequences (Phase I), the BIST circuit compensation parameters are determined using two different test signal amplitudes. Third and fourth sequences (Phase II) show the DUT measurements. Table 5.1 summarizes the BIST DC output voltages for each sequence and computed gain based on the measured DC values. In Table 5.2 computed amplitudes of the DUT using the BIST circuitry are within 2% of the actual amplitudes obtained from the simulator, which shows high accuracy.

Table 5.1. BIST Parameter Computation for Phased Array from Simulation

Parameter	Value
DC output with Cal1(M1)	414 mV
DC output with Cal1(M2)	418.1 mV
DC output with Meas1(M3)	448.9 mV
DC output with Meas1(M4)	462.9 mV/V
Computed Gain (dB)	10.7 dB

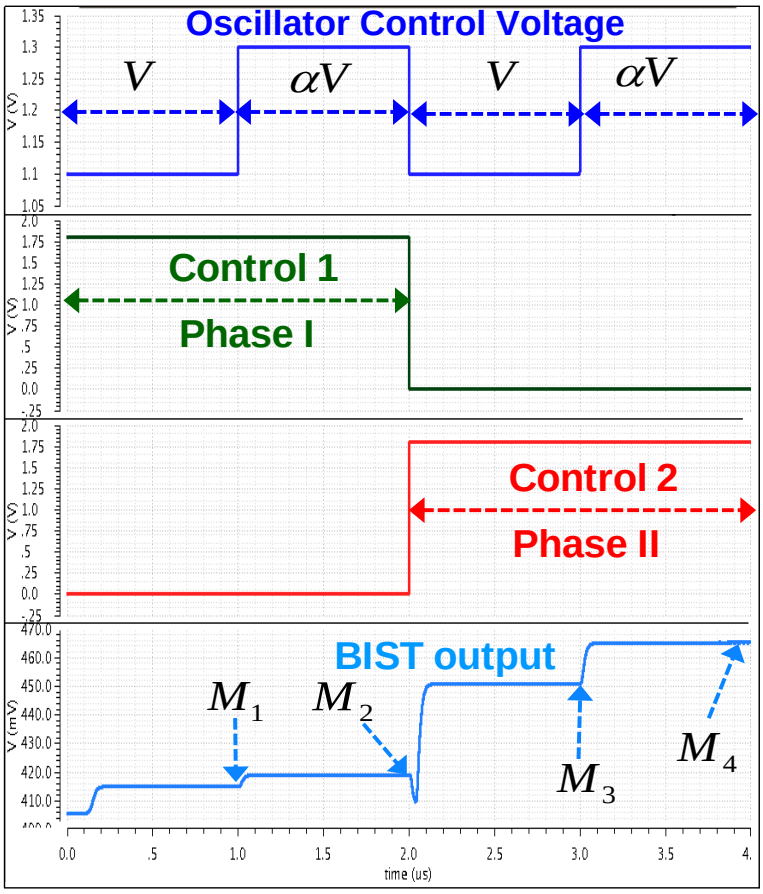


Fig. 5.9. Transient Analysis in Cadence Simulation.

Table 5.2. Gain Computation from Simulation Results

Case	**DUT Gain (dB)**		**Error (dB)**
	Computed	Actual	
1	6.9	6.9	0.0
2	10.7	10.8	0.1
3	13.7	13.7	0.0

The available process design kit is used for Monte-Carlo simulations. The oscillator output amplitude and the gain of the BIST system vary more than 20%. However, the self-compensation phase (Phase I) eliminates all error except for error from component matching values (which are within 0.1% error) such as line mismatch in traces and switch paths. From a 100-sample Monte-Carlo run, the RMS error in predicting the DUT amplitude is 1.6%, as shown in Table 5.3.

Table 5.3. Monte-Carlo Simulation Results for Gain Measurement

Actual	**Computed**	**RMS Error**
10.5 dBm	10.6 dBm	1.6 %

Monte-Carlo simulation is also conducted for the proposed BIST input circuits in order to verify functionality. Amplitude of BIST test signal is different for each sample during Monte-Carlo simulation due to process variation. However, amplitude of the test signal is same during Phase I and Phase II in each sample. Again, absolute amplitude of the test signal is not required with the proposed technique. Only requirement is that amplitude of the input signal should be same during test mode. Luckily, this requirement can be easily

satisfied since component mismatch within same die is very small. Therefore the proposed technique is still accurate.

In order to investigate how on-chip BIST input circuit affects the accuracy of the proposed technique, the error in input amplitude of the worst case was taken from Monte-Carlo simulation and substituted it into Eqn. (5.11), Eqn. (5.12) and Eqn. (5.18) for phase mismatch computation. The computed values from the worst case are compared with actual values and shown in Table 5.4. As these results show, even with the worst-case delay difference estimation, the phase imbalance can be determined within 1^{o} error. These error numbers are well within target values for polar transceiver calibration.

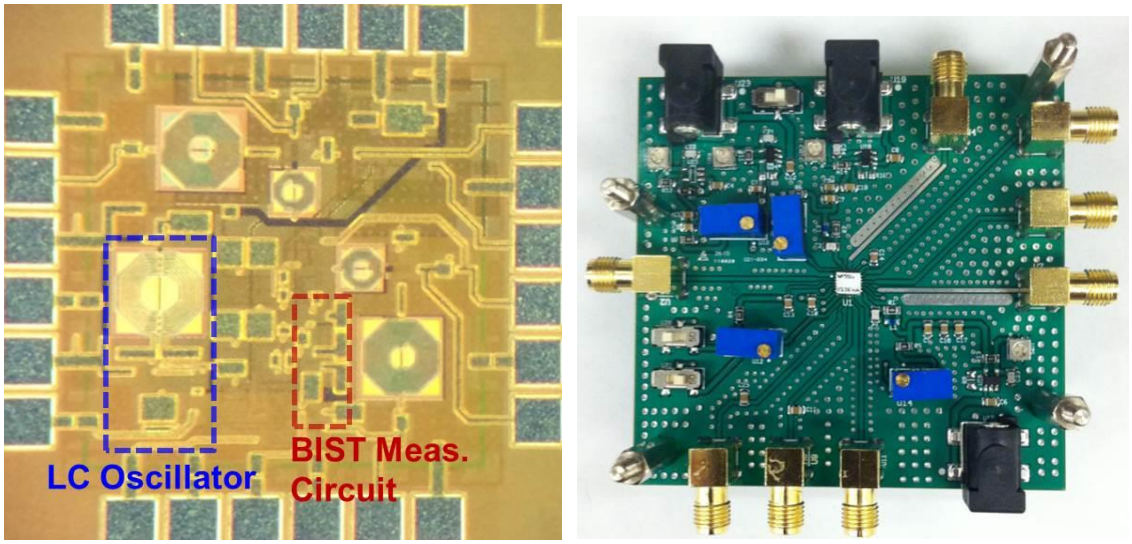
Table 5.4. Monte-Carlo simulation Results for Phase Mismatch Computation

Parameter	**Traditional**	**Proposed**	**Worst Case**
Phase MM	54.1°	54.2°	54.3°

5.4.2 BIST system design

BIST system is designed and fabricated using 0.18 μm IBM_7RF process. Fig. 5.10 (a) shows chip microphotograph. Since the chip is packaged, evaluation PCB is also designed in order to measure the chip performance. Fig. 5.10 (b) shows the evaluation PCB for the proposed BIST system. The proposed technique requires two test signals that have different amplitude although absolute amplitude or ratio of two signals don't need to be known. Two different amplitudes can be generated by changing gate bias voltage of tail transistor in LC oscillator. Hence, two different amplitudes are generated by adjusting variable resistor which is implemented on evaluation PCB. BIST measurement circuit

requires only one supply voltage and biasing circuit which is implemented on-chip provides multiple bias voltages inside the chip



(a) (b)

Fig. 5.10. BIST system (a) Chip Microphotograph (b) Evaluation PCB.

5.4.3 RF Phased Array PCB Design

For measurement verification, prototype phased array test board was designed and fabricated. The phased array is designed to work at 1GHz. The prototype phased array PCB, shown in Fig. 5.11, includes four elements, each consisting of a phase shifter (Hittite Microwave HMC934LP5E) and an RF variable gain amplifier (RFMD RF 2172). All elements are combined using a power combiner (Mini-Circuit SCN-2-11). For the BIST path, the output of the phased array is connected to the RF mixer (Hittite Microwave HMC483MS8G).

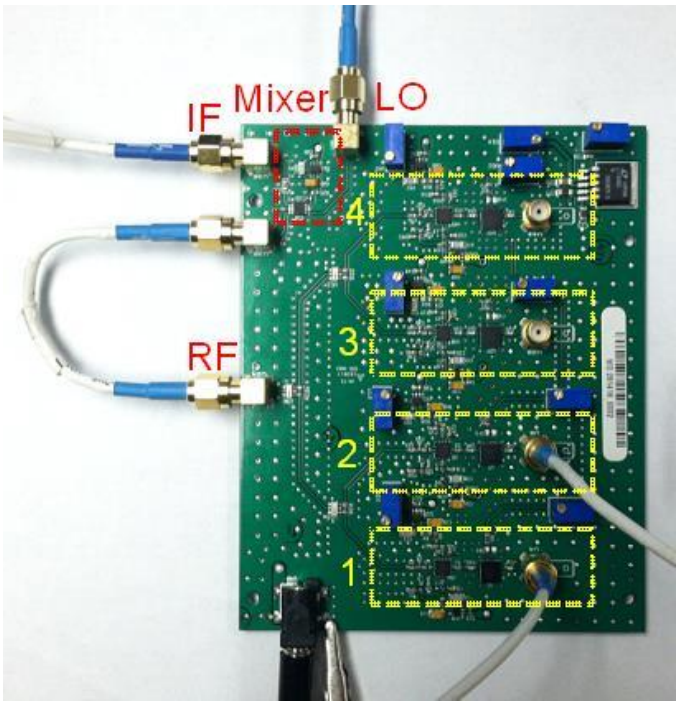


Fig. 5.11. RF Phased Array PCB.

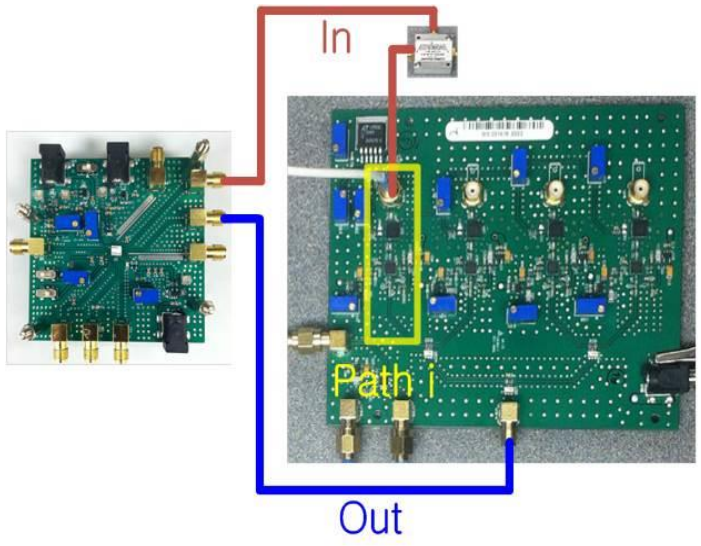
The IF port of the mixer is connected to the low pass filter (LPF) to eliminate high frequency components of the IF port signal. The control voltages of the VGAs and the phase shifters are adjusted using an adjustable low dropout (LDO) regulator (Micrel MIC5219). The LDO is adjustable from 0V to 10V (Linear Technology LT3083EQ) and allows for phase shifter phase control from 0° to 360°. The PCB includes 4 layers, where the inner layers are used as ground planes for improved DC to RF isolation. All RF lines are sized for 50 ohm characteristic impedance.

5.4.4 Hardware Measurement Test Setup

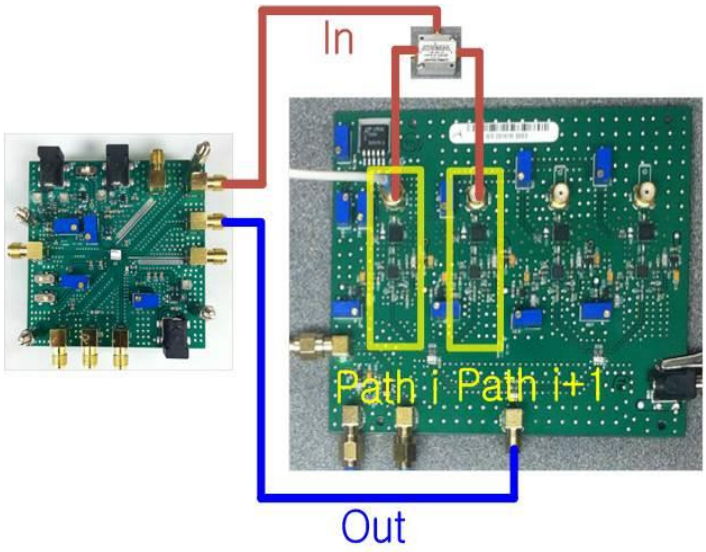
The proposed technique consists of three phases (Phase I, Phase II, and Phase III). During Phase I, only evaluation PCB for the BIST chip is used since the chip includes BIST test signal source as well as BIST test circuitry. The input signal is divided into two paths through the RF splitter. The divided signals are connected to the BIST mixer's RF and LO

ports. Since the low pass filter (LPF) at the IF port of the mixer eliminates high frequency components, only DC values are measured at the output of the BIST measurement circuit. For the experiment, the DC values are measured using an oscilloscope and the internal parameter of the BIST circuit is computed using the derived equations.

During Phases II and III, the PCB with BIST chip is connected RF phased array PCB in order to determine gain and phase differences. BIST test signal implemented on-chip is applied to the input of RF phased array PCB and the output of the phased array is connected to the input of the BIST measurement circuit located inside the chip. Fig. 5.12(a) shows the test setup for gain measurement, whereas Fig. 5.12(b) shows setup for phase difference measurement. Table 5.5 summarizes measured DC values and computed gain of each path (G_{path}), and Table 5.6 summarizes measurement results for combined gain of the phased array (G_{comb}) as well as the computed phase differences. It should be noted that any gain mismatch between the paths reflects as mismatch in G_{comb}, and hence can be measured with the proposed technique.



(a)



(b)

Fig. 5.12. Test set-up (a) Gain Measurement (c) Phase Difference Measurement.

Table 5.5. DC Output during Phase I and Phase II

Path	M1(mV)	M2(mV)	M3(mV)	M4(mV)	G_{path}
1	164.3	172.5	168.3	184.1	1.9
2	164.3	172.5	168.2	182.8	1.8
3	164.3	172.5	168.5	184	1.9
4	164.3	172.5	168.6	184.2	1.9

Table 5.6. DC Output during Phase III and Computation of Phase Difference

Path	M5(mV)	M6(mV)	G_{comb}	Phase Difference
1-2	176.3	203.4	3.3	53.9°
2-3	182	208.9	3.3	54.2°
3-4	181.3	209	3.4	54.1°

Fig. 5.13 shows the measurement setup for the proposed technique to characterize the phased array. CMOS LC oscillator is used to generate the BIST test signal and RF output of the phased array is down-converted to the baseband through CMOS Gilbert cell mixer. The frequency of the down-converted IF signal is DC signal. For the experiment, the baseband output is measured and captured using an oscilloscope. The baseband digital signal processing (DSP) unit can also be emulated using MATLAB.

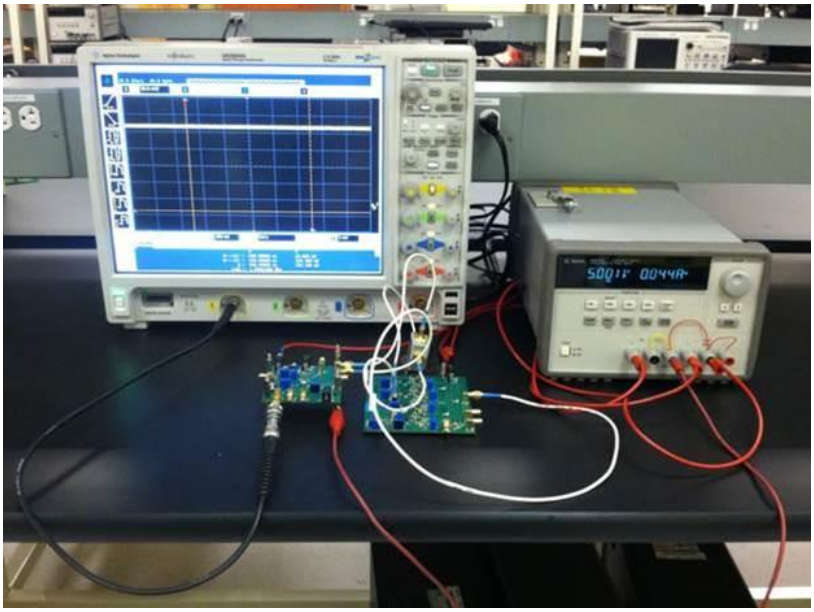


Fig. 5.13. Test Set-up for the Proposed Phased Array BIST Technique.

In order to verify the accuracy of the proposed technique, the phase in time domain was measured with a traditional method, which serves as the baseline measurement. Fig. 5.14 shows the traditional measurement setup to establish the baseline. The RF input is divided into two paths through an RF splitter. One of the splitter outputs is applied to the input of the element in the phased array and the other output is directly connected to the oscilloscope through the reference cable. Then, the RF output of the phased array and the RF output of the waveform connected through the reference cable are simultaneously measured in the time domain using the oscilloscope. Fig. 5.15 shows measured phase difference between paths in the phased array.

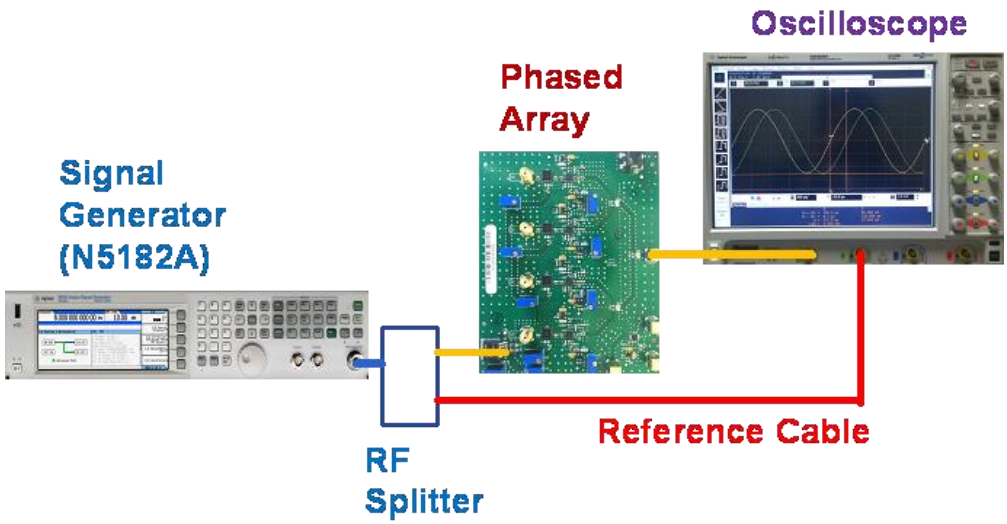


Fig. 5.14. Test Set-up for the Traditional Phase Mismatch Measurement.

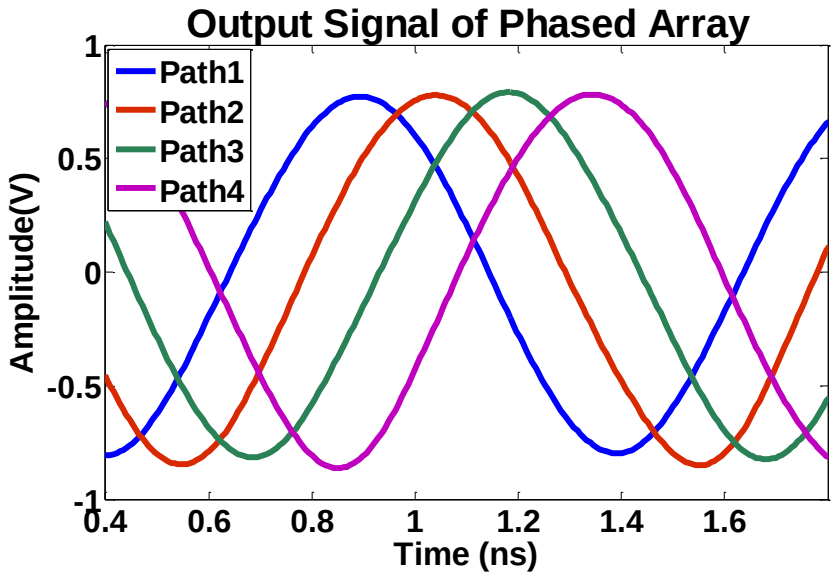


Fig. 5.15. Output Signal of each Path during Verification.

By measuring time difference between the two waveforms, an actual phase difference between elements in the phased array can be directly measured. The reference cable is kept in place, while the input is connected to each path, one at time, eliminating any unknowns in the measurement path. The proposed BIST system also was connected to another RF

phased array PCB which has different phase difference and the estimated phase difference was compared with actual phase difference.

Four evaluation PCBs for BIST chip were manufactured and phase difference of two different phased array boards was estimated with each evaluation PCB. And Table 5.6 shows comparison between estimated phase difference and phase difference from baseline method. As shown in Table 5.7, the proposed BIST system can accurately determine phase difference for different BIST chips within 1% of the traditional method.

Lastly, resolution analysis also was conducted. In the original experiments, an 8-bit ADC is used with averaging to capture the response of the circuit. In addition, further experiments was conducted with a 6-bit ADC resolution and averaging. The results of these additional experiments are shown in Table 5.8. In Table 5.7, a small degradation in the accuracy for phase mismatch computation is observed from 8-bits to 6-bits. However, this degradation is not significant enough to cause any problems with digital calibration.

Table 5.7. Phase Difference Estimation for Different Arrays

Array Board	BIST Board	Phase Difference	Proposed Method	Baseline Method	Error
1	1	**1-2**	53.9°	54°	0. 1°
		2-3	54.2°	54.1°	0.1°
		3-4	54.1°	54°	0.1°
	2	**1-2**	53.9°	54°	0. 2°
		2-3	54.2°	54.1°	0.1°
		3-4	54.2°	54°	0.2°
	3	**1-2**	54.1°	54°	0.1°
		2-3	53.9°	54.1°	0.2°
		3-4	53.8°	54°	0. 2°
	4	**1-2**	54.2°	54°	0. 2°
		2-3	54.1°	54.1°	0°
		3-4	53.8°	54°	0. 2°
2	1	**1-2**	36°	36°	0°
		2-3	35.9°	36.1°	0.2°
		3-4	35.9°	36.2°	0.3°
	2	**1-2**	35.8°	36°	0.2°
		2-3	36°	36.1°	0.1°
		3-4	36.4°	36.2°	0.2°

	3	**1-2**	36. 1°	36°	0. 1°
		2-3	35.8°	36.1°	0.3°
		3-4	36.2°	36.2°	0°
	4	**1-2**	36. 3°	36°	0.3°
		2-3	36°	36.1°	0.1°
		3-4	36.1°	36.2°	0.1°

Table 5.8. Resolution Analysis with Different Number of Bits

Phase Difference	**Proposed Method**		**Baseline Method**
	8 Bit	**6 Bit**	
1-2	53.9°	54.5°	54°
2-3	54.2°	54.5°	54.1°
3-4	54.1°	54.5°	54°

5.4.5 Test Time and Hardware Overhead

The proposed technique requires four steps. (1) BIST output measurements after applying two test signals with different amplitude to the BIST input (2 measurements), (2) calculation of the BIST system's internal parameters, (3) measurement of the phased array using the BIST system, and (4) calculation of gain and phase difference. Steps (1) and (2) require DC measurements (50-100ms each), and Steps (3) and (4) require simple mathematical manipulations. With the control sequences and 3 measurements, an IC-based test time is estimated within 500ms.

The proposed BIST circuits have been implemented using 0.18μm IBM 7RF process to verify functionality. Table 5.9 details the area estimates for the various circuit building blocks of the BIST circuit. Table 5.8 also includes the area estimate of an RF front-end phased array built with a similar technology for comparison purposes [4, 6]. The area overhead of the proposed technique is less than 1.1%.

5.5 Conclusion

In this chapter, a new BIST solution for RF phased arrays is proposed. The phase of each element in the phased array is the most important parameter for performance. Previous techniques for the characterization and calibration of the phase within a phased array require expensive RF equipment such as a network analyzer or coherently synchronized signal generators and analyzers. These solutions are not suitable for low cost testing or for in-field calibration. The proposed technique consists of three phases: BIST compensation, gain measurement, and phase mismatch measurement. The major advantage of the proposed technique is that it requires no knowledge of the exact amplitudes generated by the BIST system, nor does it require that their ratios be known. Hence, a simple amplitude control in the oscillator enables generation of all necessary BIST signals. The measured BIST output is in the DC domain, which is easy to convert to the digital domain using an existing ADC in the system. Simulation results and hardware measurements show that the proposed BIST solution determines the phase mismatch to within 1° error.

Table 5.9. Area Overhead Estimate with IBM 7RF process

Circuit	**Area (mm^2)**
Oscillator	0.088
Switches	0.0028
Mixer	0.0054
Filter	0.002
Active Splitter	0.0025
Active Balun	0.0004
Total Area (BIST)	0.11
Eight element RF phased array [28,34]	11.55
%Overhead	0.95%

CHAPTER 6

PROCESS INDEPENDENT GAIN MEASUREMENT WITH LOW OVERHEAD VIA BIST/DUT CO-DESIGN

In this chapter, a BIST solution that is robust with respect to process variations and introduces low area overhead is proposed to determine the gain of an RF DUT. The gain measurement method is similar to the method in [18] with the concept of setting up relative measurements to remove the effect of process variations. Due to the need to use weaker signals, particularly for receivers, directional couplers cannot be relied on, as in [17], which introduce negligible insertion loss and parasitic capacitance. In this chapter, RF switches are used to direct the signal flow, which inevitably introduce higher parasitics. A method for co-designing the BIST circuit together with the DUT is presented to significantly reduce the impact of the BIST circuit on the DUT performance. It is shown that by including the BIST circuit during the design process, performance degradation can be avoided. Two LNAs with the same specification are implemented, one with BIST and one without. These devices are manufactured on the same die and measurements show that (a) the BIST circuit is capable of accurate gain measurements despite high variations in its parameters, and (b) there is also no performance difference between the two LNAs. .

6.1 BIST Circuit and Methodology

The BIST system consists of a signal generator, a measurement circuit, and switches and traces to direct the signal flow. Fig. 6.1 shows how a DUT is modified (the DUT in Fig. 6.1 is an LNA; the bias network is not shown) to include the BIST circuit. There are three configurations. The first configuration is the BIST loop, where the BIST signal source is connected to the measurement system. The second configuration is the BIST/DUT loop,

where the test signal source drives the input of the DUT, and the output of the DUT drives the measurement system. The third configuration is the normal operation mode, where the DUT input and output are connected to functional input and output nodes and the BIST circuits are turned off to save power. One of the important considerations for BIST/DUT co-design is that BIST circuit should not affect LNA in terms of performance during the normal operation mode. In Fig. 6.1, when both RF switches (SW1 and SW2) are not connected to LNA, impedances looking into the RF switches (Z1 and Z2) must be sufficiently high at the operating frequency in order to avoid signal loss. In other words, the RF switches should have sufficient isolation. Another important consideration is that input impedance of BIST measurement circuits during test mode should be matched with output impedance of the LNA during normal mode in order to ensure measurement accuracy.

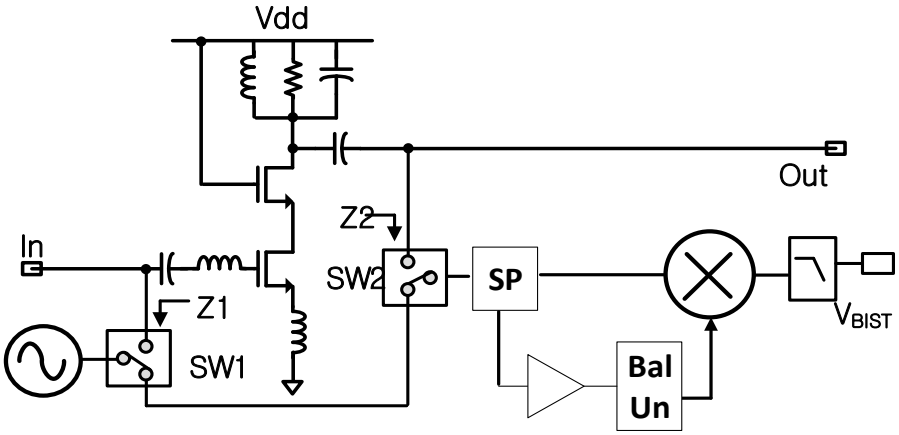


Fig. 6.1. BIST System with an LNA as the DUT.

A simple LC oscillator is used as BIST test signal source. The amplitude of this signal is not known and not well-controlled by the process. This BIST test signal is applied either to the input of the BIST measurement circuit or to the input of the LNA via an RF switch. On the measurement side, the self-mixing technique is used. The BIST test signals are

generated by the same LC oscillator, with the same amplitudes. It is noted that absolute amplitude or ratio of two different amplitudes do not need to be known for gain measurement. The gain of the LNA can be measured by simply measuring DC BIST output.

The BIST measurement circuitry consists of a mixer and low pass filter (LPF). The BIST test signal is applied to the input of the BIST measurement system and this signal is divided into two paths through the splitter before the input of the mixer. The two identical signals are applied to the RF and LO ports of the mixer. Because the RF and LO signals have the same frequency, the IF output of the mixer generates a DC component as well as high frequency component. The LPF eliminates the high frequency component. The DC value at the output of the BIST measurement circuit is used to determine the DUT gain. The proposed BIST architecture and circuit implementations in this chapter is similar to that of [18]. Major differences are in signal flow components where switches are used to be able to drive/sense a generic DUT with stronger signals and better sensitivity is provided. These circuit implementation issues are explained in the next section. The mathematical model for the BIST measurements is identical to [18]. Hence, the model derivation is skipped in this chapter but the results are summarized so as to explain the BIST/DUT co-design methodology better.

For the two amplitudes and two switch configurations, there are 4 distinct DC measurements as the switches work in phase to generate 2 configurations instead of 4. The first two measurements, M_1 and M_2, are conducted when the test signal source is directly connected to the measurement circuit. By using two different amplitudes and taking the difference of measurements, DC offsets are eliminated but the amplitudes and BIST gain remain unknown. The next two measurements, M3 and M4 are taken when the BIST signal

source is connected to the DUT input and the DUT output is connected to the measurement circuit. Again, taking the difference of two measurements eliminates the DC offset. While the two amplitudes and the BIST gain are still unknown, the ratio between these two sets of measurements yields the DUT gain. Note that here, BIST gain, DC offsets, or signal amplitudes are not determined. They are simply remove from the equations. Eqns. (6.1)-(6.7) summarize the derivation of process independent gain measurement, as it has been introduced in Chapter 5. Here, G_{BIST} is the gain of the BIST measurement circuit, G_{SW} is the total insertion loss of the switches, and *A1 and A2* are input signal amplitudes, G_{DUT} is the DUT gain.

$$M_1 = A_1 G_{SW} G_{BIST} + DC_{Meas} \tag{6.1}$$

$$M_2 = A_2 G_{SW} G_{BIST} + DC_{Meas} \tag{6.2}$$

$$M_2 - M_1 = (A_2 - A_1) G_{SW} G_{BIST} \tag{6.3}$$

$$M_3 = A_1 G_{DUT} G_{SW} G_{BIST} + DC_{Meas} \tag{6.4}$$

$$M_4 = A_2 G_{DUT} G_{SW} G_{BIST} + DC_{Meas} \tag{6.5}$$

$$M_4 - M_3 = (A_2 - A_1) G_{LNA} G_{SW} G_{BIST} \tag{6.6}$$

$$G_{DUT} = (M_4 - M_3)/(M_2 - M_1) \tag{6.7}$$

For the BIST method to deliver accurate results, it is imperative that the two signal amplitudes (A_1 and A_2) are consistent throughout the entire operation. This is achieved by (a) using an LC-coupled oscillator that is less sensitive to matching in terms of amplitude, (b) using high isolation switches that limit signal feed-through and keep the amplitude stable, and (c) matching input and output impedances of the BIST and the DUT paths.

6.2 BIST/DUT Co-Design

For the BIST method to deliver accurate results, it is imperative that the two signal amplitudes (A1 and A2) are consistent throughout the entire operation. This is achieved by (a) using an LC-coupled oscillator that is less sensitive to matching in terms of amplitude, (b) using high isolation switches that limit signal feed-through and keep the amplitude stable, and (c) matching input and output impedances of the BIST and the DUT paths.

6.2.1 Design Methodology

Fig. 6.2 shows the BIST/DUT co-design methodology. First, the DUT and the BIST circuit architectures are determined. The DUT is designed including the BIST switches and signal traces with respect to its specifications. In this step, the goal for the BIST design is to use maximum isolation for the switches to eliminate signal feedthrough from the BIST signal generator to the BIST measurement circuit and to avoid loading the DUT during normal operation mode. The DUT design flow is unaffected with the exception of the switches which now become a part of the functional circuit.

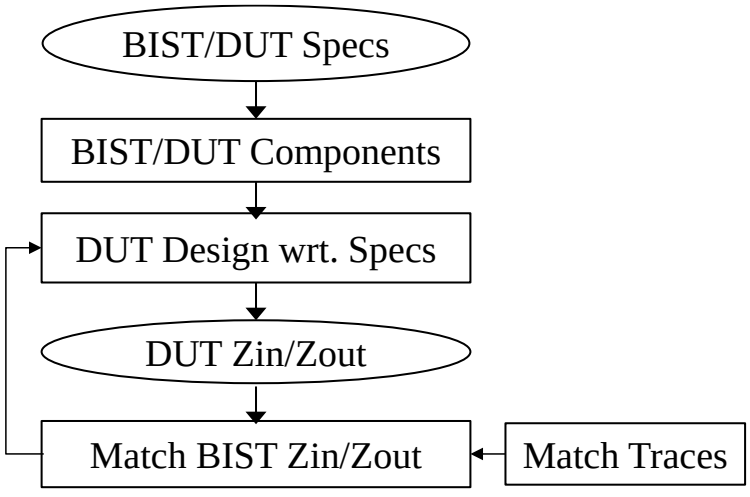


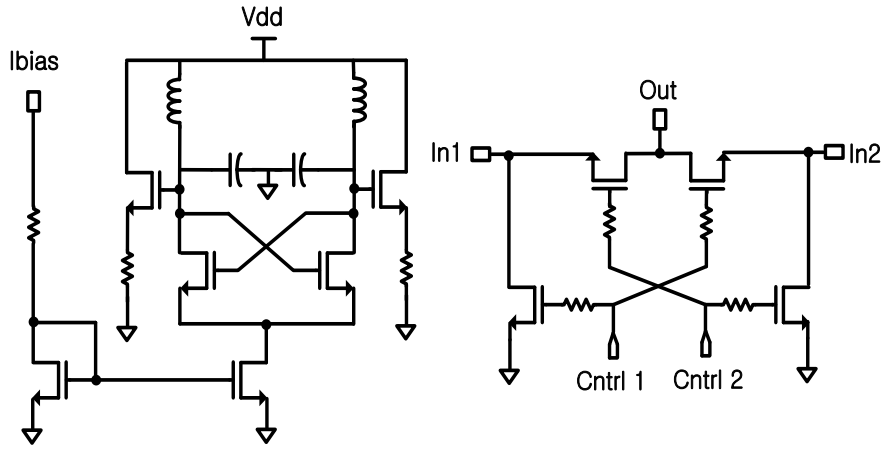
Fig. 6.2. BIST/DUT Co-Design Flow.

The next step is to match the BIST impedances with the DUT impedances at the input and at the output. Note that here within-die variation for passive components is 0.1% as opposed to much higher within-die variation for active devices 1-2%. As a result, passive matching (R-to-R, C-to-C, and L-to-L) is much more accurate compared to active matching, which constitutes the basic design principle for switched capacitor circuits. In order to accomplish the BIST/DUT matching, the switches may need to be altered in terms of resistance and transistor sizes. At this time, it is also important to match the signal traces to eliminate any mismatch in losses. If there is any alteration to the switch network, the DUT design is tweaked to ensure that specifications are guaranteed. This design flow introduces no changes to the DUT flow and the BIST design is straightforward if the three abovementioned principles are followed.

6.2.2 Circuit Implementation

The proposed BIST system has been designed using 0.18 μm IBM_7RF process with nominal power supply of 1.8V. We have implemented the test signal source with LC oscillator shown in Fig. 6.3(a) with oscillation frequency of 1 GHz. The amplitude of the signal is controlled via the control input (I_{bias}). Note that the LC oscillator is in an open-loop, which would make its frequency vary with respect to process variations. However, this does not cause an issue on the measurement side. Thanks to self-mixing, the output is always DC. The BIST method requires two input signals which have different amplitudes. However, the exact relation between them does not need to be known. This relaxation greatly simplifies the BIST design, as the exact value of the control signal and the output signal amplitudes do not need to be determined. Figure 3(b) shows the switch circuit topology, which provides the port-to-port isolation that is necessary to limit performance

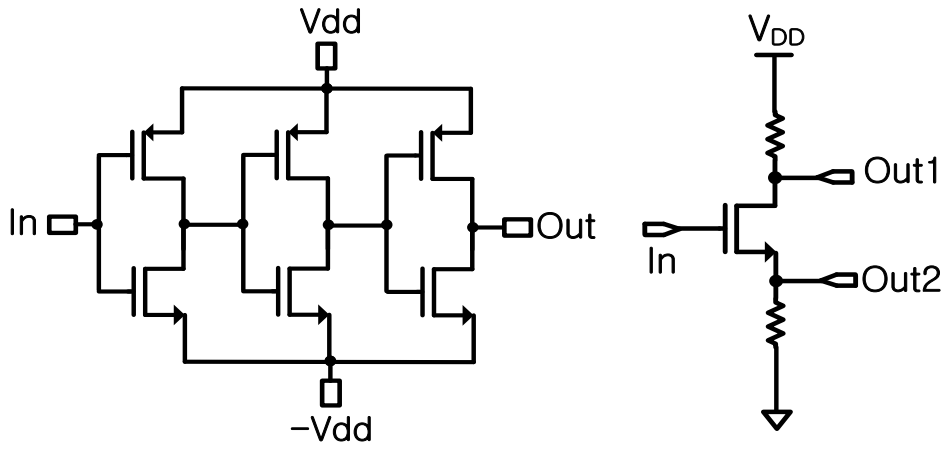
degradation. The BIST measurement circuit consists of a splitter, inverter chain, balun, and Gilbert cell mixer.



(a) (b)

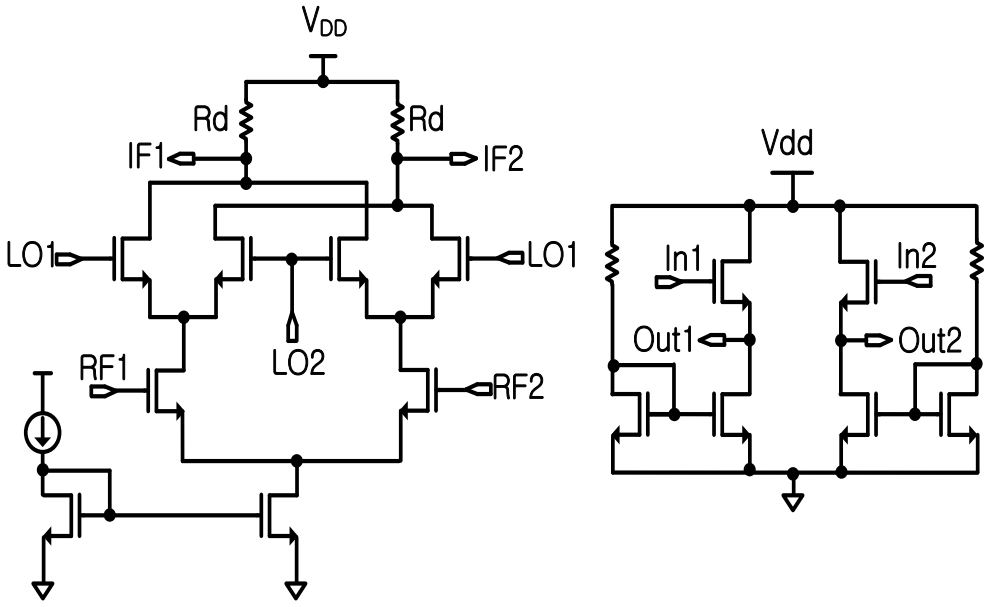
Fig. 6.3. Circuit Topology of (a) LC oscillator (b) RF switch.

An important constraint is to maintain the LO amplitude regardless of whether the BIST signal source or the LNA is driving the mixer to ensure that the BIST gain remains identical which Equation (7) relies on. Therefore, an RF inverter chain shown in Fig. 6.4(a) is used to generate a constant amplitude LO signal. Since the output of the inverter chain is single-ended, an active Balun, shown in Fig. 6.4(b), is used to convert single ended signal to differential signals for driving the mixer LO port. A Gilbert cell mixer is designed for the BIST measurement circuitry, as shown in Fig. 6.5(a). A resistive attenuator is used at the RF input of the mixer to suppress non-linearity. Finally, a buffer as shown in Fig. 6.5(b) is designed and added at the IF output of the mixer.



(a) (b)

Fig. 6.4. (a) Inverter Chain (b)Active Balun.



(a) (b)

Fig. 6.5. (a) Gilbert Cell Mixer (b) Source Follower.

6.3 Experimental Results

The proposed BIST/DUT co-design method is evaluated using both simulations and hardware measurement with a fabricated chip. Table 6.1 shows the specifications of the LNA circuit. These performance specifications are similar to LNA designs at the same

frequency with the same technology from the literature [24,25]. Co-design approach outlined in Section III is followed. The experiments are aimed at validating that the proposed technique is robust with respect to process variations, and the inclusion of the BIST circuit does not adversely affect the DUT performance.

Table 6.1. LNA Specifications

S21	> 9 dB
S11	< -10 dB
S22	< -10 dB
NF	< 2.5 dB
Id	< 10 mA

6.3.1 Simulation Results

Available process design kit has been used for Monte-Carlo simulations with 200 samples. Both the stand-alone LNA and the LNA with BIST satisfy all specifications outlined in Table 6.1. Due to process variations, it is observed that there is 1.3dB variation in the LNA gain, 4dB variation in S11, 2dB variation in S22, 0.5dB variation in Noise Figure. This is true for both LNAs. More importantly, we have compared the performance of the stand-alone LNA with the performance of the LNA with BIST. The worst case performance difference between the two LNAs for all Monte Carlo samples is given in Table 6.2. For the most part, the two LNAs have identical performance. The biggest performance difference is observed in S22, which is much smaller compared with variations due to process. These results show that the performances of the two LNAs are virtually identical.

Table 6.2. LNA Simulation Results

Difference between Standalone LNA and LNA with BIST (dB) @ 960 MHz			
ΔS21	**ΔS11**	**ΔS22**	**ΔNF**
0.06	0.18	0.48	0.06

Fig. 6.6 shows the histogram of the Monte-Carlo simulation results on LNA performance. Solid lines show the performance histogram for the LNA with BIST and the dashed lines show the performance histogram of the stand-alone LNA. The histograms are almost identical, which confirms that the BIST loading does not degrade LNA performance. In the design of the two LNAs, there are slight differences in the capacitances (~50fF) and inductances (~100pH) to account for the BIST loading. Next, the accuracy of the BIST circuit is evaluated. The oscillator output amplitude and the gain of the BIST system vary more than 20%. However, thanks to relative measurements, this variation is not a problem for BIST measurement accuracy. From a 200-sample Monte-Carlo run, the RMS error in computing the DUT gain 0.1dB. This error includes both the errors in the measurement circuit and errors in the signal generator. In Section IV.C, this error analysis is repeated for the measurement side only to be able to compare with previously proposed techniques.

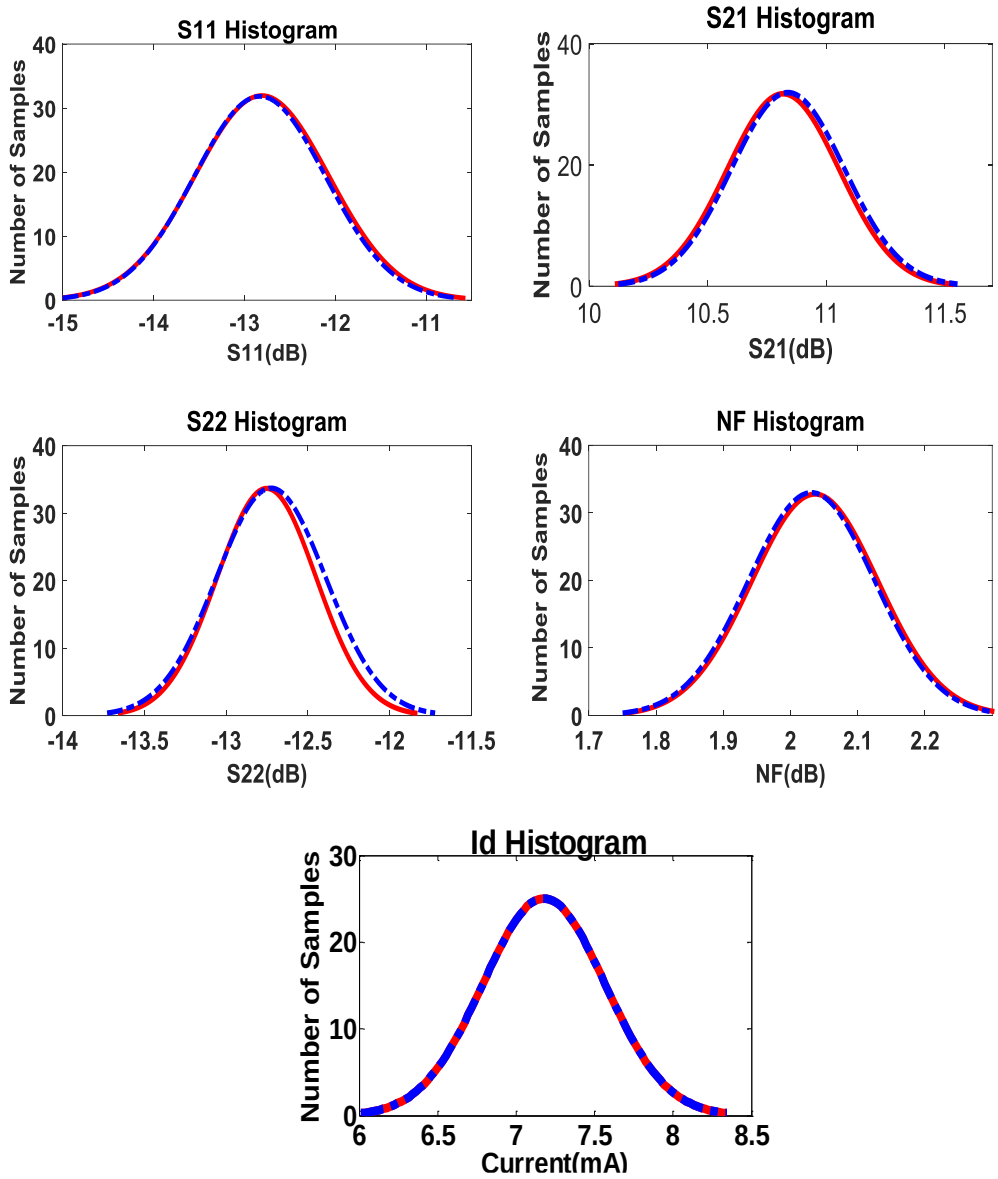


Fig. 6.6. Monte-Carlo Simulation Results (dashed line: stand-alone LNA, Solid line: LNA with BIST).

6.3.2 Hardware Measurement Results

For hardware demonstration, the BIST circuit is designed and fabricated using IBM 180nm process. Fig. 6.7(a) shows fabricated chip which includes standalone LNA as well as LNA with BIST. The chip size is 1.5mmX1.5mm. Fig. 6.7(b) shows the evaluation PCB.

Overall, 5 ICs were fabricated and placed on the PCB and they all have been measured both with the BIST technique and with traditional RF equipment.

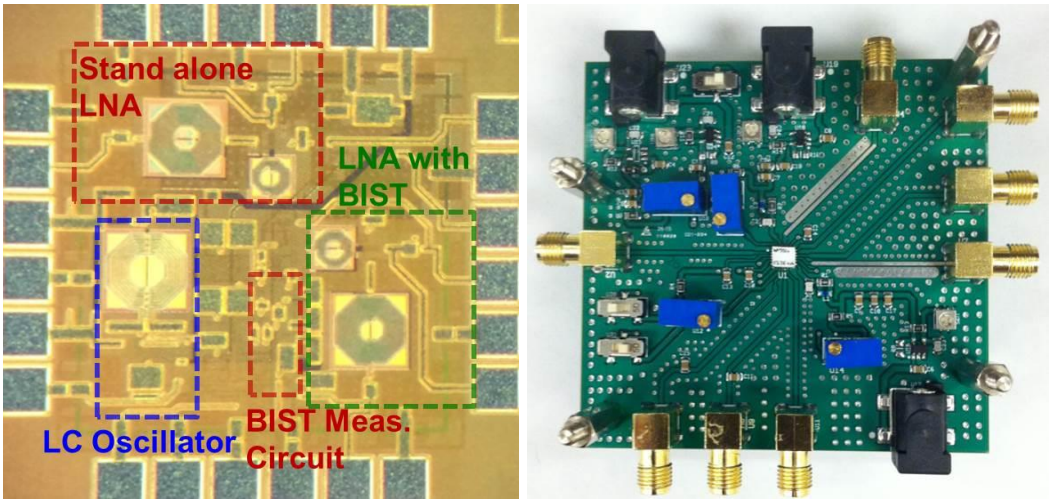
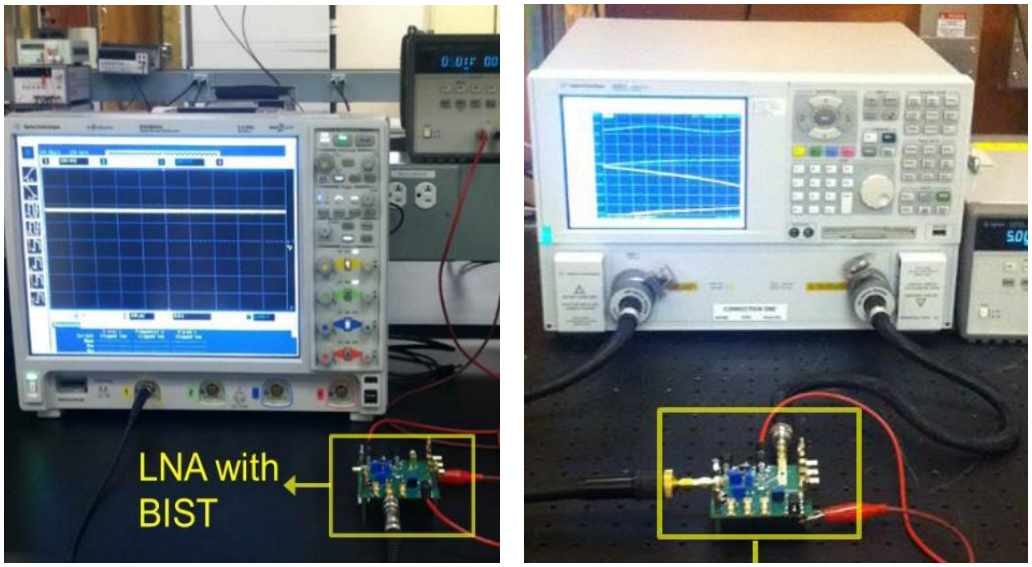


Fig. 6.7. BIST/DUT IC (a) fabricated chip with standalone LNA and LNA with BIST (b) Evaluation PCB for both LNAs.

The test setup for the BIST measurement is shown in Fig. 6.8(a) which only uses a sampling scope for DC measurements with a 9-bit resolution. Computation of Eqn. (6.7), which consists of two subtractions and one division is done manually. For verification of the BIST results, the traditional set-up of Fig. 6.8(b) is used, where S-parameters are measured using Network Analyzer (Agilent Technologies E8361A).



(a) (b)

Fig. 6.8. Measurement setup (a) with BIST output, which is DC, (b) for S-parameter measurement to compare the two LNAs.

To evaluate the effect of the BIST circuit in performance, the S-parameters of the stand-alone LNA is compared with that of the LNA with BIST. Table 6.3 shows the differences in S-parameters for the five ICs that were measured. The results confirm that the performances of the two LNAs are nearly identical. As a matter of fact, for one of the devices, the LNA with BIST has better gain. This is due to variations in the PCB traces and components. It is concluded that the inclusion of BIST does not adversely affect the performance.

Next, the accuracy of the BIST technique is evaluated. Measurement for all 5 boards is given in Table 6.4. Hardware experiments confirm that BIST yields very accurate gain measurements.

Table 6.3. Performance Comparison: Standalone LNA vs. LNA with BIST

Board Number	**Difference between Standalone LNA and LNA with BIST (dB) @ 960 MHz**		
	ΔS21	**ΔS11**	**ΔS22**
1	-0.06	0.55	0.01
2	0.05	0.54	0.05
3	-0.09	0.79	-0.49
4	-0.17	0.91	-0.57
5	-0.08	0.6	-0.5

Table 6.4. Accuracy Comparison: Proposed Technique vs. Traditional Method

Board Number	**Gain**		**Error**
	BIST	RF Equip.	
1	9.4 dB	9.5 dB	0.1 dB
2	9.3 dB	9.4 dB	0.1 dB
3	9.8 dB	9.7 dB	0.1 dB
4	9.7 dB	9.7 dB	0 dB
5	9.4 dB	9.6 dB	0.2 dB

6.3.3 Test Time and Hardware Overhead

The proposed technique requires four DC measurements. Thanks to on-chip control, the settling time for switches and the oscillator is less than 2μs, as determined by Monte-

Carlo simulations and by hardware experiments. With a 1MHz, 9-bit ADC, the output can be measured within 5μs, resulting in a total test time of 20μs. The computation time is negligible with two subtractions, and one division. Comparatively, and RF gain measurement with the ATE takes roughly 50ms since the ATE switch matrix and mechanical relays take considerably more time to settle.

Table 6.5 shows the area estimates for the various building blocks of the BIST circuit. Table 6.5 also shows the area estimate of an RF transceiver (RF front-end only) built with a similar technology for comparison purposes [19-21]. The area overhead of the proposed BIST system is less than 1.2% of the transceiver front-end. Note that the BIST circuit can be used for multiple blocks of the RF transceiver by adding more switches on the BIST side (not on the DUT side), which introduces negligible additional overhead (0.006mm^2 for each additional switch).

Table 6.5. Area Overhead Estimate with IBM 180 nm Process

Circuit	**Area (mm^2)**
Oscillator	0.1
Switches	0.006
Mixer	0.008
Filter	0.002
Total Area (BIST)	0.11
RF Transceiver [46-4]	9
%Overhead	1.2%

6.3.4 Comparison with Prior Work

Finally, the proposed BIST method is compared with similar techniques in the literature in terms of area and accuracy. For a fair comparison, the measurement side is only included as most of the prior approaches rely on an external RF stimulus generator. We repeat the experiments with an external source and use only the measurement side. Table VII shows this comparison. The work has slightly better accuracy compared with the best of prior work and similar area overhead on the measurement side. This chapter is the first to include an entire BIST system with the input signal generation and output sensing, with the switch network to avoid performance degradation for the DUT in the normal mode of operation, and to show that two identical

Table 6.5. Summary of Prior Work (Detector Only)

	Gain Error	**Area (mm^2)**
[12]	0.7 dB	0.06
[29]	0.7dB	0.04
[15]	0.06 dB	0.002
This Work	0.02 dB	0.01

6.4 Conclusion

In this chapter, a process-independent technique is proposed to measure the gain of an RF DUT using BIST/DUT co-design. The BIST system is implemented with a test signal source and a measurement system. The test signal source is designed using an LC oscillator and RF switches. The BIST measurement system consists of an RF mixer and low pass filter. By designing the BIST system as a sequence of relative measurements, the

parameters of the BIST circuit can be eliminated from the computations, ensuring robustness with respect to process variations. By using the proposed co-design methodology, the performance impact can be eliminated or minimized. The performance impact so far has been the major bottleneck in BIST adoption by RF IC designers.

CHAPTER 7

SUMMARY AND CONCLUSION

In this dissertation, BIST solutions for advanced RF transceivers are proposed and discussed in order to achieve low cost and low overhead with high accuracy.

Firstly, a BIST solution for RF polar transceivers is proposed to measure the internal parameters, namely gain and phase mismatches, delay skew between the envelope and phase signals, and the finite envelope BW. In order to solve for these parameters using baseband signal analysis, the transceiver is configured in the loop-back mode, the baseband output response of the receiver is observed, and the parameters are extracted using analytically derived equations. Special test signals are developed in the loop-back mode, which enable isolation of the effect of one parameter at a time. First, gain and phase mismatches in the receiver are determined from the measured DC values at the output of the receiver in the loop-back mode. Regarding the transmitter, the delay skew from the measured IMD3 at the output of the receiver is calculated by applying low BW two-tone signal. After compensating for the effect of delay skew, the envelope BW is measured by increasing the BW of two-tone input signal. From the second measurement of IMD3 in the loop-back mode, the finite envelope bandwidth can be estimated by comparing the measured IMD3 with a lookup table that consists of the calculated IMD3 values according to the number of harmonics included in the passband of the reconstruction filter. The loop-back path circuit is designed and verified for its functionality and performance. Based on simulation and hardware measurements, the proposed method determines the critical parameters accurately while eliminating the expensive RF equipment. In addition, the

proposed method enables implementation of BIST and internal calibration for the RF polar transceiver because with complexity, high accuracy, and short test time.

A process-robust technique to measure the output amplitude of an RF DUT using a BIST system is proposed. The BIST system is implemented with a test signal source and BIST measurement circuit. The test signal source is designed using an oscillator, an amplifier, and an RF limiter. The BIST measurement system consists of an RF mixer and low pass filter. The proposed technique consists of two phases: a BIST calibration phase and a DUT measurement phase. During the calibration phase, the internal parameters, such as gain and DC offset of the BIST circuit, are computed and calibrated using analytical equations. After calibration, the DUT is connected to the BIST system and the amplitude of the DUT is measured. The BIST system was designed and simulated in a CMOS 0.18μm IBM 7RF process to verify functionality. The BIST system was also implemented using off-the-shelf components for hardware experiments. Both the simulation and hardware experiments show that the proposed technique accurately determines the gain of an RF transmitter. The BIST system is capable of measuring RF amplitude within 0.1dB error, requires less than 500ms test time, and introduces approximately 0.1mm^2 area overhead.

A BIST solution for RF phased arrays is proposed and discussed. The phase of each element in the phased array is the most important parameter for performance. Previous techniques for the characterization and calibration of the phase within a phased array require expensive RF equipment such as a network analyzer or coherently synchronized signal generators and analyzers. These solutions are not suitable for low cost testing or for in-field calibration. The proposed technique consists of three phases: BIST compensation, gain measurement, and phase mismatch measurement. The major advantage of the

proposed technique is that it requires no knowledge of the exact amplitudes generated by the BIST system, nor does it require that their ratios be known. Hence, a simple amplitude control in the oscillator enables generation of all necessary BIST signals. The measured BIST output is in the DC domain, which is easy to convert to the digital domain using an existing ADC in the system. In addition, a BIST input circuit is designed and analyzed. BIST system is fabricated using IBM 180 nm process and simulation results and hardware results show that the proposed BIST solution determines the phase mismatch to within 1° error

A process-independent technique to measure the gain of an RF DUT using BIST/DUT co-design is introduced and discussed. The BIST system is implemented with a test signal source and a measurement system. The test signal source is designed using an LC oscillator and RF switches. The BIST measurement system consists of an RF mixer and low pass filter. By designing the BIST system as a sequence of relative measurements, the parameters of the BIST circuit can be eliminated from the computations, ensuring robustness with respect to process variations. By using the proposed co-design methodology, the performance impact can be eliminated or minimized. The performance impact so far has been the major bottleneck in BIST adoption by RF designers.

The BIST system was designed with CMOS 0.18μm IBM 7RF process to verify functionality. For performance comparison, a stand-alone LNA as well as an LNA with BIST are designed and fabricated. Gain measurements are within 0.1dB error for a 200-sample Monte-Carlo simulation and within 0.2dB error with 5 manufactured ICs. The BIST circuit introduces 0.1mm^2 area overhead, which corresponds to roughly 1.2% of the area of an RF transceiver front-end implemented with a similar technology [19-21]. Both

simulation and hardware experiments show that the proposed BIST system accurately determines the DUT gain and it does not affect performance of the DUT during normal mode.

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APPENDIX A

AM/AM AND AM/PM DISTORTION MEASUREMENT

In order to characterize AM/AM and AM/PM distortion of the PA in the loop-back mode, the supply voltage needs to be swept and the baseband output of the receiver is measured in the loop-back mode. Here, the baseband output of the receiver is DC value and several measurements and calculations are required for the PA characterization. In order to isolate DC offsets in the receiver, two measurement setups with different attenuation of the attenuator are required as follows.

$$I_{out,i} = \frac{1}{2} A_{in} \cdot G_{RX} \cdot G(v_{dd,N}) \cdot \cos(\varphi(v_{dd,N}) + \phi + \varphi_d) + DC_I \tag{A.1}$$

$$Q_{out,i} = \frac{1}{2} A_{\text{in}} \cdot G_{RX} \cdot G(v_{dd,N}) \cdot (1 + g_{RX}) \cdot \cos(\varphi(v_{dd,N}) + \phi + \varphi_d + \varphi_{RX}) + DC_Q \tag{A.2}$$

DC offsets are eliminated from the difference between two outputs that have different input signals (A_{in} and $2A_{in}$), which are given by

$$Q_{out,2} - Q_{out,1} = A_{in} \cdot G_{RX} \cdot (1 + g_{RX}) G(v_{dd,N}) \cdot \sin(\varphi(v_{dd,N}) + \phi + \varphi_{RX}) \tag{A.3}$$

$$I_{out,2} - I_{out,1} = A_{in} \times G_{RX} \times G(v_{dd,N}) \times \cos(\varphi(v_{dd,N}) + \phi) \tag{A.4}$$
$$\left(\phi = \varphi_{RF} + \varphi_d - \varphi_{LO}\right)$$

Then the phase characteristics of the PA is given by simply dividing ($Q_{out,2}$- $Q_{out,1}$) by ($I_{out,2}$-$I_{out,1}$) ,

$$\begin{aligned}
&\frac{Q_{out,2} - Q_{out,1}}{I_{out,2} - I_{out,1}} \\
&= \frac{0.5 \times A_{in} \cdot (1 + g_{RX}) G_{RX} G(v_{dd,N}) \cdot \sin(\varphi(v_{dd,N}) + \phi + \varphi_{RX})}{0.5 \times A_{in} \cdot G_{RX} G(v_{dd,N}) \cdot \cos(\varphi(v_{dd,N}) + \phi)} \\
&= \frac{1}{\cos(\varphi(v_{dd,N}) + \phi)} \Big[(1 + g_{RX}) \sin(\varphi(v_{dd,N}) + \phi) \cos(\varphi_{RX}) \\
&\qquad + \cos(\varphi(v_{dd,N}) + \phi) \sin(\varphi_{RX}) \Big] \\
&= (1 + g_{RX}) \tan\left(\varphi(v_{dd,N}) + \phi\right) \cdot \cos(\varphi_{RX}) + \sin(\varphi_{RX})
\end{aligned} \tag{A.5}$$

Therefore, the gain and phase characteristic of the PA are given by

$$\varphi(v_{dd,N}) + \phi = \tan^{-1}\left(\frac{\dfrac{-(Q_{out1,2} - Q_{out1,1})}{(I_{out1,2} - I_{out1,1})(1+g_{RX})} + \cos(\varphi_{RX})}{\sin(\varphi_{RX})} \right)$$

$$A_{in} G'_{RX} G(v_{dd,N}) = \frac{2 \times \left(I_{out,2} - I_{out,1} \right)}{\cos(\varphi(v_{dd,N}) + \phi)} \tag{A.6}$$

$$\left(G'_{RX} = G_{RX} \cos(\varphi_{RF} - \varphi_{LO}) \right)$$

APPENDIX B

DELAY SKEW AND BW LIMITATION MEASUREMENT

For delay skew measurement of the polar transmitter in the loop-back mode, a low BW two-tone signal with DC offset is applied to the polar transmitter input. Then PA output is given by

$$V_{PA,out}(t) = \left(A_{PA,out} \times \left| \cos(\omega_m (t+\tau) \right| + \Delta V_{PA,out} \right) c(\omega_m t) \cos(\omega_c t) \tag{B.1}$$

Where

$$A_{PA,out} = \left(G(v_{dd2}) - G(v_{dd1}) \right) \times A_{in}, \Delta V_{PA,out} = G(v_{dd1}) \times A_{in} \tag{B.2}$$

The above signal is applied to the receiver input through the attenuator and down converted to the baseband as follows.

$$V_{RX}(t) = \frac{1}{2} \left(A_{RX,out} \times \left| \cos(\omega_m (t+\tau) \right| + \Delta V_{RX,out} \right) c(\omega_m t) \tag{B.3}$$

Where

$$\begin{aligned} A_{RX,out} &= G'_{RX} \times \left(G(v_{dd2}) - G(v_{dd1}) \right) \times A_{in} \\ \Delta V_{RX,out} &= G'_{RX} \times G(v_{dd1}) \times A_{in}, \quad G'_{RX} = G_{RX} \cos(\varphi_{RF} - \varphi_{LO}) \end{aligned} \tag{B.4}$$

The baseband output of the receiver can be expressed as the sum of the cosine wave and distortion parts [16] given by

$$\begin{aligned} V_{RX}(t) &= \frac{1}{2} \left[A_{RX,out} \cdot \cos(\omega_m t) + A_{RX,out} \cdot u(\omega_m t) + \Delta V_{RX,out} c(\omega_m t) \right] \\ &= \frac{1}{2} \left[A_{RX,out} \cdot \cos(\omega_m t) + IMD \right] \end{aligned} \tag{B.5}$$

Where

$$u(\omega_m t) = \begin{cases} -2\cos(\omega_m t), & \pi/2 - \tau \le \omega_m t \le \pi/2 \\ -2\cos(\omega_m t), & 3\pi/2 - \tau \le \omega_m t \le 3\pi/2 \\ 0, & otherwise \end{cases} \tag{B.6}$$

$$c(\omega_m t) = \sum_{n=1,3,5,\cdots}^{\infty} c_n \cos(n\omega_m t), \qquad c_n = \frac{4}{\pi} \frac{(-1)^{(n-1)/2}}{n} \tag{B.7}$$

Since only the amplitude of the IMD product is required to calculate delay skew and BW limitation, it is more convenient to analyze,

$$u'(\omega_m t) = \begin{cases} -2\sin(\omega_m t), & 0 \le \omega_m t \le \tau \\ -2\sin(\omega_m t), & \pi \le \omega_m t \le \pi + \tau \\ 0, & otherwise \end{cases} \tag{B.8}$$

$$c'(\omega_m t) = \sum_{n=1,3,5,\cdots}^{\infty} c_n \sin(n\omega_m t), \qquad c_n = \frac{4}{\pi}\frac{(-1)^{(n-1)/2}}{n} \tag{B.9}$$

Because (B.8) is periodic function, it is represented as Fourier series and described by

$$u'(\omega_m t) = \sum_{k=1,3,5,\cdots}^{\infty} (a_k \cos(k\omega_m t) + b_k \sin(k\omega_m t)) \tag{B.10}$$

Where

$$\begin{aligned} a_k &= -\frac{2}{\pi}\left[\frac{1-\cos(k+1)\tau}{k+1} + \frac{\cos(k-1)\tau - 1}{k-1}\right] \\ b_k &= -\frac{2}{\pi}\left[\frac{\sin(k-1)\tau}{k-1} - \frac{\sin(k+1)\tau}{k+1}\right] \end{aligned} \tag{B.11}$$

Therefore, k^{th} order IMD of the V_{RX} is given by

$$\begin{aligned} IMD_k &= \frac{1}{2}\left[A_{RX,out} \cdot u(\omega_m t') + \Delta V_{RX,\text{out}} \cdot c(\omega_m t')\right] \\ &= \frac{1}{2}\left[A_{RX,out}\left(a_k \cos(k\omega_m t') + b_k \sin(k\omega_m t')\right) + \Delta V_{RX,out} \cdot c(\omega_m t')\right] \end{aligned} \tag{B.12}$$

Because IMD3 is focused on, IMD3 is expressed as follows.

$$\begin{aligned} IMD_3 &= \frac{1}{2}\times\left[A_{RX,out} \cdot u(\omega_m t') + \Delta V_{RX,\text{out}} \cdot c(\omega_m t')\right] \\ &= \frac{1}{2}\times\left[A_{RX,out}\left(a_3 \cos(3\omega_m t') + b_3 \sin(3\omega_m t')\right) + \Delta V_{RX,out} \cdot c_3 \sin(3\omega_m t')\right] \\ &= \frac{1}{2}\times\left[A_{RX,out} \cdot a_3 \cos(k\omega_m t') + \left(A_{RX,out} \cdot b_3 + \Delta V_{RX,out} \cdot c_3\right)\sin(3\omega_m t')\right] \end{aligned}$$

$$= \frac{1}{2} \times \sqrt{(A_{RX,out} \cdot a_3)^2 + \left(A_{RX,out} \cdot b_k + \Delta V_{RX,out} \cdot c_k\right)^2} \cos(3\omega_m t + \beta) \qquad \text{(B.13)}$$

Then the amplitude of the IMD3 is given by

$$\left|IMD_3\right| = \frac{1}{2} \times \sqrt{\left(A_{RX,out} \times a_3\right)^2 + \left(A_{RX,out} \times b_3 + \Delta V_{RX,out} \times c_3\right)^2} \qquad \text{(B.14)}$$

Where

$$\begin{aligned} a_3 &= -\frac{2}{\pi}\left[\frac{1-\cos(4\tau)}{4} + \frac{\cos(2\tau)-1}{2}\right] \\ b_3 &= -\frac{2}{\pi}\left[\frac{\sin(2\tau)}{2} - \frac{\sin(4\tau)}{4}\right], \quad c_3 = \frac{-4}{3\pi} \end{aligned} \qquad \text{(B.15)}$$

Regarding BW limitation

$$\begin{aligned} V_{RX}(t) = \frac{1}{2}\Bigg[A_{RX,out} \times \left(a_0 + \sum_{m=2,4,\cdots,M} a_m \cos(m\omega_m t) \right) + \Delta V_{RX,out} \Bigg] \\ \times \left(\sum_{n=1,3,5,\cdots} c_n \cos(n\omega_m (t+\tau)) \right) \end{aligned} \qquad \text{(B.16)}$$

$$\left|IMD_3\right|_{M=2} = \frac{1}{2} \times \left| A_{RX,out}\left[2a_0c_3 + a_2(c_1 + c_5)\right] + \Delta V_{RX,out} \times c_3 \right| \qquad \text{(B.17)}$$

$$\left|IMD_3\right|_{M=4} = \frac{1}{2} \times \left| A_{RX,out}\left[2a_0c_3 + a_2(c_1 + c_5) + a_4(c_3 + c_7)\right] + \Delta V_{RX,out} \times c_3 \right| \qquad \text{(B.18)}$$