Design and Analysis of a Dual Supply Class H Audio Amplifier

by

Cory Peterson

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Graduate Supervisory Committee:

Bertan Bakkaloglu, Chair
Sayfe Kiaei
Hugh Barnaby

ARIZONA STATE UNIVERSITY

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ABSTRACT

Efficiency of components is an ever increasing area of importance to portable applications, where a finite battery means finite operating time. Higher efficiency devices need to be designed that don't compromise on the performance that the consumer has come to expect. Class D amplifiers deliver on the goal of increased efficiency, but at the cost of distortion. Class AB amplifiers have low efficiency, but high linearity. By modulating the supply voltage of a Class AB amplifier to make a Class H amplifier, the efficiency can increase while still maintaining the Class AB level of linearity. A 92dB Power Supply Rejection Ratio (PSRR) Class AB amplifier and a Class H amplifier were designed in a 0.24um process for portable audio applications. Using a multiphase buck converter increased the efficiency of the Class H amplifier while still maintaining a fast response time to respond to audio frequencies. The Class H amplifier had an efficiency above the Class AB amplifier by 5-7% from 5-30mW of output power without affecting the total harmonic distortion (THD) at the design specifications. The Class H amplifier design met all design specifications and showed performance comparable to the designed Class AB amplifier across 1kHz-20kHz and 0.01mW-30mW. The Class H design was able to output 30mW into 16Ω without any increase in THD. This design shows that Class H amplifiers merit more research into their potential for increasing efficiency of audio amplifiers and that even simple designs can give significant increases in efficiency without compromising linearity.

DEDICATION

To my family for their support throughout my education, and to Caitlin for her love during all of the long nights and stressful hours spent working on this thesis.

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INTRODUCTION

1.1 Overview of Audio Amplifiers

Audio Amplifiers are found in most electronics produced today. They exist in devices like sound bars, AV receivers, smartphones, MP3 players, and tablets. One of the largest areas of research in audio amplifiers is in increasing their efficiency. For portable applications, the efficiency of the amplifier can be the determining factor between success and failure of the product line. Since portable devices are powered by a finite capacity battery, their efficiency determines their total operation time. For larger power devices such as recievers and professional grade speaker amplifiers, efficiency determines the overall size and cooling needed for the device. The increased efficiency for high end audio must come without degrading the performance of the device, because consumers desire the best quality sound. This is the challenge that designers face. How do we balance the need for low distortion and noise while still delivering high efficiency amplifiers to decrease the power consumption of the amplifier and in turn increase operation time for the device? This thesis focuses on the power amplifier in an audio setting and how to increase the efficiency without compromising on the noise or distortion properties of the output.

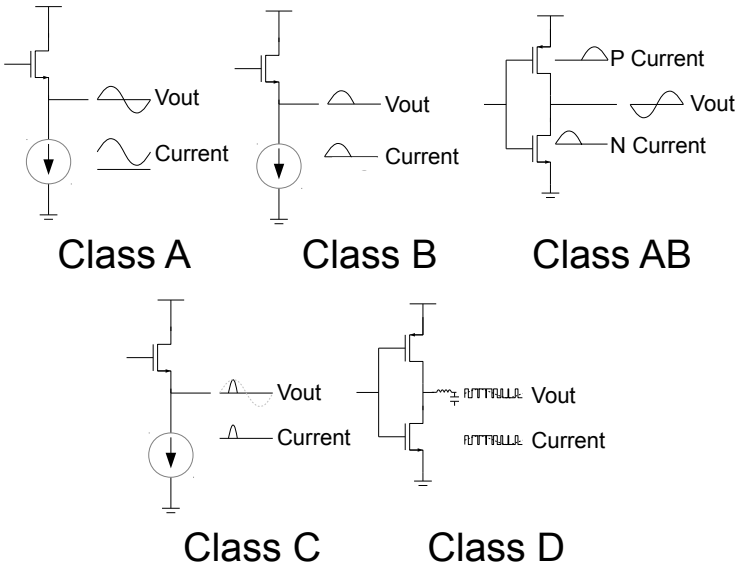

Figure 1.1: Amplifier Current and Voltage Characteristics

A common solution to the efficiency problem is to use a different amplifier design and trade off distortion for efficiency. This is most commonly found as a Class AB amplifier with a fixed supply voltage. This solution gives reasonable efficiency while maintaining good distortion and noise levels. At low output voltages, the output transistors dissipate a large amount of power. Class B amplifiers improve on this by only reproducing half of the waveform, saving half of the output power. Class C amplifiers only output when the signal is peaking, only supplying current for times when the output voltage is large. Another approach is to use a switching output stage to increase efficiency to almost the theoretical maximum of 100%. This comes at the cost of power supply noise rejection and distortion. Since switching amplifiers are essentially shorting the output to one of two supply rails, all noise from the supply is sent directly to the load. These can be mitigated through additional circuitry, but these also bring their own complexities that designers must deal with. A third solution would be to use a Class AB amplifier, to limit the distortion and noise, and modulate the supply rails to limit

the power lost to heat from the output transistors. The supply rails can either be switched to different discrete values, or modulated continuously with the input signal. This solution comes with its own design challenges though, primarily in the power supply rejection of the harmonics from modulating the supply rails. This system must use some sort of switching supply to maximize the efficiency of the conversion, but this creates large harmonics of the input signal on the power supply. The Class AB output stage must be able to reject these signals to a level below the noise floor or harmonic levels for there not to be any noticeable degradation in the signal quality. This design will focus on creating an efficient DC-DC converter that can supply the necessary power and maintain a slew rate fast enough for audio signals, as well as the design of the associated Class AB output stage that can reject the harmonics created by the switching supply.

Table 1.1: Typical Audio Amplifier Specifications

Specification	**Value**
Supply Voltage	± 2.5V
Quiescent Current	<1mA
Output Power	20mW @ 16Ω, < 0.1%THD,
Load Resistance	16Ω or 32Ω
SNR	>80dB
Bandwidth	20Hz-20kHz
PSRR	>70B
Gain	0dB/Adjustable
THD	< 1%

1.2 Thesis Outline

Chapter 2 describes the various amplifiers and power supply architectures available to use in this audio output system. The pros and cons of each architecture are discussed as well as the applications they are best suited for. Chapter 3 covers the characterization to be performed on the audio amplifier as well as the desired specifications for this design. Chapter 4 covers the actual design, as well as all simulation results. Chapter 5 will conclude with the comparisons and information learned from this research.

Chapter 2

AMPLIFIER INTRODUCTION

Amplifiers are used in many different applications, ranging from instrumentation, to loudspeakers, to transmitters in phones. Each case requires a different set of specifications with its own demands and design constraints. RF transmitters require narrowband amplification with low noise and high efficiency, audio amplifiers require wide bandwidth amplification with high current drive capabilities, and instrumentation and sensing applications need high gain and high input impedance. There are many different kinds of amplifiers, but a few main categories that are commonly used: Low Noise Amplifiers, Voltage Amplifiers, and Power Amplifiers. Low noise amplifiers are commonly used at the input stage of a system because they provide a large amount of gain with low additional noise, lowering the overall noise figure of the system. This is primarily used in transceivers where the input signal's power is low to begin with, so even the smallest added noise can mean the difference between correctly and incorrectly detecting the signal. Voltage amplifiers are required to have a high gain output and a high input impedance. Some, like the operational amplifier, are able to drive a load circuit. Others, like differential amplifiers, are used to convert a differential voltage signal to a single ended one, or used in a gain limiting feedback mode. These amplifiers are primarily used as gain stages in instrumentation or for filtering applications. Power amplifiers are commonly used as the output stage of a system, where a larger load must be driven. This is commonly the case at the speaker for an audio amplifier, and at the antenna of an RF transmitter. The audio power amplifier is the amplifier that will be discussed and designed in this thesis.

2.1 Amplifier Specifications

Amplifiers can be compared based on some basic operating characteristics. These will vary based on the application, so the specifications here will be tailored to audio applications. Sometimes these measurements are taken A-Weighted or Unweighted. In order to be more easily comparable to some other amplifier designs, we will use the unweighted measurements [21].

The primary goal of a power amplifier is to drive a load. The type of load can vary from capacitive to inductive to resistive or even a combination of them. In portable audio applications, the load is typically headphones, with an impedance of anywhere between 16Ω for standard headphones, up to 300Ω for some high end audiophile headphones. The output power of an amplifier is defined as

$$P_{Out} = \frac{V_{RMS}^2}{R} = V_{RMS} * I_{RMS} = I_{RMS}^2 * R \tag{2.1}$$

This means that the power of an amplifier is dependent both on the maximum voltage available at the output and the resistance of the load the amplifier is driving. For an output of 30mW and a typical headphone resistance of 16Ω, the amplifier must be able to supply a maximum amplitude signal of $\pm 1V$.

Another measurement done at the output of an amplifier is the Total Harmonic Distortion (THD). This measurement is a measurement of the distortion of an input signal due to nonlinearities in the amplifier. The calculation for THD is as follows

$$THD = \frac{\sqrt{V_{H2}^2 + V_{H3}^2 + ...V_{Hn}^2}}{V_1} \tag{2.2}$$

where V_H2, V_H3 ... are the harmonics of the base signal. Harmonics are usually measured in audio measurements up to 200kHz. Harmonic distortion in a amplifier produces audible results to the human ear down to values of 1%. Most

amplifiers are designed to have THD of <0.1% for this reason. One way that amplifiers can reduce distortion is through the use of negative feedback. This helps to linearize the amplifier by providing feedback on the error of the output. THD can also be used in calculating THD+N, which is a measurement of the total harmonic distortion plus noise.

Similar to harmonic distortion is the signal to noise ratio. The signal to noise ratio is the ratio of the desired output signal to the noise at the output. This measurement ignores the harmonic distortion in the output and is just a representation of the signal's ability to be detected over the noise of the amplifier. This is given by the formula in 2.3

$$SNR = 20log(\frac{V_{Sig}}{V_{Noise}}) \tag{2.3}$$

A third important measurement of an amplifier is the Power Supply Rejection Ratio (PSRR). The PSRR of an amplifier is an indication of how well the output ignores fluctuations in the power supply voltage. Since the wires connecting an amplifier to the supply have finite conductance, the noise from other parts of the circuit can travel to the output transistors in an amplifier. This can cause the power supply to be quite noisy at times, especially if there are heavy digital switching loads present. The PSRR of a circuit is defined as

$$PSRR = 20log(\frac{V_{OI}}{V_{In}}) - 20log(\frac{V_{OS}}{V_{Supply}}) \tag{2.4}$$

where V_{OS} is the output signal amplitude given only a signal on the supply, and V_{OI} is the output signal amplitude given only a signal on the input of the amplifier.

Dynamic range is another important specification for audio amplifiers. Dynamic range of an amplifier is the ratio between the maximum output signal without distortion to the noise floor of the amplifier, or the minimum signal that can be detected. This value is given by the formula

$$DR = 20log(\frac{V_{O_{MAX}}}{V_{Noise}}) \tag{2.5}$$

The last main specification for an amplifier that will be covered is the power efficiency. This value is related to the static or quiescent power of the amplifier. The quiescent power of an amplifier is defined as the current through a device not being delivered to the load times the supply voltage. The efficiency of the device is now defined as the ratio of the average power delivered to the load versus the average power delivered by the supply.

$$\eta(\%) = \frac{P_{Load}}{P_{Supply}} * 100\% \tag{2.6}$$

This can also be written as

$$\eta(\%) = \frac{P_{Load}}{P_{Load} + P_Q + P_{Loss}} * 100\% \tag{2.7}$$

This means that to increase the efficiency of an amplifier, we must reduce the quiescent power consumption of the device and the waste loss. This can be done in two ways: reducing the quiescent current, or reducing the supply voltage (if possible).

2.2 Amplifier Classes

Power Amplifiers can be categorized into classes based on their modes of operation. This categorization is based on the conducting time of the output transistors, whether the output is switching, and whether the supply rail is modulated [18].

Class A

A Class A amplifier is characterized by the fact that the output transistor(s) are conducting over the whole input cycle. This amplifier class has high speed due to this constant conduction, and has no turn on time. This design is simpler than other amplifier designs, as it only requires one transistor to function. This simplicity comes at a distinct disadvantage. The efficiency of this class of amplifier is much lower than other more complicated designs. Since there is only one transistor used, all of the change in load current must be provided by this transistor. This means that at best, this amplifier can be 50% efficient. Typical designs only reach an efficiency of 10-20%. The lack of distortion in this amplifier make it especially suitable for audio, but the low efficiency leaves them in the realm of audiophile home use.

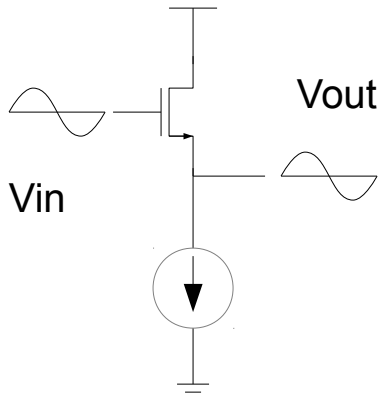

Figure 2.1: Simple Class A Amplifier

Class B

Class B amplifiers differ from Class A amplifiers in that the output transistors only conduct for half of the input cycle. This half conduction, half off cycle creates a large amount of distortion, but their efficiency is much higher than Class A

amplifiers. Since the device is off for half the time, their maximum theoretical efficiency is around 75%, but is typically closer to 40%. These amplifiers have a very distorted output, so they are not suited for use in audio applications.

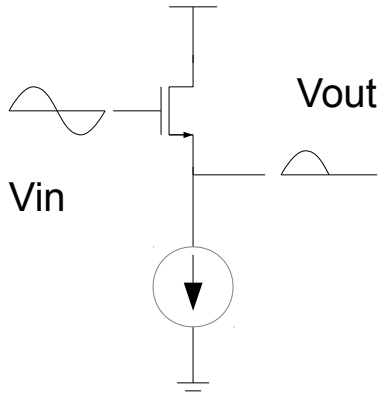

Figure 2.2: Class B Amplifier Output

Class C

A Class C amplifier conducts for even less than the Class B amplifier. The output devices usually conduct for 1/3 of the input cycle. This gives the potential for efficiencies up to 90%. The distortion from these amplifiers is usually mitigate through the use of a tuned load. This load is tuned to resonate at a fixed carrier frequency so that the harmonics are reduced compared to the carrier signal. This allows the original shape of the waveform to be restored. Typical implementations are limited by the current supply capabilities of the transistors, so they have to conduct for an increased amount of time, decreasing the efficiency. The typical efficiency of a Class C amplifier is around 65%. This class is also unsuited for audio since there is no carrier frequency used, and a tuned load is not an option.

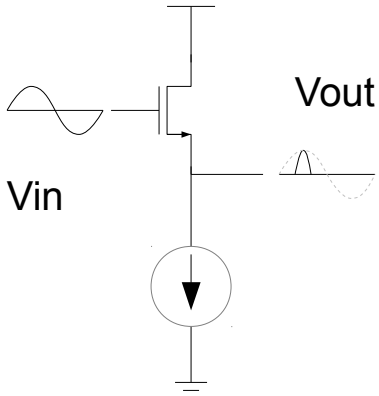

Figure 2.3: Class C Amplifier Output

Class D

A Class D amplifier is also known as a switching amplifier. This name comes from the fact that the output transistors switch between an on and off state rapidly to create and average of the input signal. The output then feeds into a low pass filter to remove the high frequency components from the constant switching of the output devices. Sometimes this filter is omitted to reduce cost, especially when the load has a natural low pass tendency. Class D amplifiers are typically used in audio because they can easily change the digital audio stream to an analog signal through the use of a PWM generation. This amplifier has drawbacks in the increased distortion, electromagnetic interference, and large current impulses.

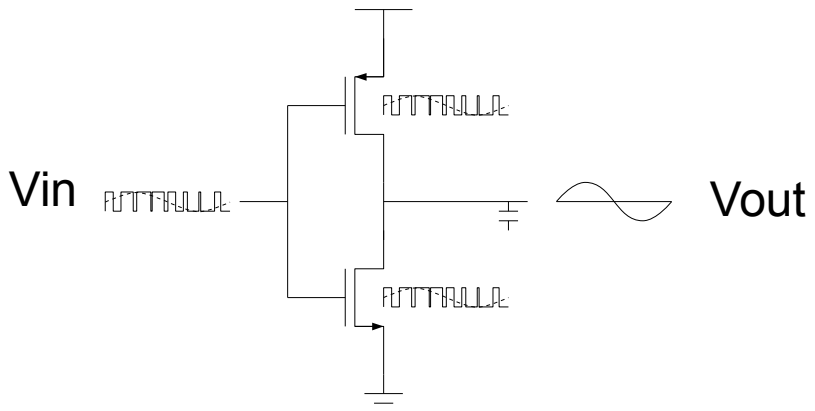

Figure 2.4: Class D Amplifier Output

Class AB

A Class AB amplifier is a compromise between the Class A and Class B amplifiers. For small amplitude signals, both output transistors conduct continuously, remaining in Class A operation. This provides a very low distortion output. As soon as the input signal amplitude is large enough, it enters Class B operation where the distortion products are smaller in relation to the input signal, but efficiency is much improved. This gives a good balance between the output quality and amplifier efficiency. Depending on the biasing, this amplifier can range anywhere from 10% to 75% efficient.

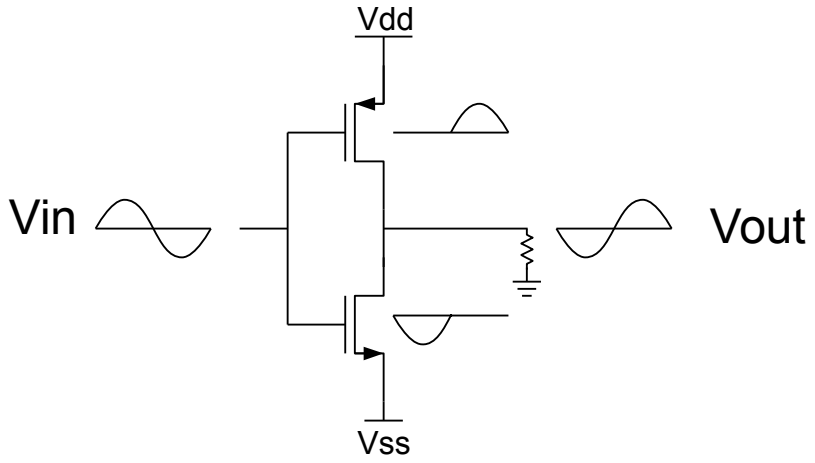

Figure 2.5: Class AB Push-Pull Amplifier

Class G

A Class G amplifier is actually a Class AB amplifier with a supply rail that can be switched between voltage levels. This increases the efficiency of the amplifier greatly. Rather than having the full supply voltage dropped across the output transistors during low amplitude periods, the amplifier switches to a lower voltage supply, reducing the power lost to heat. This helps reduce the power consumption and needed heat dissipation for the transistors. There can be any number of rails used in a Class G. Each additional rail can help to increase the efficiency even further. Their ideal use case is in digital amplitude modulated transmitters, as the amplitude switches between a couple predetermined amplitudes. These allow for easy rail switching during amplitude switching without causing any additional problems. Class G amplifiers are one of the most common amplifiers found in professional audio amplifiers. They have great linearity and harmonics performance, and have good efficiency. The main drawback of a Class G amplifier is the glitches that can result from switching voltage supplies. These can be mitigated, but this involves additional circuitry and complexity.

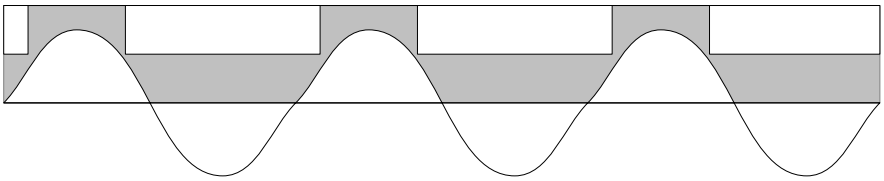

Figure 2.6: Class G Power Savings; Gray = Losses

Class H

A Class H amplifier takes the ideas from a Class G amplifier one step further, by rather than having only a few supply rails, modulating the supply voltage continuously. The rail is a replica of the input signal shifted up by some DC value. There are variations that allow for a minimum rail voltage and varying headroom levels, but they all share the same concept of minimizing the voltage drop across the output transistors for the entire cycle. The main advantage of this architecture is the large power savings in lower amplitude signals. Because there is only a minimal Vdsat across the output transistors, there is never very much power wasted as heat. This comes at a large cost though, as the output amplifier must be able to withstand large changes in supply voltage. Any harmonics present from the supply modulation will be in-band noise and can't be filtered out. This means that the power supply rejection ratio (PSRR) of the output stage needs to at least be as good as its own nonlinearities. This will guarantee that any harmonics from the supply will be masked by the large harmonics present from the output stage itself, making it comparable in quality to a constant supply design.

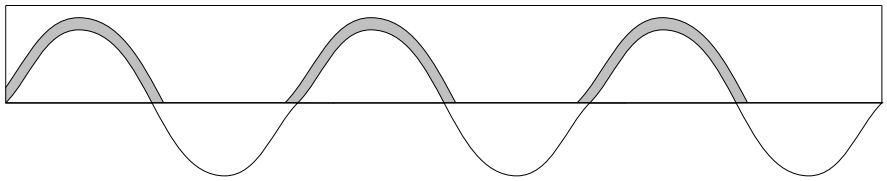

Figure 2.7: Class H Power Savings; Gray = Losses

2.3 Class AB Architectures

Input Stages

There are 3 main categories of basic input stage: Classical, Low Voltage, and Folded Cascode [9]. The classical architecture is the simplest and smallest architecture. It consists of a current multiplier differential p-input amplifier with a single ended output. This output then feeds into a floating battery or voltage offset circuit. This circuit consists of two current sources pushing and pulling from a pair of N and P transistors. The N and P transistors create a voltage offset for the output stage. This architecture is shown in figure 2.8.

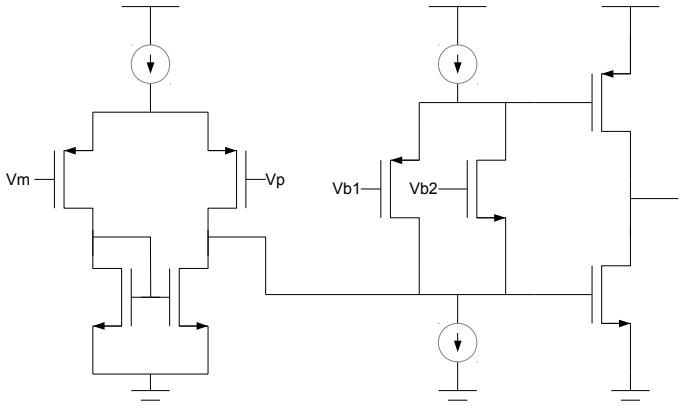

Figure 2.8: Classical AB Amplifier

The low voltage architecture is similar to the classical architecture. They both use the same floating battery and output stages, but the input stage is slightly different. Rather than using a single ended output, it uses a differential output cascaded into a second stage that generates a single ended output. This is typically a differential amplifier with diode connected loads cascaded into the same amplifier as used in the classical architecture.

The folded cascode is just a standard folded cascode design with a single ended output. This input architecture helps increase the gain, but at the cost of increased noise performance. It can feed into either the classical or low voltage output stages. This architecture is shown in figure 2.9.

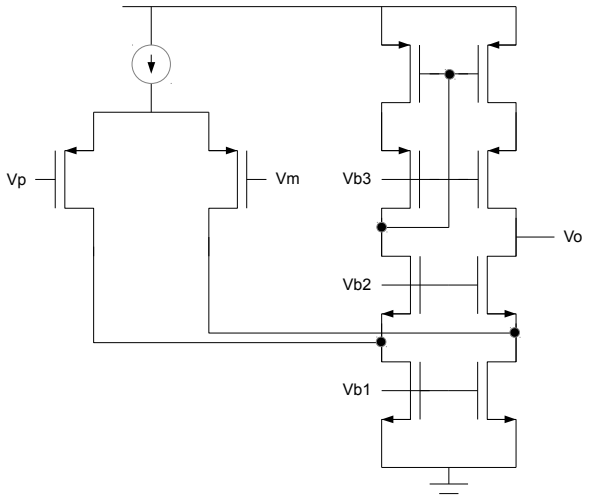

Figure 2.9: Cascode Input Stage

Output Stages

There are 3 main categories of output stage: Classical, Low Voltage, and Super AB. The classical AB output stage is the same used for the three basic input stages before. It consists of a floating battery and two N and P output transistors.

The low voltage output stage replaces the output and part of the input stage from a folded cascode. This architecture is particularly useful with low headroom constraints. It also increases the DC gain of the amplifier. The overall design of this architecture is shown below in figure 2.10.

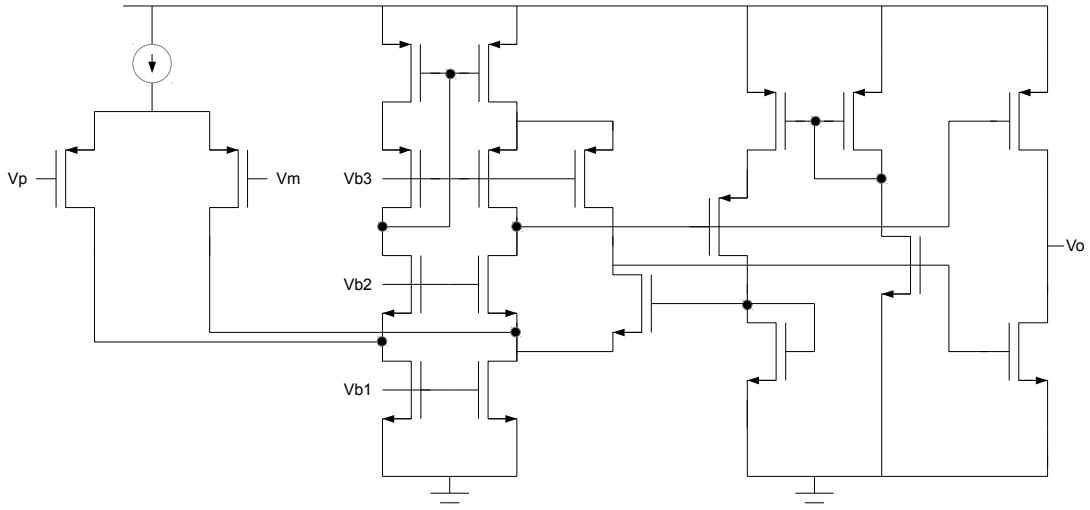

Figure 2.10: Low Voltage Folded Cascode Class AB Amplifier

The Super AB architecture is an interesting architecture that uses adaptive bias circuits to boost the current output capabilities [13]. Some of the issues that earlier attempts have encountered are large wasted currents in mirroring, large capacitive loads that must be driven to decrease current waste, and the inability to force unconditionally stable circuits. By using local common mode feedback and adaptive biasing, a Super AB amplifier can have additional current boosting, near-optimal current efficiency, and increased gain bandwidth compared to conventional Class AB amplifiers. A basic Super AB amplifier is shown in figure 2.11. When the differential input amplitude increases, the adaptive biasing circuit increases the bias current given to the input transistors. This causes a large increase in the voltage at the drain of the negative input. This increases the current in the negative branch, increasing the current delivered by the output PMOS device. This greatly increases the output voltage. The resistors between the input transistors' drains help to stabilize the circuit, increasing the phase margin. The simplest adaptive biasing circuit for this architecture is cross coupled floating batteries. This

is the bias shown in figure 2.11. This circuit has fairly good gain, PSRR, and noise characteristics for audio applications, but is not suited for a low voltage supply due to the adaptive biasing circuit.

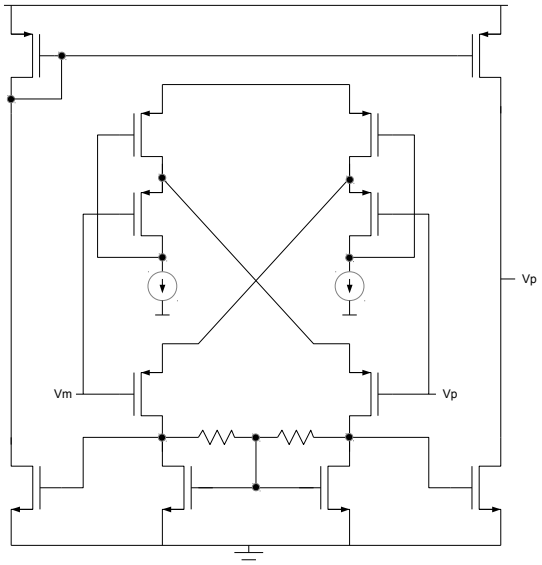

Figure 2.11: Super AB Amplifier

Class AB Flipped Voltage Follower

The Class AB flipped voltage follower is a novel architecture that combines the higher slew rate and bandwidth of a flipped voltage follower with Class AB operating characteristics to give fast settling, ouput swing, low bias current, and high slew rate and bandwidth [14]. The basic architecture of this amplifier is given in figure 2.12. A positive voltage input on Vi will lower the input transistor's drain voltage, increasing the current through this leg. It gets mirrored across to the next leg, where it is gained up by the final leg before being fed back to the source transistor of the input leg. This loop quickly adjusts to any input voltage, helping to create a good Class AB amplifier. The main downside to this design is that all positive output current must travel through two transistors as opposed to one in the

classical architectures. The output also has a constant voltage difference from the input, similar to a standard voltage follower. These two disadvantages make it less suitable for audio amplifier applications.

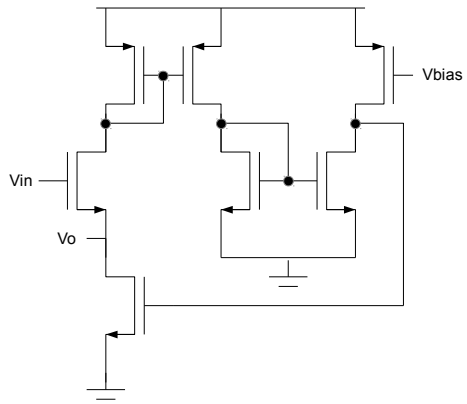

Figure 2.12: Class AB Flipped Voltage Follower

Enhanced PSRR Class AB

Another architecture that is well suited for audio applications is the Enhanced PSRR Class AB amplifier designed by Loikkanen et al [10]. This amplifier uses a Class AB control loop to improve the PSRR by upto 40dB over conventional symmetric stage amplifiers. This also comes without any additional headroom cost for the amplifier. The schematic for this architecture is shown in figure 2.13. By using a ground referenced miller compensated amplifier, the power supply noise can be attenuated. This may not work as well with the large supply swings that will be generated by a Class H architecture.

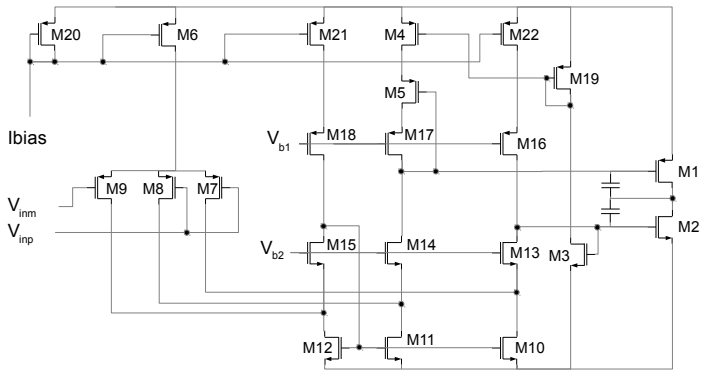

Figure 2.13: Enhanced PSRR Class AB Amplifier

Feedforward Enhanced PSRR Class AB

Another way to increase the PSRR of a Class AB amplifier is with a Feedforward Enhanced PSRR Class AB architecture [4]. This architecture uses two gain paths to correct the output. There is a high gain amplifier path that amplifies just the error in the output. This is combined with a feedforward path for the input signal. These two paths join at the input to a Class AB amplifier. This amplifier uses both a local feedback and a global feedback loop to correct for any power supply noise. The system level diagram is shown in figure 2.14. This architecture can reach up to 120dB of PSRR at a low frequency. It was primarily designed for attenuating inband noise from a GSM system on the same supply. This noise was at 217Hz (within the audio band), and was able to be rejected at over 120dB. This is an ideal example of the rejection needed for a Class H supply. The complications in this design include the high gain amplifier, and keeping all of the feedback loops stable. If the high PSRR is needed, this is a small price to pay for the given performance.

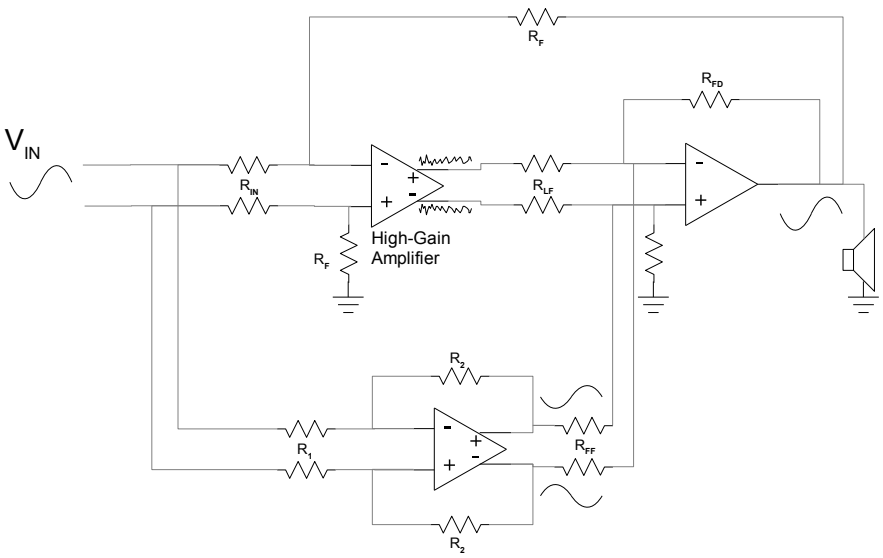

Figure 2.14: Class AB Feedforward Architecture

2.4 DC-DC Conversion Architectures

There are many different ways to convert voltage from one DC level to another. The primary ways are from a linear regulator, switched mode supply, or a charge pump. Linear regulators are the most inefficient, as they dissipate the excess voltage across transistors as heat rather than doing any conversion. Charge pumps are very efficient (up to 95%) but have a fixed voltage stepping and are better suited to a Class G supply architecture.

PWM Supply

Yamaha has developed a system called EEEngine that uses a Class D amplifier as a pwm supply for a Class AB architecture [16]. By using a Class D amplifier as the supply, they claim improved efficiency over standard Class AB amplifiers. Their design uses a zero current switching resonant mode converter. They also maintain the linearity and acoustic quality of Class AB amplifiers due to the final output stage being a standard Class AB amplifier. This has the potential to be a solution

to the power versus quality tradeoff of supplies. One big advantage of the PWM supply over a Class D amplifier is that EMI is reduced because the audio signal is not converted to a PWM signal at the output.

Buck Converter

A buck/boost converter uses reactive components to convert voltage to current or vice versa. These switched mode power supplies have been known to reach efficiencies of up to 95%. The voltage output of a buck converter is dependant on the duty cycle of the control signal. The longer the input switch is closed, the higher the output voltage gets. A buck converter operates in one of two modes, continuous, or discontinuous. The buck converter stays in continuous mode if the current through the inductor never falls to zero during a cycle. During this time, the output voltage is proportional to the input voltage. This proportion is determined solely by the duty cycle of the pulses on the switch.

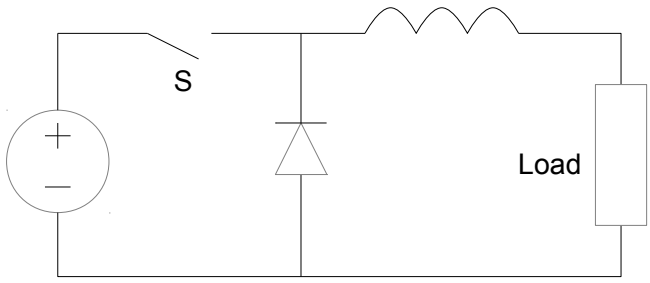

Figure 2.15: Basic Buck Converter

The converter enters discontinuous mode if the current through the inductor reaches zero during a cycle. During this phase, assuming ideal components, the output voltage is found by the expression

$$V_o = V_i \frac{1}{\frac{2LI_o}{D^2 V_i T} + 1} \tag{2.8}$$

This complicates the control of the system when the output voltage is changing. To solve this problem, a hysteretic control system can be created. This control system can be clocked at a set frequency, and turn off the switch when the output voltage rises to the desired voltage. By doing this, a closed loop can set the voltage at the output, eliminating the nonlinear system that controls the output. This does, however, create harmonics of the input signal in the output voltage. These harmonics must be able to be rejected by the amplifier for the overall output quality to not degrade. The circuit can use even more complex hysteresis control by measuring the output current, voltage, and input signal to modulate the supply switches. The system designed by Liu et. al. [7] showed great increases in efficiency with minimal increase in total harmonic distortion. The system diagram is shown in figure 2.16.

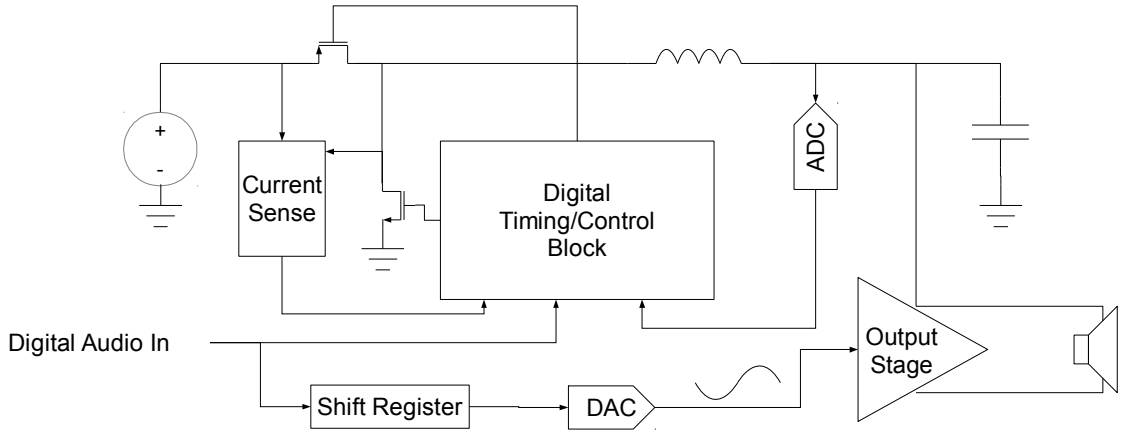

Figure 2.16: Class H Audio Amplifier [7]

2.5 Audio Signals

Audio signals have frequency components ranging from 20Hz to 20kHz. The apmplitude of the signal is dependent on the sum of all frequency components of the signal. This signal generates an magnetic field in the voice coil of a speaker, causing a diaphragm to move towards or away from a magnet in the speaker. The distance the diaphragm moves is dependent on the magnitude of the magnetic field. Increasing the voltage increases the current which increases the movement of the diaphragm. The farther the diaphragm moves, the louder the sounds generated are. Audio signals have a unique amplitude distribution compared to other types of signals. The voltage distribution of a sinusoid is shown in figure 2.17. This is compared to the distribution of an audio signal, shown in figure 2.18. The absolute value of the amplitude was divided into 500 histogram bins to calculate these distributions. A wide variety of song genres were used to give a good representation of the typical content of audio. These results match those found in [22].

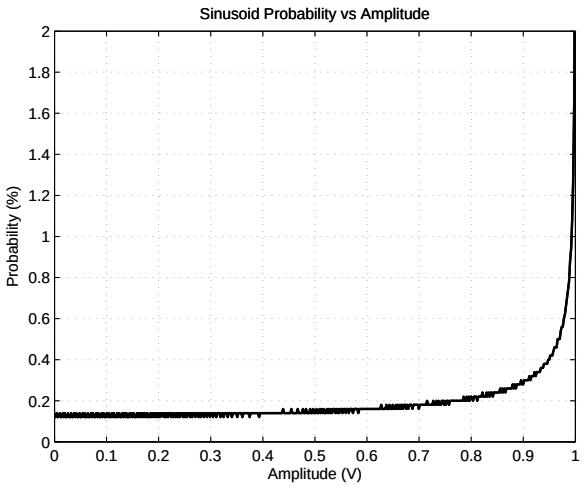

Figure 2.17: Sinusoid Amplitude Probability

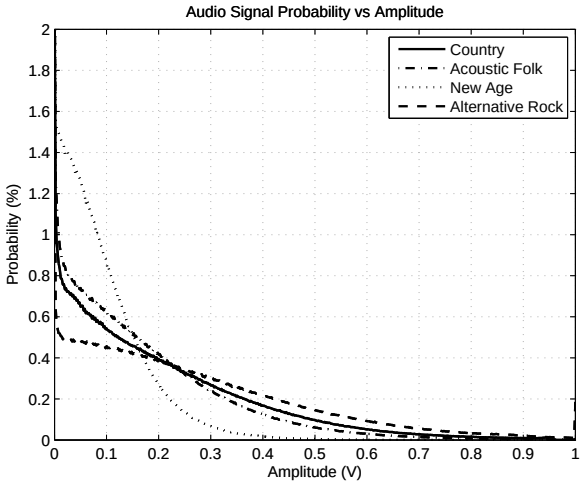

Figure 2.18: Audio Signal Amplitude Probability

This distribution means that the efficiency of an amplifier at low voltages is more important than its efficiency at high voltages. By lowering the supply voltage, this efficiency can be increased. Although testing with music would produce results more representative of real world use, the testing in this thesis will be done using sinusoids. Sinusoids can be simulated for a shorter duration, are more comparable to other research.

2.6 Chosen Architecture

For this design, the Enhanced PSRR Class AB architecture was chosen for the Class AB part of the amplifier. Schematic specifics and sizing will be further explored in chapter 3. This design was chosen because it provides for the simplest design while still improving on the PSRR statistics of prior designs. It also provides the benefit of being unconditionally stable, which helps to simplify any compensation networks needed. The power supply will be a multiphase buck converter operating in a hysteretic mode that supplies the PDRV generating and output transistors. This will minimize its impact on the performance of the amplifier while still giving maximal benefit to the efficiency during low amplitude signals.

2.7 Literature Review

Many variations of headphone audio amplifiers have been researched and compared in recent years. Many of these have been done on Class D amplifiers as they are the best suited to portable audio uses. There have been some Class AB amplifiers, some Class G amplifiers and very few Class H amplifiers implementations compared. These amplifiers can be difficult to compare directly, as many have large differences in power outputs, THD is reported at different power levels, and some don't report PSRR values.

Table 2.1: Comparison of State of the Art

Ref	Class	Load	Output Power	THD+N	PSRR@20kHz	Idle Power
[1]	AB	16Ω	15mW	-96dB	80dB	5.2mW
[2]	AB	16Ω	93.8mW	-77.9dB	65dB	1.43mW
[3]	AB	16Ω	27mW	-64dB	NR	5mW
[4]	G	16Ω	60mW	-95dB@10mW	120dB	5.2mW
[5]	G	16Ω	53mW	-70dB@10mW	84dB	10.3mW
[6]	G	16Ω	25mW	-74dB@10mW	100dB	2.2mW
[7]	H	8Ω	500mW	<0.1%	NR	12mW

Desired Specifications

The design specifications for this audio amplifier are given in table 2.2. This amplifier was designed to be competitive with current amplifiers of similar power levels. The primary focus of this design is to attempt to show power efficiency improvements in a Class H amplifier versus a standard Class AB amplifier at typically used performance levels.

Table 2.2: Table of Desired Specifications for Amplifier

Specification	**Desired Value**
Supply Voltage	± 2.5V
Process	TSMC 240nm
Quiescent Current	<1mA
Output Power	30mW @ 16Ω, < 0.1%THD,
Load Resistance	16Ω
SNR	100dB
Bandwidth	20Hz-20kHz
PSRR	80B
Gain	0dB
THD	< 1% 0-30mW

Chapter 3

IMPLEMENTATION OF CLASS H SUPPLY FOR A CLASS AB AUDIO POWER AMPLIFIER

3.1 Enhanced PSRR Class AB Amplifier

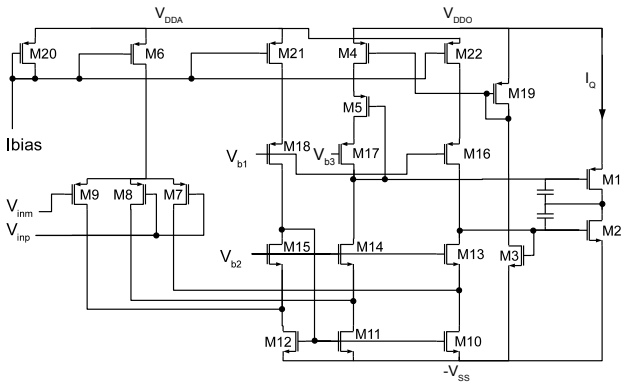

Figure 3.1: Modified Enhanced PSRR Class AB Amplifier

The previously designed Class AB amplifier architecture used was designed with a light resistive large capacitive load in mind and only one supply, so it had to be modified to work with the 16Ω load for audio use and the Class H supply. This first meant increasing the size of the output transistors. These transistors will determine the maximum current available to drive the load. This also creates a large gate capacitance that the previous stage must drive. In order to drive these loads, the circuitry driving them needed to be increased in size as well. The output transistors are labeled as M1 and M2 in figure 3.2.

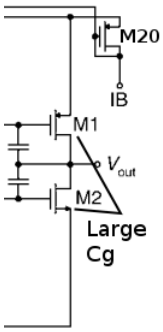

Figure 3.2: Enhanced PSRR Class AB Output Transistors

Next, a split supply had to be created in order to allow use of a modulated supply. By splitting the mirrored pmos and following stacks, the PSRR can be maintained without affecting the input stage's biasing.

Doing a small signal analysis of this circuit shows that the output NMOS gate is driven primarily by the combination of gm from M9 mirrored onto M10 and the gm from M7. These are the primary currents that will have to drive the capacitive load of the output transistor gates. Figure 3.3 shows the small signal equivalent of the overall amplifier. For simplicity, the output stage is not included, and the input stage has been replaced by current sources equal to their small signal equivalent with as an ideal current source. The Folded cascode transistors have gm's of gm_0 and $\frac{gm_0}{2}$ for the negative and positive transistors respectively.

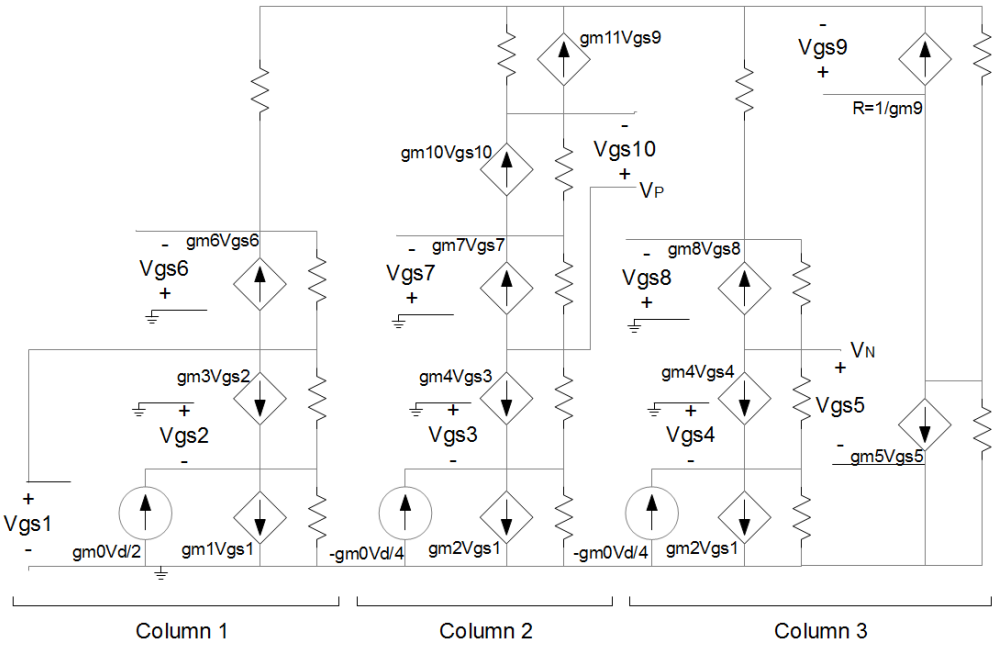

Figure 3.3: Circuit Small Signal Equivalent

Analysis starts with the first column. This is the biasing leg for the other two columns, and is independent of the other columns. Using a series of nodal analysis results, approximating that the top 3 transistors have 10x the r_o of the bottom transistors, and approximating that $gmr_0 >> 1$ for each case, V_{GS1} is found to be given by equation 3.2.

$$\begin{aligned} V_Z &= \frac{V_Y}{2 + 10gm_6r_o} \\ V_X &= V_Y \frac{1 - 10gm_1r_o}{11 + 10gm_3r_o} + \frac{V_d}{2} \frac{10gm_0r_o}{11 + 10gm_3r_o} \\ V_Z(10gm_6r_o + 1) &- 2V_Y + V_X(10gm_3r_o + 1) = 0 \end{aligned} \tag{3.1}$$

Assuming that $gmr_o >> 1$ for each gm_i,

$$V_Y = V_{GS1} = \frac{V_d}{2} \frac{gm_0}{gm_1} \tag{3.2}$$

V_{GS1} is just a function of the differential input and the ratio of gm_1 to gm_0. Using this result, column 3 can now be analyzed.

$$\begin{aligned} V_X &= V_Y \frac{1}{11+10gm_4r_o} + \frac{V_d}{2}\frac{10gm_0r_o}{11+10gm_4r_o} \\ V_Z &= \frac{V_Y}{2+10gm_8r_o} \\ V_Z(10gm_8r_o+1) &- 2V_Y + V_X(10gm_4r_o+1) = 0 \end{aligned} \tag{3.3}$$

Assuming that $\frac{1+10gm_8r_o}{2+10gm_8r_o} \approx 1$, $V_Y = V_{N_{DRV}}$ is given by 3.4.

$$V_Y = V_{N_{DRV}} = \frac{V_d(gm_0r_o)(1+10gm_4r_o)}{2} = V_{GS5} \tag{3.4}$$

V_{GS9} is easily found as being $\frac{V_d gm_5 gm_0 r_o(1+10gm_4r_o)}{2gm_9}$. Using this, column 2 can finally be solved.

$$\begin{aligned} V_X &= V_Y \frac{1}{11+10gm_4r_o} + \frac{V_d}{2}\frac{10gm_0r_o}{11+10gm_4r_o} \\ V_Z &= \frac{V_Y(\frac{r_o}{r_{o1}} - gm_{10}r_o) + V_W(\frac{r_o}{r_{o1}} + gm_{10}r_o)}{(1+\frac{r_o}{r_{o1}} + gm_7r_o)} \\ V_W &= \frac{V_Z\frac{r_o}{r_{o1}} + V_Y gm_{10}r_o - V_{GS9}gm_{11}r_o}{2+gm_{10}r_o} \\ V_Y &= \frac{V_X(1+10gm_4r_o) + V_Z(1+10gm_7r_o)}{2} \end{aligned} \tag{3.5}$$

$$V_Y = V_{PDRV} = \frac{5Vd(gm_0r_o)((gm_5gm_7gm_{11}r_o)(100gm_4r_o^2 + 120r_o + \frac{11}{gm_4}) + gm_9)}{gm_9} \tag{3.6}$$

The PMOS driving signal has a much larger gain than the NMOS driving signal. The large P-Side gain will help to reduce greatly reduce the noise from a noisy positive supply. A similar analysis can be done to find the PSRR of the architecture. Applying a signal onto the VDDA supply and removing the other sources, the input transistors and first and third stack can be neglected. By making the assumption that 1/gm19 is much smaller than ro of M3, we can then assume

that Vgs19 is equal to the supply disturbance. Doing a nodal analysis on the remaining stack, a formula for the PDRV signal can be found. The result is shown in equation 3.7.

$$V_{PDRV} = \frac{1000gm^3r_o^3 + 1200gm^2r_o^2 + 120gmr_o + 11}{1000gm^3r_o^3 + 2200gm^2r_o^2 + 420gmr_o + 41} \tag{3.7}$$

If the gain of these transistors is much larger than 1, this simplifies to Vp/Vsup=1. Since this is an approximation, the actual PSRR will be a finite but very large number based on the gain.

The sizing for each of the transistors in the design is given in table 3.1. The architecture is repeated below for reference.

Table 3.1: Table of Class AB Amplifier Transistor Sizes

Device	**W(um)**	**L(um)**	**Mult**
M1	4.32	.24	80
M2	4.32	.24	20
M3	2.16	.24	8
M4	5.4	1.08	5
M5	4.32	.24	5
M6	4.32	1.08	80
M7, M8	4.32	1.08	20
M9	4.32	1.08	40
M10, M11, M15	2.16	1.08	8
M12	2.16	1.08	16
M13, M14	2.16	1.08	4
M16, M17, M22	4.32	1.08	5
M18, M21	4.32	1.08	10
M19	.36	1.08	1
M20	4.32	1.08	1

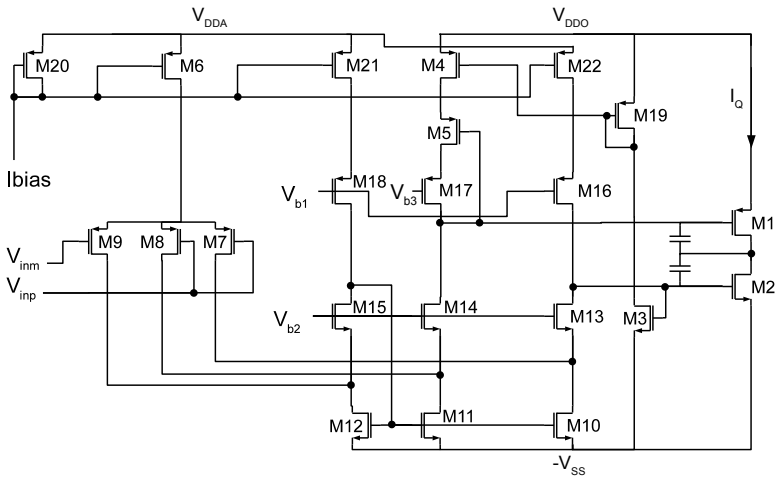

Figure 3.4: Modified Enhanced PSRR Class AB Amplifier

Most of the design time was spent optimizing this circuit, as it is the main contributor of distortion noise, and needs to have a high PSRR in order to reject any power supply ripple from the buck converter supply. Parametric sweeps were done to optimize each stage after initial sizing. Additional time was spent making sure that the circuit operated correctly with a changing supply voltage, and some changes needed to be made to ensure correct operation over a wide range of supply voltages.

3.2 Buck Converter

The buck converter will be a multiphase buck converter operating in a hysteretic PWM mode. Hysteretic PWM mode refers to operation that modulates the duty cycle based on the difference between the input and output voltage. When The clock triggers, a SR latch gets set to enable the inductor path. As soon as the output reaches the input voltage level, the reset comparator signals to reset the latch. An optional voltage reference comparator controls this reset signal to only trigger if the output is above the reference voltage. This allows for an adjustable minimum output voltage. A system level diagram of this circuit is shown in figure 3.5.

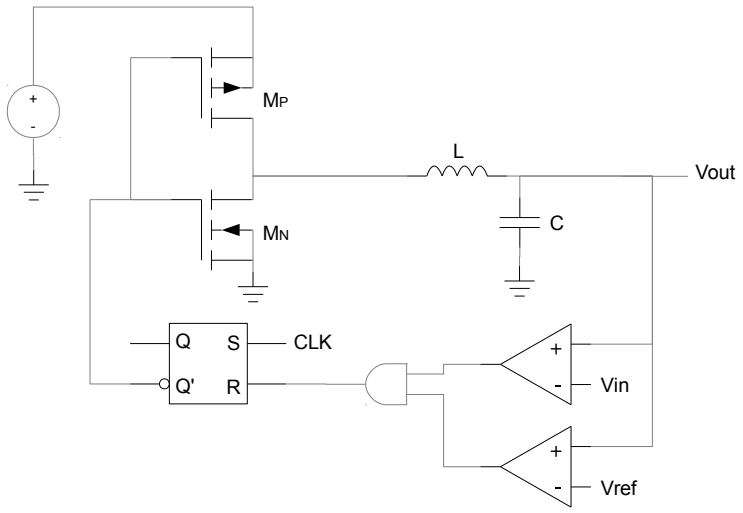

Figure 3.5: Hysteretic PWM Buck Converter System Diagram

When the output signal is above both Vin and Vref, the SR latch resets, which sets Q' high. This turns the PMOS off, and the NMOS on. Energy stored in the inductor now pulls current from ground to send to the output. Vout starts falling until the clock triggers again. This sets Q, pulling Q' low and turning on the PMOS and off the NMOS. The inductor now has a positive voltage across it and starts storing energy again. This process repeats continuously. On a falling input voltage, the SR latch stays in a reset state, allowing the output voltage to fall by supplying current to the load. The rate it falls is dependent on the load resistance and buck converter capacitance. The slew rate of the buck converter is dependent on the capacitor and inductor values chosen, resistance, and the load driven. For simplicity, the PMOS load resistance will be assumed to be 0. The system response is given by 3.8, where C is the capacitance, L is the inductance, and R_L is the load resistance.

$$V_O(s) = \frac{R_L}{s(s^2LRC + sL + R_L)} \tag{3.8}$$

The voltage ripple of the output is determined purely by the capacitor, load current, and duty cylce. For worst case, the whole clock cycle is used. For a 5MHz clock rate, this is 200ns. The load current will be the 30mW into 16Ω, or 43.3mA. To keep ripple at less than 100mV, the capacitor must be at least 86.6nF. Ideally, the voltage should fall to approximately 0 during the following low period to reduce power consumption. This gives a maximum value of the capacitor of 250nF. A value of 200nF was chosen initially for margin. To ensure fast enough response for a 16Ω load, the inductor must be sized appropriately. In order to allow for the fast transient response needed, while still maintaining increased efficiency, a nonsymmetric multiphase design was chosen. The general architecture for this design is shown in figure 3.6.

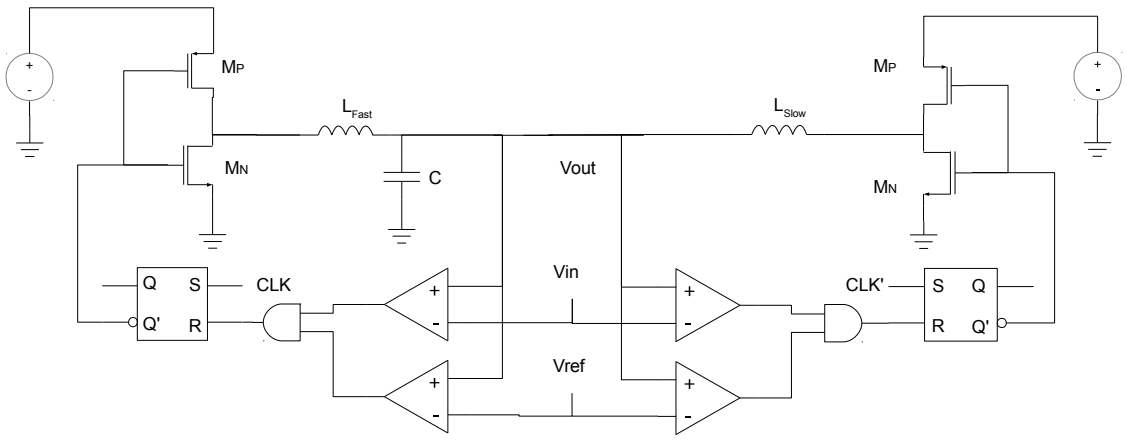

Figure 3.6: Multiphase Buck Converter

During the high clock phase, one side operates in a hysteretic mode, stopping when the output signal reaches the desired voltage. When the clock goes low, the opposite side starts conducting. This side operates in much the same as the first side, the only difference is the reset during the low clock period, as opposed to the high clock period. The sizing for the switches and inductors for the final design is given in table 3.2.

Table 3.2: Table of Class H Supply Sizing

Device	**W(um)**	**L(um)**	**Mult**
M1,M3 (PMOS)	4.32	.24	200
M2,M4 (NMOS)	4.32	.24	50

Passive	**Value**
L_{Fast}	25uH
L_{Slow}	100uH
C	1uF

3.3 Peripheral Circuitry

In order for the two circuits to be combined, some peripheral circuitry must be designed. The architectures for these circuits is very standard, as high performance is not necessary. The first such circuit is an offest voltage generator. This circuit consists of a resistor and a PMOS device in a common drain amplifier configuration. The design is shown in figure 3.7. This configuration generates an offset of approximately V_{tp}. By tying the bulk to V_{dd}, this V_{tp} can be increased even further if needed.

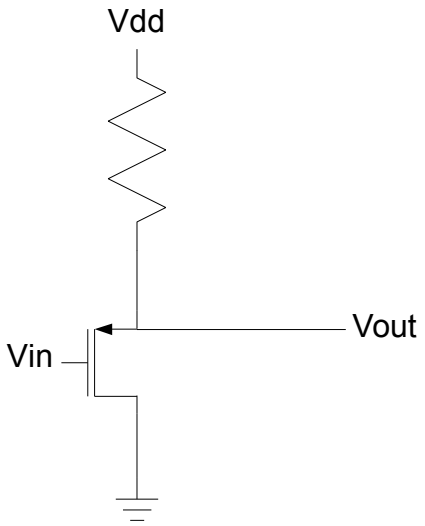

Figure 3.7: Offset Voltage Generator

The next circuit needed is a comparator. The architecture used for this is a standard comparator design as shown in figure 3.8. This circuit uses positive feedback on the PMOS devices to increase the gain at low differential voltages.

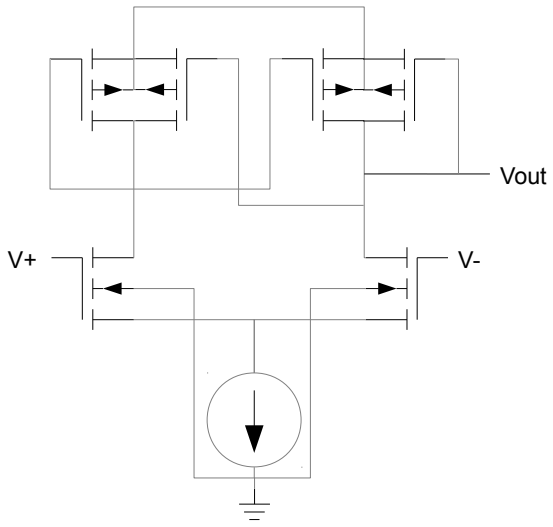

Figure 3.8: Offset Voltage Generator

The next circuit used is a simple rising edge detector. This circuit consists of an inverted and delayed verion of a signal ANDed with itself. When the input rises, the delay path will remain high for a brief time, generating a pulse on the output. This circuit is shown in figure 3.9.

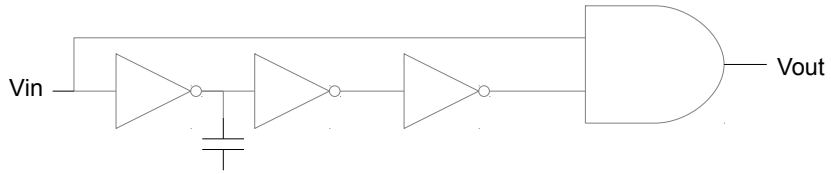

Figure 3.9: Rising Edge Detector

The last circuit is a simple SR latch with reset priority. This is just crosscoupled NOR gates with additional logic for the reset priority. Since the clock will be pulsing constantly, the reset signal needs to have priority over the output to keep it from switching during the time when both S and R are high.

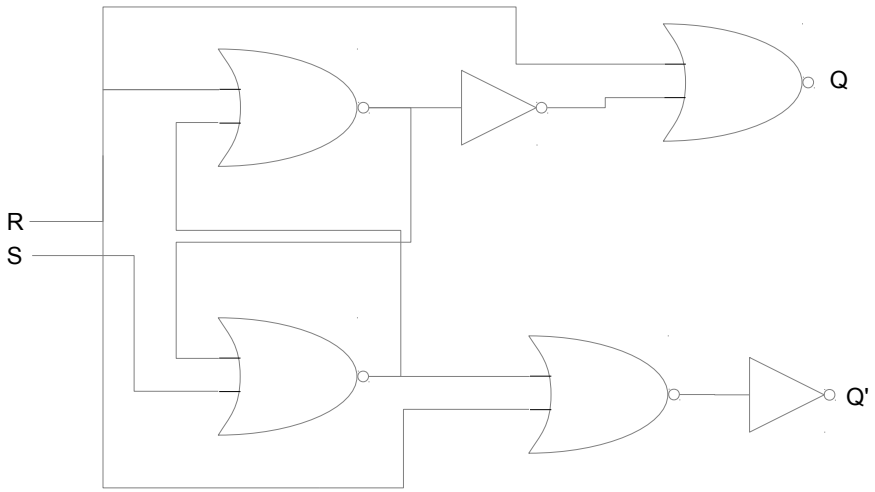

Figure 3.10: SR Latch with Reset Priority

3.4 SPICE Speaker Model

Real world speaker models are very complex and are a function of the headphone drivers, materials, human ear, and surrounding space [20]. This can and is usually simplified during simulations for easier analysis. For the purposes of the simulation of this amplifier, a simple 16Ω or 32Ω resistive load will be used for all measurements, while a complex representation of the speaker composed of resistive, capacitive, and inductive loads will be used for stability checking purposes. The basic model is shown in figure 3.11, while the frequency response in the audio band is shown in figure 3.12.

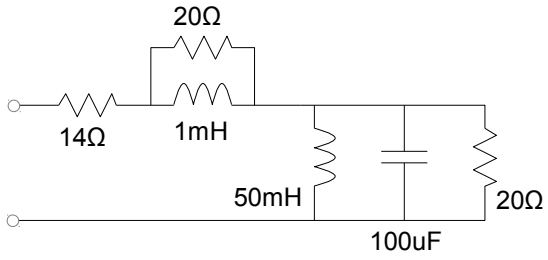

Figure 3.11: Simplified Speaker Model

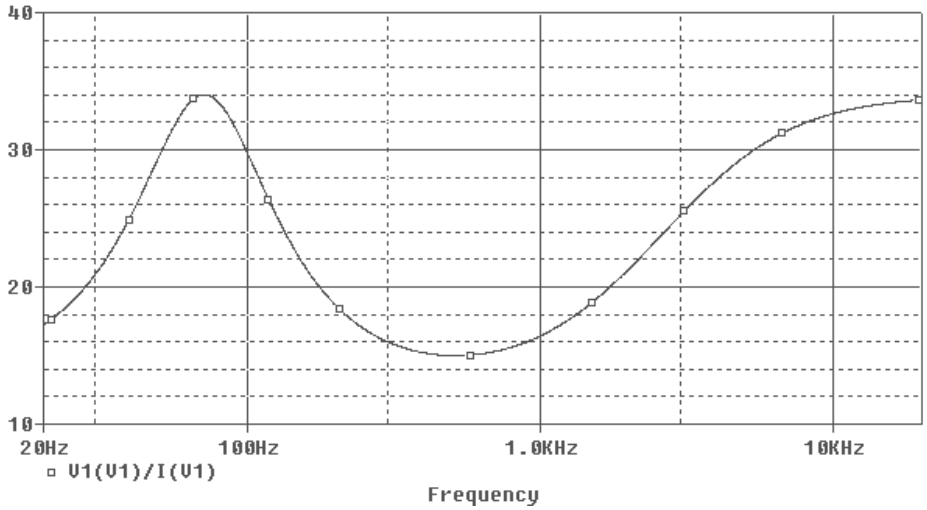

Figure 3.12: Speaker Model Impedance vs Frequency

Chapter 4

SIMULATION RESULTS

4.1 Class AB Amplifier Characterization

The Class AB Amplifier was the first circuit to be characterized. For offset voltage and NDRV and PDRV gain, an open loop configuration was used. The open loop testbench is shown in figure 4.1. By using a large capacitor and inductor, the DC biasing can be set for midband output while allowing a differential AC signal to be added. The rest of the simulations used a unity gain configuration. The testbench for this case is shown in figure 4.2. The important measurements for this amplifier are listed in table 4.1.

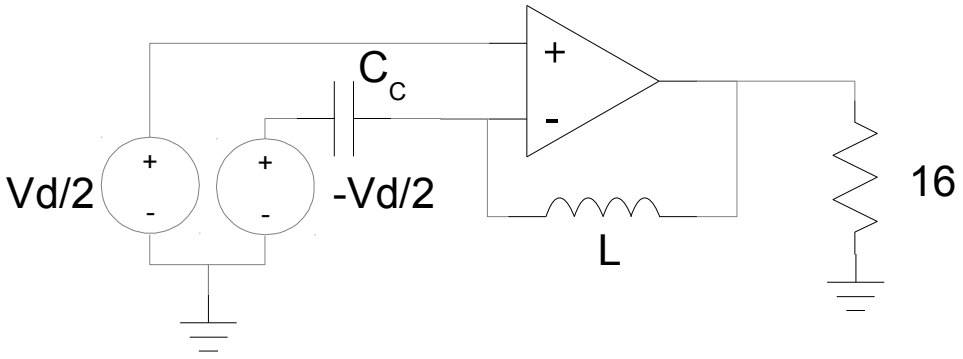

Figure 4.1: Class AB Output Testbench

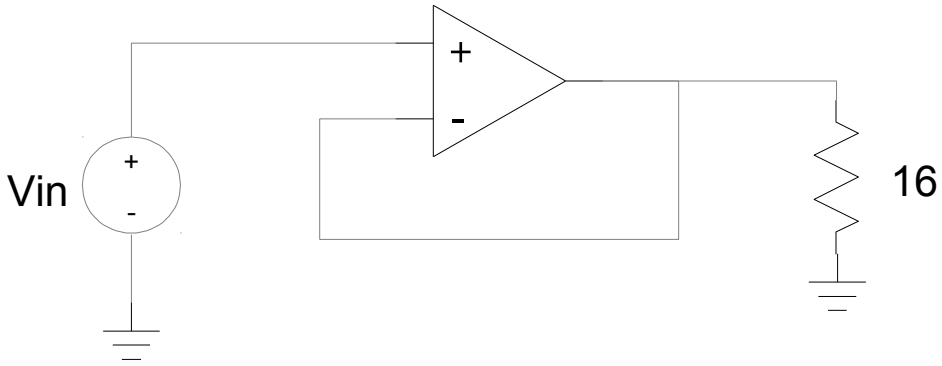

Figure 4.2: Class AB Output Testbench

Table 4.1: Table of Class AB Amplifier Measured Characteristics

Specification	**Performance**
Quiescent Power	1.575mW
Output Gain	-4.44mdB
DC Offset	-8.063uV
Closed Loop Gain	-4.44mdB
PSRR @ 20kHz	92dB
Pout @ 0.1% THD	105mW
Impedance	16Ω
Input Referred Noise	$16.23nV/\sqrt{Hz}$
Dynamic Range	115dB

A common measure of the properties of an amplifier is its response to a step input. This helps to give information on its stability as well as as its phase margin. The step response to a 200kHz square wave is shown in figure 4.3. There is some slight ringing at the N (falling) side, which shows that it is an underdamped system, but only by a small margin. The overshoot is less than 5% of the total step distance. The N side also shows slewing, which is to be expected when driving such a heavy load. The P (rising) side is overdamped, and shows some distortion. This is not a large problem, as the maximum frequencies used in this circuit are 20kHz signals, much slower than the 200kHz square wave being tested.

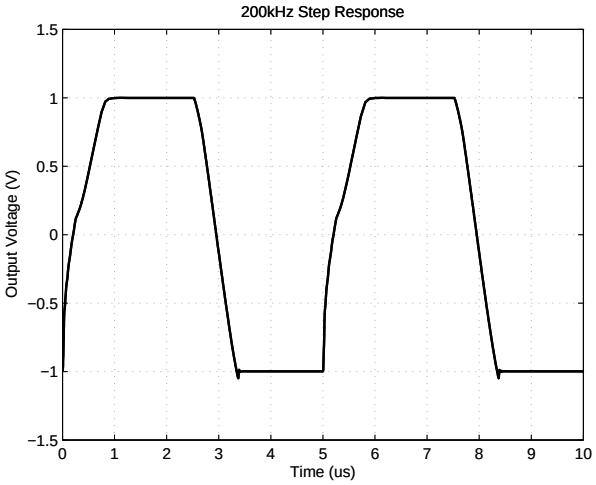

Figure 4.3: 200 kHz Step Response

The next figure shows the gain on the NDRV and PDRV signals. The PDRV signal gain is significantly smaller than the NDRV gain. This is most likely due to one or more of the devices on the PDRV side not operating in the saturation region. The gain for this signal could be improved in the future to increase the performance of this amplifier.

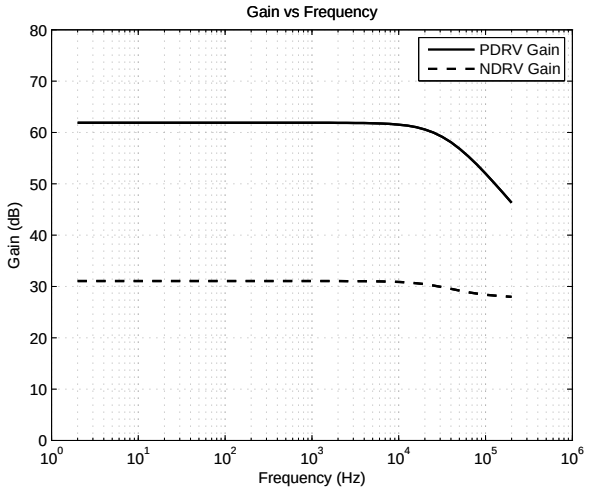

Figure 4.4: NDRV and PDRV Gain vs Frequency

The noise of this amplifier is fairly standard for a device at room temperature. The noise power over the audio spectrum is equal to -112.7dB. With a 1Vp input signal, this gives 106dB of SNR, which is acceptable for a low voltage audio amplifier.

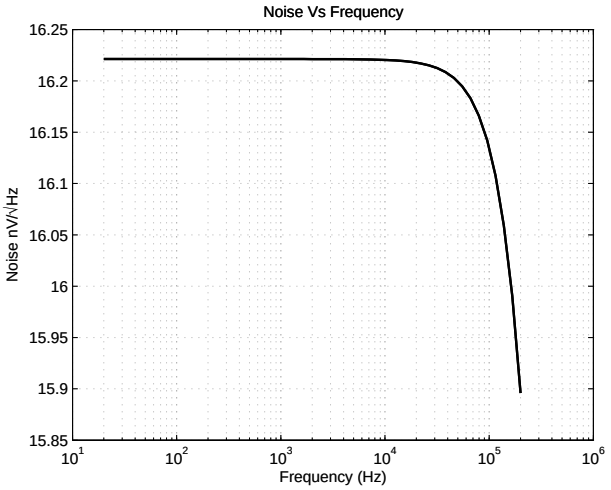

Figure 4.5: Amplifier Input Referred Noise vs Frequency

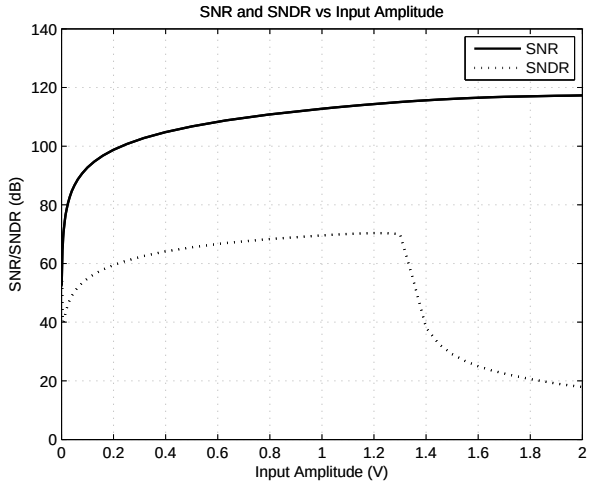

Figure 4.6: Class AB SNR and SNDR vs Input Amplitude

The PSRR of this amplifier is excellent over the entire audio band. It maintains up to 92dB of PSRR past 100kHz. This PSRR was tested on both of the amplifier's positive supplies. This PSRR will help to reduce any distortion that will be added after connecting the device to the modulated supply rail.

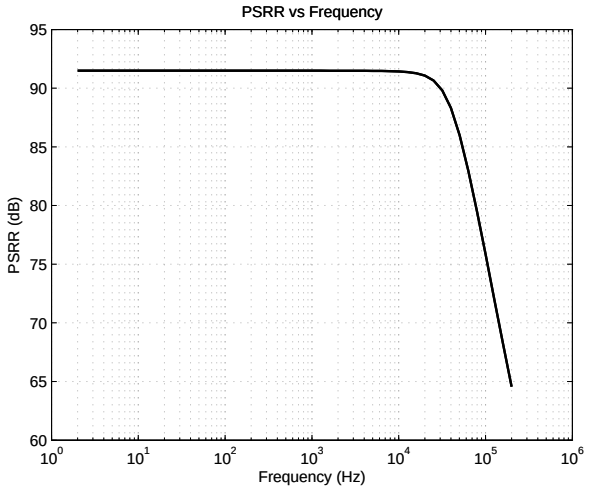

Figure 4.7: Class AB PSRR

The amplifier has average distortion performance. It can output up to 53mW at less than 0.1% distortion. The Worst case is the 20kHz distortion at 0.0985%, while the 1kHz distortion is only 0.0355%. At this power output, the amplifier starts clipping, resulting in an increase in distortion at higher powers. Distortion was measured up to 200kHz.

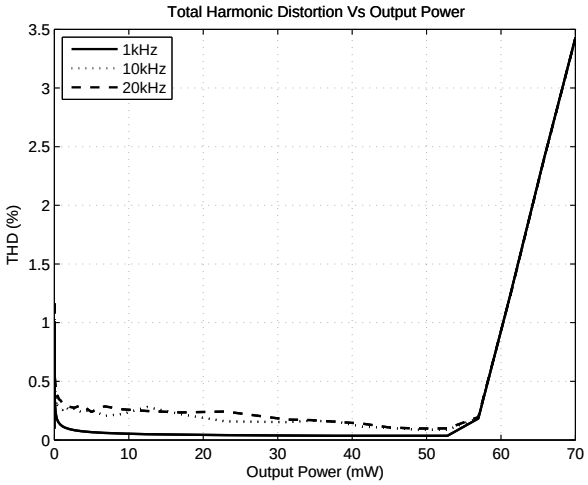

Figure 4.8: THD vs Output Power

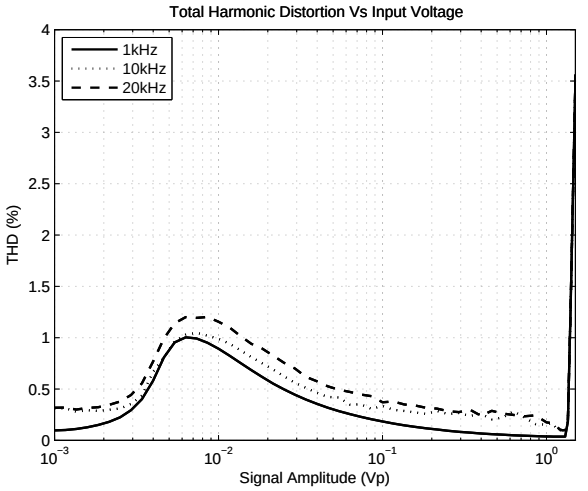

Figure 4.9: THD vs Input Voltage

The efficiency of this amplifier is average as well. It has a very low quiescent power at 1.575mW, which helps to increase the efficiency at lower input voltage. It reaches 36% efficiency at it's maximum undistorted output of 53mW and peaks at around 44% efficiency. This limit is due to the maximum current drive capability of the amplifier.

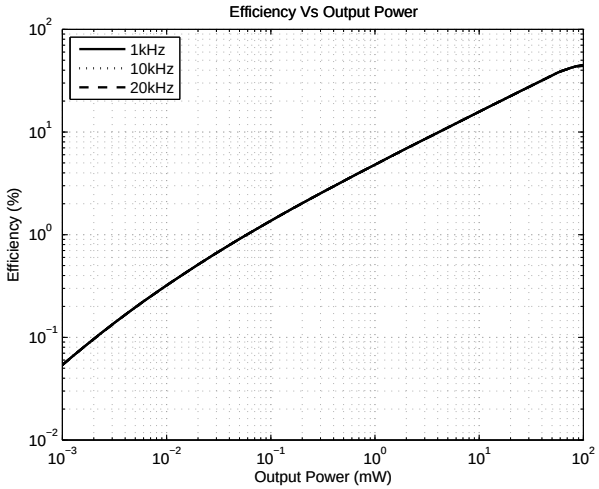

Figure 4.10: Efficiency vs Input Voltage

In order to judge this amplifier's potential performance as a Class H amplifier, the supply voltage was simulated with increasingly lower voltages, monitoring the efficiency and THD of the amplifier. A 1Vp signal at 20kHz was used as a test input. These plots of efficiency and THD are shown in figures 4.11 and 4.12. The maximum efficiency occurs at 1.5V with an efficiency of 33.8%. It drops at lower supply voltages due to the decreased output power from distortion. The THD of the amplifier increases drastically below 1.6V. Since the offset from the signal for the Class H supply is a little above 0.6V, this circuit will be able to operate at the designed level.

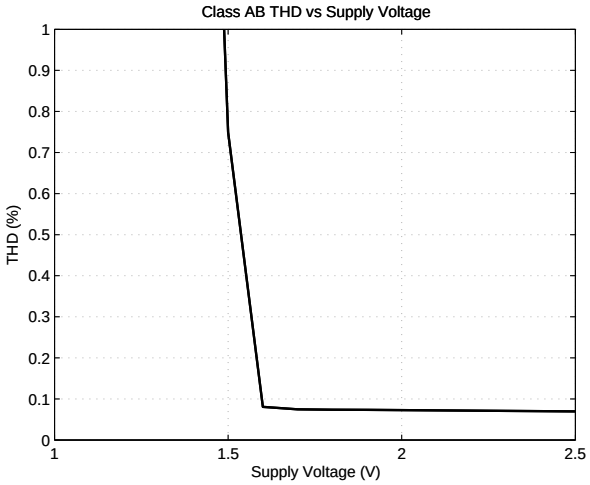

Figure 4.11: THD vs Supply Voltage

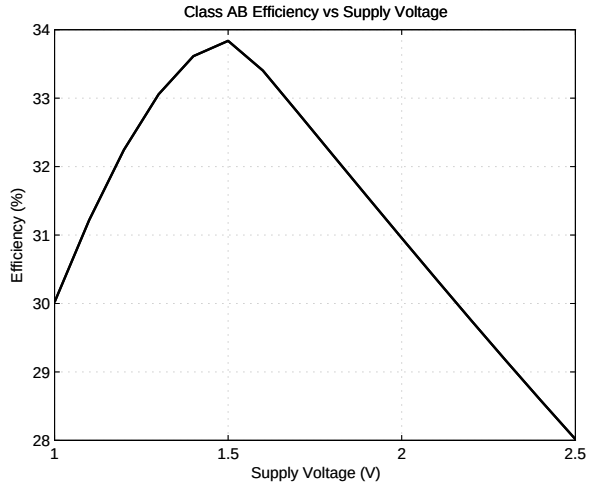

Figure 4.12: Efficiency vs Supply Voltage

4.2 Class H Supply Characterization

The Class H supply generator is a multiphase buck converter with a slow and fast phase. These two phases help to increase the responsiveness of the buck converter to rapidly changing loads of the Class AB amplifier. The fast phase has a lower efficiency but a faster response time. The slow phase has a higher efficiency, but

slower transient response time. By alternating which phase becomes active, the system can respond at twice the rate of just a single system. The transient respose of the system to a 20kHz input signal is shown in figure 4.13.

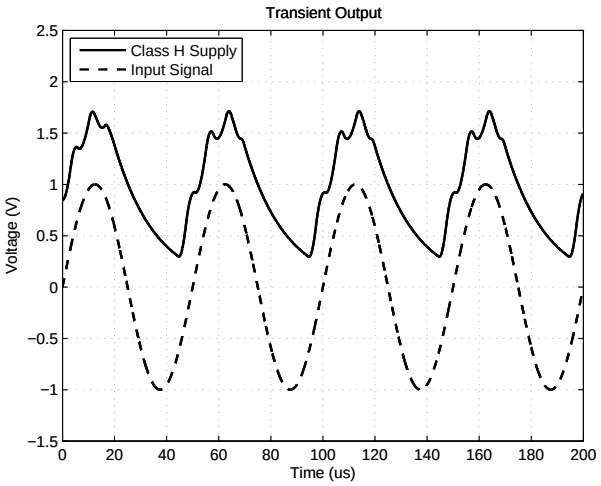

Figure 4.13: Transient Output

The supply was also tested for stability and overvoltage cases. A 20kHz square wave was input to the supply with a 2Vpp swing centered at 0V while driving a 32 Ohm load. The input signal and response are shown in figure 4.14.

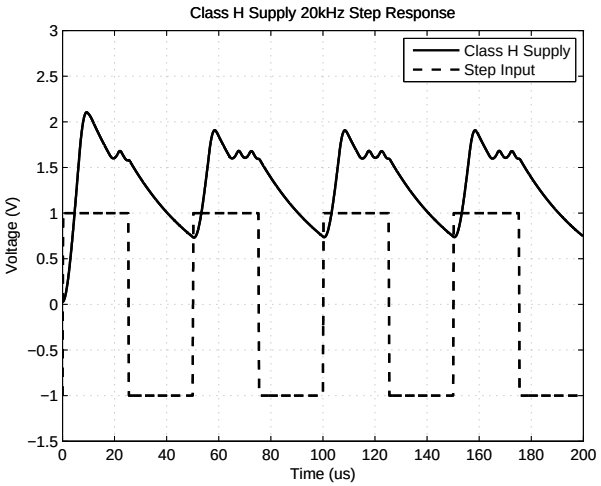

Figure 4.14: Class H Step Response with 32Ω Load

The supply was tested for its power efficiency versus output steady state voltage. This was tested at both 16Ω and 32Ω. The efficiency plots for these two loads is shown in figure 4.15. The efficiency reaches a maximum around 90% at 1.9V Output.The efficiency at the upper end is very good for a constant voltage signal, but will most likely degrade when supplying a changing load.

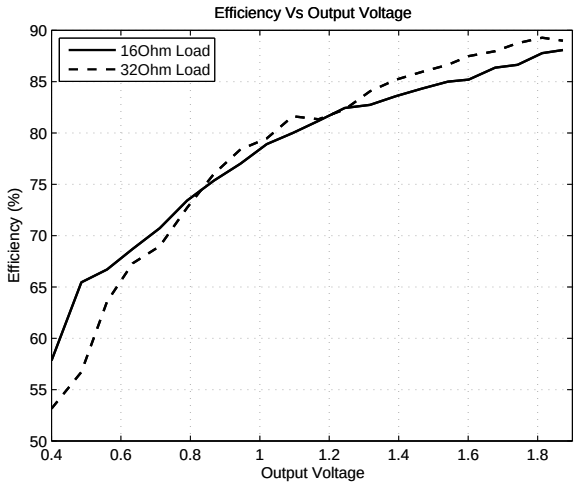

Figure 4.15: Efficiency vs Output Power at 16,32

4.3 Combined Class H Amplifier Results

The testbench for the combined Class H amplifier is shown below in figure 4.16. Ideal DC sources were used for biasing the Class AB amplifier. The input signal is sent to an offset generator, which is fed to the Class H supply generator. This supply goes to the Class AB amplifier. The Class AB amplifier is in a unity gain configuration with the 16Ω load attached to the output.

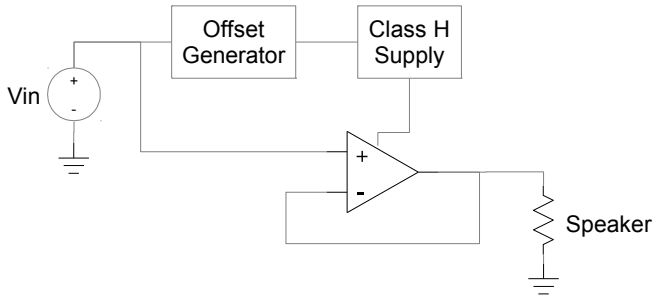

Figure 4.16: Class H Testbench

The input was tested for sine waves with frequencies of 10kHz and 20kHz, and amplitudes ranging from 0.01Vp to 2Vp. Simulations were run for 25us to start at the steady state response from the buck converter, and then recorded for 100us to measure the THD and efficiency over 1 and 2 cycles of the 10kHz and 20kHz signals respectively. Input amplitude sweeps of a 1kHz signal were omitted due to simulation space requirements. The transient response to a 1Vp 1kHz signal is shown in figure 4.17. The Efficiency at this point was 37%, with a THD of 49.45m%.

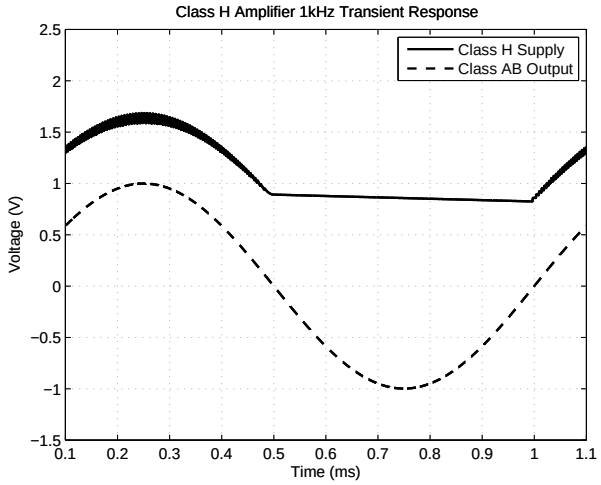

Figure 4.17: Class H 1kHz Transient Response

The Class H amplifier operates very well over the designed specifications range. The amplifier does tend to have increased distortion at lower power output than the Class AB amplifier did. It reaches about 32mW before increasing above 0.1%THD. This increase is due to the supply noise appearing during the maximum output voltage. This causes a large 3rd order harmonic, which increases the THD quickly. More headroom or a higher capacitance on the output could help to reduce this ripple, but at the cost of efficiency.

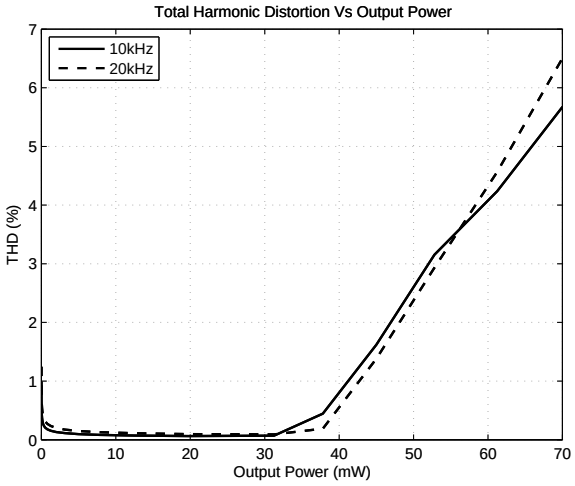

Figure 4.18: THD vs Output Power

The THD of a 10kHz tone of the two amplifiers was compared to show the differences in THD of the two amplifiers. The Class H amplifier actually has slightly better THD than the Class AB over most of the output power range. Once the Class H amplifier starts having clipping distortion at 30mW, it increases in THD very rapdily, while the Class AB maintains its low THD out until 50mW. The lower THD of the Class H may be caused by the lower source voltage of the output transistor, causing an increased quiescent current, which reduces the crossover distortion. The Class AB amplifier starts clipping after the Class H amplifier, which explains the THD for the Class AB amplifier not increasing until 50mW output power.

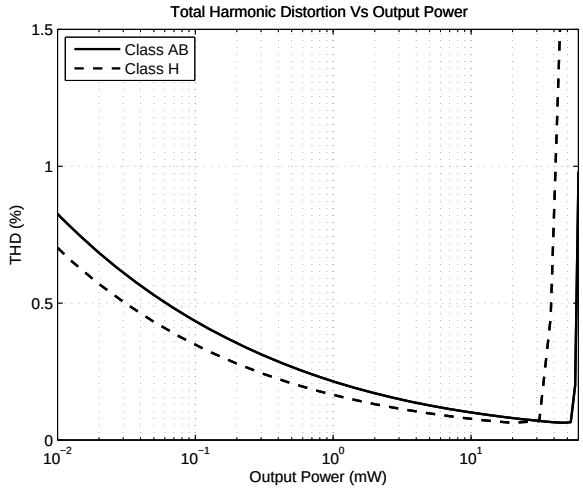

Figure 4.19: THD vs Output Power: Comparison of Class AB and Class H

The efficiency of this amplifier is an improvement over the standard Class AB design. At the target specification of 30mW, it has an efficiency of 35%. This a 7% increase over the Class AB amplifier's 28% efficiency. The efficiency stays high for lower output powers as well. It maintains at least a 5% increase in efficiency above the Class AB amplifier down to 5mW. This is shown in figure 4.21.

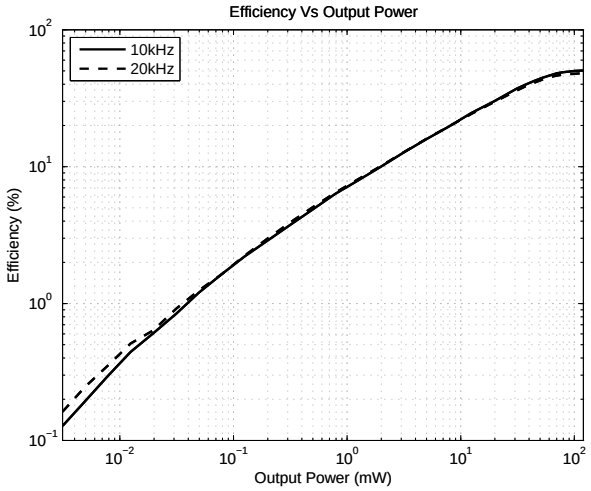

Figure 4.20: Efficiency vs Output Power

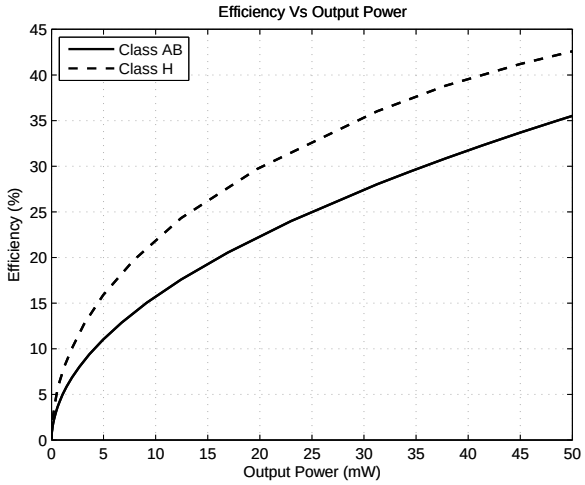

Figure 4.21: Efficiency vs Output Power of Class AB and Class H at 20kHz.

The THD increases after 30mW because the headroom on the ouput transistors drops below its minimum of 0.6V. This is partially due to the response time of the Class H supply, and partially due to the ripple on the supply. The supply voltage, output, and headroom are shown in figure 4.22.

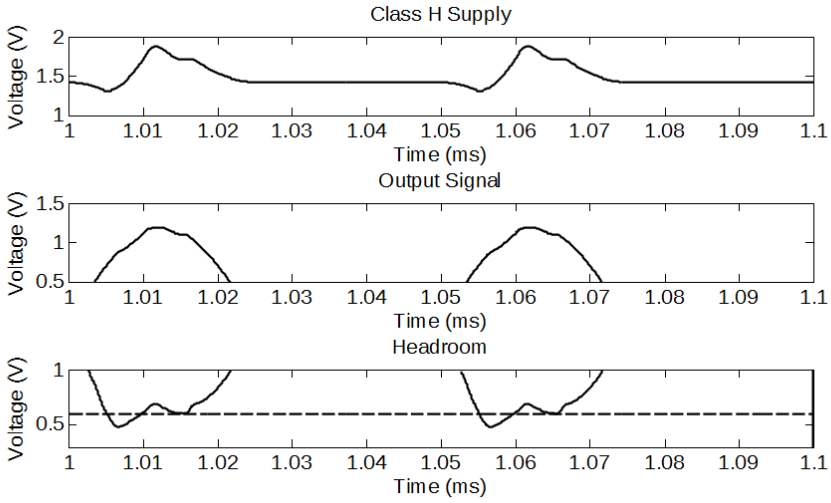

Figure 4.22: Class H THD Causes

Due to limitations in simulation space and time for the full circuit, a simplified version was built in SPICE. Using nonideal components for the Class H supply and an ideal Class AB amplifier, 1 second of a song was used as an input for the circuit. The output was plotted along side the input, and both were saved as wav files. The waveforms for a portion of the signal are shown below in figure 4.23.

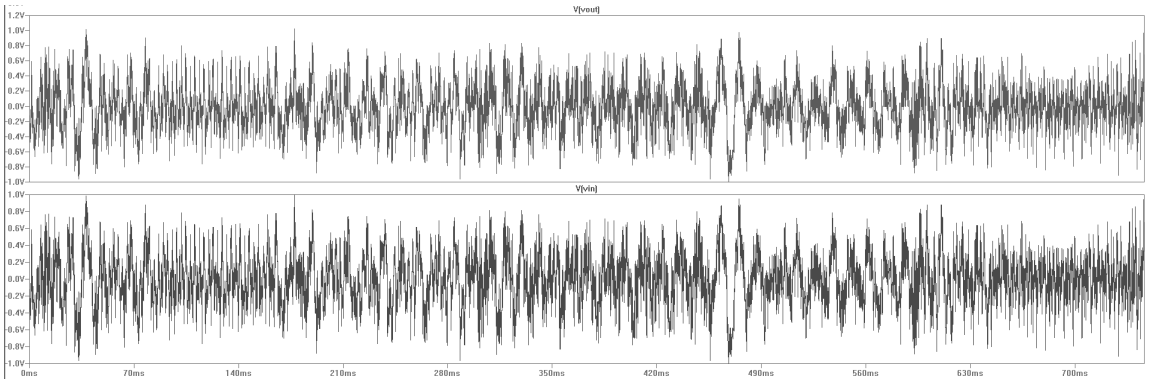

Figure 4.23: Simplified SPICE Simulation Input and Output Waveforms

As this figure shows, the output approximately replicates the input signal. In order to determine if there is any increased noise or distortion, an FFT of a small portion will have to be used. The FFT of the input and output is shown below in figure 4.24. These FFTs were taken using 512 samples at 44.1kHz.

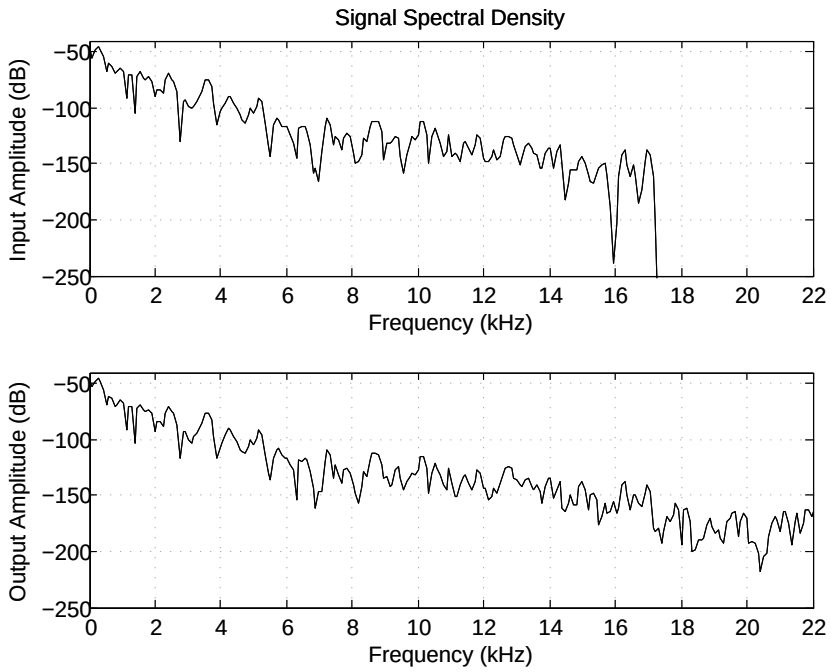

Figure 4.24: Simplified SPICE Simulation Input and Output Spectral Densities

These two FFTs are very similar, but there are discrepancies. Some of the peaks don't drop as low as others do. This is due to the increased noise present in the signal. It also shows up at higher frequencies, increasing the noise floor. The best way to determine if this change is noticeable is to compare the two signals in a side by side listening test. Using a pair of headphones, I was unable to notice any distortion or increase in noise for the 1 second clip.

Chapter 5

CONCLUSION

A high PSRR Class AB amplifier and a Class H amplifier were designed in a 0.24um process for portable audio applications. By using a multiphase buck converter, the efficiency of the Class h amplifier was increased while still maintaining a fast enough response time to respond to audio frequencies. The Class H amplifier successfully increased the efficiency of a Class AB amplifier by a significant amount without affecting the THD at the design specifications. The final Class H amplifier design met all design specifications and showed adequate performance across a wide range of input frequencies and amplitudes. It was able to output 30mW into 16Ω without a large increase in THD. For portable applications, 30mW is enough power to drive 16Ω headphones to a reasonable volume, so the reduction in maximum undistorted output compared to the Class AB is an acceptable tradeoff.The comparison of the two amplifiers designed is shown in detail in table 5.1.

Table 5.1: Amplifier Comparison Summary

Specification	Class AB	Class H
Quiescent Power	1.575mW	2.941mW
PSRR @ 20kHz	92dB	92dB
Output Power at 0.1% THD	52mW	32mW
Average Efficiency at 1Vp	28%	36%
Total Size	$1170um^2$	$1720um^2$

The Class AB is superior in THD and power output capabilities, but these come at the cost of power efficiency. As figure 4.21 showed, the Class H amplifier was over 5% more efficient than the Class AB amplifier between 5mW to 30mW.

To further improve this design, additional circuitry could be added to the Class H supply in order to increase efficiency even further. The size of inductors used in the buck converter were limited by the transient attack and current

overshoot of the design. When the input signal changed rapidly, a large change in current needs to be generated to keep up with the input, but this causes large oscillations in the output voltage. A current sensing feedback system could help to increase efficiency by allowing the system to use a larger inductance, but limiting the maximum current supplied in order to prevent large oscillations in the output supply voltage. These oscillations were the primary cause of THD in the Class H architecture, so reducing them will allow for higher power output, higher efficiency, and lower THD.

A different architecture with a higher open loop gain such as the design presented in [4] could help to reduce the supply oscillations on the output as well. By increasing the open loop gain, the power supply rejection ratio of the amplifier is increased, leading to reduced harmonics from the supply leaking through to the output. Another option would be to use an H-bridge ouptut. This would allow for a single supply architecture to be used and increase the efficiency gains.

Though there were some drawbacks to the Class H architecture designed, these can be further reduced by adding additional circuitry or changing the architecture. These designs all have more complexity than the simple design shown in this thesis. The Class H amplifier shown was successful in supplying 30mW of power for signals across the audio frequency range without an increase in THD at an improved efficiency compared to a standard Class AB amplifier with the same supply voltage.

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