MESFET Optimization and Innovative Design for High Current Device Applications

by

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ABSTRACT

There will always be a need for high current/voltage transistors. A transistor that has the ability to be both or either of these things is the silicon metal-silicon field effect transistor (MESFET). An additional perk that silicon MESFET transistors have is the ability to be integrated into the standard silicon on insulator (SOI) complementary metal oxide semiconductor (CMOS) process flow. This makes a silicon MESFET transistor a very valuable device for use in any standard CMOS circuit that may usually need a separate integrated circuit (IC) in order to switch power on or from a high current/voltage because it allows this function to be performed with a single chip thereby cutting costs. The ability for the MESFET to cost effectively satisfy the needs of this any many other high current/voltage device application markets is what drives the study of MESFET optimization.

Silicon MESFETs that are integrated into standard SOI CMOS processes often receive dopings during fabrication that would not ideally be there in a process made exclusively for MESFETs. Since these remnants of SOI CMOS processing effect the operation of a MESFET device, their effect can be seen in the current-voltage characteristics of a measured MESFET device. Device simulations are done and compared to measured silicon MESFET data in order to deduce the cause and effect of many of these SOI CMOS remnants.

MESFET devices can be made in both fully depleted (FD) and partially depleted (PD) SOI CMOS technologies. Device simulations are used to do a comparison of FD and PD MESFETs in order to show the advantages and disadvantages of MESFETs fabricated in different technologies. It is shown that PD MESFET have the highest current per area capability.

Since the PD MESFET is shown to have the highest current capability, a layout optimization method to further increase the current per area capability of the PD silicon MESFET is presented, derived, and proven to a first order.

DEDICATION

To God, my parents, and my wife for everything.

ACKNOWLEDGMENTS

Dr. Trevor Thornton for making my M.S. degree possible.

TABLE OF CONTENTS

Page

LIST OF TABLES

LIST OF FIGURES

PREFACE

The majority of this thesis is presented so that a proper understanding of the second half of the final chapter, where a new layout technique for partially depleted MESFETs to increase the current per unit area is presented, is fully and properly understood.

CHAPTER 1

INTRODUCTION

There are two different types of depletion mode MESFET devices: partially depleted (PD) and fully depleted (FD). Though there are many tradeoffs between PD and FD MESFETs in terms of area, performance, and ease of integration, the threshold voltage of PD MESFETs is set by the technology that they are fabricated in and cannot be changed by anyone other than a process engineer, while changing the threshold voltage of a FD MESFET can easily be done by a circuit designer by altering the layout of the device. The ability to choose between a MEFSET device with a very large current drive or a MESFET device with an accurately controllable threshold voltage and have MESFETs with different threshold voltages on the same chip is a very important in order for MESFETs to become considered competitive high current/voltage transistors.

1.1 MESFET STRUCTURE

1.1.1 Partially Depleted

Unlike a silicon MOSFET, a MESFET is a majority carrier device. Depending on the process it is fabricated in a MESFET may be considered either a three or four terminal device. In contrast to MESFETs made in GaAs technologies, most of which are effectively three terminal devices, the majority of silicon MESFETs are four terminal devices. Though MESFETS may be made with bulk silicon technologies [1-3], all MESFETs mentioned in this thesis are made with SOI technology. Conceptual images of a generic SOI PD MESFET can be seen in Figure 1 through Figure 3 [4].

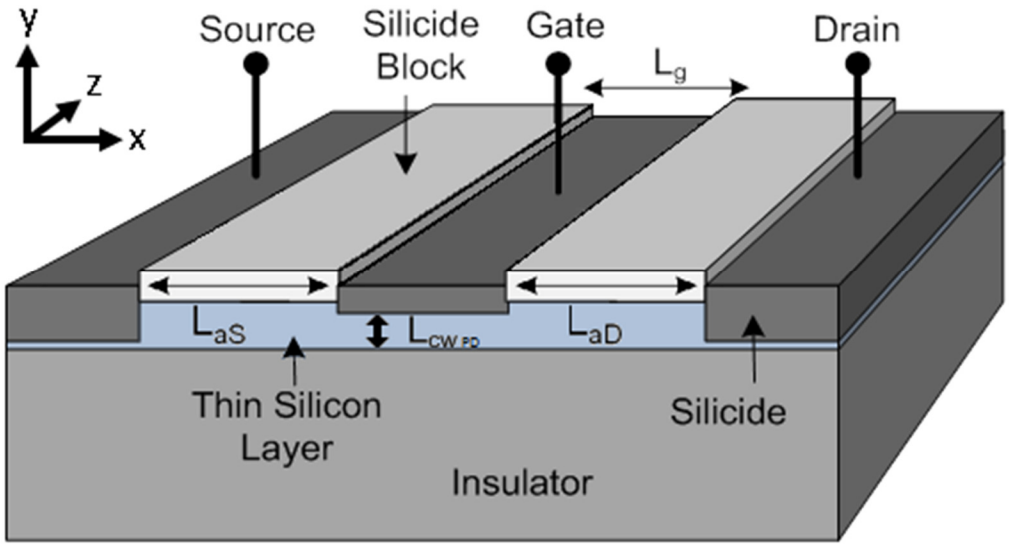

Figure 1: Basic Partially Depleted MESFET Device Structure [4] (© 2011 William Lepkowski)

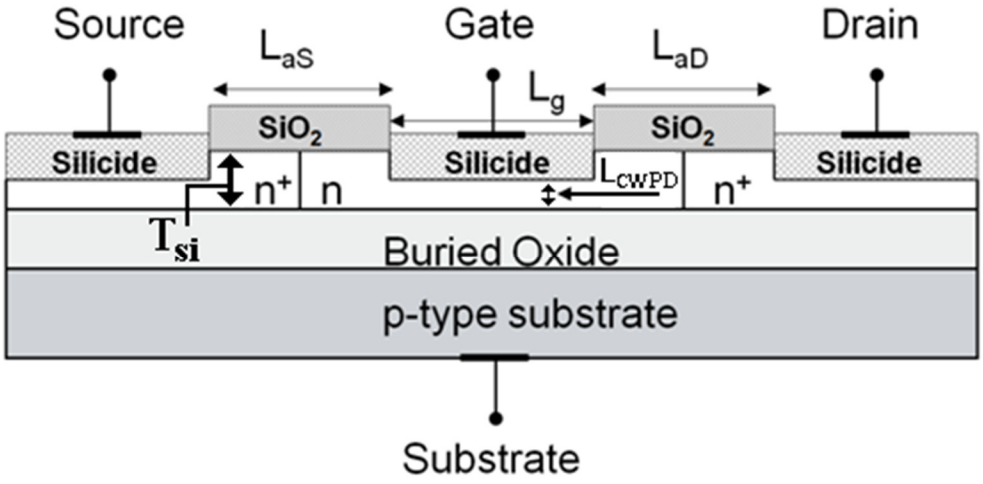

Figure 2: Basic Partially Depleted MESFET Device Structure Cross Section [4] (© 2011 William Lepkowski)

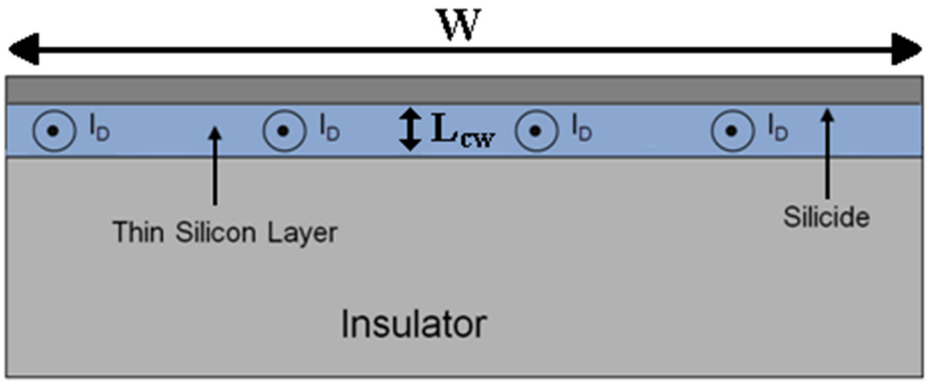

Figure 3: Single Channel of Partially Depleted MESFET Looking Down Channel [4] (© 2011 William Lepkowski)

Though it appears that it is a three terminal device from the pictures, few technologies have a buried oxide layer (BOX) thick enough to prevent a potential that is applied to the substrate contact from significantly influencing the carrier concentration/ electric field at the bottom of the device enough not to consider the substrate contact a terminal. In this thesis the substrate terminal will not be included in any of the discussions and it will always be assumed that it is at the exact same potential as the source terminal.

Whether or not the substrate contact is considered a terminal, the three terminals on the top of the device in Figure 2 are the main terminals of the device; the gate, the source, and the drain. The gate, source, and drain must all be physically separated in order for the device to be fully controllable and work properly. In addition to the active silicon separating all three contacts, they are also electrically and physically separated by islands of silicon dioxide (SiO_2) as an artifact of the fabrication process. The SiO_2 separating the contacts on the top of the device may or may not be recessed into the T_{si} layer depending on how the devices were laid out. All three contacts are made of silicide. All of these contacts are connected to the main thin film silicon layer (T_{si}) which ends at the BOX.

As seen in Figure 2 the gate-drain separation (L_{ad}) is defined as the physical distance from the drawn edge of the drain contact closest to the gate to the drawn edge of the gate contact closest to the drain. The gate-source separation (L_{as}) is defined as the physical distance from the

drawn edge of the source contact closest to the gate to the drawn edge of the gate contact closest to the source. The gate length (L_g) is defined as the drawn length of gate contact from the edge of the gate nearest to the source to the edge of the gate nearest to the drain. The channel width (L_{cwPD}) is defined as the physical distance from the bottom of the gate silicide to the top of the BOX (the bottom of the T_{si}).

1.1.2 Fully Depleted

A 3D rendering of a generic SOI FD MESFET can be seen in Figure 4. Fully depleted MESFETs have the same main terminals that PD MESFETs have: gate, source, and drain. They usually also have substrate terminals (not shown in Figure 4). Unlike a PD MESFET, a multi-channel FD MESFET uses part of two separate gate contacts to control each device channel. Although two gate contacts per channel are not necessary to make a single channel FD MESFET, they are necessary to make a device that has more than one channel. Almost all FD MESFET applications will require a multi-channel MESFET. The majority of the FD MESFET devices that are talked about in this thesis will be multi-channel devices.

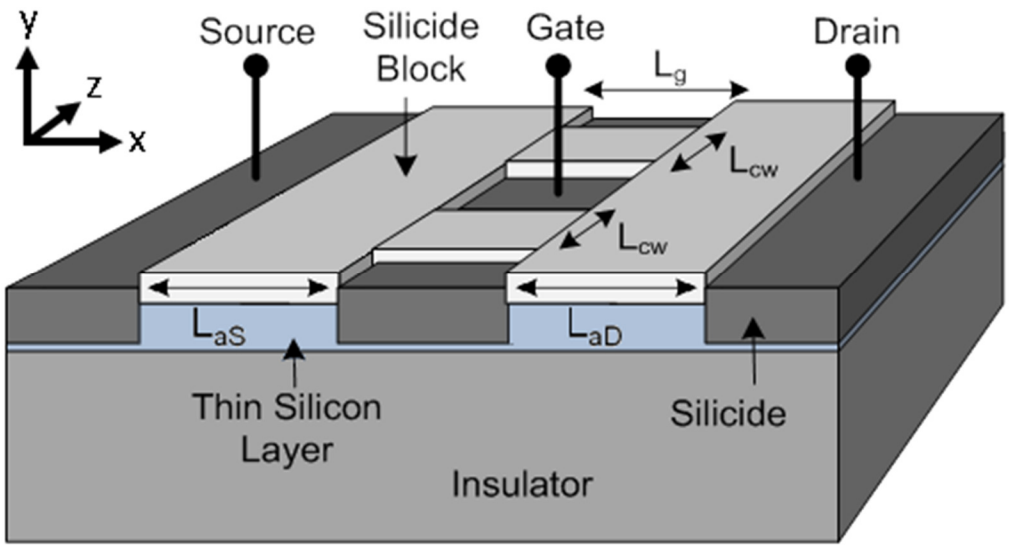

Figure 4: Basic Fully Depleted MESFET Device Structure [4] (© 2011 William Lepkowski)

Although the FD MESFET in Figure 4 is may appear to be complicated it is no more complex than a PD MESFET and for all first order calculations can often be considered a 2D device for modeling purposes when the change in variables that relate to the currents and voltages in the device in the y direction are minimal.

All of the main contacts are separated by active silicon and SiO2 and are connected to the T_{si} which is truncated by the BOX just as they are in a PD MESFET. While L_{ad}, L_{as}, and L_g are defined exactly the same way for a two-gated FD MESFET as they are for a PD MESFET, the definition of L_{cwFD} is different. The channel width (L_{cwFD}) for a two-gate FD MESFET is defined as the separation between the drawn channel-touching edge of a gate to the closest drawn edge of the other gate bounding that same shared channel. Note that in general and in the majority of this thesis the channel width of either/both MESFET types will be referred to simply as L_{cw} unless additional specificity is necessary. Also, the term L_{cw} will be redefined later for the FD MESFET device to be more accurate in terms or electrostatics. A cross section of Figure 4 in the y-z plane is visualized in Figure 5. It shows what the FD MESFET in Figure 4 looks in the direction of current flow.

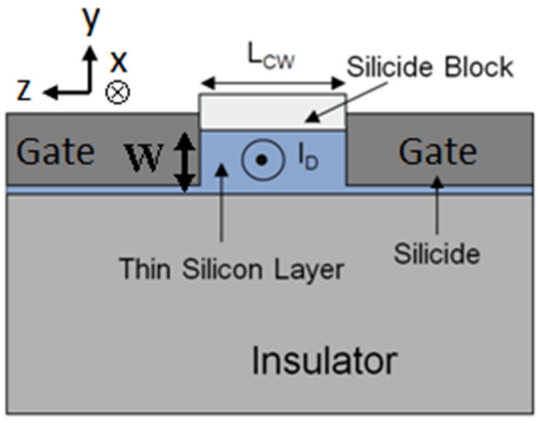

Figure 5: Single Channel of Fully Depleted MESFET Looking Down Channel
[4] (© 2011 William Lepkowski)

1.1.3 Partially/Fully Depleted

Figure 6 is a 3D rendering of a generic partially/fully depleted (P/FD) MESFET. All of the main contacts and the definitions of L_{ad}, L_{as}, and L_g are the same as they are in a FD or PD MESFET. The difference between a FD MESFET and a P/FD MESFET is the thickness of the T_{si} layer (illustrated in Figure 6 and Figure 7), the doping of the T_{si} layer, and the type of metal used to form the gate silicide. This means that although the definition of L_{as}, L_{ad}, and L_g are the same for a P/FD MESFET as they are for PD and FD MESFETs, L_{cw} is now defined as a hybrid of the PD MESFET L_{cw} and the FD MESFET L_{cw}. This makes L_{cw} overall an ill-defined and useless parameter for a P/FD MESFET as it will not be able to be used as a tool for comparing the performance of a P/FD MESFET to a PD or FD MESFET.

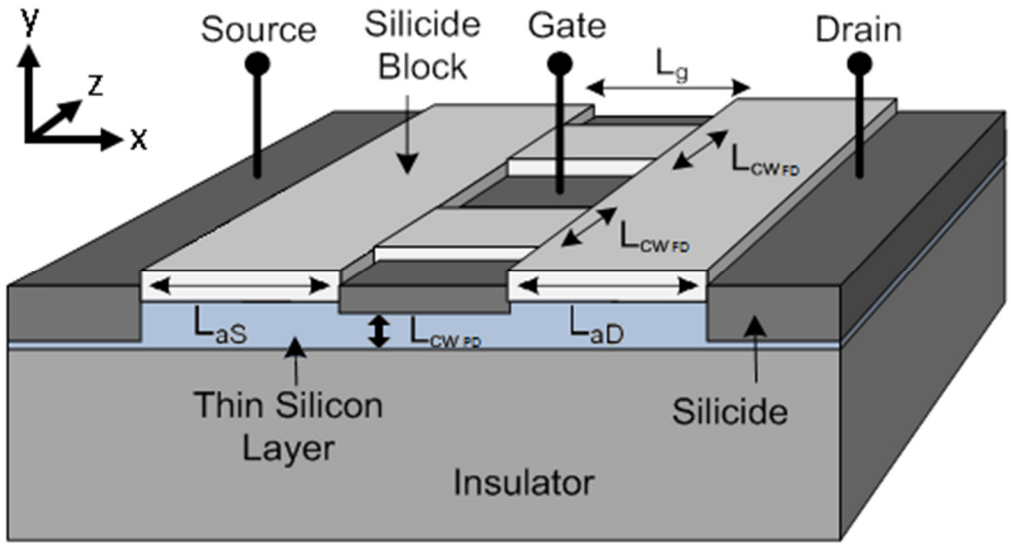

Figure 6: Single Channel of Hybrid P/FD MESFET Looking Down Channel [4]
(© 2011 William Lepkowski)

A cross section of Figure 6 in the y-z plane is visualized in Figure 7. It shows what the P/FD MESFET in Figure 4 looks in the direction of current flow. When compared to Figure 5 it is easy to see what may geometrically differentiate a FD and P/FD MESFET.

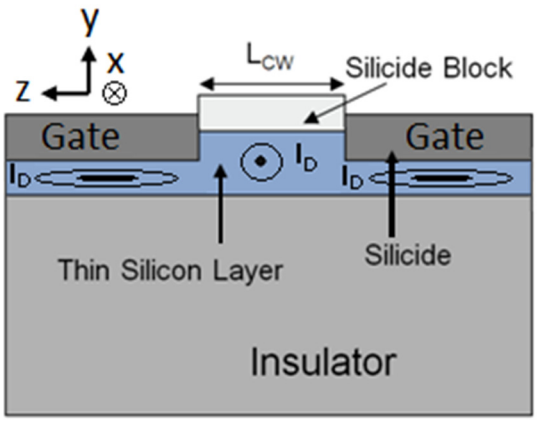

Figure 7: Single Channel of Hybrid P/FD MESFET Looking Down Channel [4]
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1.1.4 Current Structures

We have successfully designed MESFETs in 5 different CMOS processes: the MIT-LL 1D process (200nm minimum feature size), the MIT-LL 3D process (200nm minimum feature size), the Honeywell S150 process (150nm minimum feature size), the Honeywell MOI5 process (350nm minimum feature size), the Peregrine GC SOS process (600nm minimum feature size), and a SPAWAR process. We also have designs that are in the process of being fabricated in the IBMRF07 process (180nm minimum feature size) and the IBM12SO process (45nm minimum feature size).

From the processes that we have already received our designs in, we have ended up with both FD and PD MESFETs. The Peregrin and MIT-LL technologies yield FD MESFETS due to their light active silicon doping and thin T_{si} layer and the Honeywell, SPAWAR, and IBMRF07 technologies yield PD MESFETS. We predict that the IBM12SO may have the controllable capability of yielding all three types of MESFET due to thickness of the T_{si} layer and the different active silicon well dopings offered.

1.2 MESFET FABRICATION

1.2.1 Integration Into Standard Process Flow

Due to the time it can take to attain design waivers and the complexity and problems that breaking process rules can create, the ability to integrate a MESFET into the standard CMOS SOI process flow is absolutely imperative in order to deem the development of silicon MESFETs as feasible. An extensive knowledge of the CMOS processing steps and fabrication flow has allowed us to integrate MESFETs into over 5 different CMOS SOI technologies without the need for any design waivers.

The differences in key fabrication steps of an n channel MOSFET and an n channel MESFET can be seen in Figure 8. The differentiation of a MESFET from a MOSFET begins after the shallow trench isolation (STI) step (local oxidation of silicon (LOCOS) for older processes) seen in Figure 8a. The STI step isolates each devices active area from every other devices active silicon region. It does so by etching through the T_{si} to the BOX to create a trench and then depositing a fill oxide in every trench. Generally, after this step the MOSFET gate oxides are grown, the MOSFET gate polysilicon is deposited, and the MOSFET gates are patterned. Though MESFET structures must endure these steps when they are fabricated on a wafer with MOSFETs (Figure 8b), they are not part of the MESFET fabrication flow and the MESFET structure will not be affected if these processing steps are not performed. In modern processes the next step is to do a shallow lightly doped drain/source (LDD/S) doping diffusion. It will be seen that this will not affect the operation of a PD MESFETs but will affect the operation of a FD MESFET and therefore will require some attention. After the LDD/S diffusions the next step in the fabrication process as seen in Figure 8c is the plasma-enhanced chemical vapor deposition (PECVD) of the silcide block (SBLK) oxide. For the MESFET structure the formation of the SBLK oxide is the most critical step in the fabrication of a silicon MESFET as the SBLK oxides dimensions will completely define the L_{ad}, L_{as}, L_{cw} (for a FD MESFET), and L_g parameters and these parameters are the only designer-controllable design parameters in the fabrication of a silicon MESFET. For the MOSFET structure the SBLK oxide will act as a spacer between the gate oxide contact and the

drain/source contacts and as a blocking layer for the deep source/drain implants. Before the next processing step where both the MOSFET and the MESFET receive their final deep drain/source implants as depicted Figure 8d, the MESFET must have a layer of photoresist deposited across the top of its channel region. While the MOSFET's polysilicon acts as a blocking layer to prevent the MOSFET channel and gate oxide from receiving the heavy source/drain doping, the MESFET's channel region is unprotected and therefore requires a protective layer of photoresist to prevent the doping from reaching the MESFET's channel. After the deep source/drain implants are done, a layer of metal is deposited across the entire wafer through sputtering for use in the final front end of line (FEOL) processing step (in modern VLSI processes) [5]. The final step before the back end of line (BEOL) processing begins, which is identical for a MOSFET and a MESFET, is the formation of the silicides depicted in Figure 8e. This will be discussed in depth in chapter three as it is central to the operation of the MESFET device.

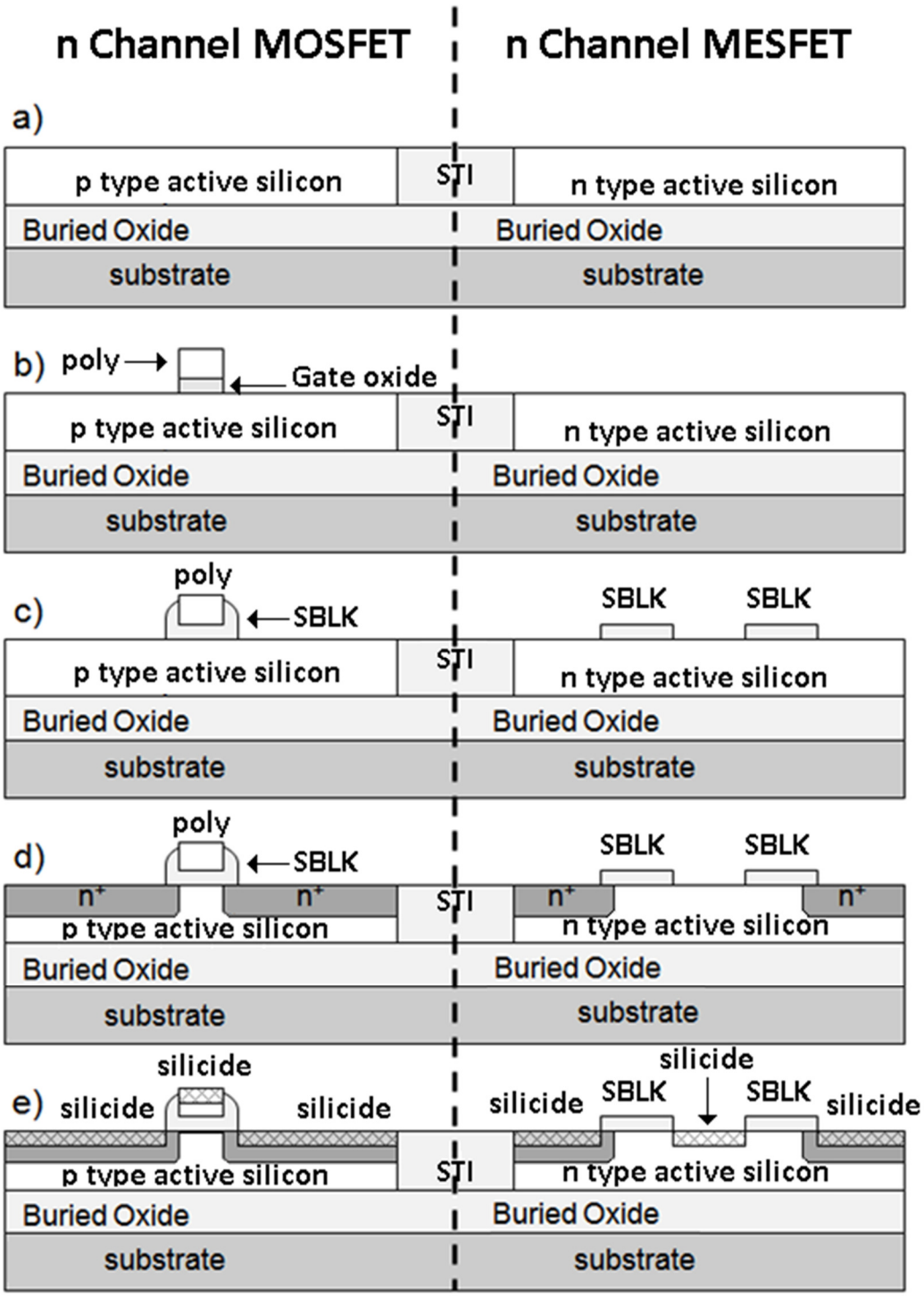

Figure 8: Fabrication Steps During Integration of a MESFET into a Standard CMOS SOI Process [4] (© 2011 William Lepkowski)

1.3 MESFET OPERATION

1.3.1 Regions of Operation

Like the MOSFET, a MESFET device had three regions of operation: cutoff, linear, and saturation. Although the border between these regions may be ill-defined in literature since the mechanisms of MESFET operation differ significantly from the MOSFET mechanisms of operation, I will explain how the different regions of operation can be differentiated from an electrostatics stand point. In order to do this I must start by explaining the Ohmic operation of an MESFET and finish by explaining the basic electrostatics of MESFET operation.

A MESFET and the majority of MOSFETs have a source, drain, and gate terminal. A MESFET is like a MOSFET in the sense that the gate is used to control the flow of current from the drain to the source. As well as in a MOSFET, the potential from the MESFET's drain terminal to source terminal also affects how much current will flow from the drain to source. Both devices can be thought of in simple terms as being a variable resistor between the drain and source terminals or more accurately, like the hybrid-pi model in Figure 9, a constant resistor in parallel with a variable current source between the drain and source terminals. Both devices "variable current source" is controlled by the current/voltage at the gate of the device. Where they begin to differ in the Ohmic sense is in the resistance and transconductance (g_m) values of the hybrid pi model. A MESFET will typically have: a much lower gate resistance (R_{in}) than a MOSFET, a similar output resistance (R_{out}) to a MOSFET, and a lower transconductance (g_m) than a MOSFET. The reasons why these values are different is obvious when comparing the electrostatic differences between the two devices.

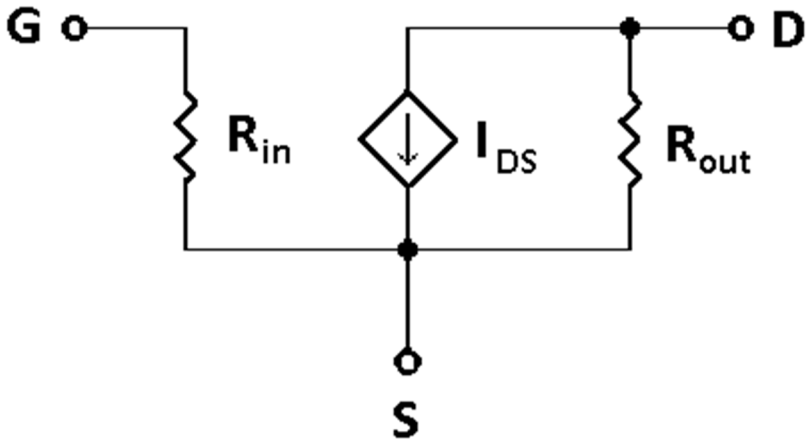

Figure 9: Generic Hybrid Pi Model

As stated previously, the MESFET is a majority carrier device. This means that the current carrying species are of the same type as the dopant species in the controlled region of the device. This is in contrast to the MOSFET, which is a minority carrier device, meaning that the current carrying species is of the opposite type of the dopant species in the controlled region of the device. Since the dopant species in the body of a MOSFET device is the opposite of the dopant species in the source and drain regions, a depletion region will exist at the drain/body and source/body junctions. It is the electric field created by these depletion regions in series with the resistivity of the body that impedes the current carrying species from traveling between the source and drain. In an enhancement mode MOSFET, the device will remain in cutoff until a large enough concentration of minority carriers, equal to or greater than that of the majority carriers as the interface at the bottom of the gate, are attracted to and accumulated at that interface. This forms a low resistance path between the source and drain regions. A MOSFET is said to be operating in linear mode when the minority carrier concentration at the gate oxide/body is equal to or greater than that of the majority carriers at the gate oxide/body interface, and the drain bias is small enough so that it does not cause a significant depletion of the accumulated carriers at the drain/body interface. A MOSFET is said to be operating in saturation when the minority carrier concentration at the gate oxide/body is equal to or greater than that of the majority carriers as the

interface at the gate oxide/body interface and the drain bias is large enough so that it does cause a significant depletion of the accumulated carriers at the drain/body interface (pinching off the channel). In opposition to the electrostatics in a MOSFET, a MESFET device must be forced into the cutoff region as it will operate in linear or saturation mode in the absence of an applied bias. This is because in a MESFET, the dopants in the body, source, and drain regions are the same species. This means that no depletion region will be formed at the source/body and drain/body junctions and the force preventing the current carrying species from traveling between the source and drain is primarily the resistivity of the body region. In order to place the MESFET in the cutoff and linear regions, the gate of the MESFET must be biased so that the depletion region created by the gate depletes the body/channel of its carriers in the body region between the source and drain terminals. In order not to cause confusion, referring to a MESFET's "channel" does not imply an excess or accumulation of carriers as it does in a MOSFET, but merely the consequential regions of the MESFET's body between its drain and source. A MESFET is said to be operating in cutoff mode when the channel is depleted of its carriers, the free carrier concentration is lower than the doped concentration throughout the channel, and in linear mode when the free carrier concentration is equal to the doped concentration in the majority of the channel. A MESFET is said to be operating in saturation when the free carrier concentration is equal to the doped concentration at the source end and center of the channel but less than the doped concentration at the drain end of the channel. This pinching off of a portion of the channel is what yields the saturation behavior. The three regions of MESFET operation can be seen in Figure 10.

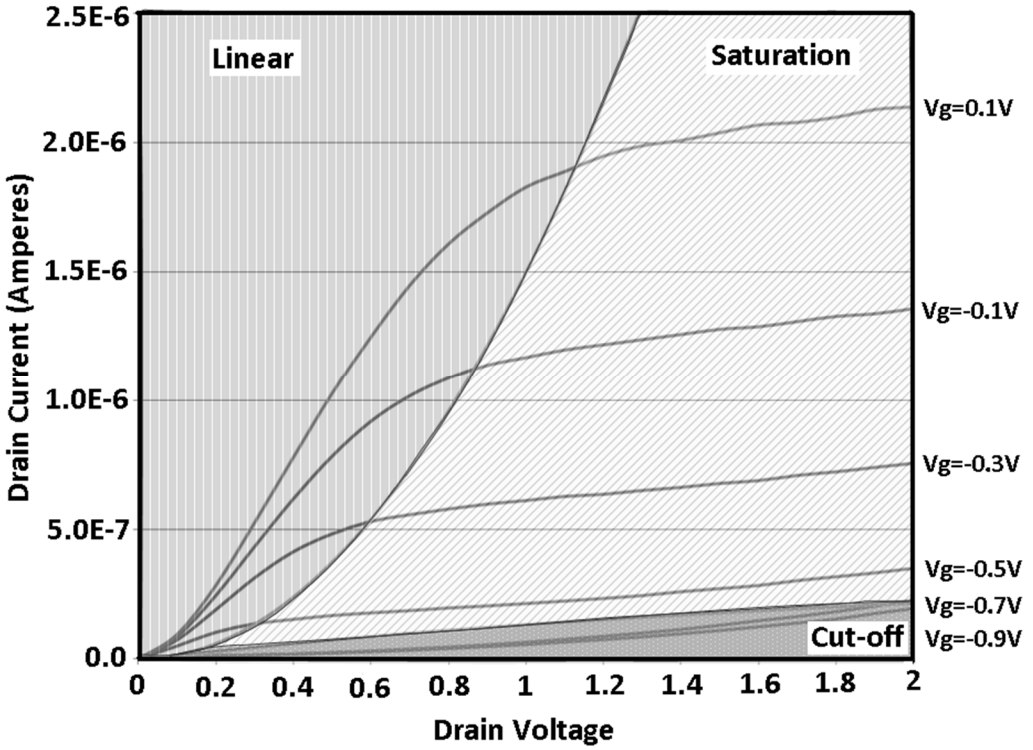

Figure 10: MESFET Regions of Operation

1.4 CONCLUSION

The MESFET device, fabrication, and operation have been discussed in a very general manner in this chapter in order to give a basic understanding of the MESFET device and to define terms for use in later chapters. Although the integration of a MESFET into a standard SOI CMOS process has been discussed, the importance of the fabrication of the MESFET gate contact needs to be discussed in additional detail as it is central to the operation of a MESFET device.

CHAPTER 2

MODERN SILICIDES

2.1 SCHOTTKY GATE

While MOSFETs make use of a metal oxide semiconductor structure as the gate to control the flow of current in a circuit, the MESFET makes use of a metal semiconductor structure/contact. More specifically, a MESFET relies on a *Schottky* metal semiconductor structure to control the flow of current through the device. The metal semiconductor junction must be Schottky and not Ohmic or else the MESFET would not act as a transistor but rather as a three terminal center-tapped resistor. Furthermore, all of a MESFET devices characteristics have a larger sensitivity to the quality and characteristics of the metal semiconductor barrier than they do to any other parameter or dimension in a fabricated MESFET, that is to say that a nominal change in the Schottky barrier characteristics will yield a larger change in the characteristics of a MESFET device than a nominal change in any other device parameter. The quality and characteristics of a metal semiconductor junction not only depend on the materials used to fabricate the junction but also vary heavily on the fabrication process through which the junction is made. It is for these reasons that the MESFET's Schottky gate fabrication and characteristics need to be carefully analyzed and play the most influential role in the design of a MESFET device.

2.2 SILICIDE FORMATION

The word silicide is used to refer to any Compound containing metal and silicon atoms. They may be binary, tertiary, or any higher order Compound. Their atomic composition can vary from being almost entirely metal to almost entirely silicon. Although the word silicide can be used to describe a very large number of Compounds, silicides are a crucial part of not only MESFET fabrication but the entire integrated circuit (IC) process.

There are three general terms used to specify the atomic composition of a silicide: metal-rich, which is used for silicides with more than a 2 to 1 metal atom to silicon atom ratio; balanced, which is used for silicides with a 1 to 1 metal atom to silicon atom ratio; and metal-depleted or silicon-ritch, which is used for silicides with more than a 2 to 1 silicon atom to metal atom ratio

[6]. These terms are important and useful when describing the electrical characteristics, physical characteristics, and thermal/resistive stability of a silicide. With a few exceptions; a silicide's resistance is proportional to its metal concentration. In contrast, the thermal and resistive stability is inversely proportional to a silicides metal concentration. Epitaxial growth of a silicide will almost always result in a silicon-ritch silicide, because silicon will be the diffusing species, while polycrystalline growth can result in a silicide with any of the three atomic ratios.

Though there have been and still are many different ways to form silicides: focused ion-beam mixing, high-pressure force-fill, cold/hot sputtering, plasma vapor deposition (PVD), chemical vapor deposition (CVD), low-pressure CVD (LPCVD), and many more; the majority of modern silicides used in IC technology are formed by rapid thermal annealing (RTA) [5]. The term rapid thermal annealing (RTA) is used to refer to the process in which a sample consisting of a thin film of pure metal that is deposited on top of crystalline silicon wafer is heated at a sufficient temperature, in the case of silicides anywhere from 200 Celsius to 950 Celsius, for a very short period of time; on the order of one minute or less. The specific stoichiometry of the metal sillicide (Me_ySi_x) depends on many things; one of which is the temperature of the RTA. The stoichiometry of the final silicide is important because it determines the electrical and physical characteristics that the final silicide will have in an IC. A very low temperature RTA (200 Celsius to 500 Celsius) will yield a combination of a metal rich silicide and a balanced silicide. A low temperature RTA (300 Celsius to 600 Celsius) will yield a combination of a balanced silicide and a metal depleted silicide. A high temperature RTA (600 Celsius to 850 Celsius) will primarily yield a metal depleted silicide [7]. These different annealing temperatures yield different silicides because the silicide formation temperature affects the reaction kinetics taking place at the metal and silicon interface.

Table 1: Typically Available Useful Parameters for Modern Silicides [7]

Typically Available Useful Parameters for Modern Silicides			
Silicide	C54-$TiSi_2$	$CoSi_2$	NiSi
Resistivity (ρ) (μ Ω cm)	13 - 20	14 - 20	10.5 – 20
Technology Node (nm)	300 - 180	180 - 65	90 – 12
nm Silicide Formed per nm Ni Deposited(nm)	2.51 -	3.49 - 3.52	2.20 - 2.34
nm Silicon Consumed per nm Ni Deposited (nm)	2.27	3.61 – 3.64	1.83 – 1.84
Schottky Barrier Height to 10 Ω m n-type Silicon (eV)	0.6	0.64	0.67
Formation Temperature (^{O}C)	600 - 700	600 - 700	400 – 600
Dominant Moving Species	Si	Co	Ni
Thermal Stability Temperature (^{O}C)	< 950	900	700
Epitaxy on Silicon	No	Yes	No ($NiSi_2$ Yes)
Reduction of SiO_2	Yes	No	No

The nucleation and reaction kinetics of the metal-silicon interface are the two most influential factors in the formation of a silicide [7]. The formation of a silicide may be nucleation controlled, diffusion controlled, or a combination of both. When the growth of the silicide is linearly proportional to the square root of the annealing time then it is considered to be diffusion controlled [8]. When the formation of the silicide is very sudden, non-planar or discontinuous, or requires the sample to be heated beyond a specific temperature to begin a reaction, then it is said that the silicide formation is nucleation controlled [8]. The nucleation and reaction kinetics of the metal-silicon interface become even more complex and important as the thickness of the silicon wafer decreases from the thickness of that in bulk CMOS technology to that of the thin silicon film thickness used in SOI technology. Since the theory and equations that describe the growth of

silicides require a near infinite supply of silicon to be valid, the growth of a silicide on a thin silicon film becomes almost entirely phenomenological [9]. Although silicide formation will further be discussed in detail herein; this aspect of the formation of silicides, nucleation and diffusion, is very involved and will not be discussed in depth as an advanced understanding of it is not necessary at this point but will be important in future work involving the optimization of MESFETs.

In the formation of a silicide there are a myriad of processes taking place and as a result, not only the region where the silicide is formed but also the surrounding silicon undergo a variety of changes. Generally in the IC process flow, silicides are used to make contact to the source, drain, and gate poly regions of a MOSFET device. Forming a high quality silicide in these regions is essential to form good contacts, keeping resistance low, and maintaining a high yield and reliability. The formation of a silicide to act as a MESFET Schottky gate is no different. The formation of a high quality silicide in the gate region of a MESFET is a very delicate process which can yield many negative results that are of concern and will impact the operation of a device if not done properly such as: spiking, dopant leaching, high resistivity, and improper thickness of growth. It is essential not only that the gate silicide is formed in a manner in order to suppress these adverse effects or with these adverse effects taken into account, but also that as many of the remnants of modern IC processing specific to MOSFETs are prevented from making it into the fabrication of the MESFET such as: halo dopings, lightly doped drain/source (LDD) dopings, and threshold adjust dopings. Unfortunately, the majority of these modern MOSFET fabrication remnants do make it into the fabrication of the MESFETs that are integrated into and fabricated in standard CMOS SOI; however, some are less detrimental than others and will be discussed in a later section.

I will begin with some background on the subject of silicide formation in order to be able to provide a more educated discussion about silicides, silicide formation, and their effect on MESFET device operation.

2.3 DIFFERENT MATERIALS

Over the course of the development of IC technologies after the introduction of silicides to the IC process flow, there have been many different silicides that have been used. Each generation of IC technology has had a specific silicide that was the used almost universally across many different foundries and companies because it was accepted as the premium silicide at the time [7]. While each generation of silicides had their upsides and downsides, continual silicide development was necessary in order to increase reliability and allow for the continual downscaling IC technology [7]. This continual silicide development came in the form of newer silicide processing techniques and materials. Since this thesis is concerned with the optimization and integration of MESFETs in modern processes, silicides that are no longer used or are currently not used in submicron technologies will not be considered.

The three most widely used modern silicides technologies for commercial IC technology are: titanium silicide (TiSi), cobalt silicide (CoSi), and nickel nickel/platinum silicide (NiSi Ni(Pt)Si) [7]. It is stated that they are the most widely used silicide technologies and it is stated in this manner, metal name followed by silicide, because the stoichiometry of the actual silicides that are used in ICs vary. The majority of silicides used in modern IC technology are disilicides (~ 70% are $MeSi_2$) while very few are balanced or metal rich silicides (< 30% are MeSi or Me_x Si) [7].

Just as titanium silicide was developed to replace its predecessor, cobalt silicide was developed to replace titanium silicide for primary use in IC technologies from 180nm to 65nm [7]. The same is true for nickel nickel/platinum silicide as it was developed to replace cobalt silicide for primary use in IC technologies from 90 nm to 12nm [7].

Cobalt silicide was developed to replace titanium silicide for a large number of reasons. Titanium silicide formation and growth kinetics are strongly influenced by the presence and type of dopant species in the crystalline silicon used in the silicide formation which is undesirable for maintaining a stable and consistent process and yield [7]. $TiSi_2$ is difficult to integrate into SOI processing because a combination of the dominant diffusive species in $TiSi_2$ formation being Si and a moderate silicon consumption ratio, $TiSi_2$ often forms voids in the thin silicon film upon

undergoing the final phase transformation from the base-centered orthorhombic C49-$TiSi_2$ to the face-centered orthorhombic C54-$TiSi_2$ due to a net reduction in volume as illustrated in Figure 11 [7, 10, 11]. The formation of $TiSi_x$ leaches dopants out of the surrounding silicon along its grain boundaries in an inconsistent manner which will lead to inconsistent barrier heights and other uncontrollable characteristic changes of the silicide/silicon interface (illustrated with tungsten silicide (WSi) in Figure 12) [7]. Ti is highly reactive with SiO_2 and Si_3N_4 which can cause the formation of shorts during the silicide growth process [7]. Since Si is the dominant moving species in $TiSi_2$,Si quickly diffuses along Ti grain boundaries and forms silicide in this manner faster than the silicide growth into the crystalline silicon which can result in shorts if not annealed in an N2 ambient [7], It is nearly impossible for $TiSi_2$ to be grown epitaxially on crystalline silicon while $CoSi_2$ can be epitaxially grown on crystalline silicon with only moderate difficulty [7, 12]. The most common phase of $TiSi_2$ has a resistivity (~65 $\mu*\Omega$cm) more than three times larger than that of $CoSi_2$ (~20 $\mu*\Omega$cm) [7]. $TiSi_2$ cannot be made to have line widths of less than 180nm and maintain good resistive stability (180nm is the approximate point where the sheet resistance of $TiSi_2$ begins to increase unacceptably and inconsistently as illustrated in Figure 13) [7]. Lastly, $TiSi_2$ has a larger sheet resistance than $CoSi_2$ above 180nm in the sub-micron regime and even slightly above as seen in Figure 11 [7].

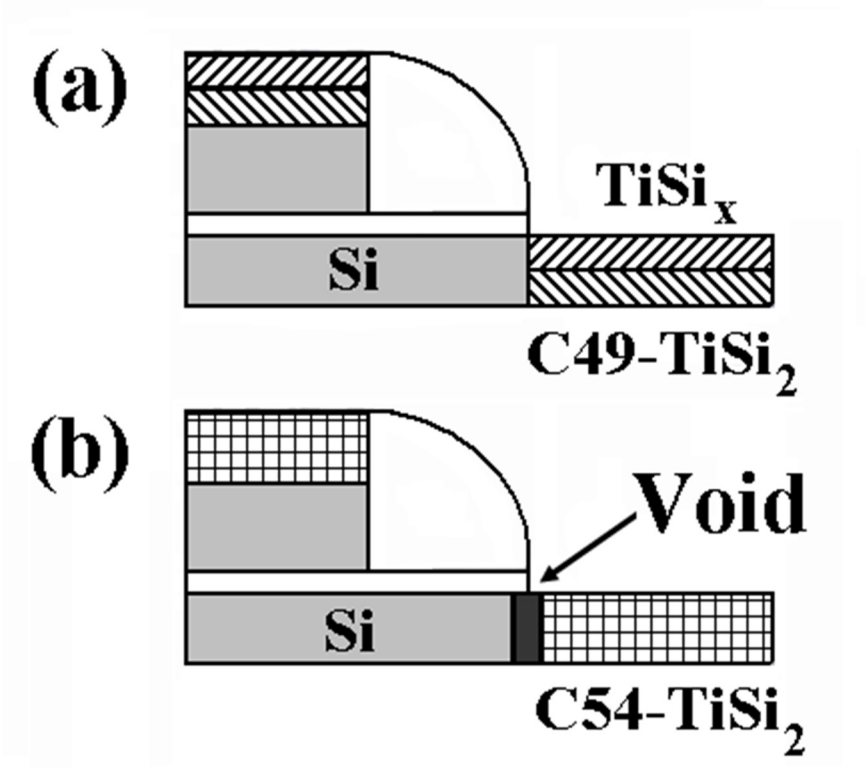

Figure 11: Void Formation During Titanium Silicide Formation on a Thin Silicon Film [7]

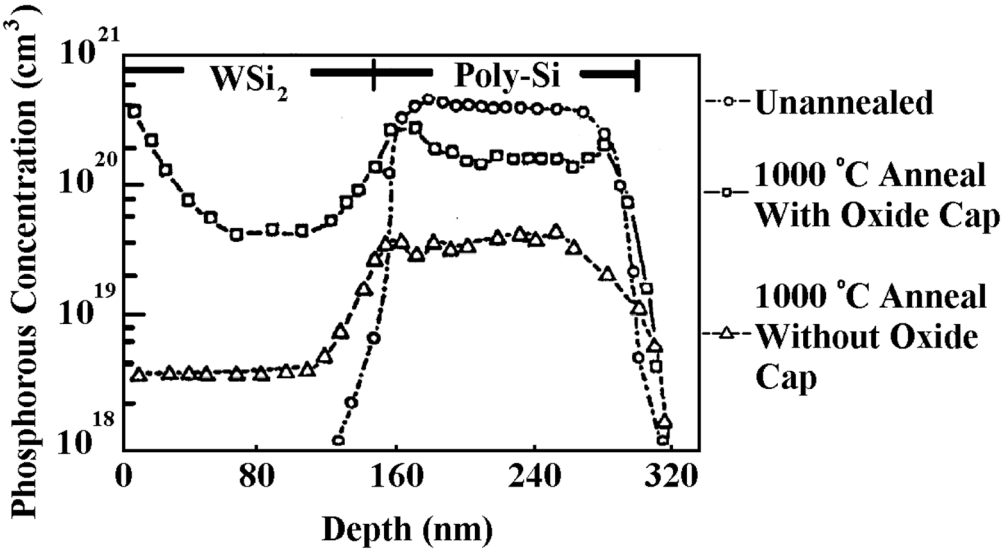

Figure 12: Leaching of Dopants as a Result of Silicide Formation

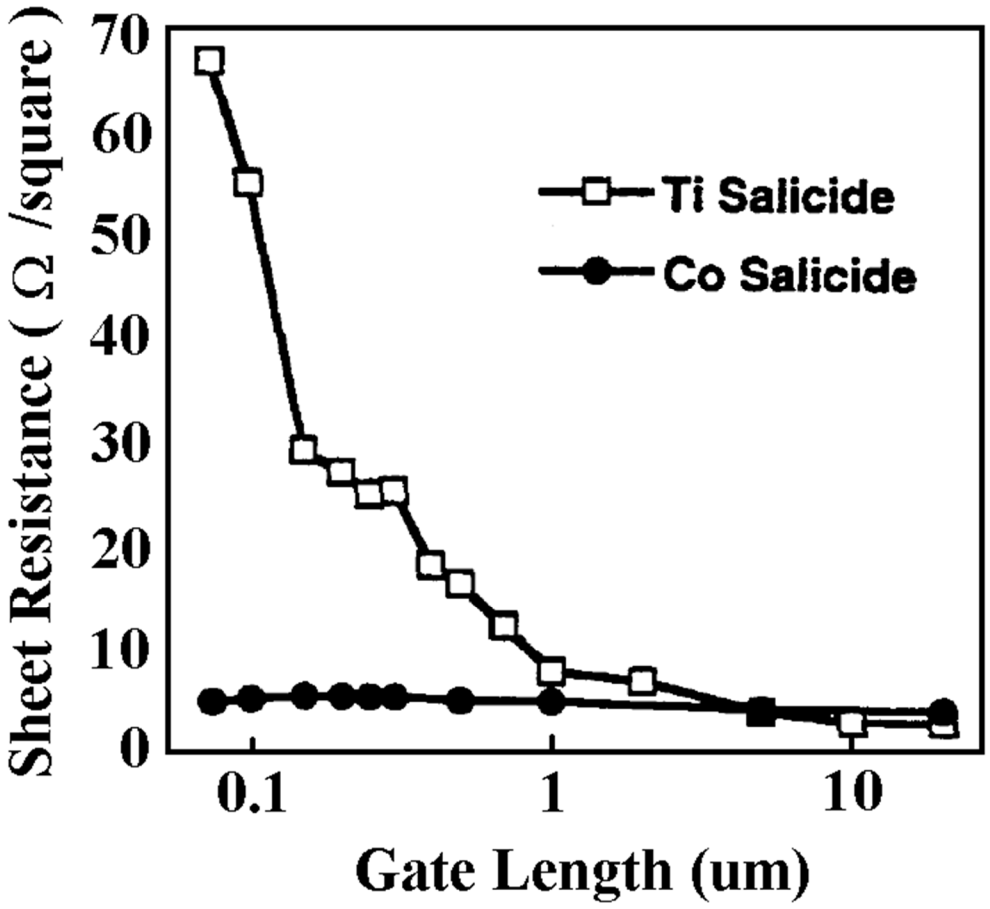

Figure 13: Sheet Resistance of $CoSi_2$ and $TiSi_2$ as a Function of Line Width/ Gate Length [13]

Nickle/platinum silicide was developed and is currently used as a replacement for cobalt silicide for many reasons. NiSi has a lower resistivity (ρ)(~15 μ∗Ωcm) than $CoSi_2$ (~20 μ∗Ωcm) [7, 14]. NiSi can be made to have line widths of less than 50nm and maintain good resistive stability (50nm is the approximate point where the sheet resistance of $CoSi_2$ begins to increase unacceptably and inconsistently as illustrated in Figure 14) [7, 13]. The nickel silicide formation to silicon consumption ratio is less than half the silicide to silicon consumption ratio of both $TiSi_2$ and $CoSi_2$ [7]. $CoSi_2$ is incompatible (leads to high resistivity and poor morphology) with Germanium implanted silicon technology which is becoming prevalent in SOI technology [15]. NiSi has a larger thermal budget than $CoSi_2$ [7, 14]. NiSi can be grown through a thin oxide while

$CoSi_2$ cannot; $CoSi_2$ is so sensitive to a small native oxide layer that the wafer it is being deposited on must be vacuum sputter cleaned *in situ* in order to form $CoSi_2$ [7].

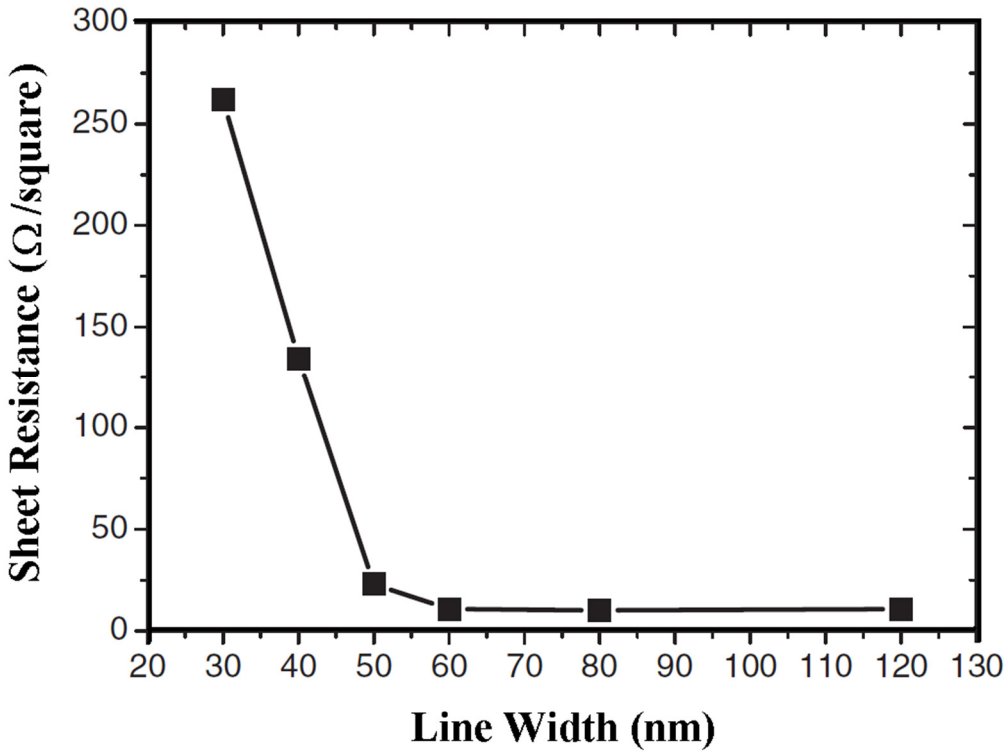

Figure 14: Sheet Resistance of $CoSi_2$ as a Function of Line Width/ Gate Width [16]

Though titanium silicide was phased out and replaced with new materials, the use of titanium in the silicide formation process has not been abandoned. Titanium has many uses in the fabrication of modern silicides. As stated previously, the formation of $CoSi_2$ requires that there is no native oxide on the wafer prior to Co sputtering; also, NiSi growth is drastically retarded by a small native oxide. In addition, a SiO_2 layer can form on the silicon under the deposited metal if the queue time between sputter deposition of the metal and the first RTA step is not kept very short [15]. As equipment capable of sputter deposition and in situ vacuum sputter cleaning is more expensive than standard sputtering equipment and the possession of this equipment does not guarantee an oxide free interface, titanium is often used to aid in the formation of modern silicides because it acts as a gettering agent and chemically reduces any oxide that exists between the

silicon and the deposited metal [15, 17]. A thin layer of titanium (~2nm has been found to be the optimum amount) can be added either on top of the deposited metal as a capping layer or in between the deposited metal and the thin silicon film as an interlayer [15, 17]. Though this method of ensuring the proper formation of a silicide in the presence of an oxide barrier has many benefits, it also has its downsides such as incompatibility with $CoSi_2Ge$ technology and a significant increase in the surface roughness of the silicide/silicon surface of NiSi as seen in Figure 15.

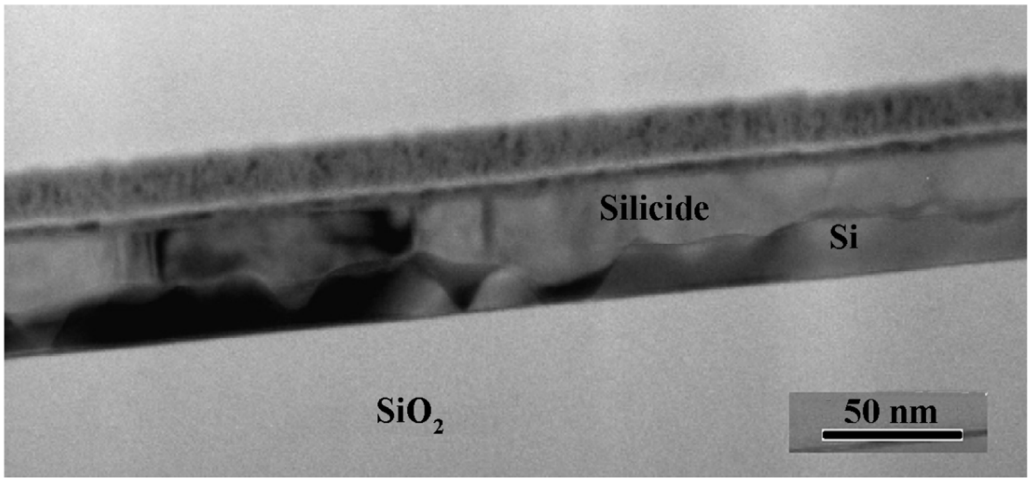

Figure 15: Cross Sectional TEM Showing the Increase in the Surface Roughness of a Nickel Silicide Formed on Silicon with a 2nm Titanium Capping Layer [15]

Along with titanium, platinum has been integrated into the most modern silicide process in order to improve its electrical and fabrication characteristics. When platinum is added to nickel silicide, it increases formation temperature window of metal rich and balanced phases of nickel silicide from 250-350 Celsius and 400-800 Celsius (seen in Figure 16) to 300-400 Celsius and 500-900 Celsius respectively, which allows for more control over the silicide formation with less temperature precision [7]. Platinum delays silicide agglomeration and suppresses the formation of silicon-rich silicides such as $NiSi_2$ which have higher resistivity than NiSi and is undesirable in non epitaxial NiSi [7]. Platinum reduces the nucleation barrier which makes the silicide formation primarily controlled by the diffusion of Ni (makes the silicide formation rate proportional to time and not a thermodynamic threshold factor) [8, 18]. Lastly, the addition of platinum to the nickel

used in the formation of a silicide increases the work function of the silicide, since platinum has a larger work function than nickel, which can be beneficial for use in Schottky and tunneling contact applications [7, 18, 19].

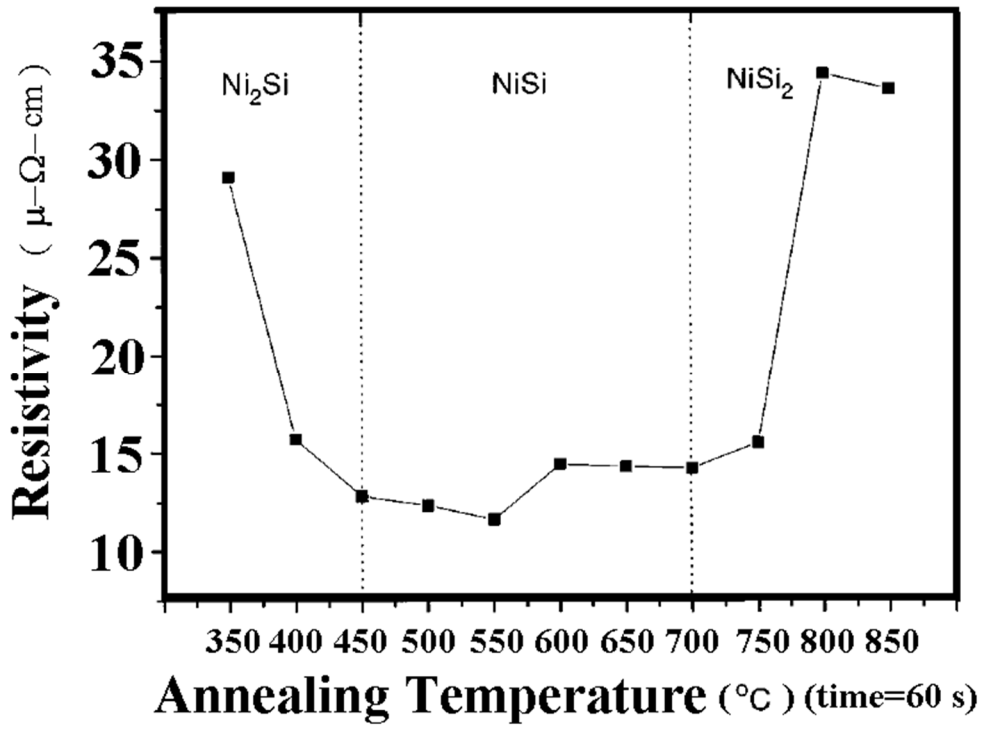

Figure 16: Nickel Silicide Resistivity as a Function of Annealing Temperature [14]

In the end, a silicide is chosen based on its physical and electrical characteristics. Since the optimization concept presented in this paper is demonstrated in a technology that uses $CoSi_2$ as its silicide, $CoSi_2$ will be the primary silicide discussed in this thesis with some lesser discussion about Ni(Pt)Si when talking about future optimization.

2.4 SILICIDE THICKNESS

Controlling the dimensions of silicide growth in an IC is very important in order to maintain good operation, yield, and reliability. In bulk CMOS processes both the lateral and vertical dimensions of silicide growth are equally important. As the CMOS processes have evolved, the use of new silicides, $CoSi_2$ and NiSi, has mitigated the majority of lateral silicide growth and shorting problems since they do not have the same growth properties and problems that $TiSi_2$ has [7]. This makes silicide growth in the vertical direction the primary process of concern. Since modern IC technology is moving toward SOI technology, it is more crucial than ever that the vertical growth of a silicide is precise, for good contact resistance, and limited so that it does not reach the buried oxide (BOX), for reliability and yield [20]. Since SiO_2 is amorphous, if a silicide grows all of the way through the thin silicon film to the BOX, it can cause: shorts, voids/opens, phase reversal, high contact resistance, and new silicide/oxide phases to occur [7, 10, 11]. It is the general consensus that the silicide growth should not reach the BOX layer not only for reliability reasons but also to maintain good device operation characteristics.

Generally, the width and length of a contact in a given technology is anywhere from 115% to 200% of the minimum lithographic size of that technology. In agreement with the ITRS roadmap and in order to maintain low parasitic resistances and minimize transconductance degradation, it has been shown that the specific contact resistance should be kept below 1 $\mu\Omega\text{-cm}^2$ (ideally < 500 $n\Omega\text{-cm}^2$) [7, 20]. In older technologies (~ >150nm), there is a sufficient amount of surface area and silicon volume below a contact, due to the limit set by the minimum lithographic size and the size of the thin silicon film, such that a terminal attains its lowest series resistance and contact resistance as the contact silicide thickness approaches zero. This effect vanishes as the size of the contact reduces as is does in the sub 150nm technologies. When the interface area and silicon volume below the contact shrink too much, the silicide contact thickness must be optimized in order to balance and maintain a low contact resistance and maintain a low series resistance. If the silicide thickness increases, the volume of the degenerately doped low resistance silicon below the contact will reduce to the point it dominates the contact resistance and as the silicide thickness decreases, the area of the silicide/silicon contact interface reduces to the point where the contact

resistance dominates the series resistance as seen in Figure 17 [20]. This means that the growth of modern silicides must be done in a manner such that a minimum silicide thickness is achieved without exceeding a maximum silicide thickness. This optimum silicide contact thickness is determined by the thickness of the thin silicon film. This is yet another reason why NiSi has come to be the prevalent modern silicide; its low silicon consumption ratio allows better control of the final silicide thickness than with previous disilicide material.

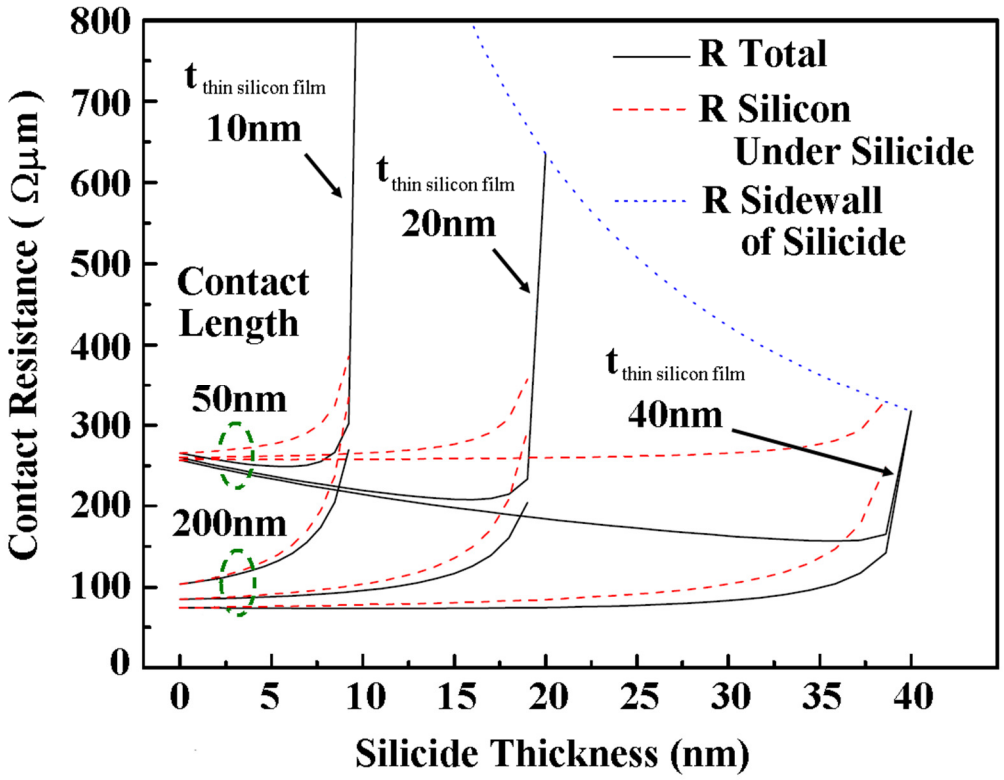

Figure 17: Contact Resistance of a Silicide Contact as a Function of Thin Silicon Film Thickness, Silicide Thickness, and Contact Length [20]

Since the overall thickness of the silicide and the ability to control that thickness has become very important, the old method of controlling the thickness of a silicide through limited metal source deposition has been replaced with multi step RTA and etch processing. Also, a new method to control the thickness of the silicide through the pre-amorphisation of silicon with germanium has been implemented in many of the modern IC technologies since the 90nm

technology node. These methods are the three primary methods for controlling the thickness of the formed silicide. Each has their own advantages and optimal applications; also, each has their own downsides and added costs.

The most simplistic method is the limited metal source deposition as it does not require any extra equipment and it is comprised only of the steps required to form a silicide. The limited source metal deposition method involves depositing a small and precise amount of pure metal on top of the thin silicon film and annealing until that metal is fully consumed. The thickness of the initial metal deposit is what determines the final resulting thickness of the silicide. Although the process has only two simple steps, in the end it is limited by the difficulty and inability to adequately control the initial deposited metal layers thickness and therefore is currently virtually unused [7].

The most common method of controlling the thickness of the grown silicide is the two step RTA. The two step RTA consists of: the deposition of a pure metal on top of the thin silicon film, a limited low to medium temperature RTA of the wafer to drive a limited amount of metal atoms into the thin silicon film, a chemical etch that removes the unreacted metal from the top of the thin silicon film, and a medium to high temperature RTA of the wafer to convert the silicide into its final phase and improve the silicides uniformity [7, 21]. Although this method is more expensive than the limited metal source diffusion method because it required special RTA and wet etch equipment, it is considered the standard way of forming modern silicides due to the reliability and quality of the silicides it produces.

The newest method for controlling the thickness of the grown silicide is through pre-amorphisation of silicon with germanium. This method consists of: a Ge^{+} implant, generally 1 x 10^{15} ions/cm^2 (> 1 x 10^{20} ions/cm^3 since the volume is dependent on implant energy), to make the crystalline source/drain and polycrystalline gate silicon amorphous, the deposition of a pure metal layer on top of the wafer, and a high temperature RTA of the wafer [7, 22]. It has been shown that the thickness of the pre-amorphised layer is what determines the thickness of the final resulting silicide so long as the annealing temperature remains low (in the diffusive growth region). Along with the ability to control the silicide thickness, germanium pre-amorphisation has also shown to

improve the reliability of a silicide contact as well [7, 21]. This method is the most expensive method of controlling the silicide thickness because it requires ion implantation of the wafer prior to the metal deposition step. A process in which a MESFET could be successfully integrated into the standard CMOS process flow, without major design waivers or a lack of recognition of an apparent device by a fabrication plant's software, could not utilize germanium pre-amorphisation of silicon as a means for controlling the thickness of the silicide growth as it would be detrimental to the gate region of the MESFET and likely prevent proper operation of the MESFET device. Luckily, this is rare in sub 90nm technologies and only becoming predominant in sub 45nm technologies [7].

2.5 CONCLUSION

As discussed in this chapter, the fabrication of a silicide in modern IC technology is a very involved process that requires a lot of control and precision and therefore it is given much care in modern standard SOI CMOS processes. Although there may be some non-ideal effects involved in the fabrication of a silicide that are unavoidable and will affect the electrostatics of the gate more than they will affect the electrostatics in the source and drain regions, the importance of silicides in IC technology will ensure that the Schottky gates of MESFETs integrated into standard SOI CMOS processes are fabricated in the best and most though out manner possible.

CHAPTER 3

NON-IDEAL MESFET FABRICATION AND OPERATION EFFECTS

As discussed in the previous section. MESFETs that are integrated into the standard SOI CMOS process flow will most likely receive some undesirable remnants from the MOSFET fabrication such as: halo doping, LDD doping, threshold adjust dopings, and sidewall leakage implants (for older processes). In this chapter a properly calibrated device model will be developed and used to show what effect on the operation of the MESFET device some of these MOSFET processing remnants will have and how to determine what the cause of a difference between the measured current-voltage characteristics and simulated current-voltage characteristics may be.

3.1 MODEL CALIBRATION

In order to properly discuss the tradeoffs between different MESFET design methods using simulation based results, the simulation model must first be properly calibrated to a real/fabricated MESFET in a comparable technology. Along with this, the physical characteristics and material properties of the simulated model and the fabricated calibration devices must remain similar so as not to put the simulated device in a technology-effects region that it is not calibrated for. This will prevent the omission of short channel effects and other sub micron regime effects from making the simulation results that are obtained better than they should be or just inaccurate. The device type that the calibration was done with was a single channel FD MESFET (concept shown in Figure 18) with similar physical characteristics to that of the one shown in Figure 4.

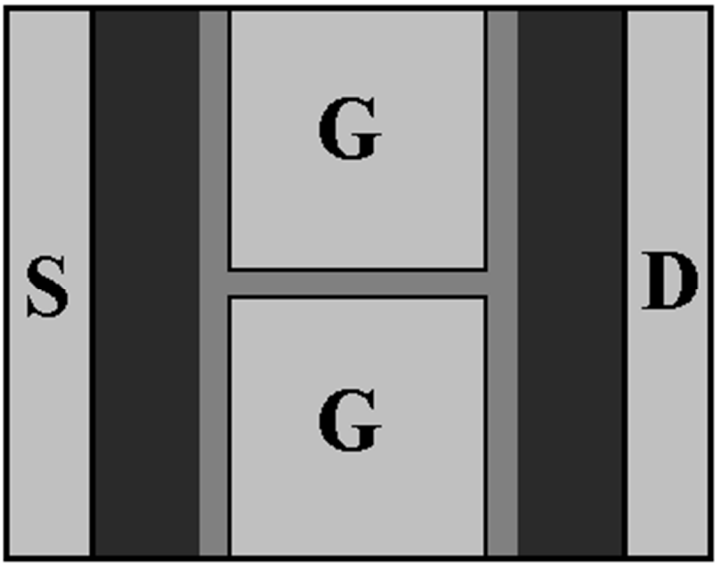

Figure 18: Single Channel FD MESFET Device

The first step towards modeling a MESFET in a technology computer aided design (TCAD)/finite element simulator is to garner as much information about the process and devices that you can from the fabrication plant or process documentation/process design kit (PDK). The PDK will have less information than a person at the fabrication plant but often direct communication with someone at the processing plant is forbidden. Also, since the PDK is local to the design folder of a process it is much more convenient to access and garner information from. If the channel, well, and contact dopings are not directly presented or evident from either of these sources, they can be calculated from sheet resistances and thickness data which *is* generally provided in the PDK. The type of silicide that is used in a process is almost always advertised in the PDK as it is used as a measurement of how cutting-edge/advanced a technology is (along with the minimum feature size). If it is not explicitly listed in the PDK it can be difficult to postulate the silicide type from provided sheet resistivities because many of the newer silicides have very comparable sheet resistivities that become even more similar when the sheet resistance variation due to fabrication is also provided. All of these values that are obtained in this method should be presented as a mean value along with the minimum and maximum values included (or in terms of

a percentage of the mean). Once all of information that can be obtained from the PDK is extracted then some preliminary calculations can be done to find the threshold voltage and drive current of the device that is being modeled (or aid in the design of a MESFET when designing) and a base TCAD model of the device can be created.

The base TCAD model should contain the mean silicide work function, mean dopant concentrations, and mean device dimensions as extracted from the PDK; however, these values are bound to deviate from their ideal values either due to process variation, fabrication process effects, or a lack of published data in the PDK. Process variation and fabrication process effects are usually included in the PDK as a minimum and maximum value for a parameter as previously discussed and the TCAD model parameters should never exceed the stated minimum and maximum values. Although this can lead to the development of a TCAD model that replicates experimental results, it may be doing so for the wrong reasons. This will prevent that TCAD model from providing correct results when other parameters of the model are adjusted thereby nullifying its purpose. A lack of published data is a broader concept but may be considered as: nonexistence of journal articles on modern technology characteristics employed in the process being used, lack of public data on a specific material being used, or the provision of only rudimentary and no advanced fabrication or design data in the PDK. An example of a lack of published data would be if the surfaces of the wafers being used in a process are (100) oriented (crystal surface orientation is not usually published in PDKs) while the value of the silicide work function obtained from literature and used in the base model is for silicides fabricated on (111) oriented surfaces. This can yield more than a 7% difference in the Schottky gate contact silicide's work function and be devastating to the operation of a MESFET device [23]. These types of problems can cause a TCAD model to be completely inaccurate if not calibrated using experimental results. So, many of the values obtained from the PDK or literature may change due to these effects. The next step toward modeling a MESFET in a TCAD simulator is to obtain experimental results for use in calibration of the base TCAD model.

One final thing to consider is the validity of using two dimensional simulations to model a three dimensional system. In the case of partially depleted MESFETs the variation in the

electrostatics of the device in the third dimension, non-simulated dimension, is very small which makes using two dimensional simulations and then multiplying the simulation results per width by the width of the device that is desired to be simulated perfectly acceptable. For the case of the fully depleted MESFET it is a little more subtle whether or not two dimensional simulations may be used to accurately represent a three dimensional system. In this thesis, calculations using data from the PDK of the calibration MESFETs show that the thickness of the silicide is anywhere in between the maximum and minimum value of 8.75 nm and 20nm. Using these values and the thickness of the thin silicon layer, calculations were done to show that when the gate was biased below 300 mV, the region of the silicon that was below the silicide gate was strongly depleted. When the gate was biased above 300 mV it was possible for a portion of the silicon under the gate silicide to become only partially depleted but it was dependent on the doping concentration below the gate which will be discussed later. So it was deemed acceptable to use two dimensional modeling to represent a three dimensional system that does have a large electrostatic variation in all three dimensions because the majority of the simulated range was able to be represented accurately with two dimensional simulations. The inaccuracy of the use of two dimensional simulations for fully depleted MESFETs may be seen in the forward region in the form or a lower than measured gate and drain current due to the omission of the small region of non-depleted silicon below the gate silicide in the device.

The calibration measurements were done for three different channel widths and two different source/drain access lengths. The measured results for the device with an L_{ad}/L_{as} of 500nm, a source voltage of 0 volts, and a drain voltage of 2 volts can be seen in Figure 19, Figure 20, and Figure 21. If not specifically stated, from this point in this thesis onward, when the drain access length is given it is implicit that the source access length is the same as the drain access length.

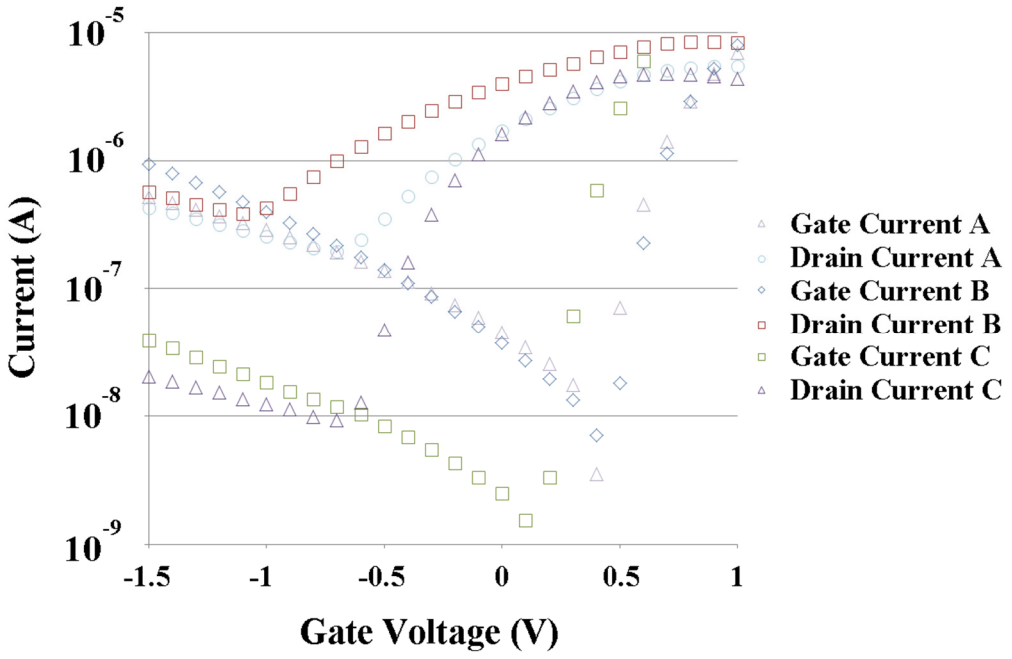

Figure 19: Results For Measured MESFETs With a Gate Separation of 200nm (Channel Length of 100nm).

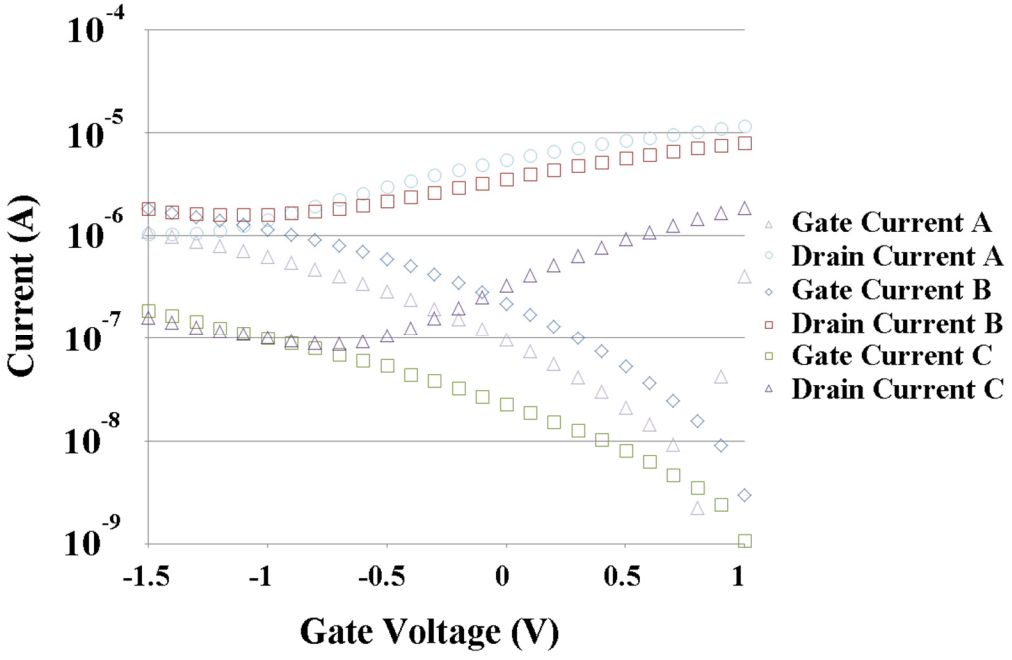

Figure 20: Results For Measured MESFETs With a Gate Separation of 250nm (Channel Length of 125nm).

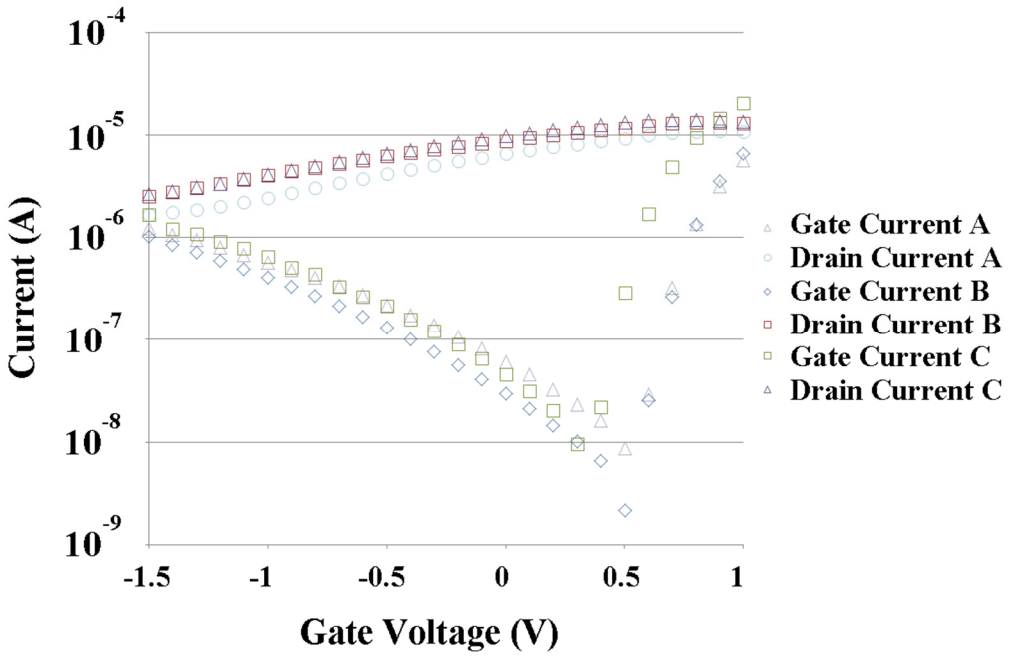

Figure 21: Results For Measured MESFETs With a Gate Separation of 300nm (Channel Length of 150nm).

The A, B, and C suffixes are there to identify which die the measured device came from and nothing more. All three devices in each graph should be identical in electrical and physical characteristics. This immediately raises the question as to why supposedly identical devices across different die are so different. This issue will be addressed in a later section; for now the calibration of the model is the primary concern.

One question that must be answered before calibration of the model can be done from these results is: to which curve should the model be calibrated? It can be seen in Figure 19 and Figure 20 that the devices measured from die C vastly differ from the results measured from die A and B; so, the model was calibrated so that the simulation results are somewhere between the measured results from die A and die B. Once the model had been calibrated the results seen in Figure 22, Figure 23, and Figure 24 were obtained.

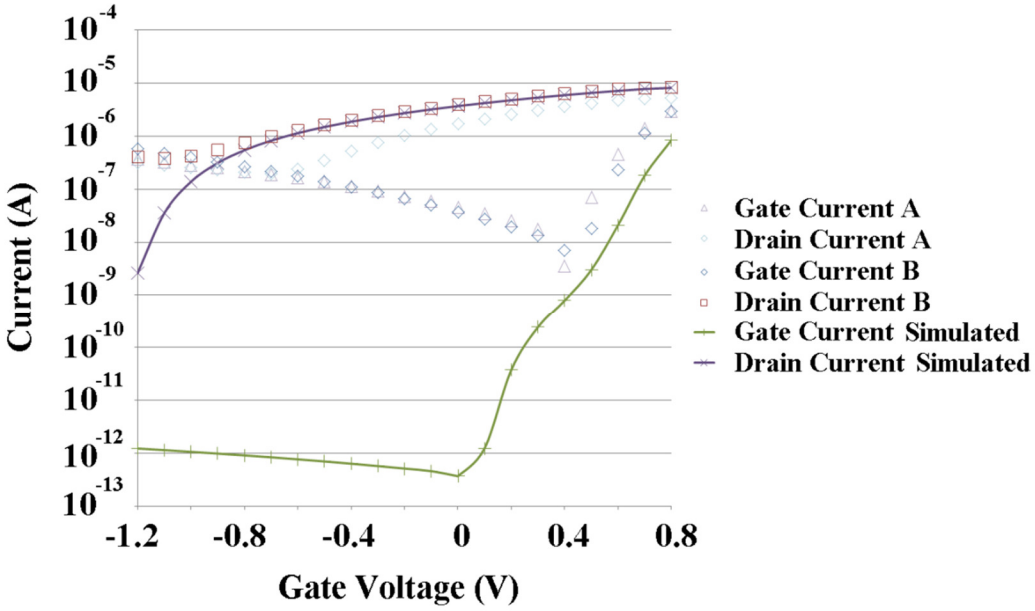

Figure 22: Results For Measured and Simulated MESFETs With a Gate Separation of 200nm (Channel Length of 100nm).

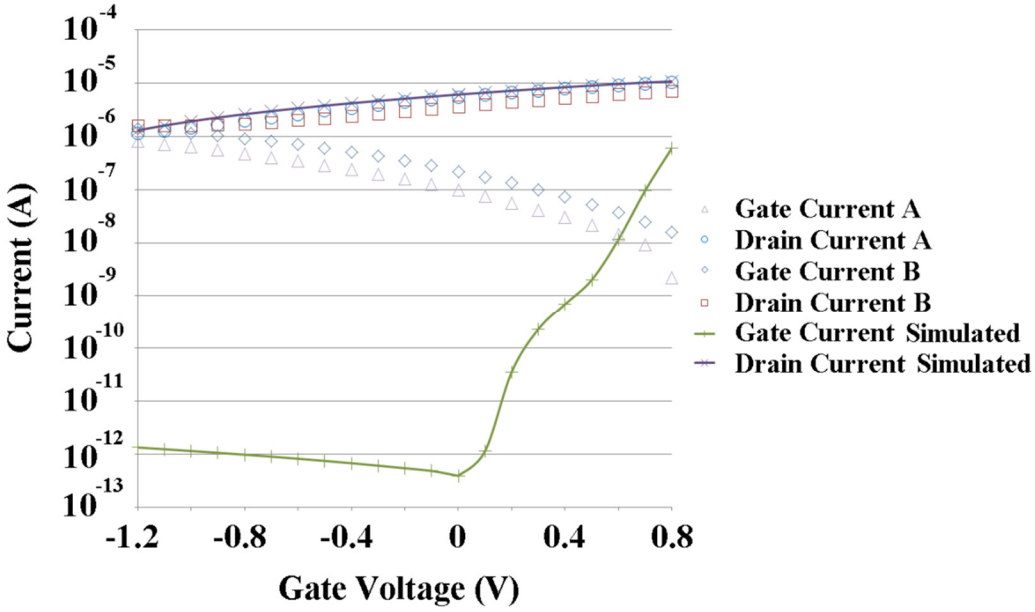

Figure 23: Results For Measured and Simulated MESFETs With a Gate Separation of 250nm (Channel Length of 125nm).

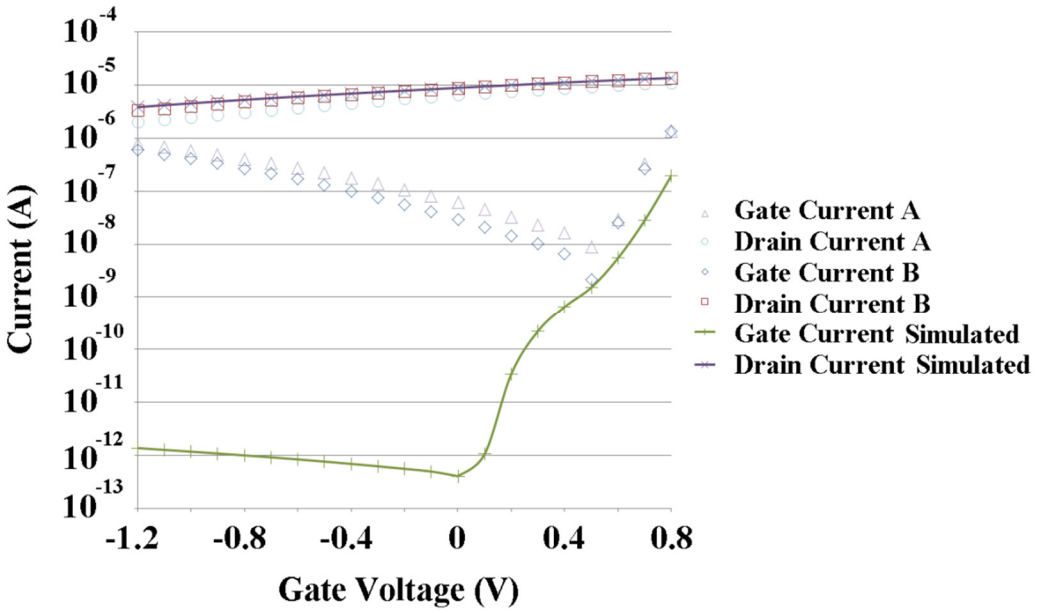

Figure 24: Results For Measured and Simulated MESFETs With a Gate Separation of 300nm (Channel Length of 150nm).

In Figure 22 through Figure 24 and Figure 28, the A and B suffixes refer to die A and B (no line) and the simulated suffix refers to the results of the calibrated model simulations (with line). With a given gate work function and channel width there are only very few channel dopings that will give the proper drain to source current characteristics. Temporarily ignoring the gross inaccuracy of the gate current, the drain current of the simulated and measured results matched closely enough to conclude that the model was calibrated. Now it is time to go back and investigate why the measured device curves displayed an extremely/anomalously high gate current, late Schottky gate diode turn on voltage, and extreme inconsistency in measured results of the same device on different die.

3.2 PROCESS EFFECTS AND VARIATION

There were three very substantial deviations of the calibration device from a near ideal device (the simulated device); in the following section, it will be shown why this is acceptable and the TCAD model is said to be calibrated. The first of which is the high Schottky gate contact current in the reverse bias region.

After much testing and troubleshooting it was found that electron tunneling from the gate into the source and drain regions is the source of the deviation of the measured gate current from that of the standard thermionic-diffusion current obtained from the device simulations. As seen from simulations of the device in Figure 18, this high gate current in the reverse bias region does not exist. However, this device is how an ideal MESFET should look but not necessarily how the MESFETs that have been fabricated do look in terms of both physical dimensions and material properties. In order to get a high gate leakage current the doping in the *silicon that is touching some percentage of the gate contact greater than zero*, the tunneling zone, must be high enough to allow for sufficient tunneling. If the silicon doping in this region is not sufficiently large enough, much larger than the channel doping, then sufficient tunneling will not occur and the resulting gate current will not be as large as it is in the experimental results presented herein. Also, the dopant species (acceptor or donor) in the tunneling zone must be the same species as the dopant in the rest of the channel region (lightly doped drain type doping (LDD)) in order for the device to operate properly. If the dopant species in the tunneling zone is of the opposite species of the dopant in the rest of the channel region (halo type doping) than intrinsic regions, pn junctions, and/or JFET type gate contacts can be created as a result.

The specific species of dopant that was creating the large gate current was postulated based of four key observations. First, if the dopant in the tunneling zone was the opposite species of the dopant in the rest of the device, the operation of the MESFET device would be affected in a way such that measurements would yield results that will not resemble a MESFET device but rather have characteristics more akin to a JFET. Second, the layout of the MESFET devices in the technology used in this thesis does not yield a gate region in the boolean extraction process which should prevent the fabrication machinery from depositing a halo doping into the tunneling zone as it does not recognize the MESFET device as having a gate. Third, if the species of dopant was of the opposite type of the dopant species in the rest of the device the dopant concentration that would be required in order to reproduce the same gate current magnitude that was obtained from measurement results would need to be unrealistically high in comparison to a realistic halo doping concentration. Fourth and final, the large gate current may not be the result of an intentional

addition of an additional dopant concentration but may be the result of a redistribution of the dopants in and around the region of the gate silicide's formation. All of this information leads up to the solution of why the experimental MESFET's reverse bias gate current is so large in comparison to reverse bias gate current of the simulated MESFETs; either the MESFETs did not avoid a remnant of MOSFET fabrication processing, the LDD doping, or the formation of the gate silicide caused the dopant concentration in the MESFET tunneling zone to increase due to dopant redistribution.

Whether or not it is an LDD doping or dopant redistribution that causes the gate current to be so much larger than the ideal gate current in these devices will not be specifically defined as from the information that is available to me it is unclear. It is expected that MESFETs integrated into standard SOI CMOS processes may receive undesirable dopings. However, it has also been shown in studies [24-26] that cobalt silicide is an excellent diffusion source for dopants. Figure 25 and Figure 26 show the out diffusion of arsenic from a pre-doped cobalt silicide layer into a silicon substrate and how dopants diffuse so easily through cobalt silicide respectively. The out-diffusion of dopants from the gate silicide would create the same result as the addition of an LDD doping in the tunneling zone. Although the cobalt silicide used in the fabrication of the calibration MESFETs is not pre-doped like the cobalt silicide in the figures, a study [24] has shown that there is the same scale of dopant redistribution created when un-doped cobalt silicide is formed on top of doped silicon which is the case in the fabrication of the calibration MESFETs used in this thesis. The amount of dopants redistributed would be approximately equal to the amount of dopant atoms that where in the volume where the cobalt silicide was formed. A preliminary calculation was done using the average redistribution distance seen in these studies and it was seen that for the dopant concentration used in the simulations of the calibration MESFETs, the dopant concentration in the tunneling zone could be raised to be the concentration necessary to replicate the measured gate current. However, this would require that the dopant redistribution between the two gate contacts was much less than the dopant redistribution into other portions of the MESFET device because if it was not then the operation of the device would be affected. Whether or not this will actually happen and why it would happen if it did is unknown at this point.

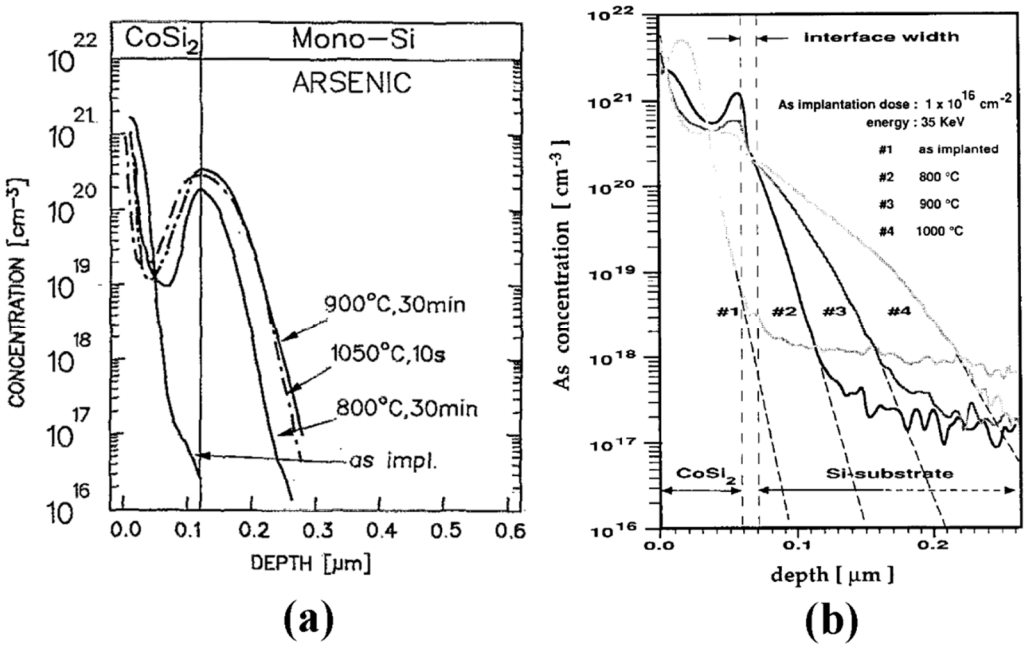

Figure 25: Out-Diffusion of Arsenic Dopant Atoms from Cobalt Silicide into Crystalline Silicon. (a) from [26] and (b) from [24].

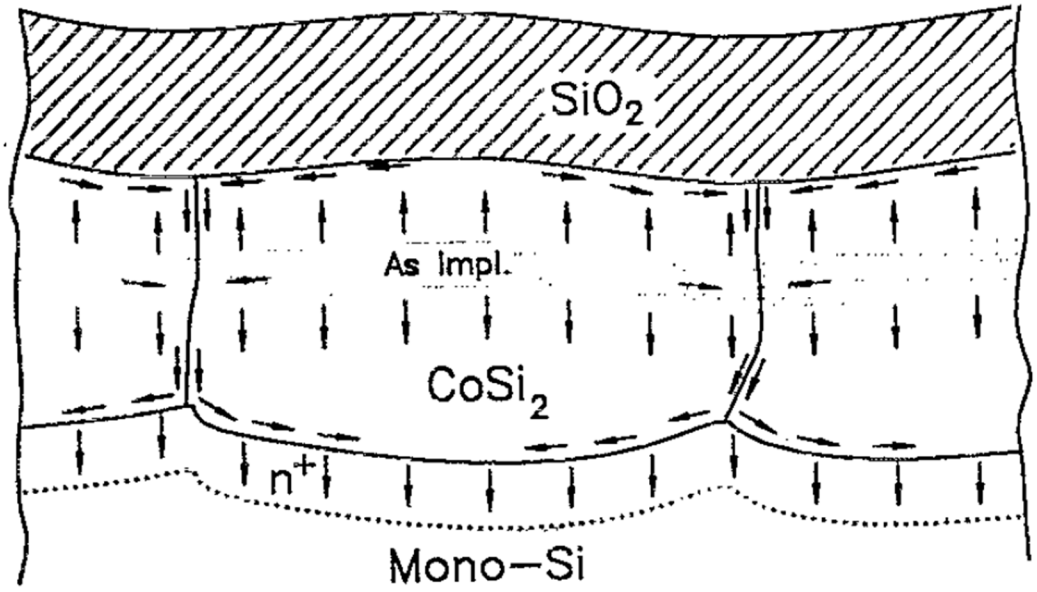

Figure 26: Conceptual Image Showing the Method by Which Dopant Atoms Leave the Cobalt Silicide and Enter the Crystalline Silicon [26]

Although it is just shown for arsenic here, it is shown in all of these studies that out diffusion of arsenic, phosphorous, and boron dopants from cobalt silicide occurs but is more

severe for arsenic and phosphorous dopants. Also, it can be seen that the magnitude of the dopant out diffusion from cobalt silicide is very considerable. Unfortunately, there is currently a lack of information on the distance of the dopant redistribution from the silicide/silicon interface as a result of the formation of an un-doped cobalt silicide on doped silicon. It is for this reasons that the exact cause of the deviation of the measured gate current from the simulated gate current cannot be specified beyond saying the it is either the result of an LDD doping or dopant redistribution.

Even with all of this said, the gate current in a MESFET that is properly/successfully integrated into the standard SOI CMOS process flow can still be very high due to tunneling if the standard channel/well doping in a process is sufficiently high. In the case of the MESFETs used for calibration of the model the standard channel doping was not sufficiently high which mandated further investigation into the causes of the large gate leakage current but this will not always be the case.

The tunneling current mechanisms in a MESFET can be understood by looking at the energy bands of the device for the given cutline as seen in Figure 27. Simulation data of a MESFET device with an LDD doping or dopant redistribution in the tunneling zone compared to experimental data can be seen in Figure 28.

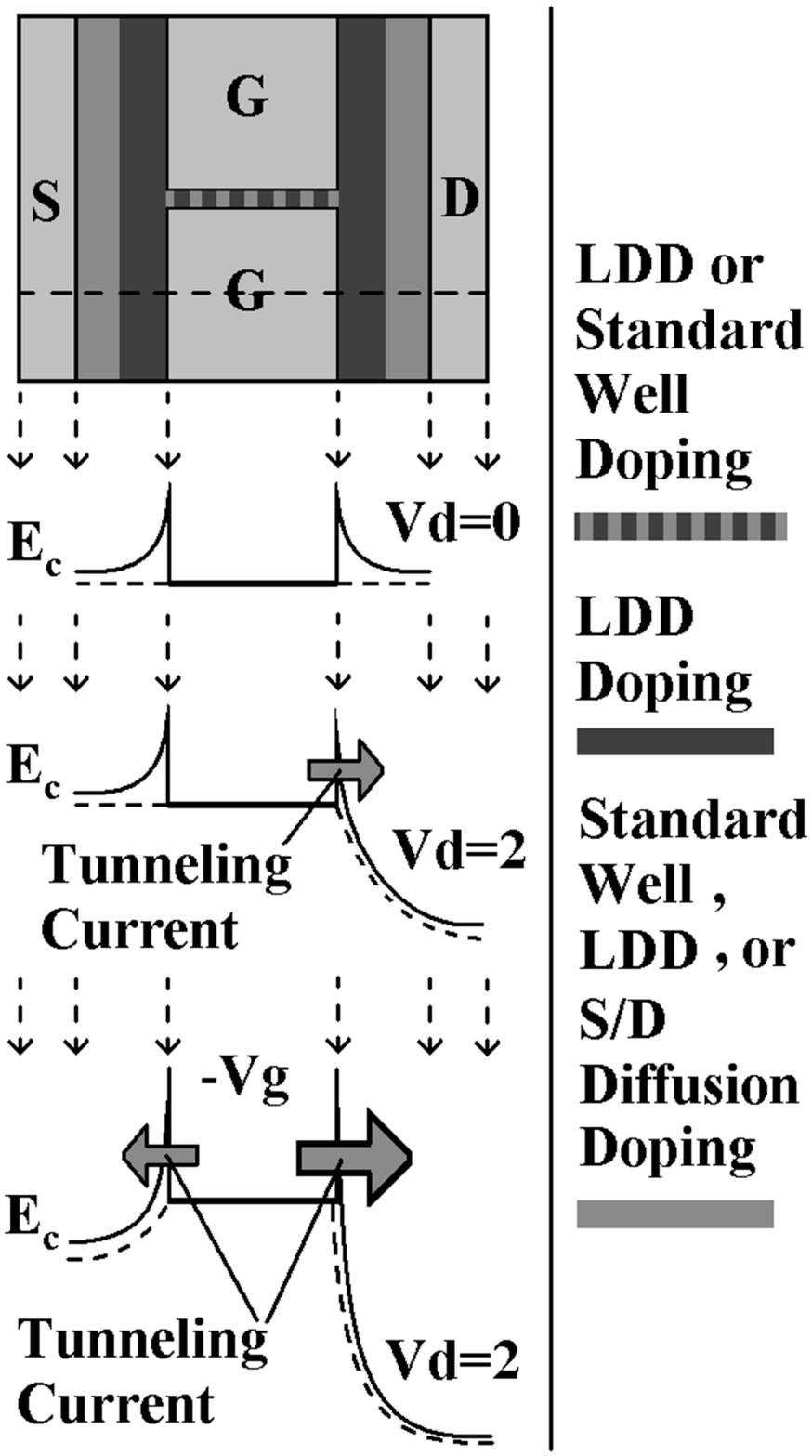

Figure 27: Tunneling Currents and Energy Bands (for the dashed cutline) in A MESFET with an LDD doping or dopant redistribution

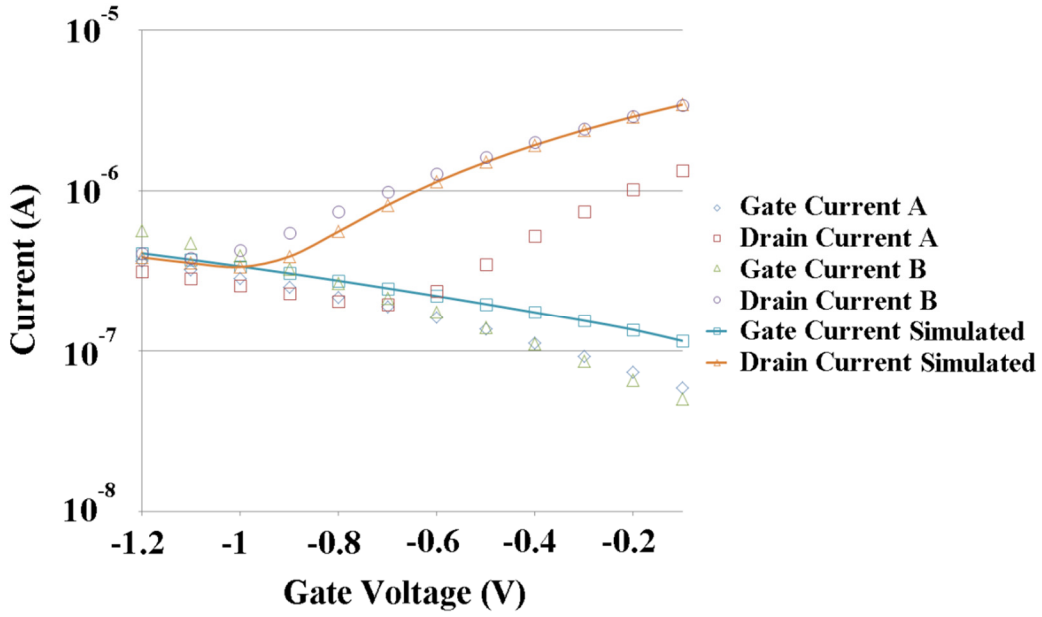

Figure 28: Simulated Tunneling Currents in A MESFET with an LDD doping or dopant redistribution

The gate leakage (tunneling and thermionic) of a MESFET is primarily determined by the work function of the gate material and the doping of the silicon around the gate. For a gate on n-type silicon, the gate tunneling current will increase very little as the work function of the gate material increases while the gate tunneling current will increase noticeably as the doping of the silicon around the gate increases. In contrast, for a gate on n-type silicon, the gate thermionic current will decrease as the work function and/or the doping of the silicon around the gate increases. If the doping in the silicon is sufficient (~>1 x 10^{17} which is a relatively low silicon doping in modern processes), the tunneling current will dominate the thermionic current the gate current will be much larger than predicted by the ideal Schottky diode equation. This will require the use of tunneling modeling in predictive TCAD simulation. The reason that the doping has the strongest effect on the gate tunneling current is the reduction in the thickness of the tunneling barrier of the gate is far greater from an increase in the silicon doping than an increase in the gate material work function. The most simple form of the Schottky barrier equation when solved for

the depletion width, which the tunneling barrier thickness is dependent on, has only a single term that is dependent on the gate material's work function while it has two terms that are dependent on the doping in the silicon: it is inversely proportional to the doping and proportional to the work function of the doped silicon which is proportional to the silicon doping. Since tunneling is proportional to the tunneling barrier thickness and not the barrier height, the greater the reduction in the tunneling barrier length the greater the tunneling current will be.

As the drain voltage of the MESFET rises above the ground potential (assuming that the source is at ground potential) the tunneling current from the drain to gate contact will dominate the tunneling current from the source to gate contact due to the elevated drain contact potential as seen in Figure 30. As a negative potential is applied to the gate, the Schottky tunneling barrier to the source and drain contacts will be reduced proportionally by the applied voltage. The elevated drain contact potential causes a larger reduction in the tunneling barrier on the drain side of the gate than on the source side of the gate which leads to the higher drain to gate tunneling current and the convergence of the gate and drain currents in the cutoff region of operation. So, the gate leakage current will increase not only as the gate potential decreases but also as the drain potential increases. This is an important trade off to keep in mind when using these MESFETs in a high voltage application. In addition to the previously stated effects, the combination of the elevated drain potential and the gate Schottky tunneling is the cause of the second substantial deviation of the experimental data from ideal simulation data: the delayed Schottky gate turn on/off voltage (applied gate voltage that yields the lowest gate current) as seen in Figure 22 through Figure 24 and Figure 29.

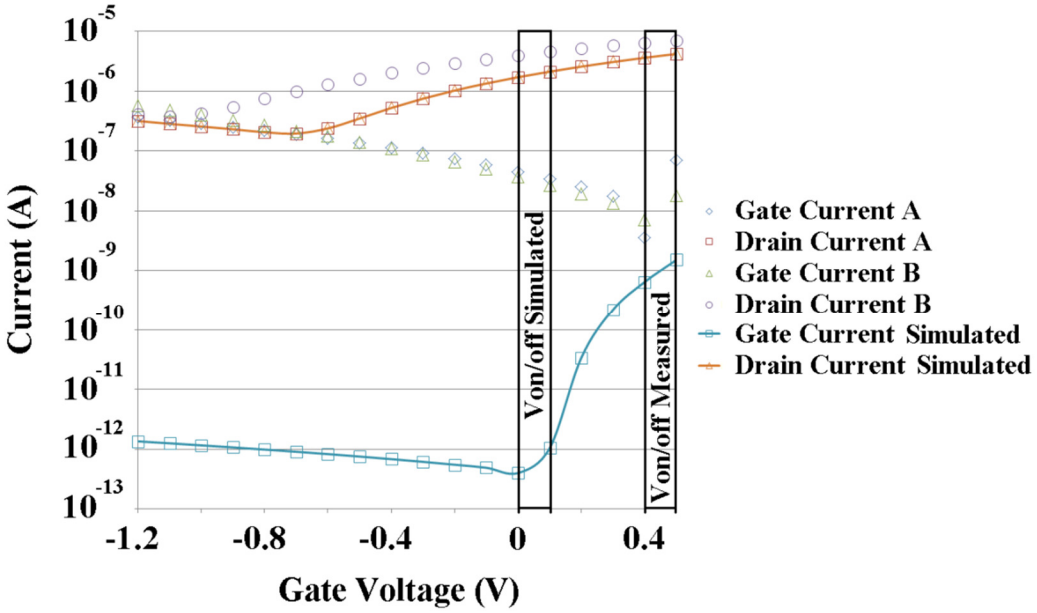

Figure 29:The Difference in Gate Diode On/Off Voltage Between Measured and Simulated Devices Without the Inclusion of Gate Tunneling in the Simulated Results

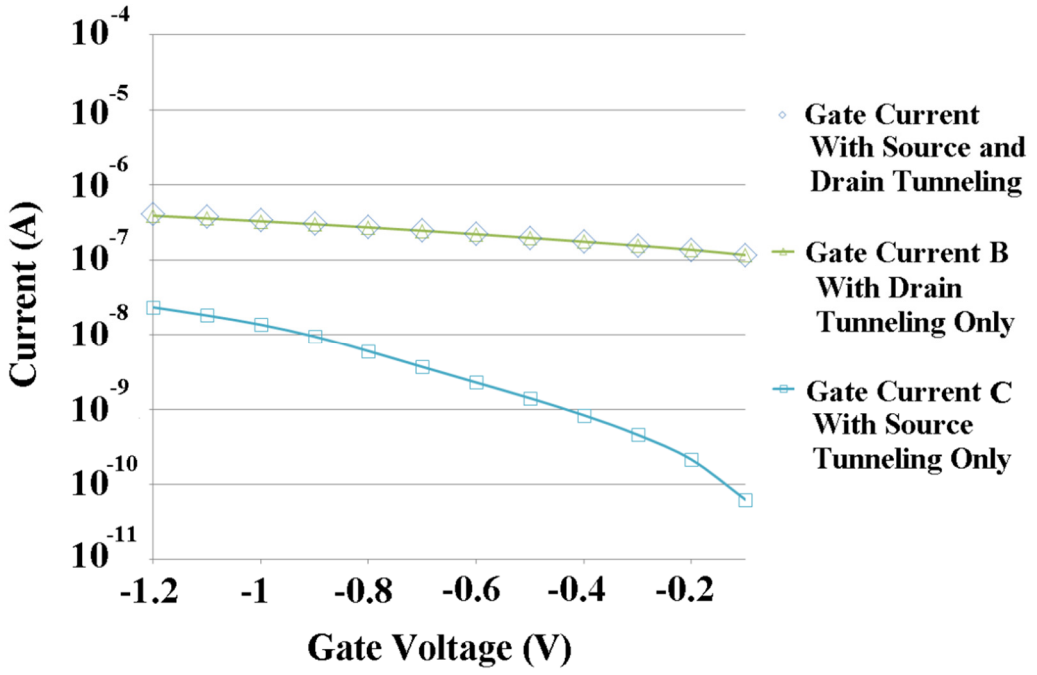

Figure 30: Simulated Tunneling Currents in A MESFET with an LDD doping or dopant redistribution. Vdrain = 2 V and Vsource = 0 V.

An ideal Schottky gate should turn off (the gate current would go to zero) when the gate potential is at the same potential as the source terminal. In the case of the calibration MESFETs this was shown in Figure 19, Figure 20, and Figure 21 not to be the case. This was discovered to be a result of the drain to gate tunneling at an elevated drain potential. The ideal Schottky diode current equation defines the diode current to be exponentially proportional to the difference in the voltage from the gate to the body of the diode. In the case of a MESFET, the body of the Schottky diode is the channel, the regions of the gate between the source and drain contacts, and the silicon underneath the gate (in the case of a PD MESFET). When the drain potential is elevated and the source potential is held at ground, although the potential in the silicon near the source side of the gate may be very close to ground potential, the potential of the silicon on the drain side of the gate is not at ground potential. The potential in the silicon on the drain side of the gate will be somewhere in between the source and drain potential as seen in Figure 31. The exact value can easily be solved for but is dependent on the region of device operation (in cutoff the potential drop across the device will be very nonlinear while in saturation it will be very linear) and many of the physical properties of the device (doping, channel width, channel length, etc…) so it is pointless to assign it an exact value for this part of the discussion. Therefore, since it was shown that the gate leakage current is dominated by the leakage out of the gate on the side of the MESFET device that has an elevated potential, the elevated potential in the silicon on the drain side of the gate is the potential at which the gate current will go to zero. The TCAD simulation program that was used in this thesis did not have the ability to properly converge while solving tunneling equations in this system due to the various and simultaneously occurring Schottky tunneling regions.

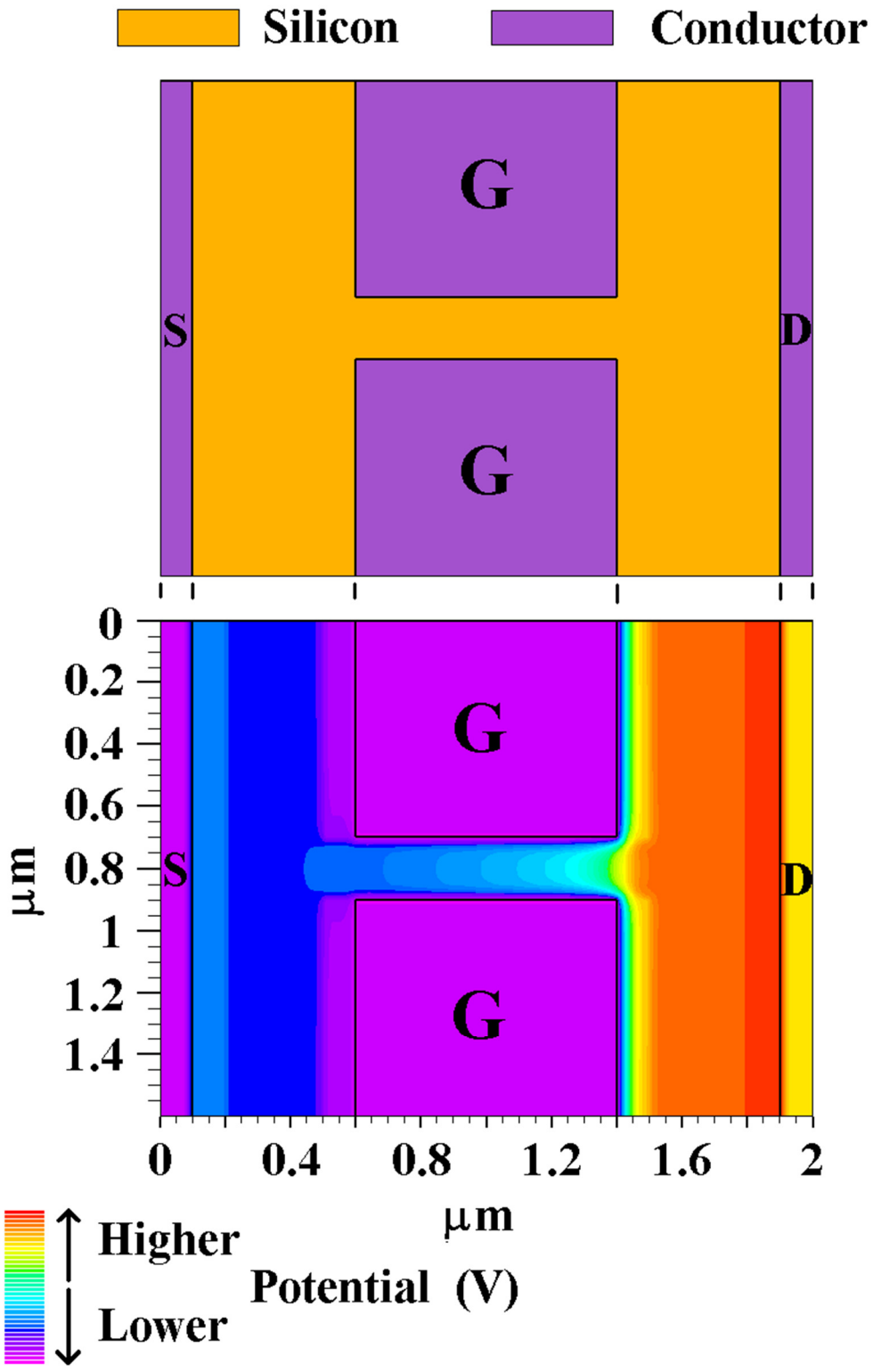

Figure 31: Potential Drop Across a Single Channel MESFET. Vdrain = 2 V and Vsource = 0 V.

The final substantial deviation of the experimental data from ideal simulation data was the large variation in experimental data obtained from supposedly identical MESFET devices on different die. Since all of the devices were tested at the same time using the exact same test setup and measurement process and the variation from die to die can be simulated by changing the parameters of the MESFET, it is thought that the large die to die variation is a result of the fabrication of the MESFETs. Through simulations it was found that an increase of 9 x 10^{16} (~50%) in the channel doping of the MESFET or a 60nm reduction in the gate spacing (30nm per channel) would cause the ideal MESFET simulated gate and drain current shown in Figure 22 to match the measured gate and drain current from die C in Figure 19. The majority of the other device parameters could also separately be altered in order in to replicate these variations in the experimental results but they will generally yield changes in the parameters that are unreasonable/non-physical and should not occur under normal processing conditions. An example of a device parameter that could be altered to a non-physical extent to simulate the die to die variation of the calibration devices is the $CoSi_2$ (gate) work function. An 11% increase in the work function of the $CoSi_2$ gate above the highest ideal (no surface pinning, just freestanding) $CoSi_2$ work function will successfully replicate the die to die variation of the calibration device but is simply not realistic. The ability to identify and ignore these false causes is crucial to preserving the accuracy, physicality, and effectiveness of the TCAD model.

These calibration MESFETs were made in a technology that was very much in development (MTILL 150nm process) at the time of their design and fabrication and to this day is continually being changed. This could either be a contributing factor or the primary reason as to why the die to die comparison of the electrical characteristics of the MESFET devices is so inconsistent.

The layers in the CMOS processes that are used to define the gate region of the MESFET are not critically controlled layers like those used to define the gate region of a MOSFET because they are not usually central to the CMOS fabrication flow. Though the tolerances are not listed in the MITLL PDK, with the fact that the critical dimensions in modern technology are allowed to vary by more than 10% (taken from a 45nm SOI process PDK), it is certain that the maximum

allowable percent variation in the noncritical dimensions of a process that is three minimum feature size generations older will be larger than that of a modern 45nm process and could be the cause of the large die to die variations.

Although the percent increase required to emulate the die to die results in the channel doping is five times greater than the percent increase in the $CoSi_2$ work function that was proclaimed unreasonable, the likeliness and ability of the dopant concentration to vary by this much between different die is acceptable due to the occurrence of leaching and redistribution of the dopants in the gate region of the channel during silicide formation. As previously discussed in chapter 2 and seen in numerous papers [7, 27-33], dopants in silicon directly in and around a region where a silicide is formed are bound to be redistributed in some form or another. Due to the relatively light doping in the channel region of the device in comparison to the doping in the source and drain regions and the ability of the formation of a silicide to leach more than an order of magnitude of the peak dopant concentration out of silicon films linger than 140nm (refer to Figure 12) if not properly fabricated (as is the case in all standard CMOS MESFETs), a percent change in the doping in the channel of this magnitude is not only reasonable but most likely, in conjunction with some variation in the channel separation as well, the cause for these large die to die variations.

3.3 CONCLUSION

In this chapter some of the non-ideal aspects of fabricating a MESFET in a standard SOI CMOS process were investigated. It was shown that if the MESFET device receives the MOSFET LDD doping or experiences dopant redistribution, the gate current in the cutoff and linear regions of operation of the MESFET will be increased proportionally to the doping concentration of the LDD. It was also shown that the zero gate current point in the operation of a MESFET is affected by the drain potential on the device such that a larger drain potential would move the zero gate current voltage in the positive direction in an amount proportional to the voltage applied to the drain.

The non-ideal effects of MESFET integration into the standard SOI CMOS process flow presented in this chapter are representative of the majority of the effects that MESFETs integrated into other SOI CMOS processes will be subject to. Although there are many MOSFET processing remnants that could make it into the fabrication of the MESFET other than the LDD doping, based on the current-voltage characteristics of other MESFETs that have been made in the processes mentioned in chapter one and the availability of PDK options to exclude the halo and sidewall dopings, they are usually left out of the MESFET fabrication. The only other MOSFET processing remnant that is most likely to make it into all of the MESFET made in every process is the threshold voltage adjust doping. This is not investigate or discussed in this chapter because the presence of the threshold adjust doping in this process technology has not been verified and even if it is present, it is not painfully evident from the measured data of the calibration MESFETs like the presence of an LDD doping or dopant redistribution is.

CHAPTER 4

MESFET OPTIMIZATION AND INNOVATIVE DESIGN

As discussed in the introduction, there are many different ways to layout and fabricate a MESFET. Each method has its unique advantages and disadvantages. These advantages and disadvantages are not solely defined by the electrical characteristics of a MESFET. Advantages of laying out and fabricating a MESFET with one method over another may range from superior drive current, to ease of multi-process integration, or enhanced reliability. Disadvantages are similarly diverse. In this section, the characteristics of different types of MESFET design will be presented in order to discuss the physical and electrical advantages and disadvantages that each design method possesses. Also, some innovative MESFET device design and layout will be presented.

4.1 FULLY DEPLETED MESFET

The fully depleted MESFET has two primary advantages and one primary disadvantage. The two primary advantages of the fully depleted MESFETs are that they can be integrated into any fully depleted CMOS SOI process and yield MESFETs with more easily controllable/designable threshold voltages, drive currents, and transconductances and they have a lower gate capacitance per unit area than PD MESFETs. The primary disadvantage is that the drive current will be much less than the drive current of a PD MESFET device of equivalent area. It is up to the designer and company to assess whether or not a fully depleted MESFET is appropriate for their application given these device qualities.

There are two different basic structures for a fully depleted MESFET: the joined channel FD (JCFD) MESFET and the separated channel FD (SCFD) MESFET. The structure a single channel of the JCFD MESFET can be seen in Figure 32 and the SCFD MESFET can be seen in Figure 33.

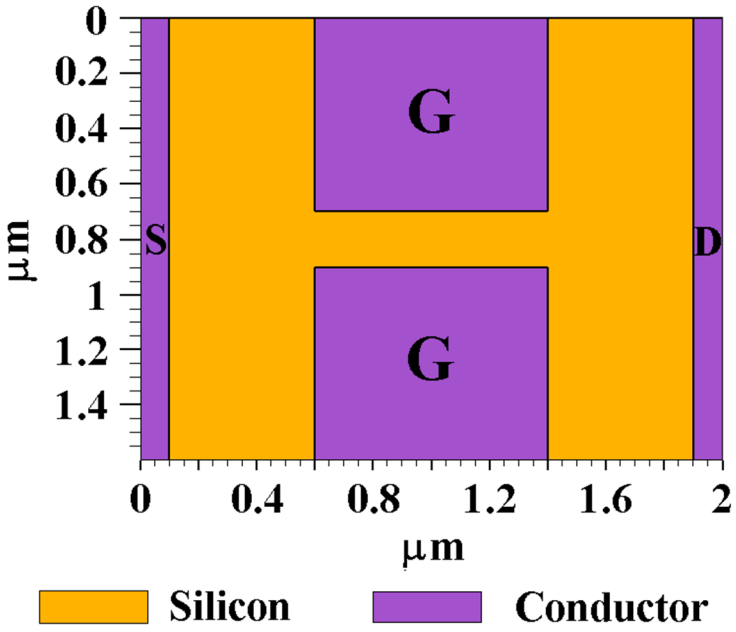

Figure 32: Single Joined Channel FD MESFET Device

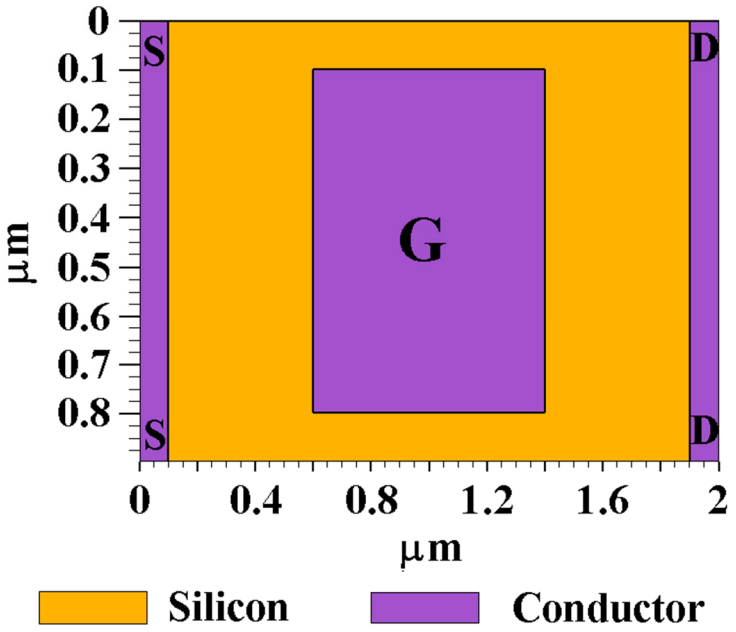

Figure 33: Single Separated Channel FD MESFET Device

Both devices in Figure 32 and Figure 33 are being shown in a plan view (the top of the wafer is pointing out of the page and the top of the BOX is located the thickness of the thin silicon

film into the page) and are surrounded by either LOCOS or STI oxides immediately outside of the colored areas. In the JCFD MESFET the drain to source current flows through the joined channel which is in between two gate contacts as shown in Figure 34. In the SCFD MESFET the current flows in the silicon in between the Schottky gate and the isolation oxide around the gate as shown in Figure 35.

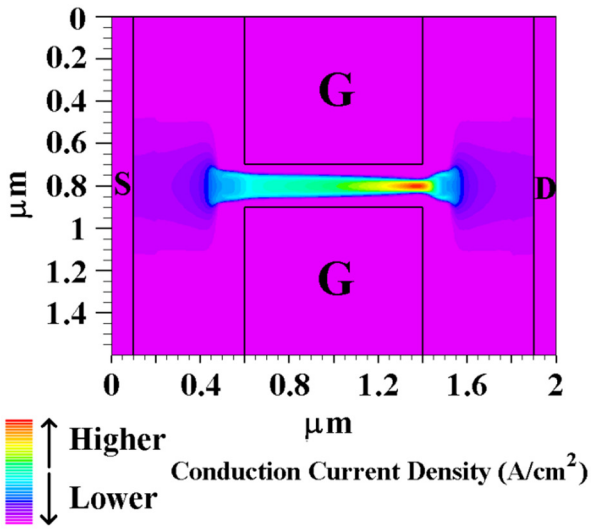

Figure 34: Conduction Current Density in a Single Joined Channel FD MESFET Device. Vdrain = 2V and Vsource = 0V.

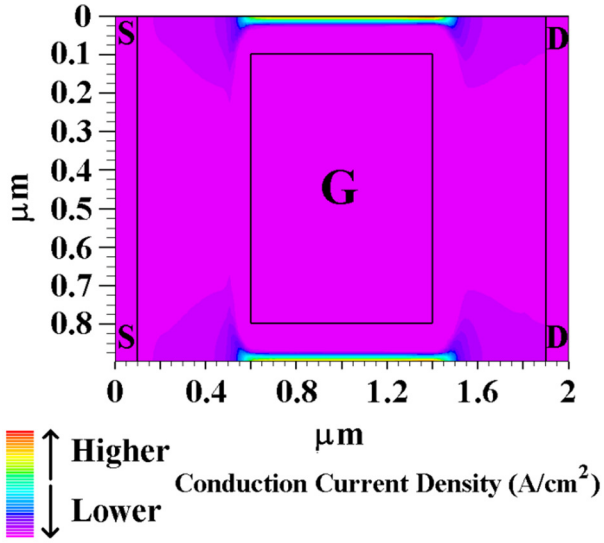

Figure 35: Conduction Current Density in a Single Separated Channel FD MESFET Device. Vdrain = 2V and Vsource = 0V.

In this thesis, the phrase “channel width” is used to refer to a design quantity that is used in the calculation of a MESFETs threshold voltage. This channel width design quantity is used to refer to the orthogonal distance from the gate of the MESFET that the active area silicon will be fully depleted of majority carriers when the gate is held at the threshold potential and the drain and source are held at ground potential which can be obtained from Equation 4.8. This is defined here to maintain clarity in the following discussion.

Since the JCFD MESFET has a gate on each side of the channel, the gate to gate spacing must be twice that of the channel width. It can also be thought of as having two channels side by side. Since a single channel JCFD MESFET has one gate per effective channel and a single channel SCFD MESFET has one half of a gate per channel, the gate area is reduced by slightly more than 50% which makes the gate leakage current of a single channel SCFD MESFET up to 10 times lower than the JCFD MESFET. Also, the area of a single channel SCFD MESFET is 44% less than the area of a single channel JCFD MESFET. However, as both FD MESFET devices are expanded to have multiple fingers (~>10) their geometries converge as seen in Figure 36. In order to increase the width of a JCFD MESFET the joined channel unit cell extensions are added to the joined channel unit cell base. To increase the width of a SCFD MESFET the separated channel unit cells are added to the separated channel unit cell base which is the same as the separated channel unit cell. It can be seen in Figure 36 that the area of the joined channel unit cell extension is the same as the separated channel unit cell. This means that as both FD MESFET types become large they become virtually the same device, and gate leakage currents converge to towards that of a single channel SCFD MESFET multiplied by the one half the number of device channels since both wide FD MESFETs will have approximately one gate per channel.

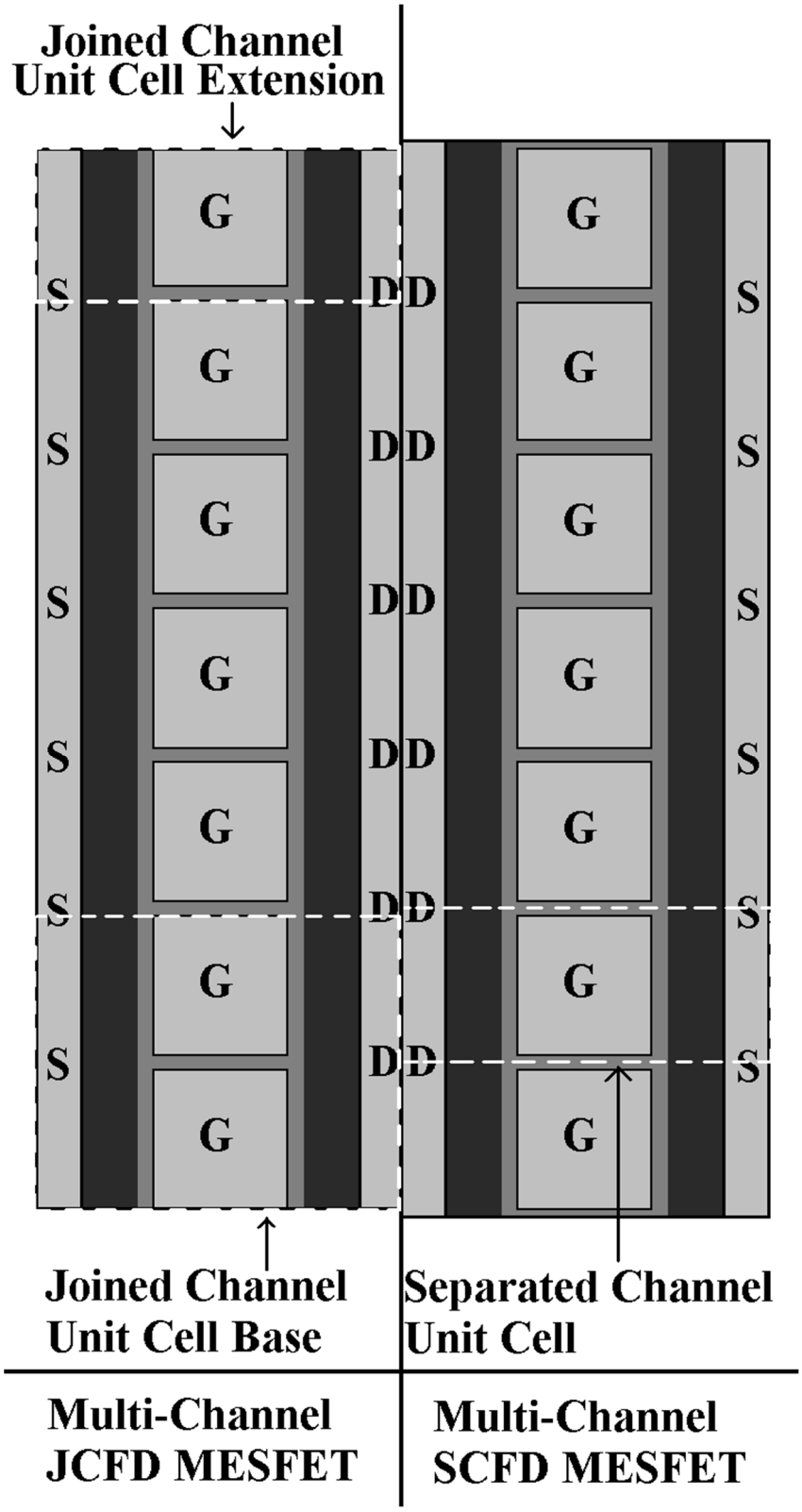

Figure 36: Multi-Channel FD MESFET Layouts with JDFD Unit Cells and SCFD Unit Cell.

Although it may seem pointless to make a distinction between the two different types of FD MESFETs since almost all MESFET devices integrated into a CMOS process are going to be much wider than the minimum width, due to the applications for which a MESFET is the most advantageous device [4], there are some MESFET applications that may use a minimum width device. In these cases the SCFD MESFET would be the more advantageous device to use due to its lower gate current. A few examples of the applications where a SCFD MESFET could be better are: the output stage of a high output impedance amplifier, a low dropout power regulator's error amplifier circuitry, or a radiation sensor.

Simulation results for both FD MESFET device types can be seen in Figure 37 through Figure 40. Note that although the gate currents in the simulation results are inaccurate, for reasons previously discussed about tunneling convergence problems with the TCAD software in the forward bias region, they will still reflect the trend that the device to device gate currents possess. In other words, the gate currents magnitude's for a given device type will be inaccurate but their magnitude's relative to the gate currents in the simulation results of another device type will be accurate in showing which device type will have a higher or lower relative gate current.

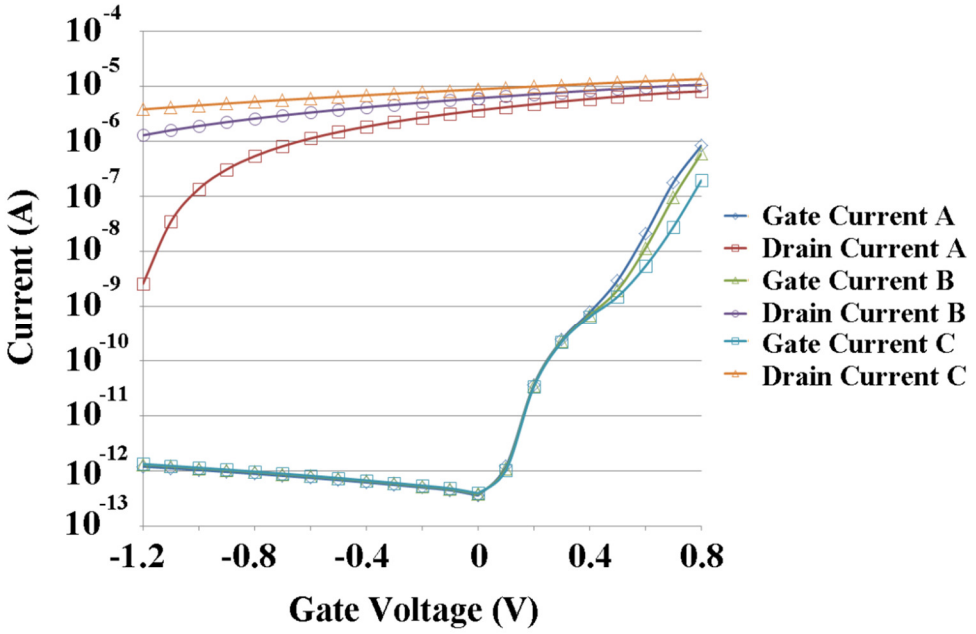

Figure 37: Simulation Results of a Single Channel JCFD MESFET With an L_{ad} of 500nm and a Gate Separation of (A) 200nm (Channel Length of 100nm), (B) 250nm (Channel Length of 125nm), and (C) 300nm (Channel Length of 150nm).

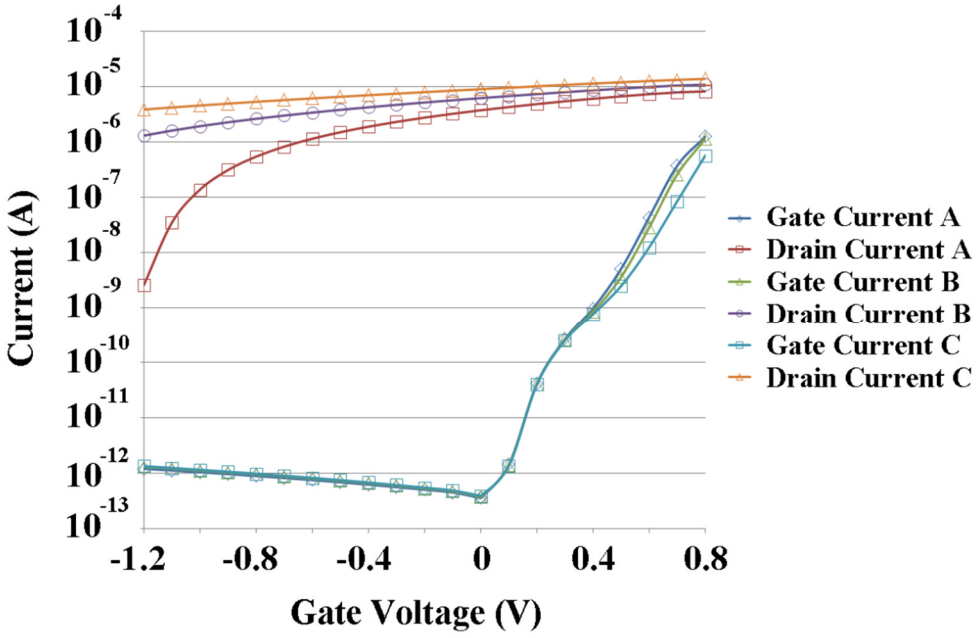

Figure 38: Simulation Results of a Single Channel JCFD MESFET With an L_{ad} of 250nm and a Gate Separation of (A) 200nm (Channel Length of 100nm), (B) 250nm (Channel Length of 125nm), and (C) 300nm (Channel Length of 150nm).

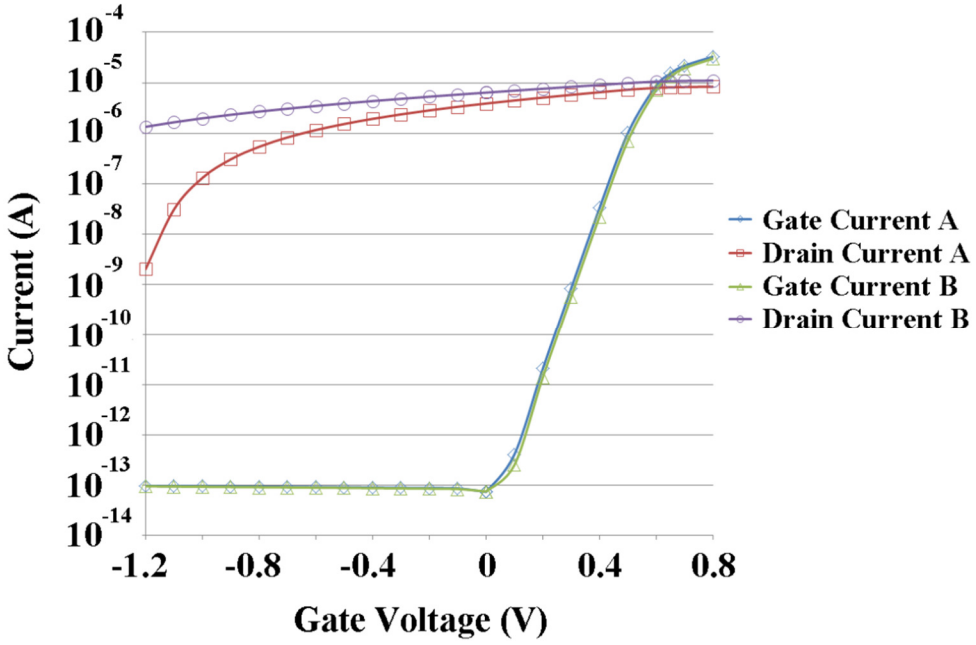

Figure 39: Simulation Results of a Single Channel SCFD MESFET With an L_{ad} of 500nm and a Channel Length of (A) 100nm and (B) 125nm.

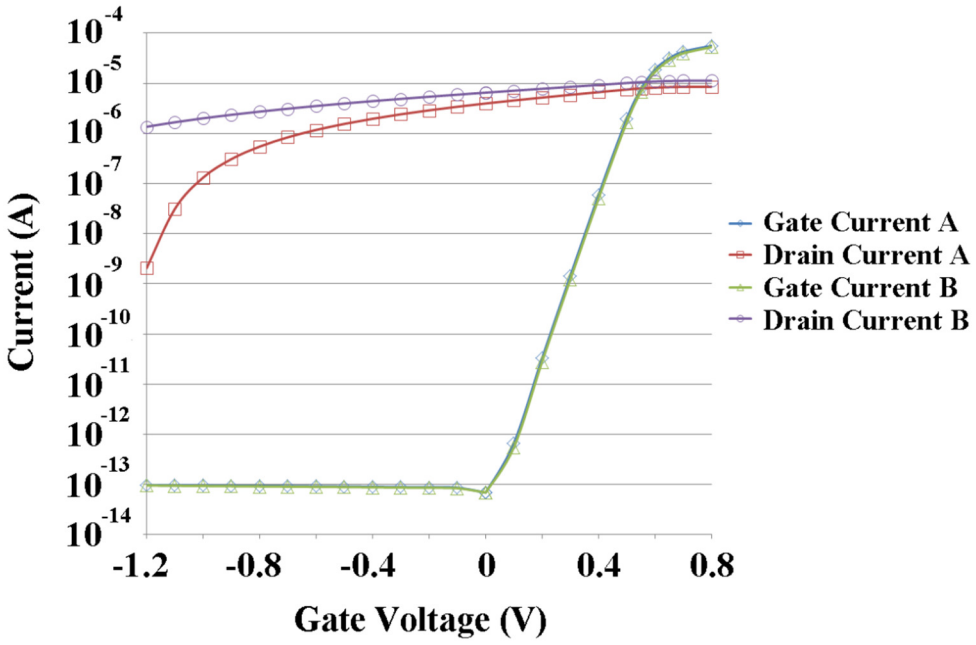

Figure 40: Simulation Results of a Single Channel SCFD MESFET With an L_{ad} of 250nm and a Channel Length of (A) 100nm and (B) 125nm.

It appears from Figure 37 through Figure 40 that the source and drain access lengths have very little influence on the DC operation of the MESFET device. The largest increase in drain current for the JCFD and SCFD MESFETs from the reduction of both L_{ad} and L_{as} for 500nm to 250nm was 2.02%. Though this makes it seem like the L_{ad} and L_{as} have almost no influence on the device, the magnitude of the effect of L_{ad} and L_{as} can be seen when the results are normalized to the unit cell or to area. The smallest percent increase in current per unit cell and current per area from changing L_{ad} and L_{as} from 500nm to 250nm for the JCFD and SCFD MESFET is 9.2% and 35.2% respectively. These minimum values are for the peak current (vg = 0.8 V) and decrease to 1.24%, 7.73%, and 33.4% for the simulated current, current per unit cell, and current per area respectively when the device is turned off (vg = -1.2 V). The reason for the decrease is that the ratio of the resistance of the silicon in between the source/drain contacts and the gate to the resistance of the silicon through the length of the channel region reduces as the gate voltage becomes more negative. However, the ratio of the resistance of the silicon in between the source/drain contacts and the gate to the resistance of the silicon through the length of the channel region is already very small for the majority of the operation of the device. This leads to the majority of the potential being dropped across the length of the channel and means that there is very little potential drop across the drain and source access lengths as seen in Figure 41 and Figure 42. Therefore, the resistance of the L_{ad} and L_{as} regions does not play a limiting role in the drain to source current in these MESFET devices. This in combination with the extreme dependence of the percent increase in current on whether or not the current is normalized shows that though there is a very small gain in the current of the device when reducing L_{ad} and L_{as} from 500nm to 250nm there is a very substantial gain in the current per area; meaning, the current in the device remains almost the same but there is a substantial reduction in that area that the device consumes.

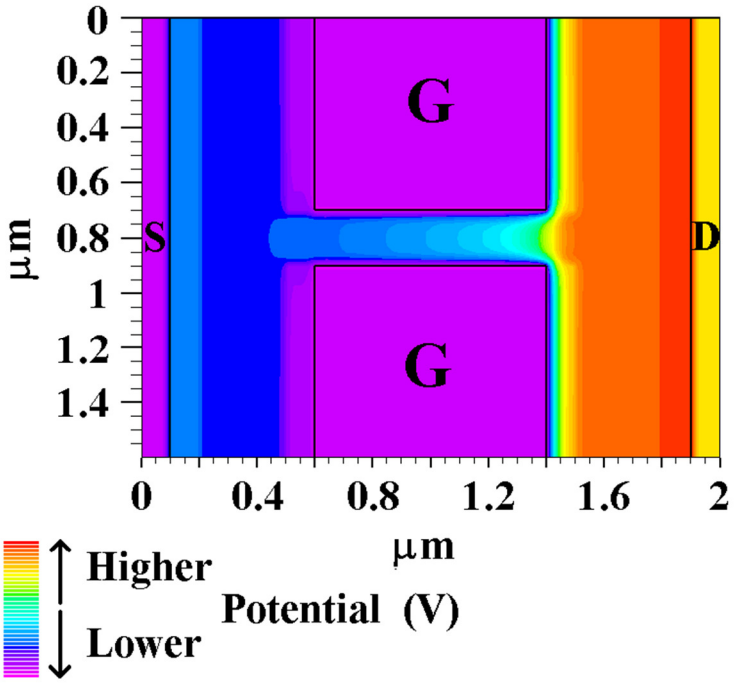

Figure 41: Potential Drop Across a Single Channel JCFD MESFET With an L_{ad} of 500nm and a Channel Length of 100nm. Vdrain = 2V and Vsource = 0V.

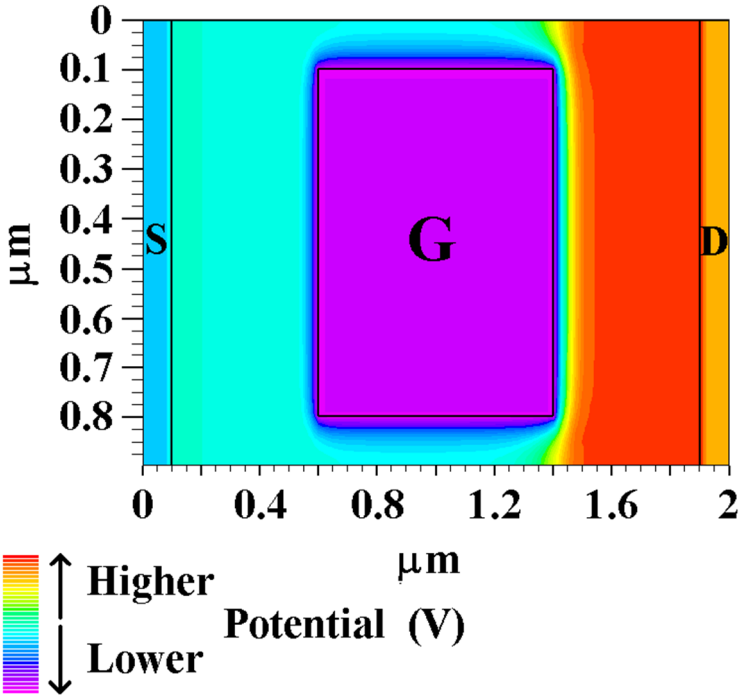

Figure 42: Potential Drop Across a Single Channel SCFD MESFET With an L_{ad} of 500nm and a Channel Length of 100nm. Vdrain = 2V and Vsource = 0V.

Though the results of the reduction of the L_{ad} and L_{as} from 500nm to 250nm are good, a larger current is achieved while reducing the device area by 19.2%, the purpose of making a device with a larger L_{ad} and L_{as} is to increase the breakdown voltage of a MESFET. From the simulation results that were obtained, there was a minimum reduction of 0.91% and a maximum reduction of 14.55% in the electric field across L_{ad} and L_{as} regions of the MESFET unit cell separately. There was a minimum reduction of 50.46% and a maximum reduction of 57.28% in the electric field across the channel of the MESFET unit cell. This reduction in the electric field should help increase the breakdown voltage of the FD MESFETs as expected.

4.2 PARTIALLY DEPLETED MESFET

The partially depleted MESFET has one primary advantage and three primary disadvantages. The one primary advantage is that the drive current will be much higher than the drive current of any FD variation of the MESFET device of equivalent area. The three primary disadvantages of PD MESFETs are: they can be difficult to integrate into a partially depleted CMOS SOI process; even if it is successfully integrated in a partially depleted CMOS process they will not yield MESFETs with easily controllable/designable threshold voltages because the doping of the device is the only parameter that the designer *may*, since there is no guarantee that multiple device dopings will be available for designer specified use, be able to use to control the threshold voltage; and they have a higher gate capacitance per unit area than FD MESFET devices. Partially depleted MESFETs integrated into standard SOI CMOS processes will however still yield MESFETs with controllable transconductances regardless of whether or not the designer has access to multiple device dopings. It is up to the designer and company to assess whether or not a partially depleted MESFET is appropriate for their application given these device qualities.

There is one basic structure for a partially depleted MESFET and one experimental structure being presented in this thesis: the partially depleted (PD) MESFET and the epitaxial stack PD (ESPD) MESFET. The structure of the PD MESFET can be seen in Figure 43 and the ESPD MESFET can be seen in Figure 44.

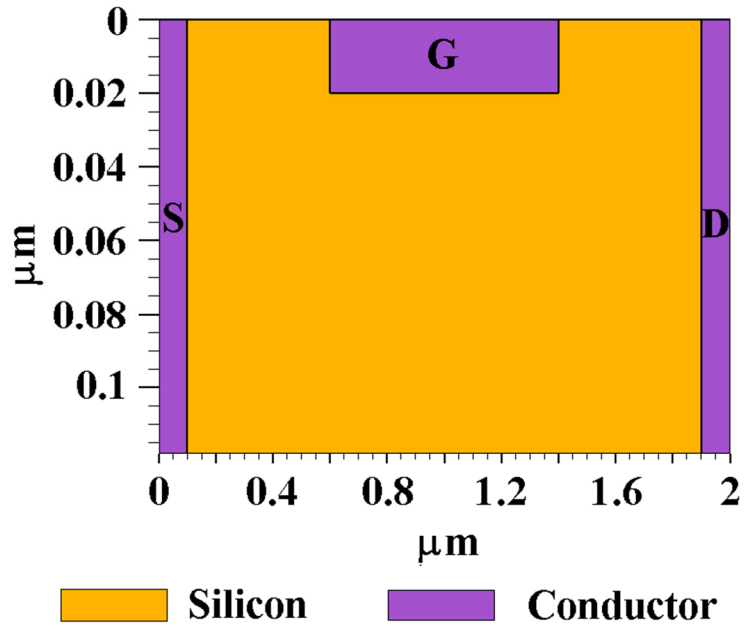

Figure 43: Partially Depleted MESFET Device in 120nm Thick Thin Film SOI (100nm Channel Length).

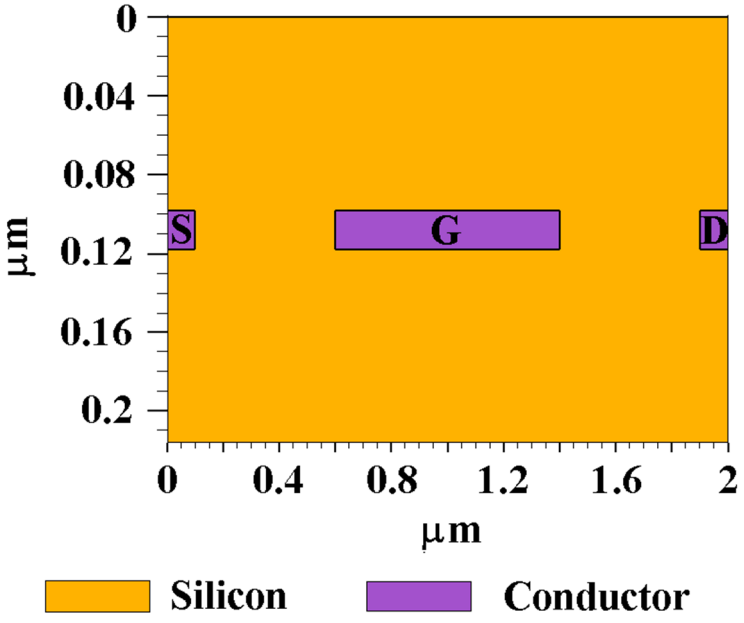

Figure 44: Epitaxial Stack Partially Depleted MESFET Device in 120nm Thick Epitaxial Thin Film SOI (100nm Channel Length).

Both devices are being shown in a cross sectional view, the top of the wafer is located at 0 on the y axis and the top of the BOX is located at 120nm on the y axis for the PD MESFET and 240nm on the y axis for the ESPD MESFET in Figure 43 and Figure 44. In the PD MESFET the drain to source current flows in the channel which is below the gate contact as shown in Figure 45. In the ESPD MESFET the current flows in the two channels comprised of the silicon above and below the Schottky gate as shown in Figure 46.

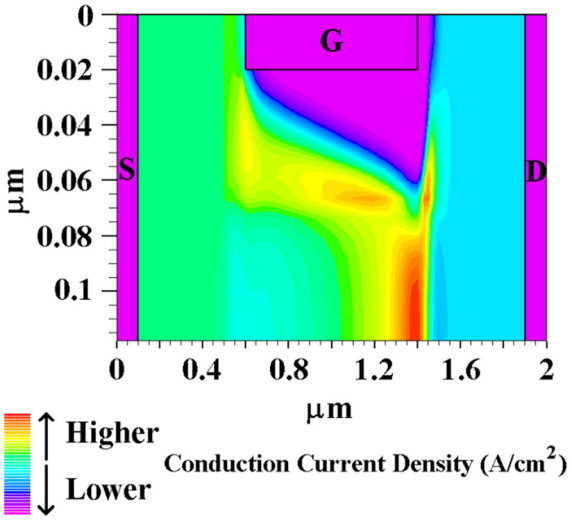

Figure 45: Conduction Current Density in a PD MESFET Device. Vdrain = 2V and Vsource = 0V.

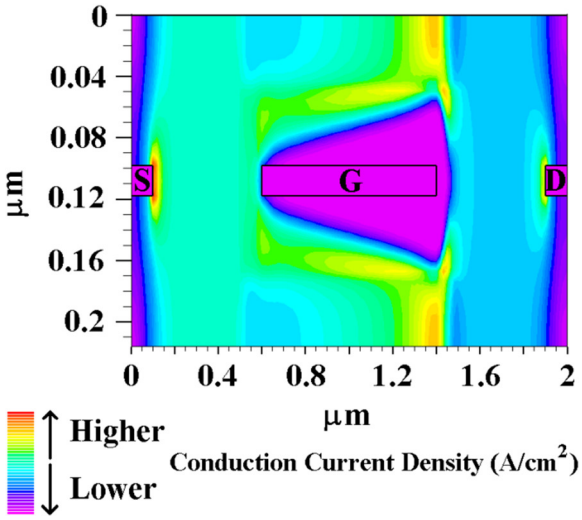

Figure 46: Conduction Current Density in an ESPD MESFET Device. Vdrain = 2V and Vsource = 0V.

The previously stated definition of channel width in the FD MESFET section holds true and remains the same for used in the design and discussion of PD MESFETs. Similar to the SCFD MESFET, the ESPD MESFET had one gate in the middle of two channels while the PD MESFET has one gate the rests above a single channel. This means that both the ESPD MESFET and the PD MESFET have one half of a gate per channel; however, the total gate area of the PD MESFET is approximately 50% of the total gate area for the ESPD MESFET which means the gate leakage current of PD MESFET could be to 10 times lower than the ESPD MESFET. Both the PD and ESPD MESFET devices have the exact same area as their plan view geometries are identical. Though the gate of the PD MESFET is accessed in the same simple manner as the FD MESFETs, the ESPD MESFET requires more care. If the gate of the ESPD MESFET is accessed frequently through the epitaxially grown silicon region above the gate in order to maintain good control of the gates potential (due to higher resistivity of silicides than BEOL metals) and adequate current paths then there will not be an area increase but the electrical characteristics of the MESFET may be slightly altered as each gate contact will block one of the two channels of the device in the region that it is contacted and provide a much larger gate area which will increase the gate leakage. These effects will or will not be substantial based on the total area/width of the ESPD MESFET device and the number of gate contacts but since the current per area is very high it is likely that the majority of ESPD MESFETs will be relatively small. If the gate is accessed only at the edges of the device than there may be the issues listed above but there will be less of an impact on the ideal operation of the device. Regardless of the number of gate contacts chosen, each access to the drain and source of the ESPD MESFET will only improve the electrical characteristics of the device by providing better potential control of the channel and more contact area for the source and drain thereby lowering the S/D contact resistance.

The standard layout of the PD MESFETs is seen in Figure 47. To increase the width of any PD MESFET, unit cells are repetitively added to each other until the device is the desired with. Additional fingers may be added as well in the same manner that they are done with MOSFETs in order to make the area of the MESFET more like a square than a long rectangle for an enhanced flexibility of integration into IC designs.

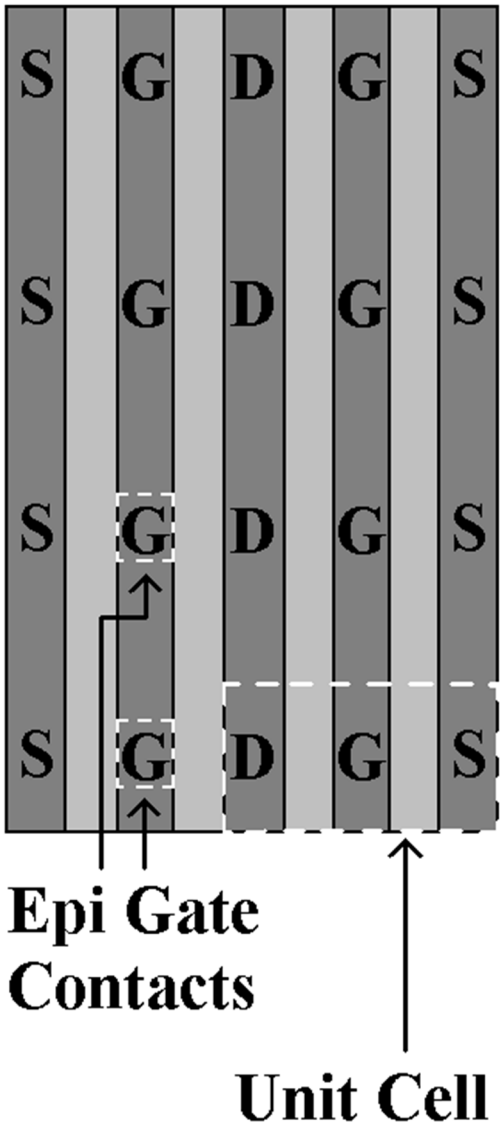

Figure 47: Plan View of a Multi-Channel ESPD or PD MESFET Layout with Unit Cell and ESPD Gate Contact.

The PD MESFET can be integrated into any PD CMOS SOI process with a varying degree of success. All of the electrical characteristics of the PD MESFET except for the drive current, which is controlled by scaling of the width of the device, will be entirely dependent on the thickness of the thin film layer and the device dopings offered/available from the process that they are fabricated in. If none of the device dopings offered by a technology in combination with the thickness of the thin silicon film form a PD MESFET with desirable electrical characteristics then

it is said that the PD MESFET cannot be integrated into that process. This is said to be a failure. There are many varying degrees of success in between a failure and a complete success where a PD MESFET may have a very low threshold voltage leading to a poor drive current with a reduced region of operation but a very good sub-saturation slope or a very high threshold voltage leading to a very poor on current to off current ratio and sub-saturation slope. If done properly, choosing a process with a suitable thin silicon film thickness and device dopings, a suitable PD MESFET can be designed. The design of the PD MESFET should be done in the same manner as the design of the FD MESFET in that the threshold voltage should be said to be the point at which the silicon in the length of the channel is fully depleted.

The most dangerous aspect of integrating a PD MESFET into a standard PD CMOS SOI process is the retrograde channel bottom doping. Often, in PD CMOS SOI processes, the bottom half or third of the thin silicon film below a MOSFET device will have a doping that is much higher than the actual device channel doping. This is done so that a PD device can be achieved on a silicon film far thinner or much more lightly doped than a PD device on a thin silicon film with a uniform doping that would otherwise yield a FD MOSFET. If this is done it will not be obvious from the PDK parameters unless it is specifically stated. A high doping at the bottom of the thin silicon film below a PD MESFET would make the MESFET useless as the gate of the transistor will not be able to fully deplete the higher doped region in order to pinch off the channel and turn the device off. Also, the effect of the control of the gate on the lightly doped region between the gate and the highly doped region on the operation of the device will be very weak as the highly doped silicon will have a much smaller resistance than the lighter doped silicon. It can be thought of there being a small resistor, the heavily doped region which the gate has very little control over, and a large resistor, the lightly doped region under the gate which the gate does have control over, in parallel in between the drain and source. Modulation of the resistance of the big resistor will have very little effect on the drain to source resistance because all of the current will flow through the small resistor which the gate has little control over. The modulation of the resistance of the big resistor will only have a significant effect on the drain to source current when its value reduces to be on the order of the magnitude of the resistance of the highly doped region. This may never

occur depending on the doping of the device channel and in the end the MESFET will look like a poorly controlled resistor.

It should be obvious that the ESPD MESFET will be much more difficult to integrate into a process and cannot be integrated into a standard CMOS SOI process. The ESPD MESFET will only be able to be integrated into a process that uses vertical devices such as HBT's or made in a university fabrication facility as they require an epitaxial layer of silicon to be grown on top of the silicide contacts. It has been seen in the literature that obtaining a epitaxial silicon layer or reasonable thickness and uniformity in order to make an ESPD MESFET is not impossible [12, 34, 35]. It is presented in this thesis as an idea that should be pursued due to its very favorable electrical characteristics.

Simulation results for both PD MESFET device types can be seen in Figure 48 through Figure 51. Note that the accuracy and purpose of the gate currents shown in these graphs possess that same stipulations stated previously in the fully depleted MESFET section.

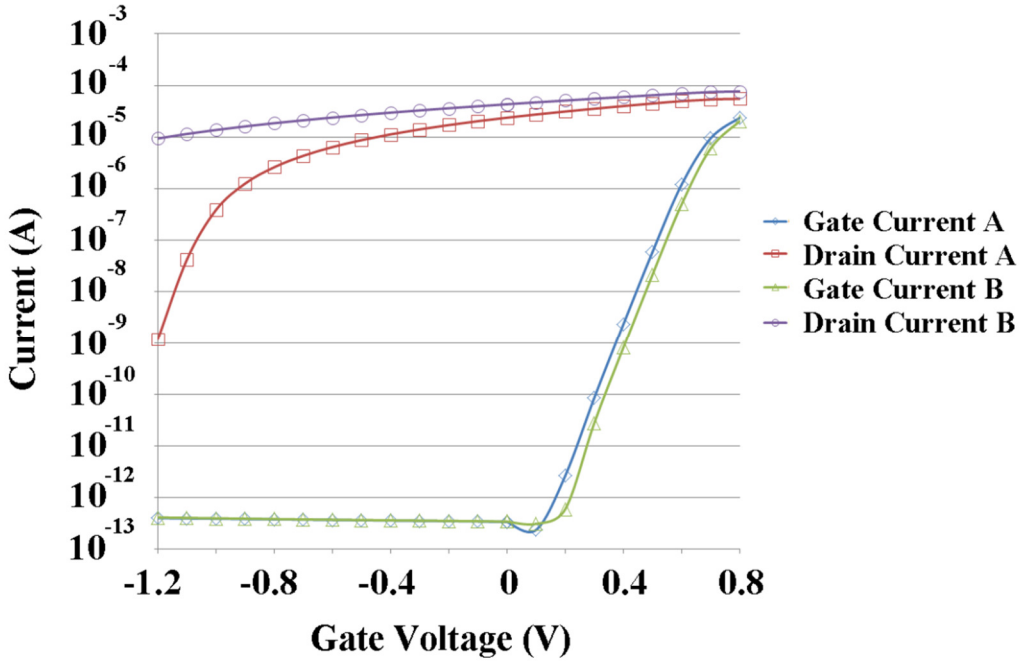

Figure 48: Simulation Results of a 700nm Wide PD MESFET With an L_{ad} of 500nm and a Channel Length of (A) 100nm and (B) 125nm.

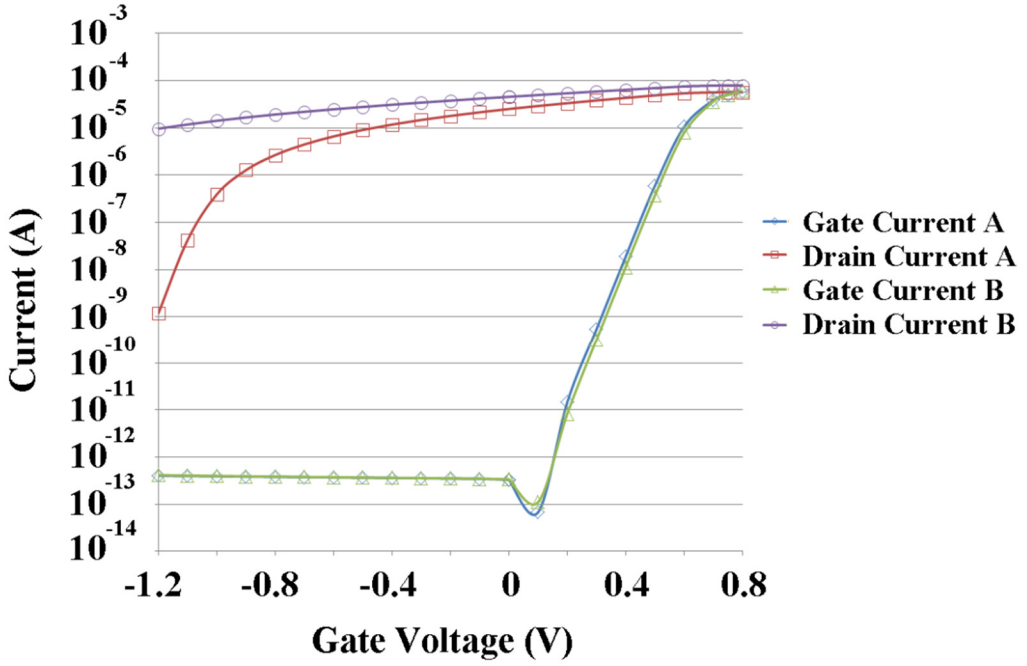

Figure 49: Simulation Results of a 700nm Wide PD MESFET With an L_{ad} of 250nm and a Channel Length of (A) 100nm and (B) 125nm.

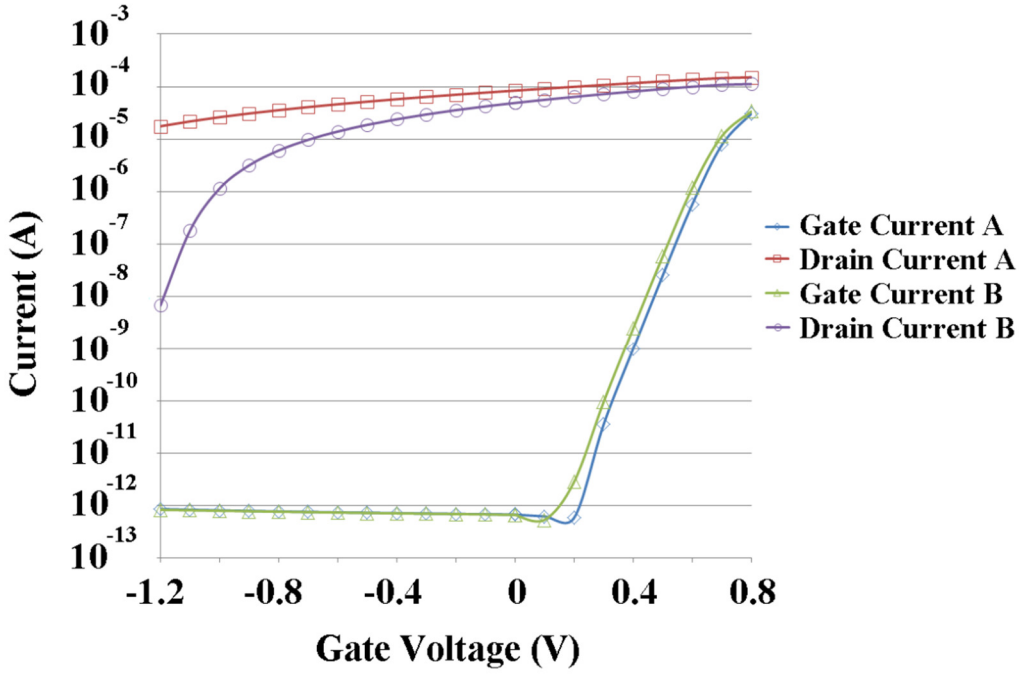

Figure 50: Simulation Results of a 700nm Wide ESPD MESFET With an L_{ad} of 500nm and a Channel Length of (A) 100nm and (B) 125nm.

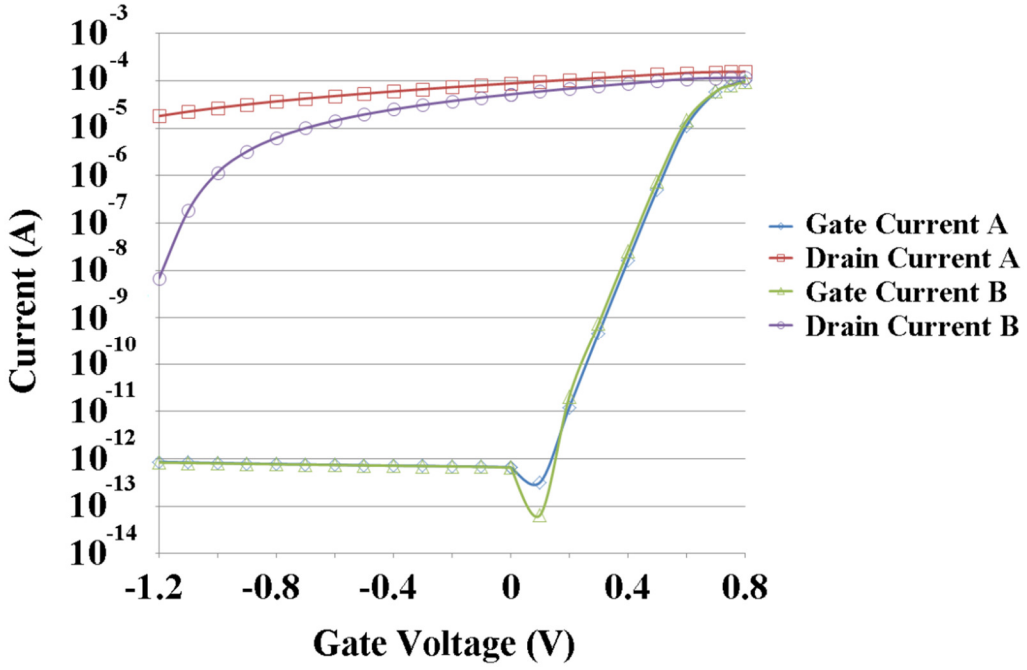

Figure 51: Simulation Results of a 700nm Wide ESPD MESFET With an L_{ad} of 250nm and a Channel Length of (A) 100nm and (B) 125nm.

Just like with the FD MESFETs, it appears from Figure 48 through Figure 51 that the source and drain access lengths have very little influence the DC operation of the PD MESFET devices. The largest increase in drain current for the PD and ESPD MESFETs from the reduction of both L_{ad} and L_{as} for 500nm to 250nm was 3.81%. Though this makes it seem like the L_{ad} and L_{as} have almost no influence on the device, the magnitude of the effect of L_{ad} and L_{as} can be seen when the results are normalized to the unit cell or to Area. The smallest percent increase in the on current per unit cell and current per area from changing L_{ad} and L_{as} from 500nm to 250nm for the PD and ESPD MESFET is 11.15% and 37.6% respectively. These minimum values for the peak current (Vg = 0.8 V) decrease to 2.57%, 7.7%, and 33.3% for the simulated current, current per unit cell, and current per Area respectively when the device is turned off (Vg = -1.2 V). The reason for the decrease is the same as explained in the FD MESFET section and once again the current in the device remains almost the same as the L_{ad} and L_{as} are decreased from 500nm to 250nm while there is a substantial reduction in that area that the device consumes leading to a

much higher current per unit area value. The potential drop across the devices can be seen in Figure 52 and Figure 53.

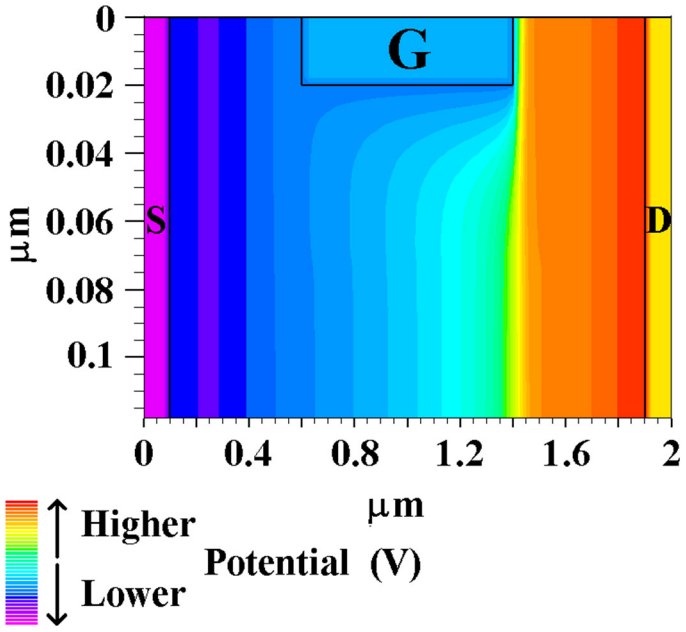

Figure 52: Potential Drop Across a PD MESFET With an L_{ad} of 500nm and a Channel Length of 100nm. Vdrain = 2V and Vsource = 0V.

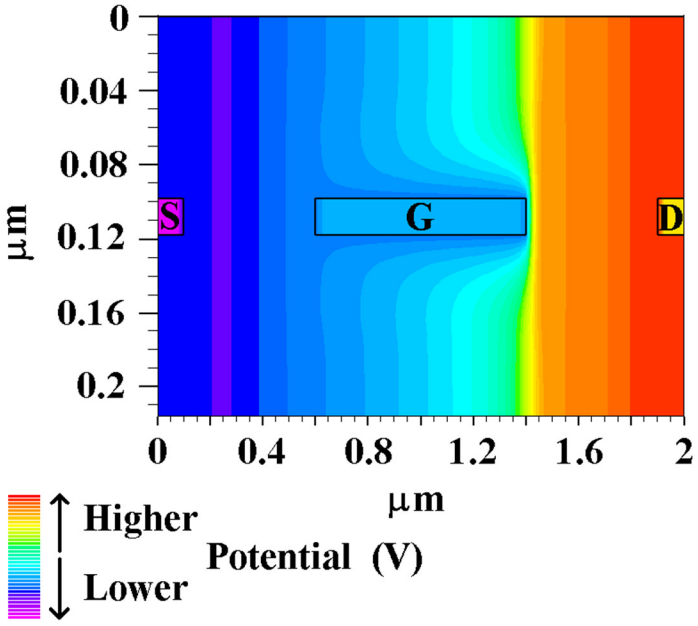

Figure 53: Potential Drop Across a ESPD MESFET With an L_{ad} of 500nm and a Channel Length of 100nm. Vdrain = 2V and Vsource = 0V.

Though the results of the reduction of the L_{ad} and L_{as} from 500nm to 250nm are good, a larger current is achieved while reducing the device area by 19.2%, the purpose of making a device with a larger L_{ad} and L_{as} is to increase the breakdown voltage of a MESFET. From the simulation results that were obtained, there was a minimum reduction of 2.05% and a maximum reduction of 24.26% in the electric field across L_{ad} and L_{as} regions of the MESFET unit cell separately. There was a minimum reduction of 51.02% and a maximum reduction of 62.13% in the electric field across the channel of the MESFET unit cell. This reduction in the electric field should help increase the breakdown voltage of the PD MESFETs more effectively than in the FD MESFETs since the magnitude of the decrease in the electric field is larger.

4.3 COMPARISON AND SUMMARY

In the previous section, the advantages and disadvantages of PD and FD MESFETs were discussed with respect to design, ease of integration, and the device physics. As this thesis is about the optimization of a MESFET to obtain high drive current, it is necessary to provide some of the most important electrical characteristics of the different MESFET types for comparison and discussion. Some of the best electrical characteristics that can be used as device metrics can be seen in Table 2.

Table 2: MESFET Device Type Electrical Characteristics Comparison and Summary

MESFET Device Type Electrical Characteristics Comparison and Summary						
MESFET Device Type			JCFD	SCFD	PD	ESPD
Varied Length Parameters	L_{ad} (nm)	L_{cw} (nm)				
Id On Current per Area ($\mu A/ \mu m^2$)	500	100	3.51	3.51	30.3	61.6
		125	4.38	4.38	42.1	82.6
		150	5.25	5.25		
	250	100	4.41	4.41	38.7	79.1
		125	5.52	5.52	53.8	106
		150	6.66	6.66		
Id Off Current per Area ($nA/ \mu m^2$)	500	100	1.13	1.13	0.655	3.78
		125	529	529	5160	9720
		150	1480	1480		
	250	100	1.4	1.4	0.811	4.68
		125	662	662	6450	12300
		150	1860	1860		
Id On/Off (A/A)	500	100	3110	3110	46300	16300
		125	8.28	8.28	8.17	8.5
		150	3.54	3.54		
	250	100	3160	3160	47800	16900
		125	8.33	8.33	8.23	8.59
		150	3.58	3.58		
Id On Current For a 0.1 mm^2	500	100	351.4	351.4	3028	6157
		125	437.8	437.8	4212	8264

Device (mA)		150	525	525		
	250	100	441	441	3871	7913
		125	552	552	5382	10600
		150	666	666		
Area Per Device	500	100	2.3296	2.3296	1.82	1.82
Unit Cell		125	2.47	2.47	1.82	1.82
(μm^2/Device)		150	2.6	2.6		
	250	100	1.8816	1.8816	1.47	1.47
		125	1.995	1.995	1.47	1.47
		150	2.1	2.1		
Peak	500	100	2.66	2.66	27.6	41.1
Transconductan		125	2.54	2.54	28.3	54
ce per Area		150	2.37	2.37		
($\mu A/V\ \mu m^2$)	250	100	3.42	3.42	38.2	76.9
		125	3.28	3.28	38.7	75.3
		150	3.05	3.05		
Peak Gm for a	500	100	266	266	2762	4107
0.1 mm^2 Device		125	254	254	2833	5399
(mA/V)		150	237	237		
	250	100	342	342	3816	7688
		125	328	328	3868	7533
		150	305	305		
Threshold	500	100	-0.7	-0.7	-0.7	-0.7
Voltage (10x		125	-1.2	-1.2	-1.2	-1.2
Less Current		150				
Method) (V)	250	100	-0.7	-0.7	-0.7	-0.7
		125	-1.2	-1.2	-1.2	-1.2

		150				
Threshold	500	100	-0.4	-0.4	-0.5	-0.5
Voltage (Set		125	-0.5	-1	-1.2	-1.2
Current		150	-1.2	-1.2		
Method) (V)	250	100	-0.4	-0.4	-0.5	-0.5
		125	-0.5	-1.1	-1.2	-1.2
		150	-1.2	-1.2		

Note that all of the values in Table 2 are for ideal MESFETs without LDD dopings, dopant redistribution, or gate tunneling. The only the values in Table 2 that could be very inaccurate when compared to an actual MESFET in a standard CMOS SOI process are values that were calculated using Ioff (also including the value of Ioff itself) as they may be affected by the incorrect values for the gate current obtained in the simulations and discussed in the previous section. This is because if tunneling was taken into account, the off value for the drain current will converge to the value gate leakage current and the gate leakage current value may be higher than the ideal off drain current values. This would raise the off drain current value to the off gate current with leakage. However, with all of this said and even with tunneling enabled, the largest value of gate current for the channel doping used in the simulations to obtain the results in Table 2 was approximately 10 pA which is far less than the lowest drain off current of any of the devices at 823 pA. Simulations were done to show that the tunneling gate current will not affect any of the values in Table 2 for these devices until the devices channel doping is made to be greater than 1×10^{18} cm^{-3}. It is at this doping where the gate leakage current will be equal to the lowest drain leakage current in Table 2. This shows that the assumption of no gate tunneling can be used to obtain accurate values for the parameters in Table 2 for the majority of MESFET device designs as a channel doping of 1×10^{18} cm^{-3} would make the depletion region of these MESFETs much smaller (about half of what it is for extracted dopings of the devices in Table 2) and therefore necessitate that the channel width be reduced to the 40nm range in order to obtain a device with a

threshold voltage that is equivalent to the threshold voltage of the devices in Table 2. This means that all of the values in Table 2 that were calculated using Ioff (also including the value of Ioff itself) should accurately resemble a measured MESFET so long as it did not receive an LDD doping or experience dopant redistribution. The rest of the values were extracted only from the simulated values for the gate voltage and the drain current and voltage and therefore should also be accurate when compared to the values that would be obtained from a measured MESFET. Also, note that there is no actual unit cell for these PD MESFETs but there was a specific area that the simulations were done with so that was deemed the unit cell. This does not affect any of the results that are normalized to area but it does affect the results that are normalized to a unit cell.

All of the values in Table 2 are presented for devices with the exact same doping. In other words, there is only one doping that was used for all of the devices in Table 2 and it was never changed. The only things that were changed were the physical dimensions of the MESFETs. This was done in order to show the effect of changes in the physical dimensions of the MESFET on their operation and characteristics. Lastly, all of the values in Table 2 for both types of FD MESFET are the same even though from the prior discussion it would appear that they should be different. This is because they are normalized to area and never to the unit cell. If they were to be normalized to the unit cell then they would be different; however, doing so would not be beneficial for use in comparing the devices as they are not likely to ever be made with a small number of channels. Although it was previously discussed that JCFD and SCFD MESFETs' geometries converge, it was not stated which unit cell simulation would provide more accurate results for a wide FD MESFET device. When normalized to area, the current of a wide SCFD MESFET converges towards the current of a wide JCFD MESFET which means the simulations of the JCFD MESFET are more accurate for use in representing a wide FD MESFET device.

The results in Table 2 clearly show the superiority of the PD MESFET's current drive capability over that of the FD MESFET. This is why PD MESFETs will be focused on in the final portion of this thesis.

4.4 PD MESFET DEVICE LATTICE LAYOUT OPTIMIZATION

The layout of a PD MESFET is very simple in nature. The gate of the PD MESFET continuously covers a portion of all regions of the active silicon area in between the drain and source contacts. The way that modern high current PD MESFETs are laid out can be seen in Figure 54. The MESFET in Figure 54 demonstrates how the layout of modern multi-finger MESFETs is done. Multi-fingered MESFETs are laid out the same exact way that modern multi-finger MOSFETs are laid out in terms on layout geometry. Although this is almost universally the primary method of laying out multi-finger devices, with the exception of specialty devices such as annular transistors, it is not necessary the most efficient or advantageous. Using the previously stated concept that the gate of a PD MESFET must cover all of the regions of active silicon in between the source and drain contacts, some geometric simplifications and optimizations were done to the layout of a PD MESFET to achieve a device with a higher current per area than could be achieved in a device laid out using the standard co-linear multi-finger method. These geometric optimizations and simplifications resulted in the creation of the PD lattice MESFET.

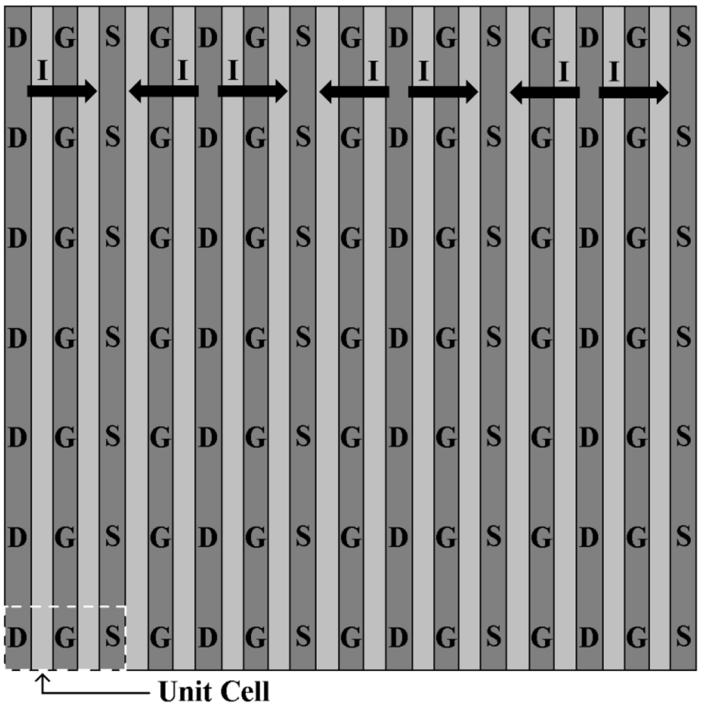

Figure 54: Standard Layout of a 7 Finger Wide PD MESFET

4.5 DEVICE CONCEPTUALIZATION 1

A concept drawing of a PD lattice (PDL) MESFET of comparable size to the standard multi-finger PD (MFPD) MESFET in Figure 54 can be seen in Figure 55. It can be seen from Figure 54 that the current that flows through the device (under standard operational polarity) will enter at each drain contact, flow under the gates that separate those drain contacts from the nearest source contacts, and exit the device through the source contacts. In the MFPD MESFET, the flow of current from the drain to the source is limited/forced to be in a single plane perpendicular to the drain and source contact rows. When a wide MESFET is laid out in this fashion, the current will flow in a straight line between the drain and source contacts since there is inconsequential variation in the potential in the device when traveling parallel along one of the devices gate fingers as seen in Figure 56. This can be seen from a simulation of the potentials and conduction current in a MFPD MESFET in Figure 57 and Figure 58 respectively. This limitation of the current to be mono-dimensional is the first part of what is limiting the current in MFPD MESFETs. The second part of what is limiting the current in a MFPD MESFET is the gate width to device area ratio. For any MESFET device with a given set of parameters, though the current increase to gate width increase may not be one to one, if properly done the drain to source current will increase as the width of the MESFET device increases. Therefore, since the MFPD MESFET does not have the maximum amount of gate width per area that a PD MESFET can have, it cannot not have the maximum amount of current per area that a MESFET can have.

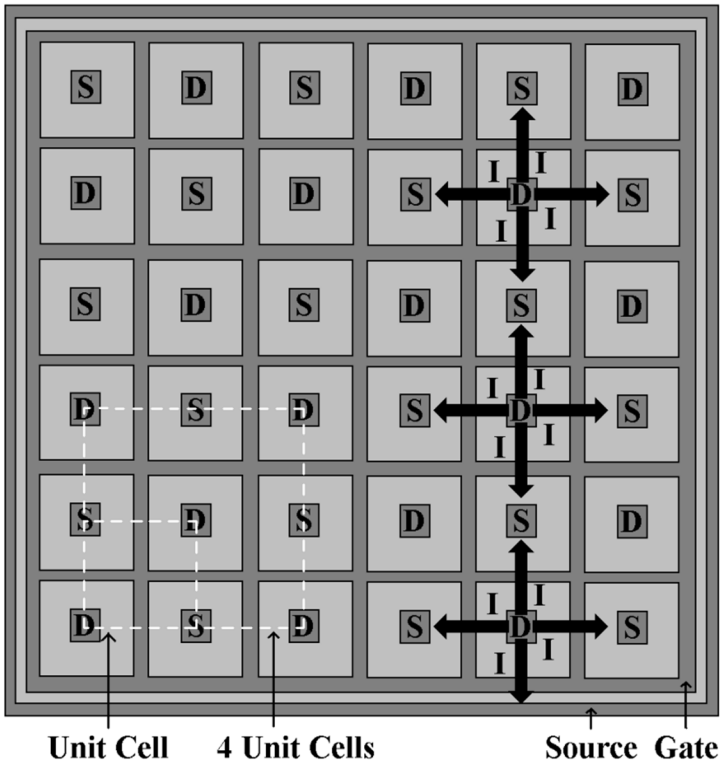

Figure 55: Layout of a 7 Finger Wide PDL MESFET

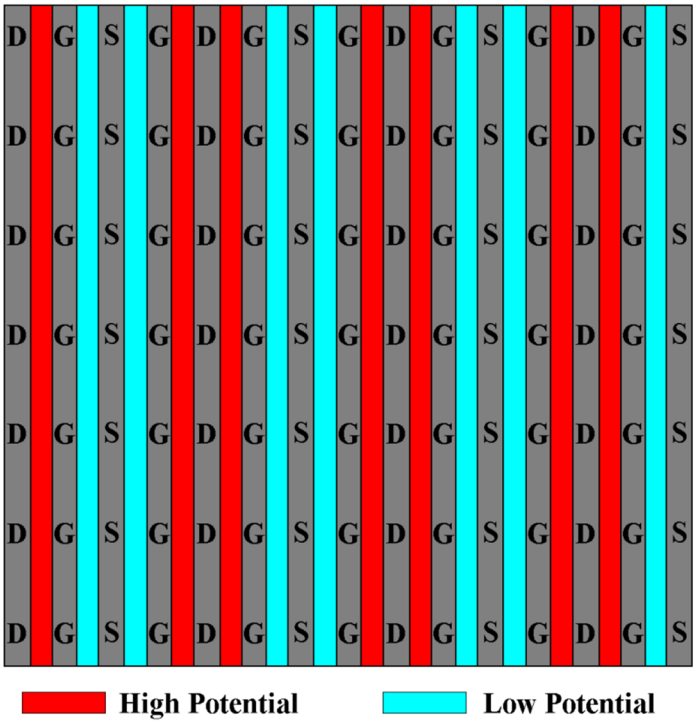

Figure 56: Layout of a 7 Finger Wide MFPD MESFET With Potential Zones

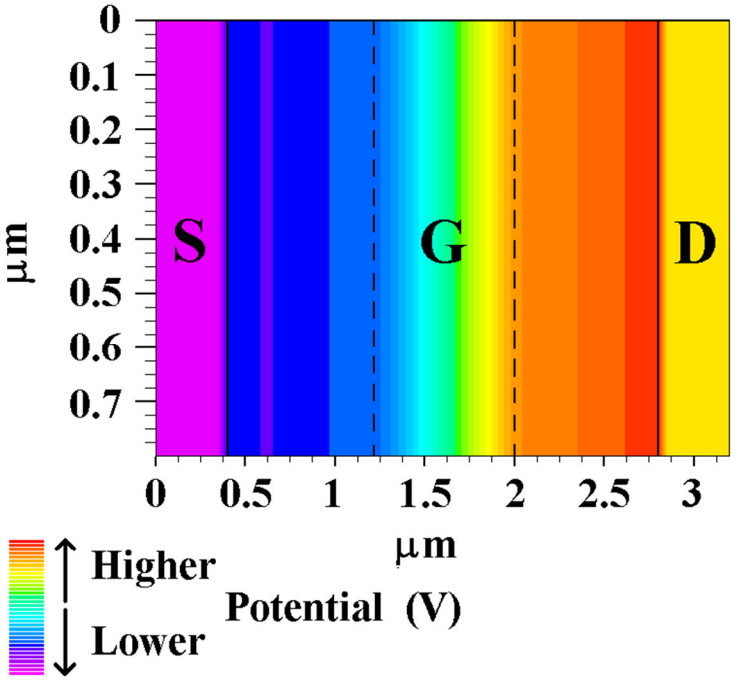

Figure 57: Potential Variation in a MFPD MESFET Unit Cell

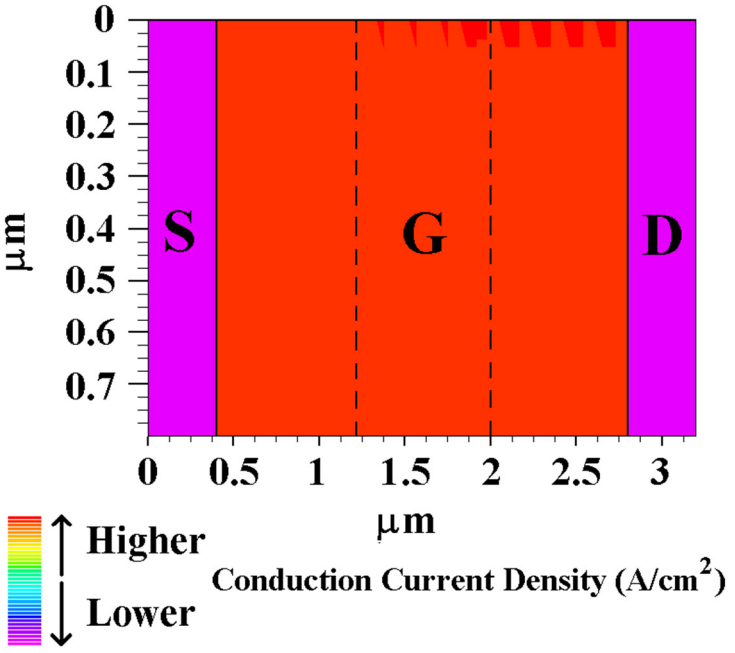

Figure 58: Conduction Current Density in a MFPD MESFET Unit Cell

The conceptual drawings and device simulation figures for the MESFETs in this thesis show the source, drain, and gate regions as continuous contacts because, due to the low resistance of the source/drain diffusions and the low resistance of the gate silicide, they effectively are. However, though it may be assumed that they are continuous for simulation purposes, the layout of MESFETs that are to be fabricated is confined/limited by the sizing and spacing of the contacts that connect the source, drain, and gate to the first metal level. The BEOL lithography of a process in which a MESFET is being integrated into is what will determine the minimum L_{ad}, L_{as}, L_{cw}, gate width (W_g), and L_g of a MESFET device made in that process. In order to design a device that will give experimental results similar to simulated results, the BOEL metal spacing rules of a process must be followed when conceptualizing or optimizing a device.

Unlike the MFPD MESFET, the PDL MESFET was designed such that it does not possess the same traits that are limiting the current in a MFPD MESFET. The current flow from drain to source is not mono-dimensional but it is bi-dimensional. Also, the gate width per area that was *able to be physically realized in the majority of foundries* was maximized. Other more experimental gate geometries could be more advantageous but are not as commonly producible.
The bi-dimensional current flow can be visualized in Figure 55. The advantage of the bi-dimensional current flow can also be thought of a reduction of resistance from the drain to the source through the addition of two resistors in parallel with the drain to source model of the MFPD MESFET since a wider region of silicon in between each drain and source contact lowers the resistance from drain to source. The potential zones in an ideal PDL MESFET device can be seen in Figure 59.

It can be seen from a comparison of Figure 54 to Figure 55 that unlike in the MFPD MESFET, the currents and potentials in the PDL MESFET will be highly non-uniform. Also, as the PDL MESFET does not end abruptly like the MFPD MESFET and must be enclosed in a very specific way. This means that electrical characteristics and physical properties of the PDL MESFET will not scale one to one with an increase in the size of the device. This is an advantage and a disadvantage of the PDL MESFET. This is disadvantageous because there are only discrete sizes that the PDL MESFET can be made to be as it does not have the ability to increase the gate

width while maintaining a constant number of fingers like in the MFPD MESFET but it is only able to be widened by increasing the number of fingers that the PDL device has. This is advantageous since the current per area in the outermost part of the PDL MESFET structure, the part of the structure that cannot be fit into the unit cell, is less than that of the current per area in an equivalent MFPD MESFET. Therefore, as the number of fingers of a PDL MESFET increases, the ratio of current loss in the outermost part of the device to the ratio of current gained in the device unit cells decreases and becomes small.

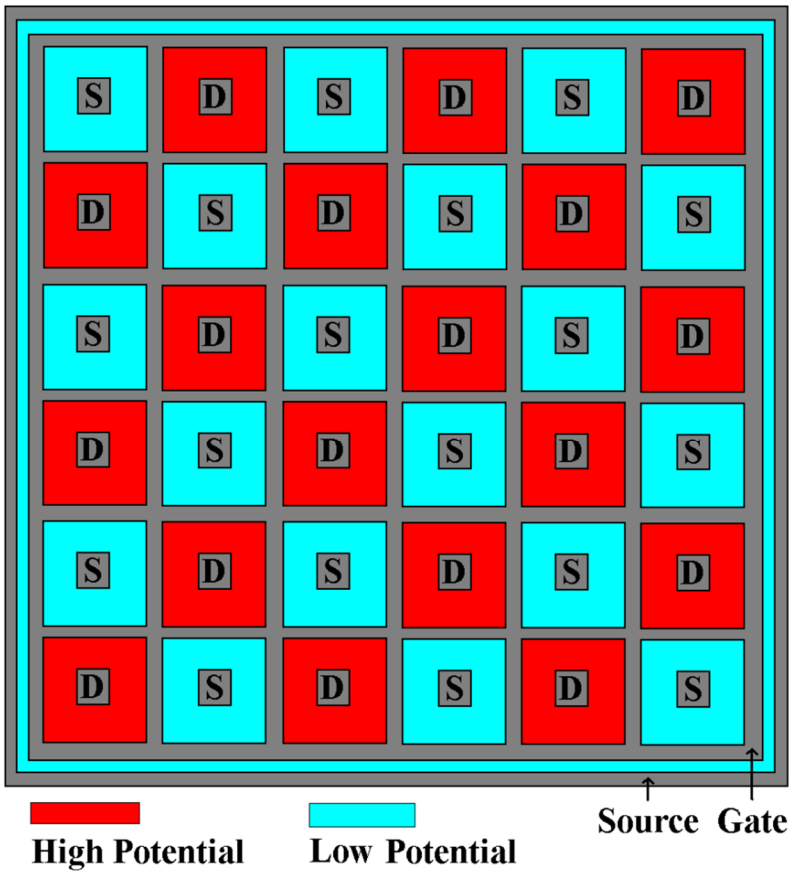

Figure 59: Layout of a 7 Finger Wide PDL MESFET With Potential Zones

4.6 DEVICE PHYSICS 1

Since the dimensions used in the proof of the concept of the PDL MESFET were for an older technology, a simulation of an entire PDL MESFET was not possible nor the most intelligent option. In order to make the simulations fast while remaining accurate a large section

of the PDL MESFET was simulated in order to extract a unit cell. The definition of a unit cell is the smallest piece of given system that can be repeated without change to build that system. Although, this definition produces a small unit cell that is able to be simulated for the MFPD MESFET, due to the non-uniform shape of the PDL MESEFT it produces a unit cell that is one quarter of the PDL MESFET device and will depend on the number of fingers that the device that the unit cell will be made to represent will have. So the standard method for unit cell extraction does not result in an acceptable or effective unit cell. Therefor an alternative unit cell must be extracted. This is why a large chunk of the PDL MESFET was simulated as seen in Figure 60. The repetition in the conduction current (with a gate silhouette) within this piece of a PDL MESFET can be seen in Figure 61. This repetition was what was used to determine the primary unit cell for the PDL MESEFT. Though the unit cell cannot be repeated to make the entire device, it can be repeated to represent the majority of the device and as the number of fingers in the device increase, the unit cell will more accurately be able to represent the PDL MESFET. Although there may be smaller scale repetition in the area deemed to be the unit cell, the chosen unit cell is the smallest piece of the system *that is able to be simulated* that can be used to build the majority of the system. Though the unit cell does not represent the outermost portion of the device, the equations that are used later on to determine the total current of the PDL MESFETs will take the outermost portion of the device into account.

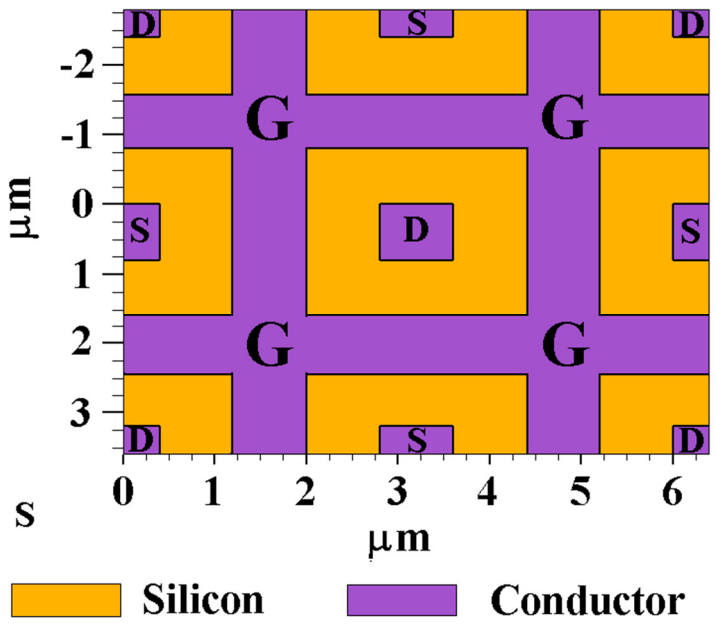

Figure 60: Section of a 7 Finger Wide PDL MESFET that was Simulated in Order to Extract a Unit Cell

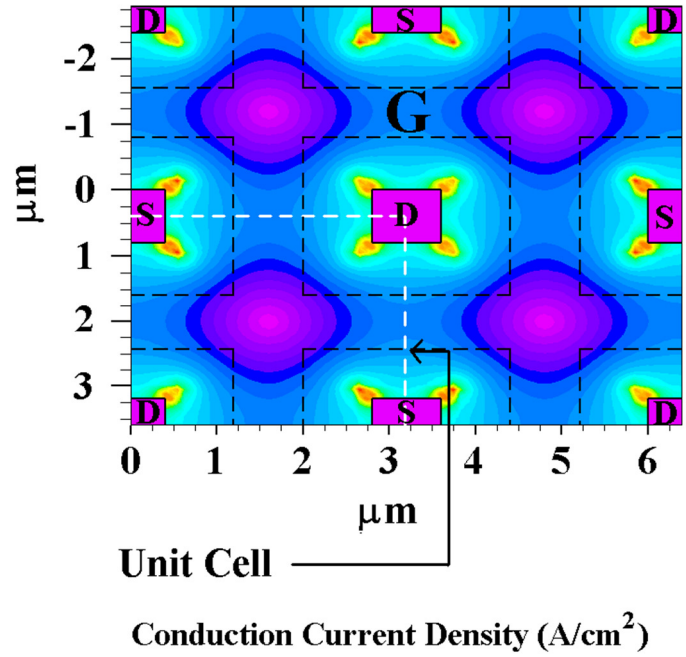

Figure 61: Section of a 7 Finger Wide PDL MESFET Showing Repetition in the Form of a Unit Cell

As it can be seen, two dimensional simulations were used to extract and verify the results of the PD MESFETs. Though a gate cannot be placed in between the drain and source regions in two dimensional simulations, the effect of the gate on the region of the device where it would be in reality can/must be incorporated into the simulations. In this thesis the effect of the gate on the drain to source characteristics was implemented through the modulation of the dopant concentration in the gate region of the PD MESFET devices. Though this does not allow the gate current to be calculated and solved for, it avoids the problems that three dimensional simulations suffer from and allow the devices to be simulated in a quick and effective manner.

4.7 DEVICE CONCEPTUALIZING 2

For the initial derivation of the design equations to see if the PDL MESFET is actually advantageous when compared to the MFPD MESFET, the geometry of the devices are simplified. A more advanced derivation will be provided later in this chapter for use in designing devices with different characteristics but for now the devices dimensions are normalized to the size of a contact. The reason for this is as was previously stated that the BEOL lithography will control the dimensions of a MESFET.

The concept of the "square" must be introduced before proceeding. Just like the geometrical definition, in this thesis a square will refer to a unit of space that has a length equal to its width. The square is used in this derivation not only to calculate the space that a device will take up but also the current that a device can handle. Defining the PD MESFET devices in terms of squares makes the calculation of both of these values much simpler than not doing so and comes at a minimal cost. Using squares to derive the design equations is not inaccurate or limiting in any way but one. The only negative effect of designing a MESFET in terms of squares is that the L_{ad} and L_{as} values cannot be varied. Also, designing a MESFET in terms of squares may prevent the MESFET from being a realistic or desirable device.

The unit cells for the MFPD and PDL MESFETs can be seen in Figure 62 and Figure 63 respectively. The unit cells with their square values for the MFPD and PDL MESFETs can be seen in Figure 64 and Figure 65 respectively.

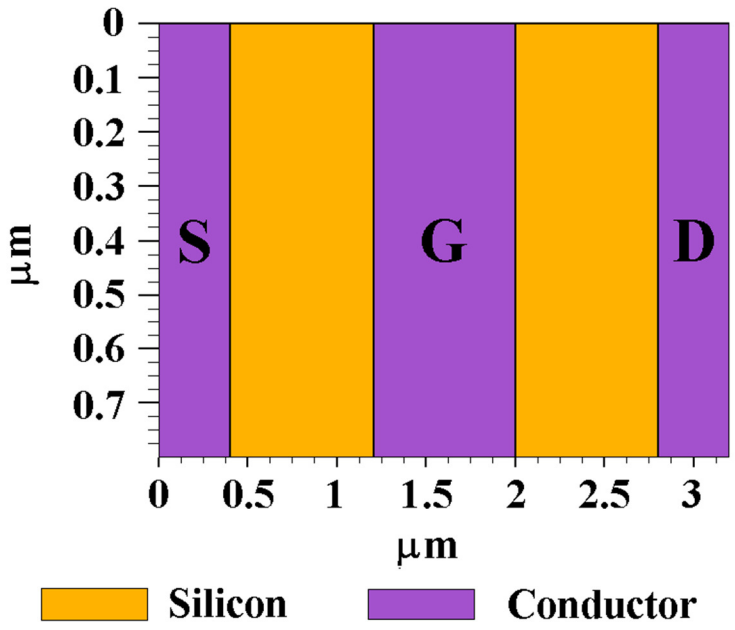

Figure 62: Unit Cell of a MFPD MESFET Showing Terminal Names

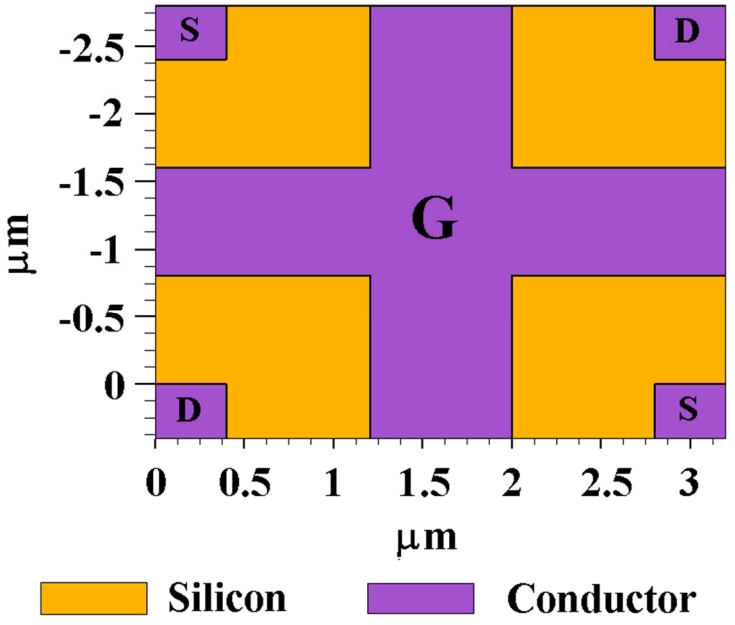

Figure 63: Unit Cell of a PDL MESFET Showing Terminal Names

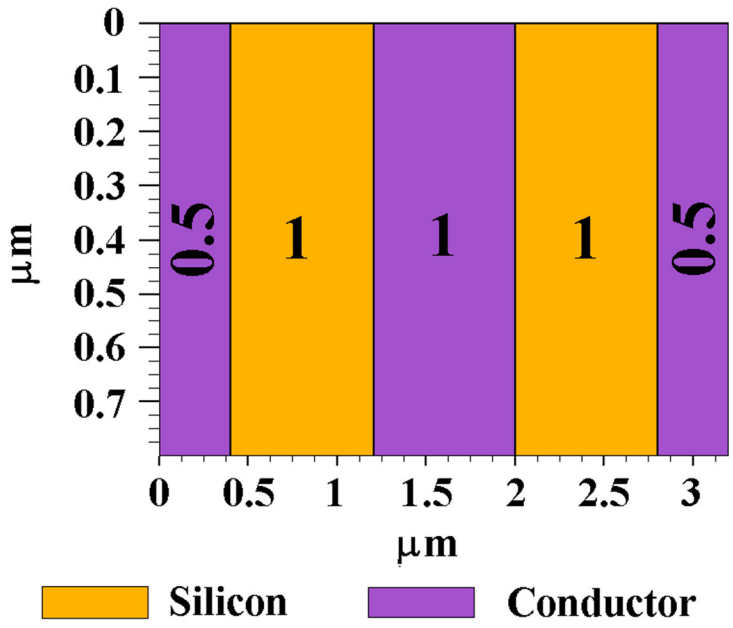

Figure 64: Unit Cell of a MFPD MESFET Showing Square Values

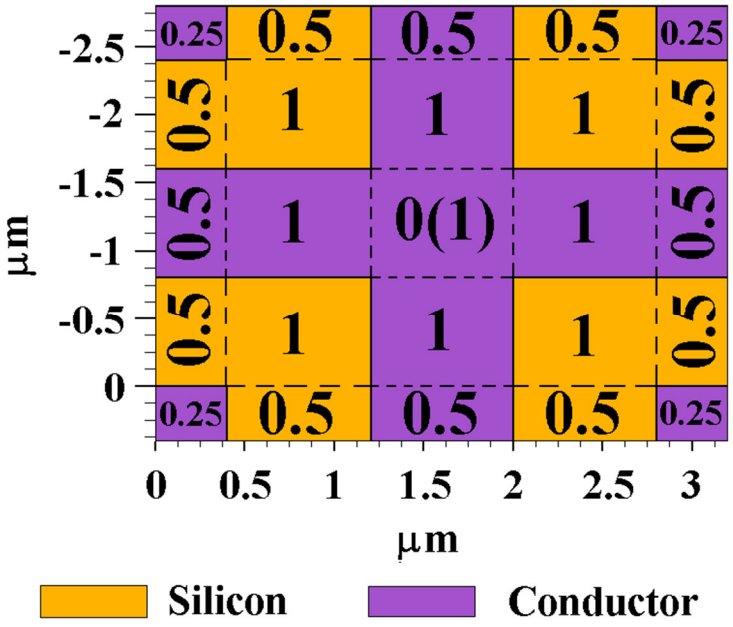

Figure 65: Unit Cell of a PDL MESFET Showing Square Values

As seen in Figure 64 and Figure 65, the value in each region is the value of the square that that region consists of. The unit cells contain some half integer values for squares because the

size of the square should be equal to the size of a contact in the process that these PD MESFETs are being designed for and the unit cells generally contain one half or one quarter of a contact. From an inspection of Figure 64 and Figure 65 it can be seen that the PDL MESFET unit cell is the same size as four MFPD MESFET unit cells. So although there is one gate square, a square of gate the is in between a drain and source region, in a MFPD MESFET unit cell each PDL MESFET unit cell will contain a total of six gate squares. Although there is a seventh gate square that can be seen in Figure 65, it is a gate square that is directly in between two drains and therefore is not considered to be a part of the drain to source conduction so it is only counted toward the area of the device and not the conduction. Counting the center gate square in the PDL MESFET unit cell toward the drain to source conduction will make a noticeable difference in the result of the design equations for small PDL MESFETs and less of a difference the larger a PDL MESFET gets as there is only minimal conduction under the seventh gate square. Although it seems that if the current per unit cell was normalized to seven gate squares and not six gate squares that the current for the device and the current per area would decrease. This is not the case because the total number of gate squares for a PDL MESFET would increase as well so in the end the increase in one value will almost completely cancel out with the decrease in the other value and this will be shown. It is just discussed here so that the reader can follow the derivation and for an understanding of the potentials and conduction within the unit cell.

The final thing must be taken into consideration before deriving the design equations. The bottom left corner of the PDL MESFET can be seen in Figure 66. The values for the formats as defined in the bottom of figure are as follows: F1 square value – source gate square value / drain gate square value; F2 square value – gate square value; F3 square value. Two important things must be taken into account during the derivation of the design equations and the design of the PDL MESFET device. The first has to do with the derivation of the design equations. As seen in Figure 66, around the edge (not just the corner) of the device there will inescapably be points where there is no conduction between the outermost contacts and the enclosing contact ring. These points must be taken into account when deriving the number of gate squares that a device has as the gate squares between two sources or two drains cannot count toward the total number of

gate squares that a device has. The second has to do with maximizing the current in the device. The contact that surrounds and encloses the entire device must be the opposite type as the contact in the bottom left corner of the device in order to get the maximum current per area for the device. This means that if the contact in the bottom left corner of the device is a drain contact then the contact that encloses the entire device must be a source contact and vice versa. It was derived to show that doing this will minimize the number of points around the device where there is no conduction between an outermost contact and the enclosing contact ring thereby maximizing the current per area of the device. Lastly, although it is not necessary as the device can be widened in a non-square fashion in order to obtain more degrees of precision in the modification of the devices width, the PDL MESFET must be expanded from the top right corner, adding additional portions of the device to the top right corner of the device, and always kept as a square, having the same number of fingers in each direction, in order to keep the current per area maximized.

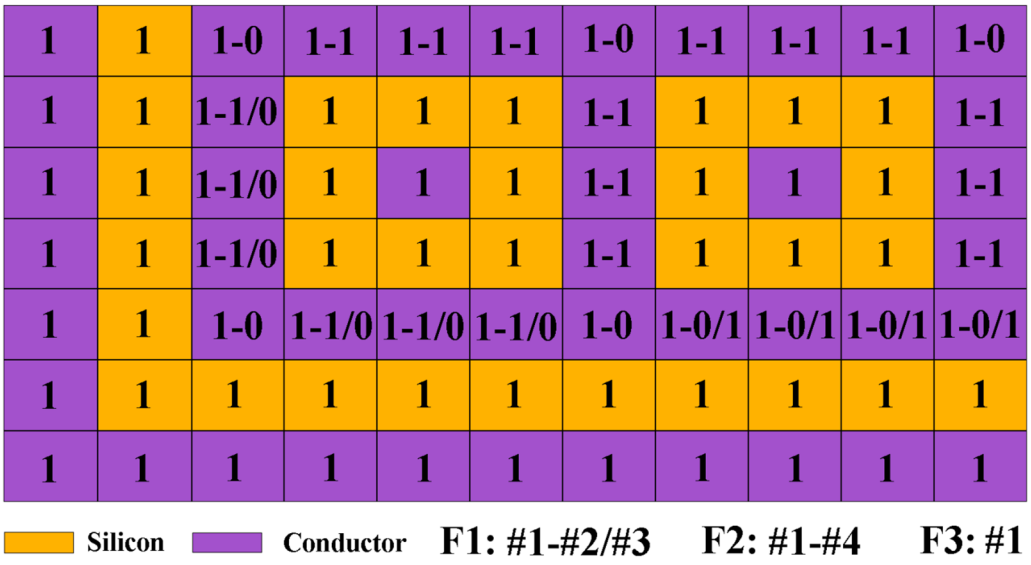

Figure 66: Corner of a PDL MESFET Showing Square and Conduction Values

4.8 DESIGN EQUATIONS 1

Below is the initial set of design equations that were derived for the PDL and MFPD MESFETs assuming a constant square size as shown in previous figures. The design equations for

the MFPD MESFET can be seen in Equation 4.1 through Equation 4.3 and the design equations for the PDL MESFET can be seen in Equation 4.4 through Equation 4.6.

$$G = N_f \times N_{gst} \tag{4.1}$$

$$T_{squares} = N_{gst} \times \left(5 + \left(4 \times \left(N_f - 1\right)\right)\right) \tag{4.2}$$

$$A_T = T_{squares} \times A_{per\ square} \tag{4.3}$$

$$G = 3 \times \left[\left(2 \times N_f \times \left(N_f - 1\right)\right) - 4 \times floor\left(\frac{N_f - 1}{2}\right)\right] \tag{4.4}$$

$$T_{squares} = \left(5 + \left(4 \times \left(N_f - 1\right)\right)\right)^2 \tag{4.5}$$

$$A_T = T_{squares} \times A_{per\ square} \tag{4.6}$$

where

G = The total number of gate squares in a device

N_f = The number of gate fingers

N_{gst} = The total number of gate squares a device is in height

$T_{squares}$ = The total number of squares in a device

$A_{per\ square}$ = The area per square

The floor function in Equation 4.4 takes the results of the calculations inside of it, rounds down to the highest integer value, and returns that value. If the result of the calculations inside of the floor function are already and integer then it just returns that integer. These design equations are complete in the sense that they do not neglect or make any approximations to the total number of gate squares or the total area of the device.

These design equations can be compared to see what the theoretical gain in current per unit area is. When compared they give the results seen in Table 3.

Table 3: Comparison of the Design Equations for a PDL MESFET and a MFPD MESFET

Comparison of the Design Equations for a PDL MESFET and a MFPD MESFET				
PD MESFET Device Type	MFPD and PDL	MFPD	PDL	-
	Device Area (mm^2)	Total Number of Gate Squares	Total Number of Gate Squares	Percent Increase in Number of Gate Squares per Area
	1.6×10^{-5}	5	-	-
	1.08×10^{-4}	39	24	-38.462
	8.76×10^{-4}	333	384	15.315
	7.6×10^{-3}	2943	4056	37.819
	6.76×10^{-2}	26325	38400	45.869
	6.06×10^{-1}	236439	351384	48.615
	5.45	2126493	3179904	49.537
	48.98	19134063	28671576	49.846
	440.8	172193445	258201600	49.949
	3967	1549701639	2324286744	49.983

This comparison is done assuming that the amount of current conduction under a single gate square is the same in either PD MESFET device. As previously discussed, it can be seen that at smaller device sizes there is actually a theoretical decrease in the conductivity of the device. Also, unreasonable device sizes are presented in Table 3 because they show the asymptotic behavior of the percent increase in the number of gate squares per area going to 50 %.

What the device design equations allow a designer to do is to take simulation results from the unit cells of the PDL and MFPD MESFETs and extrapolate those results to show some of the electrical characteristics of a complete device. So, before the electrical characteristics of a complete device can be shown, simulations of the unit cells of the PD MESFETs must be done.

4.9 DEVICE PHYSICS 2

The dopant concentration in a MFPD and PDL MESFET unit cell can be seen in Figure 67 and Figure 68 respectively. The doping that these devices will receive depends on the technology that they are being made in so the doping in the figures in this thesis are generalized so as not to be too specific while still showing the relative magnitude of the dopant concentrations. The conduction current density and potential energy distribution for the devices in Figure 67 and Figure 68 can be seen in Figure 69 through Figure 72 respectively.

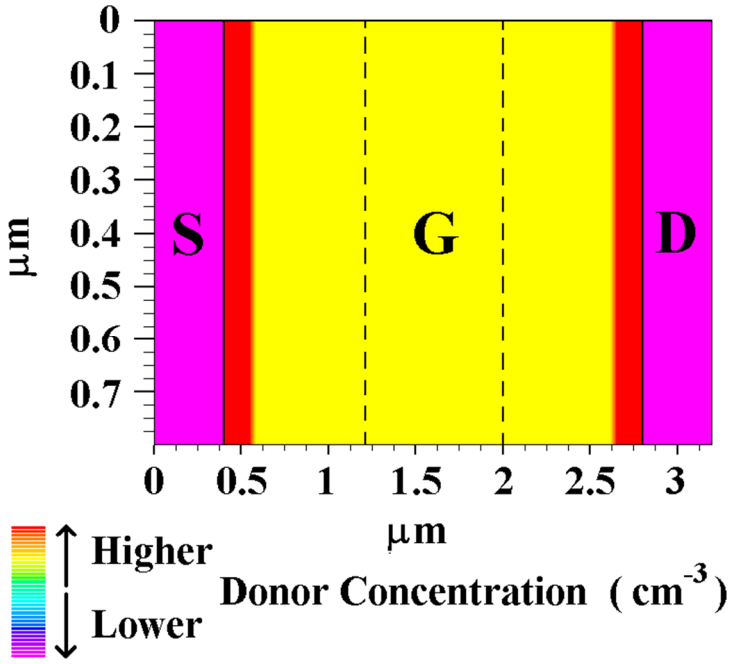

Figure 67: Unit Cell of a MFPD MESFET Showing Dopant Concentration Values

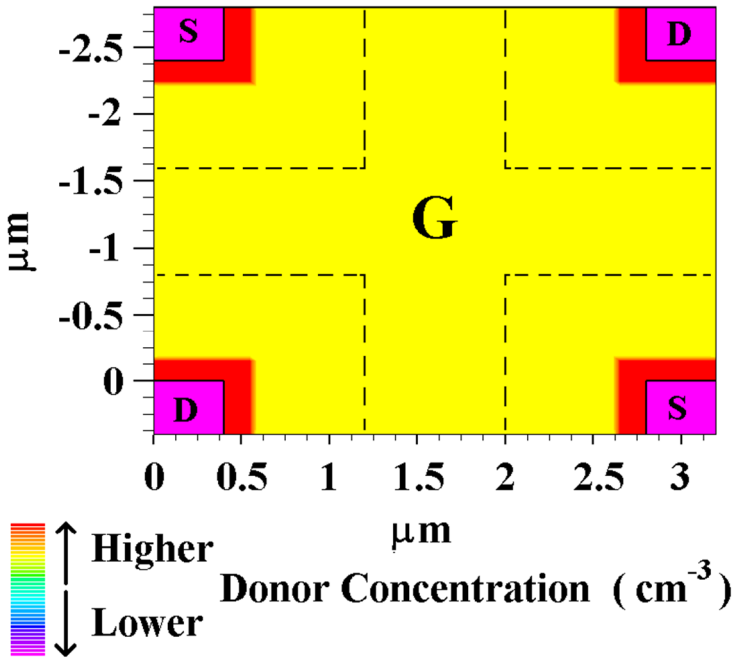

Figure 68: Unit Cell of a PDL MESFET Showing Dopant Concentration Values

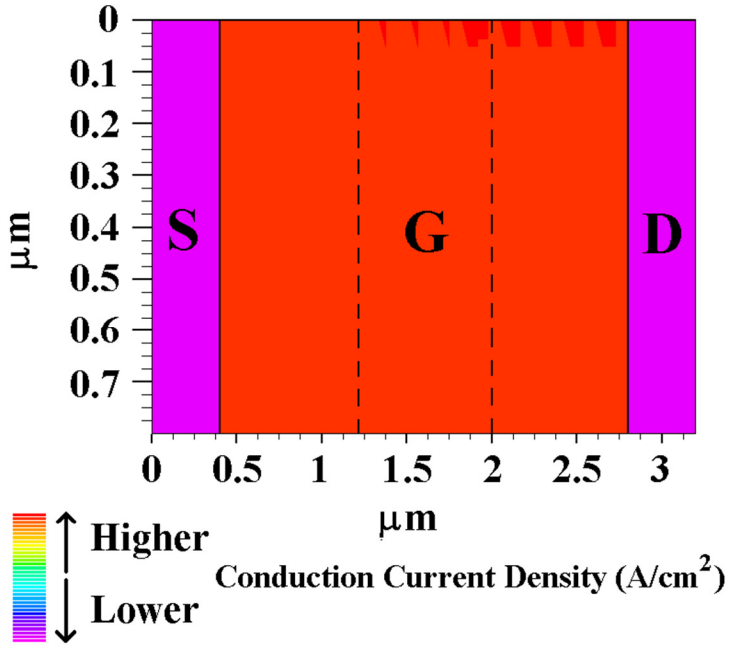

Figure 69: Unit Cell of a MFPD MESFET Showing Conduction Current Density

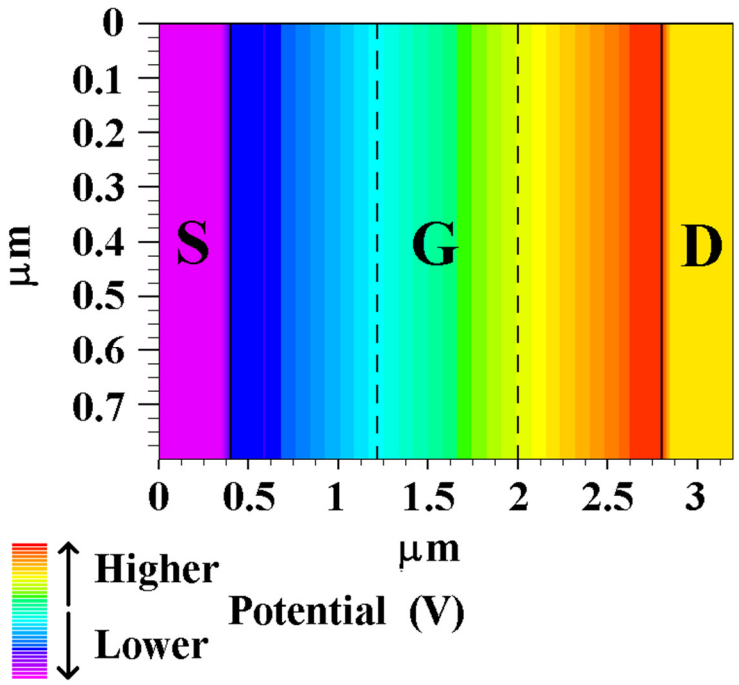

Figure 70: Unit Cell of a MFPD MESFET Showing Potential Energy Distribution

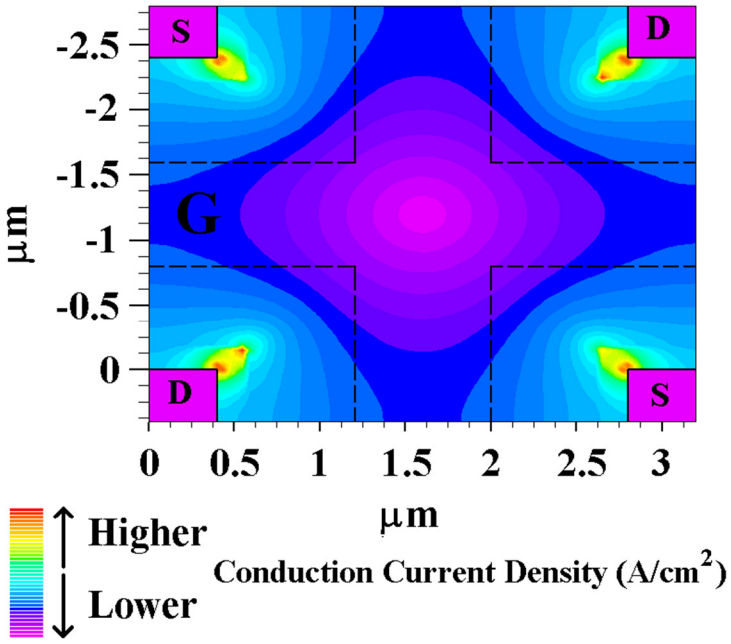

Figure 71: Unit Cell of a PDL MESFET Showing Conduction Current Density

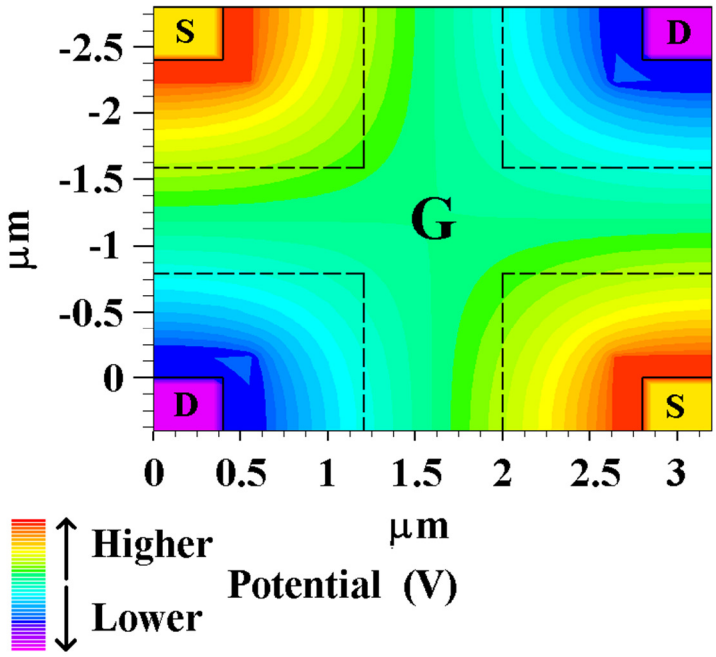

Figure 72: Unit Cell of a PDL MESFET Showing Potential Energy Distribution

These simulations were done on the PD MESFET unit cells in order to obtain the current per unit cell values and extrapolate the current per gate square values. Doing the simulations on the unit cells as they currently are shown leads to a surprising result. When the results of the simulations are combined with the design equations to find the percent increase in total device current, the results are vastly lower than the theoretical results of ~ 50%. The values for the current per device asymptote to a 14 % increase, this is 36% lower than the theoretical asymptote for the percent increase in number of gate squares. The results of the simulations can be investigated to show the cause of this gross disagreement in the percent increase in current.

The devices that were initially simulated to produce the results that were compared to the theoretical calculations were lacking a key feature of the PD MESFET device: the gate. As previously discussed, the gate of the PD MESFET could not be added to the simulations because they were done in a two dimensional simulator. After reviewing the results obtained from the simulations that showed such a poor match to the theoretical calculations, it was found that the potential in the device was what was causing the current to be so much lower than was expected.

There is a disadvantage to having the potential zones in a PD MESFET arranged in the manner that they are in the PDL MESFET (Figure 59). In a MFPD MESFET the potential zones are laid out in a linear fashion where the zones of high potential are separated from other zones of high potential by zones of low potential. When the gate of the PDL MESFET device is removed, it can be seen that unlike in a MFPD MESFET, the zones of high potential are not separated from other zones of high potential by zones of low potential. This causes the region of silicon in between two zones of high potential to sit at some intermediate potential as seen in Figure 72. This causes the potential drop from a drain contact to some portion of the silicon in between that drain contact and another drain contact to be smaller than desired/assumed thereby lowering the electric field and reducing the conduction current density towards this intermediate region. Also, it causes the potential along the gate squares that are not directly in between a drain and source contact to have a lower and more poorly controlled potential than is necessary to get the proper/necessary amount of conduction. It is because of this that the PDL MESFET layout modification will not work properly to enhance the current in a MOSFET and that the theoretical calculations are so different from the simulations. The theoretical calculations require that the conduction under each gate square be equivalent in order to be accurate. So, the effect of the potential of one drain contact on the silicon in between that drain contact and another drain contact reduces the conduction of some of the gate squares in the PDL MESFET unit cell and therefore makes the theoretical model inaccurate and results in a lower total device current. However, this inaccuracy in the theoretical model is brought about by an inaccuracy in the device simulations: the lack of a gate. Although the gates cannot be added to the two dimensional simulations in order to improve the accuracy of the theoretical calculation, the effect of the gates presence in the device can and must in order to achieve more accurate and realistic results.

In a PD MESFET, the gate of the device depletes the silicon that is underneath it in order to control the drain to source current. At various points in the operation of the device the amount of silicon that is depleted below the gate may range from virtually no silicon being depleted when the gate voltage is very positive to all of the silicon being depleted when the gate voltage is very negative. The most advantageous regions of operation to use a MESFET are: when the gate has

the same bias as the source contact; when the gate current goes to zero which should be when the gate has the same bias as the source contact but can sometimes be somewhere in the low positive gate potential region if there is a large potential bias on the drain of the device and the MESFET device has received the undesirable LDD dopings or experienced dopant redistribution; in the cut off region of operation. These regions are the most advantageous regions of operation for a MESFET because they take full advantage of the characteristics that a depletion mode device has to offer. Keeping this in mind, the effect of the gate on the silicon in the gate region of the device can be added to two dimensional simulations through the use of the formulas in Equation 4.7 through Equation 4.10.

$$\phi_{semi} = \chi_{si} + \frac{E_g}{2} - \frac{kT}{q}\ln\left(\frac{N_{ch}}{n_i}\right) \tag{4.7}$$

$$t_{depletion} = 1\times10^{7}\sqrt{\frac{2\,\varepsilon_{r\,si}\varepsilon_0 \times \left(\left(\phi_m - \phi_{semi}\right) - V_A + V_D F\right)}{q\,N_{ch}}} \tag{4.8}$$

$$R_{Gate\ Equivalent} = \frac{L}{N_{ch}\,W\left(t_{si} - t_{depletion}\right)q\,\mu_{si\,Nch}} \tag{4.9}$$

$$N_{Ch\ Equivalent} = \frac{L}{R_{Gate\ Equivalent}\,W\,t_{si}\,q\,\mu_{si\,Nch}} \tag{4.10}$$

where

χ_{si}= The affinity of silicon

E_g= The bandgap of silicon

n_i= The intrinsic carrier concentration of silicon in cm^{-3}

K= The temperature of the device in Kelvin

q= The fundamental electronic charge

eV= Electron Volts

k= Boltzmans constant in eV per Kelvin

N_{ch} = The doping concentration in the channel of the device in cm^{-3}

ϕ_{semi}= The work function of the semiconductor

ϕ_m = The work function of the metal gate

$\varepsilon_{r\ si}$= The relative permittivity of silicon

ε_0= The relative permittivity of silicon in farads per cm

V_A= The applied voltage at the gate of the MESFET in Volts

V_D= The applied voltage at the drain contact in Volts

F= An adjustment factor to incorporate the effect of the drain on the gate depletion

$t_{depletion}$= The thickness of the depleted silicon layer in cm

t_{si}= The thickness of the thin silicon film layer in cm

L= The length of the MESFET gate channel in cm

W= The width of the MESFET gate channel in cm

$\mu_{si\ Nch}$= The mobility of the carriers in the channel region of the device. It is doping dependant.

$R_{Gate\ Equivalent}$= The resistance of the undepleted silicon region under the MESFET gate contact

$N_{Ch\ Equivalent}$= The equivalent doping that can be placed in the channel region of the gate to simulate the effect of the gate on the silicon in the device.

Using the above equations, the effect of the gate on the resistance of the channel region of the PDL MESFET device can be simulated by re-doping the channel region of the two dimensional simulations so that they have a resistance equivalent to that of the resistance the channel would have in the presence of a gate contact with a given applied bias. The MFPD and PDL MESFET unit cells with modified gate-effect doping can be seen in Figure 73 and Figure 74 respectively. Also, the conduction current density and potential energy distribution of the MFPD and PDL MESFETs with the modified gate-effect doping can be seen in Figure 75 through Figure 78 respectively.

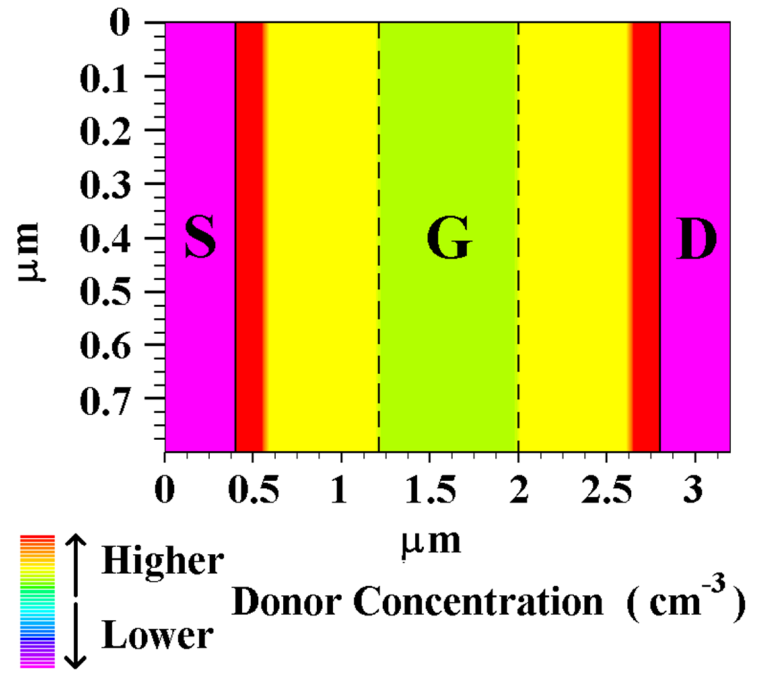

Figure 73: Unit Cell of a MFPD MESFET Showing Gate-Effect Dopant Concentration

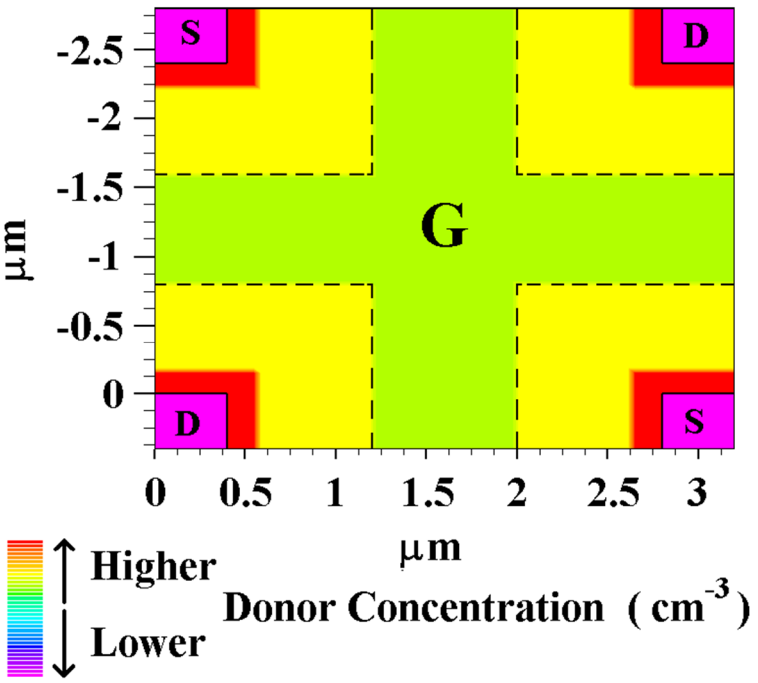

Figure 74: Unit Cell of a PDL MESFET Showing Gate-Effect Dopant Concentration

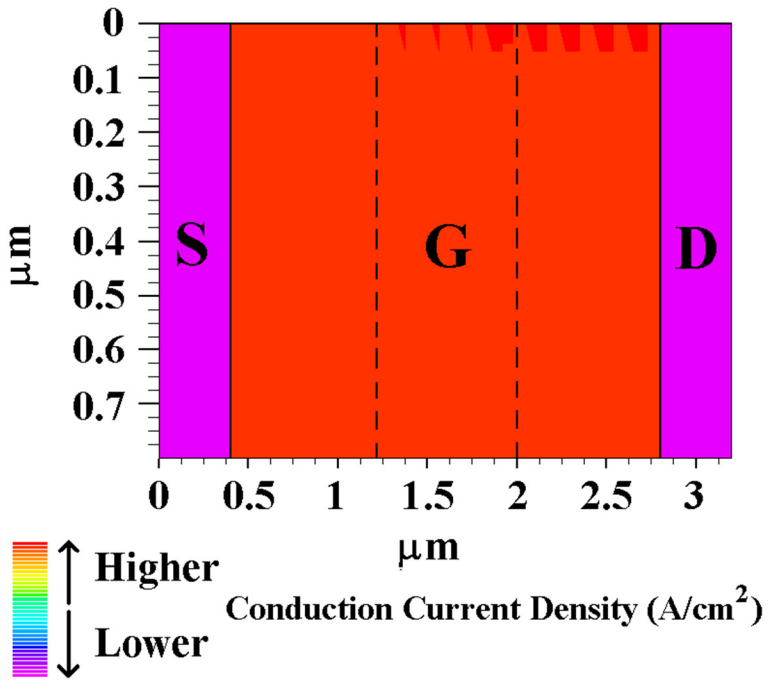

Figure 75: Unit Cell of a MFPD MESFET Showing Gate-Effect Conduction Current Density

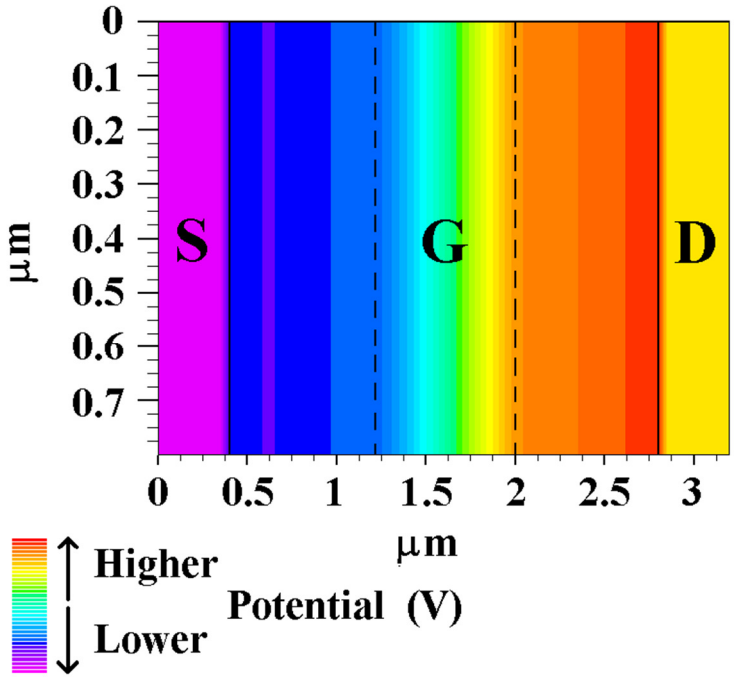

Figure 76: Unit Cell of a MFPD MESFET Showing Gate-Effect Potential Energy Distribution

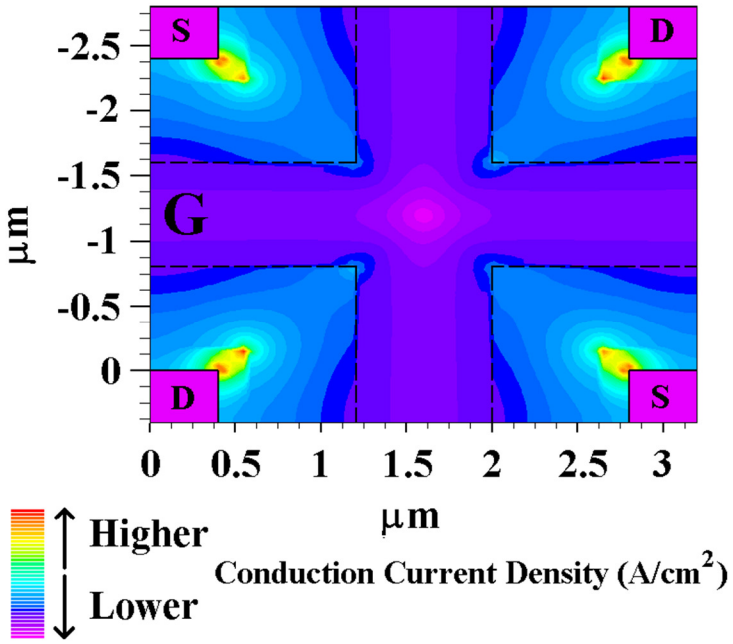

Figure 77: Unit Cell of a PDL MESFET Showing Gate-Effect Conduction Current Density

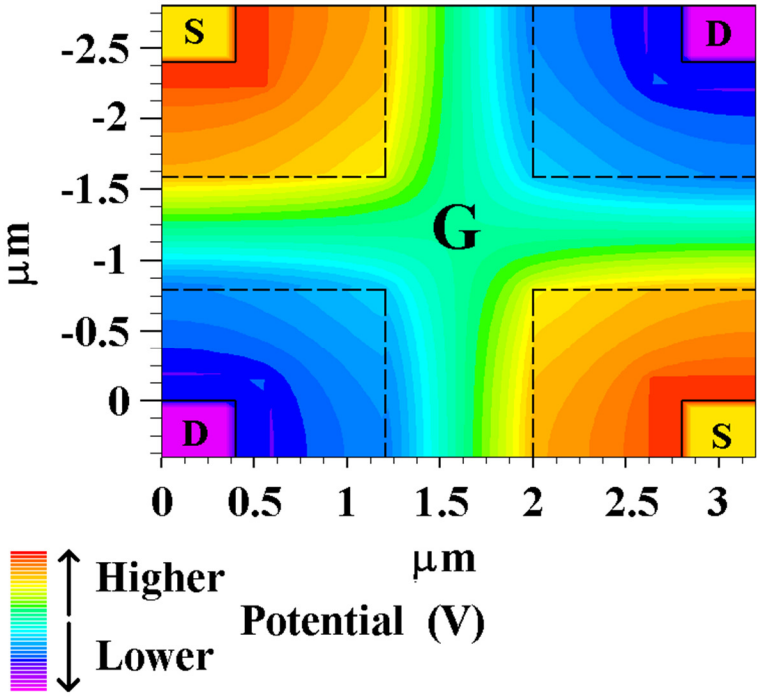

Figure 78: Unit Cell of a PDL MESFET Showing Gate-Effect Potential Energy Distribution

It can be seen from Figure 76 and Figure 78 that less of the potential energy in the device is dropped across the access length regions and the majority of the potential is now dropped across the length of the gate channel. In the PDL MESFET unit cell, this causes the potential distribution in the corners of the drain access regions to be higher than in device simulations without the gate-effect doping and in turn improves the conduction across the gate squares in the PDL unit cell that are not directly in between a drain and source contact because the potential on each side of the gate is more closely related to and controlled by the respective regions contact than previously. A comparison of Figure 71 and Figure 77 shows that the conduction current density has been expanded to be almost equal along the entire length of the gate in Figure 77 when the PDL unit cell has the modified gate-effect doping as compared to before where the conduction current density was much lower along the portions of the gate in Figure 71 that were not directly in between a drain and source contact.

The PDL and MFPD MESFET unit cells with the modified gate-effect doping can be re-simulated in order to get the current per unit cell characteristics and the total device current can be recalculated and compared.

4.10 RESULTS AND SUMMARY

The extrapolated calculation and simulation results of the PDL and MFPD MESFET with the gate-effect doping for enhanced accuracy can be seen in Table 4 through Table 7 and Figure 79 through Figure 82. The simulations were done for PDL and MFPD MESFET devices with: $CoSi_2$ and NiSi simulated gates, devices with two different designed threshold voltages, a drain voltage of two volts, and a gate voltage of zero volts.

Table 4: Electrical Characteristics Comparison and Summary of a PDL MESFET Device With $CoSi_2$ Gate and -0.5 Volt Threshold Voltage

Electrical Characteristics Comparison and Summary of a PDL MESFET Device With $CoSi_2$ Gate and -0.5 Volt Threshold Voltage				
PD MESFET Device Type Thin Silicon Film Thickness (nm)	MFPD and PDL Device Area (mm^2)	MFPD Total Device Current for a Device with Listed Area (A)	PDL Total Device Current for a Device with Listed Area (A)	- Percent Increase in Drain Current
50	2.82×10^{-4}	4.74×10^{-3}	4.69×10^{-3}	-1
	6.52×10^{-3}	1.14×10^{-1}	1.69×10^{-1}	48.2
	1.6×10^{-1}	2.82	4.51	59.51
	4	70.5	114	61.83
80	2.82×10^{-4}	3.11×10^{-3}	3.22×10^{-3}	3.47
	6.52×10^{-3}	7.47×10^{-2}	1.16×10^{-1}	54.91
	1.6×10^{-1}	1.85	3.09	66.72
	4	46.3	78.3	69.15
120	2.82×10^{-4}	2.24×10^{-3}	2.32×10^{-3}	3.73
	6.52×10^{-3}	5.38×10^{-2}	8.35×10^{-2}	55.29
	1.6×10^{-1}	1.33	2.23	67.14
	4	33.3	56.5	69.58
140	2.82×10^{-4}	2.01×10^{-3}	2.06×10^{-3}	2.92
	6.52×10^{-3}	4.82×10^{-2}	7.43×10^{-2}	54.07
	1.6×10^{-1}	1.2	1.98	65.83
	4	29.9	50.2	68.24

Table 5: Electrical Characteristics Comparison and Summary of a PDL MESFET Device With $CoSi_2$ Gate and -1 Volt Threshold Voltage

Electrical Characteristics Comparison and Summary of a PDL MESFET Device With $CoSi_2$ Gate and -1 Volt Threshold Voltage				
PD MESFET Device Type	MFPD and PDL	MFPD	PDL	-
Thin Silicon Film Thickness (nm)	Device Area (mm^2)	Total Device Current for a Device with Listed Area (A)	Total Device Current for a Device with Listed Area (A)	Percent Increase in Drain Current
50	2.82×10^{-4}	9.51×10^{-3}	9.09×10^{-3}	-4.47
	6.52×10^{-3}	2.29×10^{-1}	3.27×10^{-1}	43.01
	1.6×10^{-1}	5.67	8.73	53.93
	4	142	221	56.17
80	2.82×10^{-4}	6.36×10^{-3}	6.26×10^{-3}	-1.58
	6.52×10^{-3}	1.53×10^{-1}	2.25×10^{-1}	47.19
	1.6×10^{-1}	3.8	6.01	58.42
	4	94.7	152	60.72
120	2.82×10^{-4}	4.45×10^{-3}	4.54×10^{-3}	2.07
	6.52×10^{-3}	1.07×10^{-1}	1.64×10^{-1}	52.8
	1.6×10^{-1}	2.66	4.37	64.46
	4	66.3	111	66.85
140	2.82×10^{-4}	3.91×10^{-3}	4.02×10^{-3}	2.82
	6.52×10^{-3}	9.39×10^{-2}	1.45×10^{-1}	53.92
	1.6×10^{-1}	2.33	3.86	65.66
	4	58.1	97.7	68.08

Table 6: Electrical Characteristics Comparison and Summary of a PDL MESFET Device With NiSi Gate and -0.5 Volt Threshold Voltage

Electrical Characteristics Comparison and Summary of a PDL MESFET Device With NiSi Gate and -0.5 Volt Threshold Voltage				
PD MESFET Device Type	MFPD and PDL	MFPD	PDL	-
Thin Silicon Film Thickness (nm)	Device Area (mm^2)	Total Device Current for a Device with Listed Area (A)	Total Device Current for a Device with Listed Area (A)	Percent Increase in Drain Current
50	2.82×10^{-4}	4.6×10^{-3}	4.61×10^{-3}	-0.2
	6.52×10^{-3}	1.11×10^{-1}	1.66×10^{-1}	50
	1.6×10^{-1}	2.74	4.43	61.44
	4	68.5	112	63.79
80	2.82×10^{-4}	3.02×10^{-3}	3.15×10^{-3}	4.23
	6.52×10^{-3}	7.27×10^{-2}	1.13×10^{-1}	56.4
	1.6×10^{-1}	1.8	3.03	67.95
	4	45	76.7	70.39
120	2.82×10^{-4}	2.17×10^{-3}	2.27×10^{-3}	4.53
	6.52×10^{-3}	5.23×10^{-2}	8.18×10^{-2}	56.49
	1.6×10^{-1}	1.3	2.18	68.43
	4	32.4	55.3	70.88
140	2.82×10^{-4}	1.96×10^{-3}	2.05×10^{-3}	4.3
	6.52×10^{-3}	4.72×10^{-2}	7.37×10^{-2}	56.15
	1.6×10^{-1}	1.17	1.97	68.06
	4	29.2	49.8	70.51

Table 7: Electrical Characteristics Comparison and Summary of a PDL MESFET Device With NiSi Gate and -1 Volt Threshold Voltage

Electrical Characteristics Comparison and Summary of a PDL MESFET Device With NiSi Gate and -1 Volt Threshold Voltage				
PD MESFET Device Type	MFPD and PDL	MFPD	PDL	-
Thin Silicon Film Thickness (nm)	Device Area (mm^2)	Total Device Current for a Device with Listed Area (A)	Total Device Current for a Device with Listed Area (A)	Percent Increase in Drain Current
50	2.82×10^{-4}	9.23×10^{-3}	8.46×10^{-3}	-8.29
	6.52×10^{-3}	2.22×10^{-1}	3.05×10^{-1}	37.29
	1.6×10^{-1}	5.5	8.13	47.76
	4	137	206	49.91
80	2.82×10^{-4}	6.13×10^{-3}	6.11×10^{-3}	-0.33
	6.52×10^{-3}	1.47×10^{-1}	2.2×10^{-1}	49.21
	1.6×10^{-1}	3.66	5.87	60.6
	4	91.3	149	62.94
120	2.82×10^{-4}	4.28×10^{-3}	4.42×10^{-3}	3.08
	6.52×10^{-3}	1.03×10^{-1}	1.59×10^{-1}	54.32
	1.6×10^{-1}	2.56	4.24	66.09
	4	63.8	107	68.51
140	2.82×10^{-4}	3.76×10^{-3}	3.89×10^{-3}	3.43
	6.52×10^{-3}	9.04×10^{-2}	1.4×10^{-1}	54.84
	1.6×10^{-1}	2.24	3.74	66.66
	4	56	94.6	69.08

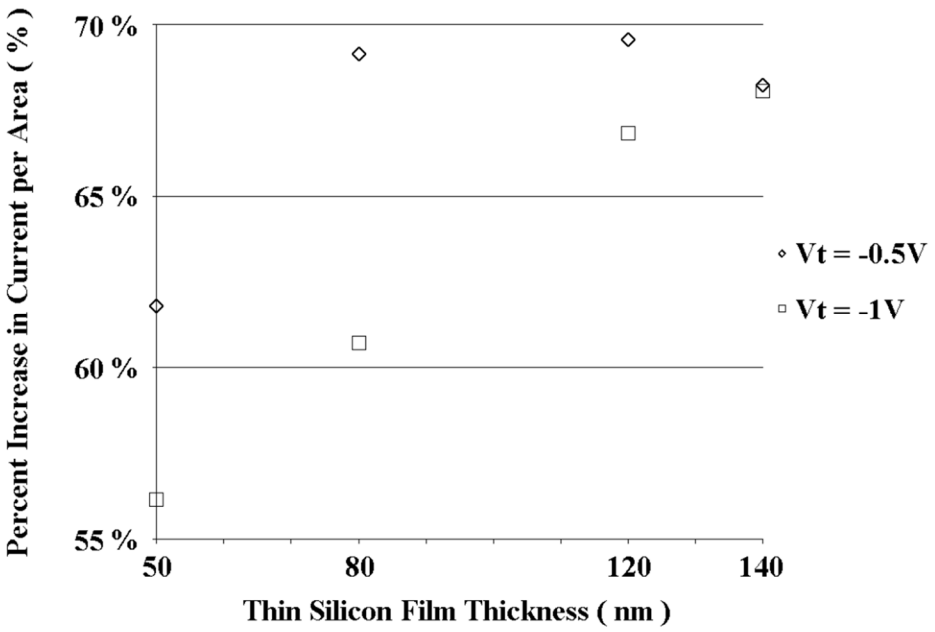

Figure 79: Percent Increase in the Current per Area from Using the PDL Layout Technique Instead of the MFPD Layout Technique for a MESFET with a $CoSi_2$ Gate and Four Different Thin Silicon Film Thicknesses

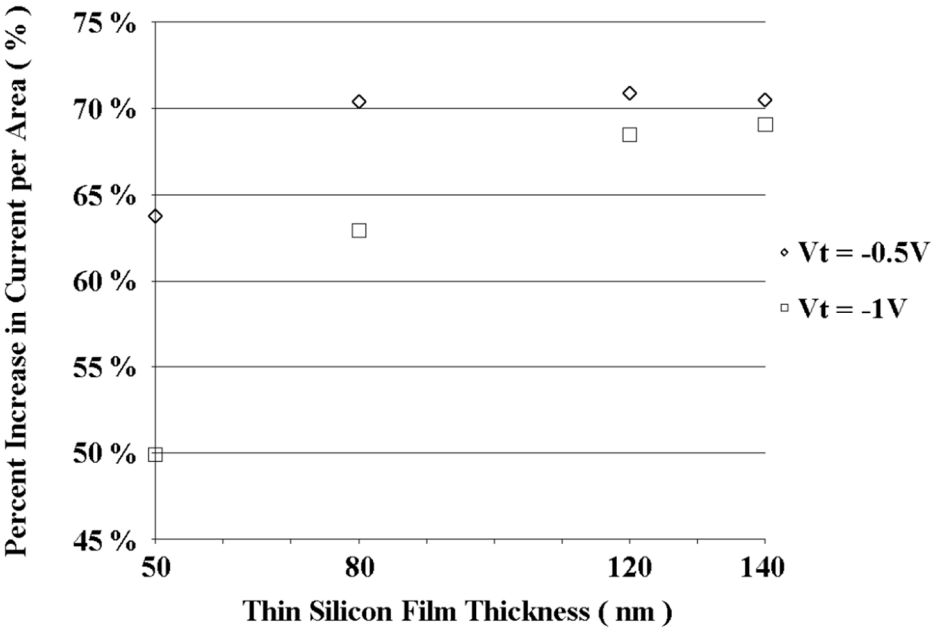

Figure 80: Percent Increase in the Current per Area from Using the PDL Layout Technique Instead of the MFPD Layout Technique for a MESFET with a NiSi Gate and Four Different Thin Silicon Film Thicknesses

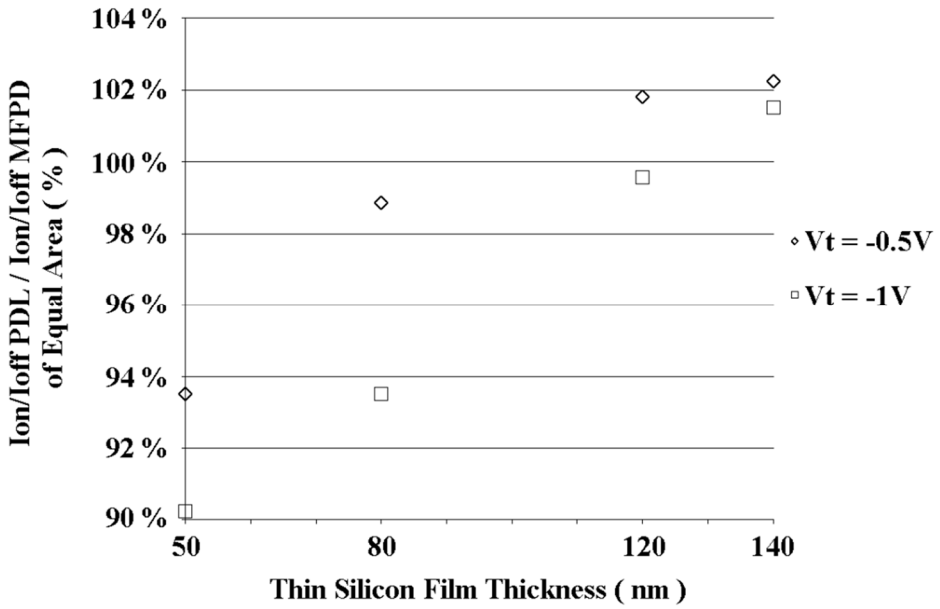

Figure 81: Ratio of the Ion/Ioff Ratio for a MESFET made Using the PDL Layout Technique to the Ion/Ioff Ratio for a MESFET made Using MFPD Layout Technique. For a $CoSi_2$ Gate and Four Different Thin Silicon Film Thicknesses

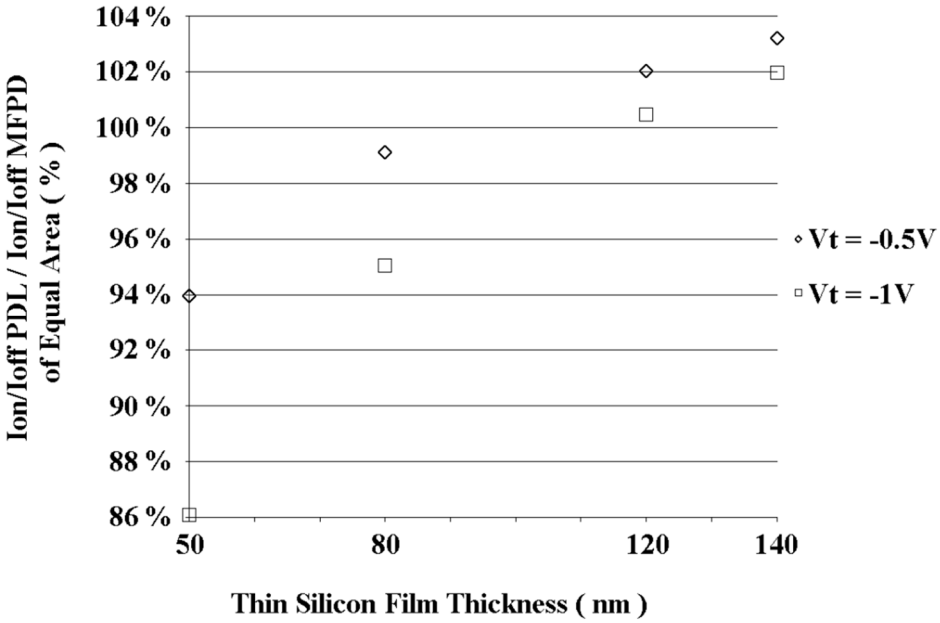

Figure 82: Ratio of the Ion/Ioff Ratio for a MESFET made Using the PDL Layout Technique to the Ion/Ioff Ratio for a MESFET made Using MFPD Layout Technique. For a NiSi Gate and Four Different Thin Silicon Film Thicknesses

As can be seen from the results, the percent increase in the drain current for a device of equivalent area by laying out a PD MESFET using the PDL technique is exceptional. In most cases the percent increase in the bigger devices exceeded the theoretical percent increase of 50%. This is because the conduction per gate square with the gate-effect doping is not equivalent between the two different device types and the theoretical percent increase was derived assuming that there were six gate squares, each of equivalent conductance to the gate square in the MFPD unit cell, in the PDL unit cell. However, unlike before the gate-effect doping was added to the unit cells when the PDL conduction per gate square was lower than the MFPD conduction per gate square, after the addition of the gate-effect doping the PDL conduction per gate square is larger than the MFPD conduction per gate square when assuming a six gate square PDL unit cell. This is because with the addition of the gate-effect doping, the potential along the length of the gate is improved to the point where the seventh gate square in the center of the device will contribute some portion of its area to conduction. In order to make the amount of conduction per gate square equivalent between the two devices, some portion of the seventh gate square would have to be added to the six base gate squares in the PDL unit cell. The fraction of the seventh gate square that would need to be added is different for each thin silicon layer thickness and type of simulated gate silicide so there is no standard gate square adjustment value that can be obtained and added to the six base gate squares. However, regardless of the choice of number of gates per unit cell, the percent increase in current per area values presented remains the same. The exact ratio of equally conducting gate squares of the two different layout techniques can be obtained simply by dividing the current from the simulation of a PDL unit cell by the current from the simulation of a MFPD unit cell. This value can then be used to modify Equation 4.4 and solve for the modified percent increase in current per area, however the modified percent increase in current per area will be exactly the same as the original percent increase in current per area using a ratio of six gate squares in the PDL unit cell to one gate square in the MFPD unit cell. This is because of the way that the equations work out and in the end, the value presented for each percent increase in current per area presented in the above tables is exactly equal to the theoretical value obtained for that device *when and only when* the theoretically calculated value is adjusted using the exact ratio of

equally conducting gate squares of the two different layout techniques per unit cell that is obtained from the ratio of the current from the simulation of a PDL unit cell to the current from the simulation of a MFPD unit cell. This is a means that the values for the percent increase in current per area obtained and presented in Table 4 through Table 7 are not more than the theoretical values due to an under-prediction in their values but that they are equal to their theoretically calculated values when the calculations are properly adjusted. This was verified extensively.

It can be seen from Table 4 through Table 7 that in order to gain current from the use of the PDL MESFET layout technique, the PDL MESFET must be made to be larger than a minimum size, approximately 290 μm^2 for a PDL device *with all equal spacings*, where the PDL MESFET actually has less current per unit area than the MFPD MESFET. This means that the PDL MESFET device is best used as a high current device. Also, from the previous discussion, as the PDL MESFETs gate voltage is increased, due to the reduction of the channel resistance through the reduction of the sub-gate silicon depletion it is likely that this percent increase in the current of the MESFET device will be reduced to a value more similar to that of the device before the gate-effect doping was added. This also means that there will be a larger increase in the percent increase of the current per area from switching from a MFPD MESFET layout to a PDL MESFET layout as the gate bias is made more negative. However, from the Ion to Ioff ratio shown, it is not devastating to the device at all as the off current still remains very low. In other words, the increase in the off current of the device is not of a comparable order to the increase in the on current of the device. One very important thing to note is that all of the simulations for the comparison of the MFPD and PDL MESFET devices were done assuming an ideal Schottky gate contact. This means that actual Ion/Ioff ratios for these devices may not be accurate as when the devices are fabricated they may receive LDD dopings or experience dopant accumulation around the Schottky gate region which will cause the gate tunneling current to force the off current of the device to be much higher than the off gate current for a device with an ideal Schottky gate with no additional and non-ideal fabrication effects as previously discussed. Fortunately, this will not affect the comparison of the two different layout techniques because the ratio of the Ion/Ioff for the PDL MESFET will increase proportionally to the ratio of the Ion/Ioff current of the MFPD

MESFET. This means that the comparison of the Ion/Ioff current of the two different techniques will remain accurate. The only thing that the inclusion of the gate tunneling current will affect is the magnitude of the presented values for the Ion/Ioff ratios of the devices separately.

From Figure 79 and Figure 80 it can be seen that there is an optimum thin silicon layer thickness for a maximum increase in the current per area from using the PDL layout technique over the MFPD layout technique. In Figure 81 and Figure 82 it can be seen that as the thin silicon layer continually becomes thicker, the ratio of the ratio of on current to off current of the PDL MESFET to the ratio of on current to off current of the MFPD MESFET continues to increase unlike the percent increase in current per unit area which is convex and has a maximum when the thin silicon film is around 120nm thick. The ratio of the ratio of on current to off current of the PDL MESFET to the ratio of on current to off current of the MFPD MESFET may also have a maximum but it is not evident from the range of thin silicon film thicknesses simulated herein.

4.11 DESIGN EQUATIONS 2

As previously discussed, the initial design equations that were derived to show that the concept of the PDL MESFET was beneficial assumed a single square value for the entirety of the PDL and MFPD MESFET device. The value that was used for the size of this square was chosen to represent the minimum contact size of a given process as the contact size is likely to be the largest and most limiting dimension in the design of a PD MESFET device. In reality the designer may want to reduce or modify the drain and source access lengths and/or the gate and source/drain contact sizes to be different than the minimum gate length. The design equations that were previously presented were re-derived in order to allow for this. The new design equations with modifiable source and drain access lengths and gate/source/drain contact sizes are presented in Equation 4.11 through 4.14.

$$A_{GT} = d_G^2 \, N_{GST} \, N_f \tag{4.11}$$

$$A_{DT} = d_G N_{GST} \times ((2 d_{D/S} + 2 L_{AD/S} + d_G) + \cdots (d_{D/S} + 2 L_{AD/S} + d_G)(N_f - 1)) \quad (4.12)$$

$$A_{GT} = (d_G (d_{D/S} + 2 L_{AD/S})) \times \cdots \left(2 N_f (N_f - 1) - 4 \, floor\left(\frac{N_f - 1}{2}\right)\right) \quad (4.13)$$

$$A_{DT} = (2 L_{AD/S} + d_{D/S} + d_G)^2 (N_f - 2)^2 + \cdots (2 L_{AD/S} + d_{D/S} + d_G)\left(2 L_{AD/S} + \frac{3}{2} d_{D/S} + d_G\right) \times \cdots 4(N_f - 2) + 4\left(2 L_{AD/S} + \frac{3}{2} d_{D/S} + d_G\right)^2 \quad (4.14)$$

where

A_{GT} = The total area under the gate of the device

N_f = The number of gate fingers

N_{GST} = The total number of gate squares a device is in height

d_G = The length of the gate

$d_{D/S}$ = The length of a drain/source contact

$L_{AD/S}$ = The drain/source access length

A_{DT} = The total area of the device

These equations can be used with simulation results in the exact same way that the previously derived equations can in order to extrapolate a total device current, current per area, and on current to off current ratio. Through a simple analysis of the presented advanced design equations two things can be seen. First, when the different lengths are all set equal to the lengths used in the initial proof of concept equations, the exact same results are given for area and percent

increase in current per area. This helps show the validity and accuracy of the advanced design equations. Second, it can be seen in Figure 83 that the percent increase in current per area increases as the ratio of the MESFET access length to the MESFETs drain, source, and gate contact length/size increases. This means that the PDL MESFET layout technique will become even more useful for higher voltage/breakdown MESFETs in one of two ways. The PDL MESFET layout technique can either allow a MESFET with a given breakdown to have a higher current capability or it can allow a MESFET to have a higher breakdown voltage to with the same current capability of a MFPD MESFET with a lower breakdown voltage. It is up to the designer to decide what is best for their given situation.

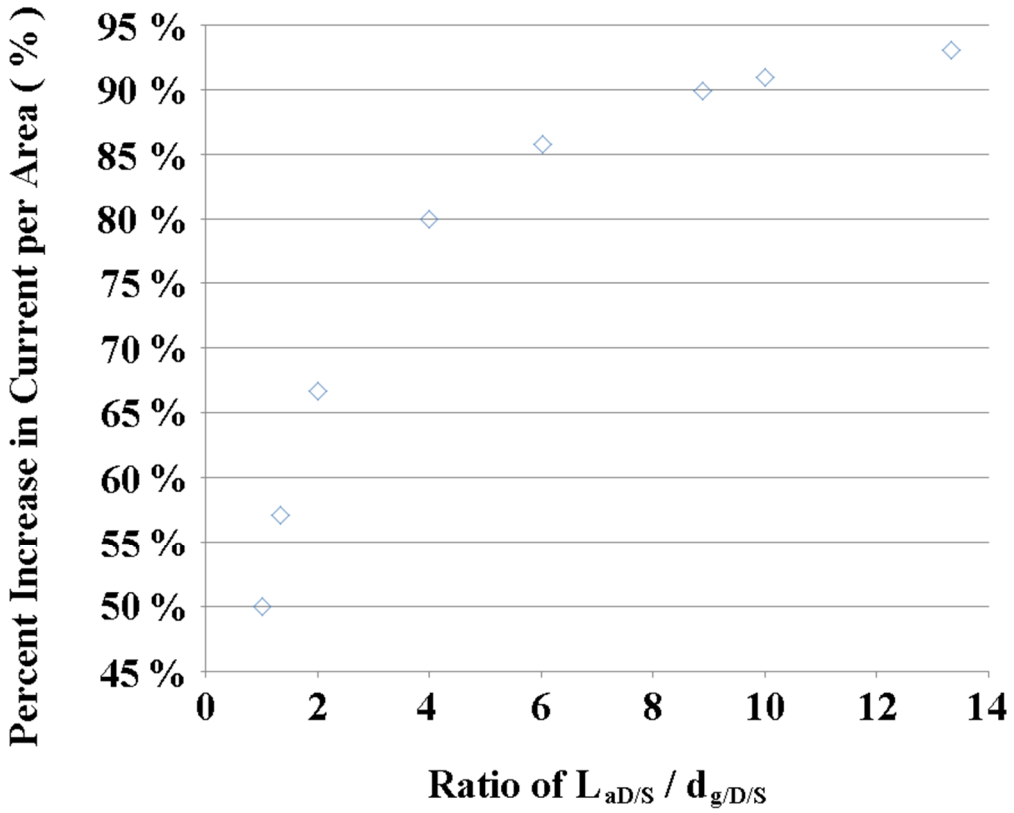

Figure 83: Theoretical Percent Increase in Current per Area as a Function of the Ratio of $L_{aD/S}/d_{g/D/S}$ where $d_{g/D/S} = d_g = d_{D/S}$ without Simulation Data

CHAPTER 5

CONCLUSION AND FUTURE WORK

The modeling of MESFETs must be done carefully in order to obtain proper results. MESFETs that are integrated into standard SOI CMOS processes will receive non-ideal implants that are remnants of the standard modern MOSFET process flow. These implants will alter and/or degrade the characteristics of the MESFET devices. However, modeling can be used to deduce the reasons for the deviation in measured MESFET electrical characteristics from ideal MESFET electrical characteristics.

The ability to easily control/design the threshold voltage of a FD MESFET is very useful and may be the most important device feature to a designer depending on what application they are designing a device for; however, if it is a high current application that a MESFET is to be used in the PD MESFET will be superior by far when compared to a FD MESFET device.

In almost all MESFET applications that do not require a small MESFET device, the PDL MESFET layout technique may be used to yield a device with superior current per area capability. For a PDL MESFET laid out with modified/non-equal dimensions the minimum transistor size for which the PDL MESFET layout technique may become advantageous may decrease or increase from the minimum advantageous size of the single square size PDL MESFET layout. This should be investigated and optimized so that an understanding of the effect of an increase or decrease in the source/drain access lengths and/or gate/drain/source contact size on the percent increase in current per unit area is garnered. Initial calculations show that the PDL MESFET device's advantage over the MFPD MESFET device increases as the ratio of the source/drain access length to source, drain, and gate length/size increases making the device even more advantageous for use in high voltage applications. Then simulations should be done to verify the accuracy of the equations for non-single square PDL MESFET layouts. The final thing that must be done in order to conclude the proof of the PDL MESFET layout technique is the fabrication and measurement of such a device, most likely the single square version.

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