1.7eV $Al_{0.2}Ga_{0.8}As$ solar cells epitaxially grown on silicon by SSMBE using a superlattice and dislocation filters

Arthur Onno[1]*, Jiang Wu[1], Qi Jiang[1], Siming Chen[1], Mingchu Tang[1], Yurii Maidaniuk[2], Mourad Benamara[2], Yuriy I. Mazur[2], Gregory J. Salamo[2], Nils-Peter Harder[3], Lars Oberbeck[3], Huiyun Liu[1]

[1]Department of Electronic and Electrical Engineering, University College London, London WC1E 7JE, United Kingdom
[2]Institute for Nanoscience and Engineering, University of Arkansas, Fayetteville, AK 72701, USA
[3]TOTAL Marketing Services, New Energies Division, 24 cours Michelet, 92069 Paris La Défense Cedex, France

ABSTRACT

Lattice-mismatched 1.7eV $Al_{0.2}Ga_{0.8}As$ photovoltaic solar cells have been monolithically grown on Si substrates using Solid Source Molecular Beam Epitaxy (SSMBE). As a consequence of the 4%-lattice-mismatch, threading dislocations (TDs) nucleate at the interface between the Si substrate and III-V epilayers and propagate to the active regions of the cell. There they act as recombination centers and degrade the performances of the cell. In our case, direct AlAs/GaAs superlattice growth coupled with InAlAs/AlAs strained layer superlattice (SLS) dislocation filter layers (DFLSs) have been used to reduce the TD density from $1\times10^{9}cm^{-2}$ to $1(\pm0.2)\times10^{7}cm^{-2}$. Lattice-matched $Al_{0.2}Ga_{0.8}As$ cells have also been grown on GaAs as a reference.

The best cell grown on silicon exhibits a V_{oc} of 964mV, compared with a V_{oc} of 1128mV on GaAs. Fill factors of respectively 77.6% and 80.2% have been calculated. Due to the lack of an anti-reflection coating and the non-optimized architecture of the devices, relatively low J_{sc} have been measured: $7.30mA.cm^{-2}$ on Si and $6.74mA.cm^{-2}$ on GaAs. The difference in short-circuit currents is believed to be caused by a difference of thickness between the samples due to discrepancies in the calibration of the MBE prior to each growth. The bandgap-voltage offset of the cells, defined as $E_g/q-V_{oc}$, is relatively high on both substrates with 736mV measured on Si versus 572mV on GaAs. The non-negligible TD density partly explains this result on Si. On GaAs, non-ideal growth conditions are possibly responsible for these suboptimal performances.

Keywords: III-V on silicon, AlGaAs solar cell, MBE, Threading dislocation density, Dislocation filter, Superlattice

1. INTRODUCTION

Silicon and III-V compound semiconductors are currently the two dominant material systems in the semiconductor industry. As the fundamental material for solid-state electronics and photovoltaics, Si is a critical industrial platform benefiting from a very mature technology and an extremely robust industrial supply chain. Its low cost, lightweight and higher mechanical strength compared with III-V materials also make it a choice material as a substrate. In contrast, due to their direct bandgap and higher electron mobility, III-V compounds are the building blocks for optoelectronics and very high efficiency multijunction photovoltaic solar cells but suffer from a serious cost disadvantage compared to Si. Integration of high quality III-V compounds on a Si substrate is therefore of great interest, opening the field for new technologies such as silicon photonics and low cost high efficiency silicon-based multijunction solar cells. The latter have experienced a strong interest from academia and the industry in the recent years [1-9].

Two main technologies are currently under investigation in order to develop III-V on silicon devices: direct epitaxy and wafer bonding. Wafer bonding consists in preparing the two materials on separate Si and III-V (usually GaAs or InP) substrates before bonding them together and removing the III-V substrate by a lift-off process, leaving the engineered layer of III-V material on the Si substrate [10-11]. Although the material quality of the III-V on Si layer is optimal using this technique and, in the case of III-V on Si multijunction solar cells, very good results have been achieved [9], issues arise with scaling up to large industrial size wafers. Moreover the bonding process requires very high surface quality and flatness for both wafers and the reuse of the III-V substrate is not ensured, leading to a high cost structure and a difficult industrialization of the technology.

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Direct epitaxy presents a more straightforward pathway by using less processing steps and fewer tools: the III-V material is epitaxially grown on the Si substrate [1-9] – sometimes using a previously grown intermediary SiGe buffer [5-8] – with the possibility of using only one growth reactor such as MBE or MOCVD [1-2]. The main obstacles are the nucleation of defects at the III-V/Si interface due to the polar-on-nonpolar nature of the heterostructure, the lattice-mismatch and the difference of thermal expansion coefficient between the materials. These defects, in particular threading dislocations (TDs) due to the lattice-mismatch, propagate upwards in the III-V material to the active regions of the device where they act as recombination centers for carriers. As a result, the lifetime and diffusion length of minority carriers is reduced, leading to low performance devices.

The issues regarding antiphase domains (APDs) caused by polar-on-nonpolar epitaxy have been resolved using (100) Si wafers with a 4° to 6° offcut in the (111) direction [12-13], ensuring a two-step organization of the Si surface prior to growth. Multiple pathways are under investigation in order to mitigate the nucleation of TDs and reduce the threading dislocation density (TDD) to a minimum [14]. Direct growth of an AlGaAs buffer followed by strained-layer-superlattices (SLS) acting as dislocation filters layers (DFLs) in order to reduce the TDD has recently yielded excellent results for III-V on Si lasers [15]. In the case of high-efficiency III-V/Si dual junction solar cells, where a 1.7eV bandgap III-V top cell is grown on a 1.12eV Si bottom cell, the main pathway followed is the use of metamorphic buffers, either through a SiGe on Si metamorphic buffer ending up in a SiGe or full Ge virtual substrate on which lattice-matched GaAs or GaAsP epitaxy is performed [5-8] or through a GaP on Si nucleation layer followed by a metamorphic GaAsP buffer on which the 1.7eV GaAsP cell is grown [1-4,9]. However direct GaAs nucleation on Si to grow a high bandgap 1.5-1.7eV AlGaAs cell on a Si substrate has not been reported since the work of Umeno and Soga [16-20] in the 1990s. Moreover, SLS DFLs for III-V on Si solar cells applications have so far only been used by Yamaguchi *et.al.* to grow pure GaAs cells [21]. We present here the first 1.7eV AlGaAs solar cell on Si using direct AlGaAs growth and SLS DFLs. Compared with the reference AlGaAs cells grown on lattice-matched GaAs, our early prototype cells grown on Si present promising results with a TDD in the lowest achieved for such a structure. Given the non-optimized growth sequence used for the active layers of the AlGaAs cells, the electrical performances of the cells are also encouraging.

2. EXPERIMENTAL METHODS

2.1 Growth technique

Samples were grown in a Veeco GEN930 solid-source Molecular Beam Epitaxy (MBE) reactor. Temperatures were measured using an infrared pyrometer and a substrate holder-mounted thermocouple. Growth was monitored in-situ using Reflection High-Energy Electron Diffraction (RHEED). Growth was performed on n-type Si (100) substrates offcut 4° toward the [110] plane in order to avoid APD formation [12-13] and on standard n-type GaAs substrates. Prior to growth, in-situ oxide desorption was carried out at 900°C for 10 minutes for Si substrates. For GaAs substrates, in-situ oxide desorption was carried out between 580°C and 610°C, using RHEED measurements to monitor the desorption process.

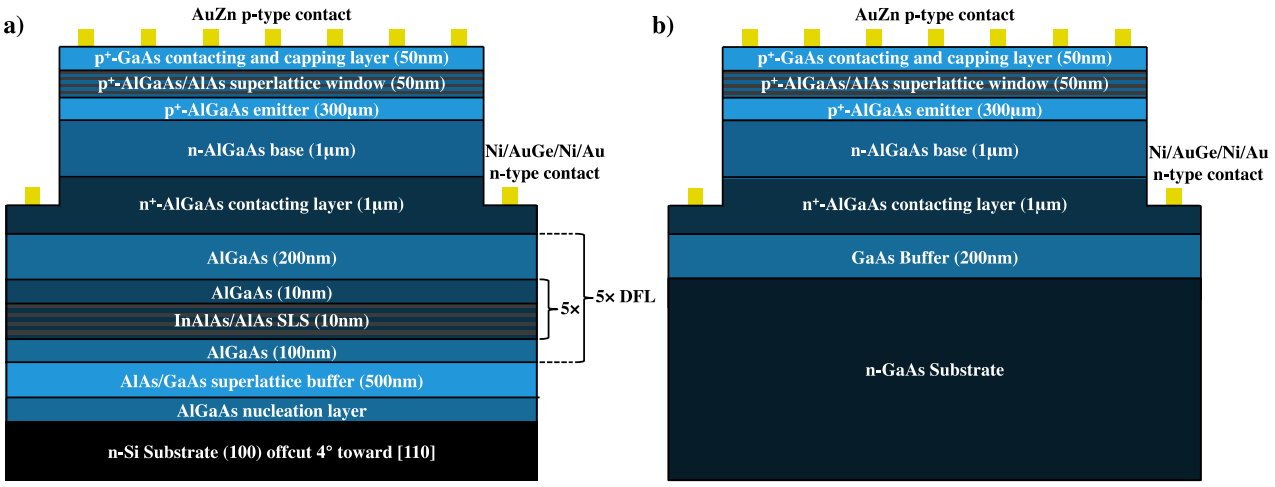

Figure 1. Detail of the structures of the devices grown and fabricated on Si (a) and GaAs (b) substrates.

The structures grown are detailed in Figure 1. For growth on Si substrates, the nucleation sequence has been detailed in previous publications [22-23]. Because of the large lattice-mismatch between Si and AlGaAs (about 4%), Stranski-Krastanov (SK) growth mode is observed during the initial stages of growth, with formation of islands that later coalesce. This is attested by the spotty RHEED measurements observed during the first steps of the growth. Because of this initial SK growth mode a wavy growth surface is obtained, impeding the fine engineering of 2-dimensionnal structures such as dislocation filters. In order to flatten out the growth interface and obtain a smooth surface, a 500nm-thick AlAs/GaAs superlattice is used, leading to a streaky RHEED pattern prior to the growth of the dislocation filters.

Following the AlAs/GaAs superlattice, 5 InAlAs/AlAs SLS DFLs were grown. Each individual InAlAs/AlAs SLS DFL consists of 5 InAlAs/AlAs SLSs separated by 10nm AlGaAs and inserted between 100 and 200nm-thick AlGaAs separation layers. Hence each DFL is separated from the precedent one by a 300nm-thick AlGaAs layer. This type of InAlAs-based SLS DFL has previously shown excellent results in improving material quality, each DFL reducing the TDD by about half to a full order of magnitude [15]. Identical cells were grown on Si and GaAs wafers: directly on the substrate in the case of GaAs, on top of the last DFL in the case of Si. The cells structure, detailed in Figure 1, consists of a 1µm n^+-$Al_{0.2}Ga_{0.8}As$ contacting layer ($N_d=2\times10^{18}cm^{-3}$), a 1µm n-$Al_{0.2}Ga_{0.8}As$ base ($N_d=2\times10^{17}cm^{-3}$), a 300nm p^+-$Al_{0.2}Ga_{0.8}As$ emitter ($N_a=1\times10^{18}cm^{-3}$), a 50nm p^+-AlAs/AlGaAs superlattice window layer ($N_a=1\times10^{18}cm^{-3}$) and finally a 50nm p^+-GaAs contacting layer ($N_a=1\times10^{19}cm^{-3}$). Si and Be sources were used for the doping.

2.2 Device fabrication

Standard photolithography techniques have been used before selective wet etching and contacts deposition. A mesa etch has been performed using H_2SO_4:H_2O_2:H_2O 1:10:80 in order to isolate $3\times3mm^2$ individual cells and to access the n^+-AlGaAs contacting layer. Before thermal evaporation of the contacts, NH_4OH:H_2O 1:19 solution has been used for 60s to deoxidize the surfaces. The 5nm/100nm/30nm/200nm-thick Ni/AuGe(Au 88%, Ge 12%)/Ni/Au contact structure deposited on the n^+-AlGaAs contacting layer has been annealed at 400°C for 60s before evaporation of the ≈200nm-thick AuZn (95% Au, 5% Zn) contact on the p^+-GaAs contacting layer. No anti-reflection coating was applied on the front surface of the cells. The 50nm GaAs top contacting and capping layer was not etched in order to protect the underlying Al-rich layers from oxidation. As a result substantial parasitic absorption is to be expected from this lower bandgap front layer. As the front contact covers a sizable portion of the front surface ($3.14mm^2$), the considered area for the reported measurements refers to the $5.86mm^2$ active area of the cells.

2.3 Characterization

Atomic Force Microscopy (AFM) and cross-sectional Transmission Electron Microscopy (TEM) have been used to characterize the structural properties of the grown samples. AFM was carried out with a Veeco Nanoscope V Dimension 3100 SPM system in ambient conditions using tapping mode. For the cross-sectional TEM measurements, the samples were prepared using mechanical polishing followed by ion-milling in a Fischione 1010 ion mill. The TEM observations were performed at 300keV in an FEI Titan 80–300 S TEM fitted with a CEOS image corrector. The cells bandgap was determined by room-temperature steady-state Photoluminescence (PL) using a Nanometrics RPM2000 rapid photoluminescence mapping system.

We measured the current density vs. voltage (J-V) relation of the devices at 25°C, in the dark and under illumination, using a Keithley 2400 sourcemeter coupled with ReRa Tracer 3.0 software. A LOT solar simulator equipped with a filtered xenon lamp, calibrated to reproduce the AM1.5G spectrum, was used as the light source. Room-temperature External Quantum Efficiency (EQE) measurements were performed with a calibrated SpeQuest Quantum Efficiency system from ReRa.

3. RESULTS AND DISCUSSION

Figure 2 shows a comparison between the surfaces of the samples grown on Si (a) and GaAs (b). Growth on Si is relatively smooth with an RMS of 2.20nm versus an RMS of 0.48nm on GaAs. This higher roughness on Si is due to relaxation of the strain caused by the 4% lattice-mismatch between the Si substrate and the AlGaAs material. As previously demonstrated by Petroff *et. al.* [24] and Xu *et. al.* [25], the AlAs/GaAs superlattice used prior to growth of the dislocation filters as contributed to the reduction of the roughness on Si. This is attested by the modification of the RHEED measurements from a spotty pattern to a streaky pattern during the superlattice growth. PL measurements show very close peaks (729.4nm on Si and 728.3nm on GaAs), indicative of a bandgap of 1.70eV for both samples.

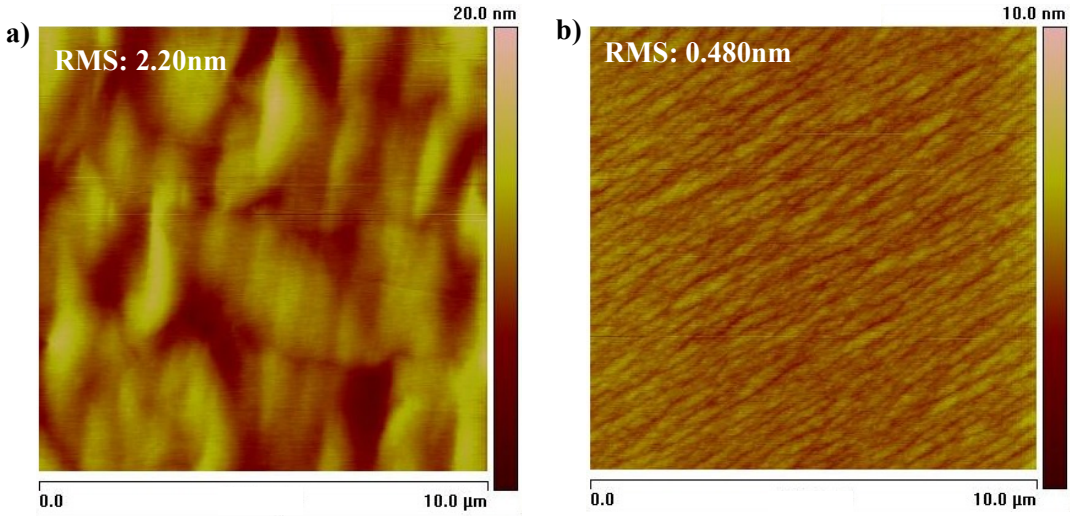

Figure 2. AFM images of the top surfaces of the samples grown on Si (a) and GaAs (b) substrates.

Impact of the DFLs on the TDD for the sample grown on Si is shown on the cross-sectional TEM image in Figure 3. As demonstrated previously [15], each SLS DFL reduces the TDD by about a half to a full order of magnitude. The TDD, calculated from TEM, has been reduced from 1×10^{9}cm^{-2} at the III-V/Si interface to $1(\pm0.2)\times10^{7}$cm^{-2} in the active layers of the devices. As the TDD approaches 10^{7}cm^{-2}, calculating a precise value becomes challenging and only an approximate count can be given. However, given the TDD reduction trend exhibited by the DFLs, a TDD in the high 10^{6}cm^{-2} can be expected in the present sample. This extrapolated TDD value would be lower than the current record of 1.1×10^{7}cm^{-2} for direct epitaxial AlGaAs solar cells on Si [18-19]. Moreover, for AlGaAs solar cells with such a high Al content (20%), the best TDD published so far is 2.1×10^{7}cm^{-2} [20]. Even considering the upper bound for our sample (1.2×10^{7}cm^{-2}), we demonstrate a 1.7eV $Al_{0.2}Ga_{0.8}As$ photovoltaic solar cell with a lower TDD.

TEM imaging of both samples also confirms a difference of thickness between the devices grown on Si and GaAs: 2.8µm on Si versus 2.35µm on GaAs for the thickness of the active layers (base, emitter, window and both contacting layers). This difference of thickness, due to discrepancies in the calibration of the MBE growth rates, explains the difference in short-circuit current and in EQE presented below.

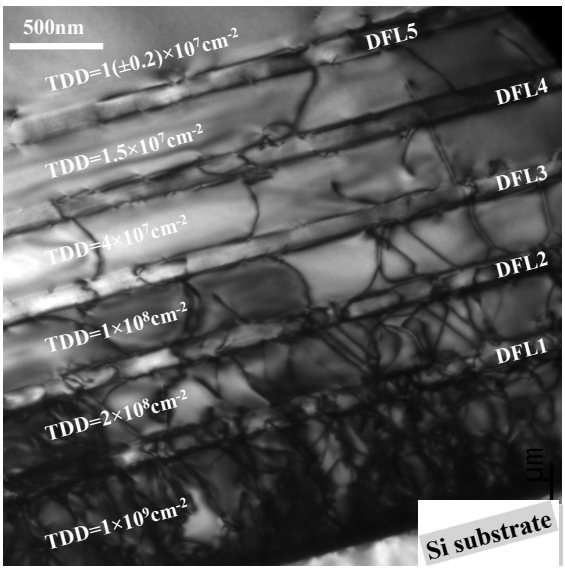

Figure 3. Cross-sectional TEM of the sample grown on Si, showing the 5 Dislocation Filter Layers (DFLs) and the associated reduction of the Threading Dislocation Density (TDD).

Light J-V curves of the best devices grown on Si and GaAs are displayed in Figure 4. The best cells exhibit a V_{oc} of 964mV on Si versus 1128mV on GaAs. This difference of V_{oc} between lattice-matched and 4%-lattice-mismatched samples is an encouraging first result given the non-negligible TDD on Si. Fill factors of respectively 77.6% and 80.2% have been extracted. Relatively low J_{sc} have been measured: 7.30mA.cm^{-2} on Si and 6.74mA.cm^{-2} on GaAs. Multiple causes are responsible for these low J_{sc} values. First the architecture of the cells is non-optimized with a thin base (1µm), not thick enough to efficiently absorb the incoming light, especially for photons with energy close to the bandgap as shown on the EQE measurements. The absence of an anti-reflection coating and the reduced roughness of the top surface are also accountable for a sizable front surface reflection. Finally the 50nm-thick top GaAs capping and contacting layer may be responsible for a non-negligible parasitic absorption. Best efficiencies are respectively 5.46% and 6.09% on Si and on GaAs. As expected, the difference of efficiency is mainly due to the 164mV drop of V_{oc} for lattice-mismatched devices compared with lattice-matched ones.

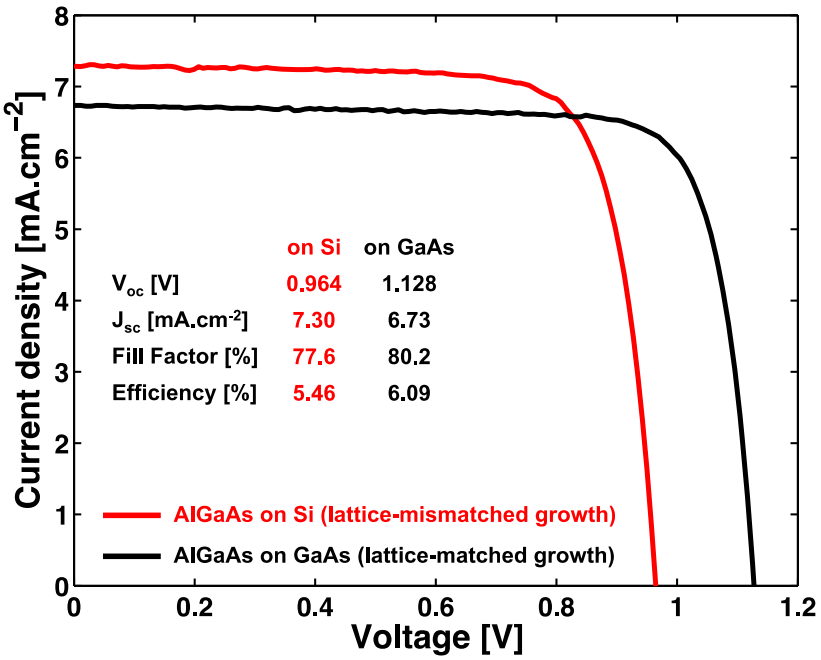

Figure 4. Under illumination J-V curves of the best devices grown on Si (red) and GaAs (black). Cells parameters are also indicated.

Although the lattice-matched sample grown on GaAs exhibits a better V_{oc} than the one grown on Si, the V_{oc} absolute value is still small at 1128mV. The bandgap-offset voltage, defined as E_g-qV_{oc}, is in particular pretty large at 572meV compared with the ≈0.3-0.4V semi-empirical value expected for high quality materials. This behavior suggests a high dark saturation current strongly dominated by non-radiative recombinations. We suspect that these suboptimal performances on GaAs are due to non-optimal growth conditions, in particular a possible oxygen contamination during growth which, as Amano *et. al.* have shown [26], severely degrades the minority carriers diffusion length. Although some oxygen-related defects are probably also present in samples grown on Si, the recombinations due to TDs dominate in these and are the main source of inefficiencies.

EQE measurements for both samples are displayed in Figure 5. As the J_{sc}-calibrated measurements (a) show, the principal source of difference between the J_{sc} of the cells is an overall better absorption for the device grown on Si. However the normalized EQE (b) indicates a better blue response for the samples grown on GaAs. These results are in line with the difference of thickness between the samples measured by TEM: the thicker base on Si allows for higher overall absorption but in return the thicker highly doped emitter reduces the blue response. The rougher surface on Si, possibly scattering the incoming light, can also explain part of this behavior. The non-optimized structure of the devices, in particular the thin base (1µm), could explain the weak absorption of higher wavelength photons with energy close to the bandgap. Short diffusion lengths could also be responsible for this phenomenon and more work is needed to exactly determine the source of these relatively poor optical performances.

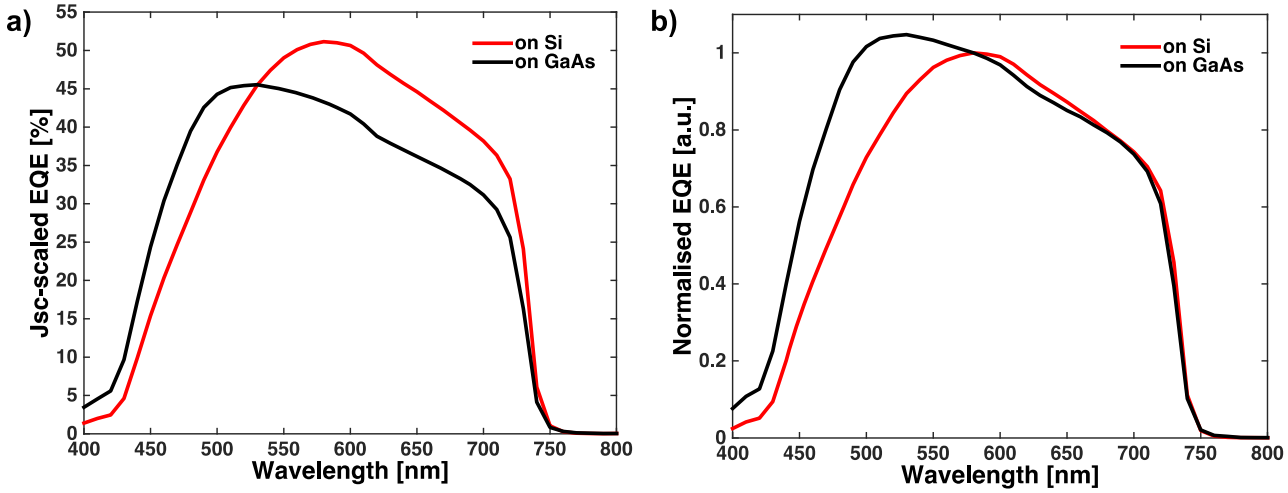

Figure 5. J_{sc}-scaled (a) and normalized (b) EQE of the samples grown on Si (red) and (GaAs) showing an overall stronger absorption in the lattice-mismatched sample grown on Si but a better blue response for the sample grown on GaAs.

4. CONCLUSION

1.70eV AlGaAs photovoltaic solar cells have been grown on lattice-mismatched Si and lattice-matched GaAs substrates by Solid Source Molecular Beam Epitaxy. For cells grown on Si, strained layer superlattice dislocation filter layers have been used to reduce the threading dislocation density (TDD) from $1\times10^{9}cm^{-2}$ at the III-V/Si interface to $1(\pm0.2)\times10^{7}cm^{-2}$ in the active region of the devices. This TDD represents one of the lowest value published for direct epitaxial growth of AlGaAs solar cells on Si substrates, in particular considering the high Al-content (20%) and the high bandgap of the grown devices. Best cells exhibit a V_{oc} of 964mV on Si versus 1128mV on GaAs with fill factors of respectively 77.6% and 80.2%. Although low in comparison with the literature, the TDD is still impacting the performances of the cells, explaining this drop in V_{oc} and fill factor. The difference of J_{sc} between the devices ($7.30mA.cm^{-2}$ on Si, $6.73mA.cm^{-2}$ on GaAs) is explained by the difference of thickness between the samples, due to discrepancies in the calibration of the MBE growth rates. More work is needed to fully characterize the samples, in particular the non-TD-related defects on both substrates and their respective impact, and to optimize the growth sequence to obtain high material quality devices on GaAs and on Si. The low TDD achieved is nonetheless an encouraging first result, showing the relevance of direct monolithic growth of AlGaAs on Si using dislocation filters for the development of high efficiency III-V/Si dual junction photovoltaic solar cells.

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