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Nanosecond Analog Programming of Substoichiometric Silicon Oxide Resistive RAM

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***Abstract*— Slow access time, high power dissipation and a rapidly approaching scaling limit constitute roadblocks for existing non-volatile flash memory technologies. A new family of storage devices is needed. Filamentary resistive RAM (ReRAM) offers scalability, potentially sub-10nm, nanosecond write times and a low power profile. Importantly, applications beyond binary memories are also possible. Here we look at aspects of the electrical response to nanosecond stimuli of intrinsic resistance switching TiN/SiO_x/TiN ReRAM devices. Simple sequences of identical pulses switch devices between two or more states, leading to the possibility of simplified programmers. Impedance mismatch between the device under test and the measurement system allows us to track the electroforming process and confirm it occurs on the nanosecond timescale. Furthermore, we report behavior reminiscent of neuronal synapses (potentiation, depression and short-term memory). Our devices therefore show great potential for integration into novel hardware neural networks.**

***Index Terms*— Nanotechnology, resistance switching, memories, dielectric materials, titanium compounds, silicon compounds, analog memories, neural network hardware, pulse measurements.**

I. Introduction

Reduced power consumption and higher device density are required in current and future portable and embedded devices. Consequently, non-volatile memory (NVM) technologies are constantly evolving. Flash memory is at present the most popular solid-state storage technology [1]. However, relatively low endurance, slow access speed, high write voltages and severe scaling issues hinder its future [2]. A replacement must therefore be developed [3].

Two-terminal filamentary resistive RAM (ReRAM) devices are an appealing alternative and exploit resistance switching. This phenomenon has been studied since the 1960s [4]. Two electrodes sandwich a dielectric film, which can be switched into a conductive state by applying an electrical voltage in a process known as electroforming [5]. Lower voltages are subsequently used to induce cycling between different resistance states, leading to a device with programmable resistance [6].

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These devices are highly non-linear, exhibit switching times in the nanosecond range [7-10] and can be separated into two categories: extrinsic devices form conductive filaments thanks to metal ion migration from an electrochemically active anode into the dielectric. Intrinsic devices [11] rely on the innate properties of their dielectric to form a conductive filament, generally associated with chains of oxygen vacancies. Filaments can have diameters in the nanometer domain, potentially allowing for device scaling beyond that of flash [12].

Away from digital memory, filamentary ReRAM [13, 14] has recently shown behavior resembling that of biological synapses. Potentiation, depression, plasticity, and short-term memory have been observed in these devices, suggesting potential deployment in hardware neural networks. This can lead to dramatically higher power efficiency than emulations run on digital computers [14].

In this study we used TiN/SiO_x/TiN devices, as they exhibit intrinsic switching and are fully CMOS compatible. We demonstrate that not only are these devices programmable using conventional voltage sweep characterization, but they may also be programmed using very simple pulses of a fixed voltage, changing only pulse duration. This novel programming approach can also be used to emulate analog behavior resembling that of biological synapses.

II. Our Devices

A. Physical description

We performed our measurements on TiN/SiO_x/TiN devices with 100 nm thick TiN electrodes sandwiching an SiO_x active layer of 37 nm thickness. This layer is amorphous, sub-stoichiometric ($x \approx 1.3$, confirmed by XPS measurements), and rich in defects, which include oxygen vacancies [15]. Further fabrication and structural characterization details are given elsewhere [15], but briefly all layers were sputter-deposited, with the active layer co-sputtered from Si and SiO_2 targets. Conventional lithography was used to pattern the top TiN layer into individual square sub-devices whose edge lengths range from 120 µm to 400 µm. Our device structure is shown schematically in Fig. 1.

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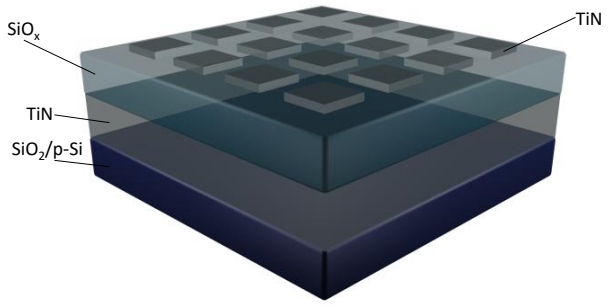

Fig. 1 Schematic of our device (not to scale). TiN layers are 100 nm thick. The active SiO_x layer is 37 nm thick.

Our devices operate in air and exhibit intrinsic switching through the formation of filaments of oxygen vacancies, which means that no metal diffusion occurs from the TiN into the SiO_x, as we have confirmed previously [15].

B. Switching mechanics

We have previously published analyses of the resistance switching mechanism in our devices, hence a detailed description of switching mechanics can be found in [11] but, briefly, similarly to most intrinsic or valence change memory (VCM) systems, oxygen is initially moved in SiO_x by the application of an external electric field [12, 15]. Fig. 2 shows schematically an initially pristine device containing only few oxygen vacancies. It exhibits very high resistance. Following application of an electroforming voltage with a current limit applied to prevent destructive breakdown, some oxygen ions will migrate towards the anode, leaving behind a filament of oxygen vacancies. These, under electron injection, provide a conductive pathway for electrons. This important forming step establishes filament strength and therefore the future resistance states of the device.

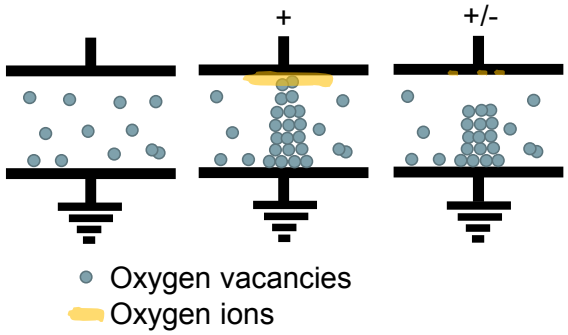

Fig. 2 The different resistance states of a device. From left to right, "pristine", "formed", and "reset".

The device has now entered a low resistance state (LRS). The conductive filament can be broken using a lower voltage bias with no current limit, which increases oxygen ion mobility through Joule heating, enabling oxygen ions to re-oxidize the top part of the filament. This *reset* process has now taken the device into a high resistance state (HRS), which is intermediate between the pristine and low resistance states. The combination of reliance on electric-field and Joule heating classifies this as a thermochemical memory system (TCM) [12]. Restoring the filament requires a lower voltage than that originally required to electroform; it is commonly accepted that there now is only a small gap requiring field-driven oxygen depletion. This third and last process is known as device *setting*. A low read voltage (<1 V) is used to sample the device resistance without disturbing it. Fig. 3 shows a typical sequence of electroforming, resetting and setting for an SiO_x-based device.

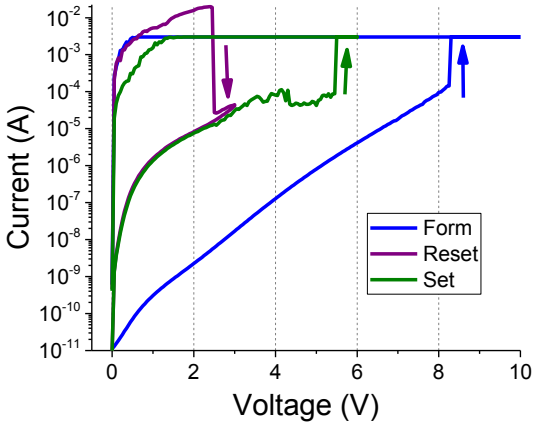

Fig. 3 Typical IV switching curves for our devices. Electroforming requires the highest voltage. Resetting requires the lowest voltage but highest current. Setting requires an intermediate voltage. Some competing processes can be seen, particularly in the set curve.

III. Device Characterization

A. Electrical approaches

Three approaches were used to electroform, reset and set. The first was to sweep the voltage across the device while sampling current – this is a standard technique in ReRAM [11, 16-20]. The voltage was gradually increased to a maximum value and then slowly returned to zero; a current compliance was enforced during electroforming and setting to prevent permanent breakdown. Current compliance was not needed when resetting as returning the device to a HRS relies on current-induced Joule heating filament breaking.

Once we determined the switching voltages of our devices using voltage sweeps, we used voltage pulses both with and without current compliance (second and third approaches, respectively) to program devices. In the third approach we switched using pulses hundreds of nanoseconds long. Compliance limits the current by reducing the applied voltage when device resistance drops during electroforming or setting, effectively reducing the length of a pulse. Therefore, programming is also possible using short pulses without compliance.

Applying pulses that are too short sets devices into unstable states whose transient behavior can be sampled by low voltage reading pulses. Applying pulses that are too long will irreversibly damage devices. The forming step defines the device by defining its filament strength. We expect devices formed with current compliance to have stronger filaments than those formed with pulses that are long enough to form a filament but too short to form an ideal filament lest we burn our device.

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B. Characterization equipment

We used a Keithley 4200 Semiconductor Characterization System to carry out voltage sweeps with current compliance using its Source Measure Units (SMUs). The same hardware, now externally controlled, was used to carry out measurements using long (tens of microseconds or longer) pulses with current compliance. The same system includes a Pulse Measure Unit (PMU), which we used to carry out short pulse measurements (in the tens to hundreds of nanosecond range) without current compliance. Custom MatLab scripts controlled the system either directly or through custom C drivers running on it. In all cases we contacted devices with tungsten needle probes in a Signatone probe station. We used a 5 Gs/sec Tektronix oscilloscope to measure device resistance changes in the nanosecond time domain.

IV. Results

A. Traditional characterization using voltage sweeps

We used more than 3000 sweeps to determine the switching voltages of our devices. On average, setting occurs at 3.7 V with a current compliance of 3 mA, and resetting at 2.7 V without compliance. Electroforming occurs at around 7 V in sweeps with a 3 mA current compliance. These values were used as the starting point for pulsed characterization. Fig. 3 shows typical IV curves for one of our unipolar 100 µm by 100 µm devices, demonstrating their highly non-linear nature. It is partially the exploitation of this property that allows fast switching and neuromorphic behavior. While other devices in the literature show slightly lower switching voltages they do not solely rely on highly CMOS compatible silica in the active layer [7, 21, 22].

B. Characterization using long pulses with current compliance.

Pulses as short as 13 µs with current compliance were used to determine device endurance and reliability. We tested cycling endurance by first electroforming a device and subsequently sending alternating reset and set pulses. These were interleaved with low voltage read pulses known not to affect the device state. Fig. 4 shows 200 switching events. Electroforming in this case was carried out at 15 V with 3 mA current compliance, resetting at 2.7 V (no current compliance) and setting at 7 V with 3 mA current compliance. In this particular case, however, pulse length was extended to minimal plus 3 seconds. Reading pulses were 1 V without compliance and their length depended on instrument settling time. While there are reports of high levels of cycling endurance in the literature, it must be noted that these do not report every switching event [23, 24], and in any case high endurance was not the goal of this study. When all switching events are provided, it is usually only over a few hundred events [18, 24]. We measured every cycle.

It was also possible using pulses to test the stability of the low and high resistance states. We did this for the low resistance state by electroforming a device and then applying a read pulse every 100 seconds for 10,000 seconds. We used the same reading operations for a reset device. Read pulses used were similar to those described above, though the device was formed into a higher resistance state (recall that electroforming determines the resistance states of the device). Results shown in Fig. 5 show that both states are stable even at an elevated temperature of 85 ˚C.

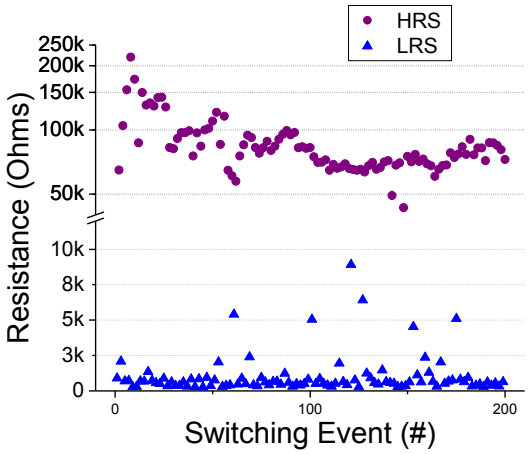

Fig. 4 Cycling endurance test of one of our devices. At least half an order of magnitude of difference is maintained between the states. Note the gap in the y-axis that allows both states to be shown clearly on a logarithmic scale.

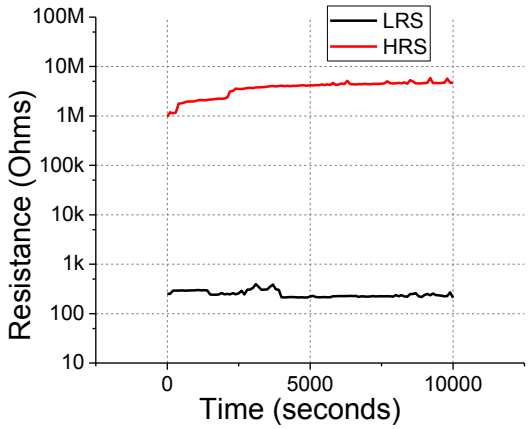

Fig. 5 Device stability at 85 ˚C over 10,000 seconds. Devices are stable in both states.

C. Characterization using short pulses to emulate current compliance behavior.

With current compliance imposed, as device resistance drops so does the applied voltage, limiting the current through the device. We observed using an oscilloscope that the voltage drops in less than 100 nanoseconds, including delays from active circuitry in the characterization system. This implies that long pulses with current compliance may be replaced with shorter pulses without compliance. Pulse duration may then be tailored to quickly drop the applied voltage once the switching event has taken place. Complex programmers that implement current compliance are therefore not necessary as similar pulses may be generated to those generated using current compliance.

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D. Switching with non-identical pulses

Switching using pulses with durations in the tens to hundreds of nanoseconds range was possible on a device formed with a fast pulse, as shown in Fig. 6. Here, we carried out setting with 7 V, 100 nanosecond pulses and resetting with 3.5 V, 100 nanosecond pulses. However, given that the output impedance of the PMU is 50 Ω, impedance mismatch must be taken into account. The PMU assumes a target impedance of 1 MΩ. This means that the voltage output applied on the device under test depends on its resistance. We can relate nominal voltage to applied voltage (equation 1). Here we assume that we have an ideal voltage source in series with a 50 Ω resistor (the output impedance of the PMU) as well as a resistor whose resistance is the one of the device under test (R_{DUT}).

$$V_O = \frac{V_i}{50+R_{DUT}} R_{DUT} \qquad (1)$$

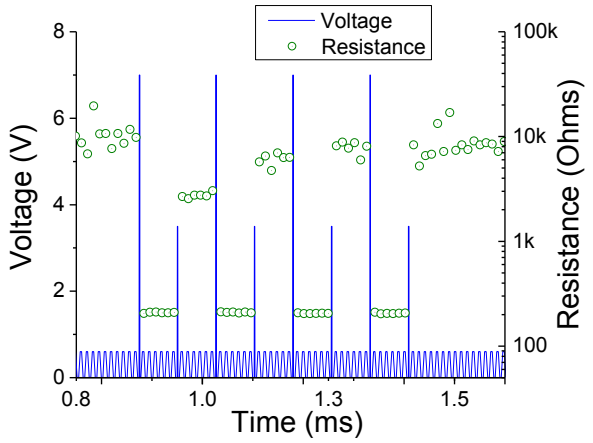

Fig. 6 Device cycling using fast pulses without current compliance. Pulses of 7 V and 100 nanoseconds were used to set, 3.5 V and 100 nanoseconds to reset. These nominal voltages are higher than those dropped across the device due to impedance mismatch. The device was formed using a fast pulse.

1) Exploiting impedance mismatch – identical pulses

Thanks to impedance mismatch, device voltages reduce as the state transitions to a low resistance. A plot showing the measured device voltage during electroforming (rather than the nominally applied voltage) is shown in Fig. 7; here the voltage tracks the device resistance, allowing us to monitor the dynamics of the forming process directly. The reset voltage must be lower than the set voltage. It therefore plays to our advantage that, as a result of (1), the applied voltage is lower when a device is in its LRS. It seems logical to exploit programmers with low output impedance in order to use a single programming voltage of varying duration. This could lead to simplified programming circuits whose nominal output voltage never needs to change.

After electroforming with 15 V, 200 nanosecond pulses, applying 15 V, 75 nanosecond pulses switches the device between states (Fig. 8). These identical switching pulses confirm that it is possible to exploit impedance mismatch to simplify programming circuits.

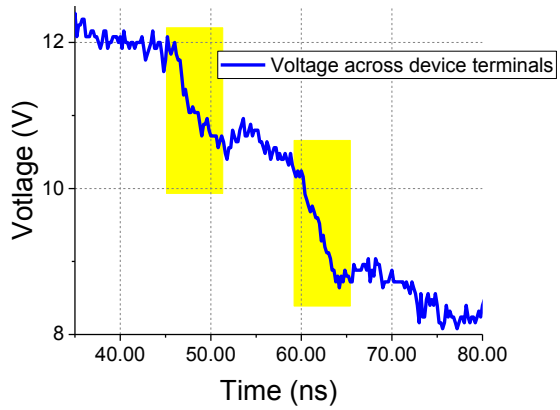

Fig. 7 Voltage across terminals of a device being electroformed using a ~100 nanosecond pulse without current compliance. Abrupt drops in voltage (highlighted) correspond to filament formation and occur due to impedance mismatch. In this case, it appears that the process has two steps with some competing elements (such as thermal effects from Joule heating), and it occurs on the scale of nanoseconds. After 80 ns the plot plateaus until the pulse ends.

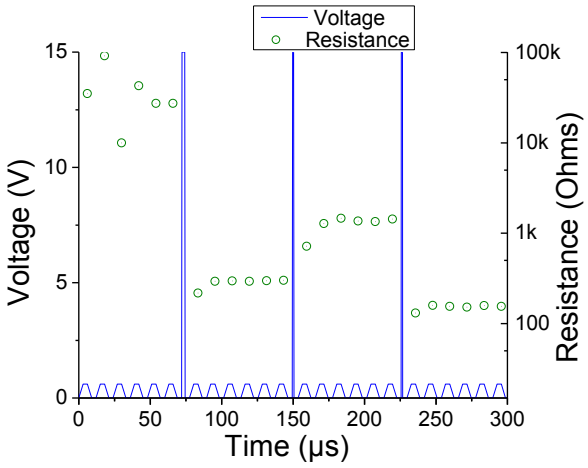

Fig. 8 Switching using pulses of identical magnitude. Following electroforming with a 15 V, 200 nanosecond pulse, the device is switched with 15 V, 75 nanosecond pulses. Due to impedance mismatch, the lower the device resistance, the lower the device voltage.

2) Emulation of neuronal behavior

Short pulses can also be used to program devices into temporary or unstable states. While this is not directly relevant for digital storage, it is a property that has interesting analog applications. One of these is the emulation of some of the behavior of biological synapses. Fig. 9 shows a temporary electroform (10 V, 100 nanoseconds) that gradually relaxes into a high resistance state. However, a further pulse (6 V, 65 nanoseconds) completes the forming process. This behavior may be used to emulate short-term memory on the microsecond scale. There are previous literature reports of similar behavior on a much slower scale in Ag_2S devices [13].

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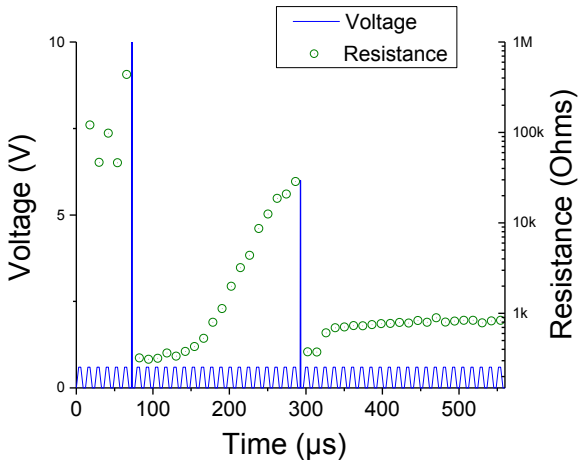

Fig. 9 A temporary electroform followed by a permanent one. The pulse sequence is 10 V, 100 nanoseconds followed by 6 V, 65 nanoseconds.

The resistance state of our devices may also be gradually increased or decreased, in a similar way to reports of the behavior of memristors using microsecond pulses of opposite polarity [14]. This may be used to emulate neuronal potentiation and depression. Fig. 10 demonstrates this behavior in our devices. The first four 6 V, 65 nanosecond pulses gradually bring the device towards a HRS. The following three 6 V, 65 nanosecond pulses (identical to the previous set of pulses) bring the device back into a LRS. Also in this case we expect the behavior to rely on impedance mismatch as well as pulses being too short for complete state changes to occur. The state of devices is read multiple times to ensure we either have expected stability or expected transient behavior. In the former case, this also provides higher quality readings. The number of read pulses is changed between programming pulses to ensure that the resistance trend is independent of these.

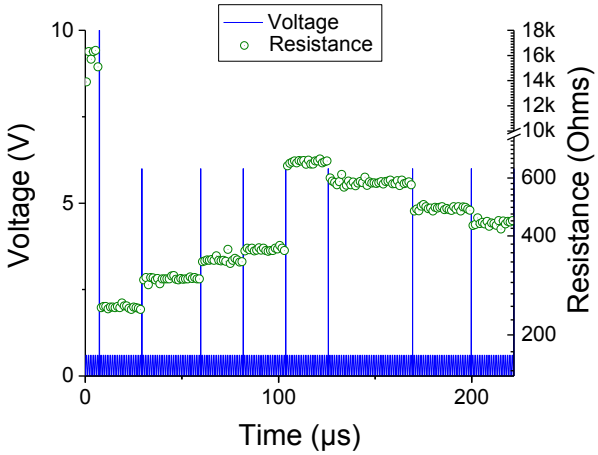

Fig. 10 Following a successful 10 V, 120 nanosecond electroforming pulse, identical 6 V, 65 nanosecond pulses were used to gradually bring the device into different resistance states. This demonstrates the possibility of potentiating and depressing a device using identical pulses. It is probable that impedance mismatch plays a role here, as well.

Fabrication process variation afflicts our experimental devices, making it hard to predict what exact pulse height and length are needed for an ideal forming process. Filament quality is therefore not fully predictable, despite clear repeatability. This issue will be addressed in our next generation of devices. Similarly, assuming that electroforming should be carried out at the foundry, complex programmers involving negative feedback could be employed to guarantee filament quality.

V. Conclusion

Here we have presented novel results in the field of intrinsic filamentary ReRAM. Our devices are simple, CMOS-compatible sub-stoichiometric TiN/SiO_x/TiN stacks that exhibit IV characteristics comparable to those found in the current research literature. Future work will concentrate on reducing operating voltages and currents, but at this stage we offer useful proof-of-principle results.

We have been able to directly track the electroforming process by exploiting dynamic impedance mismatches between the measurement system and the test device. This enabled us to confirm that electroforming occurs on the nanosecond timescale.

We also stimulated our devices with pulses whose durations were in the tens of nanoseconds range, without current compliance implemented. This resulted in remarkable behavior: it was possible to cycle devices between the HRS and LRS using identical pulses. By implementing a similarly simple pulse sequence, we also found that it was possible to obtain behavior that resembles the operation of neuronal synapses – specifically depression and potentiation. In this same context, we also observed short-term memory on the microsecond scale.

Taken together, our results confirm the nanosecond duration of electroforming and switching events, and suggest applications of SiO_x ReRAM devices in analogue and neuromorphic systems.

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From 2013 to 2015 he conducted research as part of the Resistive Switching group, University College London. From 2015 to 2016 he was a member of the Photonic Innovations Lab, University College London, and pursued his interest in experimental fabrication of self-assembled lithographic masks by means of colloidal lithography. His current research interests include development and improvement of semiconductor fabrication

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techniques as wells as implementation and testing of innovative measurement methodologies.

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