JÜLICH
FORSCHUNGSZENTRUM

Neuromorphic Systems

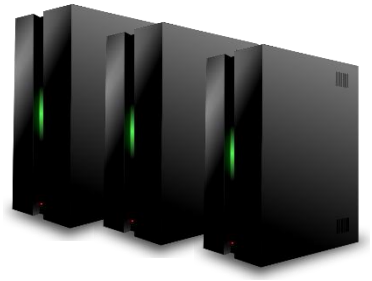
Running Neuron Models on SpiNNaker

13th December 2016 | Guido Trensch, Dimitri Plotnikov, Abigail Morrison (SimLab Neuroscience)

Interests in Neuromorphic Computing

- Large-scale simulations of the brain
  - Current technology is not well suited for large-scale parallel processing

~20 Watts



n MWatts

- Accelerated simulation of neural networks exceeding biological real-time
  - Bridge temporal scales
  - Traditional simulations are too slow for the study of plasticity and learning

- Brain-inspired computational solutions for practical applications

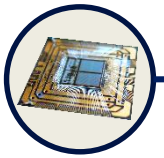
- Explore None-Von-Neumann architectures

Neuromorphic Systems Architecture

Architectural Strategy

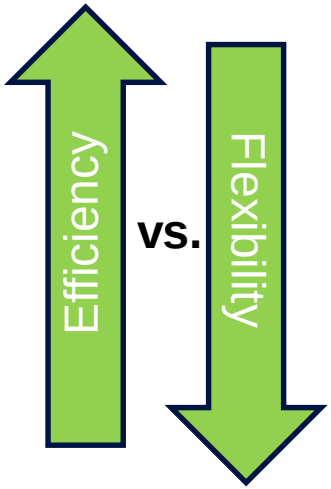
- Analog-digital mixed signal systems
- Fully digital systems
- Analog systems

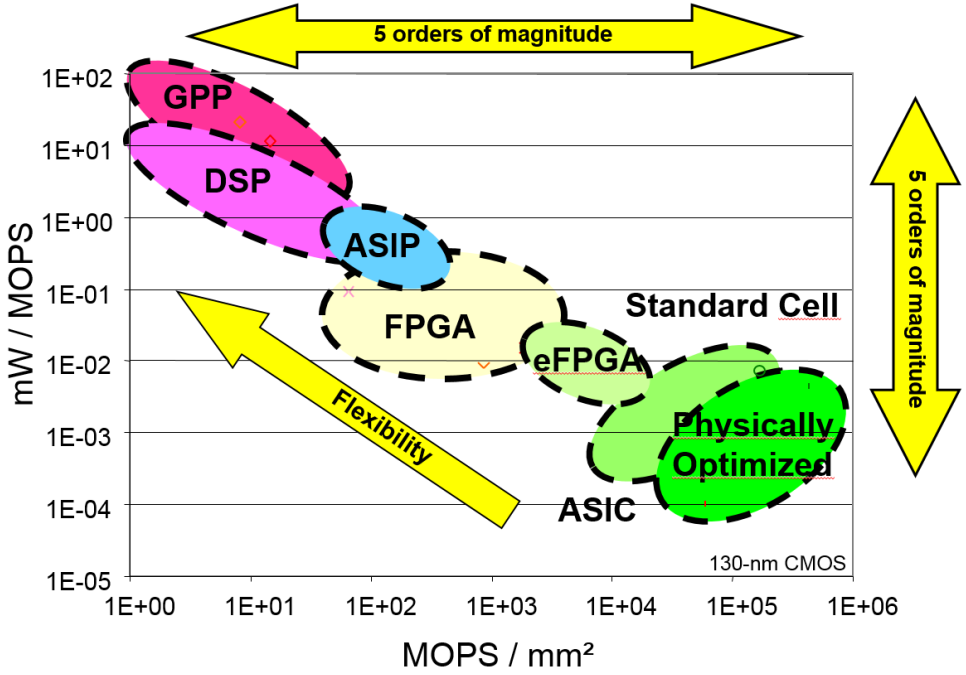
Neuromorphic Systems Architecture



Architectural Strategy

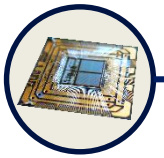
Circuit Design Space





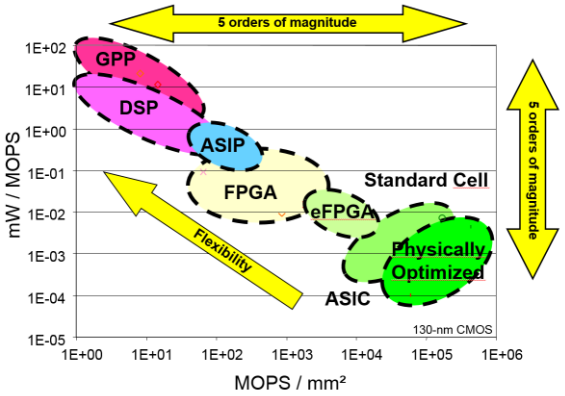
[adapded from M. Platzner et al. (eds.), Dynamically Reconfigurable Systems, Chapter 2.1, Tobias G. Noll et al.]

Neuromorphic Systems Architecture

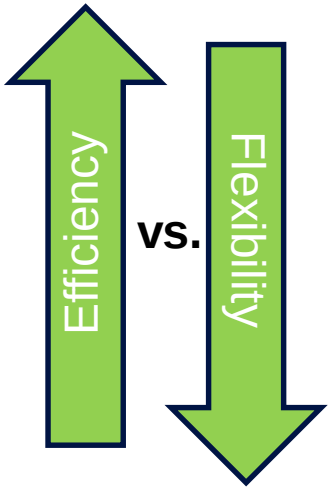


Architectural Strategy

Circuit Design Space



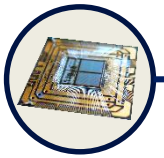
CONFLICT



- Custom chip
- Standard cell and application specific chip (ASIC)
- Field-programmable gate array (FPGA)
- Application specific instruction set processor (ASIP)
- Digital signal processor (DSP)
- General purpose processor (GPP)

[adapded from M. Platzner et al. (eds.), Dynamically Reconfigurable Systems, Chapter 2.1, Tobias G. Noll et al.]

Neuromorphic Systems Architecture



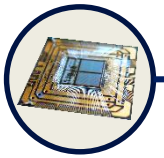
Architectural Strategy

Circuit Design Space

Neuromorphic circuit implementations

- Neuron circuits
- Synapse circuits
- Dendritec trees and axons
- Spike generators
- Spike distribution systems

Neuromorphic Systems Architecture



Architectural Strategy

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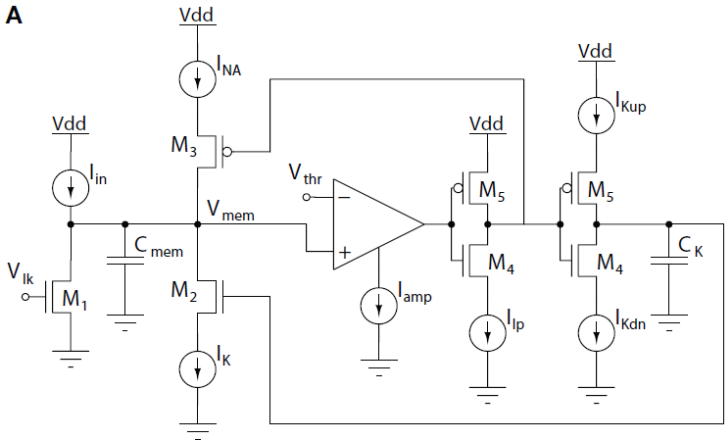
- Neuron circuits



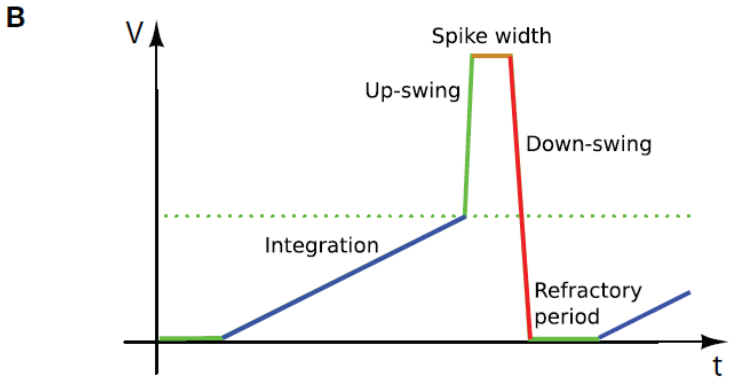
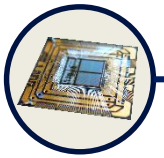


FIGURE 4 | Voltage-amplifier I&F neuron. (A) Schematic diagram; **(B)** Membrane voltage trace over time.

[Giacomo Indiveri et al., „Neuromorphic silicon circuits“, Frontiers in Neuroscience Volume 5]

Neuromorphic Systems Architecture



Architectural Strategy

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Neuromorphic circuit implementations

- Neuron circuits

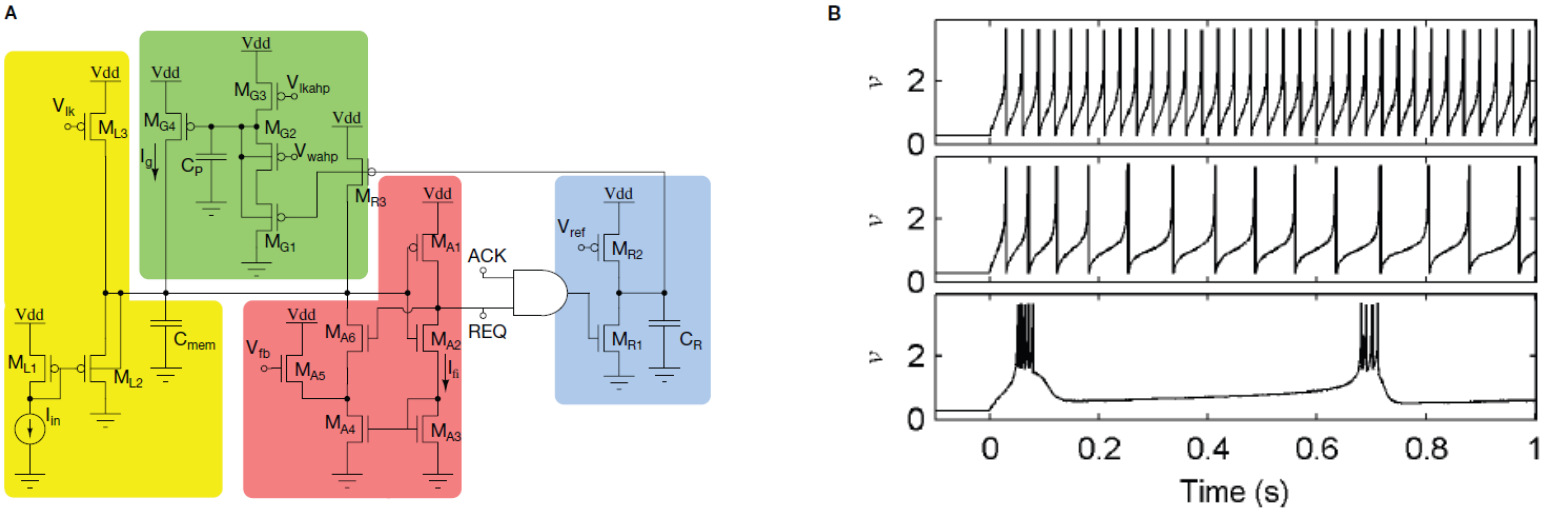
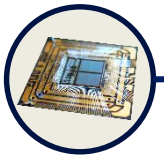


FIGURE 13 | The log-domain LPF neuron (LLN). (A) The LLN circuit comprises a membrane LPF (yellow, M_{L1-3}), a spike-event generation and positive-feedback element (red, M_{A1-6}), a reset-refractory pulse generator (blue, M_{R1-3}), and a spike-frequency adaptation LPF (green, M_{G1-4}). **(B)** Recorded and normalized traces from a LLN fabricated in 0.25 µm CMOS, exhibits regular spiking, spike-frequency adaptation, and bursting (top to bottom).

[Giacomo Indiveri et al., „Neuromorphic silicon circuits“, Frontiers in Neuroscience Volume 5]

Neuromorphic Systems Architecture



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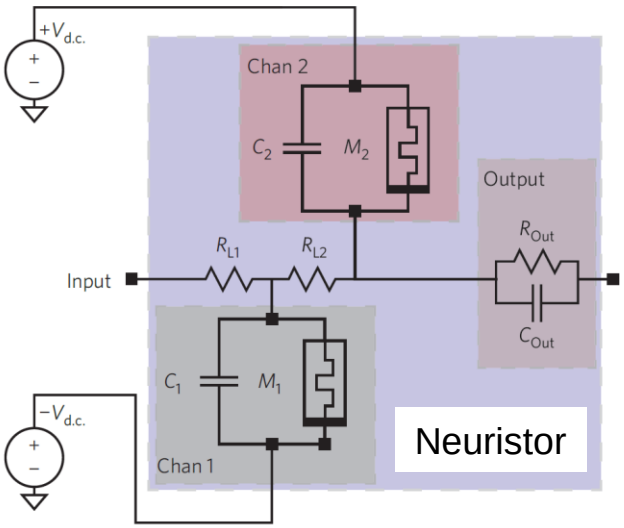
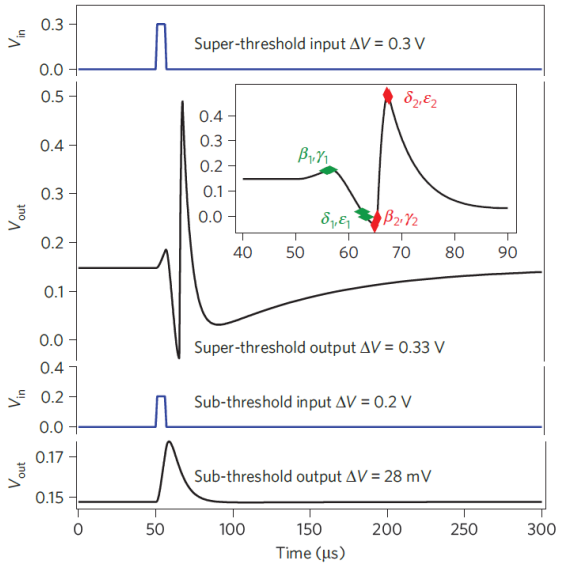
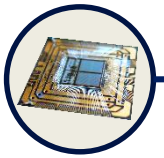
Hodgkin-Huxley model





[Matthew D. Pickett et al., „A scalable meuristor built with Mott memristors“, Nature Materials VOL12 (2013)]

Neuromorphic Systems Architecture



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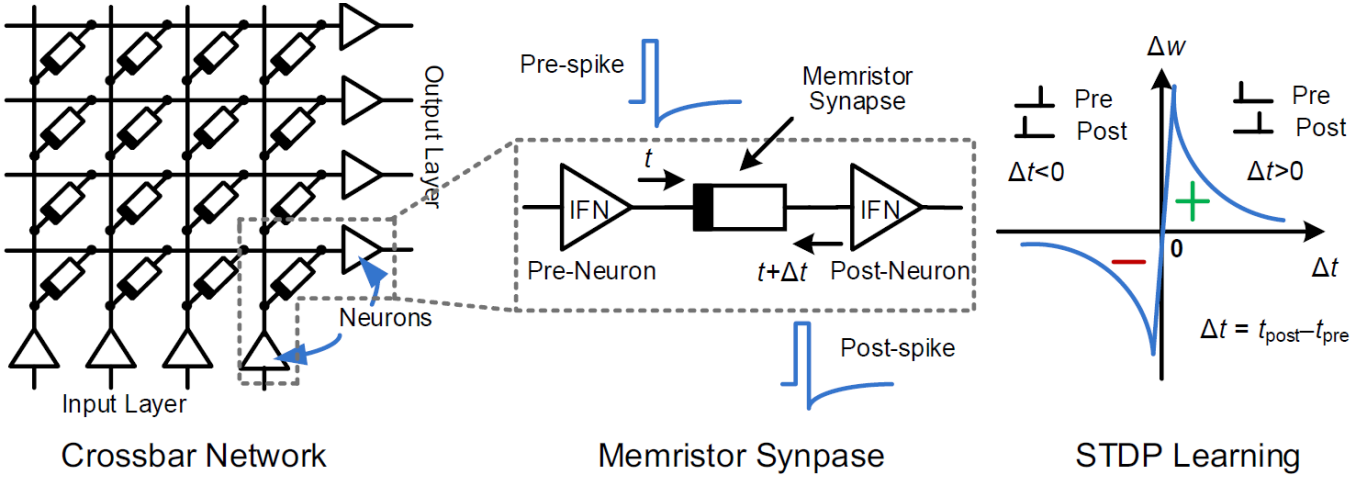
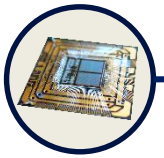


[Xinyu Wu et al., „A CMOS Spiking Neuron for Dense Memristor-Synapse Connectivity for Brain-Inspired Computing“, IJCNN (2015)]

Neuromorphic Systems Architecture



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- Neuron circuits

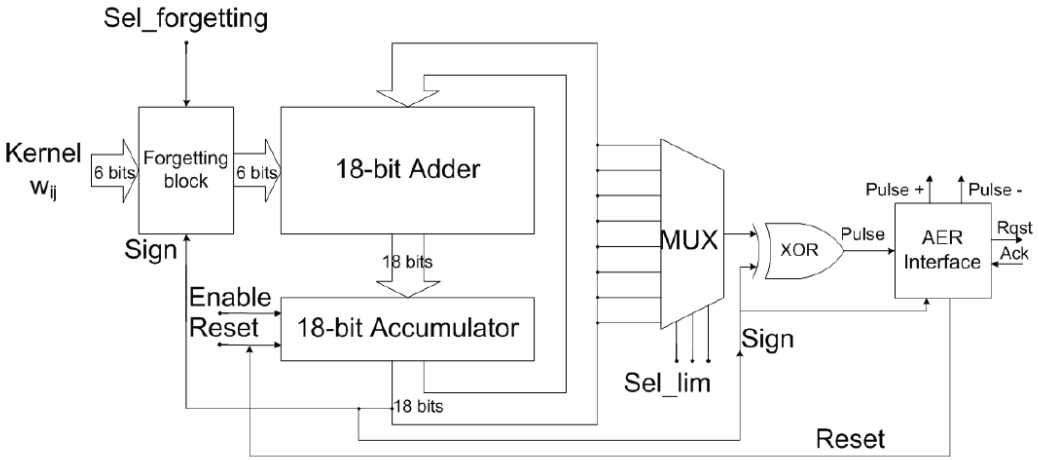
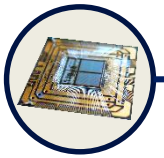


FIGURE 21 | Block diagram of a fully digital I&F neuron. Calibrated current source, pulsing current mirrors, and integration capacitors of **Figure 20**, are replaced by digital adder and accumulator circuits.

[Giacomo Indiveri et al., „Neuromorphic silicon circuits“, Frontiers in Neuroscience Volume 5]

Neuromorphic Systems Architecture



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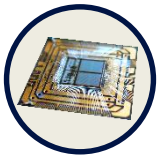
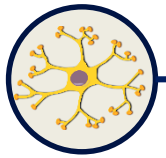


Neuromorphic
Systems Architecture

Neuroscientific Requirements



Feature richness

- Large variety of neuron types with different properties

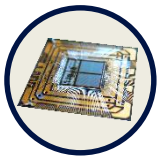
Flexibility and malleabitlity

Reproducibility and cross-validation of simulation results

Compatibility with existing tools

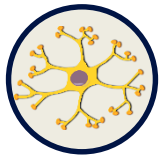
Ease of use for non hardware specialists

Neuromorphic system as research platform for neuroscience

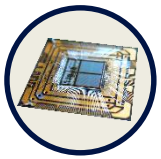


Neuromorphic
Systems Architecture

Neuroscientific Requirements

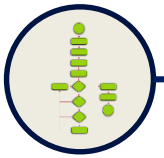


Biological & Computational
Neuroscience



Neuromorphic
Systems Architecture

Infrastructure & Services



Integration into existing HPC landscapes

Interactivity and visualization

Usability

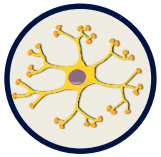
Co-design and technical standards

Software engineering

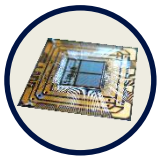
Community building and support

Methodologies and processes

… etc.

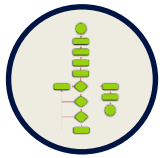


Biological & Computational Neuroscience

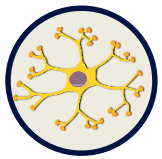


Neuromorphic Systems Architecture

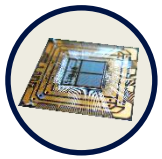
Infrastructure & Services



Infrastructure & Services

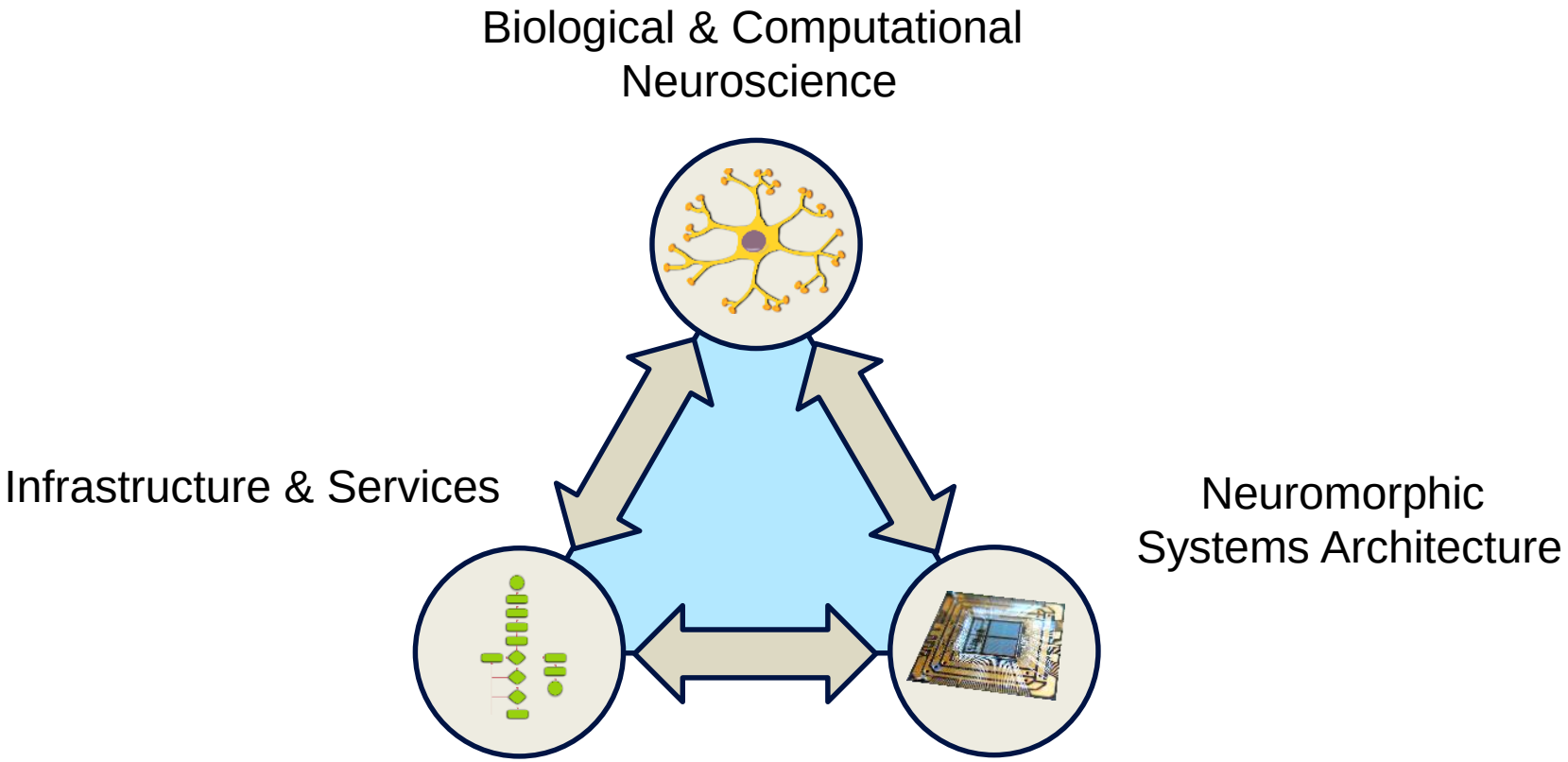


Biological & Computational Neuroscience



Neuromorphic Systems Architecture

Neuromorphic Systems



Neuromorphic Systems

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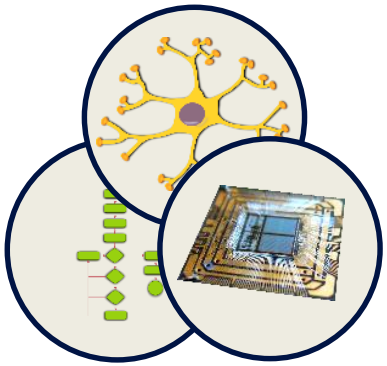
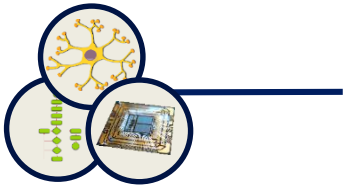


Infrastructure & Services

Neuromorphic Systems Architecture

Neuromorphic Systems



BrainScaleS

- Analog-digital mixed system
- Implements two neuron models
  - Adaptive exponential neuron model
  - Integrate & fire neuron model
- Two levels of plasticity
  - Short-term depression and facilitation
  - Spike time dependend plasticity (STDP)

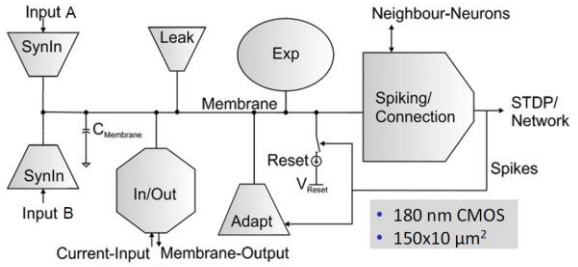


Fig. 1. Schematic diagram of the AdExp neuron circuit.

$$-C_{\mathrm{m}}\frac{dV}{dt} = g_{\mathrm{l}}(V-E_{\mathrm{l}}) - g_{\mathrm{l}}\,\Delta_{\mathrm{th}}\exp\left(\frac{V-V_{\mathrm{th}}}{\Delta_{\mathrm{th}}}\right) + g_{\mathrm{e}}(t)(V-E_{\mathrm{e}}) + g_{\mathrm{i}}(t)(V-E_{\mathrm{i}}) + w(t)$$

$$-\tau_w\frac{dw}{dt} = w(t) - a(V-E_{\mathrm{l}})$$

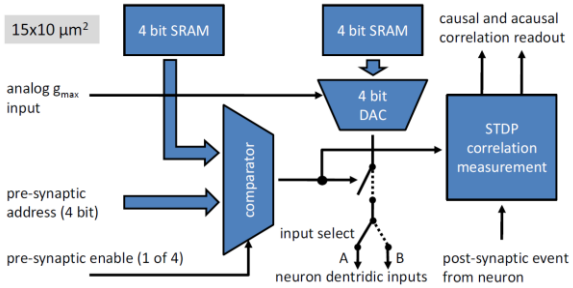
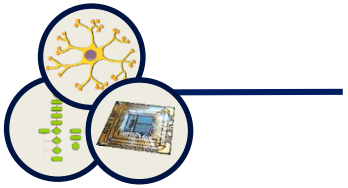


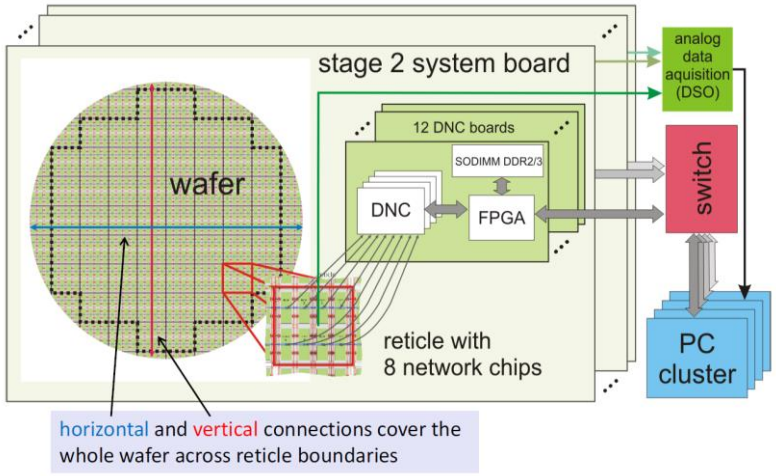
Fig. 4. Schematic diagram of a synapse.

[Schemmel et al., „A Wafer-Scale Neuromorphic Hardware System for Large-Scale Neural Modeling“ (2010)]

Neuromorphic Systems

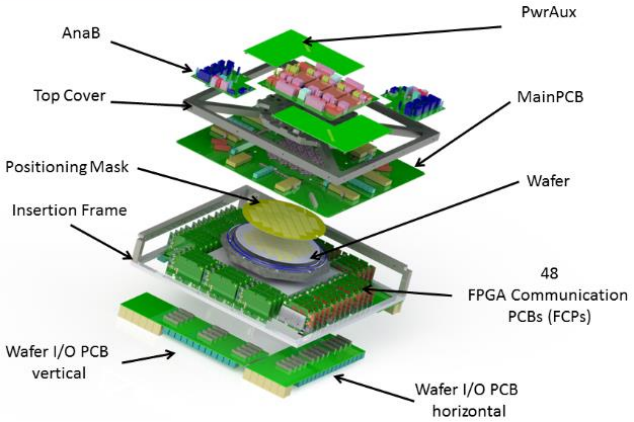


BrainScaleS



- Wafer-scale integration
- Inter-reticle connections

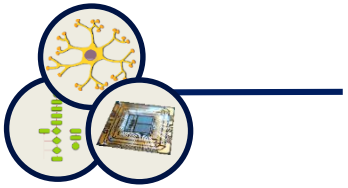
- Each wafer incorporates
  - ~200.000 neurons
  - 44 x 10^6 synapses



- 14336 pre-synaptic inputs per neuron possible
- Synapse weight is represented by a 4, 6, or 8 bit value

[Schemmel et al., „A Wafer-Scale Neuromorphic Hardware System for Large-Scale Neural Modeling“ (2010)]

Neuromorphic Systems



BrainScaleS

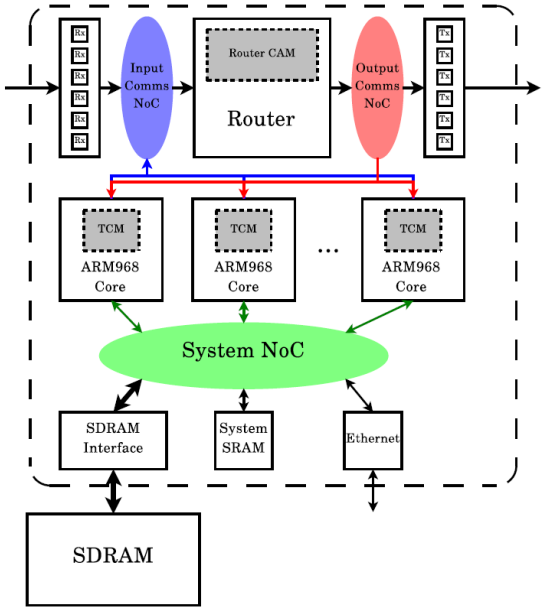
- 20 x 8-inch silicon wafers
- 4 million neurons
- Operates at accelerated biological real-time: 10^4 times faster
- Expected to stay below 1 KW/wafer

[Schemmel, „Wafer-Scale Integration of Analog Neural Networks”]

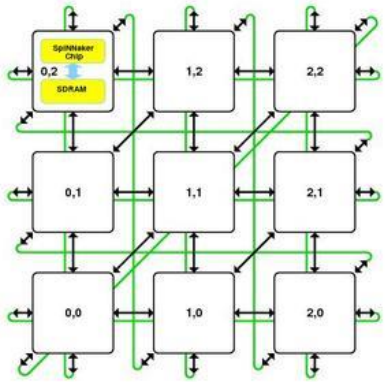
- PyNN API for simulator-independent specification of neuronal network models

[HBP Neuromorphic Platform, The BrainScaleS (NM-PM-1) system in Heidelberg on 30 March 2016]

Neuromorphic Systems

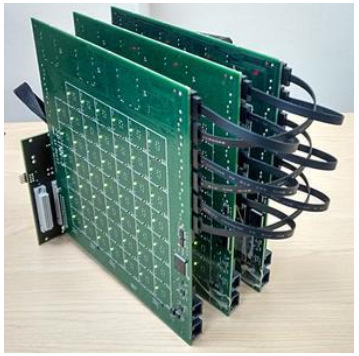


- Fully digital many-core system
- SpiNNaker chip
  - Energy efficient ARM968 processor core (~1 Watt/chip)
  - 32 Kbyte ITCM, 64 Kbyte DTCM
  - 128 Mbyte stitch-bonded SDRAM
  - Globally asynchronous locally synchronous (GALS) system with 16+2 ARM cores per chip
  - AER-based communication infrastructure
- Hexagonal mesh topology



[A. D. Rast, „The Leaky Integrate-and-Fire Neuron: A Platform for Synaptic Model Exploration on the SpiNNaker Chip]

Neuromorphic Systems



- Available hardware setups
  - Jörg Conradt‘s one-node board (TU München)
  - 4-chip board
  - 48-chip board
  - Stand-alone toroid

    (number of 48-node boards
    wired together as a single machine)
  - 600-board machine

[A. D. Rast, „The Leaky Integrate-and-Fire Neuron: A Platform for Synaptic Model Exploration on the SpiNNaker Chip]

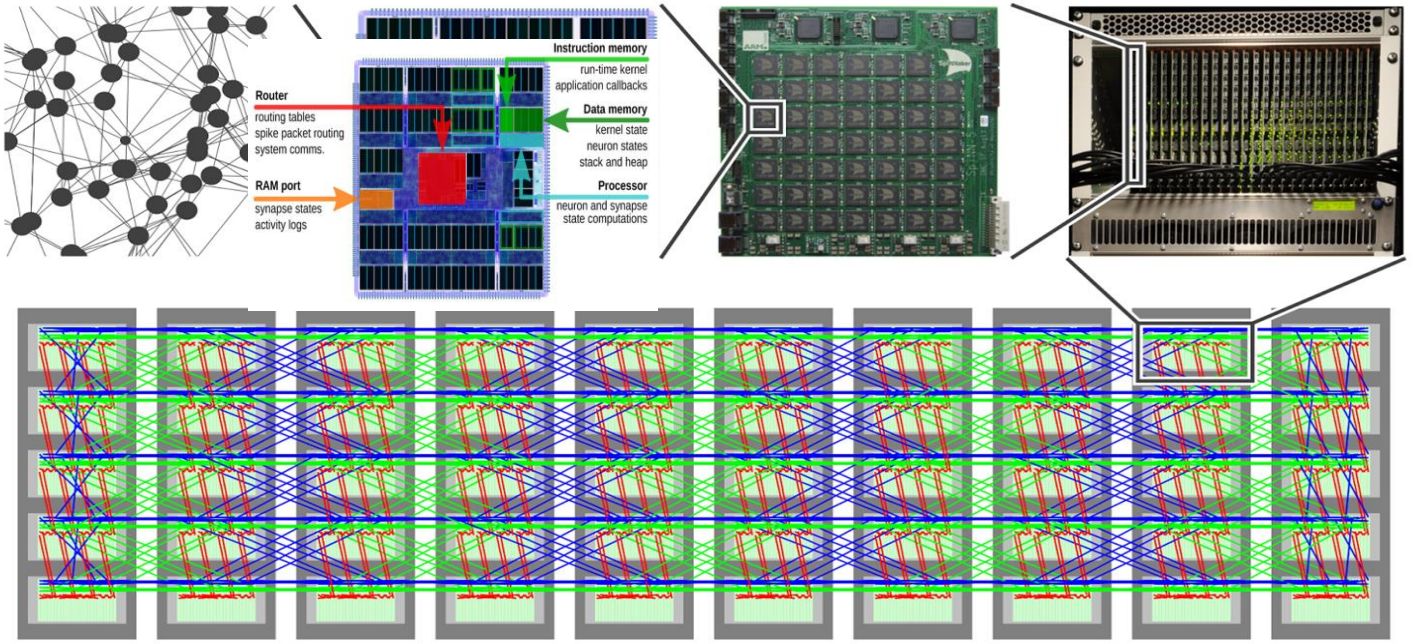
Neuromorphic Systems

1,000 neurons per core.

18 cores per chip.

48 chips per board.

24 boards per rack.



5 racks per cabinet, 10 cabinets.

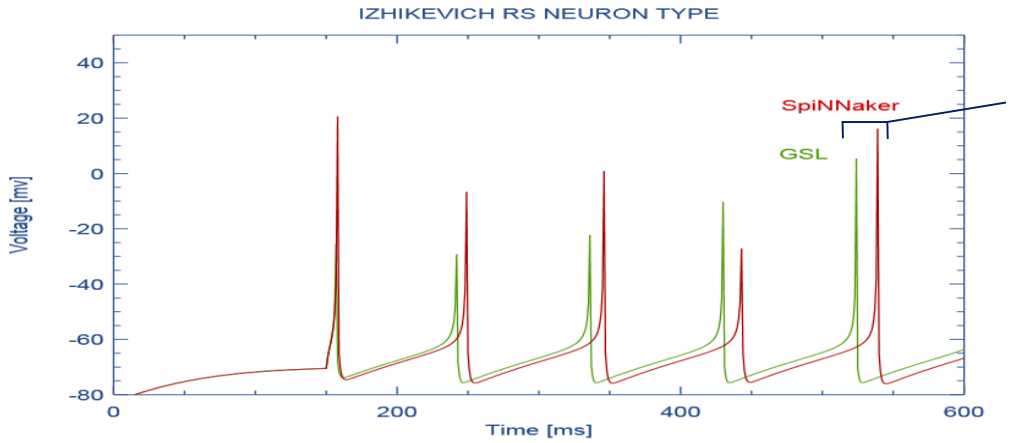
[SpiNNaker Project, APT research group, University of Manchester]

Neuromorphic Systems

- Biologically real-time simulation (1 ms resolution, adjustable)
- Targeting towards simulations of 1 billion neurons (1% of the human cortex)
- Software stack
  - PyNN API for simulator-independent specification of neuronal network models
  - 5 built-in neuron and synapse models (Current and conductance based leaky integrate & fire and Izhikevich models)
  - The software stack allows neuron models to be added.

Neuromorphic Systems

- Next generation SpiNNaker chip
  - 33 quad cores per chip
  - EXP, LOG and RNG build-in functions
  - Single precision FPU !
    - Current core has no FPU: 32Bit fixed point S16.15
      Simulation results might not be accurate and comparable



Fixed point math leads to shift in spike time

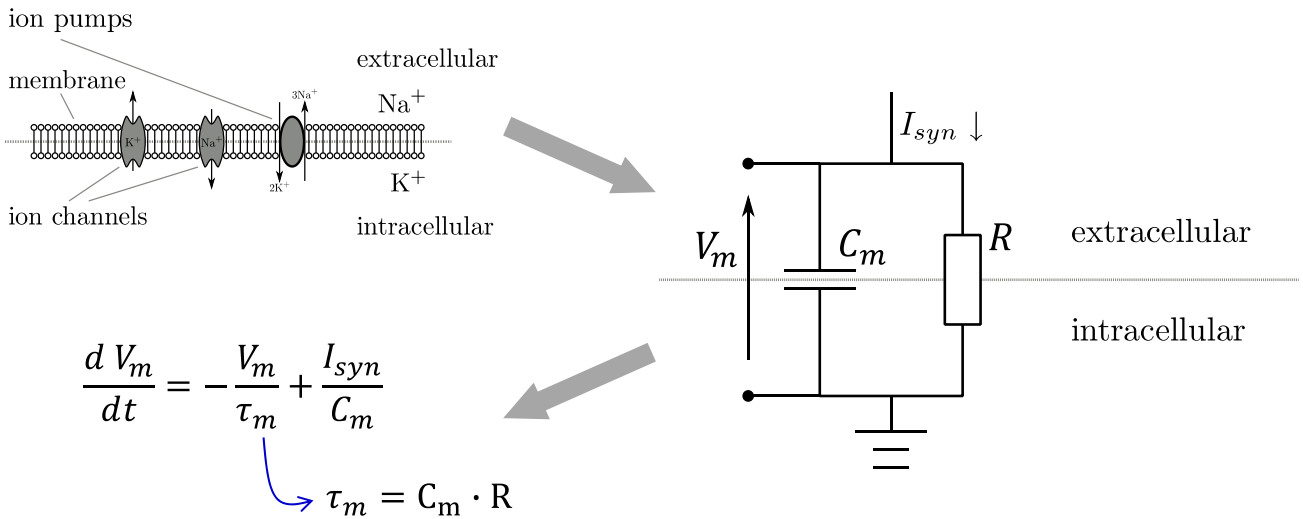
Modelling and Code Generation

Problem:

- Creating an application for the neuromorphic hardware requires expertise in a broad spectrum of disciplines.

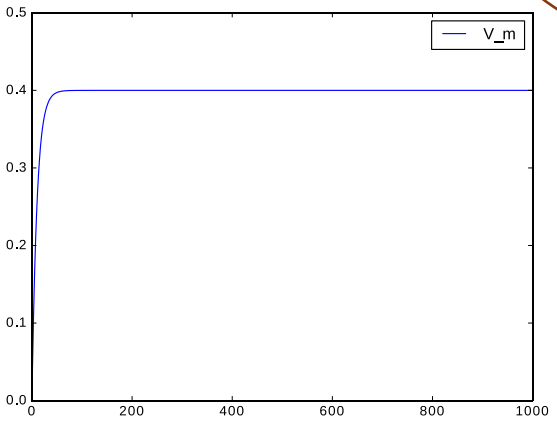
Solution:

- Create an abstract specification and use code generators to run the model.



Creating a Neuron Model with NESTML

$$\frac{d\,V_\mathrm{m}}{dt} = -\frac{V_\mathrm{m}}{\tau_\mathrm{m}} + \frac{I_\mathrm{syn}}{C_\mathrm{m}}$$



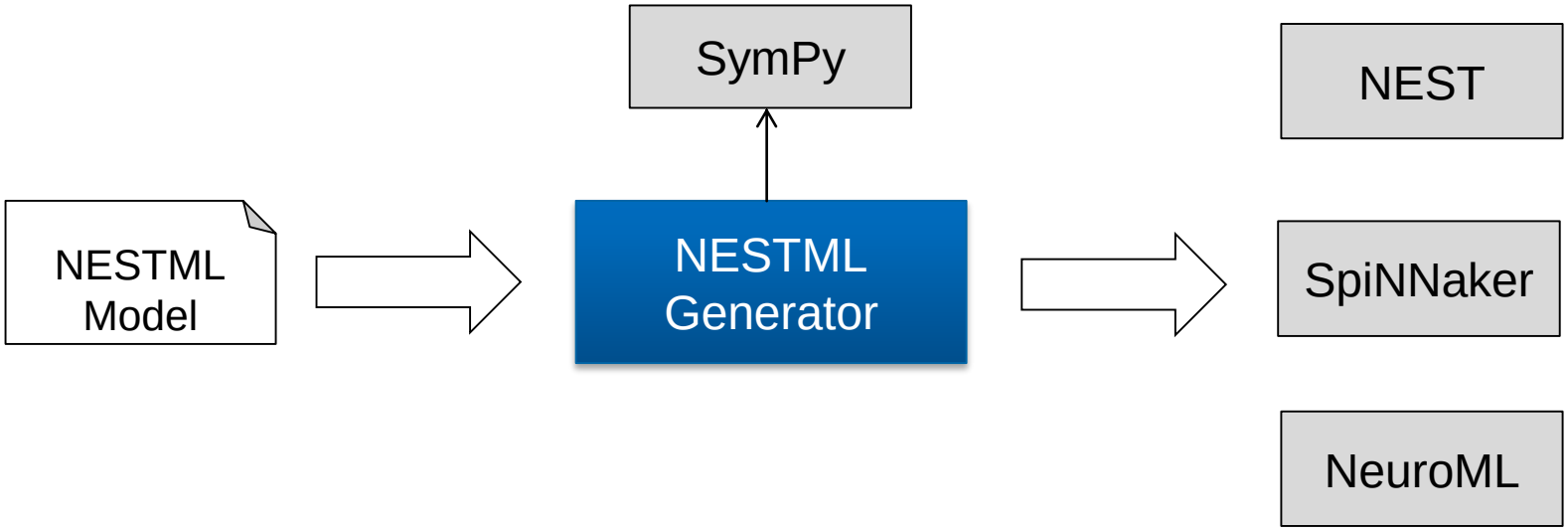

```
neuron rc_neuron:

  state:
    V_m mV = 0mV
  end

  equations:
    V_m' = -V_m/tau_m + I_syn/C_m
  end

  parameters:
    C_m pF   = 250pF
    tau_m ms = 10ms
    I_syn pA = 10pA
  end

  update:
    integrate_odes()
  end

end
```

D. Plotnikov et al., „NESTML: a modeling language for spiking neurons. “ (2016)]

Code Generators

The Code Generator captures the domain knowledge

- Instead of solving individual problems every time manifest the knowledge in a code generator.
- Use an abstract model capturing the model essence to create a portable neuron specification.



Questions ?