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Supercapacitor-based linear converter for voltage regulator modules

A thesis

submitted in fulfillment

of the requirements for the degree

of

Doctor of Philosophy in Electronic Engineering

at

The University of Waikato

by

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THE UNIVERSITY OF
WAIKATO
Te Whare Wānanga o Waikato

2016

Abstract

This thesis investigates a linear converter technique suitable for microprocessor voltage regulator modules (VRMs). The original linear regulator is the patented supercapacitor-assisted low-dropout regulator (SCALDO). A less complex, lower cost design was achieved by reducing the number of switches in the original SCALDO and adding a second low dropout regulator (LDO).

In the initial implementation of this reduced-switch SCALDO (RS-SCALDO), output regulation failed due to the presence of a parasitic body-diode in standard LDOs. The body-diode forms an unwanted discharge path to ground for the supercapacitor. In order to block this path, an application specific LDO that operates in the third quadrant of a MOSFET current-vs-voltage transfer function was investigated.

A 3.5-to-1.5 V RS-SCALDO was designed with a supercapacitor, two LDOs and two switches. Compared with the standard SCALDO approach, this new design halves the number of switches required. Discrete MOSFET-based high-current LDOs were developed and combined with a common feedback control circuit. Voltage identification (VID) capability was implemented using a digital potentiometer. Theoretically, when an LDO converts 3.5 V to 1.5 V a maximum efficiency of $1.5/3.5 \approx 43\%$ can be achieved. According to the general theory of SCALDO, a single supercapacitor configuration can achieve nearly twice the linear regulator efficiency. The 3.5-to-1.5 V, 5 A RS-SCALDO achieved an approximate end-to-end efficiency of 80%, thus, agreeing with SCALDO general theory.

Large-signal analysis was used to model MOSFET nonlinearities and predict the performance of LDOs, switches and the overall system. MATLAB modeling predictions for body-diode behaviour were cross-checked via SPICE simulation; the results agreed with bench measurements.

RS-SCALDO regulators cycle at very low frequencies, usually in the range of millihertz to hertz. Therefore, electromagnetic interference emitted by high-frequency switched-mode VRMs is not an issue here. Compared to typical high-frequency VRMs, RS-SCALDO topology provides similar efficiencies with the high slew-rate and low noise output of a linear regulator. In generalized SCALDO configuration with n supercapacitors, a total of $3n+1$ switches required; in contrast RS-SCALDO reduces the switch count to $2n$. With the elimination of the body-diode parasitics, the technique can be extended to much higher currents.

Preface

A brief history

Origin: Around 2007, Nihal Kularatna discovered a radically new DC–DC converter technique by combining a linear regulator with a supercapacitor (SC). A linear regulator connected to a DC-power source via an SC in series path works well for a limited time. With few simple experiments, Nihal found that the SC can charge in series while retaining the output voltage regulation for a couple of minutes. Then, after disconnecting the SC from DC-power source, he was able to discharge the SC to the linear regulator for certain time without degrading the output regulation. It was the very first idea to develop a low-frequency and high efficiency DC-DC converter with an SC.

Principle behind the original idea: Efficiency of a linear regulator increases as its input voltage decreases. Provided that the voltage-dropping element between the input power supply and the linear regulator does not waste energy, the end-to-end efficiency can be maintained at a high value. At the discharging phase, no power is delivered by the input supply; instead, excess stored energy of the SC delivers power to the regulator. This technique increases the overall energy efficiency. Nihal wanted to build a working circuit by appropriately automating the charge-discharge transitions of the SC.

Implementation of SCALDO and theoretical analysis: This idea was the basis for a *Jump-Start* project funded by *WaikatoLink* Ltd. in 2008. Jayathu Fernando built the practical prototype and it was patented as a *high-current voltage regulator* technique [1]. This technique opened up a major potential research area for high-current linear regulators. Standard linear regulators are usually rather inefficient, despite their excellent characteristics such as fast transient response, low noise, and simple circuit topologies. The new technique enables linear regulators to operate with higher efficiencies. An innovative linear power converter incorporating a commercially available high-efficiency low-dropout regulator was built to create the supercapacitor-assisted low dropout regulator (SCALDO).

Three converters were built for different input-output voltage combinations [2, 3]. SCALDO was then theoretically analyzed under a doctoral research project by Kosala

Kankanamge in 2010. The main conclusion of that research was "...the SCALDO approach is a viable solution that demonstrates a new approach to the design of DC-DC converters suitable for processor power supplies requiring high end-to-end efficiency" [4–7].

My thesis: In mid 2011, my research project initiated as the second phase of SCALDO. The task was to investigate a suitable topology of high-current linear converters for voltage regulator modules. A voltage regulator module (VRM) is a post-regulator to power noise-sensitive microprocessors in computer mother-boards. It should efficiently step-down voltage from a primary DC-source to processor core-voltage while maintaining a very tight output voltage tolerance at high-current transients.

SCALDO is inherently less complex than other regulator designs due to the simple operations required in charging and discharging the SC into the linear regulator. Since the load sees the clean output of the linear regulator, SCALDO has very low output noise. Although switches are required to change the SC between charge and discharge configurations, unlike conventional switch-mode converters, the switches do not contribute to the voltage conversion. These switches can cycle at very low-frequencies due to large SC capacity. Preliminary analyses of the original SCALDO circuit showed that, in order to apply this technique in VRM, static losses in the switches required to be minimized. The main aim of this project was to investigate the degree of effectiveness of SCALDO for implementing a new VRM topology, in terms of cost and efficiency.
The broad aim was subdivided to three objectives:

- Investigate design strategies to implement a VRM using supercapacitor based DC–DC conversion
- Implement a SCALDO-based proof-of-concept prototype for VRM that reduced system complexity while achieving higher performance
- Evaluate the VRM prototype with respect to efficiency and control loop functionality

Following list of specific tasks were to be performed in my project:

- Reduce number of switches
- Eliminate unwanted discharge in supercapacitors in the SCALDO circuit
- Implement a high current capable LDO
- Design a digitally controlled output voltage
- Improve control circuit for VRM implementation
- Build a proof-of-concept prototype of a SCALDO-based VRM

Contents overview

This research focuses on realization of a high-current linear regulator for VRMs. The basis for the new design was the compact single SC-based SCALDO configuration. Theory

related to the previously built 12-to-5 V and 5-to-2 V prototypes was used.

With providing a firm background and reviewing the essential basic theory in Chapters 1 and 2, I present my original work in Chapters 3, 4 and 5 and part of Chapter 2 also. These three chapters reflect the necessary sequence of events leading up to the achievement of the reduced-switch SCALDO (RS-SCALDO) design.

With the guidance of my Chief supervisor, a new and functional topology with reduced switch count was demonstrated. The new topology eliminates half of the switches required for SCALDO, but requires two separate LDOs for SC charging and discharging phases. This new approach is described in Chapters 3. Here I discuss development of an initial RS-SCALDO proof-of-concept prototype and describe its limitations.

I addressed the challenging MOSFET body-diode issue by designing an application specific LDO. This solution and its limitations are presented in Chapter 4. My second supervisor, Assoc. Prof. Alistair Steyn-Ross suggested the use of large signal modeling for the analysis of RS-SCALDO. LTSpice and MATLAB simulation results are compared with bench measurements to determine operational boundaries and expose challenges in a discrete-component-based design.

Chapter 1 provides a firm grounding in microprocessor power supplies, with an emphasis on SCALDO technique. In this chapter, I investigate DC-converter techniques to implement VRMs, and compare them based on the cost and complexity. Following an introduction to supercapacitor-based DC-DC conversion, the various converters are classified by primary features and SCALDO is positioned among the family of DC-DC converters.

Chapter 2 reviews basic physics and fundamental circuit equations for supercapacitor-based DC–DC converters that are applicable for the rest of the thesis: specifically, the electrical properties of supercapacitor for power applications and the basics of supercapacitor energy circulation. The general theory of SCALDO is reviewed and possible applications are summarized. After reviewing the SCALDO theory, I built theoretical relationships between circulation frequency and capacitance, and voltage of capacitor and equivalent resistance (ESR). Additionally, I designed a DC-UPS capable SCALDO for a lighting application, and a summary is presented with experiment results.

Chapter 3 explains the concept of topological transformation as a strategy to reduce the total number of switches in a SCALDO. Included in Chapter 3 are the RS-SCALDO concept, and design approaches to VRM. Further, specific flaws and limitations of an initial proof-of-concept prototype are presented.

In **Chapter 4**, I set specifications and design constraints for a 3.5-to-1.5 V, 5 A RS-SCALDO. Here, I present the bench measurements for the 3.5-to-1.5 V, 5 A RS-SCALDO topology, quantifying line regulation, load regulation, efficiency and transient response. The results were compared with the Intel specifications.

Chapter 5 reviews the basic physics of power-MOSFETs necessary for understanding the behaviour of MOSFET-based switches and LDOs. In each case, the circuit evaluations relate to specific design features in LDOs and switches. Furthermore, an implementation of digitally controlled output voltage capability is presented in this chapter.

Chapter 6 concludes the thesis by presenting opportunities for future work with recommendations. Details related to prototype, test-setup, the special equipment used in this research, and RS-SCALDO general theory are described in Appendices.

Original contributions

My original contributions include:

- A novel strategy to reduce number of switches
- A new design method to eliminate unwanted discharge in supercapacitors in the SCALDO circuit
- An implementation of high current capable LDOs
- A new design of a digitally controlled output voltage of an LDO
- Improvements to control circuit for VRM implementation
- An experimentally validated proof-of-concept prototype of a SCALDO-based VRM
- A design and implementation of DC-UPS capable SCALDO

The majority of the results in this thesis have been published in peer reviewed international conference publications and in a national conference. The proof of RS-SCALDO concept in Chapter 3 was published in International Symposium on Industrial Electronics conference ⟨1⟩. A solution to unwanted discharge in supercapacitors in the circuit was published in Industrial Electronics Society conference ⟨2⟩. In Applied Power Electronics conference, a very low dropout regulator with voltage identification (VID) capability and improvements to control circuit in Chapter 4 was published ⟨3⟩, and a poster was presented. A SCALDO converter with improved autonomy in Chapter 2 was presented in International conference on DC-Microgrids ⟨4⟩. The best student-presentation was awarded for the conceptual presentation of SCALDO and for the poster presentation ⟨5⟩ at the New Zealand Institute of Physics conference in 2015.

⟨1⟩ Nihal Kularatna, and Thilini Wickramasinghe. "Supercapacitor assisted low dropout regulators (SCALDO) with reduced switches: A new approach to high efficiency

VRM designs." *Industrial Electronics (ISIE), 2013 IEEE International Symposium on. IEEE*, 2013.

⟨2⟩ Thilini Wickramasinghe, Nihal Kularatna, and D. Alistair Steyn-Ross. "Reduced-switch SCALDO technique for high-current VRM implementation." *Industrial Electronics Society, IECON 2013-39th Annual Conference of the IEEE. IEEE*, 2013.

⟨3⟩ Thilini Wickramasinghe, Nihal Kularatna, and D. Alistair Steyn-Ross. "An extra-low-frequency RS-SCALDO technique: A new approach to design voltage regulator modules." *Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE. IEEE*, 2015.

⟨4⟩ Thilini Wickramasinghe, Nihal Kularatna, and D. Alistair Steyn-Ross. "Supercapacitor-based DC-DC converter technique for DC-microgrids with UPS capability." *DC Microgrids (ICDCM), 2015 IEEE First International Conference on. IEEE*, 2015.

⟨5⟩ Thilini Wickramasinghe, and D. Alistair Steyn-Ross, Nihal Kularatna. "Supercapacitor energy recovery technique to improve the efficiency of dc-to-dc converters" *2015, New Zealand Institute of Physics Conference*, 2015.

Acknowledgments

I am deeply grateful to all the people who helped me during my PhD journey. Without the support of others, it would not be possible for me to complete this thesis.

First and foremost, I would like to thank Assoc. Prof. Nihal Kularatna for offering me this research project and for his guidance over technical discussions. I would like to express my gratitude to my second supervisor Assoc. Prof. Alistair Steyn-Ross who has similarly contributed to guide me. He suggested to perform the large signal analysis for this research. It was very helpful not only during analysis, but also at the refining stage of the experiments. I am very grateful to both of them for the reviewing of my thesis with great care and attention, and for their invaluable comments and suggestions that contributed much to the improvement and completion of this thesis. I really appreciate their encouragement and patience during the difficult times of my journey.

I would like to thank the technical staff at the School of Engineering: Stewart Finlay, Ian Honey, David Nicholls, Benson Chang, Viking Zhou, and Peter Jarman for providing me and allowing me access to the resources. I would also like to acknowledge the administrative assistance received from Mary Dalbeth and Janine Williams of the School of Engineering.

My thanks go to librarian Cheryl Ward who has helped me in finding specific literature. It would not have been possible to meet the submission date of my thesis on time without the support of the scholarship office. Thank you to Gwenda Pennington for guiding me to find funds to complete this work. I would like to express my sincere gratitude to Dr. Sisira James, Leigh Utting, Andrea Haines, Anne Nicholas and Ruwan Gunaratna (from the Open university of Sri Lanka) for assisting me with the proof reading of this thesis.

Thank you to Dr. Dushanthy, Sujatha, Ajith, Charitha, Daminda, Layla, Akbar, Leigh, Graham and Liam for their generosity and encouragement. Thank you Gehan for helping me to print the soft-bound copies of the thesis. I would like to thank all my dear friends for the support given to me in many other ways during difficult times. Last but not least, words can not express my gratitude to my family and relatives for their support. Without their boundless love, I would never have had the strength to chase my dreams.

Dedication

I dedicate this thesis to all the people who believe in me, especially to my brother Chanaka, my parents Srimathie and Sene, my teachers and all my friends; without them, none of my success would have been possible.

Contents

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Acronyms and Abbreviations

AC	Alternating Current
ADC	Analog to Digital Converter
BJT	Bipolar Junction Transistor
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
DC	Direct Current
EDLC	Electrochemical Double Layer Capacitor
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
ETEE	End-to-End Efficiency
FET	Field Effect Transistor
IC	Integrated Circuit
IEEE	Institute of Electronics and Electrical Engineers
LDO	Low Dropout Regulator
MOSFET	Metal Oxide Semiconductor Filed Effect Transistor
NMOS	N-channel Metal Oxide Semiconductor
PCB	Printed Circuit Board
PIC	Peripheral Interface Controller
PMOS	P-channel Metal Oxide Semiconductor
POL	Point of Load
PSRR	Power Supply Rejection Ratio
PWM	Pulse Width Modulation
RFI	Radio Frequency Interference
RS-SCALDO	Reduced Switched SCALDO
SWC	Switch Capacitor
SCALDO	Supercapacitor Assisted Low Dropout Regulator
SMPS	Switched-Mode Power Supply
UPS	Interruptible Power Supply
VLSI	Very Large Scale Integrated Circuits
VRM	Voltage Regulator Module

Chapter 1

Investigation of DC-DC converters for VRM implementation

Over the last four decades—since 1975—integrated circuit designers have blended their engineering expertise with technological advantages to develop very large-scale integrated (VLSI) circuits into tiny chips. The microprocessor is such a design that become the brain of any smart electronic device. Due to the rapid development of new technologies and innovation of materials, the chip complexity, physical features, and operating requirements—voltage and power—have been scaled over time. The number of transistors on a microprocessor chip (processor) is increasing at an exponential rate that demands more current with significantly high-current slew rates due to fast processing functionalities. Therefore, low-voltage operation has become more attractive to reduce power consumption of the processor. A precisely controlled low-voltage is crucial for accuracy of processor operations. An additional power converter is required to step-down the voltage of the standard power supply to core voltage of the processor in a computer. These processor power converters are known as voltage regulator modules (VRMs).

The switch-mode power supply (SMPS) technique is used most commonly for the step-down conversion of VRMs [8, 9]. The size of bulky magnetic components in SMPS-based VRMs can be reduced by increasing the switching frequency [8, 10]. On the other hand, large number of buffer and filter capacitors have been utilized to handle load transients and high-frequency switch related noise [11, 12]. However, this can be achieved by compromising the real estate of the main-board (mother-board). Therefore, finding solutions for these issues has become an essential research areas under VRMs.

Efforts have been made to improve the existing SMPS technique [13–16] rather than looking for new options. The main reason is that, a similar high efficiency of a SMPS cannot be achieved with the use of a linear regulator or a switched capacitor (SWC) technique. Specifically, when the load demands high-currents and with large input to output differential voltages linear regulators and SWCs are inefficient and ineffective. However, it is evident that the ripples of output current and voltage, and the noise are ongoing issues of SMPS-based designs [17, 18].

Expanding this scope beyond SMPS techniques, a novel linear technique was developed around 2008. The new technique combines a high-efficiency low-dropout regulator (LDO) with supercapacitors [1, 2, 5, 6]. This supercapacitor-assisted low dropout regulator (SCALDO) illustrates candidacy for VRM.

A brief introduction to SCALDO is presented in this chapter with a background of processor power management. Furthermore, a fair comparison of switched-mode techniques (SMPS and switched-capacitors) with SCALDO is presented. Since, VRMs are step-down converters, this chapter includes only the step-down topologies. However, both step-down and step-up types of SWCs are briefly introduced to resolve the confusion between SWCs and SCALDOs.

1.1 Challenges of microprocessor power supply systems

A reliable and consistent power supply is a crucial requirement for any electrical system. Motivations for power management are to reduce: power wastage, noise, cost for energy and cooling systems. Reducing these factors improve the efficiency, reliability and economic viability.

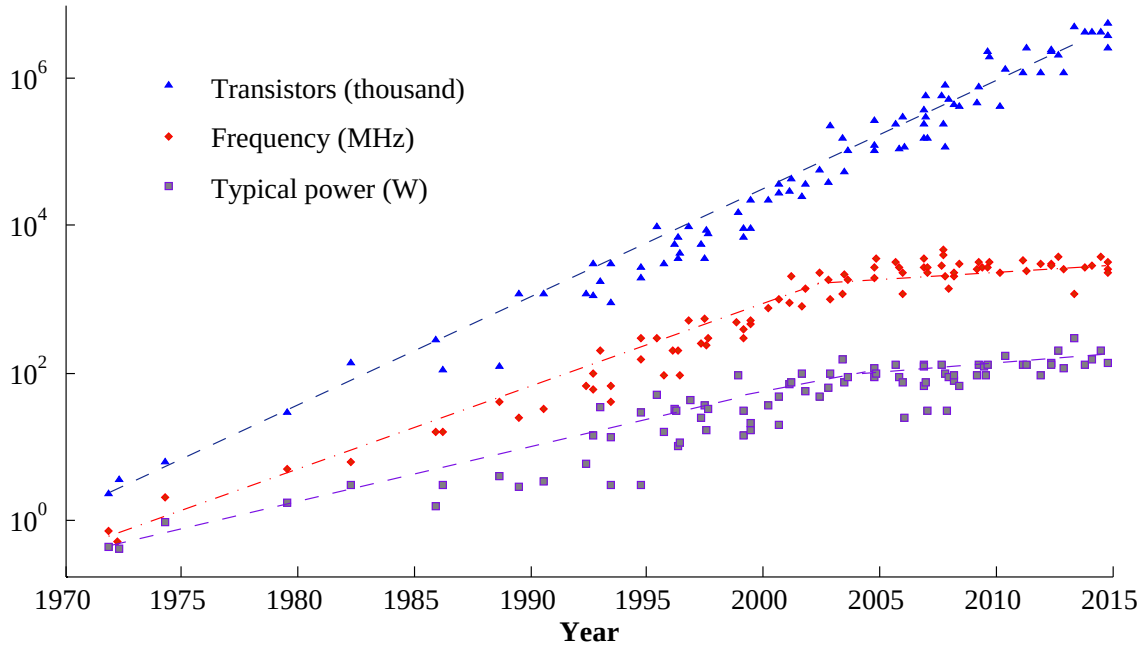


Figure 1.1: 40 years trend of parameters that challenge in designing processor power supplies; data extracted from [19]

In a computer system, microprocessor consumes more power than its peripherals. Fast technological trends become quite challenging for processor power supply designers to realize a high efficiency, low noise and low cost processor power supply. The technical trends in parameters which challenges in designing processor power supply units are illustrated in Fig. 1.1 and Fig. 1.2. They are summarized with their challenges as follows.

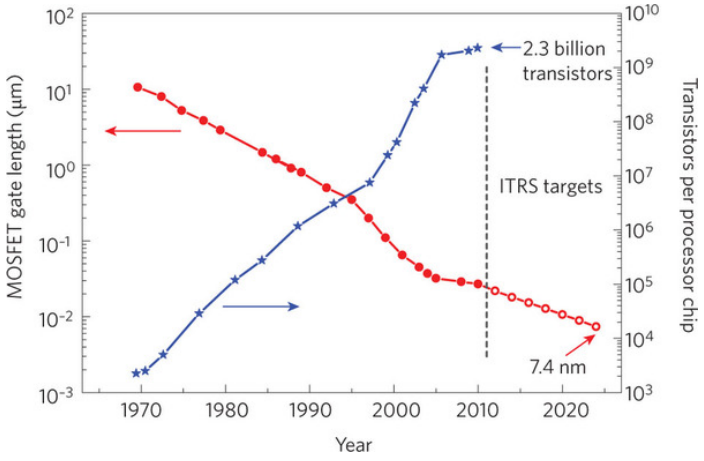
Number of transistors in the processor: Consistent with the predictions of Moores law, processor performance has improved continuously. The evolution of processing intensive applications in mobile and hand-held devices has largely been a matter of increasing the number of transistors per die. As illustrated in Fig. 1.1, from late 1990's the number of transistors in the processor has increased exponentially. By 2015, an Intel Core i7 processor has approximately 1.3×10^9 transistors [20]. With increase in transistor density of a fix-sized package minimizes the transistor size. Figure 1.2(a) depicts the transistor count trends per processor chip and the size in relation to gate length. Small sized transistors reduce the transistor gate length and improve speed of response. But they cause larger leakage current and increase the idle current of a device [19].

To power design engineers, the main challenge of power-hungry portable devices is to maintain longer work time between battery charges. Further to improve the efficiency of power modules of these miniaturized circuits dedicated power supplies placed very close to high-current demanding loads to reduce losses. At present this is managed by distributed power systems with two or more power supplies in series or point of load power supply from an unregulated rail [21].

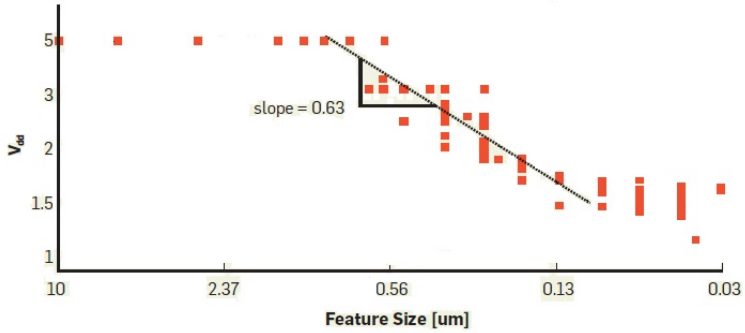
Power consumption: Due to the addition in transistor count, the current requirement for processors is increased; hence more power is required to operate these processors. Figure 1.1 typical power curve illustrates the changes in power demand of microprocessors for four decades. Early processors such as Pentium II consumed lower power of about 24 W. The processors introduced to the market around 2004, such as Intel Pentium 4 required around 84–115 W and they consumed about 120 A by 2006 [22, 23]. To control the amount of power consumed by the processor, the trend is to use power supplies with lower DC rail voltages.

Operating voltage: As the size of the transistors reduces, it is possible to reduce the operating voltage. Processor core voltage verses size of the transistor is illustrated in Fig. 1.2(b). As a result of reducing the voltage, power trend in Fig. 1.1 started to reduce. However, it was required to tighten the voltage tolerance from 5% for 3.3 V and to 2% for 1.3 V Pentium 4. The physical distance from standard computer power supply (silver-box) to processor was too far for fast delivery. Therefore, it required dedicated power supply units to power them. Initially separate modules were used to connect to a motherboard slot, therefore they were called voltage regulator module. Later they were built on the motherboard adjacent to the processor.

Processing speed: Around 1990s the processing speed of VLSI devices were scaled in Megahertz. After 2000, the scale had advanced to Gigahertz [24]. For example, the



(a)



(b)

Figure 1.2: Transistor properties and processor core voltage: (a) Transistor per processor chip and FET gate length, (b) feature size vs maximum voltage [19]

Pentium Pro processors manufactured in 1996 were running at 200 MHz [25]. From 2006 to 2009, the new Pentium processor speed had advanced from 1.3 GHz to 2.6 GHz [25,26].

As a result of increment in processing speed, processors present very dynamic loads with fast current slew rates. In recent years, the microprocessor voltage-regulator specifications from Intel and AMD present load current slew rates of 50 A/μs to 200 A/μs and peak currents from 60 A to more than 120 A [22]. Voltage regulation at a precise level is crucial for these sensitive high density devices [27,28].

In future, the processor voltage will be much lower than 1 V while demand on the load current and current slew rate are increasing continuously. A lower supply voltage can cause control challenges, introduce sensitivity limitations, and reduce overall system efficiency [29]. This represents a significant challenge to design processor power supply as controlling a very low voltage with high-current transients is technically difficult. One of the main challenges for engineers is designing a topology to improve the efficiency of

DC power conversion for these power-hungry devices.

1.2 Technology trends and processor power architecture

A typical first generation computer power supply had +5 and +12 V output voltages; and two other voltages, −5 and −12 V. This generation of computers used +5 V to power the processor while other voltages were used for the rest. At the early stage of computers conversion of AC-DC and DC-DC were developed separately as in Fig. 1.3(a). With emergence of smaller components the AC-DC power supplies were built into circuit level.

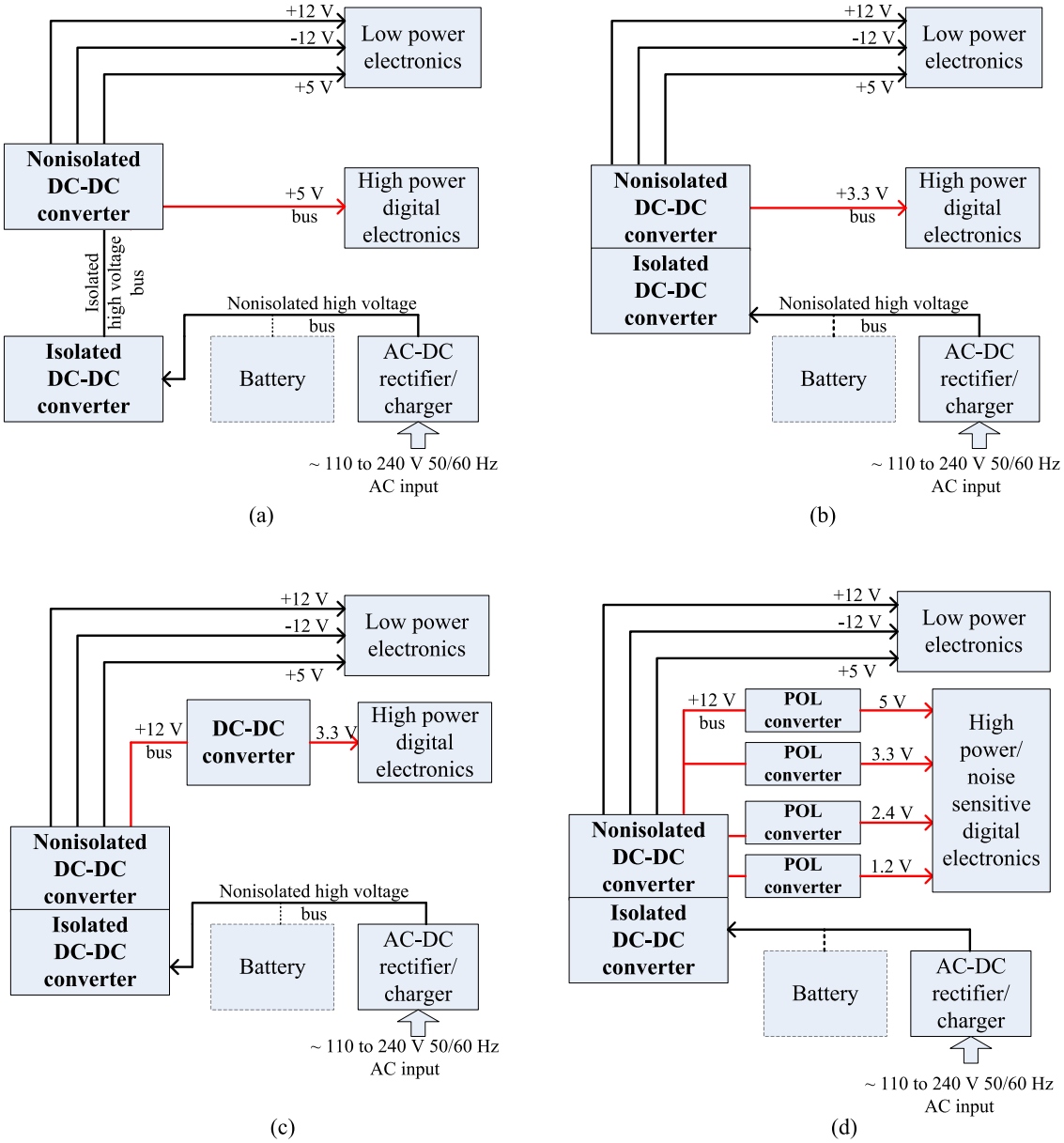


Figure 1.3: Evolution of a generalized computer power supply architecture: (a) first generation computer power supplies; processor powered by 5 V, (b) integrated modules; processor powered by 3.3 V rail, (c) first generation of VRM, (d) point of load converter architecture

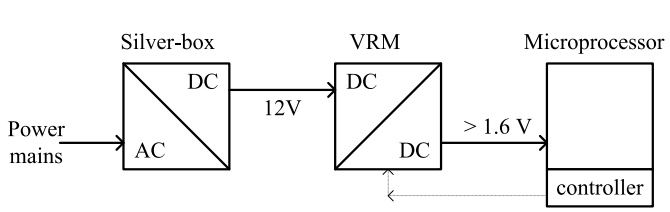
Later, a single module with AC-DC and DC-DC, and separate point of load solution architecture was emerged. Figure 1.3(b) illustrates a single Advanced Technology eXtended (ATX) power supply provides several different power outputs known as rails running at a variety of voltages (namely 3.3 V, 5 V and 12 V). Due to the increase in processor current requirements 3.3 V rail was used to reduce the total power consumption. This type of centralized power supplies were used to power single processor based systems. They were sufficient to provide all the power requirements of a processor, memory chip, video card and other peripherals of the computer.

Then, the speed of the processor increased exponentially at the expense of energy consumption. Graphic and voice data processing applications required more powerful processors so they required more power. A special DC-DC converter was required to satisfy the need of the processor. This was the first dedicated voltage regulator architecture which is introduced in computer systems; illustrated in Fig. 1.3(c). It converted 12 V rail voltage to 3.3 V processor voltage.

The operating voltage of electronic devices can be reduced due to the reduction of transistor size. However, high power devices had become sensitive and required precisely controlled voltages. The point-of-load (POL) architecture was the ultimate solution for these noise sensitive loads; illustrated in Fig. 1.3(d).

1.3 A general model of VRM and requirements specification

Typically a VRM is a step-down DC-DC converter, with external interconnections providing power to a microprocessor circuit. A VRM performs DC-DC conversion while providing a very low constant DC output voltage under a large current demand on the load side, with higher current slew rates [12]. A general model of a VRM and its specifications is seen in Fig.1.4.



(a)

Circuit parameter	Value
Output voltage	< 1.5 V
Output voltage tolerance	> 2%
Load current	> 150 A
Current slew rate	> 0.5 A/ns
Efficiency	> 90%

(b)

Figure 1.4: A general model of VRM and requirements specification: (a) a typical configuration of VRM in a desktop computer, (b) basic parameters and their values of future VRMs [8, 27]

A general VRM model can be represented with three basic blocks: the input power supply, the VRM and its load (microprocessor). Typically, the power source for the VRM

is 12 V rail of the computer power supply. VRM converts 12 V to lower voltages of microprocessor. In modern computer systems, processor send digital signals to control the voltage regulating circuit [30–33], which is briefly discussed in Appendix B. Most common implementations of voltage identification (VID) capability in SMPS-based VRM use a digitally programmed resistive ladder and a digital pulse-width-modulator. Delays in the output sensing signals (analog to digital conversion) correspond to phase shifts that may degrade loop response. This is a technical challenge for the new generation processors with fast transients [30, 31].

1.4 Choice of an efficient converter technique for VRM

One of the most discussed areas in literature and industry related to DC-power supplies is the linear and switch mode power supplies. They are the most basic technologies used for any new design. As mentioned at the beginning of the chapter, there are three fundamental techniques to achieve DC-DC voltage conversion: linear, SWC and SMPS. Each of these techniques has its specific benefits and limitations that depend on application requirements and their own specifications. Some specifications are the voltage conversion ratio range, the maximum output power, power conversion efficiency, number of components, and power density [34]. These specifications generally remain relevant, nevertheless some of them will be prominent when more restrictions in application requirements are vital. For instance when they are to be designed in monolithic integrated circuit version, the available chip area will be dominant for the production cost, limiting the value and quality factor of the passive components [34]. These limited values will in-turn have a significant impact upon the choice of the conversion technique.

VRMs power conversion efficiency is one of the primary concern to reduce losses. A formal and a fair comparison of DC-DC step-down converters, in terms of power conversion efficiency, are used in following section. Furthermore general topology is also discuss here.

1.4.1 Switch-mode approach for VRM

The basic operation of SMPS is based on commuting energy between the source, the inductor, and the output capacitor to power the load. SMPSs can convert a DC input voltage into a different DC output voltage, depending on the circuit topology. There are many SMPS topologies, which are classified into fundamental categorization power supplies step-down (buck), step-up (boost), invert, and step-up and down (buck-boost). This section presents only the buck converter as other types are not suitable for VRMs. A fundamental topology that is illustrated in Fig. 1.5 includes a MOSFET switch (SW), a diode (free-wheeling) (D), an output capacitor (C), and an inductor (L). The MOSFET switch is interfaced to a controller which generates a switching signal and actively controls

the operation [35]. This controller applies a pulse-width-modulated (PWM) square wave signal to the MOSFET gate to ON and OFF. To maintain a constant output voltage, the controller senses the output voltage V_{out} and varies the ON time t_{on} of the square-wave signal. This defines a duty ratio D dictating how long the MOSFET is on during each switching period (T). D is

$$D = \frac{t_{\text{on}}}{t_{\text{on}} + t_{\text{off}}} = \frac{t_{\text{on}}}{T} \tag{1.1}$$

where t_{off} is the OFF-time of the switching period. Duty ratio directly affects the voltage observed at the SMPS output. During each switching cycle, the inductor stores energy from source and releases the energy to load.
The efficiency of the buck converter is

$$\eta = \frac{V_{\text{out}} I_{\text{out}}}{V_{\text{in}} I_{\text{in}}} = \frac{D I_{\text{out}}}{I_{\text{in}}} \tag{1.2}$$

Buck converters have high-efficiency of 95% or higher for integrated circuits, making them useful for applications such as converting the 12 V rail voltage in a desktop computer power supply (or 12 or 24 V in a laptop) down to the processor core voltage 0.8-1.8 V.

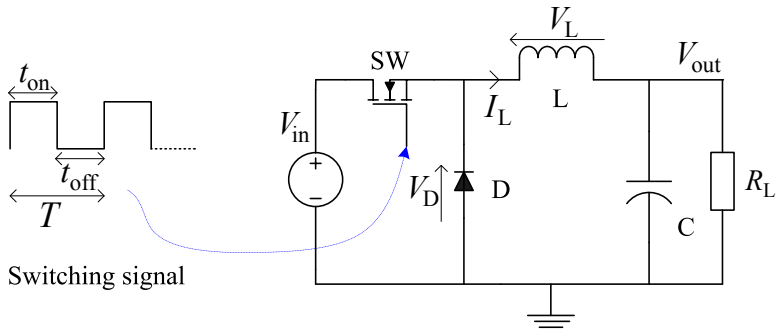


Figure 1.5: Simplified diagram of buck converter circuit with the switching signal

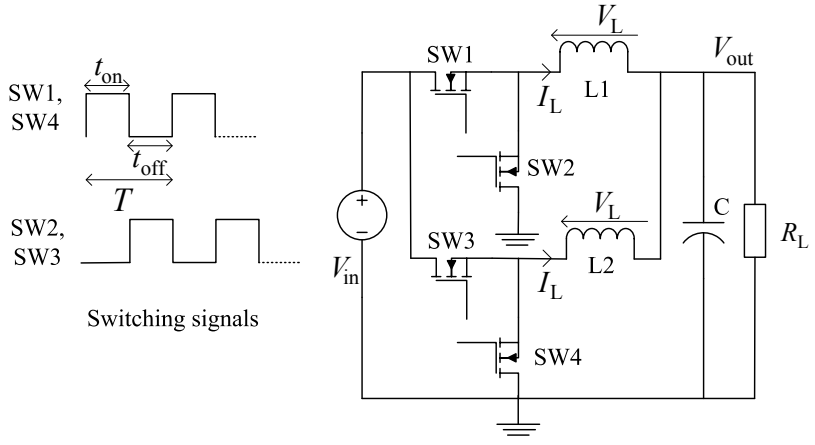


Figure 1.6: Multiphase buck converter with two phases: a simplified equivalent circuit with the switching signals

The noise in SMPS is a primary issue when utilizing them in sensitive loads [36]. It is mainly due to the high switching frequency that generates electromagnetic radiation. Rapidly changing voltages at the inductor node cause radiated electric fields, while fast-switching currents of the charge-discharge cycle produce magnetic fields. This noise propagates to input and output circuits [37].

One of the solutions to reduce the switching frequency is the multiphase buck converter [38, 39]. It is a circuit topology where basic buck converters are placed in parallel between the input and the load. It can have n number of phases. The main advantage of these buck converters is the significant decrease in output ripple. The load current is split among the n phases and there is less stress on a single element.

Figure 1.6 illustrates multiphase buck converter with two phases. Each of the two phases is turned on at equally spaced intervals over the switching period. This type of converter can respond to load changes as quickly as if it switched 2 times faster, without the increase in switching losses that it would cause. Thus, it can respond to rapidly changing loads, such as modern microprocessors. Typically, this circuit topology is used in VRMs to convert the 12 V to a lower core voltage of CPUs where a typical motherboard power supply uses 3 or 4 phases [12].

One major challenge inherent in the multiphase converter is ensuring the load current is balanced evenly across the n phases. Some load balancing techniques are technically challenging due to the switching noise and expensive than to sense resistor for each phase [40, 41].

In synopsis, though the SMPS are efficient compared to a linear DC-DC converter, the output noise and complexity in a SMPS topology are higher and cannot easily be reduced.

1.4.2 Evolution of SMPS-based VRM topologies

SMPS have become popular as they are highly efficient in step-down DC-DC conversion. The conventional model of buck circuit is the most cost-effective design approach for VRM. However, with the changes to processor power supply specifications, the basic SMPS buck (step-down DC-DC) converter topology will not be sufficient to meet the new specifications.

The first generation of VRM was developed for the Pentium II processor. It was too slow to respond to power demand of later versions of microprocessors such as Pentium III and Pentium 4. Therefore, a large number of capacitors had to be placed adjacent to the microprocessor in order to transfer power promptly. However, this approach was costly and bulky because of the large number of capacitors and the complex control circuit. Conventional controller operations of VRM were based on the output ripple voltage or

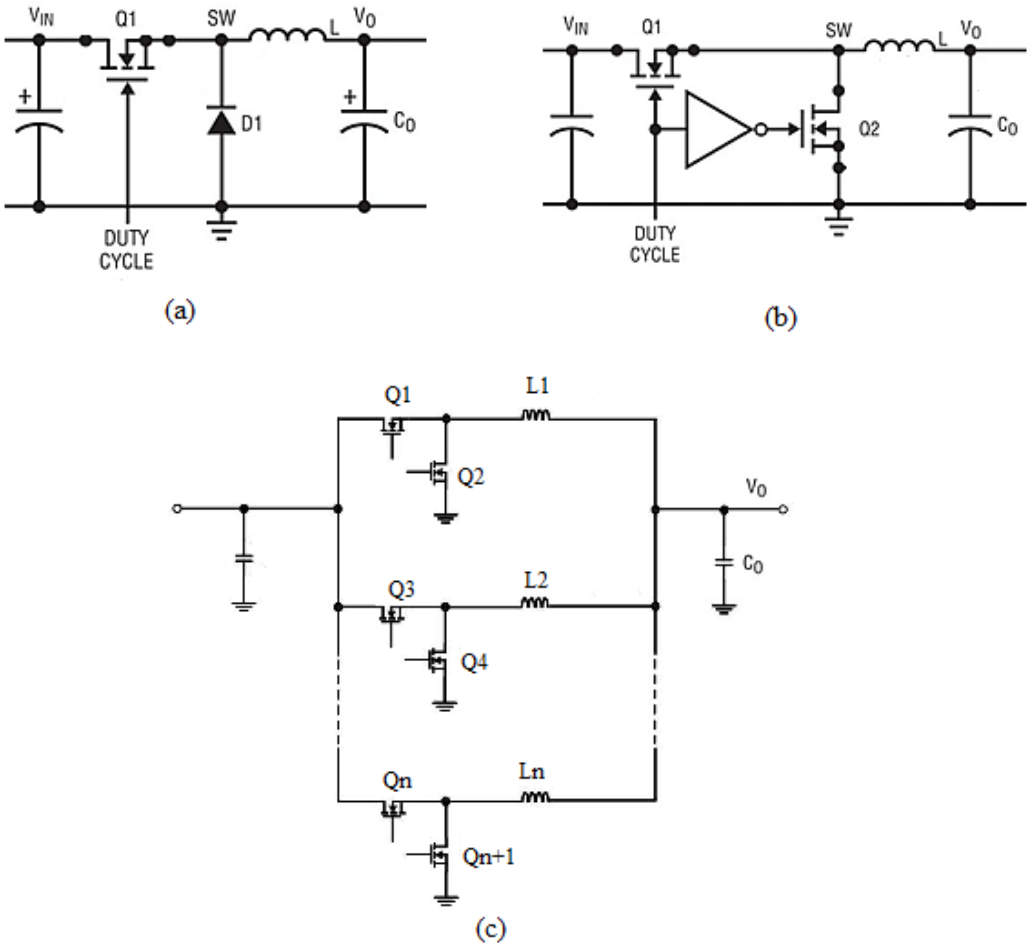


Figure 1.7: Basic VRM topologies: (a) conventional buck converter, (b) synchronous rectifier buck, (c) multiphase buck converter [8]

the inductance current. Since inductor current of a ripple-based controller lags behind the load current, capacitor-based controller topologies were proposed [42].

Most of today's VRMs use conventional buck topology or synchronous rectifier buck topology with different configurations. Their basic topologies are referred to in Figs. 1.7(a) and (b) respectively. To achieve the manufacturers objectives of high power density, high efficiency and fast transient response of VRMs, many different research approaches for VRM topologies have been presented [13, 14, 28, 43]. Even though the synchronous buck converter is a more popular VRM topology, the magnitude of voltage drop is high at the switch turn off mode. Further, the passive LC components (i.e. inductors and capacitors) used for filtering purposes occupy a large area of the board. Cost increased significantly and the real estate of the motherboard was not enough. Switching related losses in power semiconductors, inductor losses and the equivalent series resistance (ESR) losses in output capacitors are significant issues with this converter technology at high frequency operations [44]. The main losses in buck converters are (i) static, (ii) dynamic, and (iii) control circuit components. See Table 1.1. Static losses increase with the current flow, while dynamic losses increase with switching frequency f_{sw}. The control circuit of a

buck regulator consists of a feedback loop with a comparator, oscillator, integrator and a triangular-to-pulse generator. Compared to a linear regulator which has a feedback loop with an error amplifier, a buck control circuit needs to energize more components.

Table 1.1: Power losses in buck converters

Static		Dynamic		Control circuit
ESR	I^2R_{ESR}	Switch turn-on and turn-off	$[IV_{\mathrm{sw}}(t_{\mathrm{rise}}+t_{\mathrm{fall}})f_{\mathrm{sw}}]/2$	Feedback loop with comparator
ESL	I^2R_{ESL}	Body diode/diode	$IV_{\mathrm{D}}t_{\mathrm{on}}f_{\mathrm{sw}}$	Oscillator
Core	I^2R_{core}	Gate driver	$Q_{\mathrm{G}}V_{\mathrm{GS}}f_{\mathrm{sw}}$	Integrator
Switch resistance	I^2R_{sw}			Triangular-to-pulse generator
Diode	$V_{\mathrm{D}}I$			

R_{ESR} - equivalent series resistance, R_{ESL} - equivalent series inductance
R_{sw} - ON resistance, V_{D} - diode forward voltage
V_{sw} - voltage drop across the switch, V_{GS} - gate to source voltage
t_{rise} - rise time, t_{rise} - fall time, t_{on} - ON time of a switch
Q_{G} - gate charge, I - current through the element, f_{sw} - operating frequency

Synchronous buck conversion is commonly adopted in VRM with the multiphase interleaved buck converter technique [12]. The basic configuration of multiphase buck converter technique is shown in Fig. 1.7(c). Synchronous buck converter output has higher ripples of current and voltage compared to a multiphase buck converter. The requirement for high current is provided by multiphase converters. This topology is basically used to improve the efficiency and transient response [11, 17, 45, 46]. Studies in [8, 27] showed that the performance of multiphase VRM topologies is much better than the conventional buck and the synchronous buck converter topology. Multi-phasing is found to be the only approach that can deliver the performance required by VRM applications. But end-to-end efficiency and cost of these systems is still questionable. Therefore, high efficiency, high-power-density, cost effective VRMs are critical in satisfying power requirements of the fast changing processor technologies. The production cost and sensitivity of these applications continuously challenge the SMPS topologies.

1.4.3 Linear regulators for VRM: advantages and opportunities

Linear regulator technique is the simplest way of converting a higher DC voltage to a lower. The highest efficiency of a linear regulator can be obtained when the input-to-output voltage reaches its minimum (dropout voltage). The dropout voltage is defined as

the minimum voltage required to maintain a regulated output voltage and is determined by the pass-element. The pass-element of the linear regulators can be either N or P-channel BJT or MOSFET transistors. Linear regulator capabilities mostly depend on the properties of the pass-element [47, 48]. For high-current applications, Darlington transistors are used as the pass-element, but they have high collector-to-emitter voltage drop [49] due to two base-to-emitter drop.

Though there are no exact boundaries to define the values for standard and low dropout regulators, a standard linear regulator discuss above can be dropped voltage up to a minimum of 2 V. They are suitable for low power applications or an application where the efficiency is not an issue. For applications that require high-efficiency, linear regulators use low-dropout regulators.

LDO is the most widely-used linear regulator in modern electronic applications, which is usually a single IC or integrated into multi-functional power management [50, 51]. Ideally for reduced-switch SCALDO (RS-SCALDO) application, the LDO dropout voltage can be as low as 100 mV at 5 A and it should be lower as possible to minimize power dissipation and maximize efficiency. LDOs can provide either an adjustable or fixed-output voltage.

Similar to the standard linear regulators, a LDO consists of a voltage reference, an error amplifier, a feedback voltage divider, and a pass-element [52] as shown in Fig. 1.8. The most common pass-elements are P-channel or N-channel MOSFETs [52]. A very lower dropout voltage can be obtained using MOSFETs rather than a Darlington transistor in standard linear regulator [43]. Further an N-channel pass-element can drop more voltage than a P-channel element with similar specifications [52].

With control circuit current I_{cnt} (quiescent current) in the denominator, it is evident that the higher I_{cnt} is, the lower the efficiency becomes. Current LDOs have reasonably low I_{cnt}, and for simplicity, I_{cnt} can be neglected in efficiency calculations if I_{cnt} is very small compared to I_{L}. Then LDO efficiency is simplified as

$$\eta = \frac{V_{\mathrm{out}} I_{\mathrm{L}}}{V_{\mathrm{in}}(I_{\mathrm{L}} + I_{\mathrm{cnt}})} = \frac{(V_{\mathrm{in}} - V_{\mathrm{do}}) I_{\mathrm{L}}}{V_{\mathrm{in}}(I_{\mathrm{L}} + I_{\mathrm{cnt}})} \tag{1.3}$$

where load current I_{L} very large compared to control circuit current I_{cnt} is giving

$$\eta = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{V_{\mathrm{in}} - V_{\mathrm{do}}}{V_{\mathrm{in}}}$$

and therefore

$$\eta = 1 - \frac{V_{\mathrm{do}}}{V_{\mathrm{in}}} \tag{1.4}$$

As the Eq. (1.4) implies, the efficiency of a linear regulator is directly related to the voltage dropped across its pass-element (V_{do}). This drop is significant because dissipated power is equal to multiplication of the load current I_{L} and the dropout voltage V_{do}.

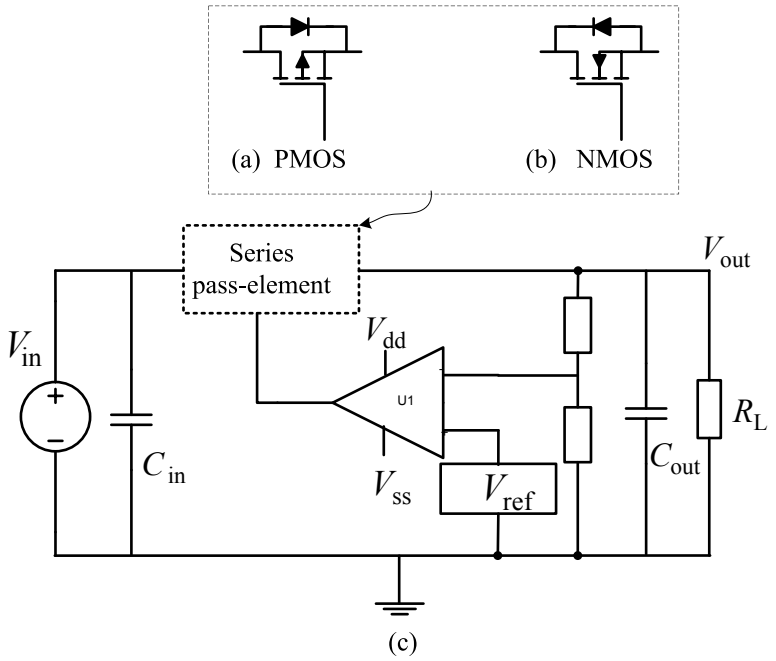


Figure 1.8: Low dropout regulator with most common pass-elements: (a) P-MOS, (b) N-MOS and (c) equivalent circuit

Selecting P-channel and N-channel LDOs are based on the application requirements (input voltage, minimum dropout, load and line performance, etc). For PMOS LDOs, same input power source can be used to power the control circuit whereas NMOS LDOs need to provide a gate drive which is higher than the output voltage. The basic performance (line and load regulations) of them can be compared as in Table 1.2 [53, 54]. The transconductance and ON-resistance of NMOS (M_n) and PMOS (M_p) are g_{mn}, g_{mp}, r_{onn}, and r_{onp} respectively. A_v is the open loop gain of the amplifier and I_{load} is the current through R_{L}. The NMOS regulator has an improved by $1/g_{mp}r_{onp}$ line regulation compared to PMOS [52].

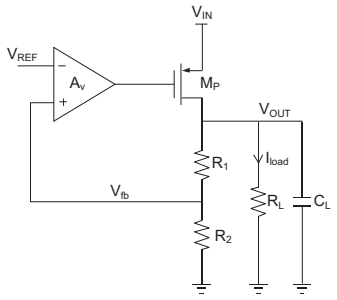
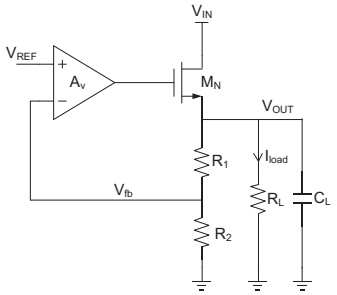
Usually, NMOS LDOs gate drive circuit is supplied by an internal charge-pump or external bias voltage. PMOS LDOs are simpler but similar sized NMOS can achieve lower dropout [52].

Loop stability and the response to transient changes in load current are affected by the output capacitance and its ESR [55]. ESR $\leqslant 1\ \Omega$ is recommended to ensure stability. Also, LDOs require input and output capacitors C_{in} and C_{out} to filter noise and control load transients [56]. Larger values of capacitors improve the transient response of the LDO, but increase the start-up time.

1.5 A comparison of LDO and SMPS

The simplest way to reduce the voltage of a DC supply is to use a linear regulator, but linear regulators waste energy as they operate by dissipating excess power as heat and

Table 1.2: Comparison of PMOS and NMOS LDO configurations

LDO	PMOS	NMOS
Topology		
Line regulation $\Delta V_{OUT}/\Delta V_{IN}$	$\simeq \frac{1}{\frac{R_2}{R_1+R_2} A_v g_{mn} r_{onp}}$	$\simeq \frac{1}{\frac{R_2}{R_1+R_2} A_v}$
Load regulation $\Delta V_{OUT}/\Delta I_{load}$	$\simeq -\frac{1}{\frac{R_2}{R_1+R_2} A_v g_{mp}}$	$\simeq -\frac{1}{\frac{R_2}{R_1+R_2} A_v g_{mn}}$

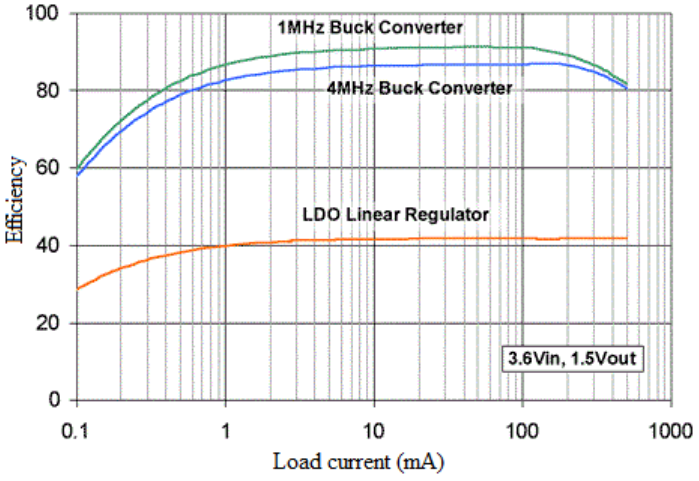
do not yield any current step-up. Switch-mode power suppliers on the other hand can improve the current capability.

The main advantage of an LDO is its relatively quiet operation, since LDOs do not involve switching. The main source of noise of an LDO is the internal band gap voltage reference [58, 59]. Its noise usually specified in microvolts rms over a specific bandwidth, such as 30 μV_{rms} from 1 to 100 kHz [60]. Compared to the noise generated from switching transients and harmonics of a high frequency switched-mode converter this low-level noise in an LDO can be ignored [4]. A small bypass capacitor at the output of the voltage-reference can minimize this noise.

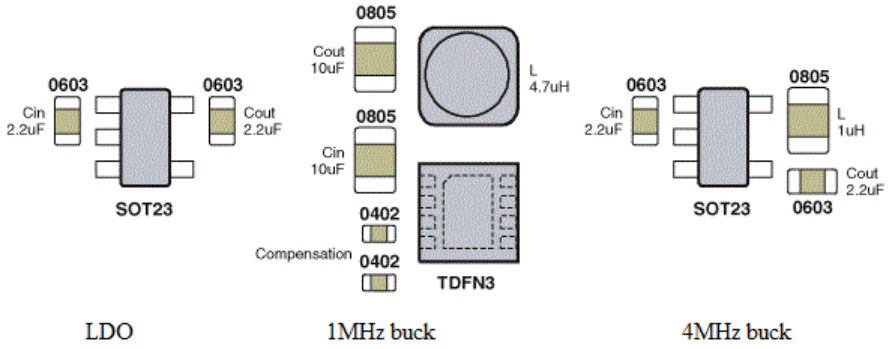
For a battery powered application of 3.6-to-1.5 V, an LDO efficiency is compared with two buck converters (operate in different switching frequencies 1 MHz and 4 MHz) in Fig. 1.9(a) and the physical size in Fig. 1.9(b). An LDO linear regulator is a physically small solution, though the efficiency is low. When stepping down a 3.6 V battery to a 1.5 V output of a 0.1 A load, 0.21 W of minimum power is dropped across the LDO. From Eq. (1.4) the maximum efficiency is

$$\eta = 1 - \frac{V_{do}}{V_{in}} = 1 - \frac{2.1\ \text{V} \times 0.1\ \text{A}}{3.6\ \text{V} \times 0.1\ \text{A}} = 1 - 0.583 \approx 42\% \tag{1.5}$$

This voltage drop yields a power loss of ∼58%, which lowers the efficiency down to ∼42%. The unused energy is dissipated as heat within the LDO and there is no element in the LDO to store them and reuse them in its operation. Therefore, the efficiency within wide input-output ranges is worse and similar to that of a standard liner regulator. However, compared to standard linear regulators, the LDO properties: low dropout voltage, and low quiescent current.



(a)



(b)

Figure 1.9: Comparison of LDO and buck converters (a) efficiency of 3.6-to-1.5 V, (b) physical size of the converters. [57]

The traditional 1 MHz buck converter provides very high efficiency, but at a large size penalty. The newest high-speed 4 MHz buck converters are sized close to the LDO and close to the 1 MHz buck in efficiency [57]. Nearly twice of an efficiency of LDO can be achieved from a buck converter. However, 4 MHz buck converter sacrifices a few efficiency points to achieve a smaller solution.

The efficiency of LDOs is high in low dropout voltage range. Low electromagnetic interference (EMI) in LDOs is attractive for portable and wireless applications. Therefore, LDOs are most commonly used for post-regulation in high efficiency applications than in a direct conversion of a high voltage to a low voltage. However, to achieve a clean output of an LDO the converter settles for a lower efficiency. For example, an SMPS pre-regulator (3.6 V to 1.8 V with 95% efficiency) combines to an LDO (post-regulator with 1.8-to-1.5 V the maximum efficiency of which can reach a value as high as 83%) achieving a maximum

of 79%. That is

$$\eta_{3.6\text{-}1.5} = \eta_{3.6\text{-}1.8} \times \eta_{1.8\text{-}1.5} = 95\% \times 83\% \approx 79\% \tag{1.6}$$

Limitations of standard computer power supply for linear VRMs

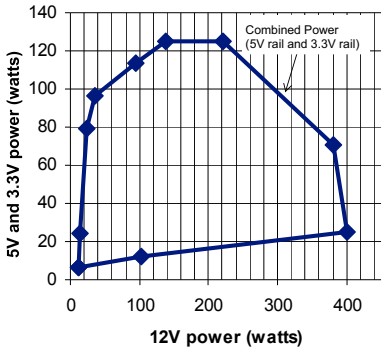
Standard computer power supply convert alternating current (AC) into direct current (DC) required by the computer motherboard. It is a pre-regulator for VRM and it rates in watts. The quoted wattage represents the maximum total power that can be provided across all of these rails simultaneously. According to the ATX, the voltage tolerance of the computer power supply is given in Table. 1.3. This table consists of data for 450 W ATX12V [61]. ATX is a motherboard configuration specification developed by Intel [61]. Amperage rating for each rail, showing how the available power is divided up. See Table 1.10(a).

Table 1.3: The ATX specification of the power supply output voltage tolerance [61]

Supply [V]	Tolerance	Range (min. to max.)[V]	Ripple (p. to p. max.)[mV]
+5	±5%	+4.75 to +5.25	50
−5	±10%	−4.50 to −5.50	50
+12	±5%	+11.40 to +12.60	120
−12	±10%	−10.80 to −13.20	120
+3.3	±5%	+3.135 to +3.465	50
+5	±5%	+4.75 to +5.25	50

Output	Min. Current (amps)	Max. Current (amps)	Peak Current (amps)
+12 V1DC(1)	1	14	15
+12 V2DC(1, 2)	1	16	19
+5 VDC	0.3	15	
+3.3 VDC	0.5	22	
-12 VDC	0	0.3	
+5 VSB	0	2.5	3.5

(a)



(b)

Figure 1.10: Typical power distribution for a 450 W ATX12V configuration: (a) current in different rails; Total combined output of 3.3 V and 5 V is 130 W Peak currents may last up to 17 seconds with not more than one occurrence per minute (1) 12V1DC and 12V2DC should have separate current limit circuits to meet 240VA safety requirements. (2) 12V2DC supports processor power requirements and must have a separate current limit and provide 19 A peak current for 10 ms; minimum voltage during peak is > 11.0 VDC. (b) 450 W cross loading graph (sum of 5 V and 3.3 V rails with vs. 12 V) [61]

Positive rail of 3.3 V supplies the maximum current, while the combination of +12 V rails provides maximum total power. For input of SMPS-based VRMs, +12 V high power rail is beneficial to obtain high-currents. However, for a standard linear approach +3.3 V high-current rail is more suitable than the +12 V rail. For example, maximum load current of 160 A can be achieved using 12-to-1.2 V VRM built based of SMPS technique. A similar linear regulator-based VRM provides only 16 A; assuming that both cases (SMPS and linear techniques) use +12 V, 16 A rail. Not only the current capability is higher in SMPS approach but also the theoretical efficiency of 12-to-1.2 V is ten times higher than a standard linear approach.

1.6 Supercapacitor-based DC-DC linear converter

SCALDO [1, 2, 5–7, 53] is a radically new DC–DC converter technique that improves end-to-end efficiency by combining a supercapacitor (SC) with a linear regulator. A topology of a basic converter is shown in Fig. 1.11.

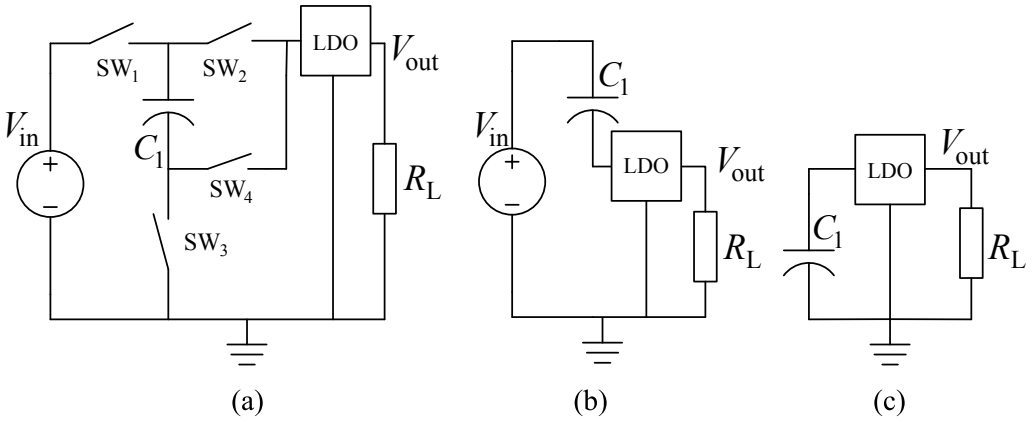


Figure 1.11: SCALDO basic topology: (a) The circuit of an ideal step-down DC-DC converter, together with (b) its equivalent charge circuit and (c) its equivalent discharge circuit

The operation of SCALDO is controlled by the system defined minimum input voltage of an efficient LDO. This input is limited by the minimum dropout voltage of the LDO where it operates at the highest efficiency. Unlike in the charging phase of SWC the negative end of the $C1$ capacitor decreases until it reaches the system defined voltage. Further, it never charges in parallel with power supply.

Figure 1.12(a) and (b) are simple equivalent circuits of charge and discharge configurations of SCALDO in Fig. 1.11(b) and (c) respectively. These assume that the components are ideal. When connecting the SC to the LDO input voltage v_{in} is extended by v_{sc}. This yield that an SC drops a high voltage of a supply V_{p} to a low v_{in}. A considerably large capacitor can maintain this series connection unblocked for quite long time while regulating the system output V_{reg}. Once LDO reaches the minimum voltage, the capacitor disconnects from the supply and powers the load via LDO as in Fig. 1.11(c).

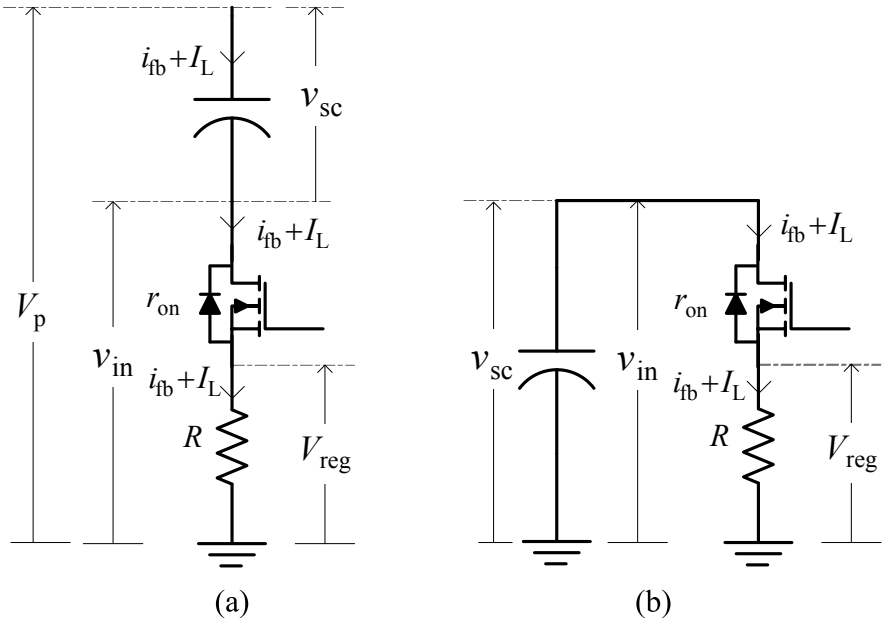


Figure 1.12: SCALDO equivalent circuit: (a) charging configuration, (b) discharging configuration

For the above SCALDO configuration, V_p should be greater than twice of the system specified minimum voltage. In SCALDO operation, charge balance is maintained. Therefore, the excess charges in the capacitor has to be removed. At the discharging phase, these excess charges release to the load on demand.

During SCALDO charge-discharge process two main instances occur (i) input voltage of linear regulator maintains closer to dropout voltage during both charging and discharging phases of the supercapacitor, and (ii) the unregulated input power supply powers circuit only when charging the supercapacitor.

Due to the first instance the efficiency of linear regulator maintains at high. The second instance improves V_{reg}/V_p by a multiplication factor (>1) which defines by the number of supercapacitors required for a configuration. If ideal components are used, the theoretical end-to-end efficiency of the above single supercapacitor configuration can be workout as

$$\eta = \frac{V_{reg} I_L}{V_p[(I_L/2) + I_{fb}]} = 2\frac{V_{reg}}{V_p} \tag{1.7}$$

where I_{fb}/I_L is very small and thereby neglected.

For example, in a typical 3.6-to-1.5 V SCALDO can achieve ∼83.34% efficiency which is approximately twice of the efficiency of a similar linear regulator with ∼41.67%. SCALDO can achieve end-to-end efficiency close to a SMPS.

The essential theory on SCALDO that required for this thesis is described in Chapter 3. With all the properties of LDOs and SCs including the high-current capability, the main conclusion of the first SCALDO research was that " the SCALDO is a viable solution that

demonstrates a new approach to the design of DC-DC converters suitable for processor power supplies requiring high end-to-end efficiency" [4].

Switches are required to change the polarity of capacitors physically to interchange from charge to discharge configuration and vice versa. Also, capacitors connect and disconnect from unregulated input supply and the ground during the operation. Gate driver loss in switching is

$$P_{\text{loss\_gate}} = Q_{\text{GS}} V_{\text{GS}} f_{\text{sw}} \tag{1.8}$$

where V_{GS} is gate voltage, gate charges Q_{GS} is in 10^{-9} C range and switch operating frequency is in 10^{2} to 10^{-3} Hz range.

Due to low frequency operation, the dynamic losses in switches are minimal. There is no external frequency oscillator to control the switches. Frequency of operation varies on the load current demand, fluctuations of input supply voltage and the system-fixed lowest input voltage of the linear regulator. Further to reduce the complexity and power losses in the circuit number of switches were minimized and introduce a new topology known as RS-SCALDO [54, 62, 63].

With the availability of large supercapacitances, supercapacitor-assisted regulators become suitable for medium to large current applications. To obtain higher efficiencies very low dropout regulators can be used. Since the load sees the steady output of a linear regulator, these regulators can be utilized for noise sensitive loads.

1.7 SCALDO compare with switched-capacitor converter

A brief comparison of the main features of SCALDO and SWC techniques can be found in the following section with an introduction to SWC.

1.7.1 Switched capacitor converters

Due to the problematic magnetic components in DC-DC converters, research towards the nonmagnetic converters has been boosted since the late 1970s [34]. The first innovation was the SWC or, as it is commonly known, the charge-pump. It is a combination of smaller sized capacitors with high-frequency switches which are suitable for low power applications. They can be built to a smaller size with lower cost, and less complexity than traditional switch-mode converters that use magnetic energy storage elements [34]. Most frequently SWCs are known for the conversion of the supply voltage to a DC-output voltage that is several times higher than the input. There are two types of converters, step-down and step-up where the circuit topology sets the ratio $V_{\text{out}}/V_{\text{in}}$.

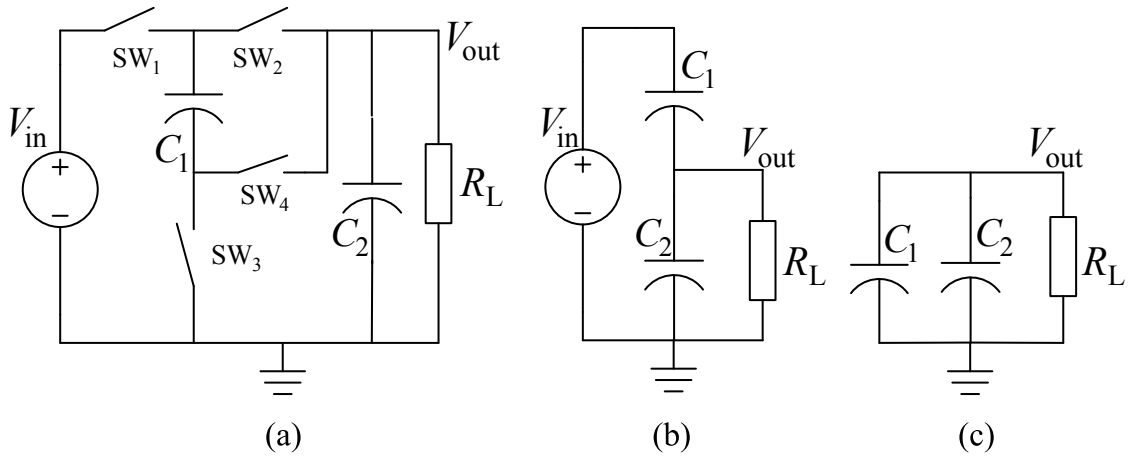


Figure 1.13: Switched-capacitor step-down converter: (a) The circuit of an ideal series-parallel charge-pump step-down DC-DC converter, together with (b) its equivalent charge circuit and (c) its equivalent discharge circuit [34]

Step-down converter: A circuit topology of a step-down converter of a SWC is illustrated in Fig. 1.13. It is an ideal series-parallel converter with ratio 2:1 illustrated with its two basic phases of operation: charging and discharging. Series-parallel refers to the operation of capacitors in the circuit: charge in series and discharge in parallel. There are two capacitors in this circuit, $C1$ and $C2$. $C1$ is called flying as in one phase of the operation its negative terminal is not connected to the ground. Typically $C1$ is smaller than $C2$ and the sharing of charges slightly increase the output voltage V_{out}.

During the charging phase the voltage source V_{in} is powering both the flying-capacitor $C1$ and the output capacitor $C2$. They are charged in series with each other by closing the switches SW1 and SW4 and opening switches SW2 and SW3, yielding the equivalent charge circuit shown in Fig. 1.13(b). Current through $C1$ is the charging current of $C2$ and the load $R_{\mathbf{L}}$ current. Output voltage increases with the voltage increase in $C2$. When the output voltage reaches $V_{\text{in}}/2$, it starts to discharge.

When the SW2 and SW3 are closed and the switches SW1 and SW4 are open, $C2$ and $C1$ become parallel, yielding the equivalent discharge circuit shown in Fig. 1.13(c). During this phase $C1$ is powering $C2$. A part of the charge current from $C1$ is drawn by the load. From this operation principle it follows that V_{out} can never exceed $V_{\text{in}}/2$, as this would cause the reversing of the energy flow from the output to the input [34], which is physically impossible. This charge-discharge (charge transfer) operation continues with a switching frequency at f_{sw} where V_{out} is

$$V_{\text{out}} = I_{\text{out}} R_{\text{L}} = f_{\text{sw}} C1 \Delta V_{\text{C1}} R_{\text{L}} = f_{\text{sw}} C1 (V_{\text{in}} - 2V_{\text{out}}) R_{\text{L}}$$

$$\Rightarrow V_{\text{out}} = \frac{f_{\text{sw}} C1 R_{\text{L}}}{1 + f_{\text{sw}} C1 R_{\text{L}}} V_{\text{in}} \tag{1.9}$$

where ΔV_{C1} is the deferential voltage of $C1$ capacitor.

For ideal switches, there are no switch losses and variations of output ΔV_{out} is zero where f_{sw} is infinitely large, therefore η_{down} is independent of switching frequency f_{sw} can be define for two special cases: (i) $C1 \gg C2$ and (ii) $C2 \gg C1$ are respectively in Eq. (1.10) and (1.11)

$$\eta_{\text{down}} = \frac{V_{\text{in}} + 2V_{\text{out}}}{4(V_{\text{in}} - V_{\text{out}})} \tag{1.10}$$

$$\eta_{\text{down}} = \frac{V_{\text{in}}V_{\text{out}} + 2V_{\text{out}}^2}{V_{\text{in}}^2} \tag{1.11}$$

Theoretically SWCs can achieve a higher power conversion efficiency than using a linear series converter [34]. For example, in a typical 2 capacitor step-down converter with 3.6-to-1.5 V can achieve ∼76-79% efficiency which is approximately twice the efficiency of a similar linear regulator with ∼42%. However, performance (efficiency and output resistance) is limited by the number of capacitors utilized in a configuration [64].

Step-up converter: A topology of a simple step-up converter of SWC is shown in Fig. 1.14. It is similar to a step-down configuration. Let us consider a topology with two capacitors driven by two complementary phases: charging and discharging of flying-capacitor $C1$.

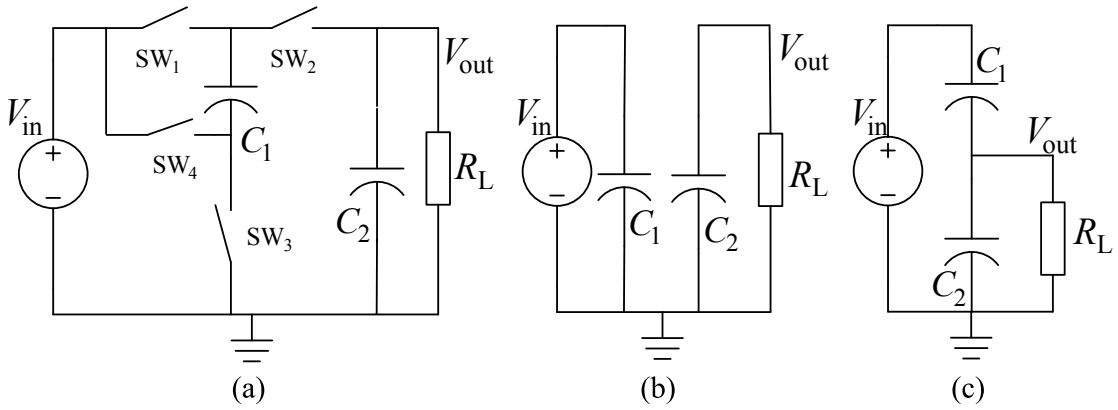


Figure 1.14: Switched-capacitor step-up converter: (a) The circuit of an ideal series-parallel charge-pump step-up DC-DC converter, together with (b) its equivalent charge circuit and (c) its equivalent discharge circuit [34]

During charging phase the voltage source V_{in} is powering the flying-capacitor $C1$ while the output capacitor $C2$ discharges to the load. For this operation, the switches SW1 and SW3 are closed and switches SW2 and SW4 are opened, yielding the equivalent charge circuit shown in Fig. 1.14(b). When the SW2 and SW4 are closed and the switches SW1 and SW3 are opened, V_{in} powers both $C2$ and $C1$ in series, yielding the equivalent discharge circuit shown in Fig. 1.14(c). Current through $C1$ is the charging current of $C2$

and the load R_{L} current. The output voltage increases with the voltage increase in $C2$. When the output voltage reaches $2V_{\mathrm{in}}$, it starts to discharge.

From this operation principle it follows that V_{out} is limited to $2V_{\mathrm{in}}$. This charge-discharge (charge transfer) operation continues with a switching frequency at f_{sw} where V_{out} is

$$V_{\mathrm{out}} = I_{\mathrm{out}}R_{\mathrm{L}} = f_{\mathrm{sw}}C1\Delta V_{\mathrm{C1}}R_{\mathrm{L}} = f_{\mathrm{sw}}C1(2V_{\mathrm{in}} - V_{\mathrm{out}})R_{\mathrm{L}}$$

$$\Rightarrow V_{\mathrm{out}} = \frac{2f_{\mathrm{sw}}C1R_{\mathrm{L}}}{1 + f_{\mathrm{sw}}C1R_{\mathrm{L}}}V_{\mathrm{in}} \tag{1.12}$$

where ΔV_{C1} is the deferential voltage of $C1$ capacitor.

For ideal switches, there are no switch losses and ΔV_{out} is zero where f_{sw} is infinitely large. Therefore η_{up} is independent of switching frequency f_{sw} can be defined by two special cases: (i) $C1 \gg C2$ and (ii) $C2 \gg C1$ are respectively in Eq. (1.13) and (1.14)

$$\eta_{\mathrm{up}} = \frac{2V_{\mathrm{in}}V_{\mathrm{out}} + V_{\mathrm{out}}^2}{8V_{\mathrm{in}}^2} \tag{1.13}$$

$$\eta_{\mathrm{up}} = \frac{V_{\mathrm{out}}^2}{2V_{\mathrm{in}}^2 + V_{\mathrm{in}}V_{\mathrm{out}}} \tag{1.14}$$

If a variable oscillator frequency is used in SWC, either a higher output ripple or a very low output current will restrict the design, but for fixed frequencies the quiescent current will be high [34].

SWCs are commonly used in a vast range of electronic applications such as operational amplifiers, N-channel LDO control circuits, nonvolatile memories, etc [65]. Since they are made of capacitors and diodes or MOSFET switches, they are allowing integration on silicon. Light weight, small size and high power density are the result of using only switches and capacitors in the power stage of these converters [66]. Since they are not regulating the output voltage a separate regulator is required for low ripple applications.

1.7.2 Compare SCALDO and SWC

Switched-capacitor technique is one that confuses with SCALDO as both the techniques have some similarities in topologies, components, etc. One of the main reasons for this confusion is, unlike the other traditional switched-mode voltage converters which employ inductors; SWC and SCALDO are only built with capacitors and switches. The basic switch configuration of both step-down converter of SWC is similar to SCALDO except the second capacitor in Fig 1.13 and LDO in Fig. 1.11. This made a confusion to consider SCALDO as a variation of SWC. Considering the operation and the features, a summary of a comparison can be found in Table. 1.4

Given the above summary, it is very clear to see that the SCALDO technique is quite different to the operation of SWC [53, 54], for four primary reasons:

Table 1.4: A summary of a comparison of switched-capacitor and SCALDO techniques [53,54]

Switched-capacitor (charge pump) technique	SCALDO technique
(i) Basically a high frequency switching technique for voltage conversion	A modified version of a linear regulator with an enormous capacitor in series path as a lossless voltage dropper. (the switches do not convert the voltage)
(ii) Can step-down, step-up or invert. Mostly used to step-up or invert a DC voltage	Always a step-down configuration
(iii) Capacitors used are in the range of few nano-farads to few tens of micro-farads	Enormously large capacitors are used
(iv) Circuit design starts with an oscillator supplying a fixed switching frequency	Operating frequency varies with the load current. Switch operation is based on the case of a maximum/ minimum voltage detected across the input of the LDO
(v) Switching frequency is in the range of 10s to few 100 kHz	Very low frequency (milli-hertz to few 100 of hertz) used for capacitor energy recovery and reuse
(vi) Load regulation is not precise and requires a another voltage regulator (linear/low drop out type) for precise output voltage	Load always sees the precise output of a linear/low drop out regulator
(vii) In one part of the cycle, capacitor comes in parallel to unregulated supply	Capacitor never comes parallel to the input unregulated supply
(viii) Technique is suitable only for very low load currents	Technique is applicable to very large load currents. (High current capable LDO is required)
(ix) Significant dynamic losses in switches	Negligible dynamic losses in switches
(x) Theoretically a voltage conversion factor applies to a given configuration	Theoretically an efficiency multiplication factor is defined for a given configuration

1. The capacitor never charge parallel with power supply (This is the unique behaviour of the SCALDO technique.)
2. SCALDO technique uses a capacitor as a lossless voltage dropper, together with an LDO for precise output regulation
3. Extremely low switching frequency, and it varies on the load current. (This is a characteristic behaviour of the SCALDO technique.)
4. If an ultra LDO can be developed for the required output current, there is no limit to precise output regulation at high load currents. (This is due to the availability of single cell supercapacitors which are in the range of fractional farads to a few thousand farads.)

The linear technique is the simplest approach to step-down the voltage of a DC power supply. It has the advantage of fast transient capabilities and reliable output voltage with little noise introduced into its DC output. However, most of the time linear regulators are the least efficient, as they waste energy through series element. Improvements

to the efficiency of linear DC-DC converter technique can give a topology with better performance.

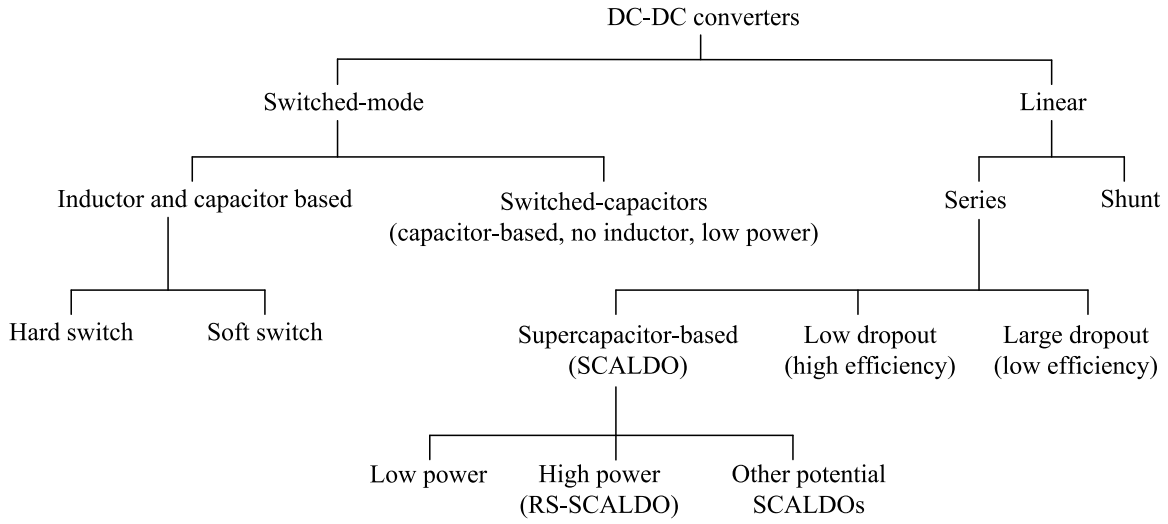


Figure 1.15: A classification of DC-DC converter techniques for SCALDO and RS-SCALDO

Comparing the features and operating basics of linear, switch mode, switched capacitor power supplies with supercapacitor-assisted linear regulator, it can be positioned as a new regulator technique as in Fig. 1.15. A comparison of cost, and complexity of DC-DC converters based on components (inductor, diode, high side MOSFET) and technology is summarized in the Table 1.5. Buck converter topologies require more components than linear, SWC, and SCALDO. The complexity is increasing on the control circuit technology and the requirements of technical expertise in designing those circuits. Multiphase interleaved synchronous buck converters are the most expensive designs due to complex control techniques and the number of components required for the circuit. Though SCALDO is more complex than a standard linear regulator, compared to other topologies in Table 1.5 it is less complex and can achieve approximately 83% efficiency from a single capacitor configuration. However, the parasitic discharge in SCs demands utilization of expensive opto-isolated switches which increase the cost. To address parasitic discharge in SCs issue, a thorough investigation was required. Further, a clear gaps in the SCALDO literature motivated for investigation of digitally controlled output capability, and the control circuit modifications for high current SCALDO version.

In many practical situations, all three converter techniques (SMPS, SWC and linear regulators) are utilized to get the optimum benefit of their characteristics. Hybrid topology is a combination of SMPS with linear DC-DC converters at the step-down stage and the regulation stage. Research in last few years focused to design active filter-based hybrid topology [67]. However, these hybrid regulators dissipate a significant amount of power through the resistive switches and therefore reduce overall efficiency [68]. Since designing

Table 1.5: Comparison of DC-DC converters: complexity, cost and efficiency

Type converter	Complexity	Cost	Efficiency and losses
Standard buck (SB)	Higher than linear regulator and SCALDO	Extra cost incurred for heat sinks at high currents and high switching frequencies	Low efficiency than SNB; losses are significant in diode and capacitor ESR
Synchronous buck (SNB)	Higher than SWC and SBs; requires special knowledge	Additional cost for MOSFET switches, switch drivers and control circuit than SBs	Higher efficiency than SB; more switching losses than MISNB in high frequency operations and high current
Multiphase interleaved synchronous buck (MISNB)	Highest of all; requires special expertise knowledge, skills and experience; complexity increases with number of phases and load balancing techniques	Higher cost incurred due to multiple components; complex control circuit, and for the expertise knowledge; no large buffer capacitors	More efficient for high current loads and less efficient than SNB at low currents
Switched-capacitor (SWC) step-down	Higher than linear regulators and SCALDO	Require separate circuit for regulation; not suitable for high power applications	Switch related losses in high frequency
Linear regulator	Low complex	Low cost; large heat sinks are required for high power applications	Lowest efficiency
SCALDO	Higher than linear regulator	Cost lower than SB/SNB/MISNB; heat sink requirement is considerably low	Similar efficiency to SB/SNB/MISNB; losses mainly due to ESR of SCs and ON resistance of switches

VRM using these hybrid approaches does not simultaneously fulfill the basic requirements of minimizing cost and size, and optimizing power efficiency.

In this chapter, I investigated the efficiency of three common DC-DC converters techniques and SCALDO; the relative complexity, cost and efficiency of the three common DC-DC converters and compared with SCALDO. Given the advantages, I review the essential theory and applications of supercapacitors and SCALDO in the next chapter.

Chapter 2

Essential theory and applications of supercapacitors and SCALDO

The existing supercapacitor energy recovery technique for low-dropout regulators is used as the basis of the new reduced-switch SCALDO topology with a view to investigate its effectiveness in terms of cost and efficiency. This chapter reviews the essential theory behind supercapacitors and the supercapacitor-assisted low-dropout regulator (SCALDO) design. Further, flexibility of customizing SCALDO topology for different applications is presented.

2.1 Electrical properties of supercapacitor for DC power applications

Capacitors are one of the fundamental and indispensable components in any electrical or electronic circuit. Capacitors are classified based on their properties, and named for their electrolyte or their dielectric (insulator) material. An overview of different types of capacitors is presented in Fig. 2.1 [69].

Supercapacitors are commonly classified as being polarized capacitors; however, non-polarized versions are available [70]. They use two types of charge storage (i) electrostatic (double layer) and (ii) electrochemical; hybrid capacitors combine both approaches.

The other type of polarized capacitors are the electrolytics. They can be divided by the type of material used for the construction of the electrolyte: aluminum (Al), tantalum (Ta) and niobium (Nb) with conductive polymer or MnO_2 in either non-solid, solid or hybrid form. Most non-polarized capacitors such as ceramic, film, paper and mica are named after their dielectric material [71, 72]. The various categories of capacitors have their own features and specifications which can be utilized in different applications. Capacitance and working voltage are the two major properties to be considered in practical applications; see Fig. 2.2.

The simplest geometry for a capacitor is shown in Fig. 2.3(a): two parallel conductor plates separated by a dielectric material. Capacitance is a function of design geometry (area A and distance between plates d) and permittivity of the dielectric material between

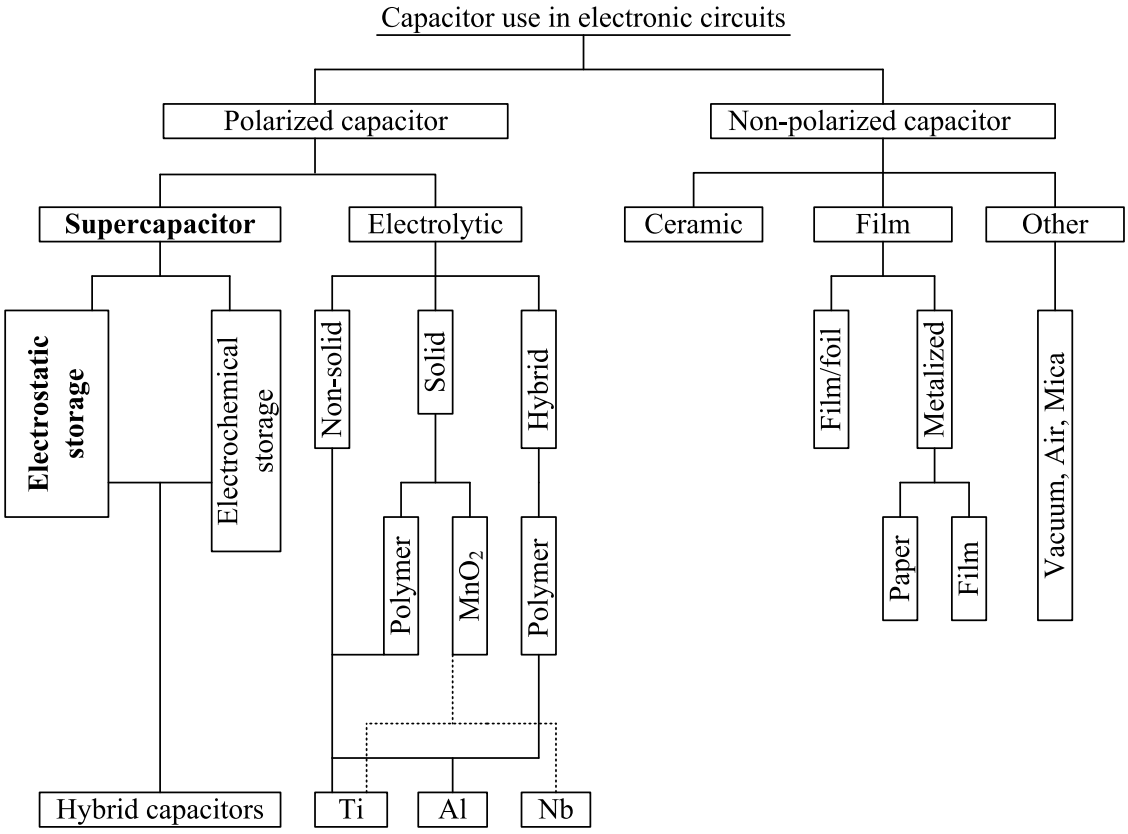


Figure 2.1: Overview of commonly used capacitors in electronic circuits [Modified from [69]]

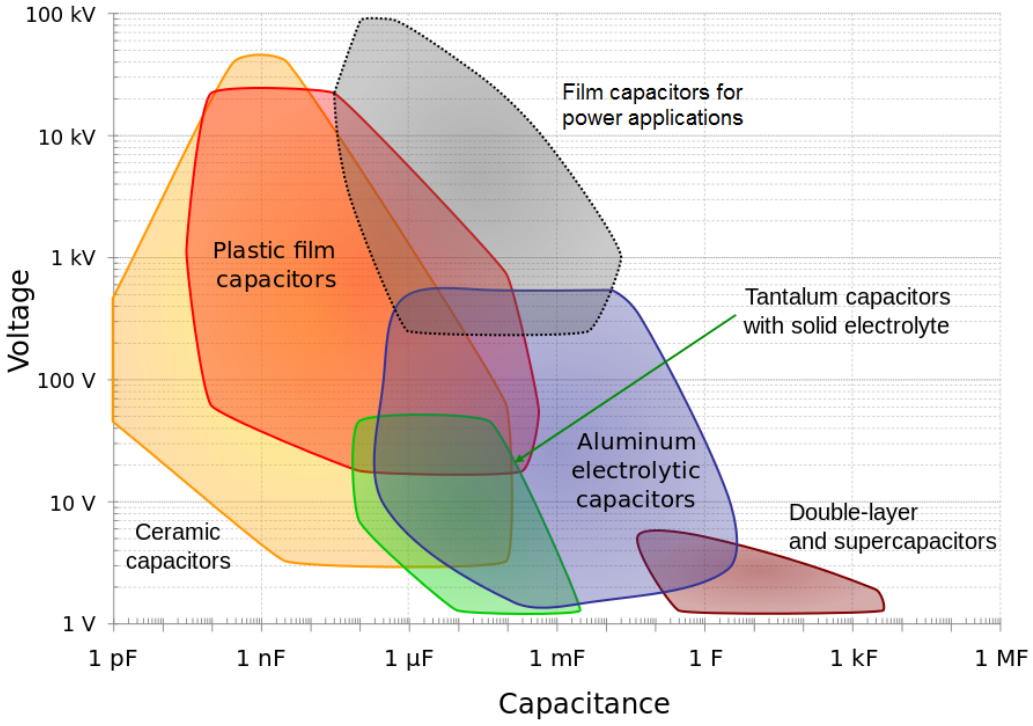


Figure 2.2: Different capacitors with their voltage and capacitance capabilities [73]

the plates ε. It is equal to $\varepsilon A/d$. Capacitance values range from fractional pico-farads (in ceramic capacitors) to thousands of farads (in supercapacitors).

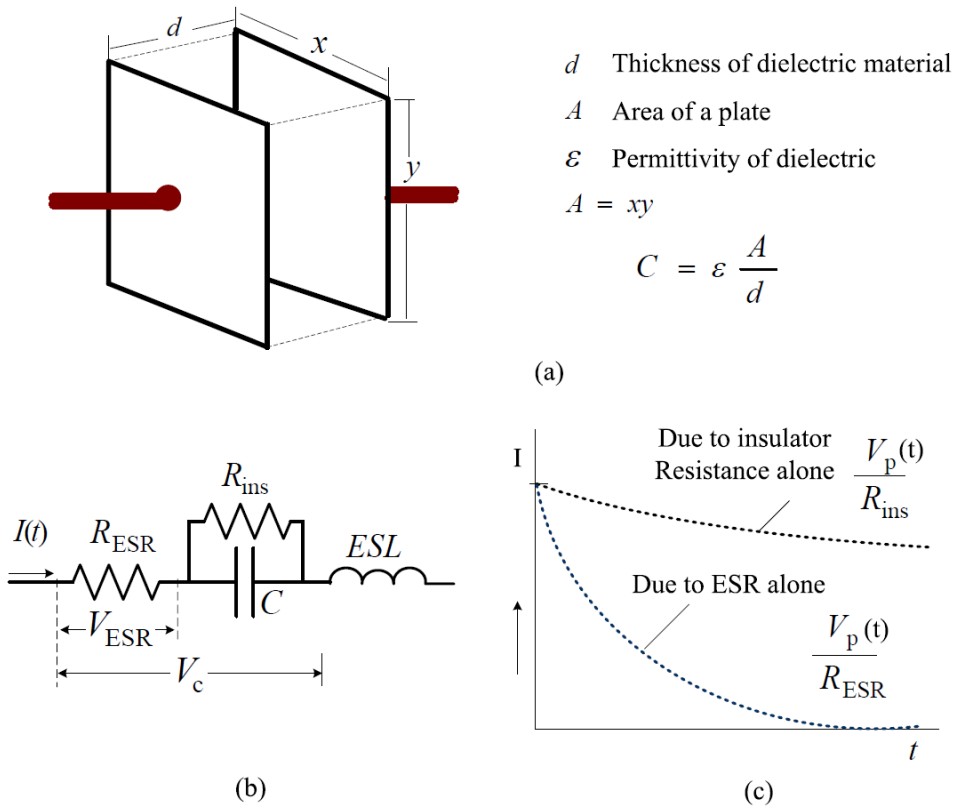


Figure 2.3: Capacitor basics: (a) Simple geometry of a parallel plate capacitor, (b) equivalent circuit of a realistic capacitor with parasitic elements (i.e. equivalent series resistance—ESR as R_{ESR}, insulation resistance R_{ins} and equivalent series inductance—ESL), (c) maximum current limits by ESR and leakage current due to insulation resistance

Capacitors have two main practical applications (i) storage and release of electric charge and (ii) blocking or passing of a current signal. The charging-discharging process is fully reversible: there is no chemical or phase change taking place; charges are stored physically by moving electrons and protons to opposite plates. When charging or discharging, a capacitor stores or releases electrical energy. This phenomenon is applied in many practical applications such as storage, buffering, and smoothing circuits [74–79]. The second function is commonly utilized in noise sensitive applications to filter or eliminate particular frequencies [74].

Important capacitor properties for DC applications are; (i) capacitance, (ii) working voltage, (iii) equivalent series resistance (ESR), (iv) leakage current, (v) polarization, (vi) working temperature, and (vii) physical size. These properties determine the maximum current that can be drawn from a capacitor, the time constant, and power and energy densities [80]. Capacitance C of an ideal capacitor is equal to the amount of charge Q acquired per unit voltage V applied, $C = Q/V$. Instantaneous voltage and instantaneous current is expressed by (2.1) and (2.2) respectively,

$$v(t) = \frac{q(t)}{C} = \frac{1}{C}\int_{t_0}^{t} i(t)dt + V(t_0) \tag{2.1}$$

$$i(t) = \frac{dq(t)}{dt} = C\frac{dv(t)}{dt} \tag{2.2}$$

where the initial voltage at the t_0 is $V(t_0)$.

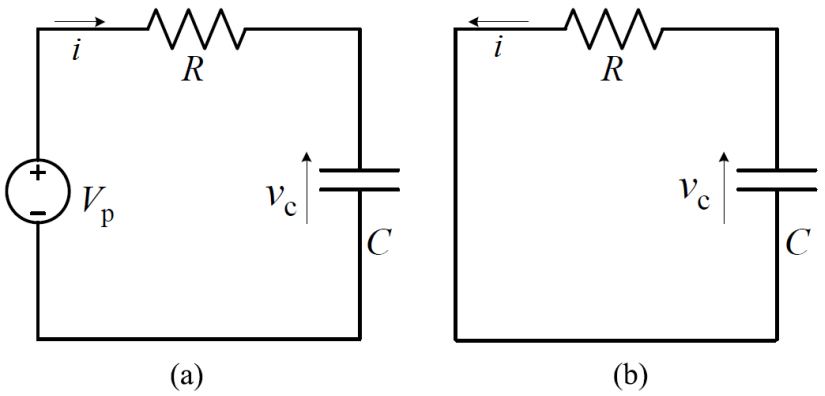


Figure 2.4: Ideal capacitor: (a) charging from an ideal voltage source, (b) discharging into a fixed resistive load

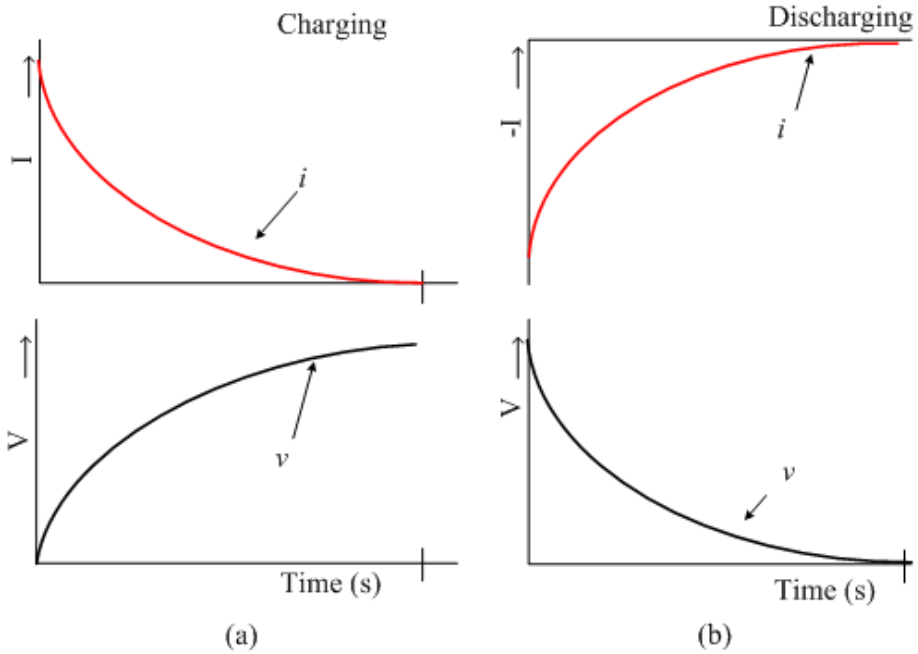


Figure 2.5: V and I: (a) charging curves, (b) discharging curves

Illustration of an ideal capacitor charge and discharge via a resistive load are in Fig. 2.4(a) and (b) respectively. When charging, the capacitor voltage increases as $V_p(1-e^{-t/\tau})$ and when discharging decay as $V_p(e^{-t/\tau})$ where V_p be the maximum voltage. When charging and discharging current decay as $I_0e^{-t/\tau}$. The related curves are illustrated in Fig. 2.5(a) and (b). The time constant $\tau = RC$ where R is the series resistive load in the circuit.

The work done to deliver a charge Q to an initially empty capacitor is given by,

$$E = \int_0^Q V(q)dq = \int_0^Q \frac{q}{C}dq = \frac{1}{2}\frac{Q^2}{C} = \frac{1}{2}VQ = \frac{1}{2}CV^2 \tag{2.3}$$

Power P is the time derivative of the stored energy E,

$$P = \frac{dE}{dt} = \frac{d}{dt}\left(\frac{1}{2}CV^2\right) = Cv(t)\frac{dV}{dt} \tag{2.4}$$

In an ideal capacitor, internal resistance (ESR) is neglected and we assume that the capacitor is 100% efficient. But in real devices, power dissipation in a capacitor arises from (i) equivalent series resistance, (ii) dielectric leakage, and (iii) dielectric hysteresis.

In a real capacitor, the impedance Z is given by Eq. (2.5); it can be increased at a particular frequency in AC as per terminal lead inductance L_{ESL} (equivalent series inductance—ESL). Impedance is,

$$Z = \sqrt{(R_{\text{ESR}})^2 + \left(\omega L_{ESL} - \frac{1}{\omega C}\right)^2} \tag{2.5}$$

where $\omega = 2\pi f$.

In DC circuits, impedance is nearly constant during both charging and discharging cycles. It defines the maximum current that can be drawn from the capacitor, therefore sets the minimum time constant. Dielectric leakage in Fig. 2.3(c) occurs due to the resistance of the insulator. It defines the maximum time constant and storage-time. A simplified equivalent circuit of a realistic capacitor is illustrated as in Fig. 2.3(b).

Dielectric hysteresis loss occurs when an alternating or pulse voltage with high slew rate is applied to the insulator [81]; losses are due to the electric field generated on dielectric and rapid reversals of orientation of randomly formed molecular dipoles. This formation changes with voltage and the dielectric properties which also depend on the temperature.

As the insulation resistance is extremely high, it is typically ignored in an ideal circuit. Dielectric hysteresis losses are also ignored in simple calculations of capacitor losses. Considering only resistive parasitics, in a non-ideal capacitor the parasitic energy loss scales as the square of the current through the ESR: at any given time t, the instantaneous dissipated power $P_{\text{loss}}(t)$ is,

$$P_{\text{loss}}(t) = \left(C\frac{dv(t)}{dt}\right)^2 R_{\text{ESR}} \tag{2.6}$$

Supercapacitors

Though the concept of supercapacitors was initiated and industrialized about 40 years ago, there was little research interest until the demand grew for enhanced energy storage

and short-term high-power bursts in certain electronic applications [75, 77, 82]. For example, battery-powered portable devices with volatile memory or alarm function require a separate backup power system of sufficient capacity to keep them alive until power is restored. Supercapacitors are being used to replace oversize batteries to power the memory and alarm systems during a temporary power failure [78].

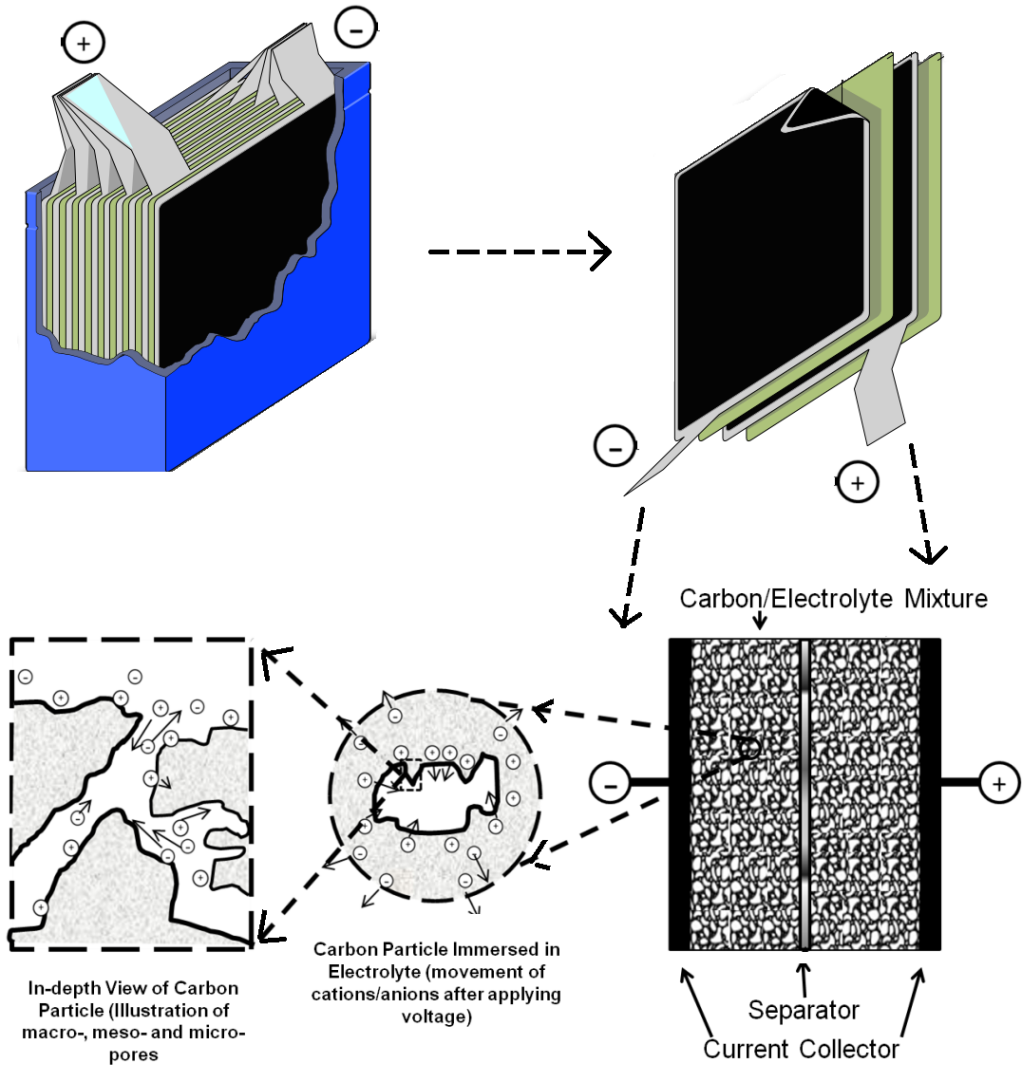


Figure 2.6: Electrochemical double layer capacitor [a modified version of [83]]

Supercapacitors or ultracapacitors are electric double-layer capacitors. The double-layer forms an interface between activated carbon and the electrolyte, allowing farad-order capacitance in a small volume [76, 84]. These two layers store electrical energy by electrostatic attraction and a small amount of redox ions in the electrolyte contribute to pseudocapacitance which arises from electrochemical action [84]. Activated carbon has high electrical conductivity and low production costs. Depositing activated carbon on electrodes creates highly distributed pores in contact with the electrolyte, resulting in extremely large surface areas and boosted capacitance. Single-cell supercapacitors are

available ranging in size from 0.2 to 5000 F. The energy density of a supercapacitor is about 1000 times larger than that of a standard electrolytic capacitor, and power density is about 10 times larger than electrochemical batteries [85]. Due to negligible chemical charge-transfer reactions, electrochemical capacitors have 100 times or longer charge-cycles than lithium batteries.

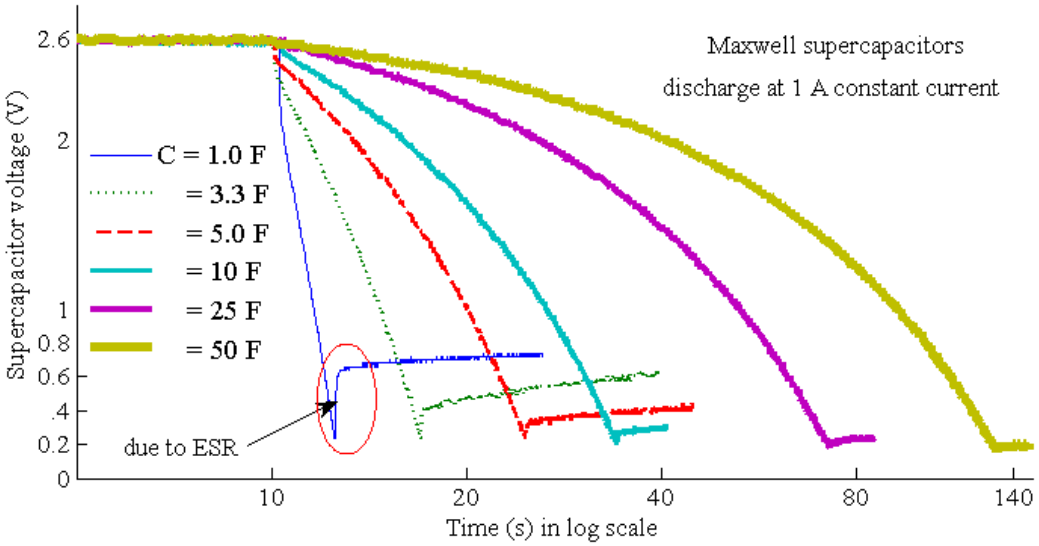


Figure 2.7: Different capacitors discharging at constant current

The equivalent-series resistance of a typical supercapacitor is in the milliohm (mΩ) range, thus can store and release energy quickly. The maximum power $P_{\mathrm{C}}^{\max}$ [86] of supercapacitors is given by,

$$P_{\mathrm{C}}^{\max} = \frac{V^2}{4R} \tag{2.7}$$

where V is the nominal working voltage and R is the ESR of the capacitor.

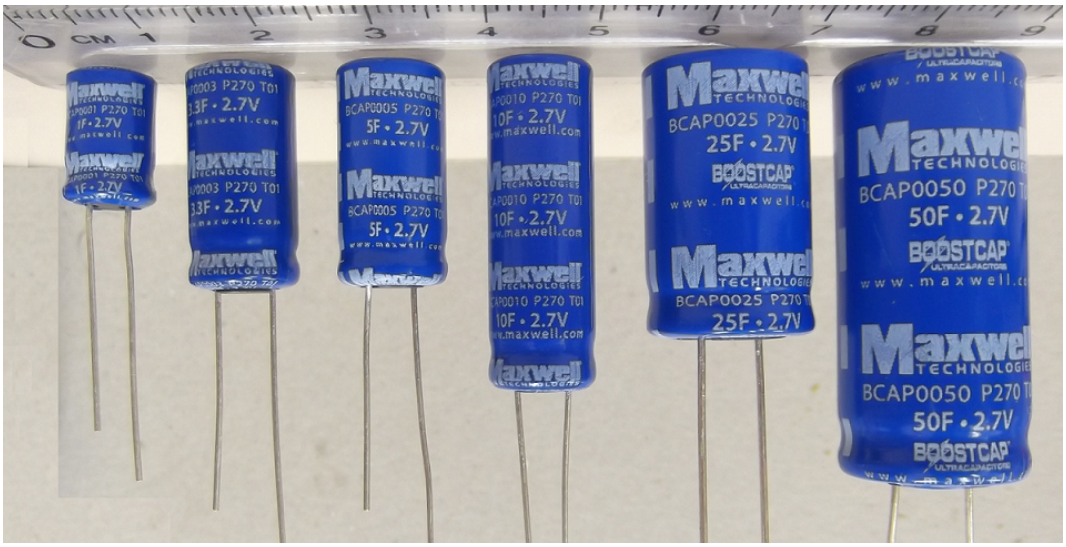


Figure 2.8: Size comparison of Maxwell BOOSTCAP capacitors

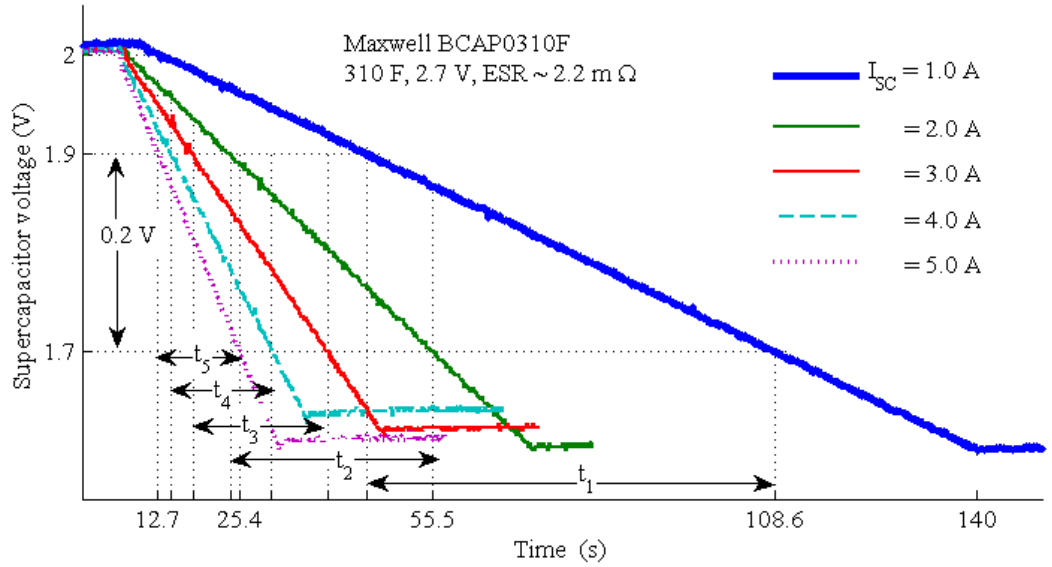


Figure 2.9: Maxwell 310 F supercapacitor discharging at different constant currents from 1 to 5 A and discharge time t to drop 0.2 V

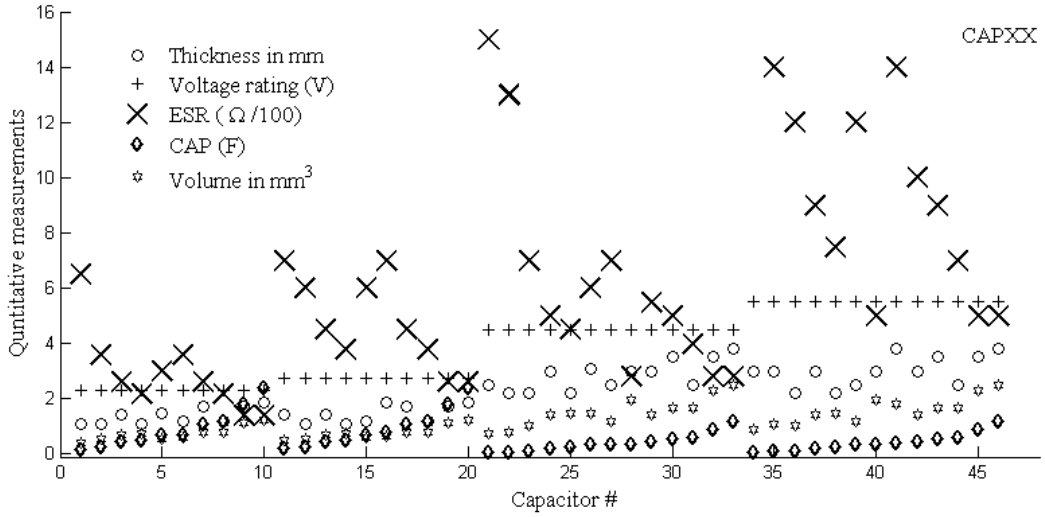


Figure 2.10: Thin profile CAPXX capacitors with their quantitative measurements (thickness, volume, voltage, capacity, and ESR)

Discharge curves of six different Maxwell capacitors at constant current 1 A are shown in Fig. 2.7. These capacitors range in size from 1 to 50 F. The ESR of these capacitors depends on capacity and physical size, being higher for smaller capacitors. Physical sizes are compared in Fig. 2.8. Figure 2.9 is an illustration of the variation of discharge time with different load currents. The time taken to drop 0.2 V voltage (from 1.9 to 1.7 V) for each current 1 to 5 A is given by t_1,..t_5 correspondingly: and for any constant current I_{SC} the time t_i is,

$$t_i = \frac{C\Delta V}{I_{SC}} \tag{2.8}$$

The operating voltage of a single-cell supercapacitor is limited by its electrolyte [78] and is usually <1 or <3 V per cell for aqueous or organic electrolytes, respectively [87]. At the early stages supercapacitors were prominent in low-voltage applications, but now are being used for higher-voltage applications as well [85, 86]. Volume and thickness are properties that a supercapacitor to use in new portable electronic devices. Forty six CAPXX capacitors [88] with their quantitative measurements (thickness, volume, voltage, capacity, and ESR) in Fig. 2.10, which are mostly use in mobile phones and cameras.

2.2 Supercapacitor voltage dropper

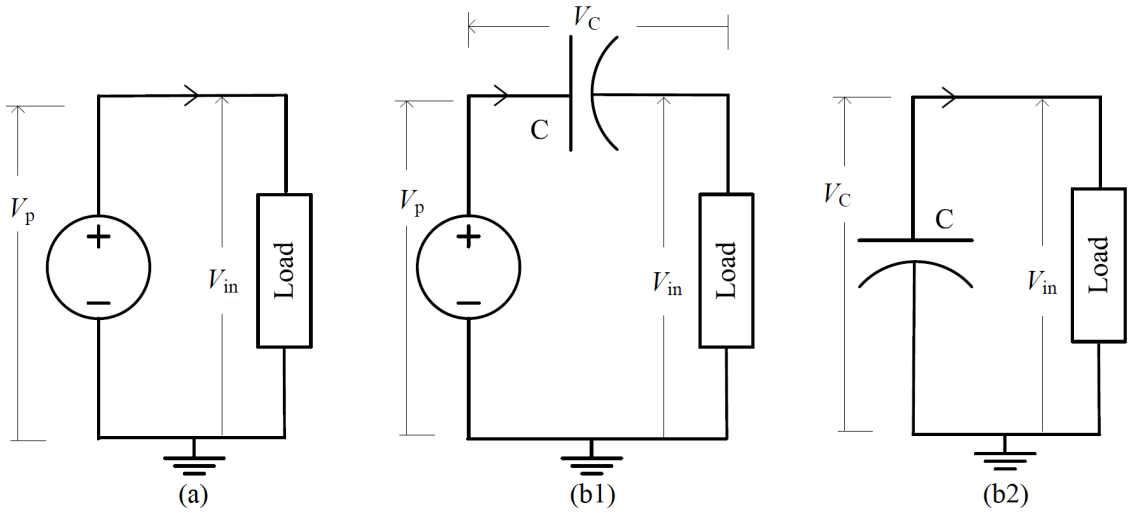


Figure 2.11: A DC-source powers a load: (a) without a capacitor, (b1) with a capacitor that charges in series for t_c time, (b2) charged capacitor powers the load for t_d time

The simplest way to power a DC-load is by connecting it to a DC source as illustrated in Fig. 2.11(a). In this configuration, the load V_{in} is equal to DC-source voltage V_p. In Fig. 2.11(a), the load draws the total energy supplied by the DC-source E_p,

$$E_p = QV_p = I^2Rt = IV_pt \tag{2.9}$$

where R is load resistance powered for time t.

However, it is important to maintain the DC-source voltage within the limits of load input voltage; minimum V_{in}^{min} and maximum V_{in}^{max},

$$V_{in}^{min} \leqslant V_p \leqslant V_{in}^{max} \tag{2.10}$$

If V_p varies beyond these limits, the load might be damaged permanently or it might cause to reduce the overall efficiency. When V_p is greater than the accepted maximum input of the load V_{in}^{max}, a capacitor can be connect in series with the source and the load to drop V_{in}.

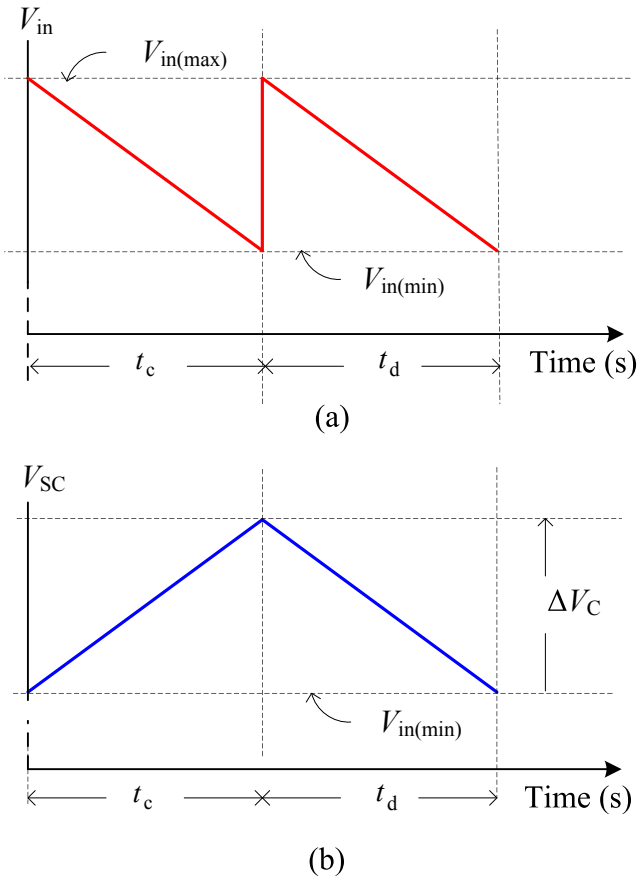


Figure 2.12: Voltages across load and supercapacitor under constant load: (a) input voltage of the load for times t_c and t_d, (b) corresponding supercapacitor voltage time-course

As shown in Fig. 2.11(b1), a higher voltage V_p drops to load input voltage V_{in} by connecting a pre-charged capacitor. Voltage in the capacitor V_C has to reduce the V_p to V_{in}. But, the V_C should not a cause to reduce the V_{in} less than minimum input voltage of the load V_{in}^{min} and it does not exceed it's maximum V_{in}^{max}. Therefore, the capacitor voltage V_C must lie in the range,

$$V_{in}^{min} \leqslant V_p - v_C(t) \leqslant V_{in}^{max} \tag{2.11}$$

If ideal components are used, the load input voltage in this new arrangement is equal to,

$$v_{in}(t) = V_p - v_C(t) \tag{2.12}$$

When the capacitor charges, the voltage V_C will increase while V_{in} decreases. For a constant current load I, these voltages will change linearly. At the beginning of charging phase ($t_{c,i}$), V_{in} is in its maximum; so, the capacitor voltage is,

$$V_C(t_{c,i}) = V_p - V_{in}^{max} \tag{2.13}$$

If the load reaches its minimum voltage at time $t1$, the changes in V_{in} and V_C is seen as in Fig. 2.12(a) and (b) respectively. At the end of charging ($t_{c,f}$), V_{in} can drop to its

minimum, then the capacitor voltage is,

$$V_{\mathrm{C}}(t_{\mathrm{c,f}}) = V_{\mathrm{p}} - V_{\mathrm{in}}^{\mathrm{min}} \tag{2.14}$$

In this case, the energy delivered from the power supply will be used by both the load and the capacitor,

$$E_{\mathrm{p}} = I^2 R t_{\mathrm{c}} + E_{\mathrm{C}}(t_{\mathrm{c}}) \tag{2.15}$$

where E_{C} is the energy stored by the capacitor during time t_{c} and is equal to,

$$E_{\mathrm{C}}(t_{\mathrm{c}}) = \frac{1}{2} C \left[\Delta V_{\mathrm{C}}(t_{\mathrm{c}})\right]^2 \tag{2.16}$$

where C is the capacitance.

The charged capacitor in Fig. 2.11(b) then disconnects from the source and connects to power the load as in Fig. 2.11(b2). So that,

$$v_{\mathrm{in}}(t) = v_{\mathrm{C}}(t) \tag{2.17}$$

Therefore, at the beginning of the charging, input voltage $v_{\mathrm{in}}(t)$ can be reached up to its maximum; so that capacitor voltage is,

$$V_{\mathrm{C}}(t_{\mathrm{d,i}}) = V_{\mathrm{in}}^{\mathrm{max}} = V_{\mathrm{C}}(t_{\mathrm{c,f}}) \tag{2.18}$$

When the load draws current, the capacitor discharges and reduces $v_{\mathrm{C}}(t)$, and so does the load voltage $v_{\mathrm{in}}(t)$. This can happen until the load reaches its minimum voltage (say for $t_{\mathrm{d,f}}$ time). So, at the end of time t_{d} the capacitor voltage is,

$$V_{\mathrm{C}}(t_{\mathrm{d,f}}) = V_{\mathrm{in}}^{\mathrm{min}} \tag{2.19}$$

The energy released at time t_{d} is given by,

$$E_{\mathrm{C}}(t_{\mathrm{d}}) = \frac{1}{2} C \left(\Delta V_{\mathrm{C}}(t_{\mathrm{d}})\right)^2 = I^2 R t_{\mathrm{d}} \tag{2.20}$$

The DC-source voltage V_{p} should be greater than twice of $V_{\mathrm{in}}^{\mathrm{min}}$. If $V_{\mathrm{p}} = 2\ V_{\mathrm{in}}^{\mathrm{min}}$, substituting to Eq. (2.14) we get,

$$V_{\mathrm{C}}(t_{\mathrm{c,f}}) = 2V_{\mathrm{in}}^{\mathrm{min}} - V_{\mathrm{in}}^{\mathrm{min}} = V_{\mathrm{in}}^{\mathrm{min}} \tag{2.21}$$

Therefore, there is no excess charges to release at discharging phase. To continue the capacitor charge-discharge process the excess energy stored in the capacitor during time t_{c} will release to the load during time t_{d}.

$$E_{\mathrm{C}}(t_{\mathrm{c}}) = E_{\mathrm{C}}(t_{\mathrm{d}}) \tag{2.22}$$

And also, the differential voltages of load and capacitor ΔV_{in} and ΔV_{C} are equal.

$$V_{\mathrm{in}}^{\mathrm{max}} - V_{\mathrm{in}}^{\mathrm{min}} = \Delta V_{\mathrm{in}} = \Delta V_{\mathrm{C}} \tag{2.23}$$

For a fixed constant current I, the charging and discharging times are equal ($t_c = t_d$). The charging frequency f_c,

$$f_c = \frac{1}{t_c} = \frac{1}{t_d} \tag{2.24}$$

Therefore, the operation frequency of capacitor based voltage-dropper circuit in Fig. 2.11(b) and (c) will be,

$$f_{op} = \frac{1}{(t_c + t_d)} \tag{2.25}$$

Substituting (2.24) in (2.25), we can find f_{op} is only half of f_c.

$$f_{op} = \frac{1}{(t_c + t_d)} = \frac{1}{2t_c} = \frac{1}{2} f_c = \frac{I}{2C\Delta V_C} \tag{2.26}$$

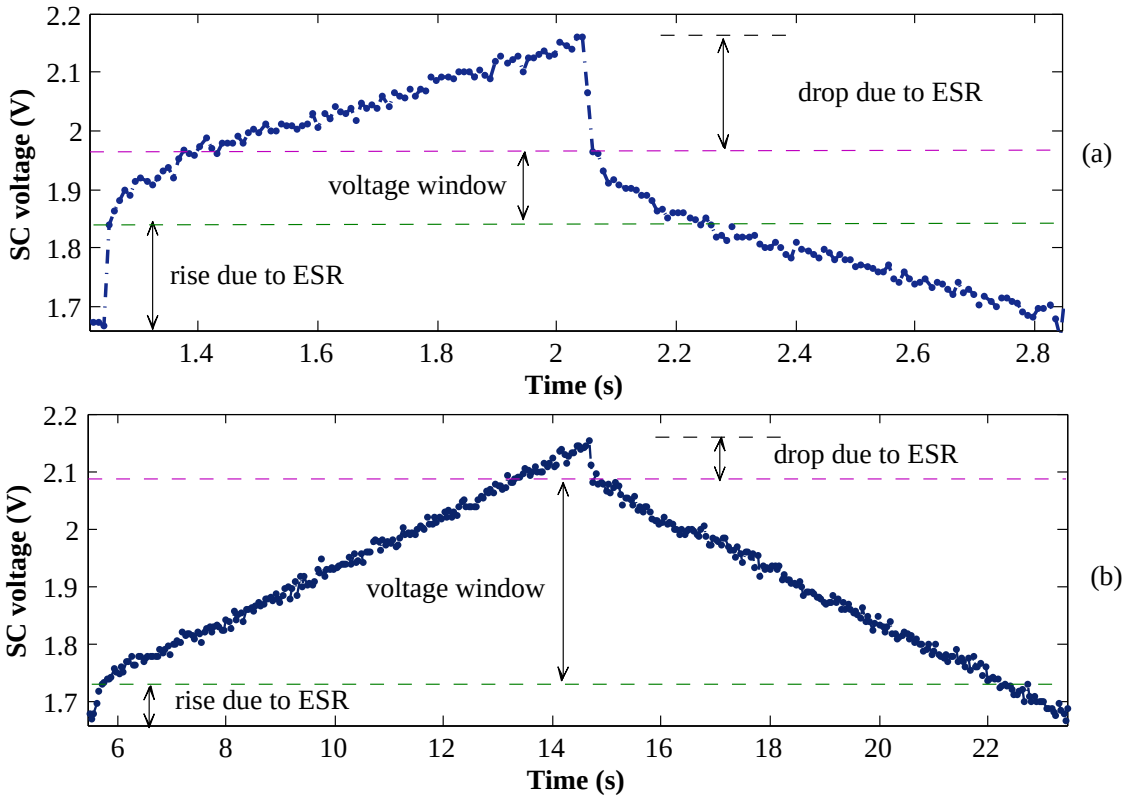


Figure 2.13: Voltage window of a charge-discharge cycle, ESR and capacitance vs. time: (a) 1 F, 600 mΩ capacitor, (b) 5 F, 170 mΩ capacitor at 300 mA

When a large capacitor is used in this configuration, it can power the load for a considerable time during charge-discharge phases. So, the frequency of operation ($f_{op} = I/2C\Delta V_C$) will be very low. If non-ideal capacitors are used, ΔV_C should be greater than IR_{ESR} to satisfy Eq. (2.26). Two Maxwell supercapacitors (1 F, 600 mΩ and 5 F, 170 mΩ) in Fig. 2.13 illustrates ESR effect on variation of voltage window. Maximum voltage window is

$$\Delta V_C^{max} = V_{in}^{max} - V_{in}^{min} - 2Ir_c \tag{2.27}$$

where r_c is ESR of the supercapacitor. Supercapacitors with low ESR are ideal to use as lossless voltage-droppers due to their high capacitance. This is the fundamental idea behind *supercapacitor energy recovery technique* based converters [1].

In synopsis, energy released by a battery to a capacitor can be recovered by releasing to a useful load while maintaining overall charge balance across multiple cycles. By using a low-dropout regulator before the input of the load, this supercapacitor-energy-recovery technique become a voltage regulator known as SCALDO. This arrangement overcomes the efficiency limitation of a linear regulator and improves the end-to-end efficiency of the overall converter.

2.3 SCALDO regulators and their topologies

Given the advantages of supercapacitors, the University of Waikato research team used a pre-charged supercapacitor as a lossless voltage-dropper with a specific arrangement to improve the efficiency of a linear regulator. Low-dropout regulators (LDO) are used to address the low efficiency issue in linear regulators. However, the LDO needs to maintain very small voltage-difference between input and the output to achieve high efficiency. These ideas are applicable to any output current range, and are supported by experimental measurements from proof-of-concept prototype converters. Early prototypes built for 12-to-5 V converters achieved overall efficiencies in the range of 78–80% [6].

A generalized model of the patented SCALDO technique [6] is shown in Fig. 2.14. At the charging stage in Fig. 2.14(b), the supercapacitor is connected in series with a linear regulator. Here, $v_{\text{in}}(t)$ and V_{reg} are LDO input voltage at time t and the regulated output voltage respectively. The supercapacitor drops supply voltage V_{p} to the LDO input voltage v_{in}, acting as a lossless voltage-dropper between the source and LDO input while storing energy to be used in the discharge phase. At the end of charging v_{sc} has increased to maximum value $V_{\text{sc}}^{\text{max}}$ that should be equal to $V_{\text{in}}^{\text{max}}$. When discharging, the supercapacitor delivers energy to the LDO until its terminal voltage drops to the minimum input voltage $V_{\text{in}}^{\text{min}}$ tolerated by the LDO. In SCALDO, this voltage is usually a system-defined constant: the minimum value is $V_{\text{reg}} + V_{\text{do}}$ where V_{do} is the minimum dropout voltage. If there is no ground current, the LDO efficiency η_{LDO} is expressed as,

$$\eta_{\text{LDO}} = \frac{V_{\text{reg}} I_{\text{L}}}{V_{\text{in}} I_{\text{L}}} = \frac{V_{\text{reg}}}{V_{\text{in}}} = \frac{V_{\text{reg}}}{V_{\text{reg}} + V_{\text{do}}} = \left(\frac{1}{1 + \frac{V_{\text{do}}}{V_{\text{reg}}}} \right) \tag{2.28}$$

Efficiency of the LDO can be increased by maintaining the input voltage $v_{\text{in}}(t)$, closer to regulated output voltage V_{reg}. The circuit draws power from the unregulated input only half the time of its operating period: during the charging phase the supercapacitor draws current from the unregulated supply, whereas during discharge phase, it delivers power to the circuit without relying on the unregulated power supply [4]. If ideal components are

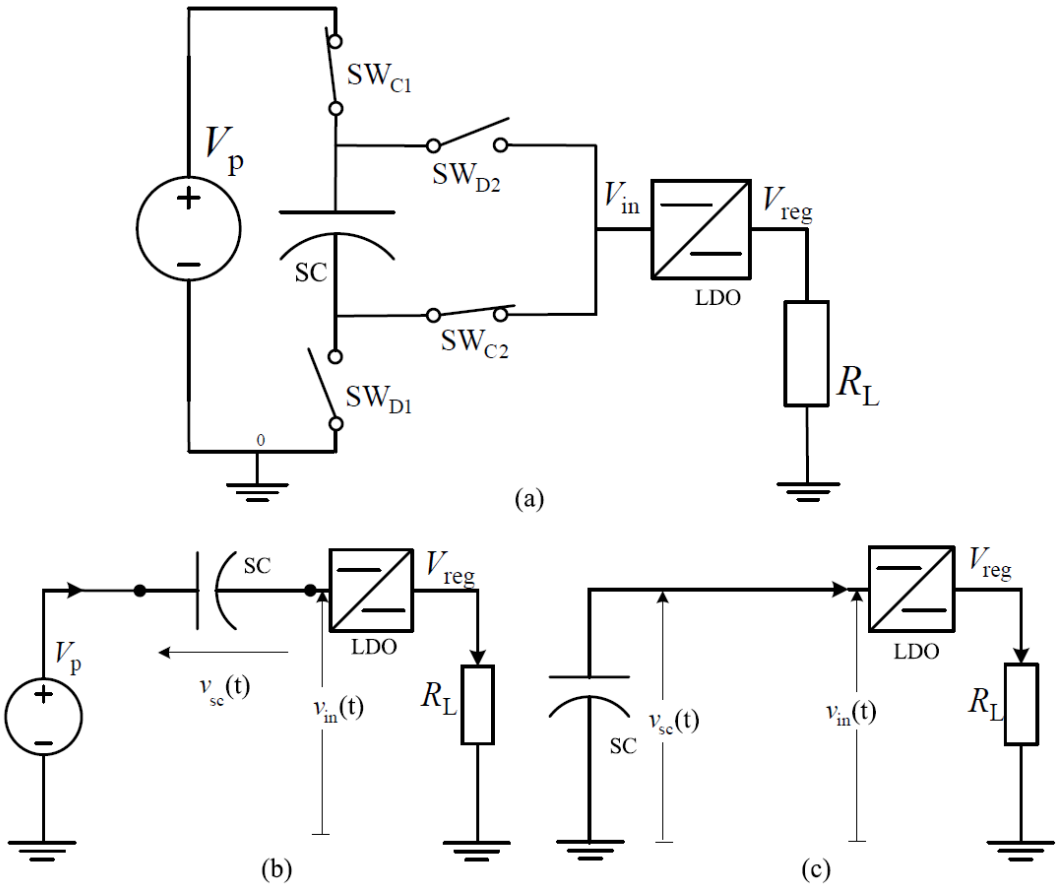


Figure 2.14: Basic SCALDO: (a) basic topology (12-to-5 V like configuration), (b) SC-charging phase, and (c) SC-discharging phase

used in the circuit, the end-to-end efficiency of the SCALDO in Fig. 2.14 is approximately equal to the efficiency of LDO,

$$\eta_{\text{LDO}} \approx \eta_{\text{SCALDO}} = \frac{V_{\text{reg}} I_{\text{L}}}{V_{\text{p}} I_{\text{L}}/2} = 2\frac{V_{\text{reg}}}{V_{\text{p}}} \tag{2.29}$$

For different input-to-output voltage requirements of SCALDO regulators, the supply voltage V_{p} can be either greater or smaller than twice of the output voltage $V_{\text{in}}^{\text{min}}$. For a 12-to-5 V case, one supercapacitor capable of dropping ~7 V is required. Practical implementation would use three series-connected capacitors with cell voltage of about 2.7 V. These capacitors are always connected in series during both charging and discharging phases, so can be treated as a single capacitor. Switch connections between unregulated power supply and the capacitor change the supercapacitor-LDO circuit configuration from series to parallel at a very low frequency, of order 100 Hz. Details and variations of the basic technique are available in [4, 5].

However, for a 5-to-1.5 V regulator where V_{p} is larger than twice the $V_{\text{in}}^{\text{min}}$, we require two capacitors in series when charging. And when discharging they connect in parallel. This SCALDO topology in Fig. 2.15 required seven switches to change between charge and

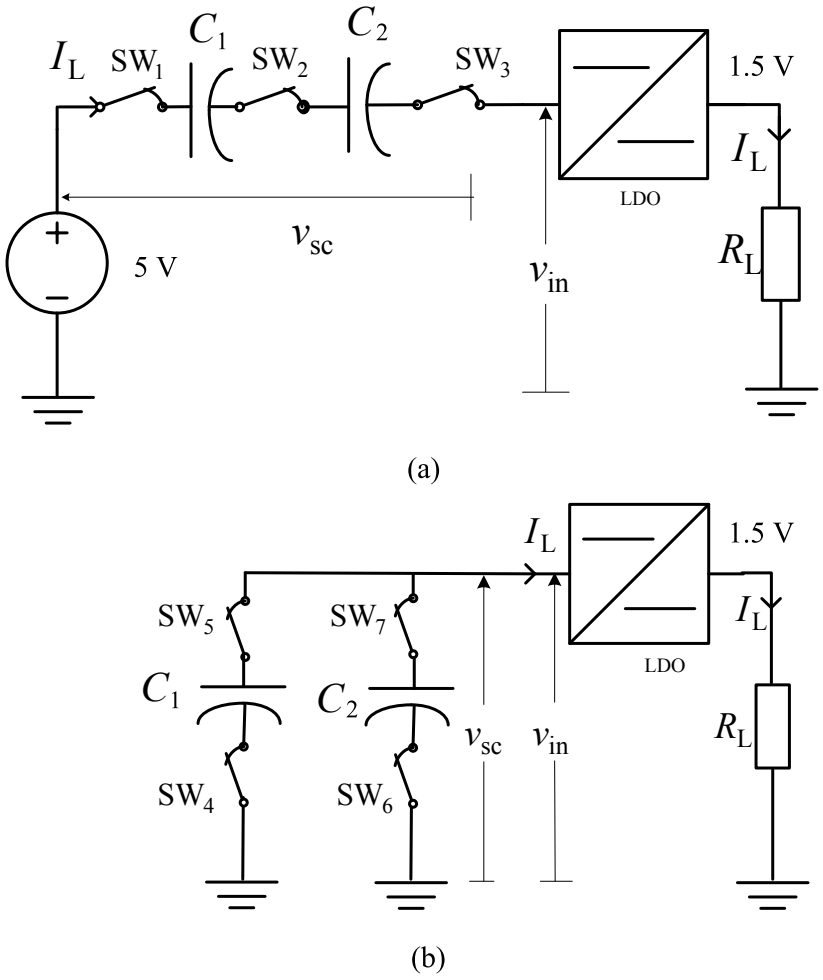


Figure 2.15: 5-to-1.5 V SCALDO: (a) SC-charging configuration, and (b) SC-discharging configuration

discharge configurations. The time taken for charging is twice that for discharging. The measured end-to-end efficiency of the 5-to-3.3 V converter was around 75-88% achieved close to its theoretical efficiency of 90% [6],

$$\eta = 3\frac{V_{\text{reg}}}{V_{\text{p}}} = 3\frac{1.5}{5} = 90\% \quad \text{for 5-to-1.5 V SCALDO regulator} \tag{2.30}$$

For other SCALDO regulators such as 5-to-3.3 V where V_{p} is less than twice $V_{\text{in}}^{\text{min}}$, three capacitors in series are required when discharging, but they are paralleled when charging. Ten switches are needed to change between charge and discharge configurations as illustrated in Fig. 2.16. The actual end-to-end efficiency of 5-to-3.3 V ranged from 75 to 83%, almost matching the theoretical efficiency [6],

$$\eta = \frac{4}{3}\frac{V_{\text{reg}}}{V_{\text{p}}} = \frac{4}{3}\frac{3.3}{5} = 88\% \quad \text{for 5-to-3.3 V SCALDO regulator} \tag{2.31}$$

The three SCALDO circuits (12-to-5 V, 5-to-3.3 V and 5-to-1.5 V) were considered to develop the generalized theory of SCALDO to find (i) the theoretical end-to-end efficiency,

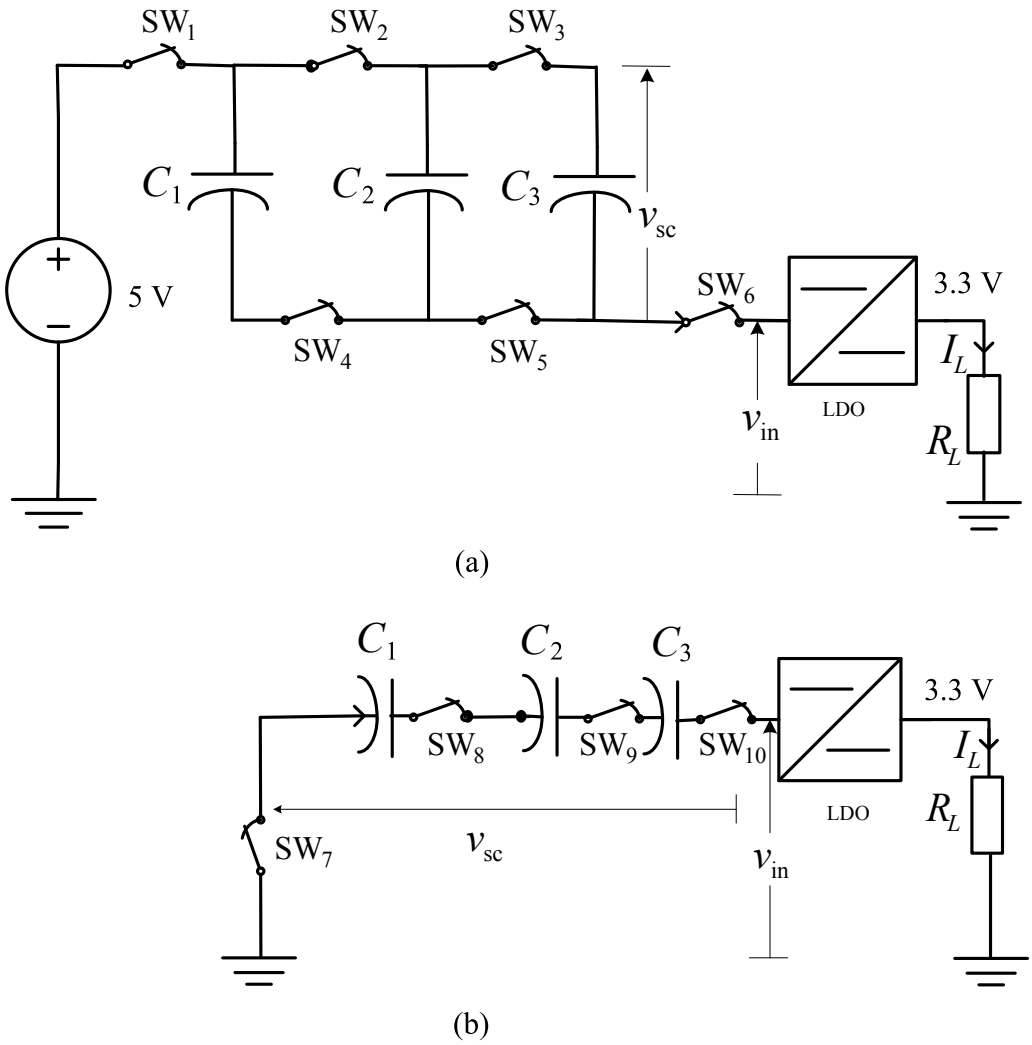


Figure 2.16: 5-to-3.3 V SCALDO: (a) SC-charging configuration, and (b) SC-discharging configuration

(ii) minimum number of capacitors required, (iii) number of switches required for a given input-to-output voltage requirement. A comparison of linear regulator efficiencies for these three SCALDO configurations is presented in Table 2.1. More detailed loss analysis of SCALDO will be considered in Chapter 3.

2.4 General theory of SCALDO

General theory was developed after implementing four SCALDO circuits (12-to-5 V, 5-to-1.5 V, 5-to-3.3 V and 5-to-2 V). The 5-to-2 V case is similar to that for 12-to-5 V as the efficiency improvement factor is the same, i.e., 2. The theoretical end-to-end efficiency is expressed as,

$$\eta = \frac{V_{\mathrm{reg}} I_{\mathrm{L}} (t_c + t_d)}{V_{\mathrm{p}} I_{\mathrm{L}} t_c} = \frac{V_{\mathrm{reg}} (t_c + t_d)}{V_{\mathrm{p}} t_c} = \left(1 + \frac{t_d}{t_c}\right) \frac{V_{\mathrm{reg}}}{V_{\mathrm{p}}} \tag{2.32}$$

For charging time t_c and discharging time t_d, energy delivered by the power supply at constant current I_L is equal to $V_p I_L t_c$ and the load absorbed $V_{reg} I_L (t_c + t_d)$. The number of switches used in the original SCALDO is equal to $3n + 1$ where n is the number of supercapacitors required for a particular configuration.

In the SCALDO operation, supercapacitors have two functions (i) store charges, and (ii) release them on demand of the load. They should maintain the charge balance. Therefore, there are two operating phases, i.e., charging and discharging. At any of the phases, supercapacitors can connect either in series or parallel to store or release charges. Therefore, there are four ways this can occur with the supercapacitors that connect in:

1. series during both charge and discharge phases
2. parallel during both charge and discharge phases
3. series during charge phase and discharge in parallel
4. parallel during charge phase and discharge in series

The 1st and 2nd occurrences, supercapacitors are acting as a single capacitor in both charge and discharge phases, where $n = 1$. With the theoretical aspect taken into account, there are three general cases for SCALDO:

1. For a single capacitor takes t_c and t_d time respectively to store charges $I_L t_c$ and to release them $I_L t_d$. Since the stored and released charges are equal, times $t_c = t_d$. Therefore, end-to-end efficiency equals is,

$$\eta = \left(1 + \frac{t_d}{t_c}\right) \frac{V_{reg}}{V_p} = 2\frac{V_{reg}}{V_p} \tag{2.33}$$

2. For cases that required n capacitors to be charged in series and discharged in parallel (CSDP): total charge stored in the capacitors equals n times charge stored in a single capacitor (assuming that the capacitors are identical). In this case, $t_d = nt_c$. Therefore, end-to-end efficiency is,

$$\eta = \left(1 + \frac{t_d}{t_c}\right) \frac{V_{reg}}{V_p} = \left(1 + \frac{nt_c}{t_c}\right) \frac{V_{reg}}{V_p} = (1 + n)\frac{V_{reg}}{V_p} \tag{2.34}$$

where the number of capacitors required is,

$$n = \frac{\left(V_p - V_{in}^{min}\right)}{V_{in}^{max}} \tag{2.35}$$

3. For cases charging n capacitors in parallel then discharging them in series—(CPDS): charge stored in one capacitor equals $1/n$ of total stored charge. In this case, $t_c = nt_d$. Therefore, end-to-end efficiency is,

$$\eta = \left(1 + \frac{t_d}{t_c}\right) \frac{V_{reg}}{V_p} = \left(1 + \frac{t_c}{nt_c}\right) \frac{V_{reg}}{V_p} = \left(1 + \frac{1}{n}\right) \frac{V_{reg}}{V_p} \tag{2.36}$$

and capacitor count is,

$$n = \frac{V_{in}^{max}}{\left(V_p - V_{in}^{min}\right)} \tag{2.37}$$

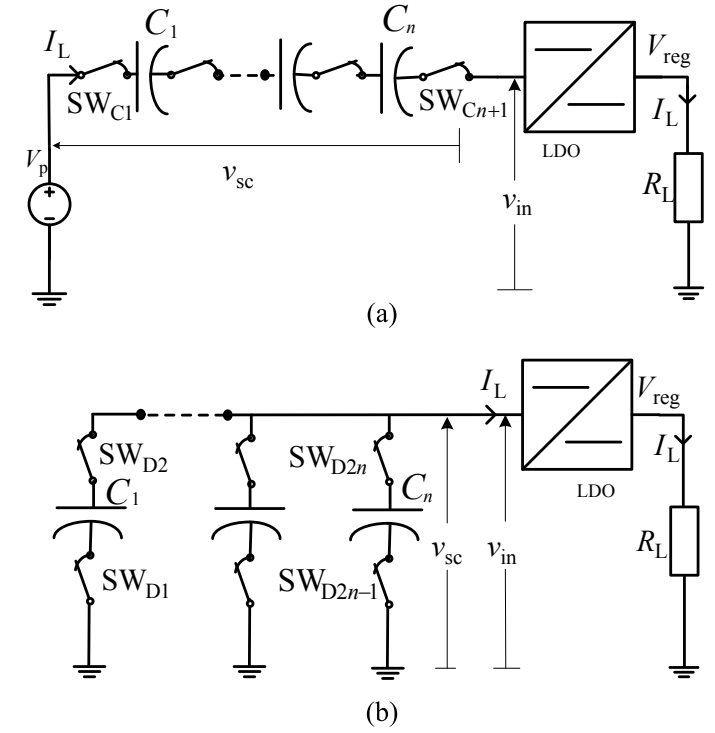


Figure 2.17: General SCALDO-CSDP: (a) supercapacitor-charging configuration, and (b) supercapacitor-discharging configuration

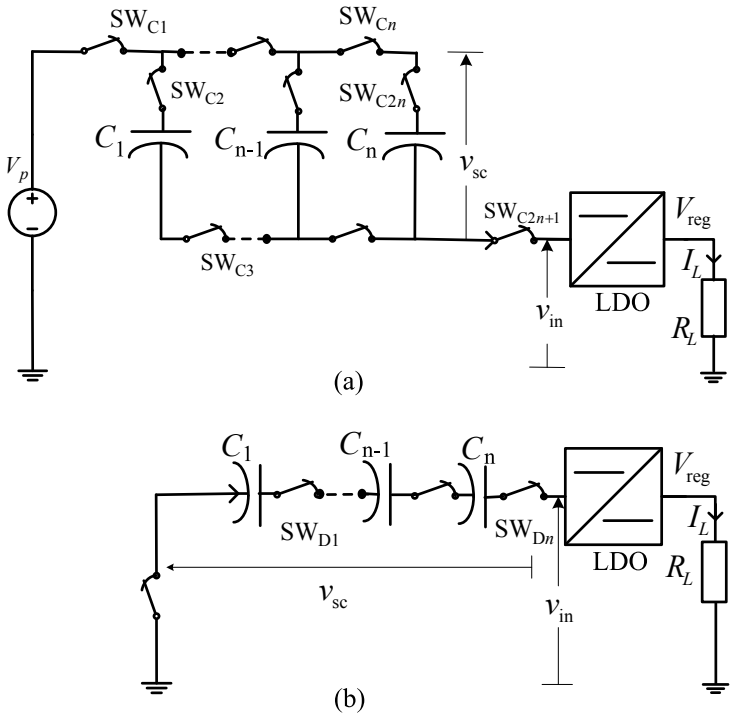


Figure 2.18: General SCALDO-CPDS : (a) supercapacitor-charging configuration, and (b) supercapacitor-discharging configuration

With different input-to-output voltage requirements the number of capacitors required will be different. Considering the above three basic cases, the SCALDO can be generalized to two main configurations with n capacitors (i) charging in series and discharging in

Table 2.1: Comparison of different linear regulators with SCALDO configurations

Converter configuration	**12-to-5 (V)**	**5-to-1.5 (V)**	**5-to-3.3 (V)**
Theoretical maximum efficiency of linear regulator	42%	30%	66%
SCALDO requirement	$V_{\mathrm{p}} > 2V_{\mathrm{in}}^{\mathrm{min}}$	$V_{\mathrm{p}} > 3V_{\mathrm{in}}^{\mathrm{min}}$	$V_{\mathrm{p}} < 2V_{\mathrm{in}}^{\mathrm{min}}$
Number of supercapacitors	1	2	3
Number of switches $(3n+1)$	4	7	10
Efficiency improvement factor $(1+k)$	(1+1) = 2	(1+2) = 3	(1+1/3) = 1.33
Theoretical maximum efficiency	84%	90%	88%
Measured achieved maximum efficiency	80%	88%	83%

parallel (CSDP) in Fig. 2.17 and (ii) charging in parallel and discharging in series (CPDS) in Fig. 2.18.

The theoretical end-to-end efficiency of SCALDO can be compared to that of a traditional series regulator $V_{\mathrm{reg}}/V_{\mathrm{p}}$ with a multiplication factor $(1+k)$ where k is equal to $(t_{\mathrm{d}}/t_{\mathrm{c}})$. Also SCALDO efficiency is related to the number of capacitors n required for a configuration. For, SCALDO-CSDP, $k = n$ and SCALDO-CPDS, $k = 1/n$. According to SCALDO theory, theoretical end-to-end efficiency is,

$$\eta = (1+k)\frac{V_{\mathrm{reg}}}{V_{\mathrm{p}}} \tag{2.38}$$

2.5 Application of SCALDO in wider areas

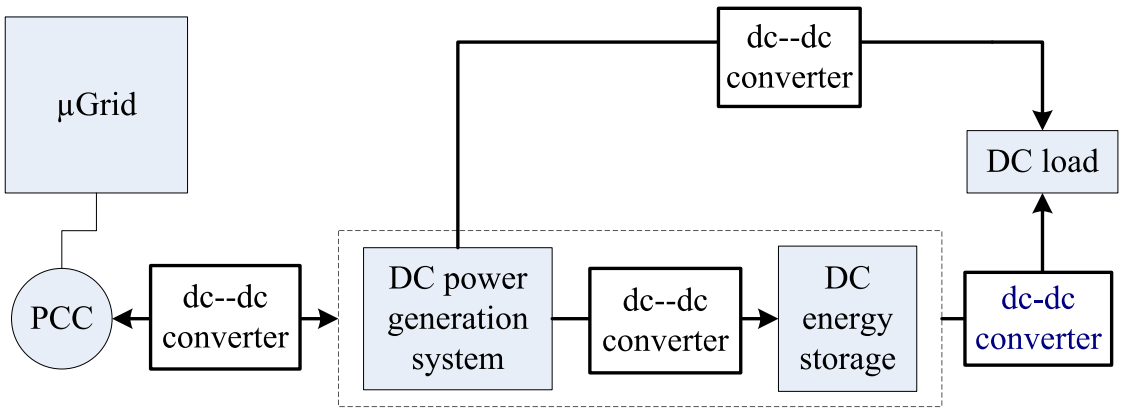


Figure 2.19: DC-microgrid components and its connection via point of common coupling (PCC) with DC-DC converters [89]

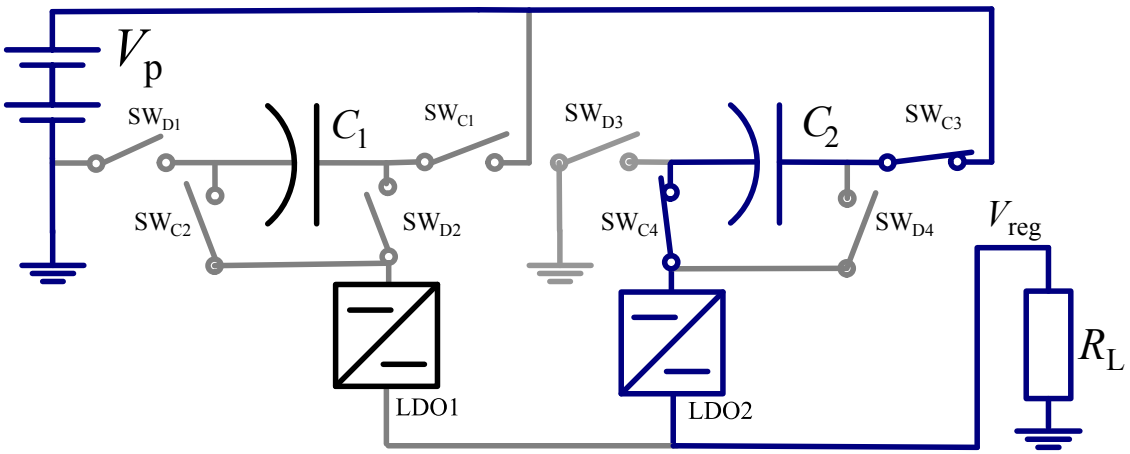


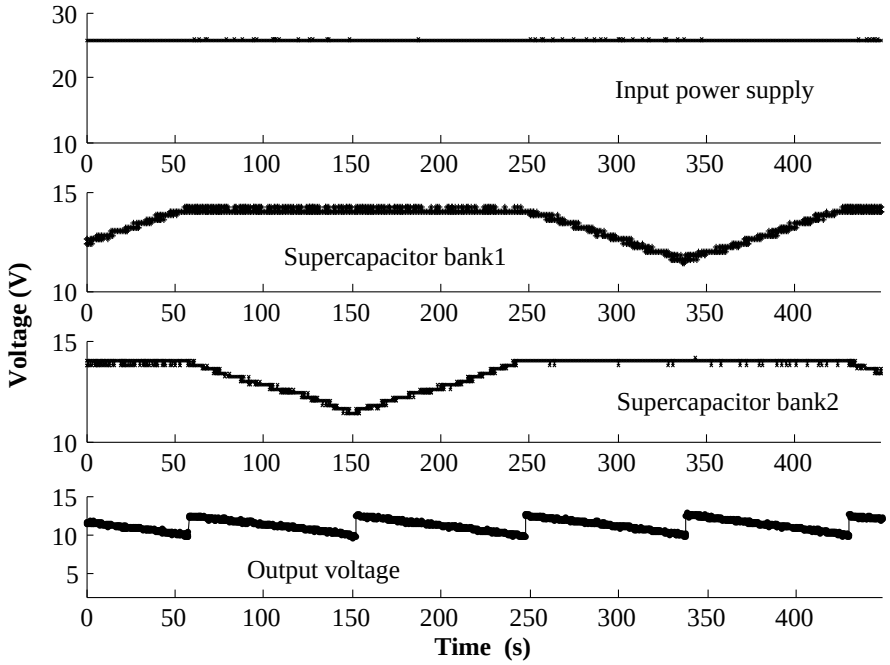
Figure 2.20: Application of SCALDO: Micro-grids lighting system with two parallel SCALDOs that operate alternately to provide UPS-capability

The supercapacitor-assisted low dropout regulators are free of electromagnetic interference issues, have low-noise, and are less complex than other DC–DC converter designs. The SCALDO topology is flexible to modify without breaking its basic concept. Therefore, these novel DC–DC converters can be used in a variety of electronic applications which require voltage step-down and regulation at high efficiency. Supercapacitors in SCALDOs can buffer against temporary power failures by functioning as uninterrupted power supplies (UPS) offer suitable changes to the topology and control signals.

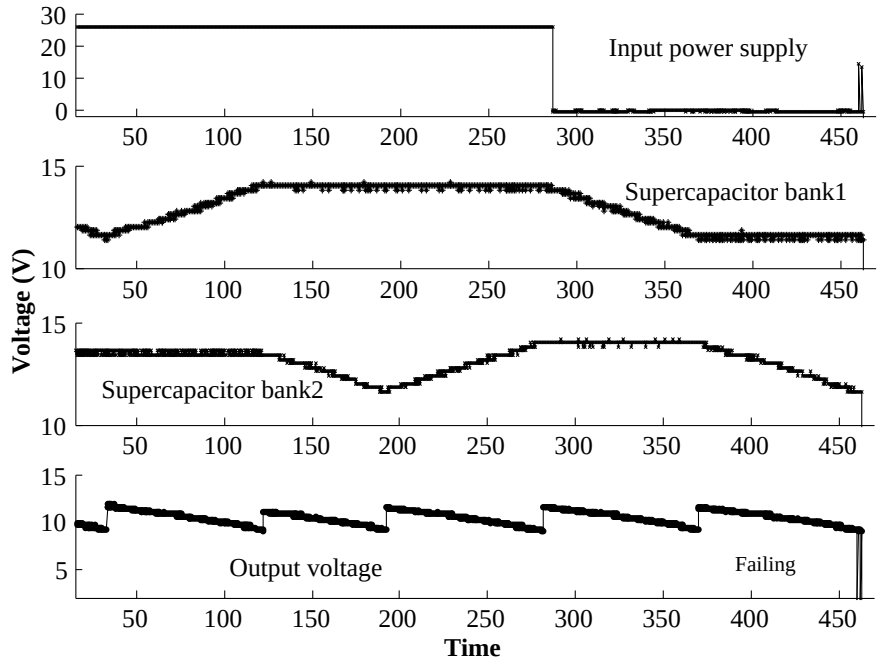
For the last few decades the applications that use renewable DC-energy sources were expanded from a simple solar powered calculator to industry level appliances such as servers in data centers [89]. Due to the proliferation of appliances with power electronic converters and DC buses within the systems, it is very practical and more energy efficient to use DC-sources to power them. This scenario encourages the implementation of DC-powered systems from standalone to grid level. Fig. 2.19 illustrates the connectivity of components via DC-DC converters in a typical DC-microgrid (DCμG) [89] and the options for energy storage.

With emergence of DC-power generators (such as photovoltaic PV) solar systems and wind power generators), storage devices (fuel cells, batteries and supercapacitors) and DC-loads, DC–DC conversion is becoming an increasingly important element in these power systems. When DC-loads are powered by a DCμG based on a renewable source such as a PV system, energy storage becomes mandatory due to fluctuating nature of the source [90–92]. Localized DC-energy storage within DC–DC converters can realize this requirement. A variation of SCALDO can provide localized energy storage with low-noise and fast transient response. A prototype of supercapacitor-assisted regulators was developed for solar-powered LED lighting [93].

This experiment was set to test two parameters; (i) autonomy of the DC-converter when input power source is disconnected, and (ii) brightness of the bulb during acceptable



(a)



(b)

Figure 2.21: UPS-capable SCALDO: (a) at normal operation with barely regulated output that did not degrade the brightness of the LED. No output or buffer capacitors were required for this experiment, (b) loss of input supply power and activation of DC-UPS capability

voltage fluctuations. The linear regulator used in this experiment is L7812CV STMicroelectronics which can convert a maximum of 24 V to 12 V. It has a minimum dropout

of 2 V. In the test setup, output voltage was varied in theoretical working range of LED to hold the brightness at constant. This was done by setting the system specified input voltage of SCALDO below the required minimum value for regulation. The variation of output can be seen as in Fig. 2.21.

In Fig. 2.20, two basic SCALDOs are connected in parallel to alternative in powering the lighting load R_{L}. To implement UPS capability using SCALDO, supercapacitors C_1 and C_2 are alternately charged and discharged in a way that keeps one supercapacitor (or supercapacitor bank) on standby at any given time. At in an interrupt situation the standby supercapacitor can serve the load without delay. More information related to this application is available in [93] and the digital control program is available in Appendix B.

Initially one supercapacitor in SCALDO (say C_1) charges to a system defined voltage $V_{\mathrm{in}}^{\mathrm{min}}$ and provide autonomy until the other supercapacitor (C_2) in second SCALDO charges. Then the first C_1 starts to discharge until LDO input voltage reaches $V_{\mathrm{in}}^{\mathrm{min}}$ and begins charging again. Once C_1 has completed a discharge-charge cycle, C_2 begins its discharging-charging cycle. This operation repeats by keeping a standby supercapacitor at any given time.

In both the charging and discharging phases, the input voltage of the linear regulator reduces until it reaches the system specified minimum voltage. In this case, the minimum voltage was specified as 11.4 V. The change in $V_{\mathrm{p}} - V_{\mathrm{sc}}$ is reflected in output voltage V_{reg}. It was found that this fluctuation in the linear regulator output did not affect the brightness of the bulb.

In an interrupt situation, and at a worse case scenario where a supercapacitor at the beginning of the charging cycle remains at minimum voltage level since there is no supply, the system lets the second supercapacitor discharge. By the end of this discharging cycle, the load starts to indicate that it has reached a critical level. The minimum time to reach the critical condition is equal to time of one discharging cycle of the supercapacitor and the maximum time doubles this value. This is four times larger than charging frequency of SCALDO. So with large supercapacitors the system can supply power for a couple of minutes uninterruptedly until the main supply becomes available again.

Fig. 2.21(a) depicts the normal operation where supercapacitors are switching discharge-charge within about 188 seconds. The Fig. 2.21(b) indicates the situation of lost input supply. Under this condition, the supercapacitors in the SCALDO configuration allow for a UPS autonomy time varying from a minimum of 110 seconds to a maximum of 220 seconds approximately for a case of 16.67 F capacitor bank. By increasing the size of the supercapacitor-bank autonomy time can be increased [93].

It is clear that SCALDO has the flexibility to be customized for different applications. However, the number of switches is a technical barrier to use in high current implementations. Switch minimization is investigated and addressed in the next chapter.

Chapter 3

Reducing the switch count in SCALDO topology

In this chapter, I describe how the supercapacitor-assisted low dropout regulator (SCALDO) topology can be transformed to a new reduced-switch version with the judicious elimination of some switches. I detail a theoretical approach to design a reduced-switch SCALDO (RS-SCALDO), discuss development of an initial proof-of-concept prototype and describe its limitations.

3.1 Basis for reduced switch-count based SCALDO

The main reasons to reduce the number of switches in SCALDO are (i) the circuit complexity due to large number of switches in a general topology, and (ii) power losses that can be incurred due to those switches. However, only static losses dominates in this case compared to both dynamic and static losses present in high-frequency power supplies. The dynamic losses increase with frequency in a switching power supply, where as a SCALDO converter operates at extra low frequencies [63]. As discussed in the previous chapter, in a SCALDO design a pre-charged supercapacitor (SC) is used as a voltage-dropper between an unregulated DC-power supply and an efficient LDO. This arrangement extends the input-to-output voltage difference and maintains a high end-to-end efficiency close to that of the LDO.

The losses incurred in a SCALDO configuration arise from:

1. overall ground current in the control circuit
2. paralleling of two capacitors (SC and the buffer capacitor at LDO input side)
3. equivalent series resistance (ESR) in the SCs
4. ON-resistance of switches

In previous publications [5,6,94], losses in the basic SCALDO technique are discussed. In SCALDO theory, pass-element loss tends to be very low and defines the overall efficiency. When the LDO control circuit losses are negligible, the approximate efficiency at

constant current is given by,

$$\eta_{\mathrm{LDO}} = \frac{V_{\mathrm{reg}}}{V_{\mathrm{in}}} = \frac{V_{\mathrm{reg}}}{V_{\mathrm{reg}} + V_{\mathrm{do}}} = \frac{1}{1 + \frac{V_{\mathrm{do}}}{V_{\mathrm{reg}}}} = \frac{1}{1 + \frac{r_{\mathrm{on}}}{R_{\mathrm{L}}}} \tag{3.1}$$

where R_{L} and r_{on} are the instantaneous load resistance and the pass-element resistance respectively. For high SCALDO efficiency, we require very small r_{on} where $r_{\mathrm{on}} \ll R_{\mathrm{L}}$.

The SCALDO control circuit consists of a microcontroller (a peripheral interface controller PIC from Microchip Technology), LDO feedback circuit, switch control circuit. The PIC16fX series controllers used in SCALDO draw very small operational currents (typically 8.5 μA at 32 kHz and 100 μA at 1 MHz at 2 V) and its absolute maximum power dissipation is 800 mW and the standby current is 1 nA at 2 V. The LDO [95] used in 5-to-2 V SCALDO has a low ground current of about 2 mA for a maximum load of 1 A. The switches are solid-state relays [96], consuming 0.4 mA at off-state and approximately 20 mA when operating at 5 V. By developing a low-power control circuit compared to full load, the losses can be kept at an acceptable level. This ensures that the ultimate efficiency of the overall circuit does not deviate too much from theoretical prediction in Eq. (1.7).

Let us consider the basic SCALDO with one SC and four switches. Most common resistive losses in this configuration are considered as in Fig. 3.1. When charging the SC as in Fig. 3.1(a) energy losses are due to,

1. the internal resistance r_{p} of the unregulated power source V_{p}
2. ON-resistance R_{sw1} of switch 1 that connects the power supply to the SC
3. ESR of SC r_{c}
4. ON-resistance R_{sw2} of switch 2 that connects the SC to the LDO
5. ESR of buffer capacitor r_{b} at LDO input
6. LDO ON-resistance r_{on}

During the operation of SCALDO the SC is placed in parallel with the LDO in the discharging phase as in Fig. 3.1(b). A buffer capacitor might be required at the input of the LDO stage to maintain load current continuity during the transition from series to parallel phase. If so, losses will be incurred when the two capacitors (with slightly different voltages) come in parallel. Approximate loss when paralleling two capacitors of different voltages is given by,

$$E_{\mathrm{loss}} = \frac{1}{2}\frac{C_{\mathrm{sc}}C_{\mathrm{b}}}{C_{\mathrm{sc}} + C_{\mathrm{b}}}(v_{\mathrm{c}} - v_{\mathrm{b}})^2 \tag{3.2}$$

where v_{c} and v_{b} are respectively the SC and the buffer capacitor voltages at the time of paralleling; C_{c} and C_{b} are their capacitances. However, if C_{b} is much smaller than the SC capacitance, the loss,

$$E_{\mathrm{loss}} \approx \frac{1}{2}C_{\mathrm{b}}(v_{\mathrm{c}} - v_{\mathrm{b}})^2 \tag{3.3}$$

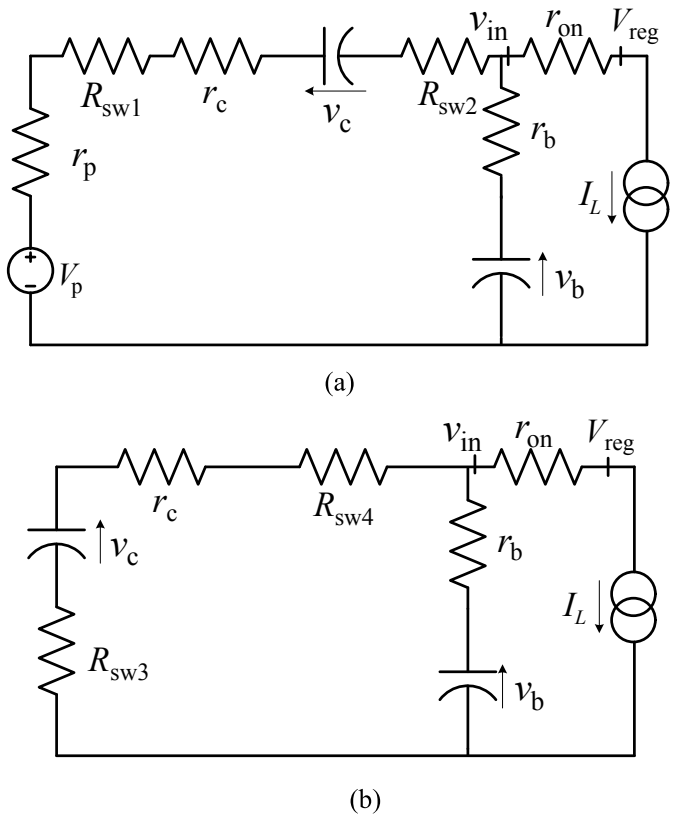


Figure 3.1: Static losses in SCALDO with four switches and one supercapacitor: (a) charging, and (b) discharging configuration

in Eq. (3.3) will be negligible and can be ignored. Therefore, power losses in charging and discharging configurations at steady-state are given by,

$$P_{\text{charge}} = I_{\text{L}}^2 \left(r_{\text{p}} + r_{\text{c}} + r_{\text{on}} + R_{\text{sw1}} + R_{\text{sw2}}\right) = I_{\text{L}}^2 \left(r_{\text{p}} + r_{\text{on}} + 2R_{\text{sw}}\right) \tag{3.4}$$

$$P_{\text{discharge}} = I_{\text{L}}^2 \left(r_{\text{c}} + r_{\text{on}} + R_{\text{sw3}} + R_{\text{sw4}}\right) = I_{\text{L}}^2 \left(r_{\text{on}} + 2R_{\text{sw}}\right) \tag{3.5}$$

where $r_{\text{c}} \ll R_{\text{sw}}$ and switches are assumed to be identical.

The losses are mainly due to ESR of SCs and the ON-resistance of the MOSFET switches. The ESR losses are of a particular concern when multiple capacitors are connected in series. By selecting supercapacitors with very low ESR values this loss can be minimized. With the availability of new materials and techniques, some families of commercial SCs have been produced with ESR values in the range of fractional mΩ to few tens of mΩ [70, 88, 97]. For SCs of values below 100 F, typical ESR is in the range 30–700 mΩ, but for larger capacitance values it drops to 0.3–10 mΩ.

In general SCALDO configurations, $2n$ switches are required to connect n SCs in parallel. When the switches are identical, their total resistance is given by,

$$\frac{1}{R} = \sum_{i=1}^{n} \frac{1}{2R_{\text{sw}i}} \quad \Longrightarrow \quad R = \frac{2R_{\text{sw}}}{n} \tag{3.6}$$

For a constant current I_{L} drawn by the load, the power loss due to paralleling these switches is,

$$P_{\mathrm{parallel}} = I_{\mathrm{L}}^2 \left(\frac{2R_{\mathrm{sw}}}{n} \right) \tag{3.7}$$

To connect those SCs in series, only $(n+1)$ switches are needed. The switch-related power loss due to this connection is,

$$P_{\mathrm{series}} = I_{\mathrm{L}}^2[(n+1)R_{\mathrm{sw}}] \tag{3.8}$$

In a SCALDO-CSDP configuration like Fig. 2.17(a), when charging $(n+1)$ switches are closed while $2n$ are open; and vice versa when discharging as in Fig. 2.17(b). The total rate of energy loss E across a charge-discharge cycle is,

$$E = I_{\mathrm{L}}^2[(n+1)R_{\mathrm{sw}}]t_{\mathrm{c}} + I_{\mathrm{L}}^2 \left(\frac{2R_{\mathrm{sw}}}{n} \right) t_{\mathrm{d}} \tag{3.9}$$

In this CSDP configuration, $t_{\mathrm{c}} = kt_{\mathrm{c}} = nt_{\mathrm{c}}$, therefore,

$$E_{\mathrm{CSDP}} = I_{\mathrm{L}}^2[(n+1)R_{\mathrm{sw}}]t_{\mathrm{c}} + I_{\mathrm{L}}^2 \left(\frac{2R_{\mathrm{sw}}}{n} \right) nt_{\mathrm{c}} = (n+3)I_{\mathrm{L}}^2 R_{\mathrm{sw}} t_{\mathrm{c}} \tag{3.10}$$

A SCALDO-CSDP such as 5-to-1.5 V configuration requires two SCs and seven switches. The energy loss for one charge-discharge cycle that supplies 5 A constant load current is,

$$E_{5-1.5} = (n+3) \times 5^2 R_{\mathrm{sw}} t_{\mathrm{c}} = 125 R_{\mathrm{sw}} t_{\mathrm{c}} \tag{3.11}$$

where $n = 2$.

Since high capacitances are used in SCALDO, charging times t_{c} will be long. Therefore, the only option for reducing energy loss in Eq. (3.10) is to use switches with very low resistance R_{sw}. Unfortunately this is not always possible in practical situations, especially for high-current applications.

When developing the SCALDO for a high-current application, all of the static losses become significant, specifically the ESR and switch resistance losses. In order to approach the ideal end-to-end efficiency for SCALDO, we can minimize switch related losses by reducing the number of switches with the development of a new SCALDO topology [54].

3.2 RS-SCALDO basics

For this thesis, I used the standard SCALDO with one SC and four switches to transform to reduced-switch SCALDO. When charging, two switches are required to connect the SC between the unregulated power supply and the LDO. Similarly, two switches required when discharging to connect SC between ground and LDO. At both instances (charging and discharging) the SC should connect to the LDO to power the load continuously. But the unregulated power supply and ground are connecting to SC alternatively and they

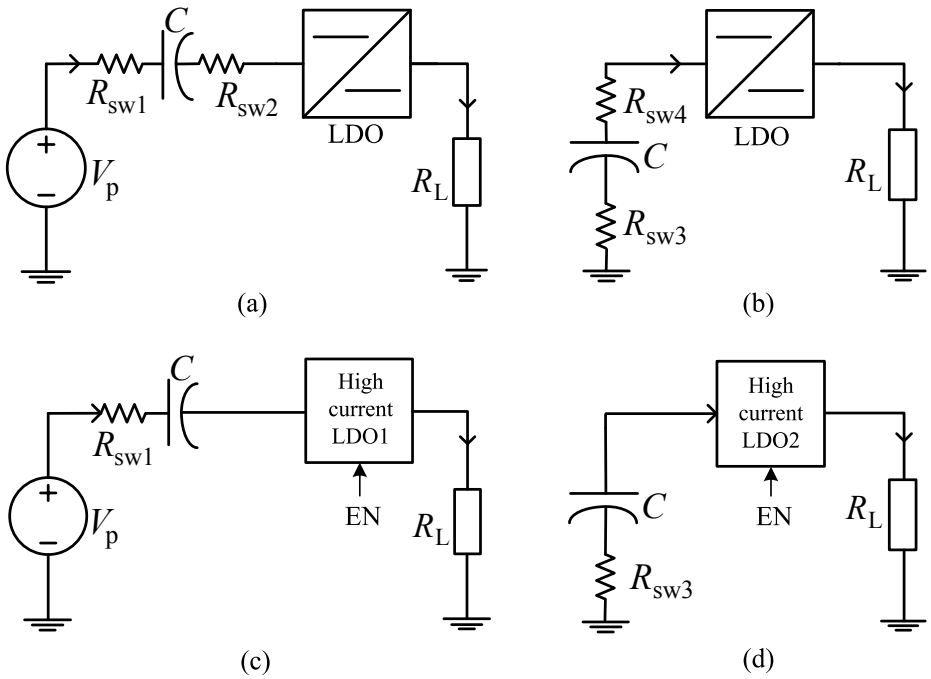


Figure 3.2: Transforming SCALDO to RS-SCALDO: immediately visible switches in SCALDO (a) R_2 in charging phase and (b) R_4 in discharging phase are eliminated. The new topology with (c) LDO1 at charging phase and (d) LDO2 at discharging phase are utilized. After eliminating R_2 and R_4 which are immediately visible to LDO, two high-current capable regulators LDO1 and LDO2 with enabling function (EN) are utilized.

must be disconnected accordingly. These two switches cannot be eliminated. This implies that any reduction in switch count can only be done at the LDO connection point.

The first step is to eliminate the switch in the immediate vicinity of the LDO (SW_2) in charging phase was eliminated as illustrated in Figs. 3.2(a) and (c). The LDO is replaced with a high-current capable regulator that has an enable feature as in Fig. 3.2(c). Next, the same procedure is applied to remove the switch in discharging phase (SW_4), as illustrated in Figs. 3.2(b) and (d). Therefore, two separate LDOs (LDO1 and LDO2) are required to work alternately during charging and discharging phases. Their output terminals should be common when connecting to the load. This elimination of switches is possible as the series pass-elements of LDOs themselves can act as switches.

When we apply this strategy to a general SCALDO with n SCs and $3n + 1$ switches, half the switches at the SCs paralleling stage can be eliminated along with a single switch at the stage of series connection of SCs. Hence $n + 1$ switches in a SCALDO can be eliminated from the total of $3n + 1$ switches. With these changes to switch numbers, the energy loss of Eq. (3.10) becomes,

$$E = I_{\mathrm{L}}^2[(n)R_{\mathrm{sw}}]t_{\mathrm{c}} + I_{\mathrm{L}}^2\left(\frac{R_{\mathrm{sw}}}{n}\right)nt_{\mathrm{c}} = (n+1)I_{\mathrm{L}}^2R_{\mathrm{sw}}t_{\mathrm{c}} \tag{3.12}$$

Thus, for a 5-to-1.5 V RS-SCALDO with 5 A load, the energy loss is,

$$E_{5-1.5} = (n+1) \times 5^2 R_{\mathrm{sw}}t_{\mathrm{c}} = 75R_{\mathrm{sw}}t_{\mathrm{c}} \tag{3.13}$$

where $n = 2$, giving a 40% reduction in energy wastage. Further, a common control circuit for both LDOs can be considered to reduce overall circuit complexity. So, a strategy to minimize the number of switches in a basic SCALDO configuration is as follows:

1. Eliminate switches immediately visible to LDO at charge and discharge phases
2. Utilize a pair of LDO stages with a common output terminal for charge and discharge phases
3. Develop a control circuit for LDOs in which the series-pass element of a LDO stage is driven into an open circuit while the other LDO is configured to regulate the output voltage

Basic RS-SCALDO operation

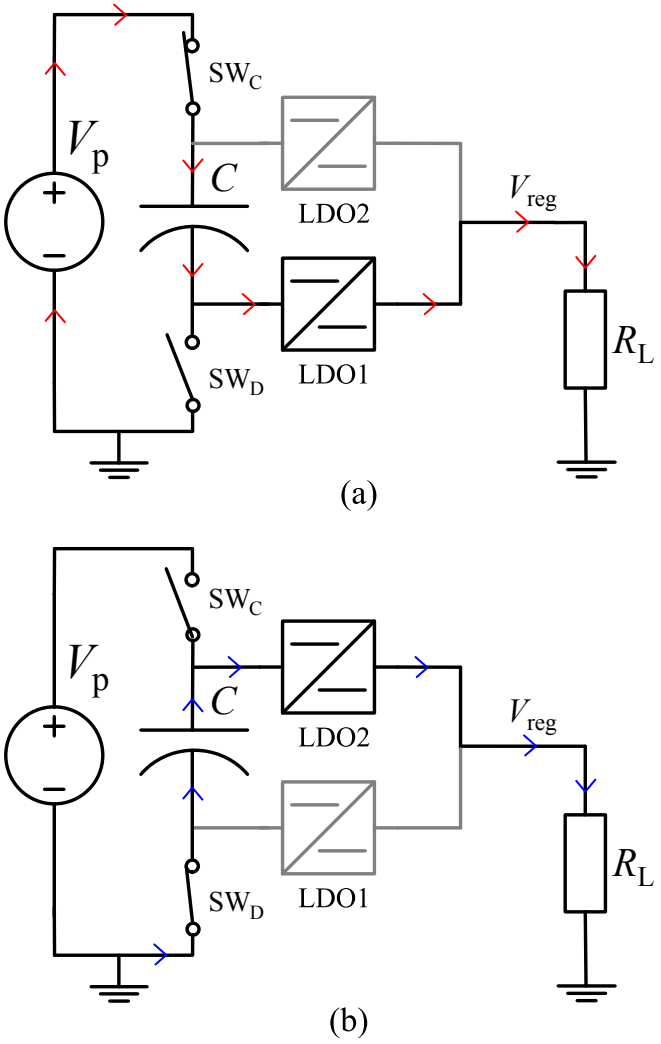


Figure 3.3: Basic RS-SCALDO with one SC and two switches (a) in SC-charging phase the modified LDO (LDO1) regulates the output voltage while LDO2 and SW_D at off-state, and (b) in SC-discharging phase, standard LDO (LDO2) regulates the output while LDO1 and SW_C at off-state

The two phases of SC energy circulation for a basic RS-SCALDO are shown in Fig. 3.3. This configuration has one SC, therefore two switches are required. A controller signal enables the power switch SW_C to connect the SC in a series configuration with LDO1 to store energy in the capacitor until the input voltage at LDO1 reaches a system-specified minimum. This SC-charging phase is shown in Fig. 3.3(a): switch SW_C and LDO1 are active while SW_D and LDO2 are inactive. The inactive components act as open circuit, so there will be no current conduction through them. Once the LDO-input voltage reaches its minimum, another control signal then allows the SC to release the excess charge to LDO2 by closing switch SW_D. This SC-discharging phase in Fig. 3.3(b) continues until LDO2 reaches its system-specified minimum voltage. At this phase SW_C and LDO1 are open circuit. After completing SC-discharging, the next charging cycle begins. In this charge-discharge process, RS-SCALDO maintains SC charge balance across cycles. For a continuous-constant current load, the input power source will connect only half the time. Therefore, its end-to-end efficiency matches that of the basic SCALDO is,

$$\eta = \frac{V_{\text{reg}} I_{\text{L}}}{V_{\text{p}} I_{\text{L}}/2} = 2\frac{V_{\text{reg}}}{V_{\text{p}}} \tag{3.14}$$

3.3 High current LDOs and RS-SCALDO technique

As discussed earlier, the circuit complexity of a SCALDO configuration due to its large number of switches was the main reason to minimize its switches. The $3n + 1$ switches are required for the n number of SCs in a general SCALDO configuration. They were reduced to a $2n$ switches by adding an extra LDO to the circuit. Thereby, it minimized the ON-resistance losses of the switch and come across with a much suitable SCALDO topology for high-current applications such as VRMs.

To upgrade the existing 1 A SCALDO circuit to a higher current capable RS-SCALDO, the LDO should be replaced. Figure 3.4 [98] presents the maximum current capability versus typical dropout voltage in some commercially available LDOs. They are packaged in a single IC that limits thermal dissipation in the pass-element.

Current capability of an LDO is limited by the ON-resistance of the pass-element, maximum available gate-bias voltage and thermal limitation of the package. A factor that affects the ON-resistance is the size of the pass-element and it is inversely proportional to the die-size. With all other factors being equal, a larger die-size has a lower resistance. Compared to IC-based small LDOs, the discrete MOSFET-based devices with larger die-size are suitable for high-current applications.

The LDO pass-element operates in the linear region to drop the input voltage down to the desired output voltage. Therefore, it behaves like a simple resistor at the steady state operation and its dropout is a function of the ON-resistance of the FET. The dropout voltage is also influenced by the gate-bias voltage of the pass-element. An N-channel

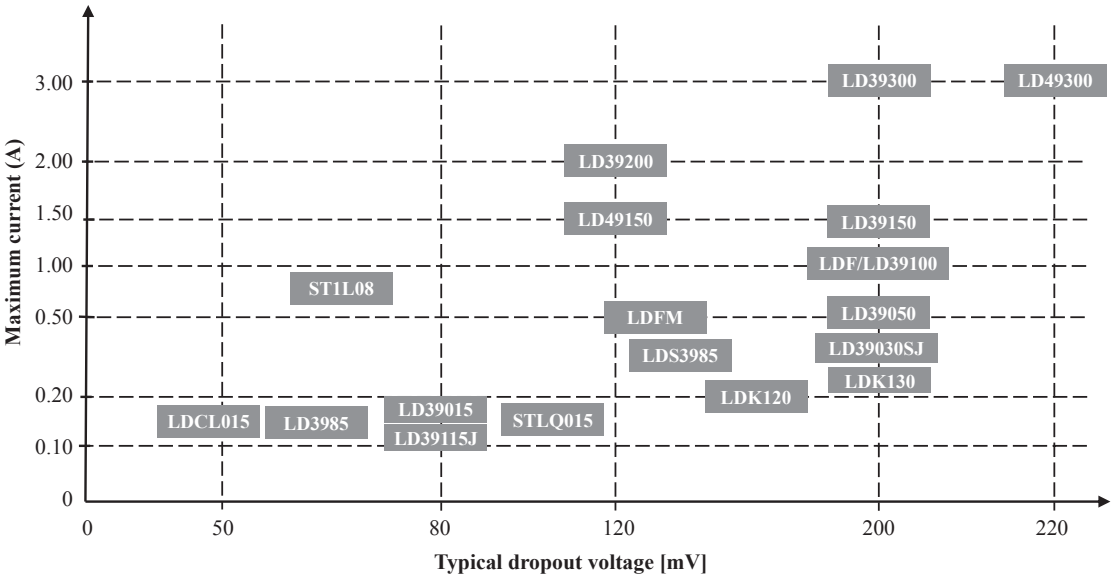


Figure 3.4: Typical dropout voltages vs. maximum current capability of LDOs [98]

LDO can be driven by low input rail voltages of about 1 V compared to a minimum input voltage of 2.5 V for a P-channel one [99]. N-channel LDOs require a positive gate-drive signal with respect to the output, where as P-channel can be driven from a negative signal with respect to the input. The N-channel FET has a higher current conduction ability than a same sized P-channel one. However, for N-channel LDOs to draw more current a charge-pump circuit or an external higher voltage supply is required [52].

In addition to the SCs with very low ESR and switches with lesser ON-resistance, a very low-dropout voltage in a pass-element is recommended for a high-current RS-SCALDO to reduce the losses and obtain a high-efficiency. Further, digitally controlled output capability and the enable feature are required. Some commercially available LDO options are discussed as follows.

Figure 3.5 shows a 10 A capable LDO from Linear Technologies [100] designed to power microprocessors. This LT1581 LDO has a 100 mV dropout voltage at light loads rising to just 430 mV and it can achieve a theoretical maximum efficiency of 85.3% at 10 A.

LT3070 is another LDO from the same manufacturer which is capable of 5 A [101] and allows paralleling them to boost current capability. LDO has a typical dropout of about 85 mV. The output voltage can be digitally programed for a range from 0.8 V to 1.8 V.

To develop very high-current capable LDOs using external MOSFET as pass-elements, the LDO controllers [102, 103] can be utilized. They can be used to realize very low-dropout and high currents. These controllers widen thermal limits of LDOs compared to single packages. For example, MIC5156/7/8 family [102] from Micrel Inc are single IC solutions for high-current low-dropout linear voltage regulation. They usually recommend N-channel enhancement-mode MOSFETs for the applications where the input or gate

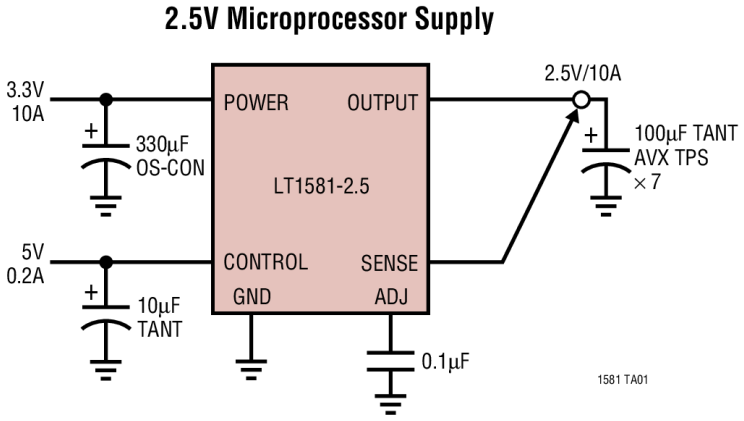


Figure 3.5: A commercially available high-current LDO LT1581 [100] with output 2.5V, 10 A

drive uses low voltage. These LDO controller can drive the gates to obtain output current as high as what the MOSFETs can provide.

3.4 Proof of the RS-SCALDO concept

In order to prove the concept of RS-SCALDO, a prototype of 7.5-to-3.3 V regulator circuit was designed using components similar to those in the basic SCALDO. Two ADP1706 [95] LDO ICs from Analog Devices and two PVN012A [96] solid-state relays from International Rectifier were used to build the power circuit together with flat-profile CAP-XX SCs [88]. LDO ADP1706 has fixed output voltages from 0.75 V to 3.3 V and it operates from an input of 2.5 to 5.5 V; it also provides up to 1 A output current. For this experiment, I used two LDOs each with a 3.3 V output. The solid-state relays are used as power switches. For this case, two series-connected 1.8 F, 2.75 V SCs were used as a single capacitor. As per SCALDO, the expected theoretical end-to-end efficiency is,

$$\eta = (k+1)\frac{V_{\text{reg}}}{V_{\text{in}}} = 2 \times \frac{3.3\text{ V}}{7.5\text{ V}}\% = 88\% \tag{3.15}$$

where $k = n = 1$, n is the number of SCs required for the case.

Early in the experiment, I discovered that the body-diodes in standard LDOs (in Fig. 3.6) create a parasitic path to discharge the SCs, causing the output regulation to fail during the RS-SCALDO discharging phase. Figure 3.3(a) shows the discharging configuration where LDO2 and SW_D are in the ON state and LDO1 and SW_C are OFF. Under these circumstances, the input of the LDO1 get shorted to the ground. The body-diode of LDO1 has enough voltage to become forward-biased due to the 3.3 V difference between output V_{reg} and input terminal of LDO1. This unnecessary path was created through the body-diode of LDO1 and the switch SW_D.

This undesirable current flow was blocked by adding a diode D1 at the output of LDO1. However, this resulted in a 0.8 V maximum voltage drop at the D1 output terminal that

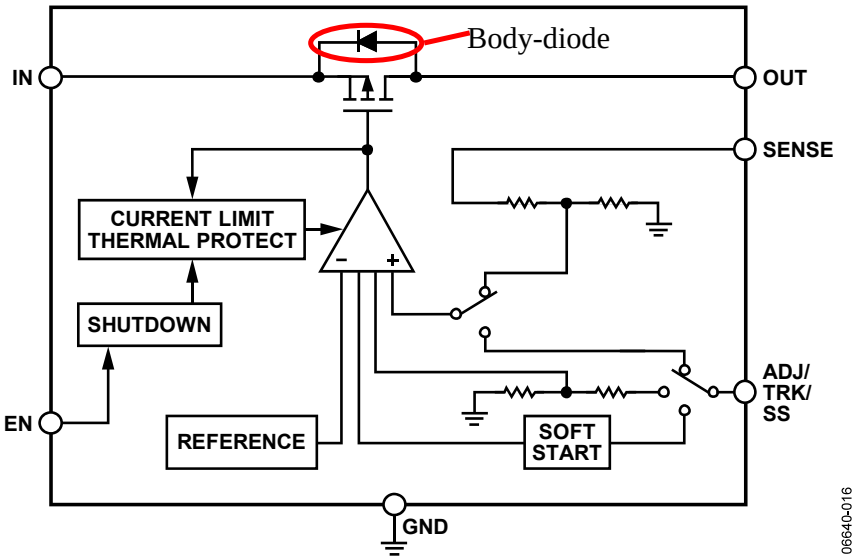


Figure 3.6: Block diagram of a ADP1706 LDO and its intrinsic body-diode [95]

was due to the forward drop of the diode. It created a sawtooth waveform varying from 2.5 to 3.3 V at D1 output and A2 respectively due to different output voltages generated from charging and discharging phases. To minimize this difference and balance the output of both phases another diode D2 was added at LDO2 output. Thereby, a 2.5 V, 300 mA output was obtained to work from a nominal input voltage of 7.5 V.

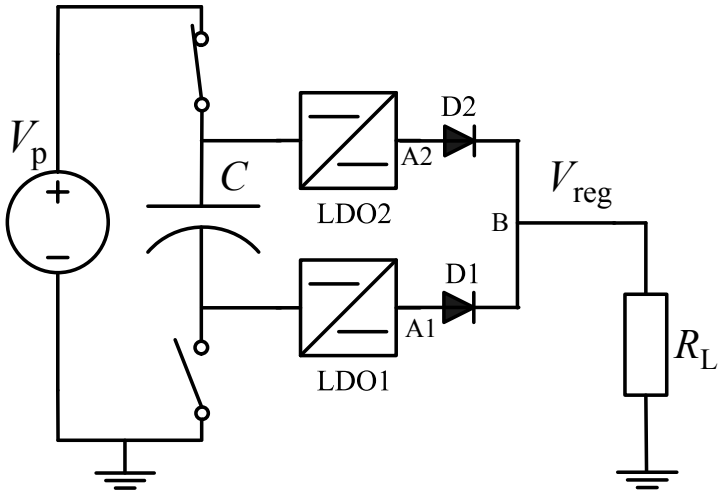


Figure 3.7: RS-SCALDO proof-of-concept prototype built with ADP1706 LDOs. Two 1N4007 diodes were used at the output to block current flow through LDO body-diodes.

This 7.5-to-2.5 V, regulator was built to prove the feasibility of the new RS-SCALDO technique [54]. Simulated results in Fig. 3.8 shows the output voltages, differential voltage of diodes and power dissipation of two diodes and the LDO pass-element against load current. Diodes dissipated twice as high as the power losses in LDO pass-elements. The current in this circuit was limited to 300 mA to control the non-linear behaviour and

power dissipation in diodes. We can use Schottky diodes with typical forward voltage drops of about 0.3 or 0.4 V at 25°C. However, additional losses will be incurred due to voltage drop in the series connection. Other issues were encountered when increasing the current; they are discussed in the following section.

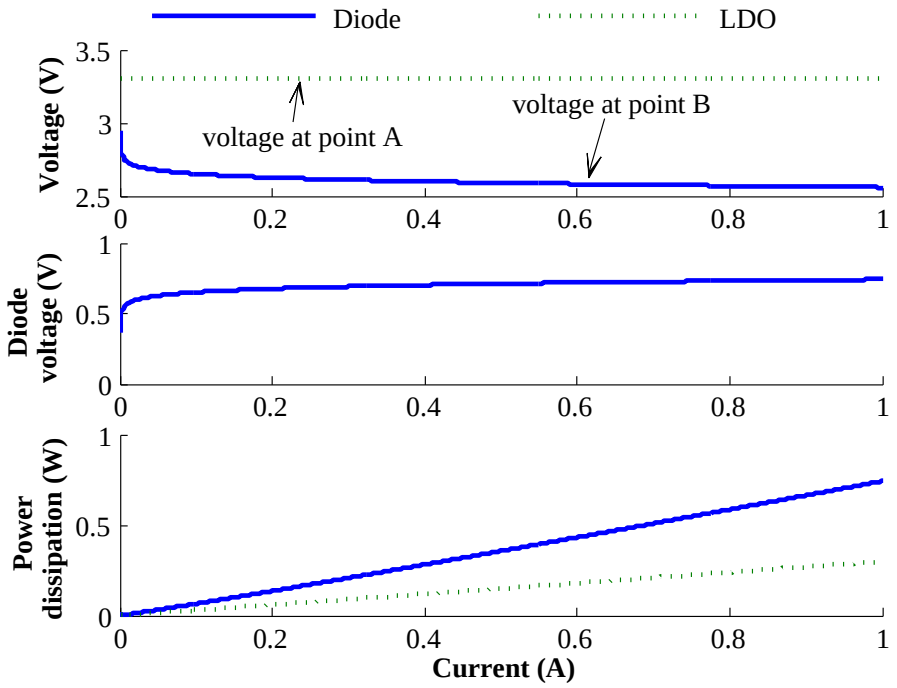


Figure 3.8: SPICE simulation results of load regulation of RS-SCALDO and power dissipation via diode and the pass-element of LDOs

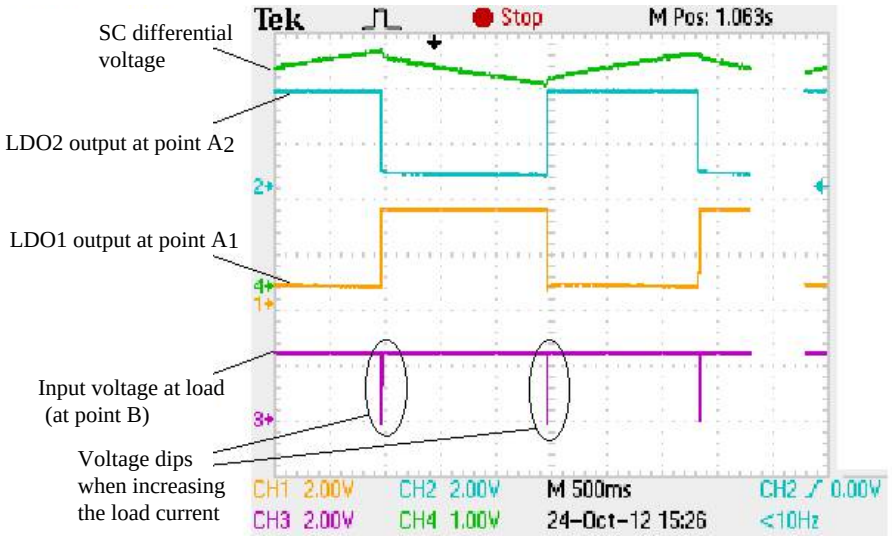


Figure 3.9: Experiment results of RS-SCALDO: waveforms at the output of LDOs (point A1 of LDO1, and point A2 of LDO2), output voltage of diodes (at point B), and the differential voltage of SC. When increasing the current over 300 mA, voltage dips were appeared due to the delays in control signals.

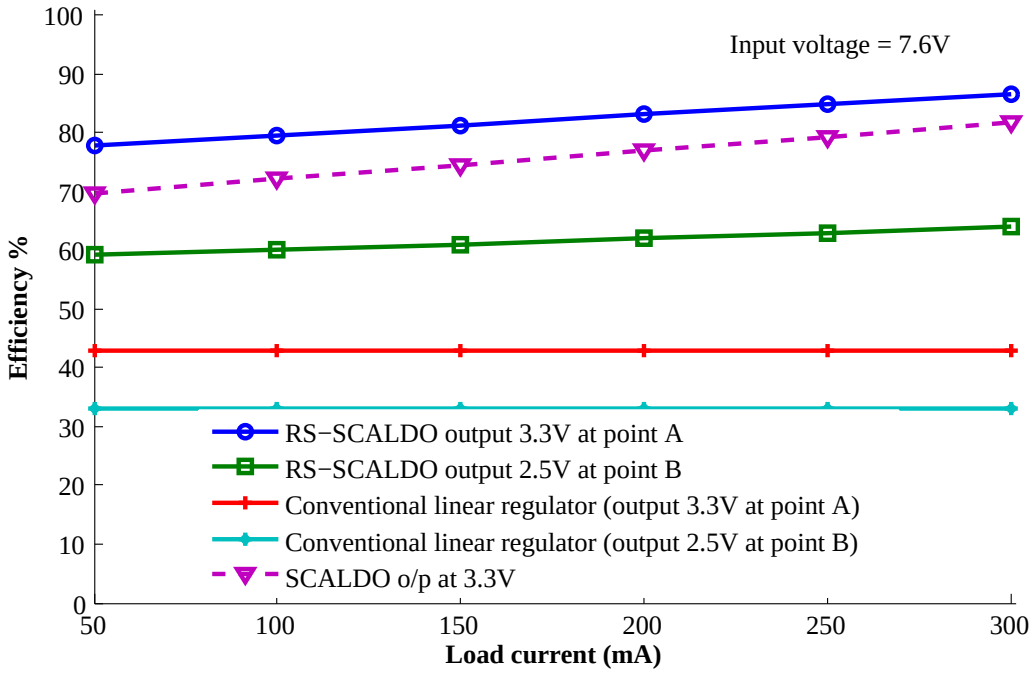


Figure 3.10: Load current (mA) vs. efficiency of a 7.5-to-2.5 V RS-SCALDO compared with SCALDO and theoretical values of conventional linear regulators

A PIC microcontroller was used to operate the two switches and LDOs while monitoring the input voltage at each LDO input. The monitored output at SC, LDO and point B are in Fig. 3.9. The two LDO waveforms at point A indicate their alternating operation.

Figure 3.10 shows the RS-SCALDO efficiency achieved with ideal diodes (output measurements were taken with respect to point A at LDO output), with real diode (output measurements were taken with respect to point B at diode output), and these results are compared against a standard 7.5-to-3.3 V SCALDO regulator. The degraded efficiency of the SCALDO occurs because of the losses associate with two extra solid-state switches. The efficiency curves in this current limit show a linear progression. However, when more current flows through the circuit, power dissipation in the switches will increase, leading to a reduction in efficiency. Nevertheless, RS-SCALDO efficiency curves indicate that approximately twice that of a conventional linear regulator should be achievable. Pass-element resistance r_{on} has a positive temperature coefficient due to decreasing carrier mobility. Therefore, power dissipation increases and reduces the overall efficiency.

It is important to mention that in a discrete implementation of this kind as in Fig. 3.7, diodes D1 and D2 are used simply to avoid activating the parasitic body-diode in the series pass-element of the LDO ICs. These diodes can be eliminated by designing discrete MOSFET-based regulator; this is discussed in Chapter 4.

3.5 Some issues in SCALDO prototype

In practical implementation, the SCALDO requires some switches without body-diodes, specifically that are connected to both SC negative terminal and positive terminal of switches at ground. The problematic switches are SW_{C2} in 12-to-5 V, SW_5 and SW_7 in 5-to-1.5 V and SW_4, SW_5 and SW_6 in 5-to-3.3 V. They can be found Figs 2.14, 2.15 and 2.16 respectively.

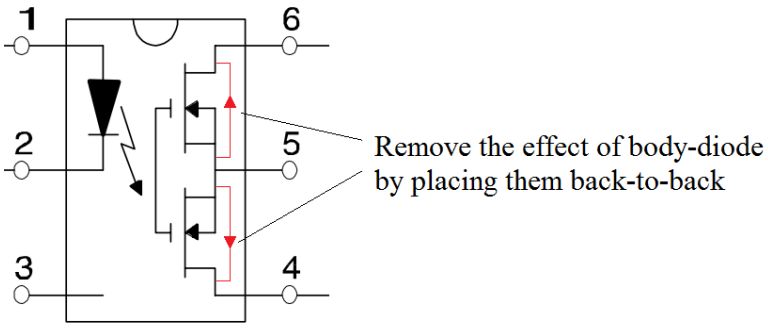


Figure 3.11: SCALDO power switch: a block diagram of a power MOSFET-based solid-state relay [96]

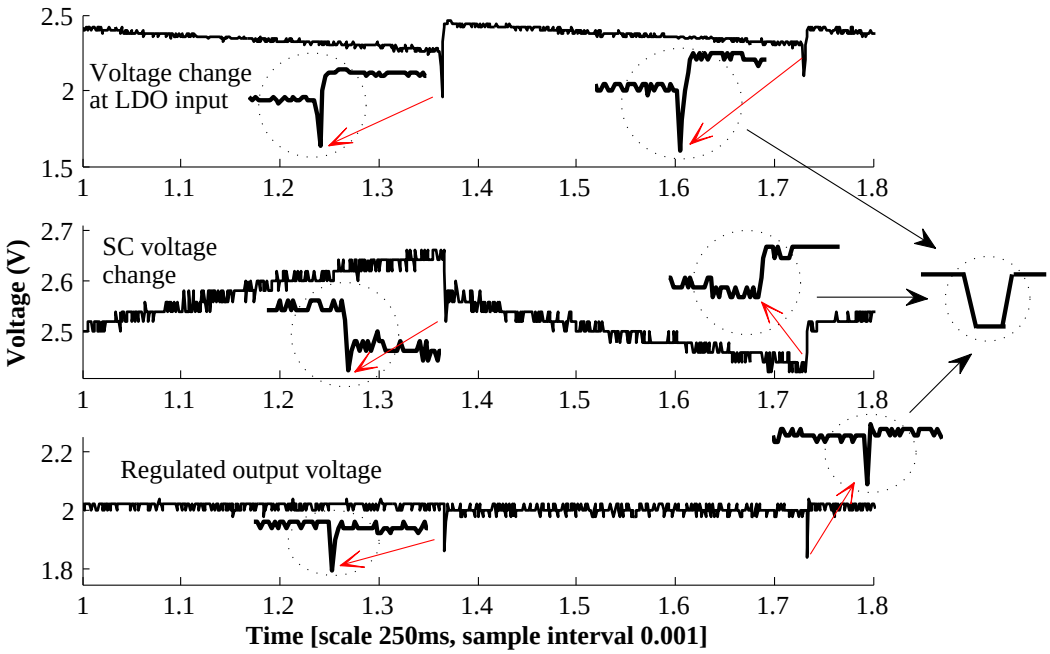


Figure 3.12: 5-to-2 V SCALDO: voltage dips in the input of the LDO, differential voltage of SC, and regulated output wave. These voltage dips can be minimized by appropriately sending control signals at transitions.

In previous proof-of-concept prototypes of SCALDO, this issue was addressed by utilizing solid-state relays; commercially available PVN012 solid-state relay from International Rectifiers [96] was used. The power path of these relays utilize two N-channel MOSFETs with their source-terminals connected together. This arrangement avoids current

conduction via body-diodes when they are in the OFF state. The device has a common gate-terminal as in Fig. 3.11 that is driven by an integrated circuit photovoltaic generator. The MOSFET-based integration improves the current capability and reduces biasing losses. However, the ON-resistance of these relays can be as high as 100 mΩ [96] compared to 6.8 mΩ [104] for discrete MOSFETs. On the other hand, the average unit price of a solid-state relay is 30 times higher than a power-MOSFET with similar current capability. These relay switches are not economically viable for high-current applications such as RS-SCALDO, and they waste more power than discrete MOSFET-based designs.

Another issue is the signal delays in the SCALDO control circuit; they create transient dips in the output voltage. These dips are reflected in the SC charge-discharge waveform as well as in the input voltage at the LDO. Figure 3.12 shows the dips in 5-to-2 V SCALDO at 500 mA load. Although not significant in low-current applications, they will be critical at higher load conditions. The ON-OFF delay between the two LDOs in RS-SCALDO can create a temporary short-time dip on the output wave that can cause a rise in overall losses and degrade the quality of regulation. To address this issue, a capacitor with very low ESR and large capacitance can be connected to the output. However, it will not be a feasible solution with regard to circuits with limited real-estate or cost minimized designs.

These limitations in SCALDO and the above basic proof-of-concept indicate that the RS-SCALDO technique can be made viable for VRMs by:

1. finding a remedy for body-diode effect in LDO pass-element
2. developing suitable linear regulator with low-dropout voltage and high-current capability
3. developing high-current capable MOSFET-based switches with less ON-resistance
4. developing low power control stage, to minimize the overall losses

These tasks are detailed in Chapter 4.

Chapter 4

RS-SCALDO for voltage regulator modules

This chapter presents the theory and the experiment results of a reduced-switch SCALDO (RS-SCALDO) applicable to voltage regulator modules (VRMs). In addition, it reviews the circuit related problems in the original SCALDO and RS-SCALDO designs and presents some possible solutions. Design details of a high-current capable RS-SCALDO proof-of-concept prototype is also included in this chapter. Specifications are selected based on the state-of-the-art techniques in VRM research together with Intel requirements. The aim of bench experiments is to investigate how best the RS-SCALDO for VRMs. A detailed discussion of results and a comparison with theoretical data are presented at the end of the chapter.

4.1 Design considerations and specifications for VRM

Modern high-performance microprocessors in computers no longer can be powered by a 5 V voltage rail which was used previously to power both core and input/output devices. As discussed in the Chapter 1, they have very stringent power requirements [12]. The new processor core-voltage requirement ranges from 1.6 V down to 0.5 V and is usually defined by specific processor performance. There are many benefits for lower core-voltages such as reduced power consumption, and less heat dissipation [105]. However, a dedicated power supply is required to regulate this very low core-voltage at very high-currents with fast transients.

VRM or voltage regulator-down (VRD) is the common name for the power supply of these new processors. It is a post-regulator that converts a higher voltage of an input power source to the lower voltage of a microprocessor core [12]. The input source of the VRM is a pre-regulator, usually a "silver box" or a separate power supply on the motherboard. Typical output rails of silver-box are 12, 5 and 3.3 V. At present, input voltage of VRM power-stage uses the 12 V rail with -8% and +5% voltage tolerance [12]. The control-stage of the VRM is powered by the 5 or 12 V rails.

Intel designed a scheme to change power consumption dynamically [12] by using a lower voltage for the processor than its peripherals. According to this scheme, VRMs are capable of continuous adjustment of output voltage in response to a processor command. It is done by identifying a voltage identification (VID) code. In the latest Intel specifications [12], an 8-bit VID code can set the reference core voltage V_{ID}. An functional diagram of a VID logic controller is illustrated in Fig. B.6. A digital-to-analog converter (DAC) accepts a VID from microprocessor and convert the digital code to the analog signal. This analog signal is feed to pulse-width-modulation (PWM) circuit and adjusts the output voltage in accordance with the 8-bit code. The output voltages have an offset boundary defined by a fixed load line with 0.8 mΩ slope [12]. However, they are only usable in the range of 0.5–1.6 V. For all specified voltages and load currents from no load to maximum, the output voltage of the VRM (V_{reg}) should be regulated within its minimum and maximum values as define in Table 4.1. However, during fast transients, it can violate the normal voltage regulation range provided that the overshoots should settle out within about 25 μs and do not exceed the maximum value defined by the processor manufacturer. Figure 4.1 illustrates an overshoot in core voltage. When developing RS-SCALDO for VRMs, these specifications were taken into account.

Table 4.1: Requirements of load regulation in Intel voltage regulator-down (VRD) 11.0 [12]

Parameter	Symbol	Value
Load line boundaries of the core voltage	$V_{\mathrm{reg}}^{\mathrm{max}}$	$V_{\mathrm{ID}} - (0.8\ \mathrm{m\Omega} \times I_{\mathrm{L}})$
	$V_{\mathrm{reg}}^{\mathrm{typ}}$	$V_{\mathrm{ID}} - (0.8\ \mathrm{m\Omega} \times I_{\mathrm{L}}) - 15$ mV
	V_{reg}^{min}	$V_{\mathrm{ID}} - (0.8\ \mathrm{m\Omega} \times I_{\mathrm{L}}) - 30$ mV)
V_{ID} overshoot voltage	$V_{\mathrm{ID}}^{\mathrm{OS}}$	$V_{\mathrm{ID}} + 50$ mV
V_{ID} overshoot time	$T_{\mathrm{ID}}^{\mathrm{OS}}$	25 μs

To obtain a 1.5 V regulated output in an RS-SCALDO, voltage rails of 3.3 and 12 V were proposed as inputs to power-stage and control-stage respectively; see Fig. 4.2. In order to demonstrate the application of RS-SCALDO technique for VRM implementation, essential functional specifications were proposed with (a) an output voltage adjustable from 1.45 to 1.55 V at 50 mV step, (b) a tight voltage tolerance of ±20 mV at load current 5 A, and (c) an input voltage 3.3 V rail with ±5% tolerance. These output voltages (1.45, 1.5 and 1.55 V) should lie within the output boundaries defined by the VID load-line of Table 4.1 as illustrated in Fig. 4.3 for an output of 1.5 V. When designing a 3.3-to-1.5 V RS-SCALDO the circuit can be divided into two functional blocks based on the voltage and the current requirements:

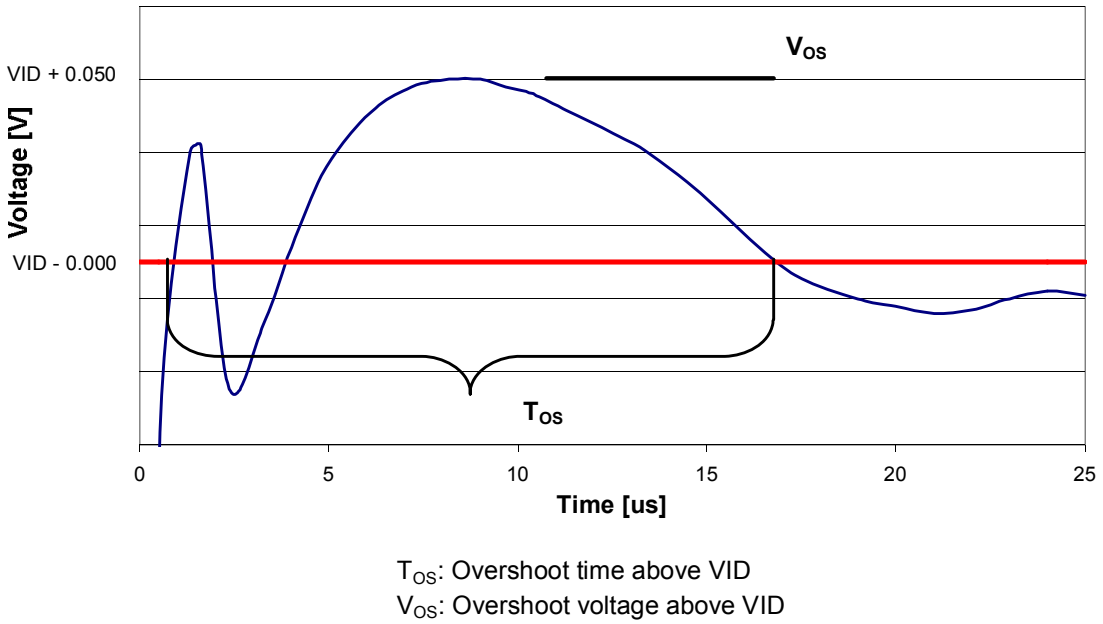


Figure 4.1: Example waveform of an overshoot of the processor core voltage [12]

1. **Power circuit stage (PCS):** PCS is powered by the 3.3 V rail and is capable of handling high-current up to 5 A between unregulated DC power source and the load. The three components in the high-current path are power switch, pass-element of LDO and the supercapacitor (SC) serving as a lossless voltage dropper.

2. **Control circuit stage (CCS):** CCS is powered from the 12 V rail and operates at verylow current (less than 5 mA) and accomplishes the PCS functions. It monitors the voltages at SC terminals and controls activation of the power switches and LDOs while regulating the output voltage. An error amplifier, voltage reference, digital potentiometer, analog switches and a PIC micro-controller are the key components. A digital potentiometer at the feedback loop of the LDO implements the VID logic.

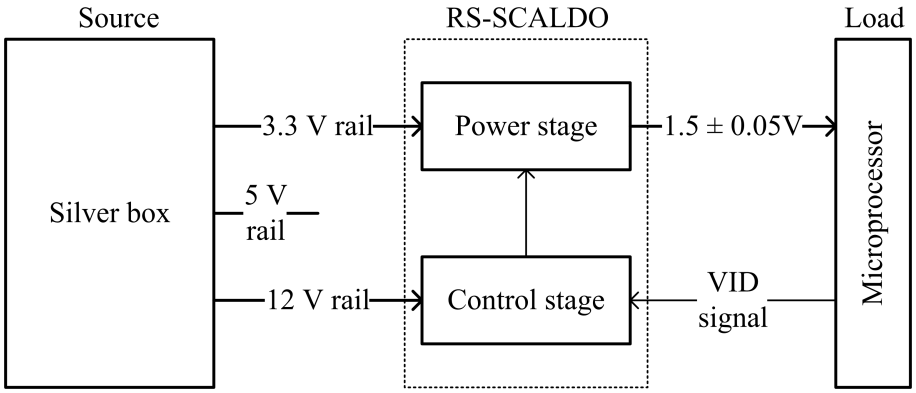


Figure 4.2: Proposed RS-SCALDO with power source and load

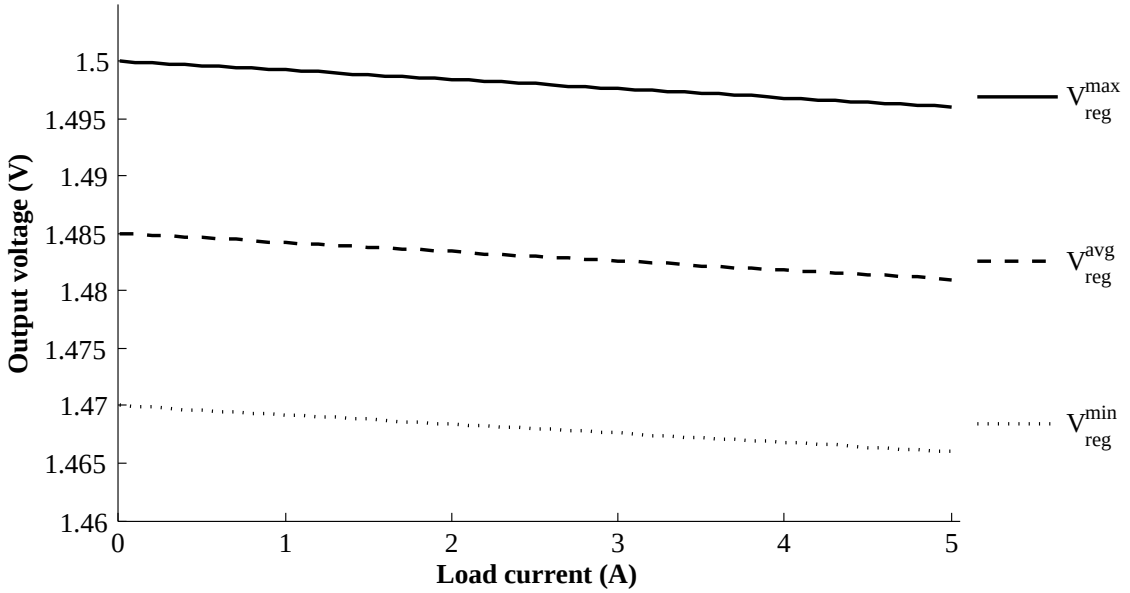


Figure 4.3: Intel specified load-line boundaries for a 1.5 V regulator driving a constant-current load varying from 0 to 5 A.

If the control circuit dissipates very low power compared to the power stage, the theoretical boundaries of other parameters can be calculated using the equivalent circuits in Fig. 4.4 as described below.

For various input source voltages V_{p} and load currents I_{L}, the RS-SCALDO will maintain its regulation voltage V_{reg} by varying the ON-resistance of pass-element of LDO r_{on}, and keep the input voltage v_{in} close to regulation. V_{reg} is given by,

$$V_{\mathrm{reg}} = \left[\frac{v_{\mathrm{in}} - I_{\mathrm{L}} r_{\mathrm{on}}}{1 + \frac{r_{\mathrm{on}}}{R_{\mathrm{fb}}}}\right] = v_{\mathrm{in}} - I_{\mathrm{L}} r_{\mathrm{on}} \tag{4.1}$$

where

$$v_{\mathrm{in}} = V_{\mathrm{reg}} + I_{\mathrm{L}} r_{\mathrm{on}} \tag{4.2}$$

and where R_{fb} is the feedback resistance with $R_{\mathrm{fb}} \gg r_{\mathrm{on}}$. SCALDO theory predicts the end-to-end efficiency of a 1.5-to-3.3 V regulator is

$$\eta = (1 + k)\left[\frac{V_{\mathrm{reg}}}{V_{\mathrm{p}}}\right] = 2 \times \left[\frac{1.5\ \mathrm{V}}{3.3\ \mathrm{V}}\right] = 90.9\%$$

To obtain this overall efficiency of RS-SCALDO, the minimum efficiency of LDO $\eta_{\mathrm{LDO}}^{\mathrm{min}}$ should be greater than or equal to 90.9%. This is achieved at the maximum input voltage of LDO input $V_{\mathrm{in}}^{\mathrm{max}}$ which can be calculated as,

$$\eta_{\mathrm{LDO}}^{\mathrm{min}} = \left[\frac{V_{\mathrm{reg}}}{V_{\mathrm{in}}^{\mathrm{max}}}\right] = 90.9\%$$

giving

$$V_{\mathrm{in}}^{\mathrm{max}} = \left[\frac{1.5\ \mathrm{V}}{0.909}\right] = 1.65\ \mathrm{V} \tag{4.3}$$

The ON-resistance of the pass-element r_{on} at the maximum current $I_{\text{L}}^{\text{max}}$ can be calculated using Eq. 4.2. It would be,

$$r_{\text{on}} = \frac{1.65\ \text{V} - 1.5\ \text{V}}{I_{\text{L}}^{\text{max}}} = \frac{0.15\ \text{V}}{I_{\text{L}}^{\text{max}}} \tag{4.4}$$

giving,

$$r_{\text{on}} = \frac{0.15\ \text{V}}{5\ \text{A}} = 30\ \text{m}\Omega$$

When selecting a suitable MOSFET for the LDO pass-element, the minimum ON-resistance should be much smaller than the above calculated value.

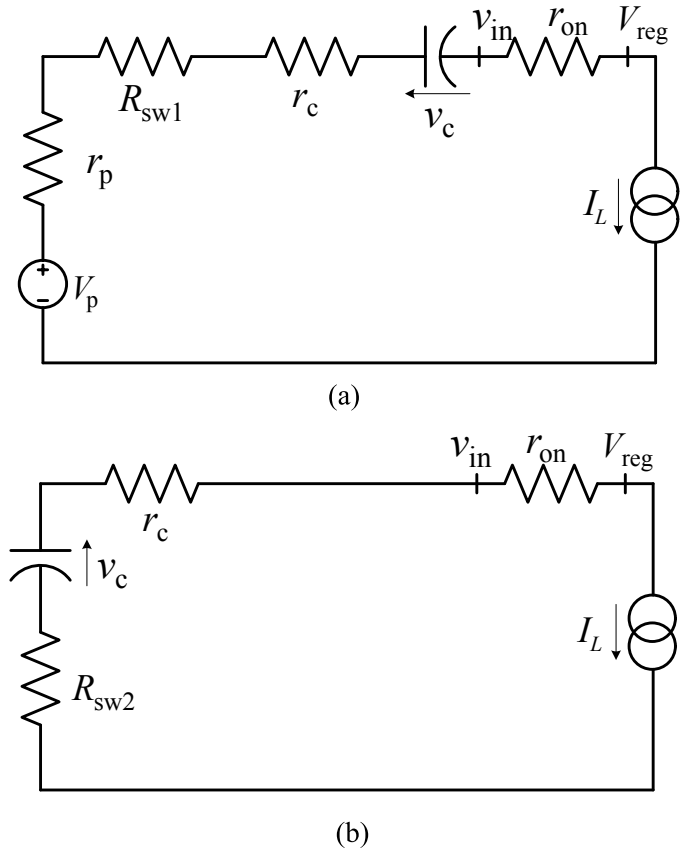


Figure 4.4: Basic RS-SCALDO static losses: (a) SC-charging configuration, and (b) SC-discharging configuration

Parameter	Symbol	Value (mΩ)
Internal resistance of the power supply	r_{p}	25*1
ESR of the SC	r_{c}	3.00*2
ON-resistances of the switch 1	R_{sw1}	6.80*3
ON-resistances of the switch 2	R_{sw2}	6.80*3

Let us consider the two phases of RS-SCALDO operation (i.e., SC charge and discharge) in Fig. 4.4. The resistances in the above circuit r_{p}, r_{c}, R_{sw1} and R_{sw2} are the

nominal values in the data sheets of the power supply TPS 2000[*1], BCAP310[*2], and AUIRL3705ZL[*3] MOSFET.
The input power supply voltage V_{p} at the charging phase in Fig. 4.4(a),

$$V_{\mathrm{p}} = v_{\mathrm{in}}(t) + v_{\mathrm{c}}(t) + (r_{\mathrm{p}} + r_{\mathrm{c}} + R_{\mathrm{sw1}})I_{\mathrm{L}} \tag{4.5}$$

At the end of SC charging, LDO input voltage reach the system specified minimum value $V_{\mathrm{in}}^{\mathrm{min}}$ and SC reaches the maximum voltage $V_{\mathrm{c}}^{\mathrm{max}}$. Therefore, the source voltage is given by

$$V_{\mathrm{p}} = V_{\mathrm{in}}^{\mathrm{min}} + V_{\mathrm{c}}^{\mathrm{max}} + (r_{\mathrm{p}} + r_{\mathrm{c}} + R_{\mathrm{sw1}})I_{\mathrm{L}} \tag{4.6}$$

For discharging phase in Fig. 4.4(b):

$$v_{\mathrm{in}}(t) = v_{\mathrm{c}}(t) - (r_{\mathrm{c}} + R_{\mathrm{sw2}})I_{\mathrm{L}} \tag{4.7}$$

At the beginning of the discharge phase, the input voltage of the LDO reaches the maximum voltage $V_{\mathrm{in}}^{\mathrm{max}}$,

$$V_{\mathrm{in}}^{\mathrm{max}} = V_{\mathrm{c}}^{\mathrm{max}} - (r_{\mathrm{c}} + R_{\mathrm{sw2}})I_{\mathrm{L}} \tag{4.8}$$

$$1.65\ V = V_{\mathrm{c}}^{\mathrm{max}} - 0.049\ \mathrm{V}$$

and $V_{\mathrm{c}}^{\mathrm{max}}$ is given by

$$V_{\mathrm{c}}^{\mathrm{max}} = 1.699\ \mathrm{V}$$

From Eq. 4.6 the minimum possible output voltage $V_{\mathrm{in}}^{\mathrm{min}}$ is

$$V_{\mathrm{in}}^{\mathrm{min}} = 3.3\ \mathrm{V} - 1.699\ \mathrm{V} - 0.174\ \mathrm{V} = 1.427\ \mathrm{V} \tag{4.9}$$

At the end of discharge phase, the SC reaches to the maximum voltage $V_{\mathrm{c}}^{\mathrm{min}}$,

$$V_{\mathrm{c}}^{\mathrm{min}} = V_{\mathrm{in}}^{\mathrm{min}} + (r_{\mathrm{c}} + R_{\mathrm{sw2}})I_{\mathrm{L}} \tag{4.10}$$

giving

$$V_{\mathrm{c}}^{\mathrm{min}} = 1.476\ \mathrm{V}$$

The minimum ON-resistance of the pass-element should be

$$r_{\mathrm{on}}^{\mathrm{min}} = \frac{V_{\mathrm{reg}} - V_{\mathrm{in}}^{\mathrm{min}}}{I_{\mathrm{L}}} = \frac{1.5\ \mathrm{V} - 1.427\ \mathrm{V}}{5\ \mathrm{A}} = 2.92\ \mathrm{m\Omega} \tag{4.11}$$

The maximum frequency of operation is given by

$$f_{\mathrm{op}} = \frac{I_{\mathrm{L}}}{2C\Delta V_{\mathrm{c}}} \tag{4.12}$$

$$f_{\mathrm{op}} = \frac{5\ \mathrm{A}}{2 \times 310\ \mathrm{F} \times 174\ \mathrm{mV}} = 46.35\ \mathrm{mHz}$$

RS-SCALDOs are designed to operate at very low frequencies that are 10^3 to 10^6 orders lower than high-frequency switch-mode converters. Due to these extremely low frequencies, the dynamic losses related to MOSFET switches can be neglected; moreover, RS-SCALDOs do not use any magnetic components in their circuits.

The above calculations are necessarily iterative due to assumptions made about real component values. Here, I assumed that they have a minimum resistance, and the printed circuit board (PCB) track resistance r_{pcb} was calculated as

$$r_{\mathrm{pcb}} = \frac{\rho \times \mathrm{Length}}{\mathrm{Thickness} \times \mathrm{Width}} \left(1 + (\alpha \times (T - 25))\right) \tag{4.13}$$

where ρ is the resistivity, α is the temperature coefficient and T is the temperature. For copper ρ and α are $1.7{\times}10^{-8}$ Ωm and $3.89 \times 10^{-3}/^{\circ}$C respectively. When the combined resistance of the PCB tracks and the power cables is considered, the practical value of the input voltage V_{p} has to be kept at slightly higher than theoretical value (by about 0.2 V).

To build the LDOs the same MOSFETs with minimum ON-resistance $r_{\mathrm{on}}^{\mathrm{min}}$ of about 6.8 mΩ were used. Compared to the calculated value in Eq. 4.11 this is nearly two times high, but are three to four times cheaper than the low ON-resistance devices.
With 6.8 mΩ the lowest possible dropout is given by

$$V_{\mathrm{do}}^{\mathrm{min}} = 6.8\ \mathrm{m\Omega} \times 5\ \mathrm{A} = 34\ \mathrm{mV} \tag{4.14}$$

giving the theoretical minimum input voltage of LDO for regulation

$$V_{\mathrm{in}}^{\mathrm{min}} = V_{\mathrm{reg}} + V_{\mathrm{do}}^{\mathrm{min}} = 1.5\ \mathrm{V} + 0.034\ \mathrm{V} = 1.534\ \mathrm{V} \tag{4.15}$$

Compared to Eq. 4.9 the value in Eq. 4.15 is 0.107 V difference and it can be achieved by increasing the input voltage to 3.407 V. By slightly increasing the input power supply voltage the concept of RS-SCALDO was proved. It is a matter of reducing these static losses to realize within the intended input voltage.

According to these design considerations, the specifications of Table 4.2 were selected for the proof-of-concept prototype.

In the previous chapter, the new topology with a less complex SCALDO circuit was identified yet with some challenges. The RS-SCALDO topology to be applicable in VRMs, it is necessary to overcome those challenges: the body-diode effect in the LDO pass-element, very low-dropout voltages and high-current capable LDOs, and low-power control stage.

4.2 Remedy to MOSFET body-diode effect and limitations

The Fig. 4.5 shows the components of the power stage circuits of the basic SCALDO and two RS-SCALDOs. Q1, Q2, Q3 and Q4 are switches and Q5, Q6 and Q7 are LDO

Table 4.2: Setting RS-SCALDO design specifications

Parameter	Symbol	Range
Nominal input voltage		
- for power circuit (PCS)	V_{p1}	3.5 V +15%
- for control circuit (CCS)	V_{p2}	12 V ±5%
Nominal output voltage	V_{reg} or V_{ID}	1.5 V
Output voltage step	ΔV_{ID}	± 50 mV
Maximum load current	I_L^{max}	5 A
Current slew rate	V_{ID}^{OS}	25 A/ μs

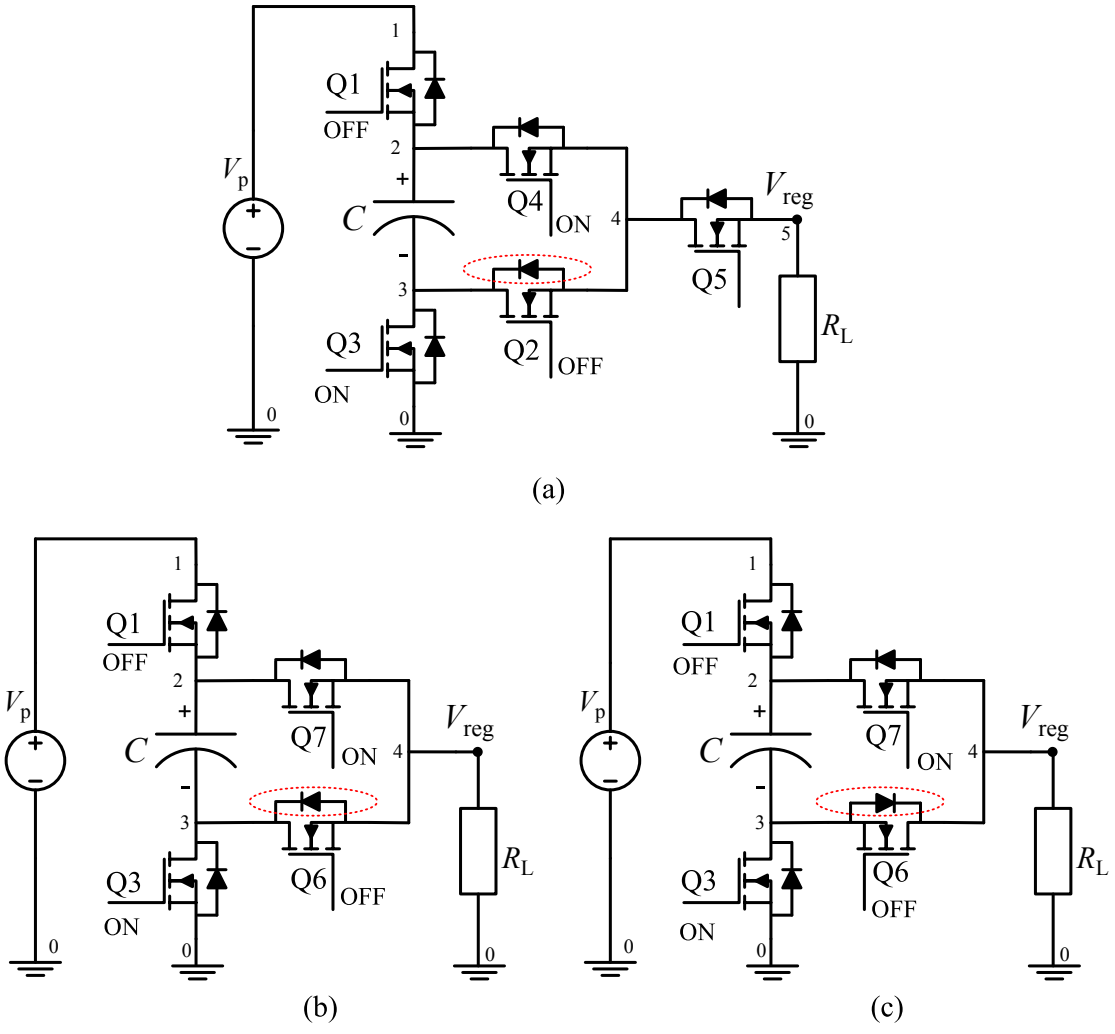


Figure 4.5: Basic SCALDO and RS-SCALDO: (a) SCALDO design with standard LDOs and MOSFET switches and Q2 body-diode can form a path to ground when Q3 is at ON-state, (b) RS-SCALDO design with standard LDOs and MOSFET switches and Q6 body-diode can form a path to ground when Q3 is at ON-state, (c) RS-SCALDO design with a remedy where the Q6 body-diode blocks the path to ground when Q3 is at ON-state.

pass-elements. The circuits shown in Fig. 4.5(a) and Fig. 4.5(b) use standard LDOs and standard MOSFET-based switches. The body-diodes in Q2 and Q6 create parasitic paths allowing discharge of the SC. This occurs during the SC discharging phase of SCALDO operation due to point 3 in the circuit being shorted to ground so that the voltage at point 4 is high enough to forward-bias the body-diode. In principle, MOSFETs are symmetrical, so the drain and source can hypothetically be interchanged. A weak or an undesirable device turn-on may occur due to a parasitic transistor that is created by the use of the body, the channel and the drift regions of these devices [106, 107]. To address this issue, one of the substrate-wells is connected to the body via an external contact terminal, where this terminal being referred to as the source. The parasitic diode that is created at the body and the epitaxial regions also gets connected to the source. (A detailed discussion and an analysis of power-MOSFETs and its body-diode can be found in the next chapter.)

The body-diode effect in the switches of RS-SCALDO can be prevented by interchanging the source-drain terminals of the pass-element as shown in Fig. 4.5(c). Due to the homogeneous properties in the drain-source channel, it was possible to interchange these terminals when designing the modified-LDO. This radical decision was taken by breaking the traditional practice of LDO design that is illustrated in Fig. 4.6(a). However, this new orientation of the MOSFET pass-element in Fig. 4.6(b) too has its limitations and will be discussed subsequently.

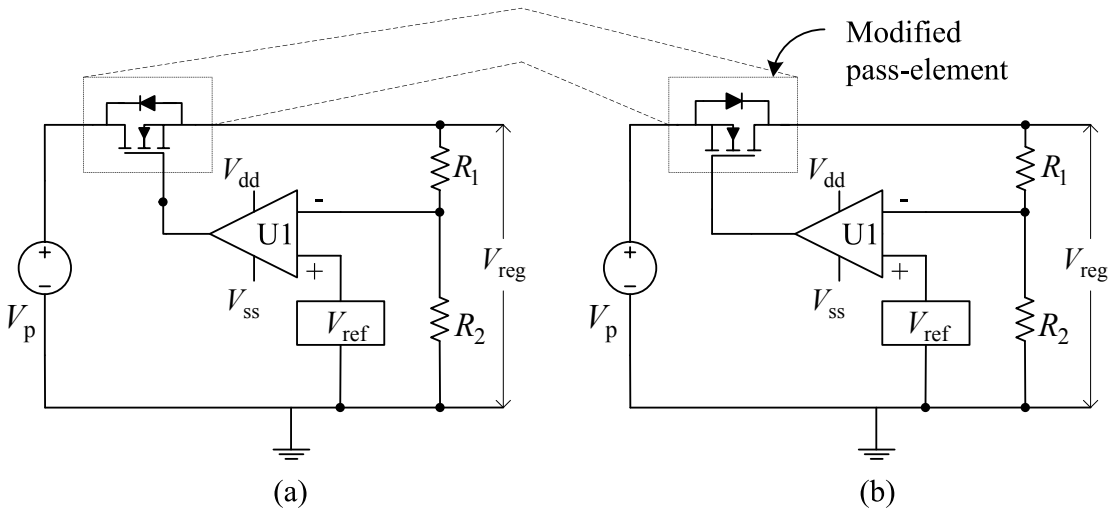


Figure 4.6: LDOs in an RS-SCALDO: (a) typical arrangement of drain-to-source of LDO (LDO2), (b) modified arrangement of source-to-drain LDO (LDO1)

In spite of the above improvements, there is a restriction to the application of the modified-LDO in Fig. 4.6(b); specifically it limits the input-to-output (source-to-drain) voltage difference. During SC charging, the LDO1 body-diode gets forward biased, although it should not conduct for proper regulation. However, the requirement of voltage

dropout of the LDOs in 3.5-to-1.5 V RS-SCALDO is less than the diode forward conduction voltage. That is,

$$V_{\mathrm{do}} = v_{\mathrm{in}} - V_{\mathrm{reg}} < V_{\mathrm{d}}$$

where v_{in} and V_{reg} are respectively the input and the output voltage of the LDO, V_{do} is the dropout voltage of the LDO, and V_{d} is the diode forward conduction voltage.

Since the modified-LDO is regulating the output voltage under the above condition ($V_{\mathrm{do}} < V_{\mathrm{d}}$), a small voltage variations in the input power source ($\Delta V_{\mathrm{p}} < V_{\mathrm{d}}$) are excepted. In such cases, the additional component requirement will not arise in order to prevent the body-diode conduction issue in the LDO.

The minimum ON-resistance of MOSFETs use in this project is determined by external connector resistances marked R_{cnt} in Fig. 4.7. The total external connector resistance is typically 6.8 mΩ in a device. A simplified MOSFET model can be represented with a large resistor R_{sub} in parallel with the body-diode and the FET with their resistances R_{d} and R_{chn} respectively as shown in Fig. 4.7 and the two series contact resistances.

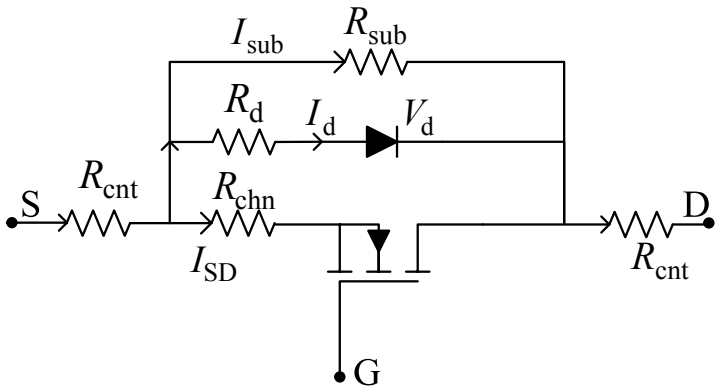


Figure 4.7: A simplified MOSFET model. R_{cnt} are the external metal connector resistance.

The dynamic resistance of diode R_{d} and the dynamic resistance of channel R_{chn} are varying with the source-drain voltage V_{SD} and the currents I_{d} and I_{SD} through those terminals. According to SPICE simulations, R_{d} and R_{chn} resistances are varied from 0 to 10^7 Ω. (More information about the simulations is given in the next chapter.)
The total ON-resistance of the MOSFET pass-element is,

$$R_{\mathrm{ON}} = \frac{R_{\mathrm{d}} R_{\mathrm{chn}} R_{\mathrm{sub}}}{R_{\mathrm{d}} R_{\mathrm{chn}} + R_{\mathrm{d}} R_{\mathrm{sub}} + R_{\mathrm{chn}} R_{\mathrm{sub}}} + 2R_{\mathrm{cnt}} \tag{4.16}$$

If $V_{\mathrm{S}} > V_{\mathrm{D}}$, $I_{\mathrm{SD}} > 0$; the current through R_{sub} is given by,

$$I_{\mathrm{sub}} = \frac{V_{\mathrm{SD}}}{R_{\mathrm{sub}}} \tag{4.17}$$

In the SPICE model of the MOSFET, R_{sub} is a fixed valued resistance of approximate value 10^6 Ω. Therefore, I_{sub} is very small and can be neglected.

The current through the body-diode is given by,

$$I_{\mathrm{d}} = \frac{V_{\mathrm{SD}} - V_{\mathrm{d}}}{R_{\mathrm{d}}} \tag{4.18}$$

The forward characteristic curve of the body-diode in the modified-LDO is illustrated in Fig. 4.8. The current flow through the body-diode of the LDO increases with an increase in the source-to-drain voltage V_{SD}. When voltage V_{SD} reaches about 0.4 V the body-diode starts conducting very small currents. Up to this stage the channel resistance R_{ON} is lower than the diode-resistance R_{d}. When source-to-drain is 0.4 V, and at no load, the body-diode current become dominant and the pass-element of LDO is working as a resistor with a constant value of R_{d}. But for a 5 A load, the current flow in FET channel is dominant until the source-to-drain voltage reaches 0.655 V.

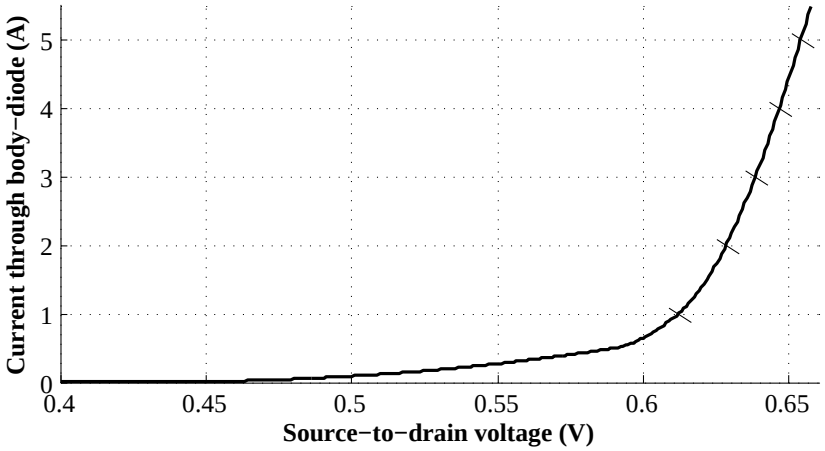


Figure 4.8: The body-diode forward characteristic curve in the modified-LDO which estimated from the measured values of line regulation curves in Fig. 4.11

Above discussed behaviour of the pass-element can be predicted in its line-regulation curve. For different load currents, the output voltage variation of modified-LDO with a 1.5 V, 5 A output capability was simulated using SPICE and the results are illustrated in Fig 4.9. There are three regions of operation the line regulation curve of RS-SCALDO;

1st region: $V_{\mathrm{p}} < V_{\mathrm{reg}} + V_{\mathrm{do}}$ where there is no sufficient dropout voltage for output regulation

2nd region: $V_{\mathrm{p}} \geq V_{\mathrm{reg}} + V_{\mathrm{do}}$ and $V_{\mathrm{d}} > V_{\mathrm{do}}$, where there is sufficient dropout voltage for output regulation and the dropout voltage is less than the diode forward conduction voltage

3rd region: $V_{\mathrm{p}} > V_{\mathrm{reg}} + V_{\mathrm{do}}$ and $V_{\mathrm{d}} < V_{\mathrm{do}}$ where dropout voltage exceeds the diode forward conduction voltage

In the 1st region, the input voltage V_{p} is lesser than the expected regulation voltage V_{reg}, the feed-back loop increases the gate voltage to a maximum of V_{SS} which is the supply voltage. When V_{G} is high, the ON-resistance R_{ON} is smaller than the body-diode

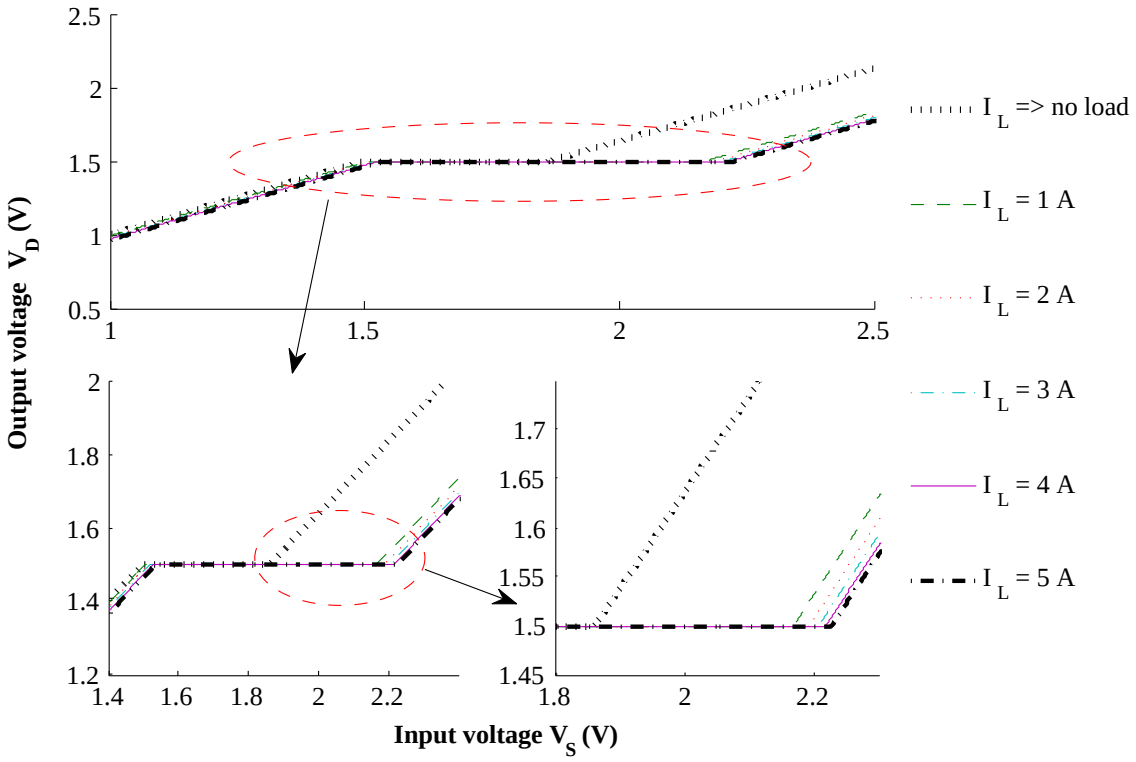


Figure 4.9: Simulation results of modified-LDO (LDO1): Line regulation for different constant load currents from no load to 5 A

resistance R_{d}. In this occasion, the FET function dominates and the current flow is through R_{ON}. The output voltage at the drain terminal V_{D} is,

$$V_{\mathrm{D}} = V_{\mathrm{p}} - I_{\mathrm{SD}} R_{\mathrm{ON}} \tag{4.19}$$

When the input voltage V_{p} is less than or equal to the output voltage, the gate increases to the maximum voltage. Therefore, R_{ON} is very small and will be equal to the external contact resistance.

$$V_{\mathrm{D}} \simeq V_{\mathrm{p}} - 2 I_{\mathrm{SD}} R_{\mathrm{cnt}} \tag{4.20}$$

Since $I_{\mathrm{SD}} R_{\mathrm{ON}}$ is less than the minimum dropout voltage, LDO output voltage is out of regulation. Until the input exceeds the minimum voltage for regulation, the output V_{D} increases linearly with V_{p}. This can be seen in the Fig. 4.9, before the LDO starts to regulate.

The output regulates only when the dropout voltage V_{do} is less than the diode conduction voltage V_{d}) and the input voltage V_{p} is sufficiently high. This occurs in the 2nd region. When LDO is in regulation, the gate voltage V_{G} gets modulated to allow an appropriate current to flow through the MOSFET channel. The current through MOSFET source terminal I_{S} is the sum of the load current I_{L} and the feed-back current I_{FB} through R1 and R2 in the LDO circuit in Fig. 4.6(b). And it is also equal to sum of the current through the channel and body-diode.

$$I_{\mathrm{S}} = I_{\mathrm{SD}} + I_{\mathrm{d}} = I_{\mathrm{L}} + I_{\mathrm{FB}} \tag{4.21}$$

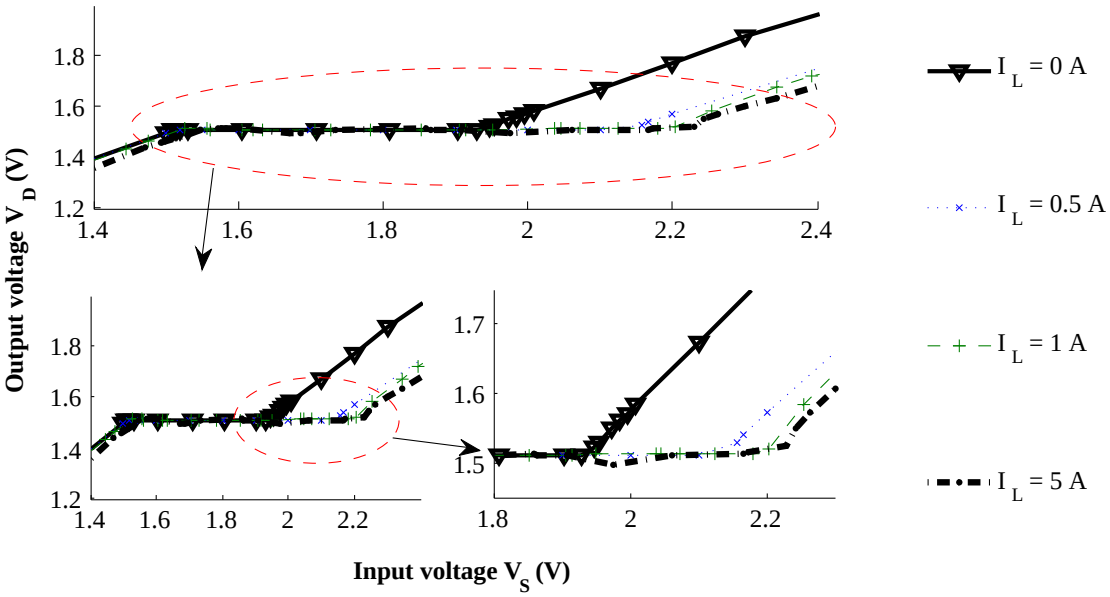


Figure 4.10: Experimental results for LDO1: Line regulation for different constant load currents from no load to 5 A

When the input V_{p} greater than expected regulated voltage V_{reg}, the feed-back loop pulls-down the LDO gate voltage V_{G} from its maximum value V_{SS} to corresponding gate voltage and therefore R_{ON} increases.

$$V_{\mathrm{D}} = V_{\mathrm{p}} - I_{\mathrm{SD}} R_{\mathrm{ON}} \tag{4.22}$$

From this point, the LDO starts to regulate.

If there is no load current, then the only current through the circuit is the feed-back loop current I_{FB}, which is very small as R_1 and R_2 values are in the order of 10^4 Ω. Therefore, the gate voltage V_{G} is very low and R_{ON} is increasing.

With the further increase of V_{p}, the gate-to-source voltage V_{GS} decreases and operation enters to 3rd region. When the channel resistance R_{ON} is greater than the resistance R_{d}, the body-diode dominates and the current starts to flow through it. This is seen in the Fig. 4.9 where regulation stops at no-load. The output voltage $V_{\mathbf{D}}$ at no-load is

$$V_{\mathrm{D}} = V_{\mathrm{p}} - I_{\mathrm{FB}} R_{\mathrm{d}} - V_{\mathrm{d}} \tag{4.23}$$

Since I_{FB}, R_{d} and V_{d} are very small;

$$V_{\mathrm{D}} \simeq V_{\mathrm{p}} \tag{4.24}$$

When V_{p} is greater than the regulation voltage V_{reg} and I_{L} is large, the feedback loop pulls the gate voltage to corresponding voltage and regulates the output voltage. When V_{p} increases, V_{GS} become smaller and increases R_{ON} and decreases R_{d}. At particular V_{p}, the body-diode dominates again while ceasing the output regulation. This behaviour

was observed by LTspice simulation as illustrated in Fig 4.9. Simulation results were confirmed with the experimental results in Fig. 4.10.

Other possible solutions and limitations

For cases which have large voltage variations in input-to-output, the interchanged source-drain of MOSFET pass-element solution is not viable. Instead, MOSFETs can be connected back-to-back as shown in Fig. 4.11(a) and Fig. 4.11(b) either common source or drain. Also a Schottky diode D can be used to block the current path of the body-diode of Q1 in Fig. 4.11(c). MOSFETs Q1 and Q2 can be used as: (i) an LDO pass-element, (ii) an LDO pass-element combined with a switch, and (iii) an LDO pass-element combined with a Schottky diode. Similar solutions used to completely isolate the power source from the load, or from another power source, when the switch is turned off [108]. However, they are used in switches but not in LDOs. These LDO alternatives are described in following section.

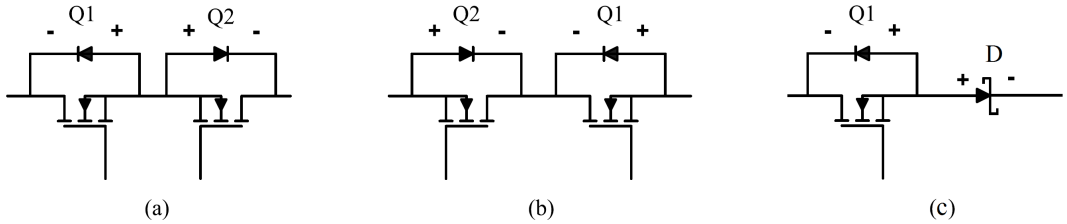


Figure 4.11: N-channel MOSFET blocking the body-diode effect: (a) drain as input and source as output, (b) source as input and drain as output, and (c) drain as input and Schottky diode at output

Figure 4.12(a) and (b) illustrate an LDO pass-element combining Q1 and Q2 back-to-back with common gate. The source terminals are common in Fig. 4.12(a), and the drain terminals are common in Fig. 4.12(b). When the LDO is active the current path is shown with a blue dashed line. Q2 has less resistance than Q1 due to both body-diode and the channel conduction.

The body-diode in Q2 will block any current that can flow from output to input when the LDO is at OFF state in Fig. 4.12(a) and (b). Simulation results shown in Fig. 4.13(a) and (b) indicate a positive results for regulation. The transitional behaviour of Q1 and Q2 are presented with their differential voltages V_{Q1} and V_{Q2} along with differential voltage of the combined Q1, Q2 MOSFETs V_{Q1Q2}. The output voltage performance of these solutions is illustrated in corresponding V_{op} curve.

Figure 4.12(c) illustrates that Q1 used as LDO pass-element and Q2 as a switch. When they are at ON state, the body-diode of Q1 is reverse-biased from input to output so no current flows through it, though Q2 creates an additional current path. These configurations in Fig. 4.12 illustrate similar regulation performance except for the Schottky diode configuration in Fig. 4.12. Until the Schottky diode reaches its forward conduction

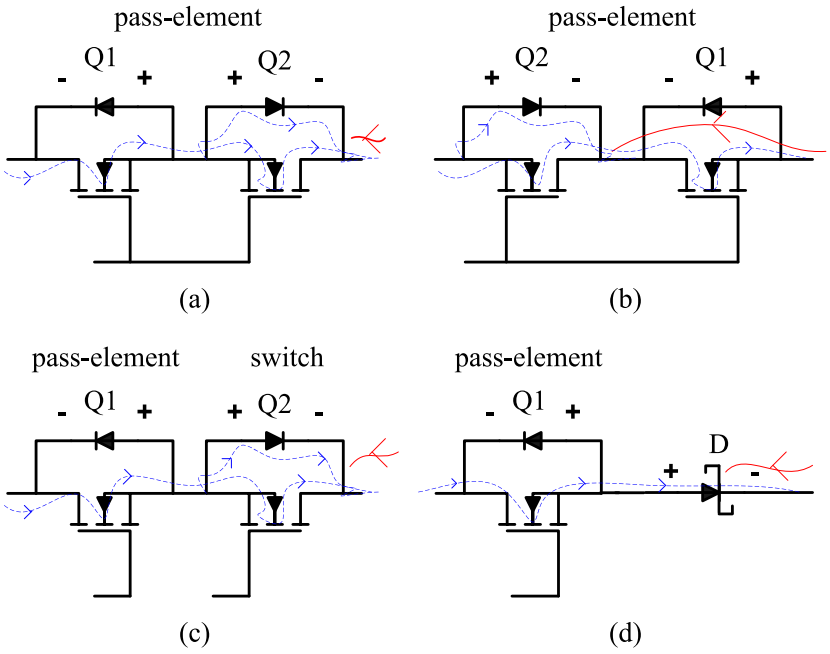


Figure 4.12: Alternative implementations of LDO pass-elements: a) two MOSFETs with common source and gate, (b) two MOSFETs with common drain and gate, (c) MOSFET pass-element and switch with common source, (d) MOSFET pass-element and Schottky diode

voltage, the output will not regulate as illustrated in Fig. 4.13(d). Therefore, the dropout and the losses in this configuration are higher than other solutions.

The alternative solution in Fig. 4.12(a) was implemented, tested and compared with simulation results. Practically, when the load current increases the output voltage decreases. When compared to the simulation results, a difference of about 20 mV can be seen. By adjusting feedback sampling resistors, this difference can be reduced.

The LDO in Fig. 4.14(a) illustrates an alternative solution where two MOSFETs are connected with common source terminals. When a constant current I_{D} is drawn from the load, the voltage across Q1 MOSFET is

$$V_{\mathrm{Q1}} = I_{\mathrm{D}} R_{\text{chn-DS1}} \tag{4.25}$$

where $R_{\text{chn-DS1}}$ is the drain-source channel resistance of Q1.

Since the body and the source are connected, the body-drain diode and the source-drain channels can be considered as parallel. Therefore, voltage across Q2 MOSFET is

$$V_{\mathrm{Q2}} = I_{\mathrm{D}}[R_{\text{chn-SD2}} // R_{\text{d-BD2}}] \tag{4.26}$$

where $R_{\text{chn-DS1}}$ is the drain-source channel resistance of Q2 and $R_{\text{d-BD2}}$ is the resistance of body-drain diode of Q2.

$$I_{\mathrm{D}} = \frac{V_{\mathrm{Q1}} + V_{\mathrm{Q2}}}{R_{\text{chn-DS1}} + [R_{\text{chn-SD2}} // R_{\text{d-BD2}}]} = \frac{V_{\mathrm{Q1Q2}}}{R_{\text{chn-DS1}} + [R_{\text{chn-SD2}} // R_{\text{d-BD2}}]} \tag{4.27}$$

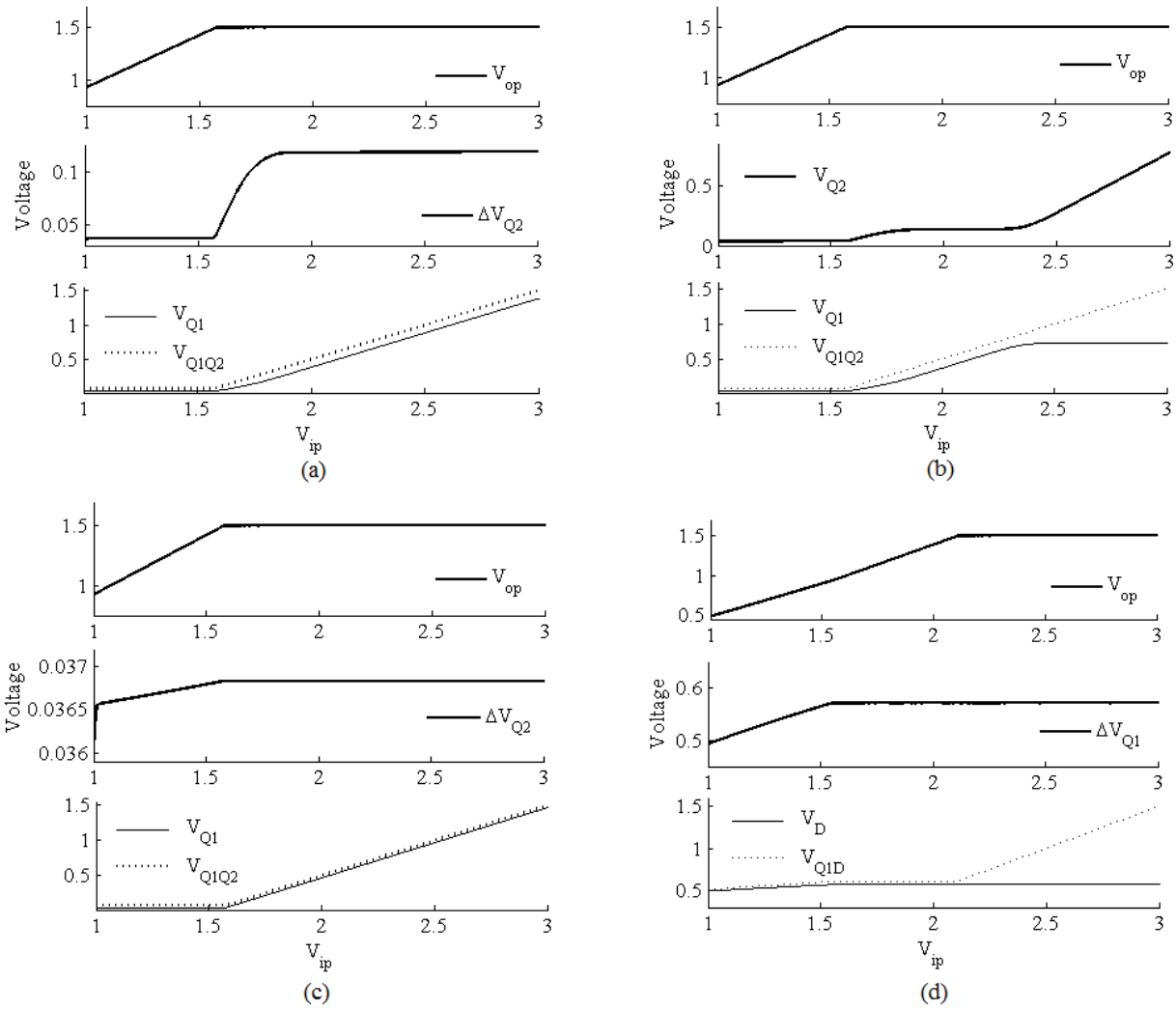


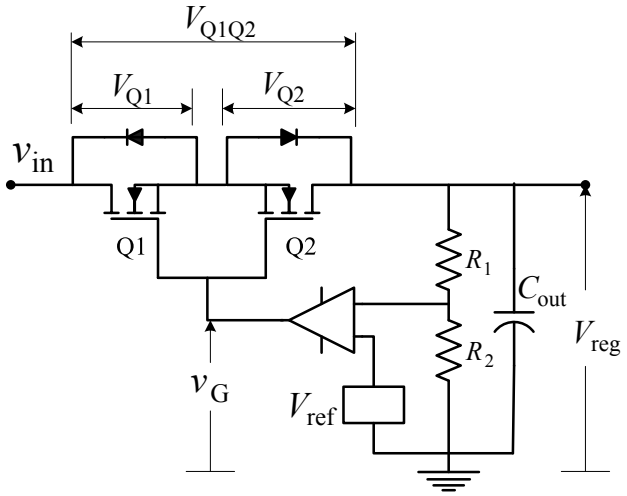
Figure 4.13: Voltage regulation and related simulation graphs of Fig. 4.12 (a) LDO with common source, (b) LDO with common drain, (c) LDO and switch with common source, (d) LDO and Schottky diode. This configuration has large dropout

The output voltage of LDO V_{reg} is

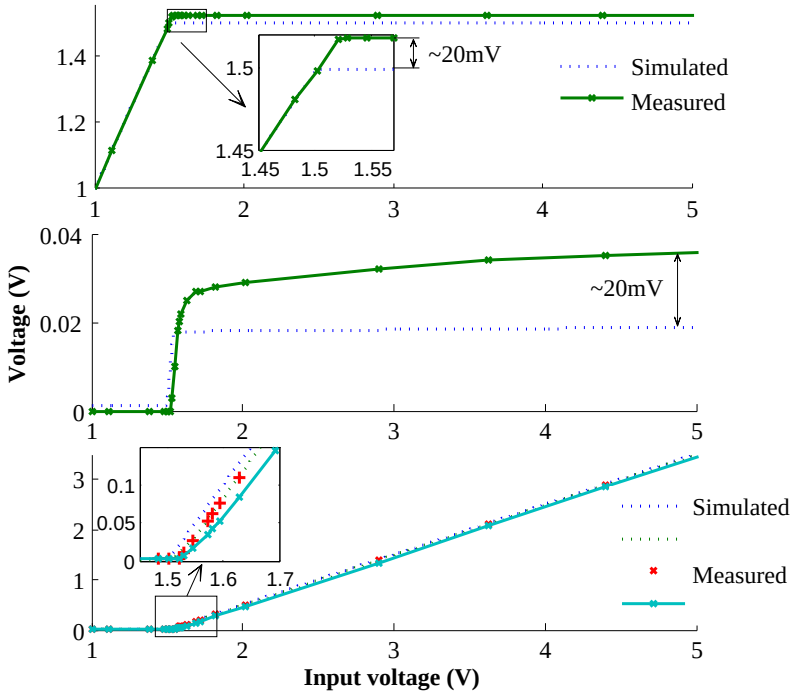
$$V_{\text{reg}} = V_{\text{in}} - \{R_{\text{chn-DS1}} + [R_{\text{chn-SD2}} // R_{\text{d-BD2}}] I_{\text{D}}\} \tag{4.28}$$

$$V_{\text{reg}} = V_{\text{in}} - \left[R_{\text{chn-DS1}} + \frac{R_{\text{chn-SD2}}.R_{\text{d-BD2}}}{(R_{\text{chn-SD2}} + R_{\text{d-BD2}})}\right] I_{\text{D}}$$

Comparing all the four alternatives in Fig. 4.12, the remedy shown in Fig. 4.5(c) has fewer components, therefore less complexity, and satisfied the requirements of the proof-of-concept prototype. Further, if the solutions in Fig. 4.12 are implemented using discrete components, they add more series resistance (in the metal contact terminals) than the single MOSFET-based implementation. The additional metal contacts in the LDO in Fig. 4.14(a) can be reduced by implementing an integrated circuit.



(a)



(b)

Figure 4.14: Voltage regulation and related simulation graphs of Fig. 4.12 (a) LDO with common source, (b) a comparison of simulated and experimental results

4.3 RS-SCALDO for application of VRMs

The basic SCALDO configuration with one supercapacitor was used to develop a high-current ($\leq$ 5 A) version. In order to demonstrate the applicability of RS-SCALDO to VRM, essential functional specifications were drawn up: a tight output voltage tolerance of $\leqslant \pm 20$ mV at load current 5 A for an output voltage adjustable from 1.45 to 1.55 V at

50 mV step with an input voltage ranging from 3.55 to 3.95 V. A pair of LDOs and two power switches were used with a large capacitance (50–310 F) in the design.

4.3.1 RS-SCALDO design

The power stage circuit of RS-SCALDO consists of pair LDOs and two switches and a SC. LDOs and switches were built with discrete MOSFET in order to (i) enable high-current capability, (ii) prevent body-diode effect, (iii) achieve a voltage dropout less than 80 mV in high-current LDO and (iv) minimize ON-resistance losses in switches. As mentioned in the previous section, the parasitic body-diode is an intrinsic feature which cannot be eliminated from a single power MOSFET. If the LDO1 uses a standard pass-element as shown in Fig. 4.5(b) the RS-SCALDO operation cannot be performed. This requires a slightly different pass-element such as Q6 in Fig. 4.5(c). The design allows us to use commercially available power-MOSFETs for switches. It is possible to implement a common feedback control circuit for both LDOs regardless of their pass-element orientations, thereby reducing component count. A simplified diagram of the common feedback control circuit is illustrated in Fig. 4.15. The circuit consists of two analogue switches at each gate of the pass-element. Enabling signal (EN) activates the corresponding analogue switch during charging and discharging phases. Resistors $R1$ and $R2$ are used to prevent floating gate voltages.

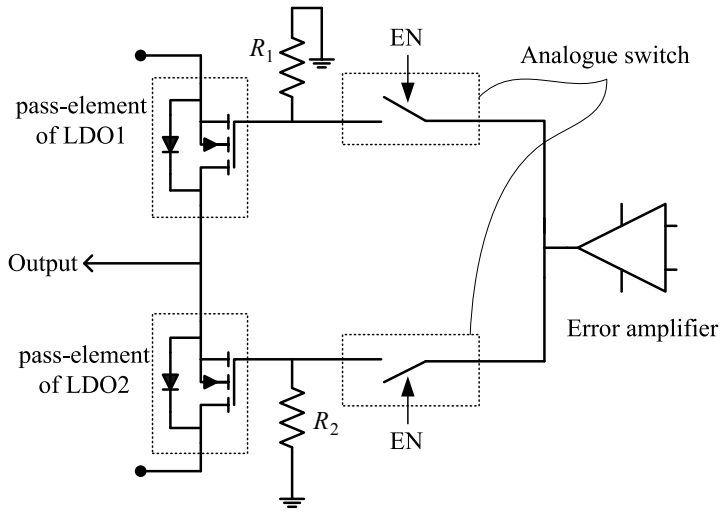


Figure 4.15: Simplified diagram of a common feedback control circuit

As discussed in Chapter 1, modern VRMs can adjust their output voltage via microprocessor command to suit different working conditions [12]. Usually, digital pulse width modulation (DPWM) is used to adjust the output-voltage in SMPS-based VRMs [31]. To implement this feature in RS-SCALDO, the voltage divider at the LDO output was replaced with a digital potentiometer as illustrated in Fig. 4.16. This technique is comparatively uncomplicated and less expensive than DPWM-based designs.

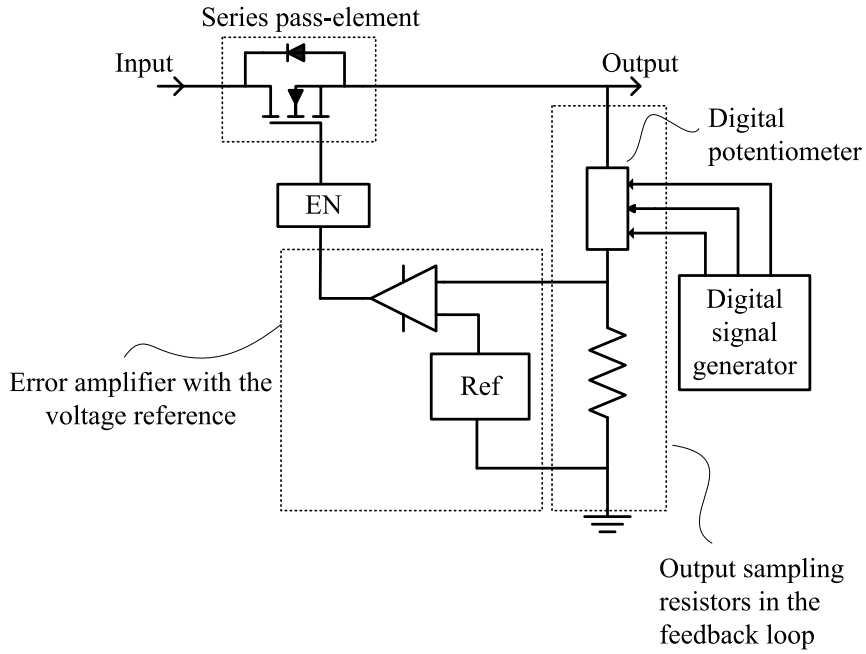


Figure 4.16: Illustration of implementation of VID

Figure 4.17 shows a simplified block diagram of RS-SCALDO. Q1 and Q2 are the pass-elements of the LDOs. According to the RS-SCALDO switch-reduction strategy discussed in Chapter 3 and [54], these LDOs (with pass-elements Q1 and Q2) alternatively power the load. The two discrete MOSFET-based switches SW1 and SW2 connect the supercapacitor SC to the unregulated power supply and ground during charge and discharge phases. They are operated using a simple low-power gate-drive circuit that consists of signal MOSFETs. Digital control signals enable and disable these switch drivers.

LDOs and two switches are built using AUIRL3705 N-channel MOSFETs. A common feedback loop with an error amplifier OP491 [109] from Analog Devices is used to drive both pass-elements of LDOs. The error amplifier requires very low current (of about 300 μA/A) and has a small offset voltage of 700 μV. The control circuit has bilateral analogue switches HEF4016B [110] from Philips (NXP) for signal gating; these control the LDO feedback and the voltage sensing signals. A prototype model of a 3.5-to-1.5 V is available in Appendix B.8(c).

The brain of the control circuit is a low-power digital micro-controller PIC16F684 [111] from Microchip. It has 12 input-output pins including a 10-bit ADC. Their in-out directions can be controlled individually. An ADC signal senses the corresponding input voltage of the LDO as illustrated in Fig. 4.18 and compares this with the system specified voltage. If it is not greater than the sensed voltage, the controller sends signals to enable the relevant LDO and switch to change the SC between charging-discharging phases appropriately. Corresponding PIC program of this operation is in Appendix B.

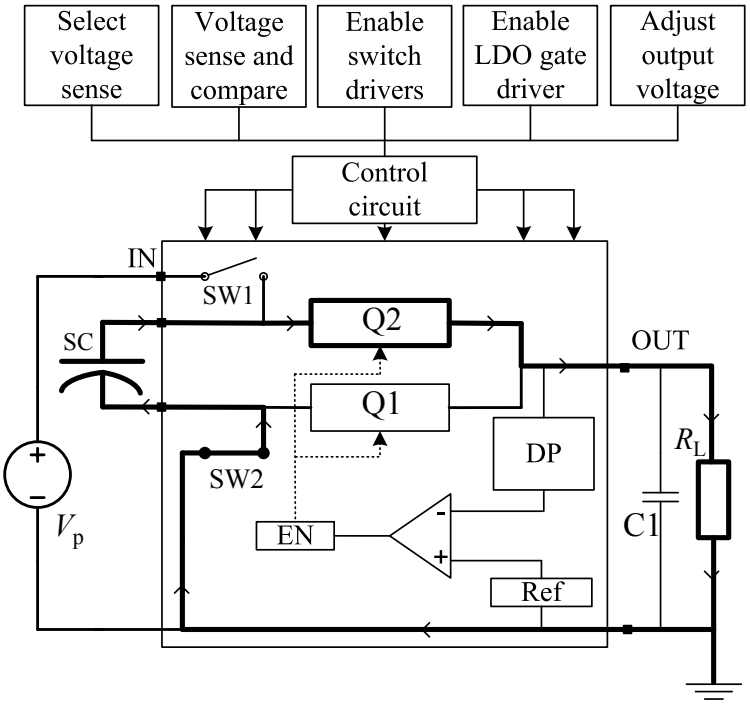


Figure 4.17: Block diagram of RS-SCALDO

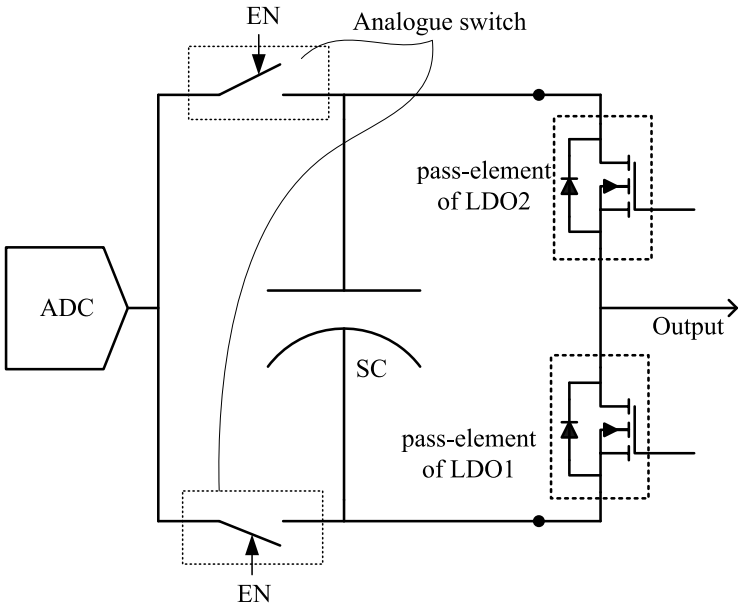


Figure 4.18: Simplified diagram of an analog to digital converter (ADC) senses the corresponding input voltage of the LDO

4.3.2 Test setup and bench measurements of RS-SCALDO

The test setup of the RS-SCALDO included (i) a 3.5-to-1.5 V, 5A RS-SCALDO prototype, (ii) 10 A and a 2.2 A power supplies, (iii) a solid-state electronic load (SSL) with maximum 150 A, 300 W capability, (iv) a digital oscilloscope with 4 isolated channels, (v) an AC/DC current probe range from 1 to 50 A/V.

SSL is an electronic load developed using parallel MOSFET array, where it can simulate an electrically variable resistance. It is applicable to different operating modes; (i) constant current (CC), (ii) constant resistance (CR), (iii) constant power (CP), and (iv) constant voltage (CV). For this project CC mode of the model PXL-151A [112] was used.

Appendix B.10 illustrates the test setup of the prototype. The steady state voltage and current was measured using true RMS multimeters. TPS2000 (10 A) and TPS4000 (2.2 A) power supplies were used to energizing the power stage and control-stage respectively. SSL provided the constant and dynamic current waveforms required for the tests. A dummy digital signals generator was used as the processor signals to send data to the digital potentiometer that change to the required output voltage. The performance of RS-SCALDO was measured in basic terms of line and load regulation, efficiency and transient response. Results were compared with the theoretically set values.

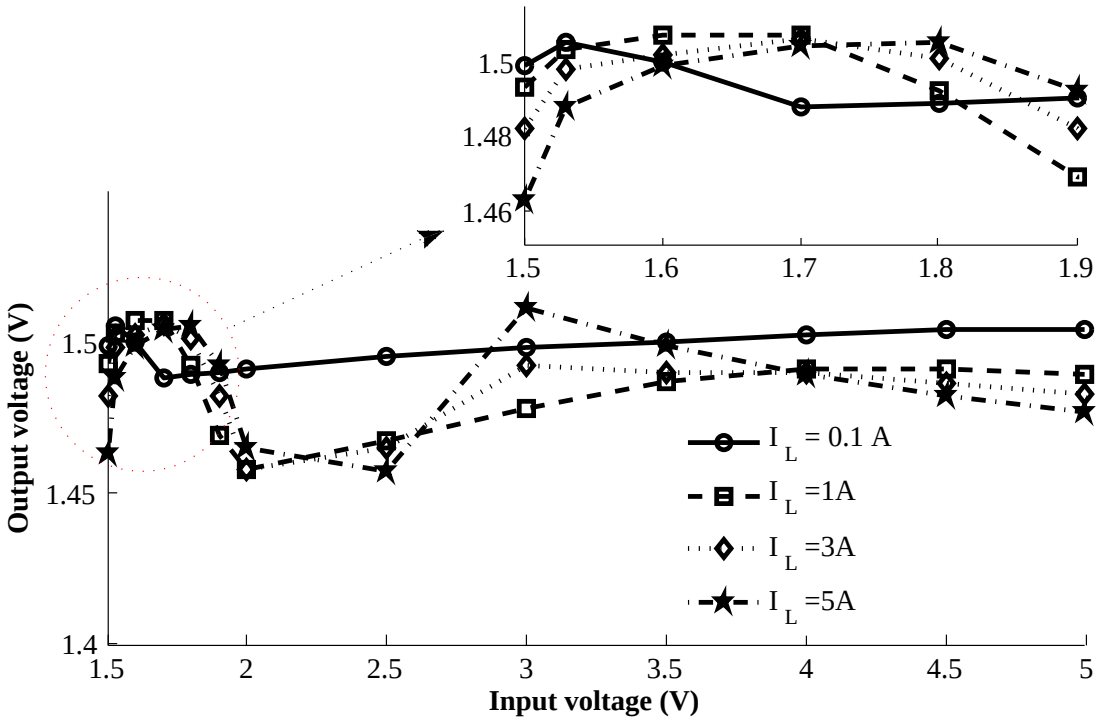


Figure 4.19: The line regulation of the standard LDO (LDO2) at different constant loads from 0.1 to 5 A

Line and load regulation performance of standard-LDO (LDO2) are in Fig. 4.19. The modified-LDO regulates within a limited dropout voltage range from 35 mV to 425 mV for no load to 5 A (Fig. 4.10). In this range, the LDO1 has slightly better regulation than LDO2 in Fig. 4.19 and 4.20 respectively. Within the specified input voltage range in Table 4.2, the performance of LDO1 and LDO2 are similar.

Figure 4.21 indicates line regulation for different load currents of an RS-SCALDO circuit which reflect the modified-LDO (LDO1) characteristics. The best input voltage

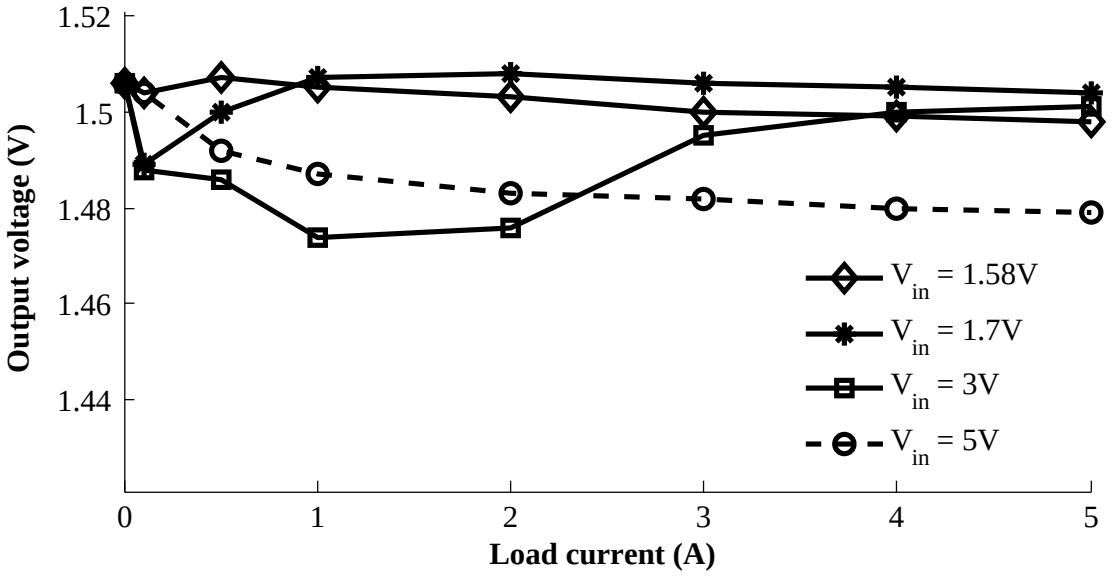


Figure 4.20: The load regulation of the standard LDO (LDO2) at various input voltages

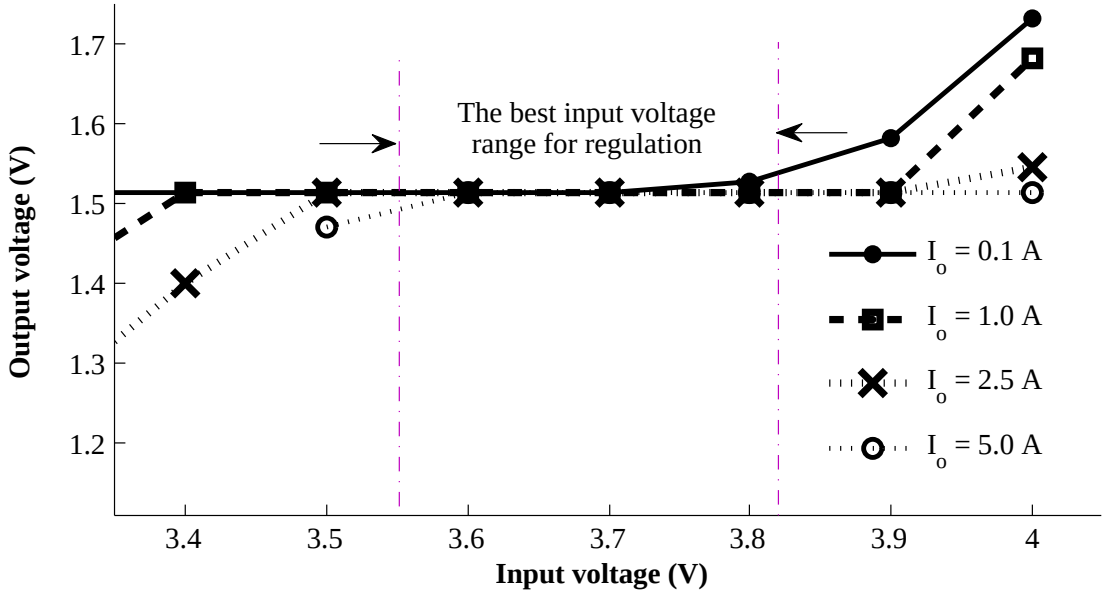


Figure 4.21: RS-SCALDO line regulation performance: the best input voltage range for output regulation at different constant loads from 0.1 to 5 A

range for output regulation is marked in the Fig. 4.21. However, the predicted input voltage range is shrink by a 9%.

To adjust the output voltage of the RS-SCALDO, a digital potentiometer AD8400 [113] was used by replacing the two-resistor voltage divider in the LDO feedback loop. There, the VID logic was implemented using a 8-bit code with two control bits. This provides a 5.859 mV resolution for 1.5 V output.

Three set output voltages (1.45, 1.50, and 1.55 V) were tested. As shown in Fig. 4.22, the measured end-to-end efficiency of overall RS-SCALDO of 81 to 86 % at 5 A load compares well with theoretical ideal of 83.6 to 89.5 %. The losses were reduced by utilizing

a capacitor BCAP310 from Maxwell with ESR typically in 2.2 mΩ [97]. Further the large capacity reduced the operating frequency of the RS-SCALDO. An estimation for maximum power consumption in the control circuit is presented in Appendix: B.

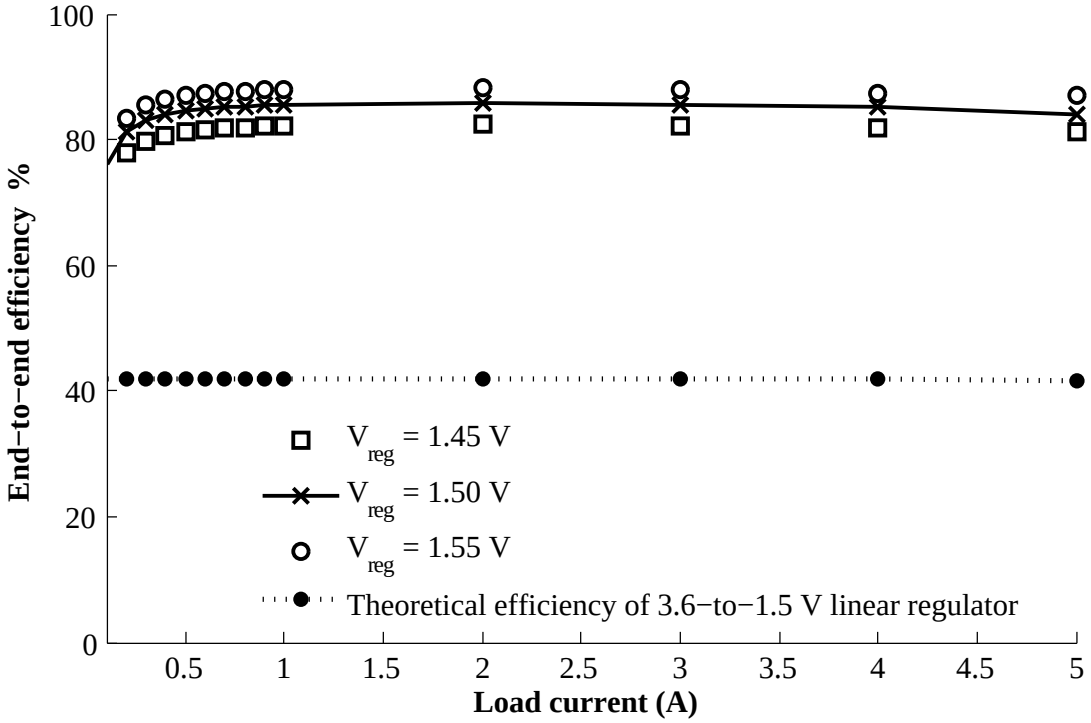


Figure 4.22: End-to-end efficiency of RS-SCALDO with VID logic

By selecting different values for SC over the range from 1 to 310 F [97,114], circulation frequency can be varied from 1 to 600 mHz as shown in Fig. 4.23, with minimum dynamic losses occurring in power switches SW_C and SW_D. Consistent with theoretical prediction, the log-log graph shows the frequency is inversely proportional to capacitance. The deviations at the lower-end of Fig. 4.23 arose from the higher equivalent series resistance of the lower-capacity SCs.

The transient response of the RS-SCALDO was measured for slew rates 25 A/μs. The SSL was set to the slew rate 25 A/μs of 0.2 to 5 A load transient for a 8 kHz waveform. Both 37.5 A and 150 A ranges in SSL were used with setting as shown in Table 4.3.

Table 4.3: Current transient settings of SSL

Item		Setting
Discharge mode		constant current (CC)
37.5 A range	Setting range Resolution	25 A/μs; 0.2 to 5 A 0.25 A/μs
150 A range	Setting range Resolution	25 A/μs; 0.4 to 5 A 0.5 A/μs
Frequency of the signal		8 kHz
Duty cycle		50%

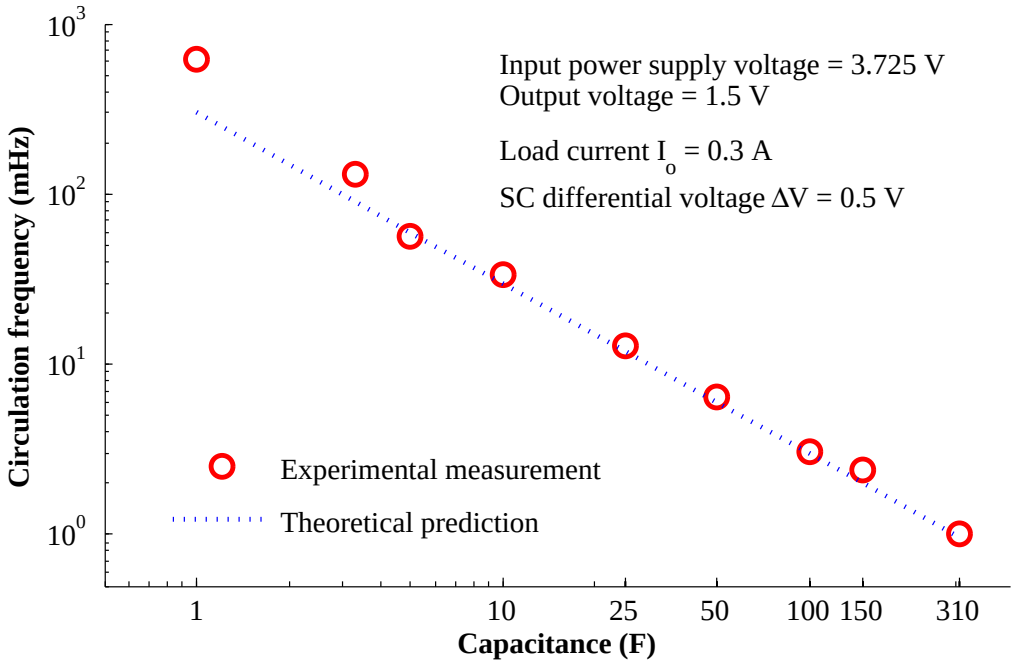


Figure 4.23: SC energy circulation frequency of RS-SCALDO with different-value capacitors

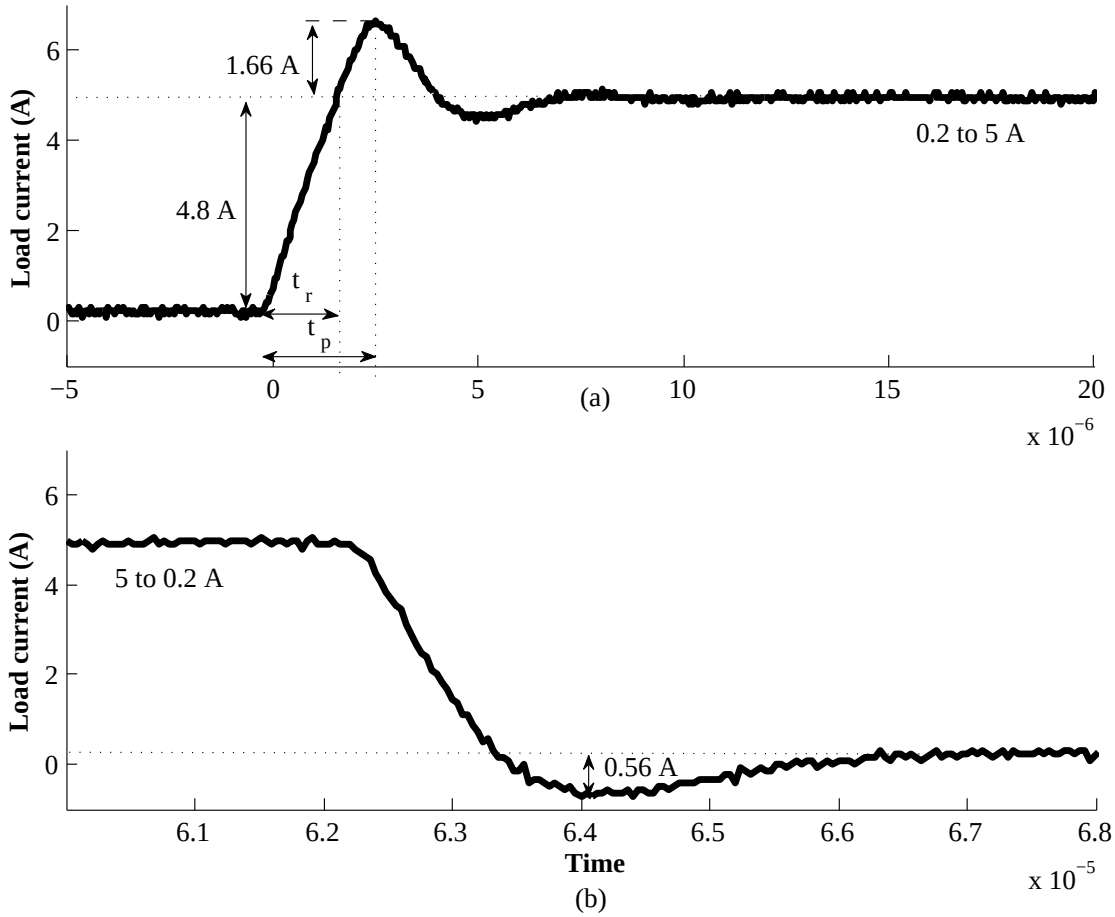


Figure 4.24: Load transient behaviour of 0.2-to-5 A with slew rate 25 A/μs: (a) rising from 0.2 to 5 A, (b) falling from 5 A to 0.2 A

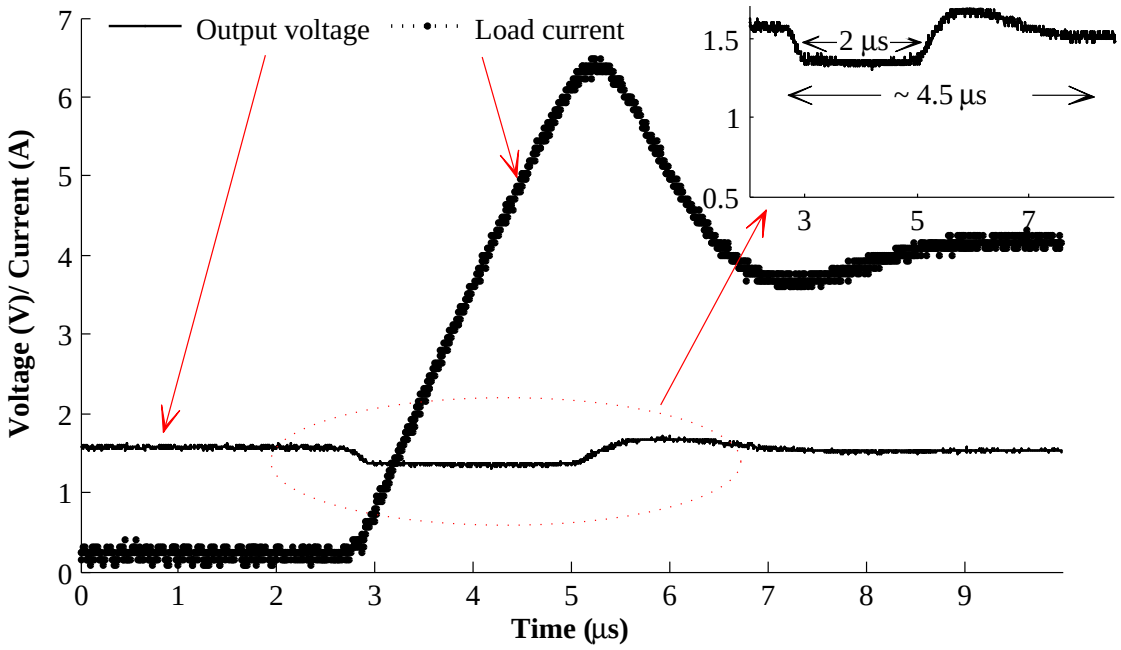


Figure 4.25: Transient response of RS-SCALDO with output voltage 1.5 V. 150 F SC was used in this experiment

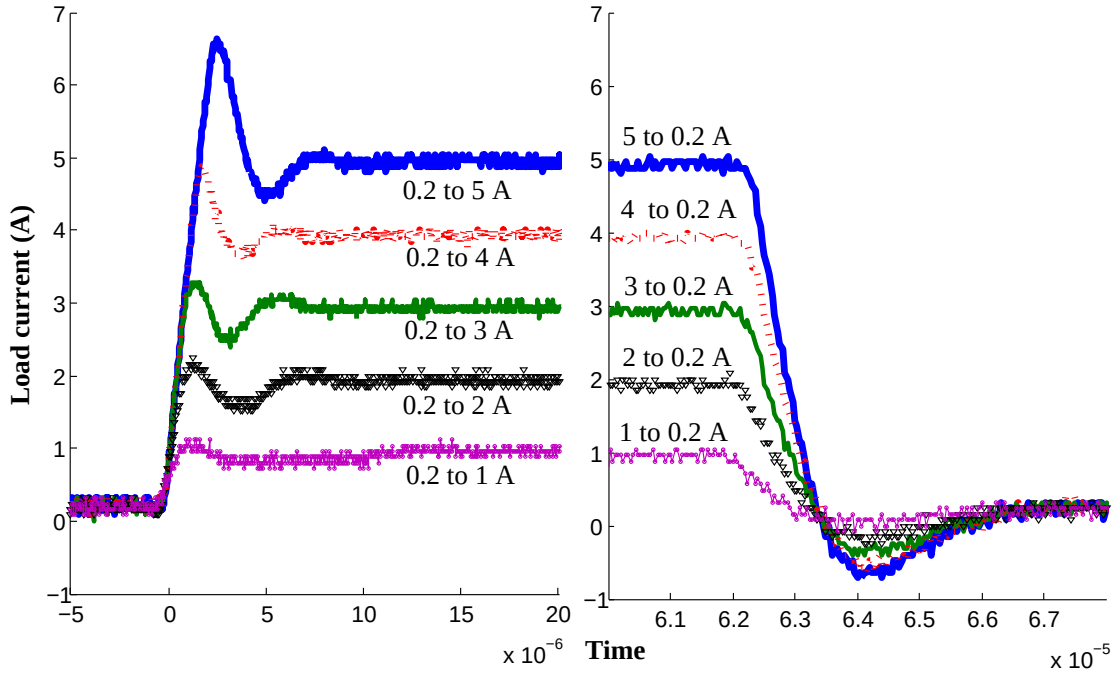


Figure 4.26: Transient behaviour of the load with 25 A/μs: (a) rising from 0.2 to 5 A, (b) falling from 5 to 0.2 A

Overshooting current of about 1.66 A was found in the load transient wave at the rising side at maximum current of 5 A. At falling edge the overshoot was about 0.56 A. This was reflected in the RS-SCALDO output signal as seen in Fig. 4.27. RS-SCALDO has a good transient settling behaviour which is less than 20 μs. However, during transient, a 0.18 V sag and a 0.15 V swell can be found for 2.5 μs. The transient behaviour was

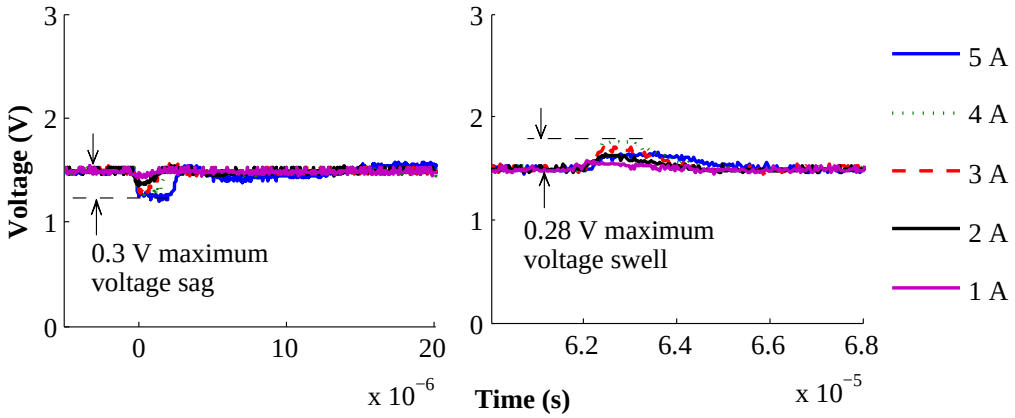


Figure 4.27: Transient response for different loads with 25 A/μs: (a) rising from 0.2 to 5 A, (b) falling from 5 to 0.2 A

observed for both SC-charging and discharging phases in RS-SCALDO. Similar transient characteristics were obtained in SC-charging and discharging phases as well as in both operating modes of SSL (37.5 A and 150 A).

3.6-to-1.5V, 1 A SMPS-based approaches in Fig. 1.9 achieved a maximum $\sim$ 80-83% efficiency at 0.5 A load. Compared to SMPS-based approaches, RS-SCALDO linear method achieves similar efficiency. Due to resistance in the power path (i.e. PCB rail, SC and MOSFETs) the experiment input voltage has to be increased to 3.6 V nominal value. For the input voltage range of 3.55–3.82 V, line regulation tests obtained a 1.5 V $\pm$15 mV output regulation. Though the overshoot voltage of RS-SCALDO is nearly six times larger, a reduced settling time of 4.5 μs was obtained.

Table 4.4: Comparison of results with Intel specifications

Parameters	Theoretical (Intel)	Experiment results (RS-SCALDO)
Input voltage range (V)	3.135–3.465	3.55–3.82
Nominal Input voltage (V)	3.3	3.6
Load line (maximum)	$V_{\text{reg}}-$ (0.8mΩ $\times I_{\text{L}}$)	V_{reg}*
Load line (minimum)	$V_{\text{reg}}-$ (0.8mΩ $\times I_{\text{L}}$)-30 mV	$V_{\text{reg}}-$ (2.4mΩ $\times I_{\text{L}}$)-30 mV**
Overshoot voltage (V)	0.05	0.28
Overshoot time (μs)	25	4.5

*Input voltage range of 3.55–3.75 V

**Input voltage 3.5 V

The new RS-SCALDO approach changes the topology without compromising the desired efficiency ($2V_{\text{reg}}/V_{\text{p}}$). Implementation of digital potentiometer-based dynamic output voltage capabilities was successful. Compared to a generalized SCALDO with $3n+1$ switches (for a case of n supercapacitors) in the RS-SCALDO topology only $2n$ are required.

Chapter 5

Simulation and analysis of RS-SCALDO

LDO pass-elements and switches in the power stage of RS-SCALDO are implemented with discrete-MOSFETs; in this project enhancement-mode, N-channel devices are used. There were many reasons to select N-channel over P-channel devices; most importantly their ability to support very low dropout at low-input voltages, inherent fast performance, and low ON-resistance.

This chapter reviews the basic physics of power MOSFETs and applies it to the SCALDO models used in this project. The theoretical analysis allows us to predict circuit performance. SPICE, along with some MATLAB simulations, is used to analyze the behavior of components and functional blocks of the RS-SCALDO circuit. Simulation results are compared with bench measurements to determine operational boundaries and expose challenges in a discrete-component-based design. This information will assist in design of an integrated SCALDO circuit in the future.

5.1 Power MOSFETs

Four-fifths of component count of RS-SCALDO power stage is used discrete power-MOSFETs. These operate in two quadrants of the voltage-current plane: the two switches and LDO2 operate in the first quadrant while the modified-LDO (LDO1) operates in the third. In order to analyze RS-SCALDO, it is important to investigate the behaviour of MOSFETs in both regions.

The history of the metal-oxide-semiconductor field-effect transistor (MOSFET) concept goes back to the 1930s [115]. However, it was not successfully demonstrated until the 1960s due to the issues arose in control and reduction of the surface states with early fabrication technologies. The surface states is a result of formation of a low quality oxide on a bare semiconductor surface when exposing to air or low vacuum [116].

MOS implies the structure while FET is related to its basic operation. An N-channel MOSFET consists of two heavily doped N-channel regions named *source* and *drain*; these are separated from a metal-deposited *gate* region by a thin oxide layer that provides excellent electrical insulation. The gate, source, drain and body regions (optional) have metal contacts connecting to the external environment. Figure 5.1 illustrates a schematic

diagram of an N-channel power MOSFET and its device symbol. In operation, a voltage signal applied to the oxide-insulated gate electrode can generate a channel to conduct a current which flows between source and drain. The MOSFET is in its conducting or ON-state when its gate-to-source voltage is above a specific threshold value, typically in the range 1–4 V. For gate voltages less than the threshold, the device remains in the OFF-state.

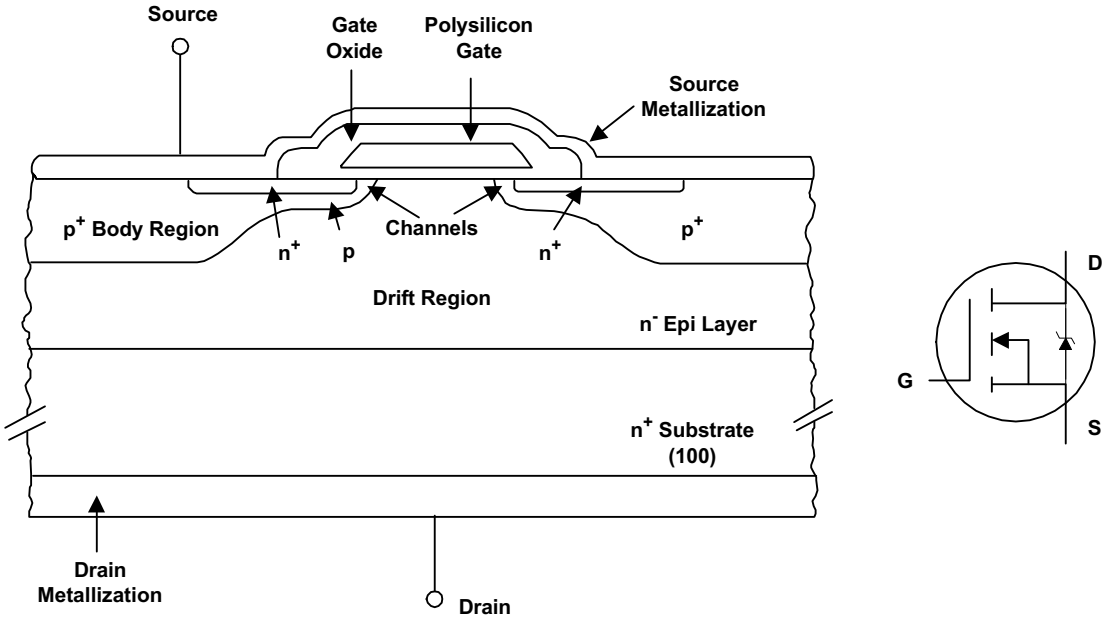


Figure 5.1: Schematic diagram for an N-channel power MOSFET and its device symbol [117]

In early fabrications the device had a conducting channel between the source and the drain even without the application of a gate voltage. It was only possible to deplete this existing channel by applying a negative voltage to the gate of the N-channel device (or a positive voltage to a P-channel device), hence they were known as *depletion-mode* devices. Later, the fabrication process was improved to eliminate the surface-states. These newer devices do not have a conduction channel unless an appropriate voltage is applied to the gate. These so-called *enhancement-mode* MOSFETs are the most commonly used devices at present.

MOSFETs are categorized based on their capabilities for handling voltage, current or frequency. This chapter focuses on *power* MOSFETs, which can operate at significantly higher power levels compared to standard devices, but are otherwise similar to standard MOSFETs.

Summary comparison of BJT with MOSFET devices

In modern power electronics power MOSFETs are in common use by power-system designers, and have largely displaced bipolar junction transistors (BJTs). Although the cost of fabrication is high compared to BJTs, MOSFET technology has many advantages.

MOSFET advantages include: efficient gate drive, fast switching speed and excellent paralleling capability. A comparison between BJT and MOSFET devices is presented in Table 5.1.

Table 5.1: Summary comparison of BJT with MOSFET devices [118]

BJT	MOSFET
Fewer layers to fabricate; therefore, low cost	Multi-layer fabrication and higher cost than BJT
Minority carrier	Majority carrier
Current control device; output is controlled via base current	Voltage control device;Output is controlled via gate voltage
Relatively slow turn-off characteristics (current tail)	Fast on-off characteristics
Negative temperature coefficient	Positive temperature coefficient
Paralleling of BJTs is difficult	Paralleling of MOSFETs is easy

Though the geometry, voltage and current levels are different, modern discrete power MOSFET processing techniques are similar to those for integrated circuits (IC). BJT has a negative temperature coefficient so that forward voltage decreases with increasing temperature. Therefore, paralleling them is difficult as it can lead to thermal runaway and device destruction. In contrast, MOSFETs are easy to parallel as they have a positive temperature coefficient [118]. However, for a single device higher temperatures result in higher power dissipations due to the increase of ON-resistance.

Simple gate-drive circuitry is sufficient to control current in a power MOSFET, whereas a power BJT requires a more complicated base driver. Due to the current tails [119, 120], BJTs cannot turn off as fast as MOSFETs. BJT rise and fall times are hundreds of times greater than those of power MOSFETs which are of the order of nanoseconds. Therefore BJTs are usable at frequencies lower than 100 kHz while MOSFETs can operate up to 1 MHz. However, switching losses in MOSFETs increase significantly with operating frequency.

If the RS-SCALDO were to use BJT for switches and LDOs the body-effect issue disappears. However, the delay and the current tails in switching-off process can cause the SC to discharge unnecessarily and a very low dropout in LDOs cannot be achieved.

5.2 Basic device structure and operation of power MOSFETs

Most power MOSFETs have a vertical structure with the source and the drain on opposite sides of the wafer allowing high-current and voltage values. Vertical power MOSFETs are even categorized on their physical structures. Double-diffused metal-oxide-semiconductors (DMOS) are commonly used in power applications, further categorized into two structures: (i) vertical MOS (VDMOS) that are capable of handling high current/voltage (100 A, 40-60 V) applications, and (ii) double-diffused drain (DDDMOS) [121].

The two most common vertical structures, trench and planar, are shown in Fig. 5.2 [122]. The basic difference is the presence of a junction gate field-effect transistor (JFET) parasitic in the planar. The trench structure has a high channel density and thus lower ON-resistance yet are more difficult to manufacture than planar devices [123].

An epitaxial-silicon layer, also known as *epi*, controls the amount of blocking voltage the MOSFET can sustain. The ON-resistance of planar is dominated by epi-layer resistance and therefore, high cell density is not beneficial [123]. When scaled-down to smaller dimensions, current is constrained to flow in a narrow N-region by the adjacent body region. Due to the absence of JFET in trench structures, high density scaling is possible to achieve very low ON-resistance.

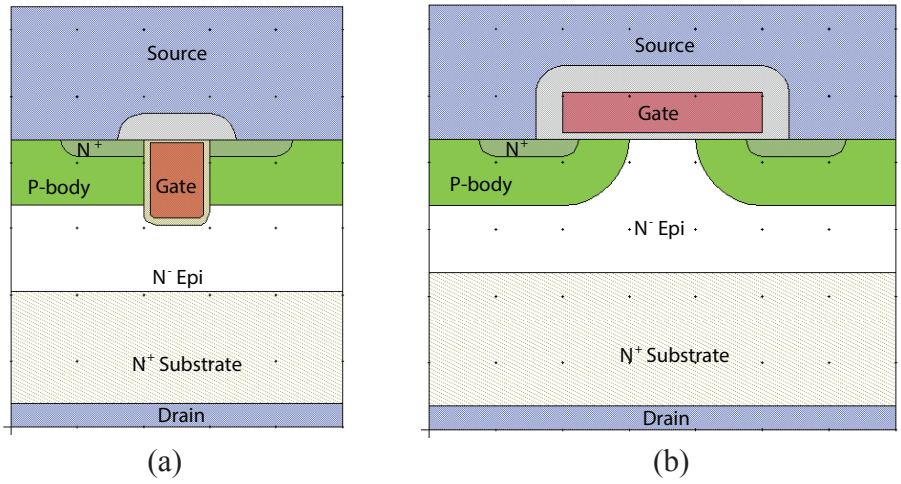


Figure 5.2: Power MOSFET structures: (a) trench, (b) planar [122]

When there is no signal applied to the gate, a power MOSFET can hold a high input voltage in the drain through the N^- epi and P^+ body junction. Thicker, lightly doped epi can withstand high breakdown voltages has high ON-resistance losses. In lower-voltage devices, body thickness and doping are sufficiently high to prevent the depletion region punching through to the N^+ source and cause low breakdowns [122]. However, over-designed epi and body can increase channel resistance and threshold voltage.

There are many parasitic components present in these structures arising from the multiple layers in the MOSFET. ON-resistance is one of the main concerns in this research

when selecting a suitable device from the voltage spectrum in Fig. 5.3, since it determines the minimum dropout voltage of an LDO and the losses via switches.

Figure 5.3 illustrates the relative importance of layers and their resistive components that contribute to ON-resistance for different voltage ratings. Channel resistance, metalization, metal to semiconductor contacts, and lead frame are dominant in low voltage devices while epi-resistance and JFET components are dominate in high voltage devices. The ON-resistance of low voltage MOSFETs is primarily dependent on channel resistance. Selecting low voltage MOSFETs was beneficial for the implementation of LDOs and power switches in RS-SCALDO due to the controllability of channel resistance.

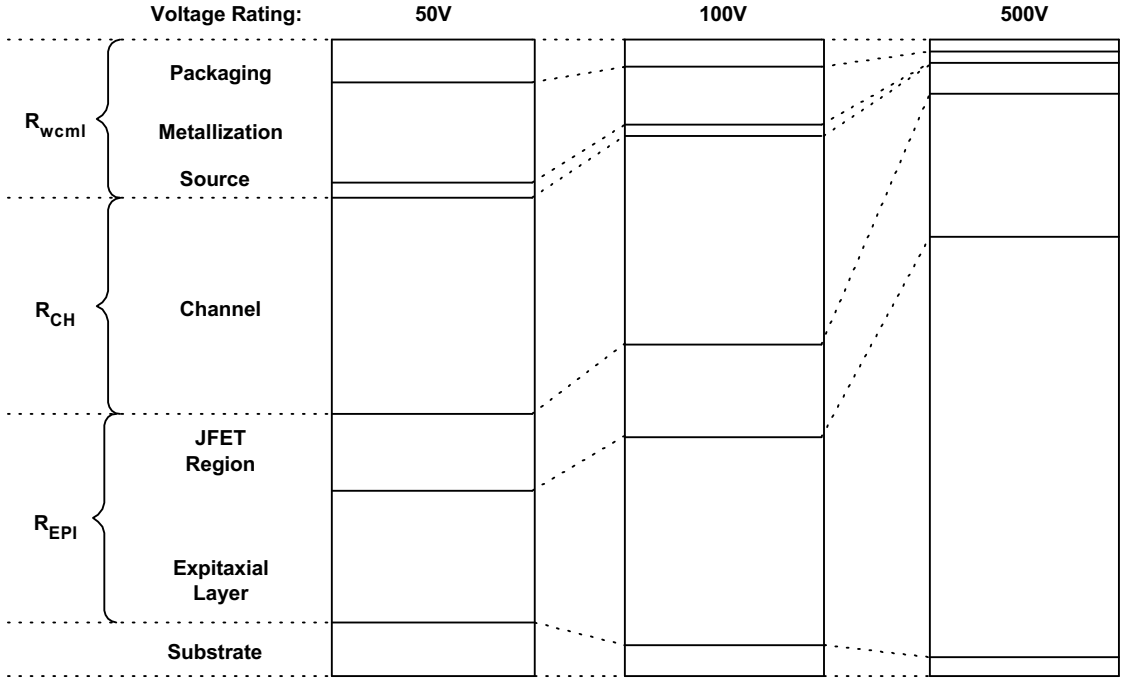


Figure 5.3: Relative contributors to planar MOSFET ON-resistance with different voltage ratings [117]. R_{wcml} is sum of bond wire resistance, R_{CH} channel resistance, and R_{EPI} epi resistance

For a trench MOSFET, R_{ON} consists of source resistance R_{S}, channel resistance R_{CH}, resistance from the accumulation region R_{ACC}, resistance from epi R_{EPI}, and resistance from the silicon substrate R_{SUBS} on which the epi is grown:

$$R_{\mathrm{ON}} = R_{\mathrm{wcml}} + R_{\mathrm{CH}} + R_{\mathrm{EPI}} + R_{\mathrm{SUBS}}$$

where $R_{\mathrm{wcml}}$is the sum of bond wire (R_{w}), contacts of source (R_{S}) and drain (R_{D}) metalization and packaging resistances, R_{CH} is the sum of channel (R_{ch}) and channel accumulation (R_{ACC}) resistances, R_{EPI} is the sum of JFET (R_{JFET}) and drift region of epi (R_{dft}) and R_{SUBS} is the substrate resistance.

$$R_{\mathrm{ON}} = R_{\mathrm{w}} + R_{\mathrm{S}} + R_{\mathrm{D}} + R_{\mathrm{ch}} + R_{\mathrm{ACC}} + R_{\mathrm{JFET}} + R_{\mathrm{dft}} + R_{\mathrm{SUBS}} \tag{5.1}$$

R_{ON} is important for determining power loss and associated heating of the device. Low R_{ON} drastically reduces heat-sinking requirements and eliminates the need to parallel MOSFETs in practical applications, thus lowering parts count and assembly costs while improving reliability [118].

The existence of a MOSFET channel allows current to flow between drain and source in either direction depending on potential difference, implying that a conduction channel has no intrinsic polarity. In most power MOSFETs, the source and body junction are shorted through metalization to avoid unexpected device turn-ON due to the parasitic BJT that is created by the neighboring N^+, P-body and N^- epi regions. Hence, the p-n junction between the body and drain becomes parallel with the drain and source conduction channel. The internal body-diode activates if a voltage is applied in its forward-bias direction which, for in N-channel MOSFETs, is source to drain. Therefore, distinct voltage and current curves can be seen in the first and the third quadrants as illustrated in Fig. 5.4. The overall shape of the behavioural curves of N-channel power MOSFETs are all rather similar.

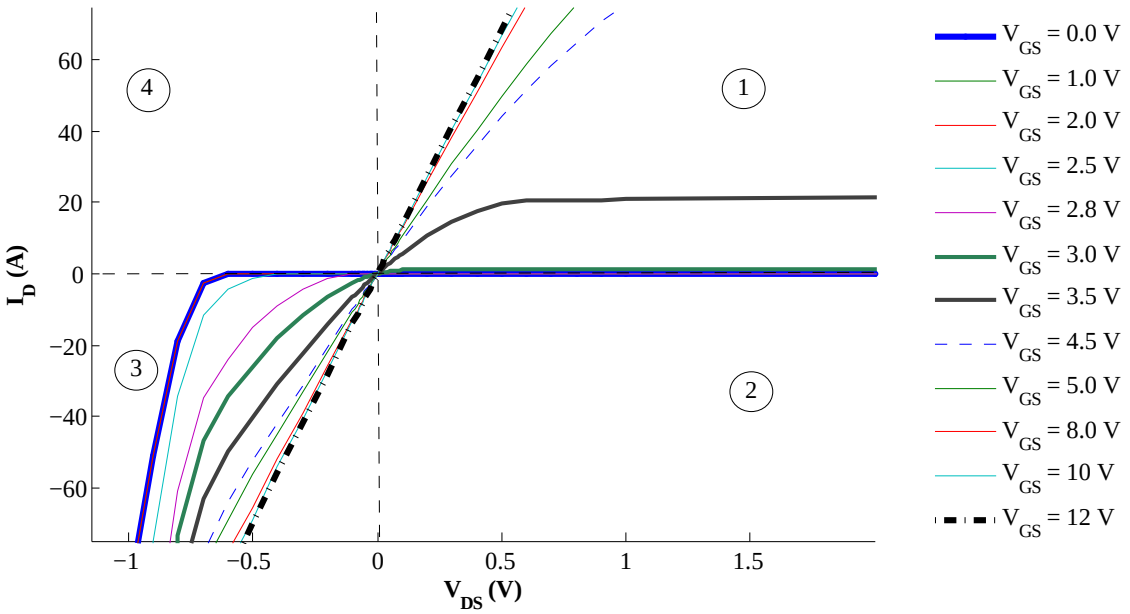


Figure 5.4: SPICE simulation results of the full VI-curve of AUIRL3705 N-channel MOSFET

There are various models used to define a power MOSFET are based on mathematical expressions or SPICE meta-structure [124–127]. Most common mathematical expressions of MOSFETs are simplified representations that do not carry enough details to enable accurate prediction of practical behaviour in high-current applications. In contrast SPICE models use meta-structure which defines a physical system with a collection of fundamental electrical elements (parameters) and their interrelations. A single device can be defined with many parameters that effect the accuracy of the simulation. Main reason of selecting SPICE as the base for analysis is the availability of well-defined and detailed

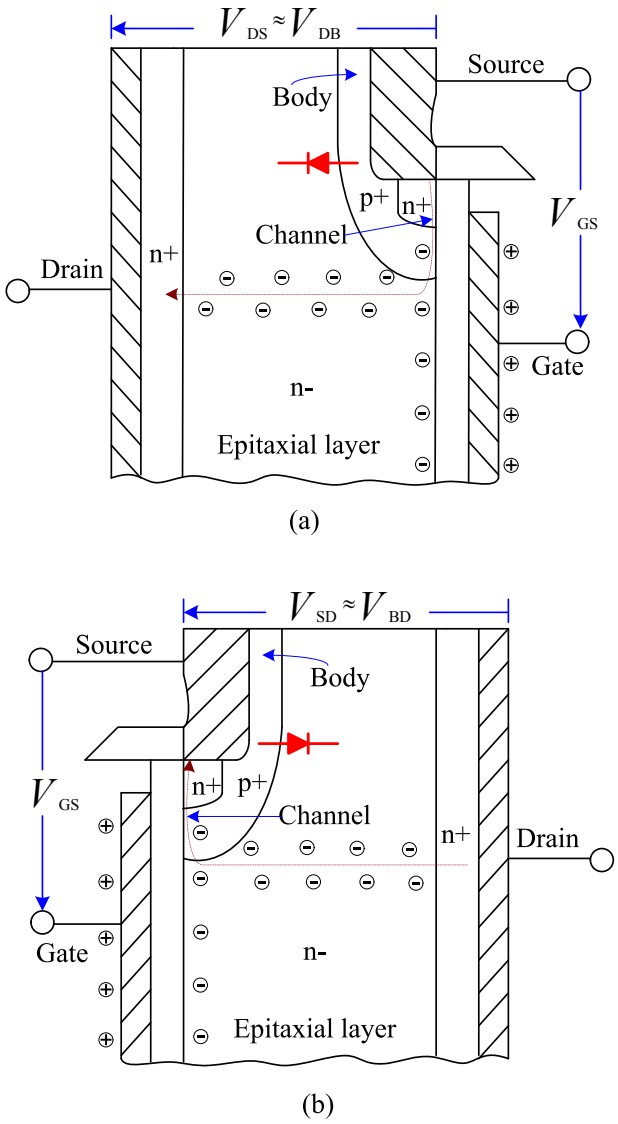


Figure 5.5: Simple illustration of a cross-section of an N-channel MOSFET: (a) drain voltage is higher than source and the electrons are moving from source to drain thus current flows to the opposite, (b) source voltage is higher than drain

meta-structure which also commonly accepted for high-current applications. The parameters in the SPICE model were used to develop MATLAB simulations of the body-diode.

The power-MOSFETs used in this project are AUIRL3705ZL by International Rectifier Corp. SPICE simulation results of AUIRL3705ZL for two quadrant operation are shown in Fig. 5.4.

Most electronic devices are designed to operate in the first-quadrant region in order to withstand high-voltage differences. But for some practical applications, third quadric operation is favoured to prevent current stress on the device. Typical LDO pass-elements are operated in the first-quadrant region, but in RS-SCALDO the third-quadrant operation was utilized in an LDO as discussed in Chapters 3; the reasons are presented as follows.

5.2.1 First-quadrant Operation

An N-channel MOSFET operates in the first quadrant when a positive voltage is applied to the drain. The drain-source channel starts to conduct current when the gate voltage V_{GS} increases above the threshold voltage V_{TH} (the minimum gate-source electrode bias required to form a conducting channel between source and drain regions). One of the commonly used expressions for the amount of current flow through the channel is given by Shichman and Hodges [128]. The current I_{DS} is

$$I_{\mathrm{DS}} = \begin{cases} 0 & \text{if } V_{\mathrm{GS}} < V_{\mathrm{TH}} \\ \mu_{\mathrm{n}} C_{\mathrm{ox}} \frac{W}{L} \left[(V_{\mathrm{GS}} - V_{\mathrm{TH}}) V_{\mathrm{DS}} - \frac{{V_{\mathrm{DS}}}^2}{2} \right] & \text{if } V_{\mathrm{DS}} < V_{\mathrm{GS}} - V_{\mathrm{TH}} \\ \frac{1}{2} \mu_{\mathrm{n}} C_{\mathrm{ox}} \frac{W}{L} (V_{\mathrm{GS}} - V_{\mathrm{TH}})^2 & \text{if } V_{\mathrm{DS}} > V_{\mathrm{GS}} - V_{\mathrm{TH}} \end{cases} \tag{5.2}$$

with length L, width W, gate oxide capacitance C_{ox} and N^+ carrier mobility μ_{n}. The W to L ratio defines the channel acceptance.

An empirical correction to these equations accounts for the channel length modulation via parameter λ

$$I_{\mathrm{DS}} = \begin{cases} 0 & \text{if } V_{\mathrm{GS}} < V_{\mathrm{TH}} \\ \mu_{\mathrm{n}} C_{\mathrm{ox}} \frac{W}{L} \left[(V_{\mathrm{GS}} - V_{\mathrm{TH}}) V_{\mathrm{DS}} - \frac{{V_{\mathrm{DS}}}^2}{2} \right] (1 + \lambda V_{\mathrm{DS}}) & \text{if } V_{\mathrm{DS}} < V_{\mathrm{GS}} - V_{\mathrm{TH}} \\ \frac{1}{2} \mu_{\mathrm{n}} C_{\mathrm{ox}} \frac{W}{L} (V_{\mathrm{GS}} - V_{\mathrm{TH}})^2 (1 + \lambda V_{\mathrm{DS}}) & \text{if } V_{\mathrm{DS}} > V_{\mathrm{GS}} - V_{\mathrm{TH}} \end{cases} \tag{5.3}$$

However, the following equations were used in SPICE for the static level 1 model [129]. For linear region,

$$I_{\mathrm{DS}} = KP \frac{W}{L - X_{\mathrm{ij}}} \left[(V_{\mathrm{GS}} - V_{\mathrm{TH}}) V_{\mathrm{DS}} - \frac{{V_{\mathrm{DS}}}^2}{2} \right] (1 + \lambda V_{\mathrm{DS}}) \tag{5.4}$$

For saturation region,

$$I_{\mathrm{DS}} = \frac{KP}{2} \frac{W}{L - X_{\mathrm{ij}}} (V_{\mathrm{GS}} - V_{\mathrm{TH}})^2 (1 + \lambda V_{\mathrm{DS}}) \tag{5.5}$$

where X_{ij} is the lateral diffusion parameter. Figure 5.6 shows a closer illustration of SPICE simulation results for the first quadrant with a magnified view of linear region.

The current-voltage curve appears linear when a sufficiently large voltage is applied to the gate to overdrive V_{TH}. The maximum amount of current I_{DS} is limited by the ON-resistance R_{ON}, as defined by

$$R_{\mathrm{ON}} = \frac{V_{\mathrm{DS}}}{I_{\mathrm{DS}}} \tag{5.6}$$

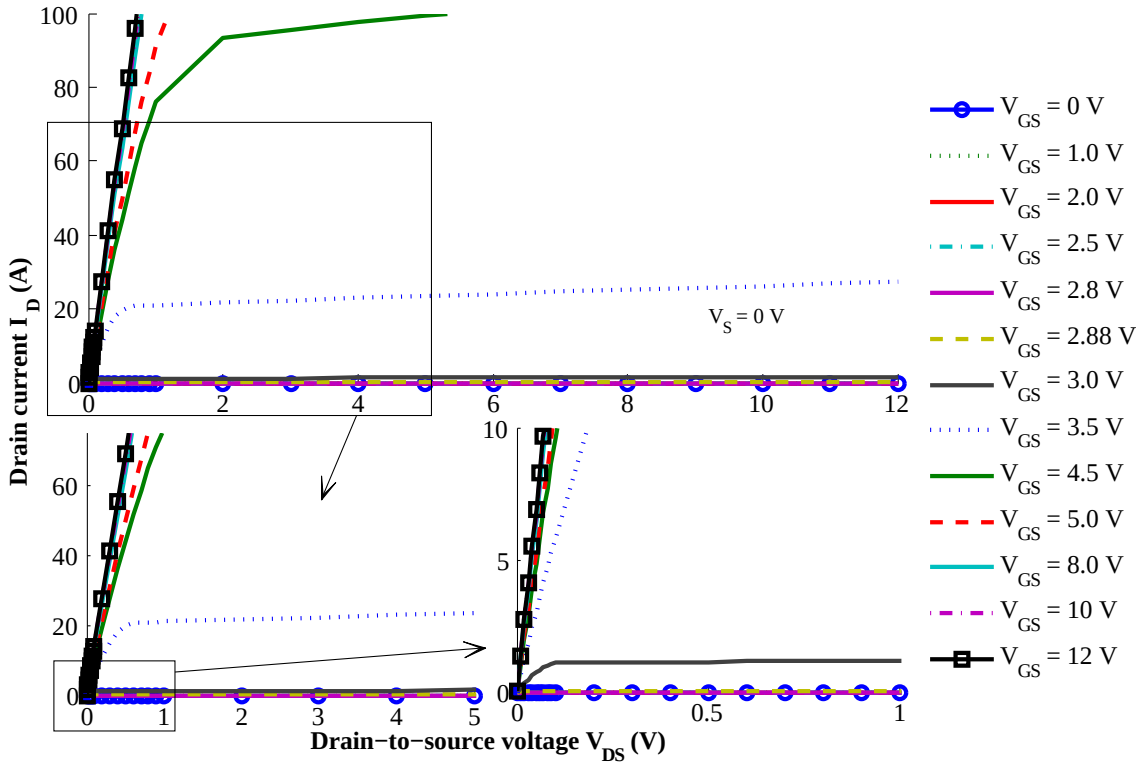


Figure 5.6: SPICE simulation results of the 1st quadrant V-I curve of AUIRL3705ZL N-channel MOSFET

In low gate voltages, the drain current reaches a saturation point when the drain-to-source voltage V_{DS} is greater than the overdrive voltage ($V_{\mathrm{GS}} - V_{\mathrm{TH}}$) due to a pinch-off effect of the channel.

The channel resistance R_{CH} is highly dependent on the amount of the gate overdrive. With increasing V_{GS}, R_{CH} decreases. R_{ON} initially decreases rapidly as V_{GS} increases above V_{TH}, indicating the turning-on of the MOSFET channel. As V_{GS} increases further, R_{ON} saturates because the channel is fully turned on and the MOSFET resistance is limited by the other resistive components. However, R_{ON} increases with temperature due to the decreasing carrier mobility. This is an important characteristic for device paralleling.

5.2.2 Third-quadrant operation

When a negative voltage is applied to V_{DS} or the value of V_{SD} increases, forward biasing of the body-diode will occur. Current can flow in to the reverse direction compared to the first-quadrant operation. A sufficiently overdriven gate voltage can form a channel from source to drain parallel with body-diode. Current ratio of body to channel are inversely proportional to their resistances. The channel is dominant for an overdriven gate voltage until V_{SD} rises sufficiently to allow current to flow through the body-diode. When increasing V_{SD} the current increases but no channel saturation behavior is observed in third quadrant. This can be seen in Fig. 5.7.

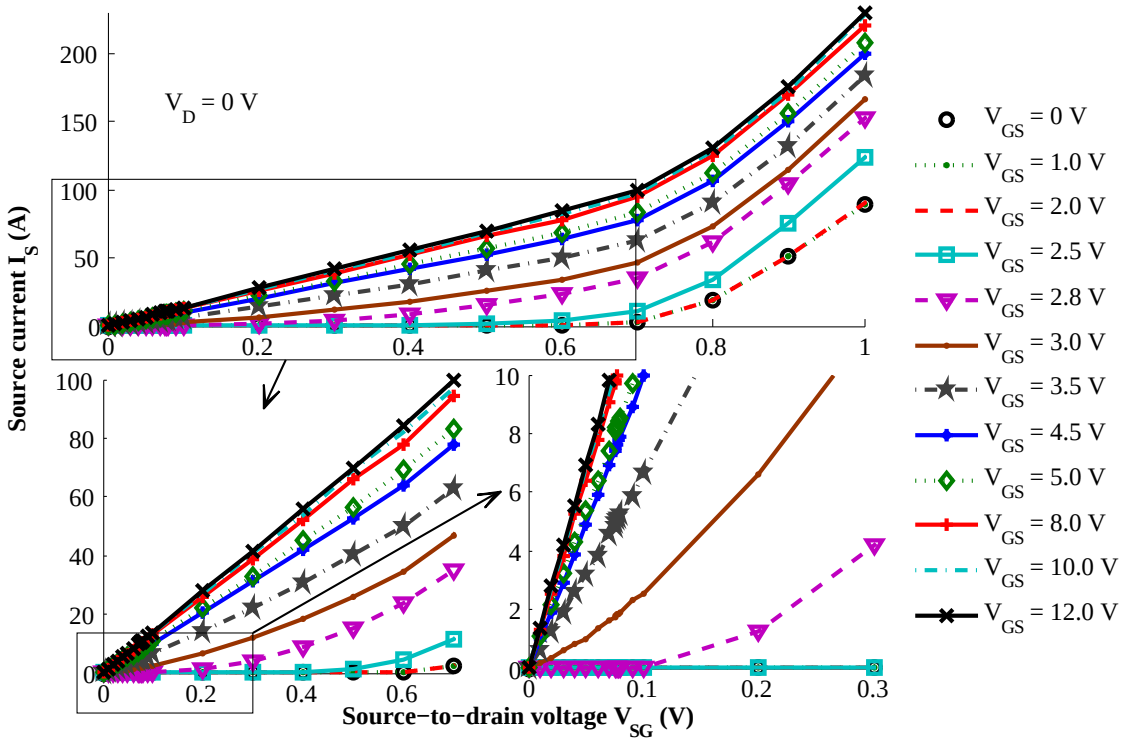


Figure 5.7: SPICE simulation of third quadrant operation of AUIRL3705ZL

This behaviour is heavily influenced by the body-diode. In low voltage (<100 V) devices with low ON-resistance, the body-diode forward voltage drops are typically 0.4-0.5 V and a maximum of 1.6 V can be found in high voltage (>100 V) devices with high ON-resistance [117].

The large-signal behaviour of a standard SPICE diode is characterized by the DC current and voltage relationship at its terminals; Fig. 5.8 illustrates the equivalent circuit. The parameters used in the model represent the physical structure related components. The reverse saturation current I_{SAT} is considered to be the same as for the ideal diode. The resistance of the metal contacts and the neutral region are represented by ohmic resistance R_{S}.

From Fig. 5.8, the voltage across the external terminals of the diode V_{F} is,

$$V_{\mathrm{F}} = R_{\mathrm{S}} I_{\mathrm{d}} + V_{\mathrm{d}} \tag{5.7}$$

where the forward bias current of a diode I_{d} is a function of diode voltage V_{d}.

From the four regions of the diode operation described in [130], for this project where $V_{\mathrm{d}} \geqslant -5NV_{\mathrm{t}}$ region is applicable as it represents the forward-bias operation, where emission coefficient and V_{t} is thermal voltage. Hence the relationship of I_{d} and V_{d} is given by

$$I_{\mathrm{d}} = I_{\mathrm{SAT}} \left[\exp\left(\frac{V_{\mathrm{d}}}{NV_{\mathrm{t}}} \right) - 1 \right] - G_{\mathrm{min}} V_{\mathrm{d}} \tag{5.8}$$

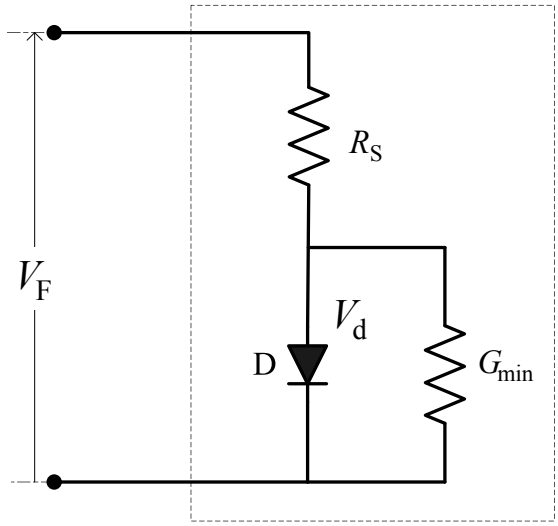


Figure 5.8: DC large signal SPICE model of a diode [4]

where the shunt conductance $G_{\min}$ and the reverse saturation current I_{SAT} are taken to be constant in SPICE, and N is emission coefficient that modifies the slope of the V-I curve.

The thermal voltage V_{t} is defined by

$$V_{\mathrm{t}} = \frac{kT}{q}$$

where k is Boltzmann constant, T the absolute temperature and q the magnitude of charge of an electron. Applying the diode equation to body-drain or the source-drain diode of the MOSFET gives the body-drain current,

$$I_{\mathrm{BD}} = I_{\mathrm{SAT}} \left[\exp\left(\frac{V_{\mathrm{SD}}}{N V_{\mathrm{t}}} \right) - 1 \right] - G_{\min} V_{\mathrm{SD}} \tag{5.9}$$

assumes that there is no potential difference between source and body.

The SPICE model of the body-diode (source-drain or body-drain) in the AUIRL3705ZL consists of parameters defining the large signal DC model. These were used to develop the large signal DC-model of the diode behaviour in MATLAB. See Appendix B.

To check how well the SPICE and MATLAB models predict real diode behaviour, comparisons are made with bench data from real MOSFETs. Five randomly chosen AUIRL3705ZL MOSFETs were tested in the setup illustrated in Fig. 5.9. To obtain the current through the body diode, the voltage across the load R_{L} (V_{RL}) was measured and divided by R_{L}. The resistive load R_{L} is a 1$\pm$0.2 Ω, 10 W resistor. Simultaneously, the terminal voltage of the device (V_{SD}) was recorded at an average temperature of 23.5°C measured by the TMP in Fig. 5.10 (a Fluke-179 multimeter with 0.1°C maximum resolution and accuracy $\pm 1\% + 10$ for the range -40°C /400°C). Voltages V_{SD} and V_{RL} were

measured using Keysight Technologies U3402A multimeter (with a 6 mV smallest voltage measurement, up to 0.012% basic DC voltage accuracy).

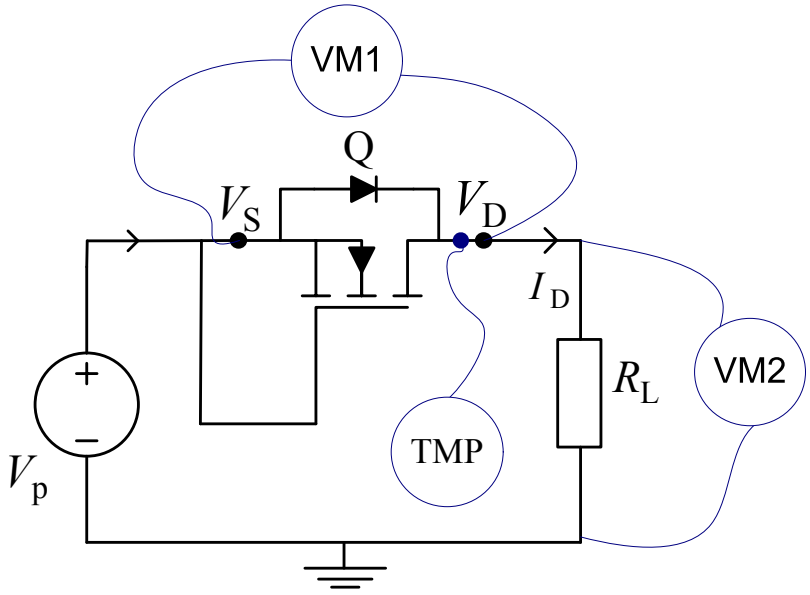


Figure 5.9: Schematic diagram of testing the body-diode of a discrete MOSFET

The behaviour of V-I curves of for predicted and measured data are shown in Fig 5.10. MATLAB simulation is based on Russell's diode SPICE model [130]. The discrete SPICE model of the diode was developed from the meta-data for the AUIRL3705ZL MOSFET. The SPICE MOSFET body-diode model was built by simulating the experimental circuit. The MATLAB and SPICE simulations are identical, but offset to the left of the measured curves for currents higher than 100 mA, with a 0.024 V shift.

The discrepancy was corrected by tuning the theoretical parameter values $N = 0.931$ (previously 1.20602), and $I_{\mathrm{SAT}} = 4.8{\times}10^{-13}$ A (was $5.37063{\times}10^{-10}$ A). One of the possible reasons for I_{SAT} to be lower is the influence of other layers in the MOSFET. Figure 5.11 shows the modified theoretical curves that are generated to match with the practical curve.

The dynamic resistances of the diode and the channel are R_{d} and R_{chn} respectively. They can be obtained by differentiating Eq. (5.9) and Eq. (5.3) (with respect to voltage) and computing the reciprocal. They are

$$R_{\mathrm{d}} = \frac{NV_{\mathrm{t}}}{I_{\mathrm{SAT}}\left[\exp\left(\frac{V_{\mathrm{SD}}}{NV_{\mathrm{t}}}\right) - G_{\mathrm{min}}\right]} \tag{5.10}$$

and

$$R_{\mathrm{chn}} = \frac{2L}{\mu_{\mathrm{n}} C_{\mathrm{ox}}\left[2(V_{\mathrm{GS}} - V_{\mathrm{TH}})(1 + 2\lambda V_{\mathrm{SD}}) - V_{\mathrm{SD}}(2 - 3\lambda V_{\mathrm{SD}})\right]} \tag{5.11}$$

Therefore the total resistance R_{SD} is given by

$$\frac{1}{R_{\mathrm{SD}}} = \frac{1}{R_{\mathrm{d}}} + \frac{1}{R_{\mathrm{chn}}}$$

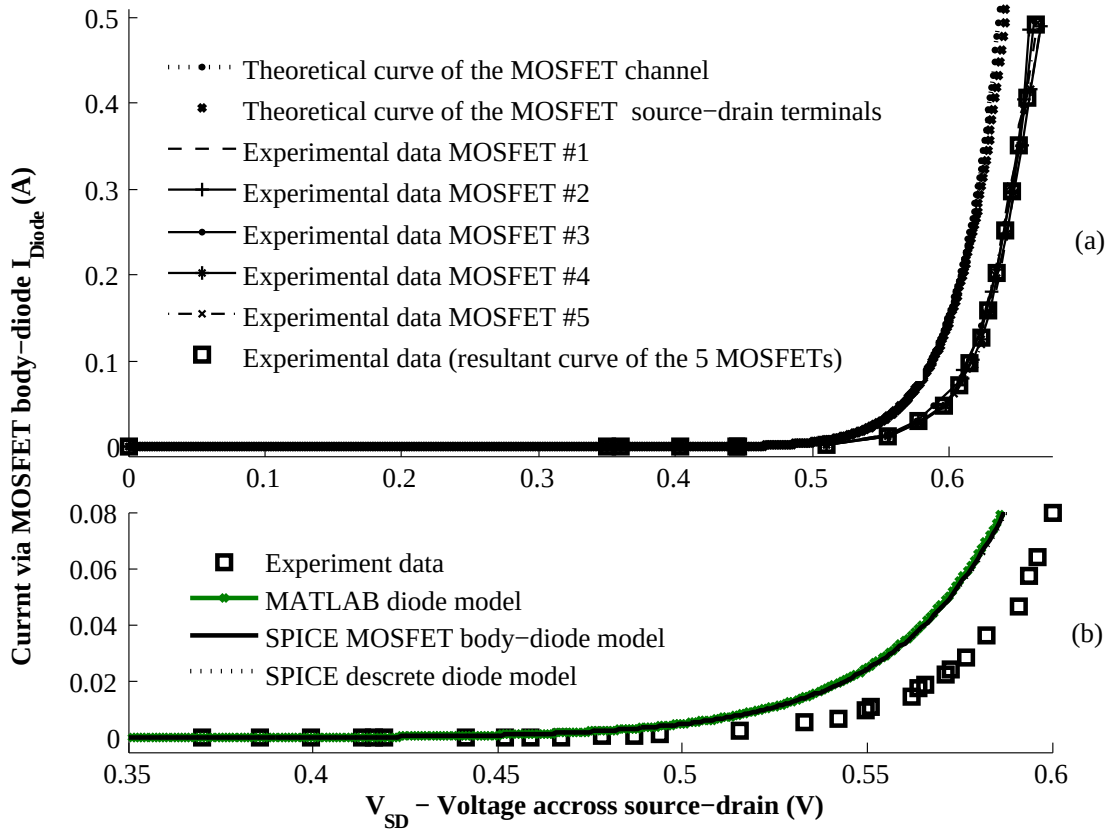


Figure 5.10: AUIRL3705ZL N-channel MOSFET body-diode equivalent characteristic curve : Theoretical and experimental data

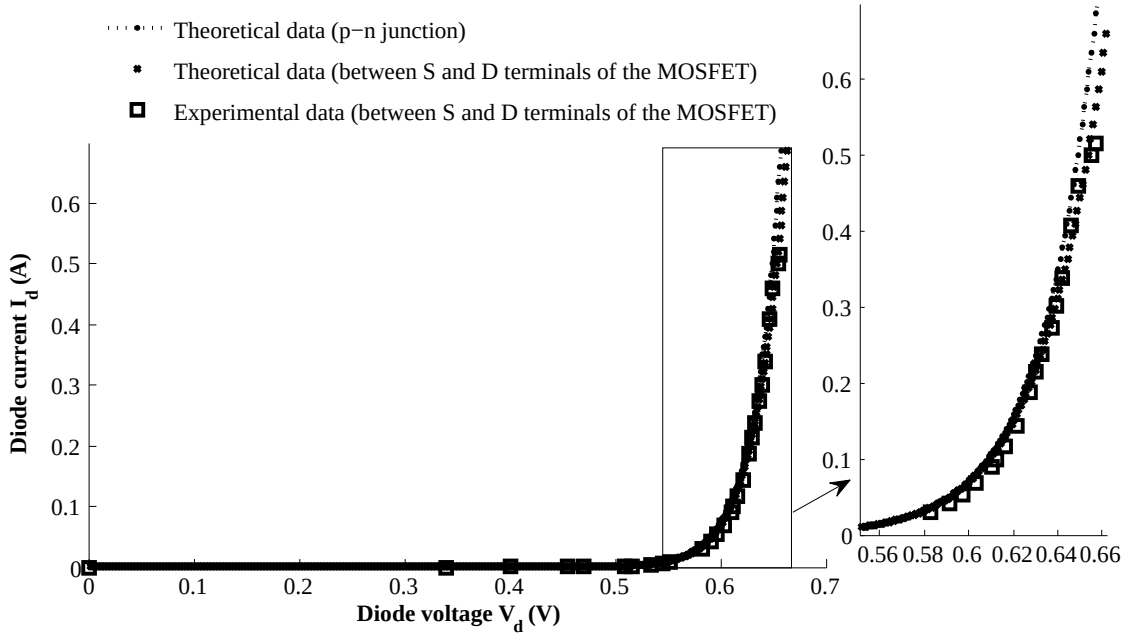


Figure 5.11: Modified MOSFET body-diode

$$R_{\mathrm{SD}} = \frac{R_{\mathrm{d}} R_{\mathrm{chn}}}{R_{\mathrm{d}} + R_{\mathrm{chn}}} \tag{5.12}$$

A theoretical comparison of the two resistances R_{d} and R_{chn} are illustrated in Fig. 5.12.

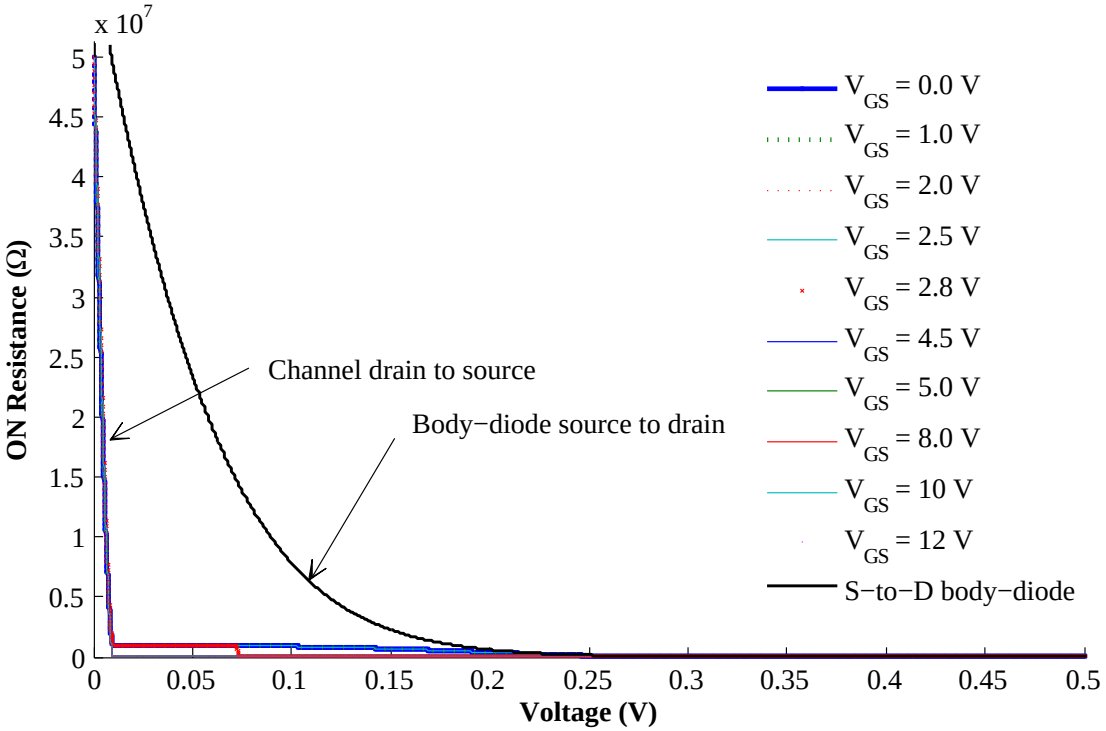


Figure 5.12: A theoretical comparison of channel resistance R_{chn} and body-diode resistance R_{d}

For lower V_{SD} and higher V_{GS}, R_{chn} is lower than R_{d} and more current flow through the channel whereas when V_{SD} increases the body-diode will dominate. This behaviour is reflected in the third-quadrant operation of N-channel MOSFET illustrated in Fig. 5.7.

Third quadrant operation is commonly utilized in DC-DC buck converters [131, 132], where current conduction occurs under V_{SD}. For low-side FETs in synchronized buck converters, a low V_{SD} can help to reduce power loss [133] during body-diode conduction.

5.3 LDO in third-quadrant operation

In RS-SCALDO, the LDO that activated in the charging phase (LDO1) uses the third-quadrant operation though it is not the usual practice in a linear regulator design. This LDO1 eliminates the need of additional components for blocking the unwanted SC discharge path that created by MOSFET switches. Further, it regulates well within the requirement specifications of the 3.5-to-1.5 V RS-SCALDO and maintains a higher efficiency greater than 80%.

The equivalent circuit for the LDO1 is shown in the Fig. 5.13. Except the orientation of the series pass-element, the rest of the circuit is a typical LDO design. The pass-element is driven by an error signal of an operational amplifier (op-amp) in a negative feedback control loop.

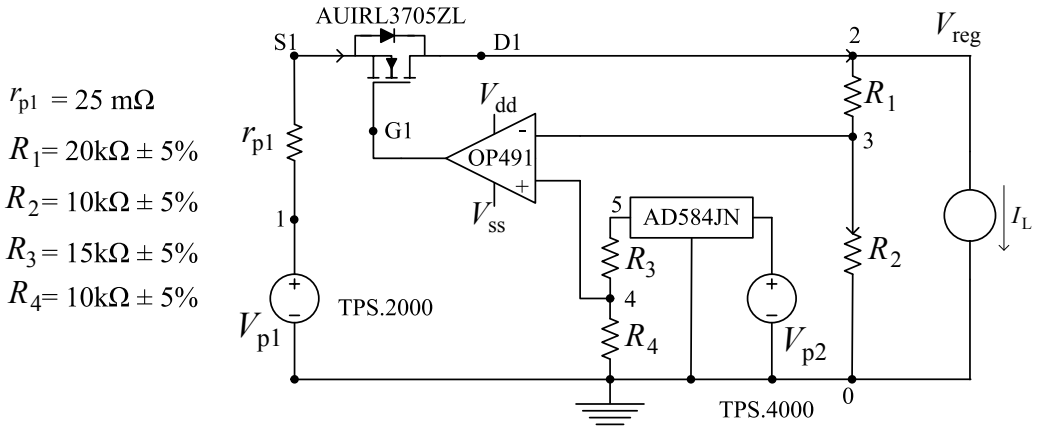


Figure 5.13: Equivalent circuit of AUIRL3705ZL N-channel MOSFET LDO1

When current i_d passes through the body-diode from a total current I_S, the residual current $I_S - i_d$ will flow through the channel. Assuming the body-diode and channel are parallel and terminal voltages are equal

$$R_{chn} = \left(\frac{i_d}{I_S - i_d}\right) R_d$$

R_{chn} is a function of V_{SD} that changes with V_{GS} accordingly thus relies on R_d. The body-diode is fully activated for a sufficiently large V_{SD} thus $R_d \ll R_{chn}$ and negligible current will flow through the channel, thereby the gate voltage reduces and reaches zero. Therefore, the pass-element act as a constant resistor with a value R_d where that has no control on V_{GS}.

This can be seen in the LDO1 line regulation curves of Fig. 4.10. For the regulation of LDO1, the linear region operation of pass-element only valid until V_{SD} reaches V_d. A no-load curve will determine the upper limit of the regulation while full load defines the lower limit.

For $V_{SD} \leqslant V_d$

$$\text{line regulation} = \frac{\Delta V_o}{\Delta V_{in}} = \frac{\Delta V_{reg}}{\Delta V_p} \approx \frac{1}{A_v \beta}$$

The load regulation is,

$$\text{load regulation} = \frac{\Delta V_o}{\Delta I_L} = \frac{\Delta V_{reg}}{\Delta I_L} \approx \frac{1}{g_m A_v \beta (r_o + R_L)}$$

where ΔV_p and ΔI_L are small change in the input voltage and load current respectively; g_m is the transconductance gain of the FET, A_v is the gain of the amplifier, β is the voltage divider gain, r_o is the output impedance of the FET pass-element and R_L is the load resistance [134].

$$\beta = \frac{R_2}{R_1 + R_2}$$

For a constant current, V_{SD} increasing proportional to LDO input voltage V_p,

$$V_{reg} = V_p - V_{SD}$$

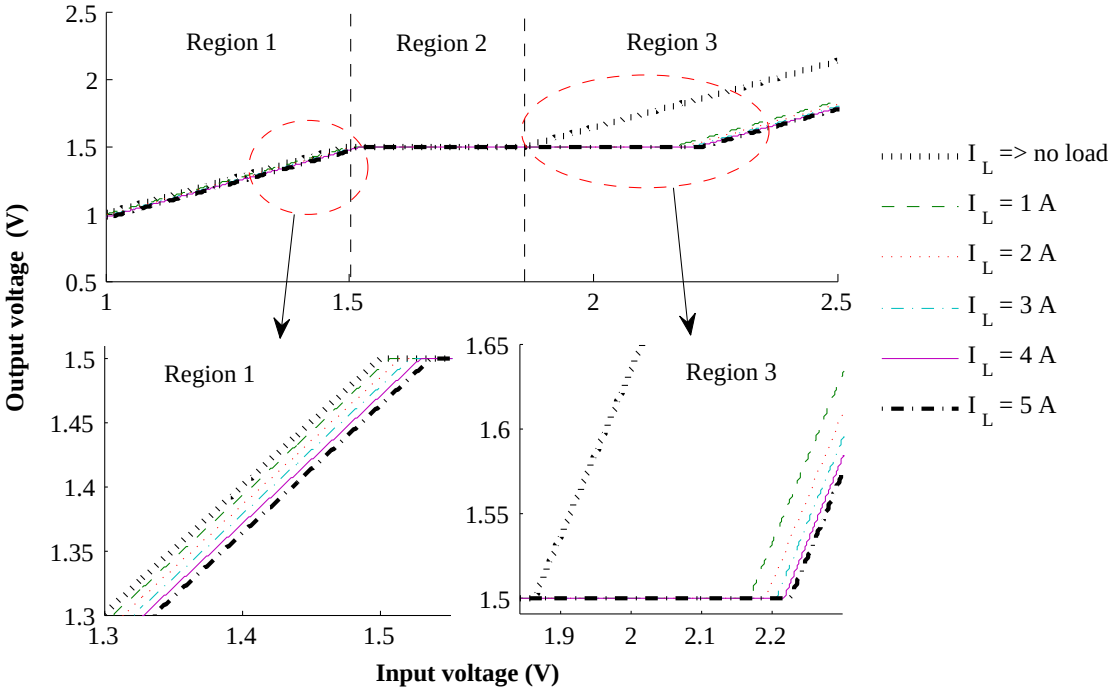


Figure 5.14: Simulation results of LDO1 line regulation: Region 1:$V_{\mathrm{p}} < V_{\mathrm{reg}} + V_{\mathrm{do}}$ where there is no sufficient dropout voltage for output regulation, Region 2:$V_{\mathrm{p}} \geq V_{\mathrm{reg}} + V_{\mathrm{do}}$ and $V_{\mathrm{d}} > V_{\mathrm{do}}$, where there is sufficient dropout voltage for output regulation and the dropout voltage is less than the diode forward conduction voltage, and Region 3:$V_{\mathrm{p}} > V_{\mathrm{reg}} + V_{\mathrm{do}}$ and $V_{\mathrm{d}} < V_{\mathrm{do}}$ where dropout voltage exceeds the diode forward conduction voltage

For larger loads, the regulation curve can be extended to a wider input range. The behaviour of LDO1 reflects on the RS-SCALDO as shown in Fig 5.15. These simulations are in agreement with the experiment results that were discussed in the previous chapter.

SPICE simulation circuits of RS-SCALDO related documents can be found in the Appendix C.2.

5.4 RS-SCALDO circuit simulation and analysis

The primary experimental work in the research is carried out to prove the SCALDO can be viable for low-voltage, high-current and high-efficiency applications, especially for VRMs. Accordingly, a new SCALDO topology has been designed, and a prototype was built adapting the basic SCALDO design. Circuit components in the previously built SCALDO were replaced appropriately to develop the high-current prototype. As discussed earlier, I replaced the two power switches and LDOs with discrete MOSFETs, and upgraded the control circuits by utilizing a common feedback circuit for the two LDOs.

Two switches in RS-SCALDO was driven by simple MOSFET-based circuits as shown in Fig. 5.16. Digital signals alternatively enable the gate-drive circuit and thereby the

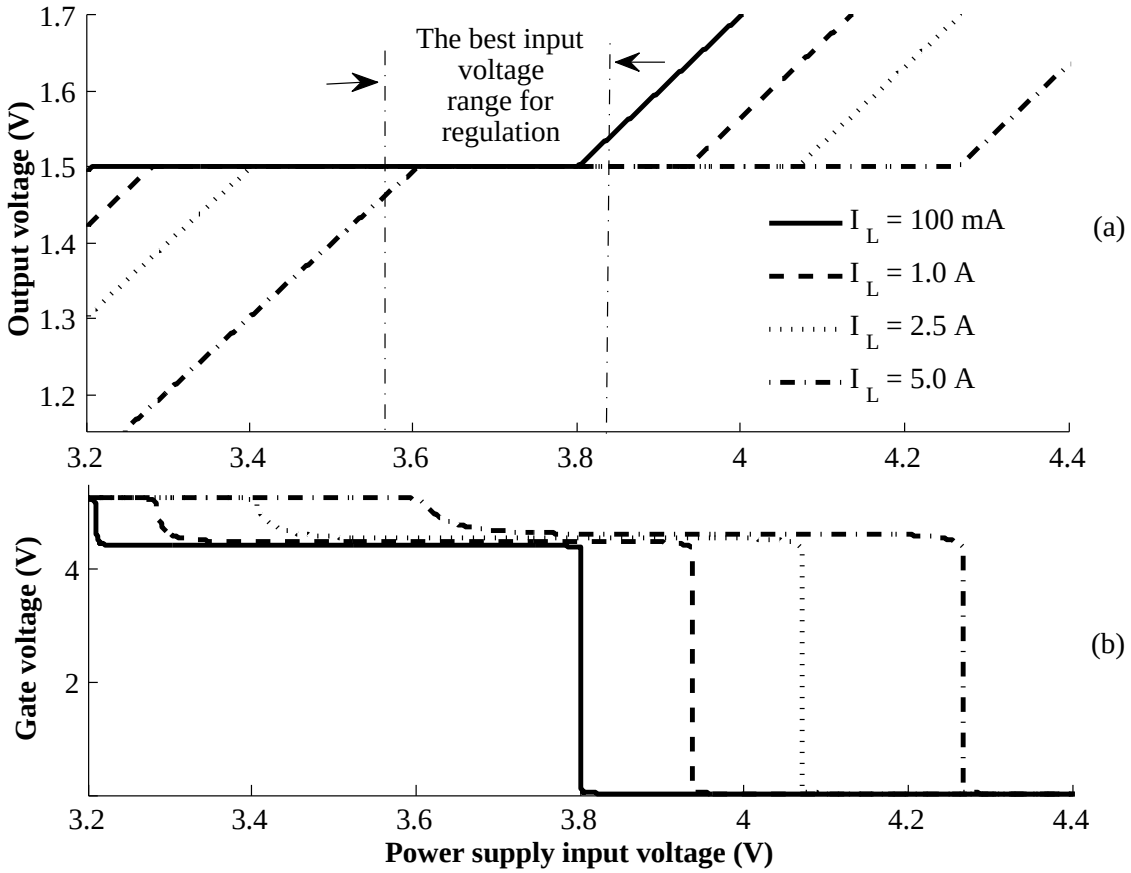


Figure 5.15: SPICE simulation of (a) the line regulation of the RS-SCALDO and (b) the gate voltage of LDO1

two switches. The gates of two switches are driven into the maximum available voltage, hence reduce the ON-resistance. Resistor R_1 controls the output voltage level (signal to switch) and the current flow through the MOSFET Q. R_2 used to stabilize and prevent floating the control signal.

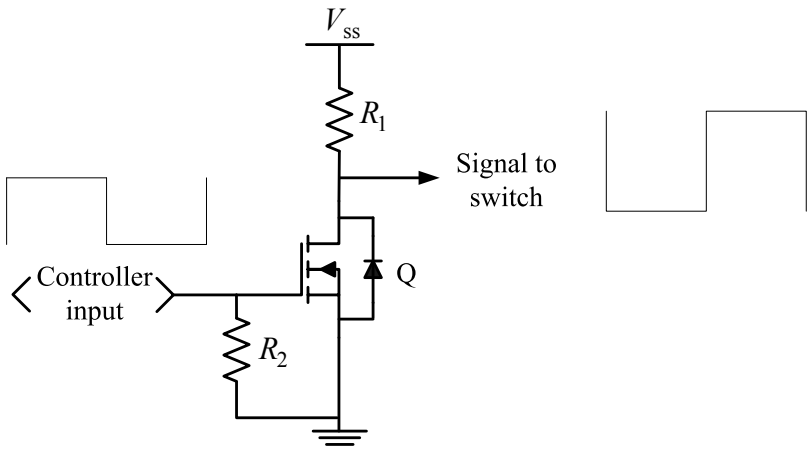


Figure 5.16: Equivalent circuit of the gate driver of a switch

Simulated behaviour of the two gates is shown in Fig. 5.17; panels (a) and (b) illustrate the source-drain differential voltage versus drain voltage of switches SW1 and SW2

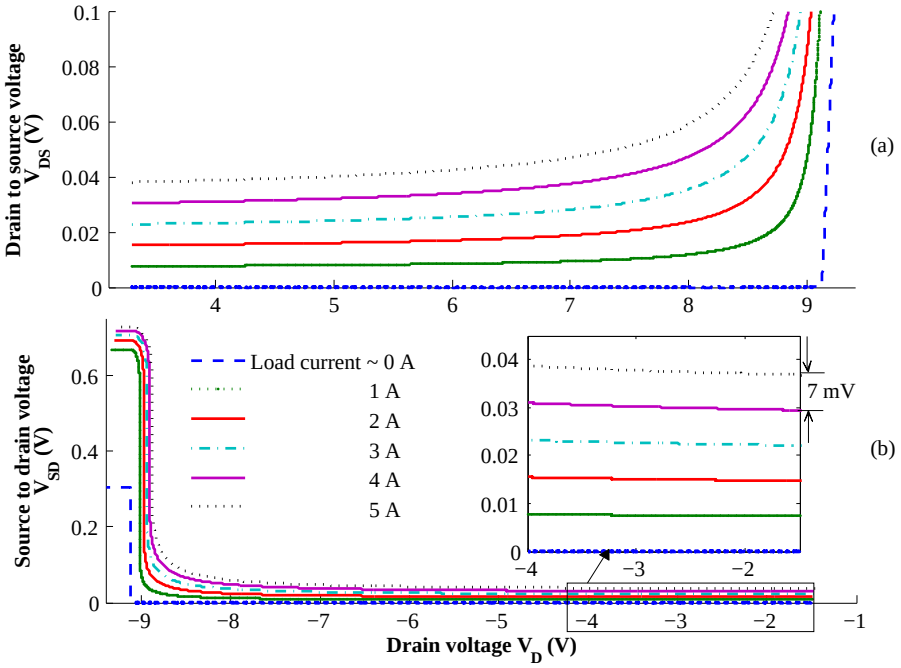


Figure 5.17: Simulation of the behaviour of switches: (a) SW1 which connects the unregulated power supply with SC at the charging phase, (b) SW2 connects the SC to ground at the discharging phase

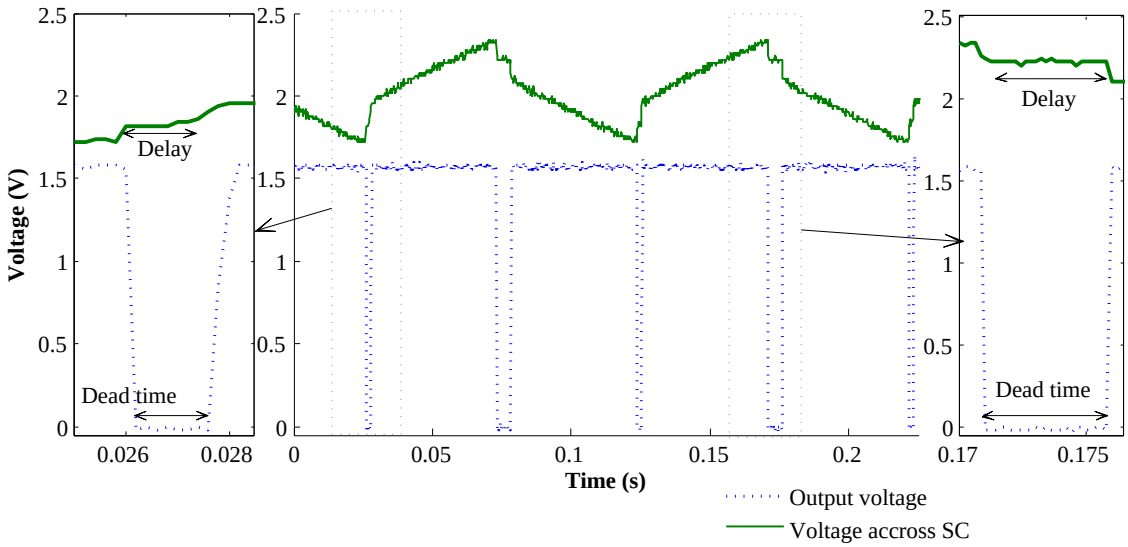


Figure 5.18: Delays in the digital signal creates dips in the output of the RS-SCALDO

respectively. The drain of the MOSFET in SW1 is connected to the unregulated input power supply and the source is to the positive terminal of the SC and input of the LDO2. In RS-SCALDO, this drain only change between 3.3 V and 4 V while the gate dive to maximum of 12 V. SW2 is the switch that activates in SC discharging phase, where its source is shorted to ground while the drain is connected to negative terminal of the SC and input of the LDO1 while the drain varying close to the ground. When SW2 is in the active stage, the current flow from source to drain. Approximately about 7 mΩ resistance can be found in both the switches, which is a 93 % less compared to a switch with

100 mΩ in the original SCALDO; similar percentage of the switch ON-resistance losses were reduced.

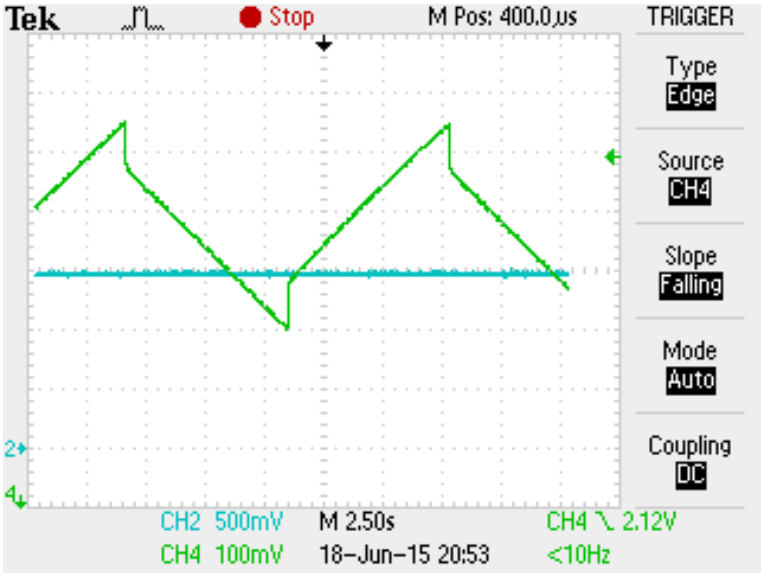


Figure 5.19: RS-SCALDO actual results: CH2(blue) trace is the regulated output voltage, CH4(green)trace is the differential voltage of the SC

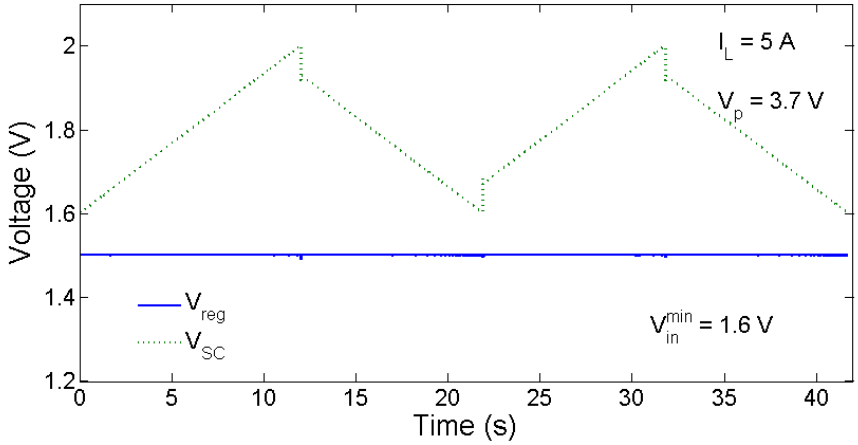


Figure 5.20: RS-SCALDO simulation results: The blue trace is the regulated output voltage, and the green trace is the differential voltage of the SC

Theoretically, this drain-source voltage V_{DS} can be calculated with an approximation. If the channel does not pinch-off at drain-end, and gate-to-source voltage V_{GS} and I_{D} known, V_{DS} is,

$$V_{\mathrm{DS}} = (V_{\mathrm{GS}} - V_{\mathrm{TH}}) - \sqrt{(V_{\mathrm{GS}} - V_{\mathrm{TH}})^2 - \frac{2I_{\mathrm{D}}}{K}} \tag{5.13}$$

where K is device transconductance parameter. (Assumption: channel length modulation is negligible.)

In the practical operation, when a single control signal or simultaneously operated signals is being used in to control the gates and LDOs, the ON/OFF delays create a

voltage dip in the output as seen in Fig. 5.18. Here, a 2 A load was applied and BCAP150 capacitor was used. This issue was not serious in original SCALDO circuits as they use for low-current applications and the input capacitor was sufficient to handle the delays. Further, a possible unavailability of LDO stage was never in SCALDO circuit. This issue was addressed by moderating the delays and the properly committed digital signals.

Figure. 5.19 shows the waveform after reduction of these control signal delays in the prototype. The dead-time issue can be controlled digitally without utilizing capacitors at the input side of LDO. The program is available in Appendix B. A 4900μF buffer capacitor has to be utilized at the output of the RS-SCALDO during transients with 5 A load. Both the simulation in Fig. 5.20 and the validation in Fig. 5.19 show very similar results. With the possibility of the body-diode issue eliminated, the technique can be extended to achieve much higher currents.

Chapter 6

Conclusions and Recommendations

6.1 Summary

Linear regulator techniques had never been considered as possible solutions for voltage regulator modules (VRM) until University of Waikato researchers found a novel DC-DC converter technique to combine a supercapacitor lossless voltage-dropper with a low dropout (LDO) regulator as described in Chapters 1 and 2. This innovative technique opened up many potential applications from which linear regulators had been excluded previously, particularly where the requirement is for high efficiency at high load currents with the output voltage much lower than the supply.

The aim of my research was to improve the supercapacitor-based linear converter known as SCALDO for VRMs. It was motivated by the demand for low cost, low noise, reduced complexity, fast transient response and high-efficiency VRM. These goals are difficult to achieve using standard high-frequency switched-mode power supply techniques. SCALDO regulators can meet these goals if the number of switch elements is reduced.

This thesis has presented a novel topology to realize a less complex SCALDO by minimizing the number of switches. The new topology is more cost effective and efficient, particularly for high-current applications. As described in Chapters 3, 4 and 5, a detailed analytical study of the design was carried out using practical experiments and simulations in SPICE and MATLAB.

6.2 Conclusions

The reduced-switch SCALDO (RS-SCALDO) is a better match for VRM requirements than the original SCALDO. The reduction in switch count reduces cost and energy losses. The 3.5-to-1.5 V RS-SCALDO proof-of-concept prototype achieved 76 to 85% end-to-end efficiency for 2 to 100% of a 5 A maximum load. Relative to the performance of a standard linear regulator, this represents an efficiency improvement close to a factor of two. Unlike switched-mode power supplies, the charge-discharge cycling frequency for SCALDO can be lowered to a few millihertz with appropriate choice of supercapacitor values. For constant load current I_{L}, the cycling frequency is $f_{\mathrm{op}} = I_{\mathrm{L}}/2C\Delta V_{\mathrm{C}}$. At these modest switching rates, RFI/EMI is no longer an issue. The new topology addresses three issues

in the original SCALDO design.

(a) Complexity and cost

The original SCALDO circuits are complicated by the need for a large number of switches. Typically implemented with expensive solid-state relays can be replaced with power MOSFETs which have 40 times more current capability and 15 times smaller ON-resistance with approximately 8 times less cost per component.

The switch reduction strategy introduced in this thesis reduces the number of switches in a general SCALDO from $3n+1$ to $2n$ for a general SCALDO design with n supercapacitors. Consequently, half of the switches can be eliminated from a single supercapacitor 3.5-to-1.5 V SCALDO design; this was achieved by implementing an application specific LDO. There is a limitation of the discrete MOSFET-based implementation: in the RS-SCALDO proof-of-concept prototype, power losses were minimized at the cost of a reduction in the allowable variation of input voltage. However, this is not an issue for this project considering the input power supply of the VRM (computer power supply unit) is a pre-regulator that varies within these limits.

In RS-SCALDO, two LDOs are required to work alternately in supercapacitor charge and discharge phases. However, it is possible to utilize a common control circuit to drive their series pass-elements; this also reduces the cost of components.

(b) Body-diode effects

Power MOSFET switches are the most common and inexpensive devices used in power applications. For high-current application, discrete or module scale devices are feasible. However, practical implementation of SCALDO is not possible without isolated MOSFET switches in order to avoid an unwanted body-diode discharge path. An analytical study identified the limitations in the SCALDO circuits, including the source of the parasitic body-diode path that shorts the charged supercapacitor to ground. These problematic switches for 12-to-5 V, 5-to-3.3 V and 5-to-1.5 V SCALDO configurations are identified in Chapter 3.

The body-diode issue was addressed by eliminating the problematic switches and adding an application specific LDO. This new high-efficiency LDO can be implemented by changing the polarity of the series pass-element (source-drain) at the cost of a reduction in allowed voltage variation of its input. This application specific remedy (modified LDO) has better regulation within the limits of expected input variation, thus it works for the VRM presented here. With this new approach it is possible to implement the remaining RS-SCALDO switches using inexpensive discrete MOSFETs. The modified LDO reverse-biases its body-diode and blocks short-circuit current path of the supercapacitor to ground.

(c) Voltage identification capability

In order to reduce power consumption, modern microprocessors are required to change their core voltage according to operational conditions. Therefore the VRM has to adjust its output voltage continuously to satisfy this requirement. This is done using a digital signal (voltage identification code) that is sent from the processor to the VRM to adjust its output. This digitally controlled output capability was implemented in RS-SCALDO using a digital potentiometer in the common sampling circuit of the two LDOs. Compared to the rather sophisticated techniques utilized in present buck converters this method is cost effective and has a straightforward design.

6.3 Recommendations

(a) Monolithic integrated circuit for RS-SCALDO

One of the long-term goals in SCALDO research is an integrated on-board compact design. The control stage of the RS-SCALDO can easily be fabricated in a monolithic integrated circuit. The high-current power stage that consists of LDO pass-elements and switches has to be separated from the control stage, either by design with discrete components or a circuit module. Coherent details presented in this thesis are useful in this regard. With the availability of microscopic supercapacitors a very compact circuit can be built.

Further, an integrated circuit (IC) design can remove the limitations in the application-specific LDO. An IC process can couple MOSFETs with fewer resistive connections than discrete components connected externally, enabling reduction of ON-resistance losses in the series pass-element. Prospective solutions which are suitable for IC based design of pass-elements are proposed in Chapter 4. They can eliminate restrictions that apply to the use of wider input voltage ranges. These solutions can also be used in other applications, such as battery-reversal protection in batteries chargers.

Basic VID capability was implemented in RS-SCALDO as proof of concept. Simple linear operation of LDO can provide opportunity to improve digital controllability, but a thorough analysis is necessary to improve transient response of high-current LDOs.

(b) Input source of the VRM

Linear series regulators operate as voltage dividers which constantly change the resistance of the series-pass element to regulate the output voltage. Assuming that there is a negligible quiescent current in the circuit, the amount of current demanded by the load is matched by the input supply current. Inherently, linear regulator techniques cannot increase output voltage or current to exceed that at the input. Therefore, the maximum current a load can demand is limited by the input source.

The operation of SCALDO is based on an LDO, therefore it must comply with the above voltage and current constraints. As discussed in Chapter 2, LDO has two phases

defined by the charging and the discharging of supercapacitors. In the charging phase the power source is the unregulated DC power supply which, for VRM applications, will be the computer power supply (silver-box). And in the discharging phase the power is supplied by the supercapacitors. Delivering large load currents exceeding 100 A is possible for supercapacitors as they are available with large capacities and very low ESR. However, such a large current demand by the processor at the charging phase will be an issue since a standard silver-box typically delivers less than 50 A from a single rail. There are computer power supplies which can deliver more than 100 A from a 12 V rail, but these are specially built for high-end gaming computers, so are costly to use for general VRM applications. As a general rule, it is recommended to use SCALDO for loads requiring currents less than the maximum available from the input power supply.

This issue can be addressed by properly designed RS-SCALDO as the pre-regulator of VRMs. One possible option is to improve the UPS-capable SCALDO discussed in Chapter 2; here a supercapacitor or both the supercapacitor and the power supply can energize the processor for high-current demand.

6.4 Future work

More complex configurations of RS-SCALDO (5-to-1.5 V or a 12-to-1.5 V and 5-to-3.3 V) can be built to prove the concept and generalized theory with practical experiments. Such configurations will require LDO designs with parallel MOSFETs. Feasibility of these LDOs can be tested along with the configurations.

With growing demands for supercapacitor-based portable applications, microscopic supercapacitors will be available soon in the market. For high-current applications, paralleling them will increase capacity while reducing the ESR, which is advantageous when designing RS-SCALDO in an IC version.

From a design point of view, future work should be carried out in three aspects:
(1) designing single input LDO with an efficient charge pump to drive the error amplifier;
(2) improving the transient response by reducing the sags and swells in output voltage to be smaller than ± 50 mV;
(3) designing energy efficient supercapacitor-based AC-DC power supplies with high-current capability (in a single rail) to replace conventional silver-box computer power supplies.

Appendix A

General theory of RS-SCALDO

As mentioned in Chapter 3, the general SCALDO-CSDP with n number of SCs, requires $n+1$ switches to connect the SCs to unregulated power supply and LDO. $2n$ switches to connect ground and LDO when discharging. Considering the basic SCALDO topology, the first step of this strategy is to eliminated and added pass-elements to an LDO. So that the switch in the immediate vicinity of the LDO in charging phase was removed as illustrates in in Fig. A.1. This was possible as series pass-element itself can act as a switch. Next, the same procedure was followed to remove the switch in discharging phase; as illustrates in in Fig. A.2.

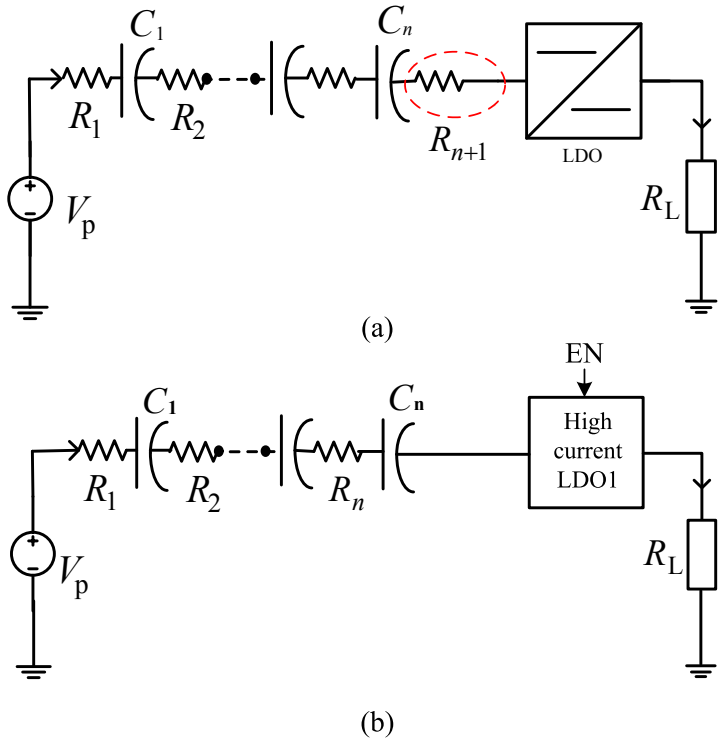


Figure A.1: n number of SCs connected in series: (a) SCALDO charging configuration. one switch is immediately visible to LDO and (b) removed the switch in SCALDO and include the enabling function to high current LDO

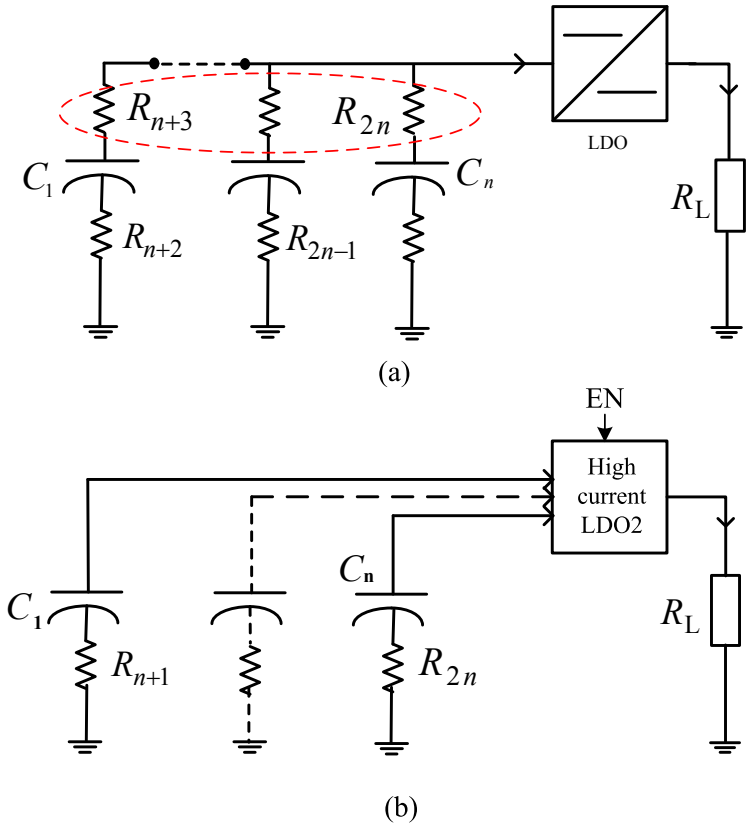


Figure A.2: n number of SCs connected in parallel: (a) SCALDO discharging configuration. n switches are immediately visible to LDO and (b) removed the switched in SCALDO and include the enabling function to a high current LDO with parallel pass-elements

A.1 Generalized RS-SCALDO circuit

The switches that can be removed from SCALDO are shown in Fig. A.1(a) and Fig. A.2(a). Therefore, two LDOs with a common output are required for the operation of the new reduced-switch SCALDO (RS-SCALDO) as in Fig. A.1(b) and Fig. A.2(b). They are connected in parallel with a common output, work alternatively in the charging and discharging phases. Compared to a general CSDP-SCALDO case, $n + 1$ switches can be eliminated by applying this strategy. A similar number of switches can be reduced by applying it to the SCALDO-CPDS configuration. This new reduced-switch SCALDO (RS-SCALDO) is in Fig. A.3. Paralleling the MOSFET pass-elements in LDO can reduce its ON-resistance losses and increase the current capability of LDO.

In practical prototypes, a low-power micro-controller is used to control these very low frequency switches, which change state at milihertz to a few hundred hertz frequencies. This alternative operation of LDOs reduce the load-stress applied on the circuit, unlike a single LDO configuration. The ESR and the dynamic losses in switches are found to be less significant than the static (conduction) losses in switches as discussed Chapter 3.

During SCALDO operation, SCs store and release energy back to the LDO at very low cycle rates. As shown in Fig.s 2.17 and 2.18, $(3n+1)$ power switches are required

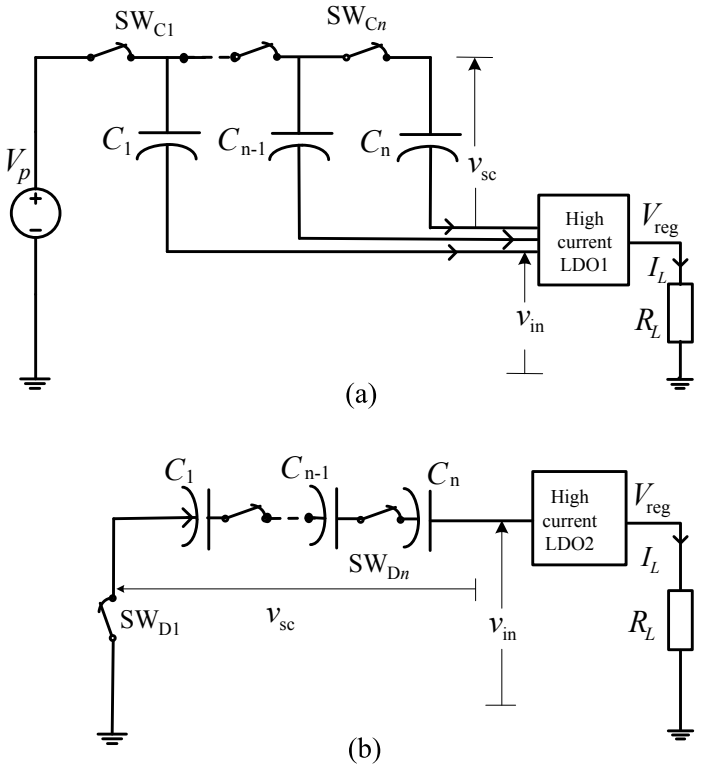


Figure A.3: General RS-SCALDO-CPDS configuration: (a) supercapacitor charging, and (b) discharging

for a general SCALDO configuration, where n is the number of SCs in the topology. The switches are used exclusively for the purpose of changing SCs between charging and discharging configurations, and do not contribute to voltage conversion. Since the capacitance is high, the frequency of switch operation f_{op} is very low,

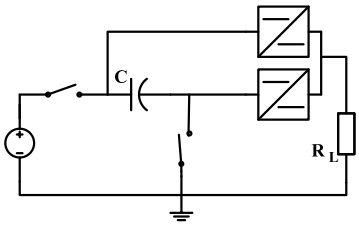
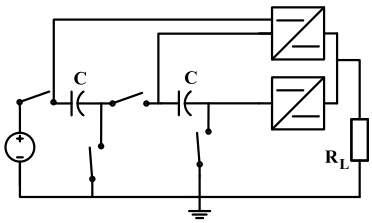
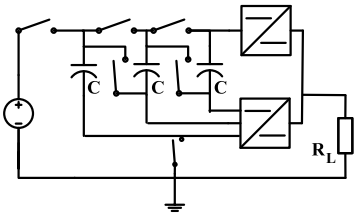
$$f_{\text{op}} = \frac{1}{t_{\text{c}} + t_{\text{d}}} = \frac{1}{(1+k)t_{\text{c}}} = \frac{1}{(1+k)} f_{\text{c}} = \frac{I}{(1+k)C\Delta V} \tag{A.1}$$

where t_{c} and t_{d} are respectively charge and discharge times for constant I and $(1+k)$ is the efficiency multiplication factor. Here, f_{c} is the capacitor charging frequency. For $n = 1$, $k = 1$, therefore, f_{op} is $f_{\text{c}}/2$.

A.2 Comparison of SCALDO and RS-SCALDO circuit topologies

Table A.1 compares RS-SCALDO topologies with three basic cases of SCALDO configurations in terms of number of switches required. It shows that the switch reduction strategy can reduce 40–50% of switches from these common SCALDO configurations.

Table A.1: Comparison of SCALDO and RS-SCALDO switches

SCALDO Configuration	RS-SCALDO Topology	No. switches in SCALDO $3n+1$	No. of switches in RS-SCALDO $2n$
12-to-5V		4	2
5-to-1.5V		7	4
5-to-3.3V		10	6

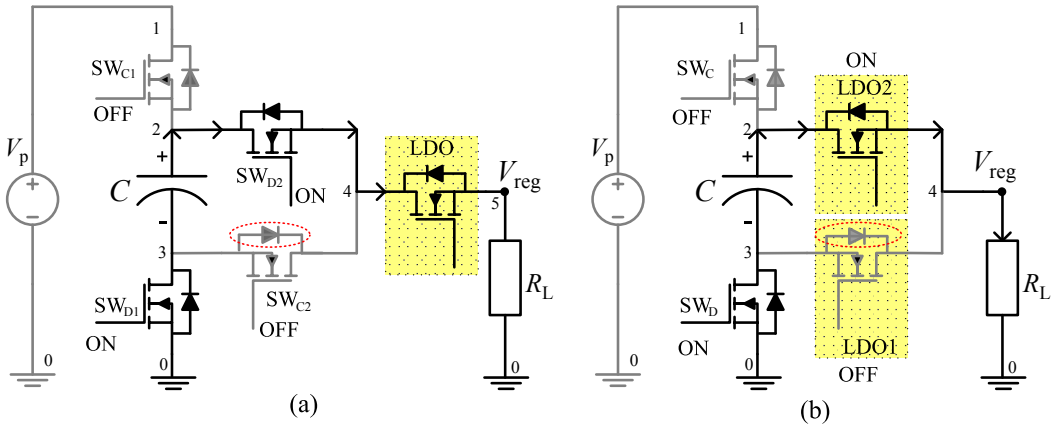


Figure A.4: Remedy for unwanted SC-discharge and discrete design for high current applications: (a) SCALDO, and (b) RS-SCALDO

Previously built 5-to-2 V, 1 A SCALDO consists of an off-the-shelf LDO, four solid-state relays and a thin profile SC. These solid-state relays eliminate the unwanted discharge in SC. However, a high-current design requires an LDO with very low dropout voltage and solid-state relays with very low ON-resistance. One possible solution to increase current handling capability is to connect many LDOs in parallel, although this increases

the cost. Compared to a discrete MOSFET-based design, off-the-shelf high-current components are expensive. To reduce the cost power-phase of the high-current SCALDO version can be designed with discrete components. The MOSFET-based switches can be arranged as in FigA.4(a) to eliminate body-diode issue. However, a discrete version occupies a larger PCB area than an IC-based design.

Figure A.4 shows the power-stage of discrete design for single SC-based, high-current SCALDO and RS-SCALDO. As seen in Fig. A.4(a), there are two extra switches (MOSFETs) required for the SCALDO, and those two switches require two driver circuits. Table A.2 summarizes the basic blocks of SCALDO and RS-SCALDO. When compared to the cost of the PCB area and number of switches, RS-SCALDO is a better solution than SCALDO. However, the RS-SCALDO control circuit has additional components which are the four analog switches. They are activated alternatively (i) to connect one of the pass-elements to the output of the common feedback loop, and (ii) to direct the voltage sensing signal of ADC to the input sides of the activated LDO. Analog switches in this design handle very low power signals and they can easily be found in smaller packages.

Table A.2: Comparison of single SC-based SCALDO and RS-SCALDO

Components	Existing SCALDO circuit	SCALDO	RS-SCALDO
LDO	Off-the-shelf LDO	1 MOSFET for pass-element 1 feedback circuit	2 MOSFETs for pass-element 1 feedback circuit
Power switches	4 solid-state relays	4 MOSFETs	2 MOSFETs
Control circuit	PIC micro-controller with an ADC	PIC micro-controller with an ADC	PIC micro-controller with an ADC 4 Analog switches
Switch drivers	Solid-state relays are driven by PIC signals	4 switch divers	2 switch divers

Appendix B

Implementation of 3.5-to-1.5 V, 5 A RS-SCALDO

B.1 PCB design of the RS-SCALDO

A simplified the schematic in Fig. B.1 form a basic configuration where a single supercapacitor (SC) based RS-SCALDO configuration. 3.5-to-1.5 V regulator is a compact prototype version designed utilizing a single SC, two switches, two LDOs with a common control circuit; the PCB design and the implementation are shown in Fig. B.8 and B.8(c). In designing this prototype, following basic components in the Table B.3 were used.

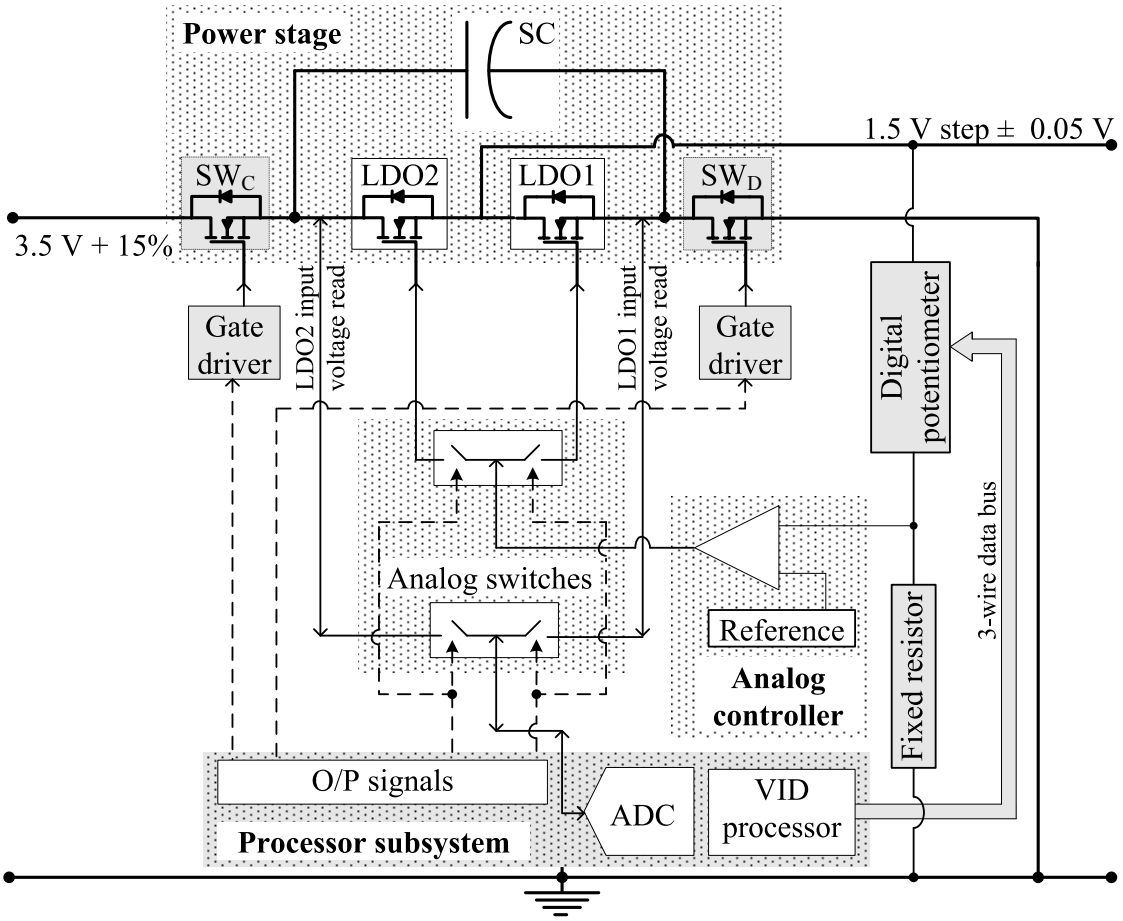


Figure B.1: Simplified diagram of the schematic of the 3.5-to-1.5V SCALDO regulator

B.2 VID logic implementation in RS-SCALDO

Theory of operation RS-SCALDO-based VID logic

In order to change the output voltage of RS-SCALDO, the value of R_2 resister in the output sampling circuit of the feedback control-loop was changed. The reference voltage of non-inverting input of the error amplifier is equal to V_{ref} and therefore, inverting input voltage is

$$V^{-} = V_{\text{reg}} \left(\frac{R_1}{R_1 + R_2} \right)$$

The R_2 is the sum of a fixed resistor R_{21} and a variable resister of digital potentiometer R_{22}. Here, R_{21} value limit the minimum resistance of the R_2, that will prevent occurring a high output voltage during a delay transition.

$$R_2 = R_{21} + R_{22}$$

Therefore,

$$V_{\text{ref}} = V_{\text{reg}} \left(\frac{R_1}{R_1 + R_2} \right)$$

The variable resistance is

$$R_{22} = R_1 \left(\frac{V_{\text{ref}}}{V_{\text{reg}} - V_{\text{ref}}} \right) - R_{21}$$

A single channel, digital controlled variable resistor device (DVM) was used to change the R_2 resistor. Changing the programmed DPM setting is accomplished by clocking in a 10-bit serial data word into s serial input pin. It has two address bits, most significant bit (MSB) first, followed by eight data bits, also MSB first. A serial data output pin at the opposite end of the serial register allows simple daisy chaining in multiple DPM applications without additional external decoding logic.

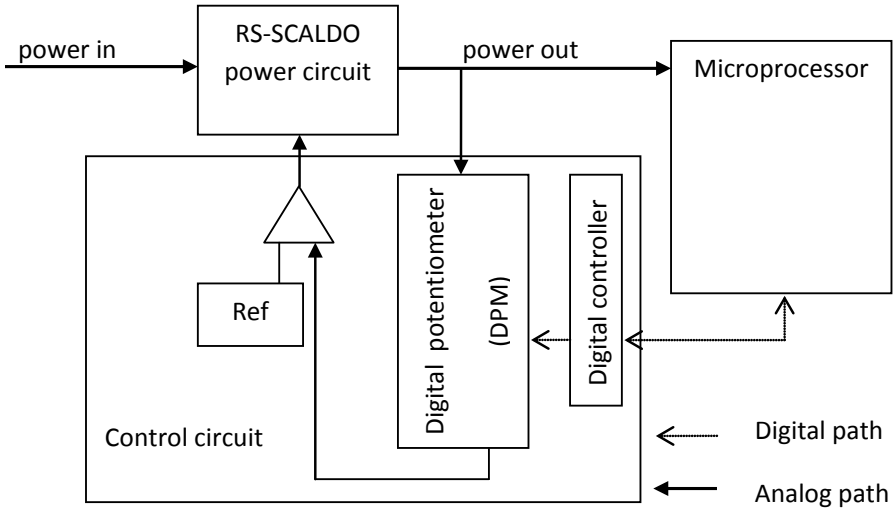


Figure B.2: A block diagram of a digitally-controlled RS-SCALDO-based VRM

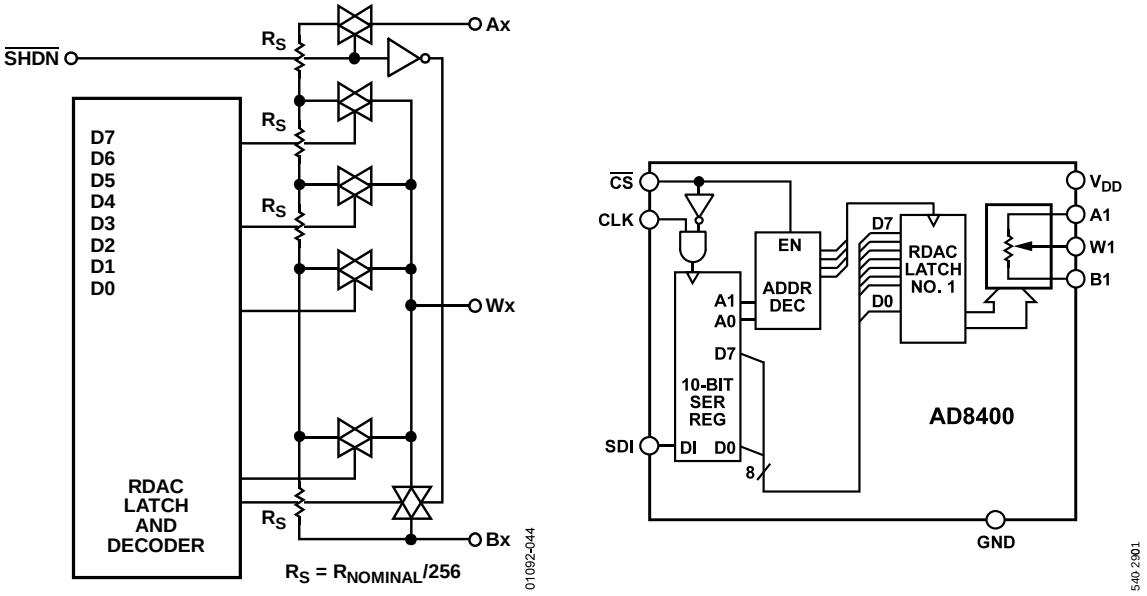


Figure B.3: Equivalent circuit and the block diagram of AD8400 digital potentiometer [113]

Mnemonic	Description
B1	Terminal B RDAC.
GND	Ground.
$\overline{CS}$	Chip Select Input, Active Low. When $\overline{CS}$ returns high, data in the serial input register is decoded, based on the address bits, and loaded into the target DAC register.
SDI	Serial Data Input.
CLK	Serial Clock Input, Positive Edge Triggered.
V_{DD}	Positive Power Supply. Specified for operation at both 3 V and 5 V.
W1	Wiper RDAC, Addr = 00_2.
A1	Terminal A RDAC.

Figure B.4: AD8400 pin function descriptions [113]

ADDR		DATA							
B9	**B8**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
MSB	LSB	MSB							LSB
2^9	2^8	2^7							2^0

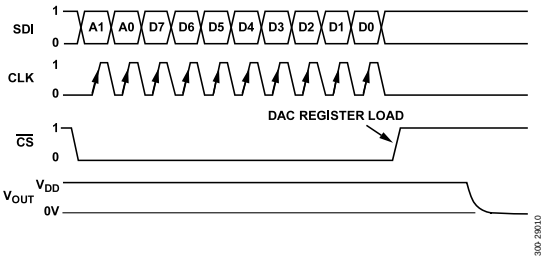


Figure B.5: Data word and the timing diagram of AD8400 digital potentiometer [113]

For this experiments, AD8400 was used which contains a single variable resistor with 10 kΩ. These devices perform the same electronic adjustment function as a mechanical potentiometer or variable resistor. It offers a completely programmable value of resistance between the A terminal the wiper or the B terminal and the wiper (W). The format of the data word and an illustration of clock diagram is seen in Fig. B.5.

The nominal resistance (R_{AB}) of the DPM has 256 contact points accessible by the wiper terminal, and the resulting resistance can be measured either across the wiper and B terminals (R_{WB}) or across the wiper and A terminals (R_{WA}). The wiper's first connection

Table B.1: 8-bit data samples for VID

Output voltage (V)	8-bit data word
1.45	0000 1110
1.50	0001 1001
1.55	1101 0101

Table B.2: Control bits for VID

	Bit	Status
Initially (no operation)	$\overline{CS}$	high
	CLK	low
Input bits to DPM	$\overline{CS}$	low
	CLK	high
	$\overline{SDI}$	data bits
Stop input bits to DPM	$\overline{CS}$	high
	CLK	low

starts at the B terminal for data 00_{H}. This B terminal connection has a wiper contact resistance of 50Ω. The resolution of DPM is approximately 39 Ω (10 kΩ/256 ≈ 39 Ω). For n^{th} connection, the $(n-1)^{th}$ tap point located at $39n + 50$ Ω. The 8-bit data-word loaded into the RDAC latch is decoded to select one of the 256 possible settings.

The general transfer equation that determines the digitally programmed output resistance between Wx and Bx is

$$R_{\mathrm{WB}} = R_{\mathrm{W}} + \left(\frac{D}{256}\right) R_{\mathrm{AB}}$$

where D, in decimal, is the data loaded into the 8-bit RDAC# latch, and R_{AB} is the nominal end-to-end resistance that equals $50 + 39D$ (Ω).

The dummy processor signals (serial data word) was generated using a PIC16F468 micro-controller. They do not have inbuilt serial communication modules; therefore, the data word was manually fed to DPM. Corresponding data words for output 1.45, 1.5 and 1.55 V cases and the control signals of the operation are given in Table. B.1 and B.2 respectively. PIC programs of these is in Appendix B.3.3.

Compare RS-SCALDO-based VID with SMPS-based VID logic

The multiphase synchronous buck converter is the most popular topology for voltage regulator modules (VRMs). Using dynamic voltage identification (VID) technology, a microprocessor is able to dynamically set an optimal operating voltage based on its utilization condition and sends a serialVID (sVID) command to the VRM. The sVID bus is running at 25 MHz and is transferring the power management information between CPU-

and sVID-based VRMs. The VRM will then execute and position its reference voltage to the targeted operating voltage upon receiving the command. It is desirable that the VRM respond to the sVID command immediately and settle its output voltage with the allowed delay [135].

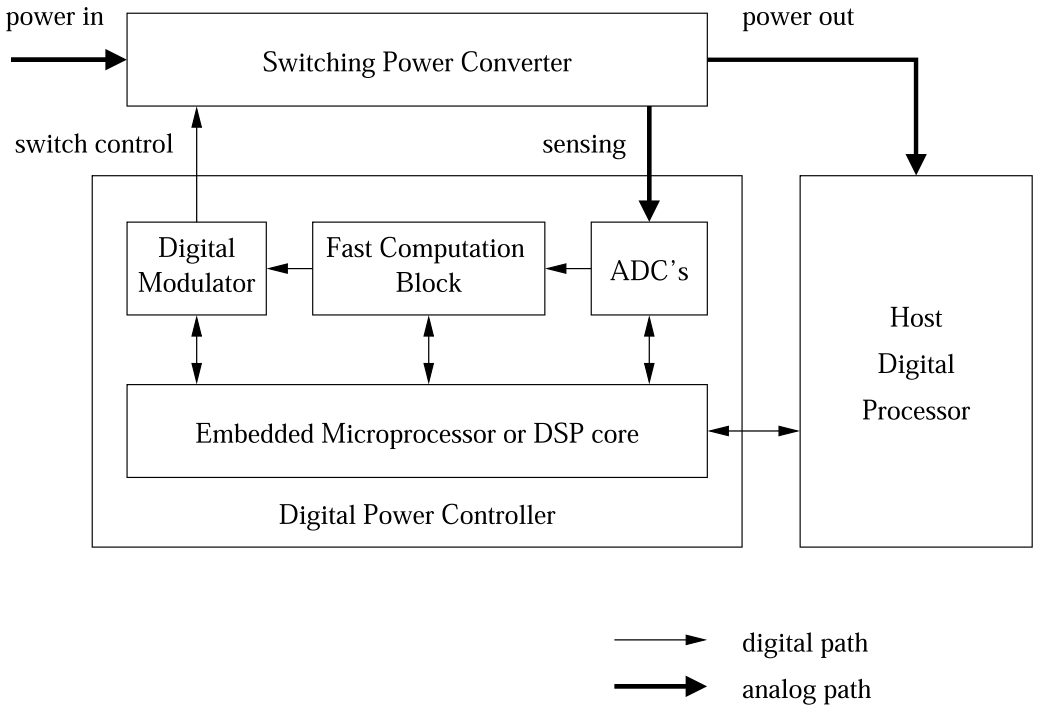


Figure B.6: A block diagram of a digitally-controlled VRM delivering power to a microprocessor [32]

Fig. B.6 illustrates a block diagram of a digital controller for a SMPS-based VRM delivering power to a host microprocessor. The input power supplies to SMPS is a AC-DC power supply or a battery. The output power of SMPS is fed to a microprocessor, graphics processor, etc. The digital power controller uses analog-to-digital converters (ADC) to sample analog power supply variables, such as voltages, currents, and temperature. These quantities are processed by control laws implemented in a fast computational block. The control laws calculate control signals which are converted to switch on/off command sequences by a digital modulator, such as a digital pulse-width modulator (DPWM) [32].

Compared to dynamic VID approaches in SMPS-based, the method used in RS-SCALDO is less complex.

B.3 Estimation of control circuit power requirement and losses

The RS-SCALDO control circuit uses very low power components. Circuit components are listed in Table. B.3 with their essential specifications.

Table B.3: A summary of components in the RS-SCALDO prototype

Component	Part#	Manufacturer	Essential specifications
N-channel MOSFETs for LDOs and switches	AUIRL3705	Analog Devices Inc	minimum R_{on} 6.8mΩ; breakdown V_{DS} 55V; forward transconductance 150S; threshold V_{GS} 1.0 to 3.0V
N-channel MOSFETs for gate control circuit	2N7000	Fairchild semiconductor	maximum I_{DS} 200mA, maximum power dissipation 400mW; maximum R_{on} 60V; turn-ON/OFF time 10ns
Operational amplifier of the LDO feedback loop	OP491	Analog Devices Inc	supply I 300μA/A; bandwidth 3MHz; slew rate 0.5V/μs; offset V 700μV
Band gap reference for the feedback circuit	AD584	Analog Devices Inc	maximum quiescent I 1.0mA ; output I 10mA; maximum error at 2.5V output maximum ±7.5 mV; maximum deviation from 25°C 30pmm/°C
12-to-5 V pre-regulator	REF195	Analog Devices Inc	temperature coefficient: 5ppm/°C maximum; high output current: 30mA; low supply current: 45μA maximum; initial accuracy: ±2mV; sleep mode 15μA maximum I; load regulation 4 ppm/mA; line regulation 4ppm/V
Analog switch	HEF4016B	NXP	isolation resistance 8kΩ; maximum ground I 30μA; maximum leakage at off 200nA, maximum power dissipation per switch 100mW
Buffer capacitors	RL80G821	NICHICON	V 4V; capacitance 820μF ± 20%; ESR 0.006Ω; lifetime at temperature: 10000hrs at 105°C
Microcontroller (to sense voltage and send signals to operate the control system)	PIC16F486	Microchip	single-cycle instructions except branches; 200ns instruction cycle; software selectable frequency range of 8MHz to 125kHz; standby I: 50nA at 2.0V; operating I 11μA at 32kHz, 2V and 220μA at 4MHz, 2V ;
Digital potentiometer	AD8400	Analog Devices Inc	256-position variable resistance device; power shutdown less than 5μA;3-wire; SPI-compatible serial data input

Here, I divided the control circuit to five sub-circuits to analyze power consumption. The control circuit consists of: [i.] feedback control loop; [ii.] two gate drivers and LDOs

enabling circuit; [iii.] PIC micro-controller; [iv.] analog switches; and [v.] 12-to-5 V converter.

The error amplifier, gate drivers and analog switches are powered by 12 V rail. The PIC micro-controller and the voltage reference IC use 5 V from a low power 12-to-5 V converter.

i. The feedback control loop;

Powering the feedback control loop = digital potentiometer + two resistors + error amplifier (for maximum load 5 A)

$$P_{\text{fb}} = P_{\text{pm}} + I_{\text{fb}}^2 R + P_{\text{amp}} \tag{B.1}$$

$$P_{\text{fb}}^{\max} = 5\mu\text{A} \times 5\text{V} + \left[\frac{1.55\ \text{V}}{30\text{k}\Omega}\right]^2 \times 30\text{k}\Omega + [5 \times 300\mu\text{A} \times 12\text{V}] = 356\mu\text{W}$$

ii. Two gate drivers;

Powering the two gate drivers and enabling LDOs= power supply side switch + ground side switch + enabling LDOs

$$P_{\text{gd}} = P_{\text{sw1}} + P_{\text{sw2}} + P_{\text{LDO\_cnt}} \tag{B.2}$$

$$P_{\text{gd}}^{\max} = \left[\frac{5\ \text{V}}{2.2\text{k}\Omega}\right]^2 \times 2.2\text{k}\Omega + \left[\frac{12\ \text{V}}{1\text{M}\Omega}\right]^2 \times 1\text{M}\Omega + \left[\frac{5\ \text{V}}{3.3\text{k}\Omega}\right]^2 \times 3.3\text{k}\Omega = 18.72\text{mW}$$

iii. PIC micro-controller

Powering the PIC micro-controller = I/O pins + operating + standby

$$P_{\text{pic}} = 2 \times 2.27\text{mA} \times 5\text{V} + 2.25\mu\text{A} \times 5\text{V} + 2.5\text{nA} \times 5\text{V} \approx 22.81\text{mW} \tag{B.3}$$

iv. Four analog switches(operating + leakage)

$$P_{\text{asw}} = P_{\text{asw}} + P_{\text{lkg}} \tag{B.4}$$

$$P_{\text{asw}} = 21\mu\text{A} \times 12\text{V} + 1\mu\text{A} \times 12\text{V} = 264\mu\text{W}$$

v. Losses in 12-to-5 V converter

$$P_{\text{12-5}} = V_{\text{12-5}} I_{\text{12-5}} \tag{B.5}$$

$$P_{\text{12-5}}^{\max} = 12\ \text{V} \times 45\mu\text{A} = 540\mu\text{W}$$

Total power required for the control circuit at maximum load 5 A:

$$P_{\text{cnt}} = P_{\text{fb}}^{\max} + P_{\text{gd}}^{\max} + P_{\text{pic}} + P_{\text{asw}} + P_{\text{12-5}}^{\max} = 42.69\text{mW} \tag{B.6}$$

B.3.1 PIC program with two control signals

```
// PIC16F Configuration Bit Settings
// By Thilini Wickramasinghe
#include <stdio.h>
#include <htc.h>
#include <pic16F684.h>
#include <stdlib.h>
#include <pic.h>

__CONFIG(FOSC_INTOSC & WDTE_OFF & PWRTE_OFF &
__MCLRE_OFF & CP_OFF & CPD_OFF & BOREN_OFF &
  __CLKOUTEN_OFF & IESO_ON & FCMEN_ON);
__CONFIG(WRT_OFF & PLLEN_OFF & STVREN_ON & BORV_LO & LVP_ON);

const int ldo_v_min = 340; //316; // 1.543V at Vin(LDO) sensing point
 //(1.5V output; voltage divider)
int i, state_ch, ADC_value ;  //For delay loop and configuration state
// If charging state_ch=1 and when discharging state_ch=0
// PIC16F1826 Configuration Bit Settings

void main(){
  TRISC= 0B00000000; //Define DIRECTION of channels- OUTPUT=0
  ADCON1= 0B10010000; // ADFM=1; ADCS=001; Vref-=Vss; Vref+=Vdd
                      //A/D conversion clock selection bit,
            //2 us FOSC/8
                      // Totla convertion time ~100us
 //---------------------------------------------------------------------
  PORTC= 0B00000000;  //Reset the port - open all the switches
  for(i=0; i<100; i++); // Delay
  TRISA= 0B00000010; //Define DIRECTION of channels- INPUT=1, pin 18
  ANSELA= 0B00000010; //Port configuration - 12(ANS1-AN1) pin as analog,
    //RC0-RC3 digital chanels- pin 18
  ADCON0= 0B10000101; //conversation stop, Analog channel selection
                       //- 18(ANS1-AN1) pin
 for(i=0; i<100; i++);
 // Delay for acquisition time 10 us for CHOLD cap of ADC
 state_ch =1;
 PORTC=0B00001000;//Initially set to charge pin-7=ON, pin-9=OFF
```

```
 for(i=0; i<100; i++);
while(1)
     {    //Charging Cycle
           while(state_ch==1)
           {
             GO_nDONE=1;
             while(GO_nDONE);
             ADC_value= 0;
             ADC_value= ADRESH;
             ADC_value= ADC_value<<8;
             ADC_value= ADC_value | ADRESL;     // copy results
            if (ldo_v_min > ADC_value)
            {  state_ch =0;
               PORTC=0B10000000;
               //set to discharge pin 9=ON, 7=OFF
               for(i=0; i<100; i++);
 // Delay for acquisition time > 10 us for CHOLD cap of ADC
 //-------------------------------------------------------------------
            }
         }
         //Discharging Cycle
         while (state_ch==0)
         {   GO_nDONE=1;
             while(GO_nDONE);
             ADC_value= 0;
             ADC_value= ADRESH;
             ADC_value= ADC_value<<8;
             ADC_value= ADC_value | ADRESL;// copy results
            if (ldo_v_min > ADC_value)
            {
       state_ch =1;
             PORTC=0B00001000;//set to charge pin-7=ON, pin-9=OFF
             for(i=0; i<100; i++);
        // Delay for acquisition time > 10 us for CHOLD cap of ADC
            }
        }
      }
 }
```

B.3.2 PIC program with four control signals with transition delays

```
//Modified to change the dead time during transitions
//to prevent regulation reach to zero
#include <stdio.h>
#include <htc.h>
#include <pic16f684.h>
#include <stdlib.h>
// Initial configuartions
const int ldo_v_min = 340; //1.66V ;316;// 1.543V at Vin(LDO) sensing point
//(1.5V output; voltage divider)
int i, state_ch, ADC_value;  //For delay loop and configuration state
// If charging state_ch=1 and when discharging state_ch=0
// PIC16F684 Configuration Bit Settings
__CONFIG(FOSC_INTOSCCLK & WDTE_OFF & PWRTE_OFF &
__MCLRE_ON & CP_OFF & CPD_OFF & BOREN_OFF & IESO_OFF & FCMEN_OFF);

void main(){
  TRISC= 0B00000000; //Define DIRECTION of channels- OUTPUT=0
  ADCON1=0B00110000; //A/D conversion clock selection bit ,
//ADCS0= 1 and ADCS1=0 => 2 us FOSC/8
                        // Totla convertion time ~100us
 //---------------------------------------------------------------------
  PORTC= 0B00000000;  //Reset the port - open all the switches
  for(i=0; i<100; i++); // Delay
  TRISA= 0B00000010; //Define DIRECTION of channels- INPUT=1, pin 12
  ANSEL= 0B00000010; //Port configuration - 12(ANS1-AN1) pin as analog,
   //RC0-RC3 digital chanels- pin 12
  ADCON0= 0B10000101; //Right justified, voltage reference =Vdd,
//conversation stop, Analog channel selection
                        //- 12(ANS1-AN1) pin
 for(i=0; i<100; i++);
 // Delay for acquisition time 10 us for CHOLD cap of ADC
 state_ch =1;
 //PORTC=0B00001110;//Initially set SW1 ON
 PORTC=0B00001100;//Initially set SW1 and LDO1 ON >>>> SC CHARGING
 for(i=0; i<750; i++);
```

```
while(1)
     {
      //Charging Cycle
           while(state_ch==1)
           {
             GO_nDONE=1;
             while(GO_nDONE);
             ADC_value= 0;
             ADC_value= ADRESH;
             ADC_value= ADC_value<<8;
             ADC_value= ADC_value | ADRESL;     // copy results
            if (ldo_v_min > ADC_value)
            {
            state_ch =0;
                PORTC=0B00001000;
                //set to LDO1 OFF, LDO2 ON, SW1 ON Sence1 ON, SW2 OFF
                for(i=0; i<120; i++);
                PORTCbits.RC1=1;//LDO1 OFF -SLOW
                PORTC=0B00001010;
                for(i=0; i<100; i++);
                PORTCbits.RC3=0;//SW2 OFF -SLOW
                PORTC=0B00000010;
                PORTC=0B00000011; //set to LDO1 OFF,
     //LDO2 ON, SW1 OFF,SW2 ON Sence2 ON>>>> SC DISCHARGING
      for(i=0; i<200; i++);
      // Delay for acquisition time > 10 us for CHOLD cap of ADC
     //-----------------------------------------------------------------
            }
         }
         //Discharging Cycle
         while (state_ch==0)
         {
             GO_nDONE=1;
             while(GO_nDONE);
             ADC_value= 0;
             ADC_value= ADRESH;
             ADC_value= ADC_value<<8;
             ADC_value= ADC_value | ADRESL;// copy results
```

```
            if (ldo_v_min > ADC_value)
            {
 state_ch =1;

                 PORTCbits.RC1=0;//LDO1 ON -SLOW
                 PORTC=0B00000010;
                 //set to LDO1 OFF, LDO2 ON, SW1 ON Sence1 ON, SW2 OFF
                 for(i=0; i<120; i++);
                 PORTCbits.RC3=1; //SW2 OFF - FAST
                 PORTC=0B00001010;
                 //set to LDO1 OFF, LDO2 ON, SW1 ON Sence1 ON, SW2 OFF
                 for(i=0; i<100; i++);
                 PORTC=0B00001000;
                 //set to LDO1 OFF, LDO2 ON, SW1 ON Sence1 ON, SW2 OFF
                 for(i=0; i<30; i++);
                 PORTC=0B00001100;
                 //set to LDO1 ON, LDO2 OFF, SW1 ON, SW2 OFF >>>> SC CHARGING
                 for(i=0; i<200; i++);
                 // Delay for acquisition time > 10 us for CHOLD cap of ADC
            }
        }
      }
 }
```

B.3.3 Simulation of processor signals for VID

```
#include <stdio.h>
#include <htc.h>
#include <pic16f684.h>
#include <stdlib.h>
#include <pic.h>
// Initial configuartions
int i, j,k, state_on ;

#define _XTAL_FREQ 4000000

// PIC16F684 Configuration Bit Settings
__CONFIG(FOSC_INTOSCCLK & WDTE_OFF & PWRTE_OFF &
__MCLRE_ON & CP_OFF & CPD_OFF & BOREN_OFF & IESO_OFF & FCMEN_OFF);
```

```
void main(){

 PORTC=0B00000000;      //Reset the port
 __delay_us(10); // Delay for acquisition time 10 us for CHOLD cap of ADC
 TRISC= 0B00000000; //Define DIRECTION of channels- for OUTPUT=0 in PORTC
 PORTA=0B00000000;  //Clear the port - open all the switches
 __delay_us(10); // Delay for acquisition time 10 us for CHOLD cap of ADC


 ANSEL=0x00;// Define as Digital data
 IRCF0=0;   //set the internal clock to 4MHz Usually the default 4MHz
 IRCF1=1;
 IRCF2=1;

 RA2= 0;//CLK clock // pin 11
 __delay_us(100);

    while(1)//never ending loop
    {
         while(state_on==1)
        {    //1.45 V
             // RS=1; SHDN=1; CS=0; SDI=X; Shift one bit from SDI

             PORTC=0B00001100;   //D0 RS=1; SHDN=1; CS=0; SDI=X;
             __delay_ms(110);    //Initial delay of first bit
             RA2=1;              //CLK clock 1
             __delay_ms(150);
             RA2=0;              //CLK clock
             __delay_ms(150);

             PORTC=0B00001100;   //D1 RS=1; SHDN=1; CS=1; SDI=X;
             __delay_ms(50); //Initial delay of first bit
             RA2=1; //CLK clock 1
             __delay_ms(150);
             RA2=0; //CLK clock
             __delay_ms(150);

               PORTC=0B00001100;   //D2 RS=1; SHDN=1; CS=1; SDI=X;
```

```
 __delay_ms(50);
 RA2=1; //CLK clock 2
 __delay_ms(150);
 RA2=0; //CLK clock
 __delay_ms(150);

 PORTC=0B00001100;   //D3 RS=1; SHDN=1; CS=1; SDI=X;
 __delay_ms(50);
 RA2=1; //CLK clock 3
 __delay_ms(150);
 RA2=0; //CLK clock
 __delay_ms(150);

 PORTC=0B00001100;   //D4 RS=1; SHDN=1; CS=1; SDI=X;
 __delay_ms(50);
 RA2=1; //CLK clock 5
 __delay_ms(150);
 RA2=0; //CLK clock
 __delay_ms(150);

 PORTC=0B00001101;   //D5 RS=1; SHDN=1; CS=1; SDI=X;
 __delay_ms(50);
 RA2=1; //CLK clock 6
 __delay_ms(150);
 RA2=0; //CLK clock
 __delay_ms(150);

 PORTC=0B00001101;   //D6 RS=1; SHDN=1; CS=1; SDI=X;
__delay_ms(50);
RA2=1; //CLK clock 7
 __delay_ms(150);
 RA2=0; //CLK clock
 __delay_ms(150);

 PORTC=0B00001100;   //D7  RS=1; SHDN=1; CS=1; SDI=X;
__delay_ms(50);
RA2=1; //CLK clock 8
 __delay_ms(150);
 RA2=0; //CLK clock
```

```
        __delay_ms(150);

        PORTC=0B00001100;   //A0 data RS=1; SHDN=1; CS=1; SDI=X;
        __delay_ms(50);
        RA2=1; //CLK clock 9
        __delay_ms(150);
        RA2=0; //CLK clock
        __delay_ms(150);

        PORTC=0B00001100;   //A1 data RS=1; SHDN=1; CS=1; SDI=X;
        __delay_ms(50);
        RA2=1; //CLK clock 10
        __delay_ms(150);
        RA2=0; //CLK clock
        __delay_ms(150);

        PORTC=0B00001110;   //FINAL State:
        //Load data RS=1; SHDN=1; CS=1 -> Load data; SDI=X;
        __delay_ms(1);

     //  __delay_ms(10000);//10 s delay
        // state= 3; //Regulation 1.55 V
        state_on=0;
}

 while(state_on==2)
{       //1.5 V
        // RS=1; SHDN=1; CS=0; SDI=X; Shift one bit from SDI

        PORTC=0B00001100;   //D0 RS=1; SHDN=1; CS=0; SDI=X;
        __delay_ms(110); //Initial delay of first bit
        RA2=1; //CLK clock 1
        __delay_ms(150);
        RA2=0; //CLK clock
        __delay_ms(150);

        PORTC=0B00001100;   //D1 RS=1; SHDN=1; CS=1; SDI=X;
        __delay_ms(50); //Initial delay of first bit
        RA2=1; //CLK clock 1
```

```
 __delay_ms(150);
 RA2=0; //CLK clock
 __delay_ms(150);

 PORTC=0B00001100;   //D2 RS=1; SHDN=1; CS=1; SDI=X;
 __delay_ms(50);
 RA2=1; //CLK clock 2
 __delay_ms(150);
 RA2=0; //CLK clock
 __delay_ms(150);

 PORTC=0B00001100;   //D3 RS=1; SHDN=1; CS=1; SDI=X;
 __delay_ms(50);
 RA2=1; //CLK clock 3
 __delay_ms(150);
 RA2=0; //CLK clock
 __delay_ms(150);

 PORTC=0B00001100;   //D4 RS=1; SHDN=1; CS=1; SDI=X;
 __delay_ms(50);
 RA2=1; //CLK clock 5
 __delay_ms(150);
 RA2=0; //CLK clock
 __delay_ms(150);

 PORTC=0B00001101;   //D5 RS=1; SHDN=1; CS=1; SDI=X;
 __delay_ms(50);
 RA2=1; //CLK clock 6
 __delay_ms(150);
 RA2=0; //CLK clock
 __delay_ms(150);

 PORTC=0B00001101;   //D6 RS=1; SHDN=1; CS=1; SDI=X;
__delay_ms(50);
RA2=1; //CLK clock 7
 __delay_ms(150);
 RA2=0; //CLK clock
 __delay_ms(150);
```

```
        PORTC=0B00001101;   //D7  RS=1; SHDN=1; CS=1; SDI=X;
       __delay_ms(50);
       RA2=1; //CLK clock 8
        __delay_ms(150);
        RA2=0; //CLK clock
        __delay_ms(150);

        PORTC=0B00001101;   //A0 data RS=1; SHDN=1; CS=1; SDI=X;
        __delay_ms(50);
        RA2=1; //CLK clock 9
        __delay_ms(150);
        RA2=0; //CLK clock
        __delay_ms(150);

        PORTC=0B00001101;   //A1 data RS=1; SHDN=1; CS=1; SDI=X;
        __delay_ms(50);
        RA2=1; //CLK clock 10
        __delay_ms(150);
        RA2=0; //CLK clock
        __delay_ms(150);

        PORTC=0B00001110;   //FINAL State:
        //Load data RS=1; SHDN=1; CS=1 -> Load data; SDI=X;
        __delay_ms(1);

      // __delay_ms(10000);//10 s delay
      // state= 1; //Regulation 1.45 V
        state_on=0;
}
while(state_on==3)
{      //1.55 V
       // RS=1; SHDN=1; CS=0; SDI=X; Shift one bit from SDI

       PORTC=0B00001100;   //D0 RS=1; SHDN=1; CS=0; SDI=X;
       __delay_ms(110); //Initial delay of first bit
       RA2=1; //CLK clock 1
       __delay_ms(150);
       RA2=0; //CLK clock
       __delay_ms(150);
```

```
 PORTC=0B00001100;   //D1 RS=1; SHDN=1; CS=1; SDI=X;
 __delay_ms(50); //Initial delay of first bit
 RA2=1; //CLK clock 1
 __delay_ms(150);
 RA2=0; //CLK clock
 __delay_ms(150);

 PORTC=0B00001100;   //D2 RS=1; SHDN=1; CS=1; SDI=X;
 __delay_ms(50);
 RA2=1; //CLK clock 2
 __delay_ms(150);
 RA2=0; //CLK clock
 __delay_ms(150);

 PORTC=0B00001100;   //D3 RS=1; SHDN=1; CS=1; SDI=X;
 __delay_ms(50);
 RA2=1; //CLK clock 3
 __delay_ms(150);
 RA2=0; //CLK clock
 __delay_ms(150);

 PORTC=0B00001101;   //D4 RS=1; SHDN=1; CS=1; SDI=X;
 __delay_ms(50);
 RA2=1; //CLK clock 5
 __delay_ms(150);
 RA2=0; //CLK clock
 __delay_ms(150);

 PORTC=0B00001100;   //D5 RS=1; SHDN=1; CS=1; SDI=X;
 __delay_ms(50);
 RA2=1; //CLK clock 6
 __delay_ms(150);
 RA2=0; //CLK clock
 __delay_ms(150);

 PORTC=0B00001100;   //D6 RS=1; SHDN=1; CS=1; SDI=X;
__delay_ms(50);
RA2=1; //CLK clock 7
```

```
                __delay_ms(150);
                RA2=0; //CLK clock
                __delay_ms(150);

                PORTC=0B00001101;   //D7  RS=1; SHDN=1; CS=1; SDI=X;
               __delay_ms(50);
               RA2=1; //CLK clock 8
                __delay_ms(150);
                RA2=0; //CLK clock
                __delay_ms(150);

                PORTC=0B00001100;   //A0 data RS=1; SHDN=1; CS=1; SDI=X;
                __delay_ms(50);
                RA2=1; //CLK clock 9
                __delay_ms(150);
                RA2=0; //CLK clock
                __delay_ms(150);

                PORTC=0B00001100;   //A1 data RS=1; SHDN=1; CS=1; SDI=X;
                __delay_ms(50);
                RA2=1; //CLK clock 10
                __delay_ms(150);
                RA2=0; //CLK clock
                __delay_ms(150);

                PORTC=0B00001110;   //FINAL State:
                //Load data RS=1; SHDN=1; CS=1 -> Load data; SDI=X;
                __delay_ms(1);
            //   __delay_ms(10000);//10 s delay
                // state= 2; //Regulation 1.5 V
                state_on=0;
        }
    }
}
```

B.3.4 PIC program for μGrid control circuit

```
#include <stdio.h>
```

```
#include <htc.h>
#include <pic16f684.h>
#include <stdlib.h>
// Initial configuartions
const int ldo_v_min = 340; //316; // 1.543V at Vin(LDO) sensing point
 //(1.5V output; voltage divider)
int i, state_ch, ADC_value ;  //For delay loop and configuration state
// If charging state_ch=1 and when discharging state_ch=0
// PIC16F684 Configuration Bit Settings
__CONFIG(FOSC_INTOSCCLK & WDTE_OFF & PWRTE_OFF &
__MCLRE_ON & CP_OFF & CPD_OFF & BOREN_OFF & IESO_OFF & FCMEN_OFF);

void main(){
  TRISC= 0B00000000; //Define DIRECTION of channels- OUTPUT=0
  ADCON1= 0B00110000; //A/D conversion clock selection bit ,
 //ADCS0= 1 and ADCS1=0 => 2 us FOSC/8
                        // Totla convertion time ~100us
 //---------------------------------------------------------------------
  PORTC= 0B00000000;  //Reset the port - open all the switches
  for(i=0; i<100; i++); // Delay
  TRISA= 0B00000010; //Define DIRECTION of channels- INPUT=1, pin 12
  ANSEL= 0B00000010; //Port configuration - 12(ANS1-AN1) pin as analog,
    //RC0-RC3 digital chanels- pin 12
  ADCON0= 0B10000101; //Right justified, voltage reference =Vdd,
 //conversation stop, Analog channel selection
                         //- 12(ANS1-AN1) pin
 for(i=0; i<100; i++); // Delay for acquisition time 10 us
                      //for CHOLD cap of ADC
 state_ch =1;
 PORTC=0B00001000;//Initially set to charge pin-7=ON, pin-8=ON
 for(i=0; i<750; i++);
while(1)
     {
      //Charging Cycle
           while(state_ch==1)
           {
             GO_nDONE=1;
             while(GO_nDONE);
             ADC_value= 0;
```

```
            ADC_value= ADRESH;
            ADC_value= ADC_value<<8;
            ADC_value= ADC_value | ADRESL;     // copy results
           if (ldo_v_min > ADC_value)
           {
             state_ch =0;
               PORTC=0B00000001;     //set to discharge pin 9=ON, 10=ON
               for(i=0; i<750; i++);// Delay for acquisition time > 10us
                                    //for CHOLD cap of ADC
            }
        }
        //Discharging Cycle
        while (state_ch==0)
        {
            GO_nDONE=1;
            while(GO_nDONE);
            ADC_value= 0;
            ADC_value= ADRESH;
            ADC_value= ADC_value<<8;
            ADC_value= ADC_value | ADRESL;// copy results
           if (ldo_v_min > ADC_value)
           {
 state_ch =1;
      PORTC=0B00001000;//set to charge pin-7=ON, pin-8=ON
      for(i=0; i<750; i++); // Delay for acquisition time > 10
                           //us for CHOLD cap of ADC
           }
      }
    }
}
```

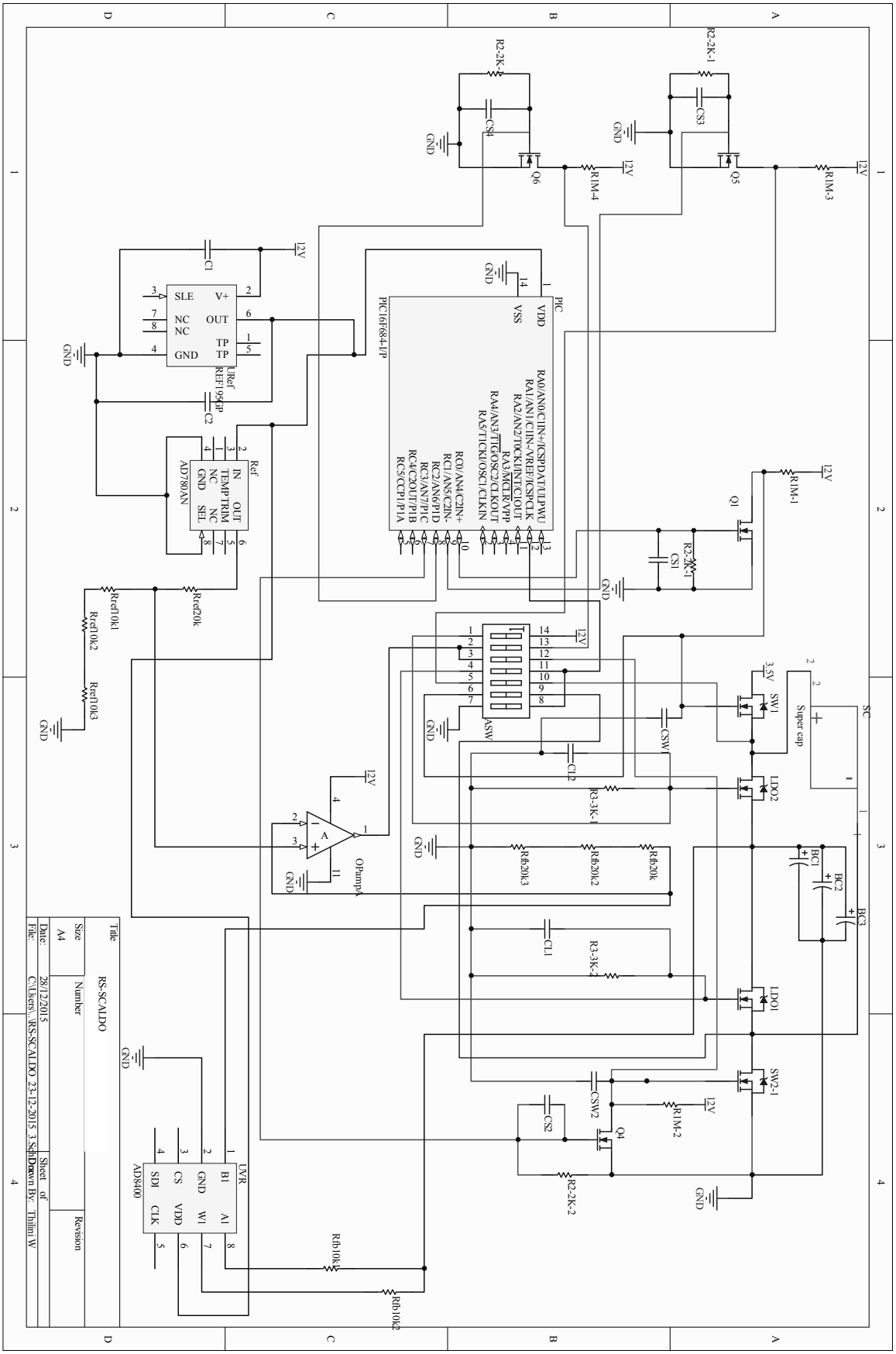
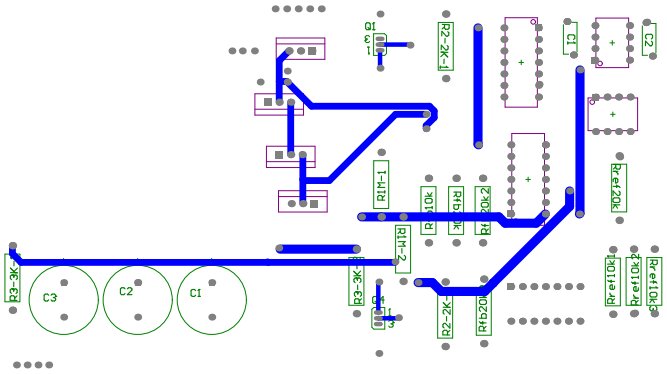
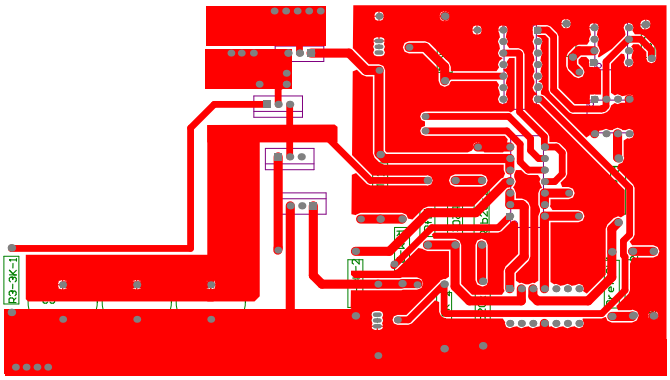


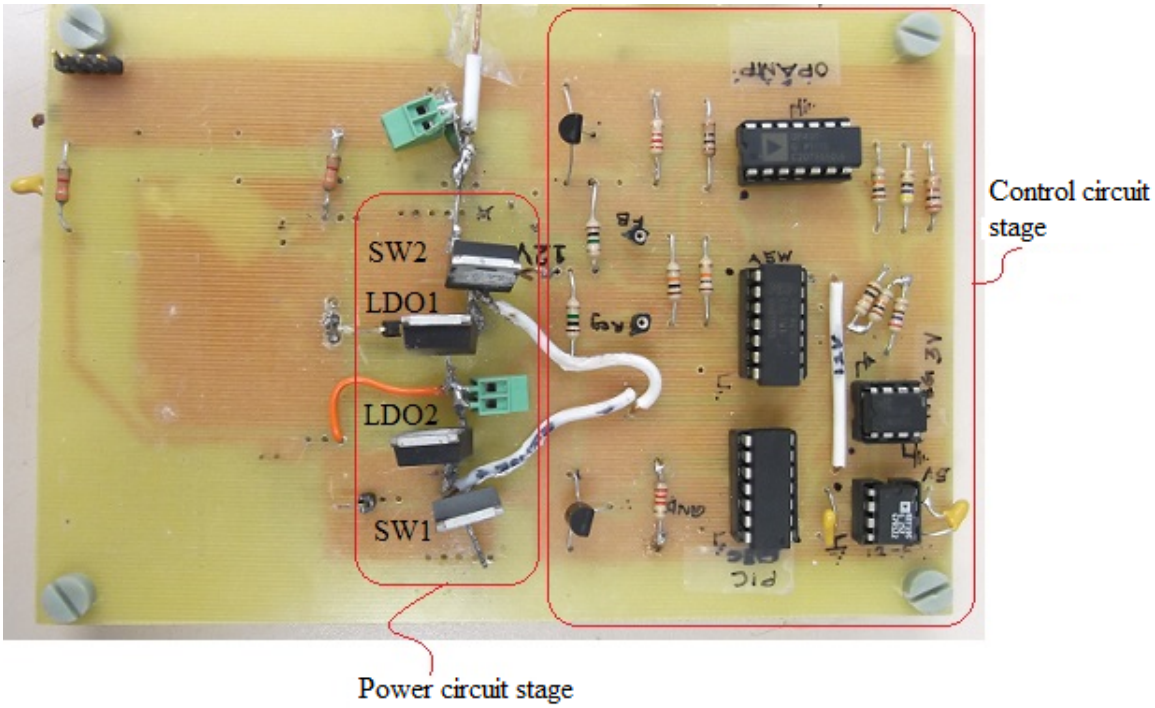
Figure B.7: RS-SCALDO schematic diagram



(a)



(b)



(c)

Figure B.8: PCB layouts of the 3.5-to-1.5 V RS-SCALDO: (a) top layer, (b) bottom layer (c) RS-SCALDO power and control circuit stages

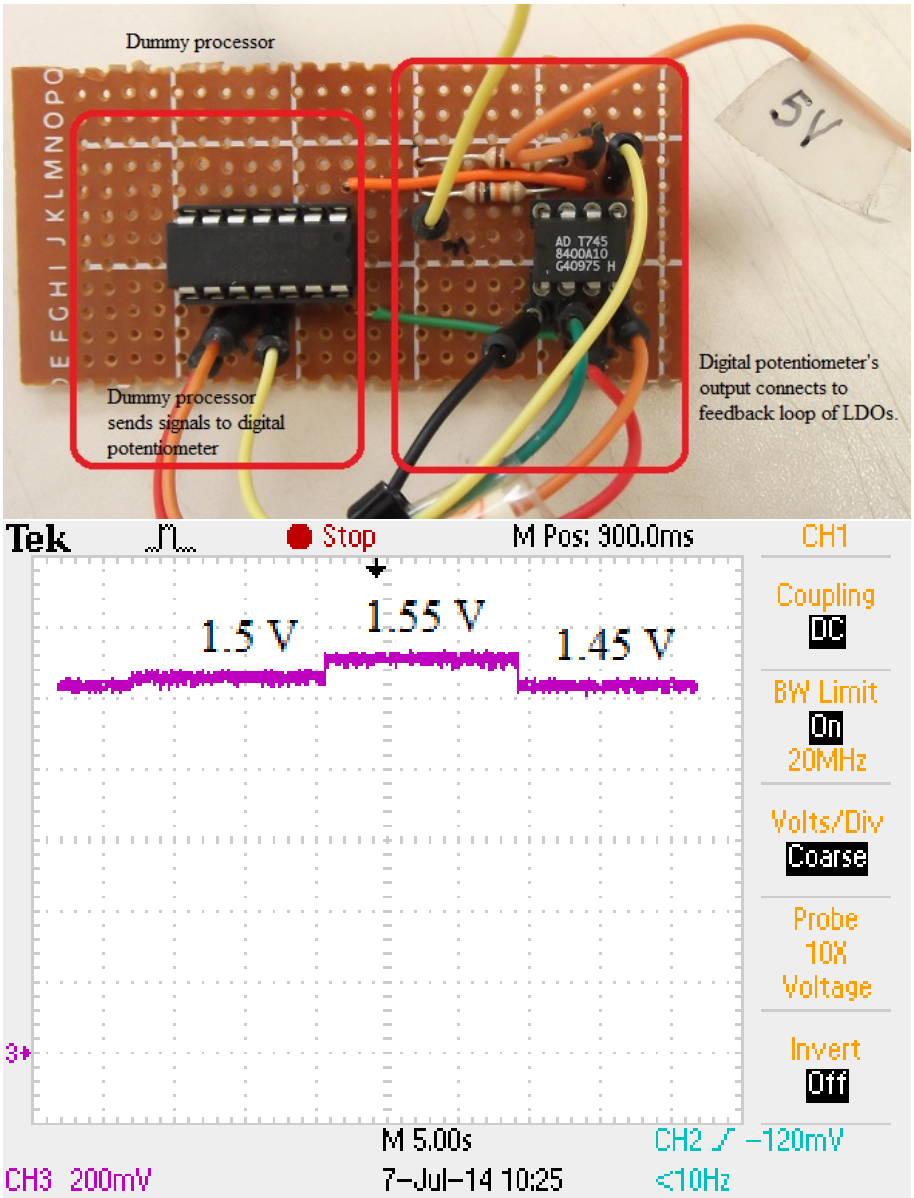
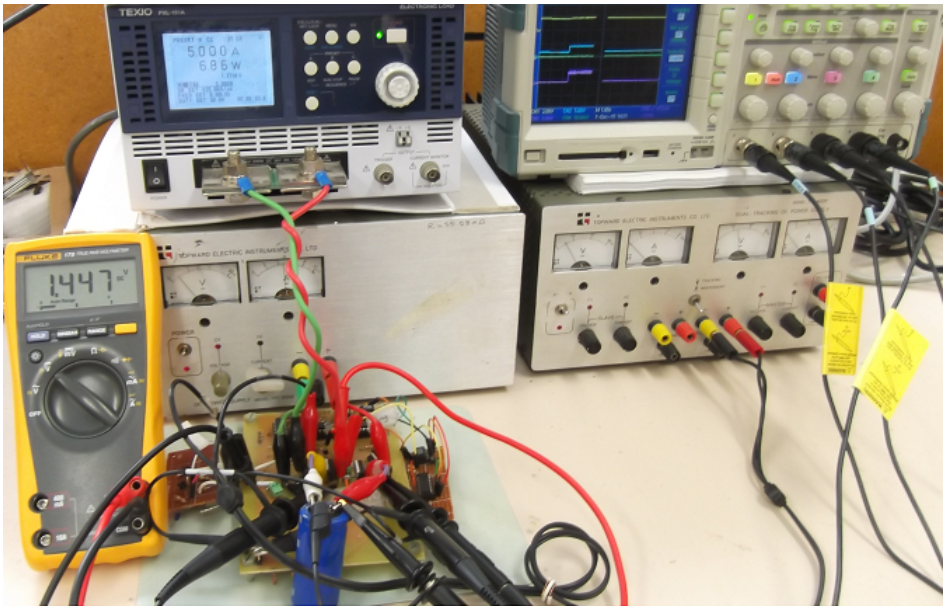
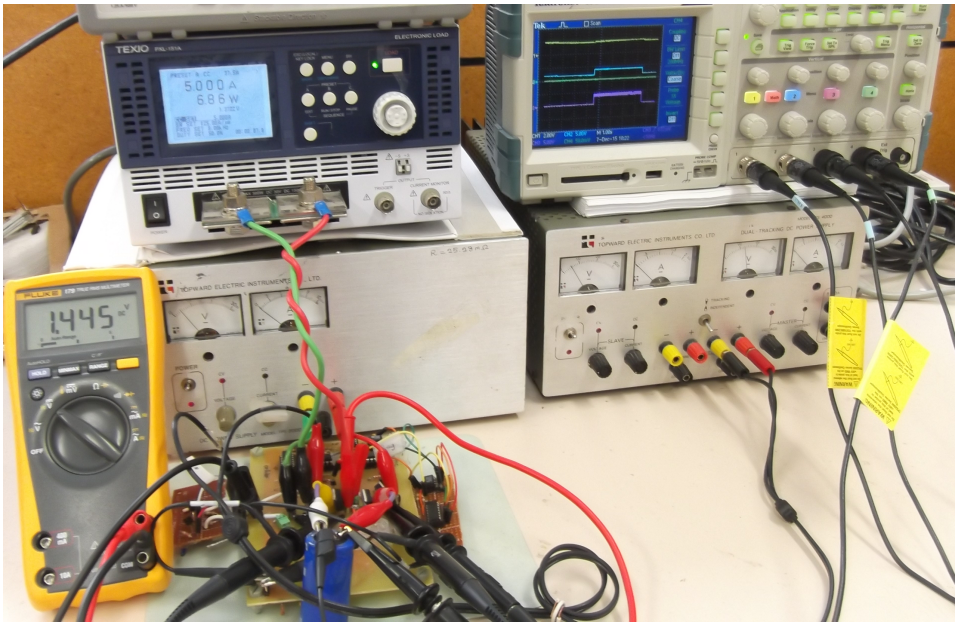


Figure B.9: Prototype of a dummy processor and changing of output voltage



(a)



(b)

Figure B.10: 3.5-to-1.45 V RS-SCALDO test setup: Discharging at full load 5 A

Appendix C

Matlab and SPICE simulations

SPICE AUIRL3705 MOSFET meta model

```
.SUBCKT irl3705z_s_l 1 2 3
**************************************
*      Model Generated by MODPEX     *
*Copyright(c) Symmetry Design Systems*
*         All Rights Reserved        *
*    UNPUBLISHED LICENSED SOFTWARE   *
*   Contains Proprietary Information *
*      Which is The Property of      *
*     SYMMETRY OR ITS LICENSORS      *
*Commercial Use or Resale Restricted *
*   by Symmetry License Agreement    *
**************************************
* Model generated on Jun 14, 04
* MODEL FORMAT: SPICE3
* Symmetry POWER MOS Model (Version 1.0)
* External Node Designations
* Node 1 -> Drain * Node 2 -> Gate * Node 3 -> Source
M1 9 7 8 8 MM L=100u W=100u
.MODEL MM NMOS LEVEL=1 IS=1e-32
+VTO=2.87769 LAMBDA=0.0534823 KP=168.86
+CGSO=2.82959e-05 CGDO=4.47424e-07
RS 8 3 0.00648905
********Body diode**********************
D1 3 1 MD
.MODEL MD D IS=5.37063e-10 RS=0.00217857 N=1.20602 BV=55
+IBV=0.00025 EG=1.2 XTI=3.06218 TT=1e-07
+CJO=1.46699e-09 VJ=0.5 M=0.491263 FC=0.5
**************************************
RDS 3 1 1e+06
```

```
RD 9 1 0.0001
RG 2 7 3.06366
D2 4 5 MD1
* Default values used in MD1:
*   RS=0 EG=1.11 XTI=3.0 TT=0
*   BV=infinite IBV=1mA
.MODEL MD1 D IS=1e-32 N=50
+CJO=8.7595e-10 VJ=0.5 M=0.422718 FC=1e-08
D3 0 5 MD2
* Default values used in MD2:
*   EG=1.11 XTI=3.0 TT=0 CJO=0
*   BV=infinite IBV=1mA
.MODEL MD2 D IS=1e-10 N=0.4 RS=3e-06
RL 5 10 1
FI2 7 9 VFI2 -1
VFI2 4 0 0
EV16 10 0 9 7 1
CAP 11 10 3.0097e-09
FI1 7 9 VFI1 -1
VFI1 11 6 0
RCAP 6 10 1
D4 0 6 MD3
* Default values used in MD3:
*   EG=1.11 XTI=3.0 TT=0 CJO=0
*   RS=0 BV=infinite IBV=1mA
.MODEL MD3 D IS=1e-10 N=0.4
.ENDS irl3705z_s_l

*SPICE Thermal Model Subcircuit
.SUBCKT irl3705z_s_lt 2 0

R_RTHERM1         2 1  0.541285466
R_RTHERM2         1 0  0.598494499
C_CTHERM1         2 0  0.000709422
C_CTHERM2         1 0  0.004641647

.ENDS irl3705z_s_lt
```

C.0.5 SPICE meta modal for diode simulation

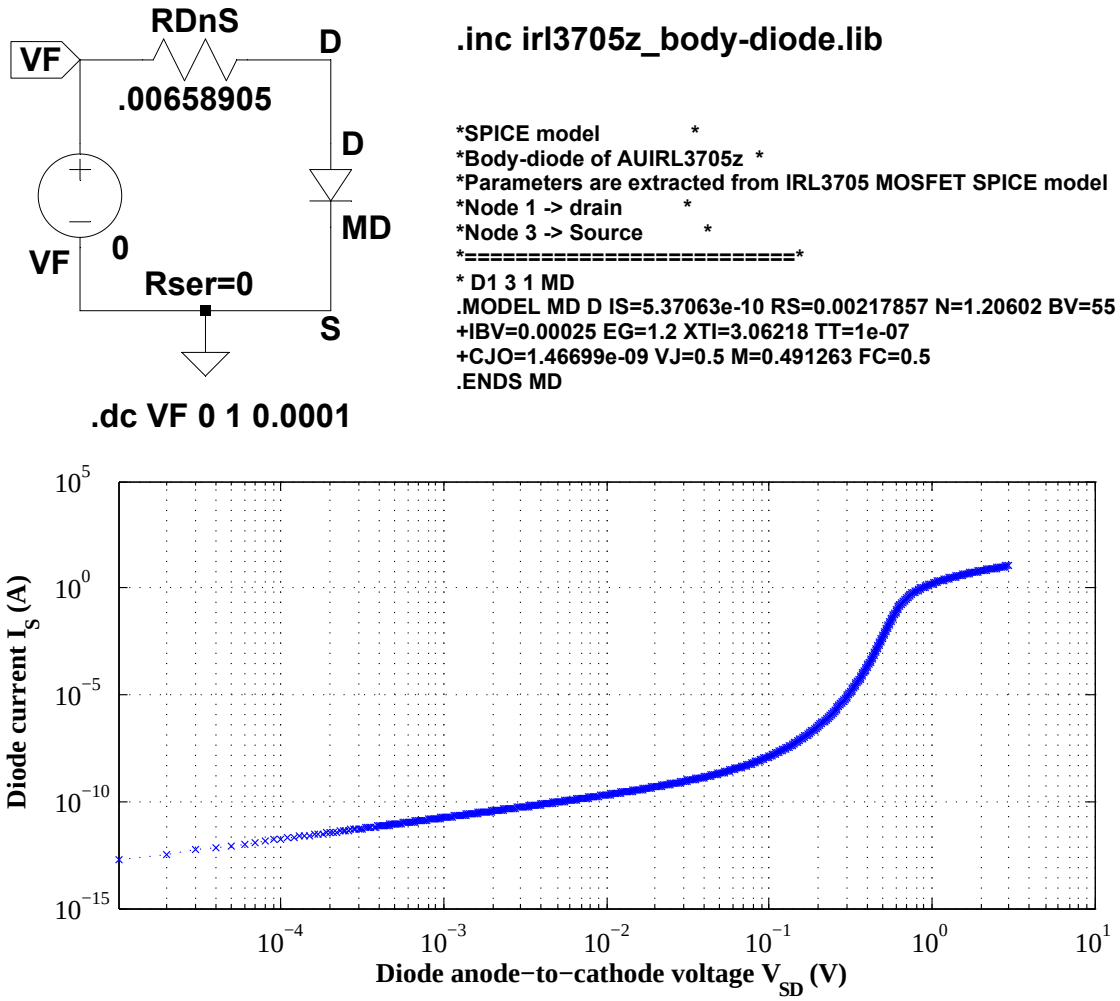


Figure C.1: SPICE circuit to simulate body-diode behaviour

C.0.6 Matlab program for diode simulation

```
% Body-diode of AUIRL3705z
% Diode parameters
% By Thilini Wickramasinghe
IS= 4.8e-13;      % Saturation current 5.37063e-10
RS=0.002178;      % Diode Omic resistance 0.00217857
N=0.931;          % Emission coefficient 1.20602
BV=55;            % Reverse reakdown voltage
IBV=0.00025;      % Reverse reakdown current
EG= 1.2;          % Energy gap
GMIN=1e-12;       % Shunt conductance
XTI=3.06218;      % IS temperature exponent
```

```
TT=1e-07;        % Forward trasit time
CJO=1.46699e-09; % Reverse reakdown
VJ=0.5;          % Contact potential
M=0.491263;      % Junction capacitance grading exponent
FC=0.5;          % Reverse reakdown
RDnS=0.00658905; % Contact resistace 0.00658905
k=1.3800e-023;   % Boltzmann constant
q=1.60218e-019;  % Charge of electron
T=(273.15+23.5); % Temperature
% Variables

Vd_min=0; Vd_max=.7;scale1=0.001;
VS=Vd_min; VD=Vd_max;
n=(Vd_max - Vd_min)/scale1;
% Diode parameters
Vt=(k*T)/q;      % Thermal voltage
L_max=(-5*N*Vt);
L_min= -BV;

% This program is developed on the SPICE discrete diode model defined
% by Howard T. Russell
% 1.) Minimum & maximum voltage > L_max
if Vd_min>= L_max && Vd_max > L_max
   Vd1=Vd_min:scale1:Vd_max;
   Id1 =IS*(exp(Vd1./(N*Vt))-1) + (Vd1.*GMIN);
   VF1 = Id1.*(RDnS+RS) + Vd1;

    axis xy; axis tight;
    FS=14;
    xlabel('Voltage (V)', 'fontsize', FS);
    ylabel('Current (A)', 'fontsize', FS);
    %title('Diode curves','fontsize',  FS);
    plot(VF1, Id1, Vd1,Id1)
end

% 2.)L_max > Minimum voltage  &  Maximum voltage > L_min
if Vd_min >= L_min && Vd_max <= L_max
   Vd1=Vd_min:scale1:Vd_max;
   Id1 =Vd1./Vd1.*(-IBV);
```

```
   VF1 =Id1.*(RDnS+RS) + Vd1;

    axis xy; axis tight;
    FS=14;
    xlabel('Voltage (V)', 'fontsize', FS);
    ylabel('Current (A)', 'fontsize', FS);
   % title('Diode curves','fontsize',  FS);
   plot(VF1, Id1, Vd1,Id1)
end

% 3.)Maximum voltage < L_min
if Vd_max < L_min
   Vd1=Vd_min:scale1:Vd_max;
   Id1 =-IS + (Vd1.*GMIN);
   VF1 =Id1.*(RDnS+RS) + Vd1;
   axis xy; axis tight;
   FS=14;
   xlabel('Voltage (V)', 'fontsize', FS);
   ylabel('Current (A)', 'fontsize', FS);
   %title('Diode curves', 'fontsize', FS);
   plot(VF1, Id1, Vd1,Id1)
end

% 4.)Minimum voltage> L_min & Maximum voltage > L_max
if Vd_min>= L_min && Vd_max > L_max
   Vd1=Vd_min:scale1:L_max;
   Id1 =Vd1./Vd1.*(-IBV);
   VF1 = Id1.*(RDnS+RS) + Vd1;

   Vd2=L_max:scale1:Vd_max;
   Id2 =IS*(exp(Vd2./(N*Vt))-1) + (Vd2.*GMIN);
   VF2 = Id2.*(RDnS+RS) + Vd2;
   axis xy; axis tight;
   FS=14;
   xlabel('Voltage (V)', 'fontsize', FS);
   ylabel('Current (A)', 'fontsize', FS);
   %title('Diode curves','fontsize',  FS);
   plot(VF1, Id1, Vd1,Id1,VF2, Id2, Vd2,Id2)
end
```

```
% 5.)Minimum voltage <= L_min & Maximum voltage < L_min
if Vd_min<= L_min && Vd_max < L_max
   Vd0=Vd_min:scale1:L_min;
   Id0 =-IS + (Vd0.*GMIN);
   VF0 = Id0.*(RDnS+RS) + Vd0;

   Vd1=L_min:scale1:Vd_max;
   Id1 =Vd1./Vd1.*(-IBV);
   VF1 = Id1.*(RDnS+RS) + Vd1;
   axis xy; axis tight;
   FS=14;
   xlabel('Voltage (V)', 'fontsize', FS);
   ylabel('Current (A)', 'fontsize', FS);
   %title('Diode curves','fontsize',  FS);
   plot(VF0, Id0, Vd0,Id0, VF1, Id1, Vd1,Id1)
end

% 6.)Minimum voltage < L_min & Maximum voltage > L_min
if Vd_min< L_min && Vd_max > L_max
   Vd0=Vd_min:scale1:L_min;
   Id0 =-IS + (Vd0.*GMIN);
   VF0 = Id0.*(RDnS+RS) + Vd0;

   Vd1=L_min:scale1:L_max;
   Id1 =Vd1./Vd1.*(-IBV);
   VF1 = Id1.*(RDnS+RS) + Vd1;

   Vd2=L_max:scale1:Vd_max;
   Id2 =IS*(exp(Vd2./(N*Vt))-1) + (Vd2.*GMIN);
   VF2 = Id2.*(RDnS+RS) + Vd2;

   axis xy; axis tight;
   FS=14;
   xlabel('Voltage (V)', 'fontsize', FS);
   ylabel('Current (A)', 'fontsize', FS);
%title('Diode curves','fontsize', FS);
   plot(VF0, Id0, Vd0,Id0, VF1, Id1, Vd1,Id1,VF2, Id2, Vd2,Id2)
end
```

C.0.7 SPICE simulation

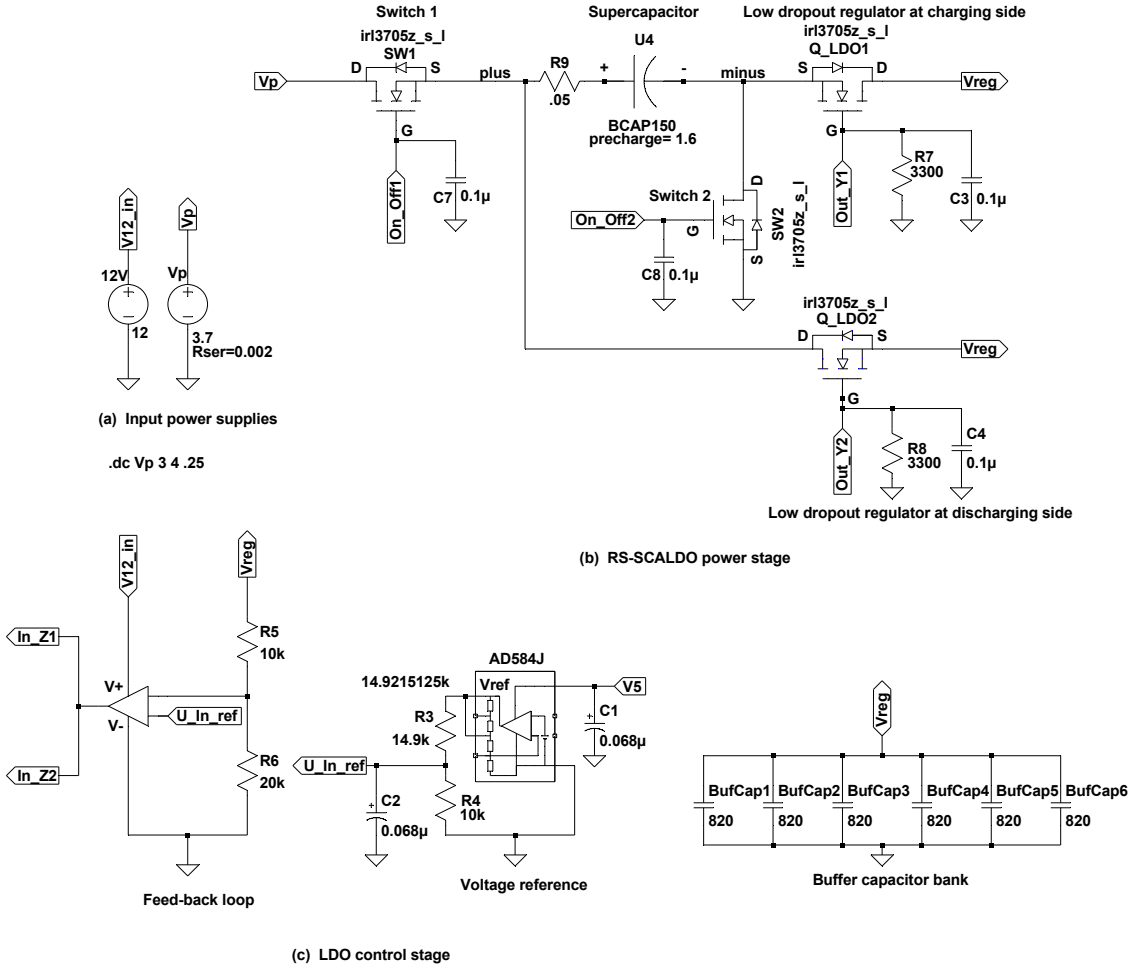
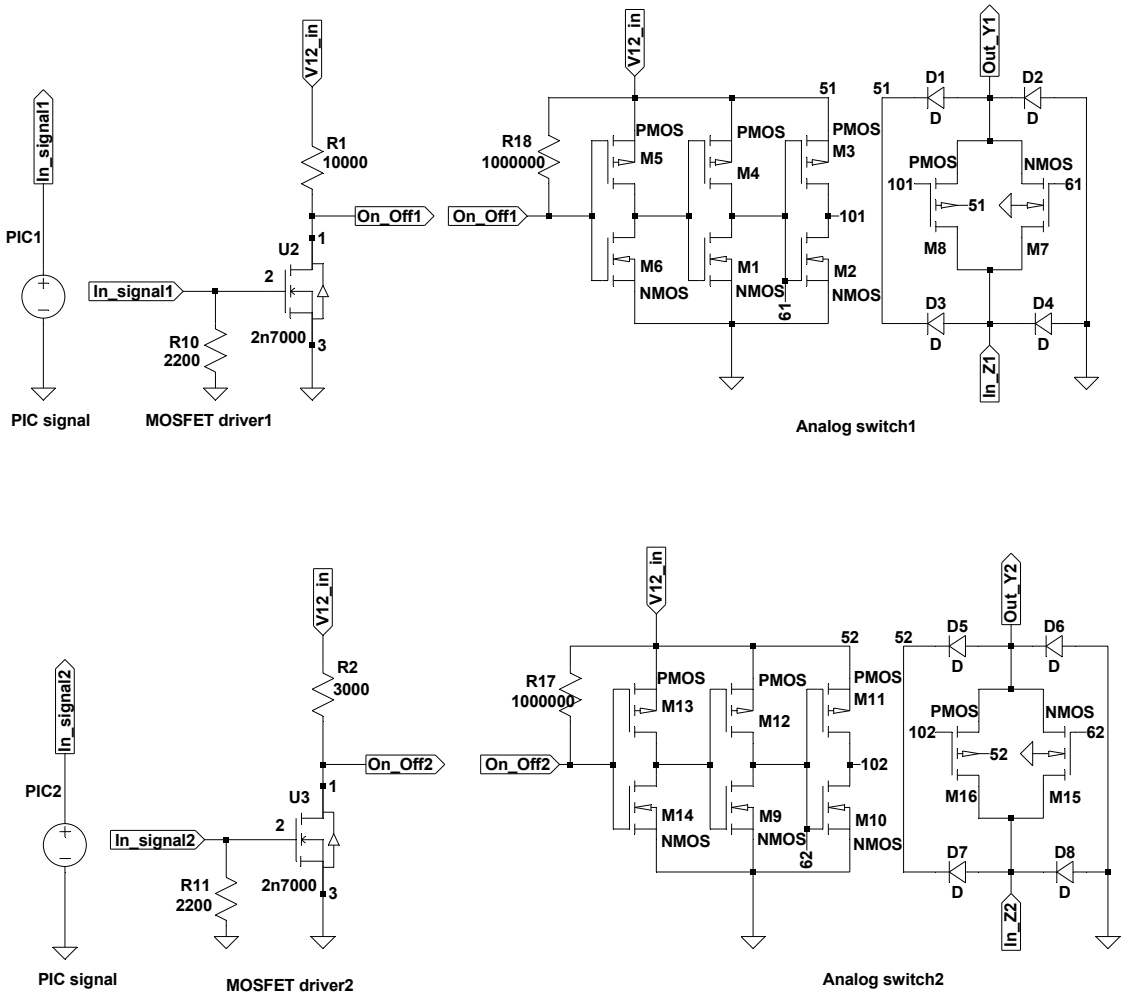


Figure C.2: SPICE simulation: power circuit and feedback loop of RS-SCALDO



PWL(0 5 12s 5 12.0002s 0 21.9s 0 21.900001s 5 31.8s 5 31.8002s 0 41.7s 0)

PWL(0 0 12s 0 12.000001s 5 21.9s 5 21.9002s 0 31.8s 0 31.800001s 5 41.7s 5)

Figure C.3: SPICE simulation: analog switches of RS-SCALDO

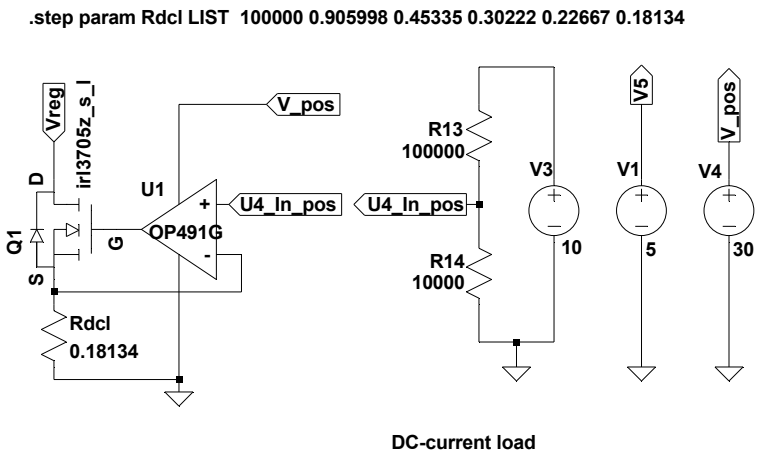
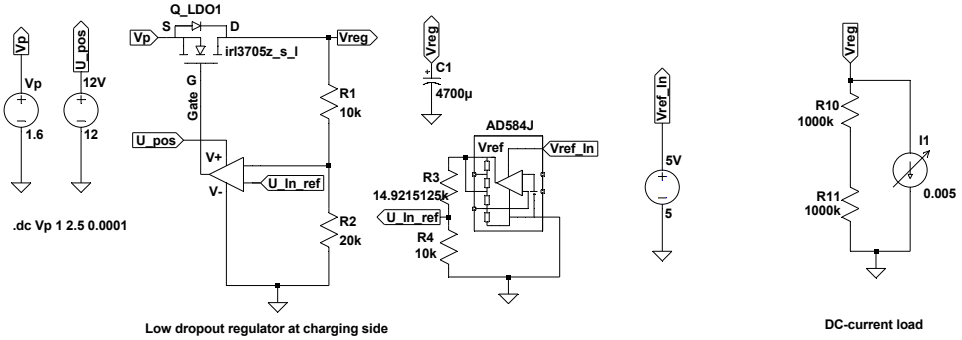
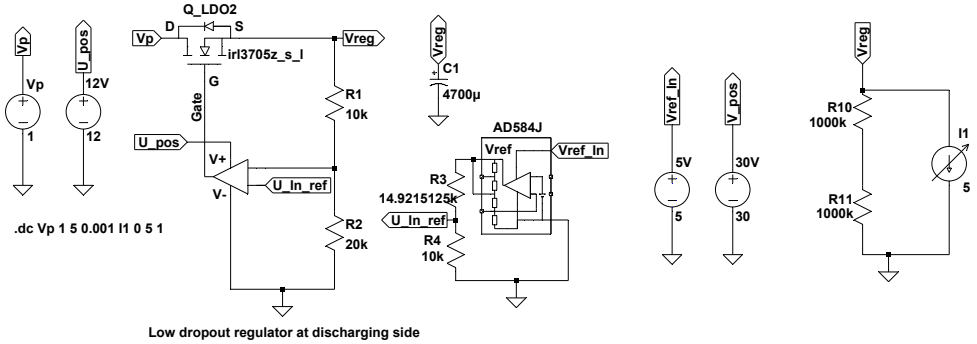


Figure C.4: Simplified simulation of DC-load




```
* C:\Users\tcpkw1\Desktop\WRITING\SIMULATION\LTSPICE\LDO_1\LDO1_IRL3705Z_30102015.asc
V§5V Vref_In 0 5
XQ_LDO1 Vreg Gate Vp irl3705z_s_l
XOpAmp U_In_ref N002 U_pos 0 Gate OP491
XVref N001 NC_01 N001 0 NC_02 NC_03 NC_04 Vref_In AD584J
R1 Vreg N002 10k
R2 N002 0 20k
R3 N001 U_In_ref 14.9215125k
R4 U_In_ref 0 10k
V§12V U_pos 0 12
Vp Vp 0 1.6
R10 Vreg N003 1000k
R11 N003 0 1000k
C1 Vreg 0 4700µ V=10 Irms=1.55 Rser=0.06 Lser=0 mfg="Nichicon" pn="UPG1A472MRH" type="Al electrolytic"
I1 Vreg 0 0.005
.dc Vp 1 2.5 0.0001
* Low dropout regulator at charging side
* DC-current load
.lib C:\Program Files\LTC\LTspiceIV\Experimets\irl3705z_s_l.spi
.lib C:\Users\tcpkw1\Desktop\WRITING\SIMULATION\ad584j.cir
.lib C:\Users\tcpkw1\Desktop\WRITING\SIMULATION\op491.cir
.backanno
.end
```




```
* C:\Users\tcpkw1\Desktop\WRITING\SIMULATION\LTSPICE\LDO_2\LDO2_IRL3705Z_30102015.asc
V§5V Vref_In 0 5
XQ_LDO2 Vp Gate Vreg irl3705z_s_l
XOpAmp U_In_ref N002 U_pos 0 Gate OP491
XVref N001 NC_01 N001 0 NC_02 NC_03 NC_04 Vref_In AD584J
R1 Vreg N002 10k
R2 N002 0 20k
R3 N001 U_In_ref 14.9215125k
R4 U_In_ref 0 10k
V§12V U_pos 0 12
Vp Vp 0 1
V§30V V_pos 0 30
R10 Vreg N003 1000k
R11 N003 0 1000k
C1 Vreg 0 4700µ V=10 Irms=1.55 Rser=0.06 Lser=0 mfg="Nichicon" pn="UPG1A472MRH" type="Al electrolytic"
I1 Vreg 0 5
.dc Vp 1 5 0.001 I1 0 5 1
* Low dropout regulator at discharging side
.lib C:\Program Files\LTC\LTspiceIV\Experimets\irl3705z_s_l.spi
.lib C:\Users\tcpkw1\Desktop\WRITING\SIMULATION\ad584j.cir
.lib C:\Users\tcpkw1\Desktop\WRITING\SIMULATION\op491.cir
.backanno
.end
```

Figure C.5: SPICE simulation of LDO1 and LDO2

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