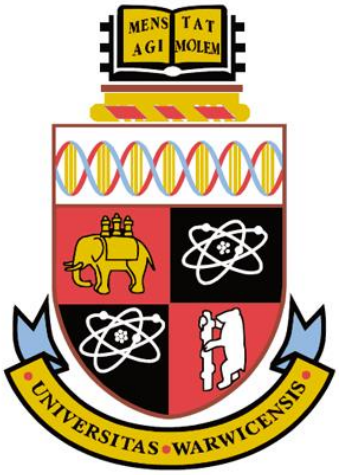
Finite Element Electrothermal Modelling and Characterization of Single and Parallel Connected Power Devices



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A thesis Submitted to the University of Warwick

in partial fulfilment of the requirements for the degree of

Doctor of Philosophy

School of Engineering

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Ji Hu

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Declaration

This thesis is submitted in partial fulfilment for the degree of Doctor of Philosophy under the regulations formulated by the School of Engineering of the University of Warwick. I herewith declare that this thesis contains my own research performed under the supervision of Dr. Olayiwola Alatise and Prof. Li Ran, without assistance of third parties, unless stated otherwise. The research materials have not been submitted in any previous application for a degree at any other university. All sources of information are specifically acknowledged in the content. The work presented in Chapter 2 has been partly published in J3, J4 and C5. Majority of the work presented in Chapter 3 has been published in C2 and C3. The work presented in Chapter 4 has been published in J2 and C7. The work presented in Chapter 5 has been published in J1, C1 and J2.

List of Publications

This section presents the complete list of 1st and co-authored published journal and conference papers by Ji Hu. The 1st author papers result directly from the work presented here.

J1. **J. Hu**, O. Alatise, J. A. O. González, R. Bonyadi, L. Ran and P. Mawby, "The Effect of Electrothermal Nonuniformities on Parallel Connected SiC Power Devices Under Unclamped and Clamped Inductive Switching," *IEEE Trans. Power Electron.*, vol. 31, pp. 4526-4535, 2016.

J2 **J. Hu**, O. Alatise, J. A. O. González, R. Bonyadi, P.Alexakis, L. Ran and P. Mawby, "Robustness and Balancing of Parallel-Connected Power Devices: SiC Versus CoolMOS," *IEEE Trans. Ind. Electron.*, vol. 63, pp. 2092-2102, 2016.

C1 **J. Hu**, O. Alatise, J. A. O. González, P.Alexakis, L. Ran and P. Mawby, "Finite element modelling and experimental characterisation of paralleled SiC MOSFET failure under avalanche mode conduction," *Power Electronics and Applications (EPE'15 ECCE-Europe), 2015 17th European Conference on, 2015,* pp. 1-9.

C2 **J. Hu**, O. Alatise, J. A. O. González, L. Ran and P. Mawby, "Avalanche Ruggedness of Parallel Connected Diodes: SiC Schottky Diodes vs Silicon PiN Diodes," submitted to *Power Electronics, Machines and Drives (PEMD), the 8th IET International conference on*, accepted 9th Mar. 2016.

C3 **J. Hu**, O. Alatise, J. A. O. González, L. Ran and P. Mawby, "Comparative Electrothermal Analysis between SiC Schottky and Silicon PiN Diodes: Paralleling and Thermal Considerations," submitted to *Power Electronics and Applications (EPE'16 ECCE-Europe), 2016 18th European Conference on,* accepted on 1th Mar. 2016.

J3 R. Bonyadi, O. Alatise, S. Jahdi, **J. Hu**, J. A. O. González, L. Ran and P. Mawby, "Compact Electrothermal Reliability Modeling and Experimental Characterization of Bipolar Latchup in SiC and CoolMOS Power MOSFETs," *IEEE Trans. Power Electron.*, vol. 30, pp. 6978-6992, 2015.

J4 P. Alexakis, O. Alatise, **J. Hu**, S. Jahdi, L. Ran, P. Mawby, "Improved Electrothermal Ruggedness in SiC MOSFETs Compared With Silicon IGBTs," *IEEE Trans. Electron Devices*, vol. 61, pp. 2278-2286, 2014.

C4 P. Alexakis, O. Alatise, **J. Hu**, S. Jahdi, J. A. O. González, L. Ran and P. Mawby., "Analysis of power device failure under avalanche mode Conduction," in *Power Electronics and ECCE Asia (ICPE-ECCE Asia), 2015 9th International Conference on*, 2015, pp. 1833-1839.

C5 R. Bonyadi, O. Alatise, S. Jahdi, **J. Hu**, L. Evans, and P. A. Mawby, "Investigating the reliability of SiC MOSFET body diodes using Fourier series modelling," in Energy Conversion Congress and Exposition (ECCE), 2014 IEEE, 2014, pp. 443-448.

C6 J. A. O. González, O. Alatise, N. Nobeen, **J. Hu**, L. Ran and P.Mawby, "Electrothermal Considerations for Power Cycling in SiC Technologies," in *Integrated Power Electronics Systems (CIPS), 2016 8th International Conference on*, 2016, pp. 1-7.

C7 R. Bonyadi, O. Alatise, **J. Hu**, Z. Davletzhanova, J. A. O. González, L. Ran and P.Mawby, "Compact Temperature Dependent Physics-Based IGBT Model for Parallel IGBTs in Clamped Inductive Switching Circuit," in *Applied Power Electronics Conference and Exposition (APEC), 2016 IEEE*, 2016.

C8 J. A. O. González, O. Alatise, **J. Hu**, L. Ran and P. Mawby, "Temperature Sensitive Electrical Parameters for Condition Monitoring in SiC Power MOSFETs," submitted to *Power Electronics, Machines and Drives (PEMD), the 8th IET International conference on*, accepted 9th Mar. 2016.

C9 Y. Bonyadi, P. Gammon, R. Bonyadi, O. Alatise, **J. Hu**, V. Shah and P. Mawby, "The Impact of Triangular Defects on Electrical Characteristics and Switching Performance of 4H-SiC PiN Diodes," submitted to *the 8th Annual IEEE Energy Conversion Congress & Exposition (ECCE 2016).*

Abstract

Power modules typically comprise of several power devices connected in parallel for the purpose of delivering high current capability. This is especially the case in SiC where small active area and low current MOSFETs are the only option due to defect density control and yield issues in the epitaxial growth of SiC wafers. Electrothermal variations between parallel connected devices can emerge from manufacturing variability, non-uniform degradation rates, variation in gate driving just to mention a few. The impact of electrothermal variation between parallel-connected devices as a function of device technology is thus important to consider especially since failure of the power module requires only failure in a single device. Furthermore, the impact of these electrothermal variations in parallel-connected devices on the total electrothermal ruggedness of the power module under anomalous switching conditions like unclamped inductive switching is important to consider for the different device technologies. In this thesis, the impact of initial junction temperature variation, switching rates and thermal boundary conditions between parallel-connected diodes have been evaluated for SiC Schottky and silicon PiN diodes under clamped and unclamped inductive switching. Finite element simulations have been used to support the experimental measurements. Similar studies have been performed in CoolMOS super-junction MOSFETs, silicon IGBTs and SiC power MOSFETs. New insights regarding the failure of parallel connected devices under unclamped inductive switching have been revealed from the models and measurements. Overall, the thesis makes a major contribution in the understanding of the electrothermal performance of parallel connected devices for different transistor and diode technologies.

Abbreviations

N_D	background doping concentration
p	Hole concentration
τ_{HL}	Ambipolar carrier lifetime
D	Ambipolar diffusivity
$D_{n(p)}$	Diffusivity for electrons (holes).
$\mu_{n(p)}$	Carrier mobility for electrons (holes).
w_d	Drift region width
n_i	Intrinsic carrier concentration
A_R	Effective Richardson's constant
T	Absolute temperature in Kelvin.
V_{FS}	Bias voltage
Φ_{BN}	Schottky barrier height
k	The Boltzmann's constant
J_s	Saturation current density
R_{CONT}	Schottky contact resistance
R_{SUB}	The resistance in the substrate
R_D	The resistance of the drift region
t_{OX}	Thickness of the gate oxide
ε_{OX}	The oxide dielectric constant
ε_s	Semiconductor dielectric constant
N_A	Doping concentration in the p-base region
n_i	Intrinsic carrier concentration
L_{CH}	Channel length
W_{cell}	Cell pitch width
μ_{ni}	Inversion layer mobility
C_{OX}	Specific capacitance of gate oxide
x_{JP}	The P-base junction depth
μ_{nJ}	The bulk mobility appropriate to the doping level of the JFET region
N_{DJ}	Doping concentration in the JFET region
W_0	Zero-bias depletion width for the JFET region
W_G	Gate width
ρ_D	Resistivity of the drift region
a	JFET region width
x_{PL}	Overlap length of gate oxide and p-body region
t_{IEOX}	Oxide thickness between the gate and the source metal
J_C	Total current flow
W_N	Width of the lightly doped N-drift region
W_{ON}	The depletion width

L_a	Ambipolar diffusion length
λ_{th}	Specific heat conductance
c	Thermal capacitance
ρ	The density of material
x	The coordinate distance in the direction of heat transfer
$G_{n(p)}$	Generation rates for electrons (holes)
R_n	Recombination rates for electrons (holes)
T_L	Lattice temperature
ε	Local permittivity
ψ	Electrostatic potential
E_G	Bandgap energy
N_C	Effective density of state in the conduction band
ρ_L	Local space charge density
N_V	Effective density of state in the valence band
U	Recombination rate
E_t	Trapping energy level
$C_{A\Delta n}$	High-level injection Auger coefficient
V_{bi}	The built-in potential
E_{FC}	Fermi level position in the semiconductor
E_C	Conduction band of semiconductor

Chapter 1.

INTRODUCTION

1.1 Background

Power electronics has enabled the more efficient and flexible use of electricity. This has been of benefit to all levels of power conversion ranging from a few watts in low voltage hand-held electronic devices, to several kilowatts in medium voltage electric drivetrains for electric vehicles and several giga watts in grid connected converters used in applications like high voltage direct current (HVDC) converters and flexible AC transmission systems (FACTS) [1-8].

The increased electrification of heat and transportation coupled with the need to reduce the reliance on fossil fuels so as to mitigate global warming has made power efficiency and power electronics a very critical technology. Traditional coal and gas based power stations are well known for their significant contributions to global warming, hence, there has been a proliferation of alternate sources of renewable energy including solar and wind energy conversion systems [9-11]. Connecting these renewable sources of energy to the power grid requires power electronics to convert a variable voltage variable frequency AC source to a fixed frequency fixed voltage rating AC delivered to the grid

in the case of wind energy conversion systems. Older HVDC systems were based on thyristor technologies implemented as line commutated current source converters, however, newer HVDC systems use self-commutated voltage source converters based on IGBT technology [12-14]. In the case of solar power, a grid tie inverter is required to convert the DC power generated by the solar cells into single or 3 phase AC power for grid connection. Furthermore, for long distance power transmission over land or connection of off-shore wind-farms, HVDC is preferred technology [15, 16]. Power electronic converters are also useful for connecting asynchronous power systems or even power systems operating at different frequencies.

Power electronic converters are also the core technology behind the electrification of vehicle transportation [17]. Traditional internal combustion engines are a key contributor to greenhouse gas emissions; hence, the drive towards electric vehicles is important to mitigate climate change. The 2 level 3 phase voltage source converter is required in electric vehicles for converting the DC electrochemical power stored in the lithium ion battery to a controllable 3 phase AC voltage for controlling the electrical machine used for traction [18, 19]. The bi-directional capability of voltage source converters means that power generating from regenerative breaking can be transferred back to the battery. The converter is used to control the speed and torque of the machine through modulation [20]. Power electronic converters are also critical in electric rail transportation where AC machines are driven and controlled by converters [21]. The power rating of these converters are typically higher than electric vehicle converters since greater torque is required. Medium voltage electric drives comprising of back-to-back 2 level 3 phase voltage source converters are also used in ship propulsion [22]. To improve the efficiency and reduce the carbon emissions of shipping, electric drivetrains are increasingly being used in large ships [23]. Here, the diesel or gas turbine powered engine

initially used for direct propulsion is instead used to power a generator which supplies electric power to an electrical motor through a back-to-back power electronic converter. With increased efficiency and controllability of the electrical motor, energy consumption can be significantly reduced. Power electronics is also critical in the drive for increased electrification of aircraft. This is called the More-Electric-Aircraft (MEA) where functions initially implemented by pneumatic and hydraulic power are increasingly being replaced with electric power [24, 25]. As aircrafts move towards higher degrees of electrification, power electronic controllers, breakers and converters will be required for connecting loads and increasing controllability of the power system.

At the heart of power electronic converters, are the power semiconductor devices that control power flow to the load through energy storage components like inductors and capacitors. Power semiconductors act as switches in this manner. Ideally, power semiconductor devices should have zero on-state loss, zero off-state loss and instantaneous switching speed, however, this is not possible. The devices have conduction losses due to series resistances, blocking losses due to leakage current and finite switching speeds due to parasitic resistances, inductances and capacitances. Power semiconductor devices can be 2 terminal devices like diodes or 3 terminal devices like transistors and thyristors. Diodes are passive elements that rectify by conducting in one direction while blocking in the opposite direction. Transistors are switches that can be controlled either by current as is the case in a BJT or a voltage as is the case in an FET. While the other three terminal devices like thyristors are semi-controllable in the sense that they can be turned ON but not turned OFF [26, 27]. Power semiconductor devices can also be unipolar devices meaning that carrier flow is due to a majority carrier or they can be bipolar meaning that carrier flow is due to both majority and minority carriers [26, 28]. Unipolar devices include MOSFETs and Schottky diodes while bipolar devices include

Thyristors, IGBTs, BJTs and PiN diodes. Power devices can also be classified according to the semiconductors used to fabricate them. Historically, power devices have been exclusively silicon based, however, now there are wide bandgap devices based on silicon carbide and gallium nitride [29, 30].

It is generally well recognised that high power applications use low switching frequencies while low power applications use high switching frequencies [31-33]. For example, a switch mode power supply used for connecting a laptop to the mains can run at switching frequencies in megahertz, while the kilowatt rated converter used in an electric vehicle will run at a few kHz and the megawatt rated converter used in a modular multi-level HVDC converter will run at grid frequency (50 Hz or 60 Hz). Hence, high power low speed applications are usually implemented by thyristors, while low voltage high speed applications are implemented by discrete power MOSFETs. IGBTs have become popular for medium voltage medium frequency applications [34]. Thyristors with voltage ratings as high as 8 kV and current ratings as high as 4 kA are available as phase controlled thyristors and as typically deployed to line commutated current source converters for multi-gigawatt HVDC systems [33, 35, 36]. However, wide bandgap materials like SiC have pushed MOSFETs into the medium voltage arena. Thanks to SiC, 1.2 kV and 1.7 kV power MOSFETs and diodes are now available in TO-247 packages and as power modules. SiC MOSFETs with breakdown voltages as high as 10 kV and even 15 kV have been demonstrated by Wolfspeed (formerly CREE) [37, 38]. Gallium nitride is another wide bandgap semiconductor, however, due to processing issues and the lack of availability of a bulk GaN substrate, GaN devices are limited in scope and application.

1.2 A Brief History of Power Electronics

Solid state power electronic devices were first proposed as a point contact germanium transistor by Bardeen and Brattain in 1947 [39, 40]. The bipolar junction transistor (BJT), which was formed as a variable resistance with a third terminal to control the current flow, was proposed by Shockley [41]. Eventually, such solid state devices were developed and fabricated in silicon for low cost, hence, vacuum tubes were replaced to improve the cost performance balance. In the 1950s, power conversion performed by semiconductor switching devices became a reality. In 1956, the silicon controlled rectifier (SCR) was introduced by General Electric [42-44]. In the same year, the thyristor became commercially available. These greatly increased the range of power electronic applications. In 1976, the vertical power Metal-Oxide-semiconductor field effect transistor (MOSFET) became commercially available. Due to the insulating gate and increased controllability, it was an improvement over BJTs. In 1979, the Insulated Gate Bipolar Transistor (IGBT) was introduced as a hybrid between a MOSFET and a BJT. It has a MOS input and a bipolar output, thus taking advantages of the ease of controllability of the MOSFET and the current density capability of the BJT. In 1999, the super-junction MOSFET became commercially available. This improved the conduction loss performance of the MOSFET by using the concept of charge balance from alternating p and n columns to reduce the drift layer thickness. More recent research interest has been paid to the wide band gap material silicon carbide as it shows superb performance in fabricating high power devices than the silicon. Table 1-1 shows the comparison of fundamental property between silicon and SiC. In 2011, the very first SiC power MOSFET became commercially available by CREE although the Schottky barrier diode was first released in 2002. The Schottky diode exhibited significantly reduced switching losses compared to the PiN diode due to its unipolar nature, hence, no stored charge and

no reverse recovery current. Today SiC power MOSFET devices and modules are commercially available from CREE and ROHM. GE also make SiC MOSFETs although they are not commercially available likewise Mitsubishi. Low current SiC thyristors are also available from GeneSiC. It is envisaged that over the coming years, the power handling capability of SiC modules will increase and the cost will decrease, however, this will be driven by market forces. Nevertheless, there are still significant technology barriers impeding the realisation of low cost SiC wafers and devices. Stacking faults, basal plane defects and other crystalline defects associated with SiC limit the wafer yield and the reduced epitaxial growth rate limits the wafer-line production throughput.

Properties	Silicon	4H-SiC
Energy Band Gap (eV)	1.11	3.26
Electron Affinity (eV)	4.05	3.7
Relative Dielectric Constant	11.7	9.7
Thermal Conductivity ($W/cm \cdot K^{-1}$)	1.5	3.7
Density of States Conduction Band (cm^{-3})	2.8×10^{19}	1.23×10^{19}
Density of States Valence Band (cm^{-3})	1.04×10^{19}	4.58×10^{18}

Table 1-1: Fundamental material properties.

1.3 Research Objectives and Contribution

This thesis focusses on the finite element modelling and experimental characterisation of different power semiconductor devices ranging from silicon PiN diodes, to SiC Schottky diodes, silicon IGBTs, CoolMOS super-junction MOSFETs and SiC power MOSFETs. The electrothermal characteristics of these devices under clamped and unclamped inductive switching conditions have been considered both as single devices and as parallel-connected devices. When power devices are implemented in converters, they are

typically connected in parallel to deliver higher current ratings. They can also be connected in series for high voltage blocking capability however, this has not been considered in this thesis. Parallel connection is more so the case for silicon carbide devices where small area MOSFETs with low current conduction ratings are the only option. These devices can exhibit electrothermal non-uniformities arising from several factors including manufacturing variability, gate drive variability, non-uniformities in circuit parasitic inductances, variability in packaging and non-uniformities in the rate of device degradation. How these electrothermal variabilities impact energy balance between the devices will vary from technology to technology. For instance, if parallel-connected MOSFETs have different switching speeds arising from different gate resistances, how will this impact the balance of the switching losses between the devices in transients and in steady state. This is important to consider because it will determine the overall reliability of the converter since the devices will not be equally stressed, hence, one device will degrade faster than another. Furthermore, in potentially destructive switching conditions like unclamped inductive switching, the impact of device-to-device variability between parallel-connected devices on the overall ruggedness of the power converter is very important to be considered since the devices are working beyond the safety operation area (SOA). This thesis also uses finite element simulations to investigate the electrothermal dynamics between parallel connected devices under balanced and unbalanced conditions. Lattice temperature and current density plots extracted from the finite element simulator are used to understand the electrothermal characteristics of the parallel devices. Specifically, this thesis has

(1) Finite Element modelling of power semiconductor devices including silicon PiN diodes, SiC Schottky diodes, silicon MOSFET, CoolMOS, IGBT and SiC MOSFET. This modelling includes avalanche mode conduction for silicon

MOSFET, CoolMOS, IGBT and SiC MOSFET. The internal physics of these device in avalanche mode conduction is used to understand the experimental measurements.

(2) A comparison evaluation of the avalanche ruggedness for silicon 600V/20A MOSFET and silicon 600V/20A CoolMOS device.

(3) A comparative electrothermal analysis between parallel connected SiC Schottky diodes and parallel connected silicon PiN diodes. The impact of variation in the switching speed of the complimenting transistor and initial junction temperature of the devices is investigated for both technologies.

(4) A comparative avalanche ruggedness evaluation between parallel connected SiC Schottky diodes and silicon PiN diodes. The impact of variation in the thermal boundary conditions, switching speed and initial junction temperature on the avalanche ruggedness of the parallel diodes is investigated. Alongside with finite element modelling characterise the diode failure mode in avalanche mode conduction.

(5) A comparative electrothermal balancing analysis between parallel connected CoolMOS, NPT IGBT and SiC MOSFET under clamped inductive switching conditions. The impact of variation between the thermal boundary conditions (heatsink thermal resistance), the initial junction temperature and the switching speed has been analysed for the different technologies for single and repetitive switching events. Experimental measurements have been confirmed with finite element modelling of each technology.

(6) A comparative electrothermal ruggedness evaluation between parallel connected CoolMOS devices and parallel connected SiC MOSFETs. The impact of variation in initial junction temperature and switching speed on the

overall ruggedness performance of the parallel pair is investigated for both technologies. The failure mechanism and internal physics is modelled and extracted by the finite element simulator.

1.4 Outline of Thesis

Chapter 2 provides a brief introduction to the physics of power semiconductor devices for the different device types. Compact modelling and finite element modelling of the power devices are introduced. This section of the thesis focuses on finite element modelling and experimental characterisation of single power devices (transistors and diodes) under clamped and unclamped inductive switching conditions. The finite element simulator is used to explain certain characteristics peculiar to certain devices and experimental measurements are used for confirmation.

Chapter 3 presents the impact of electrothermal imbalance between parallel connected silicon PiN and SiC Schottky diodes under clamped and unclamped inductive switching conditions. Switching and conduction loss balance between the diodes as a function of electrothermal variation is investigated for both technologies. Also, the avalanche ruggedness of the parallel diodes is investigated as a function of electrothermal variation between the parallel connected pair for both technologies. The results of this chapter have been reviewed, critiqued and accepted as conference publications and will be presented in the IET Power Electronics Machines and Drives (PEMD) conference in Glasgow 2016 as well as the IEEE European Power Electronics (EPE) conference held in Karlsruhe, Germany in 2016.

Chapter 4 presents the investigation of electrothermal balancing performance between parallel connected devices for silicon IGBTs, SiC MOSFETs and CoolMOS super-

junction MOSFETs. The impact of variation in the thermal boundary conditions, initial junction temperature and switching speeds between the parallel pair have been investigated for the different technologies. This is supported by finite element simulations that give insight into the internal physics of the device through 2-D current density and lattice temperature plots. The methods, analysis and results of this chapter have been published in the IEEE transactions of power electronics and industrial electronics as first author papers by the author is this thesis. The results have also been presented in the IEEE European Power Electronics Conference (EPE) held in Geneva Switzerland in 2015.

In chapter 5, the experimental measurements on the impact of electrothermal variation between parallel connected SiC MOSFETs and parallel connected CoolMOS devices are presented. This chapter investigates how electrothermal variations affects the avalanche ruggedness of the parallel connected devices for different technologies. It explores how this electrothermal variation between the parallel pair degrades the avalanche ruggedness for different avalanche pulses i.e. high power low duration pulses and low power high duration pulses. Electrothermal variations between the parallel pair are introduced by varying the switching rate and initial junction temperature between them. Finite element simulations are used to support the experimental observations and explain the results. The methods, analysis and results of this chapter have been reviewed, critiqued and published as first author journal papers in the IEEE Transactions on Power Electronics and IEEE Transactions on Industrial Electronics by the author of this thesis. The results have also been presented in the IEEE European Power Electronics Conference (EPE) held in Geneva Switzerland in 2015.

Chapter 6 concludes the thesis and states where further work can improve the results presented here.

Chapter 2.

POWER DEVICE MODELLING

2.1 Introduction to Modelling of Power Semiconductor Devices

Power semiconductor devices are at the heart of power electronic converters. They are typically two terminal devices like diodes or three terminal devices like transistors or thyristors. They can be bipolar devices like PiN diodes, BJTs, IGBTs and thyristors or unipolar devices like MOSFETs and Schottky diodes. The modelling of power devices is critical for understanding and predicting the energy conversion losses as well improving reliability. The design loop can be simplified and significant cost saving ensured by using predictive modelling. Since power devices generate heat as a result of conduction and switching losses, and device electrical parameters like threshold voltage, on-state resistance and breakdown voltage are all temperature sensitive, then the device models must account for the feedback loop between the electrical characteristics and junction temperature. In other words, the models must be electrothermal. Electrothermal models can be realized in two major ways: by using (a) behavioural-based model, or by (b) physics-based model. Behavioural models are empirical in that they are typically derived from experimental measurements. They can also be reduced forms of more complicated

simulations. Behavioural models are computationally inexpensive and are particularly useful when large systems are simulated in a manner that does not require detailed physical knowledge of the power device [47, 48]. For example, if a wind energy conversion system comprised of the rotating electrical generator, gearbox, converter and transformer were to be simulated, given the time constants of the mechanical components of the system, a behavioural model of the power devices in the converter will suffice. On the other hand, the physics based model requires detailed knowledge of the semiconductor physics behind the operation of the device. This is important for low level device fabrication, converter design and device reliability modelling. Physics based models vary in complexity and speed. For example, SPICE models as less computationally expensive than finite element models, however, cannot account for certain physical phenomena that finite element models can explain. In general, there is a trade-off between simulation accuracy and computational cost. The more accurate a model is, the more computationally expensive it will be.

2.1.1 Compact Device Models

Compact models are more accurate and computationally intensive than behavioural models but not as accurate as finite element models. The mathematical compact model is based on solving physics-based equations with varying degrees of complexity thereby resulting in analytical expressions describing carrier and electrical behaviour.

In the lumped-charge models, carrier dynamics are divided into discrete charges within the device with the charge of each region being considered as its average charge [49, 50]. This offers rapid simulation time however at the cost of reduced accuracy. The lumped-charge model initially developed for simulation of the power diode has also been

exploited for the MOSFET [51] and IGBT [52]. The model is capable of simulating the reverse recovery of the power diode [50].

2.1.2 Numerical models

The ambipolar diffusion equation (ADE) model used in compact model implemented the semiconductor equations based on the assumption of quasi-neutrality or principle of the ideal depletion layer behaviour. However, certain non-linear characteristics like the exponential dependence of carrier density on potential limits the accuracy of compact models. Therefore, for a high degree of accuracy, numerical schemes such as finite element or finite difference are good candidates. There are several commercial device simulators including ATLAS, Sentaurus and Medici [47, 53]. These simulators decompose the device under study into a pre-defined mesh with each mesh point investigated individually based on doping level, potential and lattice temperature, etc. During static and dynamic simulations, the hole and electron carrier density at each mesh point is used to derive the electric field and current, and is fed back into the neighbouring mesh points to generate a distributed model. The mesh size must be implemented carefully to avoid numerical instability due to the discrete nature of the model. The mesh size also determines the accuracy of the simulation. Fine meshes will result in higher accuracy but at a cost of reduced computational speed and increased computational cost. ATLAS from SILVACO is typically used by the semiconductor designers for designing devices as well as modelling static and dynamic characteristics. Hence in this thesis, all the simulations are carried out from ATLAS.

2.2 Compact Models for Power Semiconductor devices

Structural design improvements such as trench gates [54, 55], super-junctions [56, 57], Junction-Barrier-Schottky designs [58, 59] and thick-bottom-oxide/split gate trench designs [60, 61] in power semiconductor devices have led to increased application range and improved efficiency of power electronics. Recently released power semiconductor devices can sustain higher blocking voltage, switching at higher frequencies and exhibit lower on-state resistance [62-64]. However, these improvements can also cause reliability problems like ringing, voltage overshoots resulting from high *dI/dt* and *dV/dt*, parasitic turn-on and/or turn-off due to cross-talk between devices. Therefore, accurate compact models for power semiconductor devices are required by circuit designers to evaluate and predict circuit behaviour, though, they have limited insight into the internal physics of the device.

PiN diode

The PiN rectifier is fabricated by simply inserting a lightly doped voltage blocking epitaxial n layer between a conductive n+ cathode and a conductive p+ anode as shown in Figure 2.1.

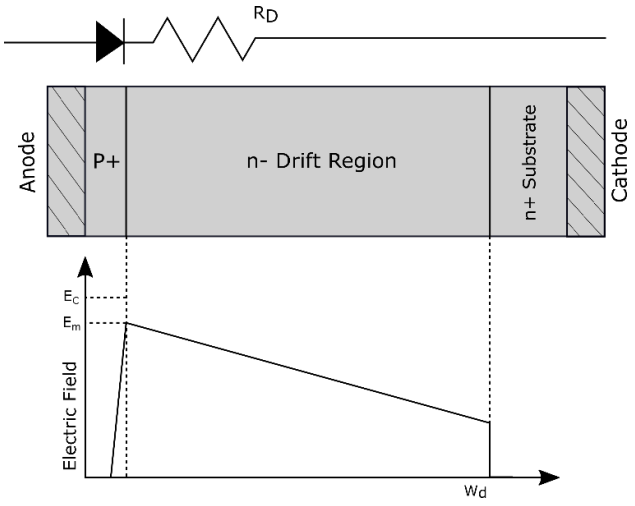


Figure 2.1: The electric field distribution of the PiN diode.

PiN diodes are designed for high voltage applications where high blocking voltage in one direction and high current conductivity in the opposite direction is required. The on state conductivity is improved by minority carrier injection into the drift region, which results in charge storage during the on-state. This charge storage in the drift region leads to non-ideal behaviour like forward and reverse recovery charge during switching transients. The PiN diode exhibits on-state current conduction mechanisms at different current level [26]. At very low current density, the recombination current in the space-charge layer is the dominant component of the current. At low current density, minority carriers from the highly doped terminals are injected into the drift region and the diffusion of these carrier dominates the current transported. At high current densities, there is significant minority carrier injection into the drift region from the p+ region. When the injected hole concentration into the drift region exceeds the background doping concentration (N_D), charge neutrality requires that the concentration of electrons and holes must become equal: $n(x) = p(x)$. The excess carrier density in the drift region is determined by the ADE as [26, 65-67]:

$$D\frac{\partial^2 p(x,t)}{\partial x^2} = \frac{p(x,t)}{\tau_{HL}} + \frac{\partial p(x,t)}{\partial t} \tag{2.1}$$

where p is the hole concentration; τ_{HL} is the ambipolar carrier lifetime; D is the ambipolar diffusivity

$$D = \frac{2D_n D_p}{D_n + D_p} \tag{2.2}$$

where D_n and D_p is the diffusivity for electrons and holes, respectively. The carrier diffusivity is related to carrier effective mobility using Einstein relationship given by:

$$D_{n(p)} = \frac{kT}{q}\mu_{n(p)} \tag{2.3}$$

By solving the continuity equation for the drift region, the carrier distribution within the drift region can be obtained as:

$$\frac{\partial n}{\partial t} = -\frac{n}{\tau_{HL}} + D_n \frac{\partial^2 n}{\partial x^2} + \mu_n \frac{\partial}{\partial x}(nE) \tag{2.4}$$

$$\frac{\partial p}{\partial t} = -\frac{p}{\tau_{HL}} + D_p \frac{\partial^2 p}{\partial x^2} - \mu_p \frac{\partial}{\partial x}(pE) \tag{2.5}$$

where μ_n and μ_p is the carrier mobility for electrons and holes, respectively. E is electric field. The current flow occurs exclusively by hole transport and electron transport at the drift region end junction with p+ and junction with n+, respectively. The total current flow through the PiN diode is give as:

$$J_T = 2qD_n\left(\frac{dn}{dx}\right)_{n+n-Junction} = 2qD_p\left(\frac{dn}{dx}\right)_{p+n-Junction} \tag{2.6}$$

The on-state voltage drop for a PiN diode is given as [26, 68]:

$$V_{ON} = \frac{2kT}{q}\ln\left(\frac{J_T w_d}{4qn_i F\left(\frac{w_d}{2L_a}\right)}\right) \tag{2.7}$$

where w_d is drift region width, $F(\frac{w_d}{2L_a})$ is a function of drift region width and character length and n_i is the intrinsic carrier concentration. More accurate and detailed simulations based on these equations has been presented in [65-67, 69-72].

The diode is typically operating as a freewheeling diode in clamped inductive switching circuit as presented in section 2.5.1. Due to the stored charge during the on-

state, PiN diodes exhibit reverse recovery during its turn-Off. Figure 2.2 shows the current and voltage waveforms of the PiN diode during the turn off transient. Between t_0 and t_1, the diode turns off with a negative current commutation rate which is determined by the switching rate of the external circuit and parasitic series inductance. Between t_1 and t_2, the current becomes negative as a result of carrier extraction from the charge storage region in the drift layer. At this point the PiN diode is still forward biased, however, the rising voltage starts to reverse bias the cathode to drift layer junction as well the drift layer to anode junction. At the point where the diode starts becoming reverse biased, the junctions start becoming depleted, thereby causing the supply of carriers to cease. It is at this point that the negative current through the diode reaches its peak at time t_2. As the voltage across the diode increases and the diode becomes more reverse biased, the remaining charges stored in the drift layer recombine at a rate that depends on the minority carrier lifetime and the recombination rate. Between time t_2 and t_3, the diode recombination current takes the negative current back to zero and diode voltage reaches the peak voltage.

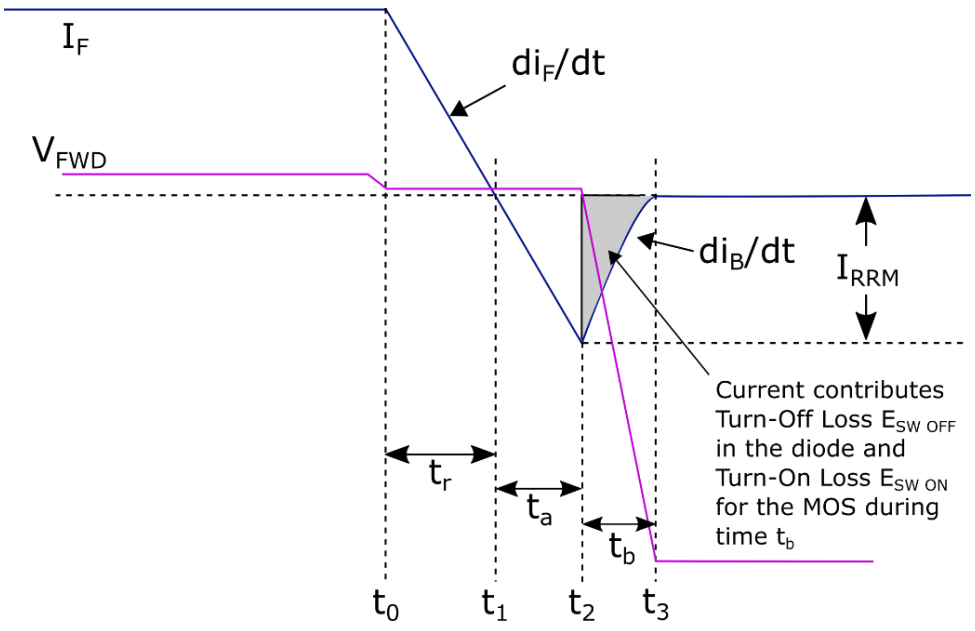


Figure 2.2: The reverse recovery characterize waveform for the PiN diode.

The reverse recovery charge results in a significant switching losses in PiN diodes which is dissipated as heat. Because minority carrier lifetime increases with temperature, the stored charge and reverse recovery losses increase with temperature. It is important to ensure that the recovery of the diode is not too snappy (high dI/dt) i.e. the positive slope of the recombination current is not too high. This is due to the fact that a high dI/dt from the recombination current coupled with parasitic inductance can cause significant over-voltages capable of destroying the diode and even the complimentary transistor commutating current away from the diode. There are diodes designed for high switching frequencies with reduced stored charge. This is usually achieved by using a minority lifetime treatment process that involves injecting lifetime killers to limit the amount of stored charge. This is at the cost of higher conduction losses, since the on-state resistance of the PiN diode reduces with increasing stored charge. Hence, in designing PiN diodes, there is a trade-off between the conduction and switching losses depending on the switching frequency used in the application [64, 73].

SiC Schottky Barrier Diode

The SiC Schottky Barrier Diode (SBD) is a unipolar power device formed by intimate rectifying contact between SiC and a metal. An in-built potential is formed by the depletion of the semiconductor adjacent to the contact with the magnitude of the voltage being proportional to the difference between the work-function of the metal and the fermi-level of the semiconductor. SiC SBDs rely on the electric field distribution in the drift region to block the reverse voltage. Schottky diodes do not use conductivity modulation from minority carrier injection, hence, ultra-thin voltage blocking drift layers are needed to minimise the conduction losses. This is why newer Schottky diodes are usually fabricated out of SiC and not silicon, since the high critical field and wide bandgap

enables the use of thin voltage blocking epitaxial layers. When the metal-semiconductor contact is forward biased with a voltage greater than the in-built value, the electrons in the drift region gain sufficient energy to transit from conduction band in the semiconductor to a state of rest in free space outside the surface of the semiconductor. Therefore, the forward current density with applied forward bias voltage is given as:

$$J_F = A \cdot T^2 e^{-\left(\frac{q\Phi_{BN}}{kT}\right)} \left[e^{\left(\frac{qV_{FS}}{kT}\right)} - 1 \right] \tag{2.8}$$

where A is the effective Richardson's constant, T is the absolute temperature, V_{FS} is the bias voltage, Φ_{BN} is the Schottky barrier height, k is the Boltzmann's constant. The on-state voltage drop for a Schottky diode, including the voltage drop in the drift region can be expressed as:

$$V_F = V_{FS} + V_{R(drift\ region)} = \frac{kT}{q} \ln\left(\frac{J_F}{J_s}\right) + J_F \cdot \left(R_D + R_{sub} + R_{cont}\right) \tag{2.9}$$

where J_s is the saturation current density, R_{CONT} is the Schottky contact resistance and R_{SUB} is the resistance in the substrate. R_D is the resistance of the drift region which is related to the breakdown voltage as [26]:

$$R_D = R_{on-ideal}\left(4H-SiC\right) = 2.97 \times 10^{-12} BV^{2.5} \tag{2.10}$$

Silicon and SiC MOSFET

The MOSFET has three terminals namely the Source, Gate and Drain. The vertical power MOSFET was developed as a modification of the lateral MOSFET with high voltage and high current applications as the target. It relies on the vertical drift region to support the high reverse bias voltage, while using an insulated gate to control the current flow between the source and drain. Since, the MOSFET gate interfaces with the channel

through an insulator (the gate oxide), the input current during steady state operation is ideally zero, hence, the gate drive losses are reduced compared to a thyristor or BJT gate driver. As a result, MOSFET gate drivers are easier to design since current is supplied only during the switching transients and the currents can easily be controlled using voltage sources, opto-couplers and gate resistors [26]. Figure 2.3 shows an example of vertical-diffused (VD) MOSFET structure together with the circuit representation showing the parasitic inter-terminal capacitances. The source and drain terminals are ohmic contacts formed on highly doped n+ regions. The n-type source is surrounded by the p-type body as shown in Figure 2.3 while the gate interfaces the p-type body through a thin layer of oxide. It can be seen from Figure 2.3 that the MOSFET is a complex device consisting of a parasitic npn BJT and an internal anti-parallel PiN diode. Hence the p-body is shorted to the source by using a heavily doped p-type implant to prevent a floating body. In the off-state, the MOSFET is able to block high voltages by using think and lightly doped voltage blocking drift layers to sustain the electric field.

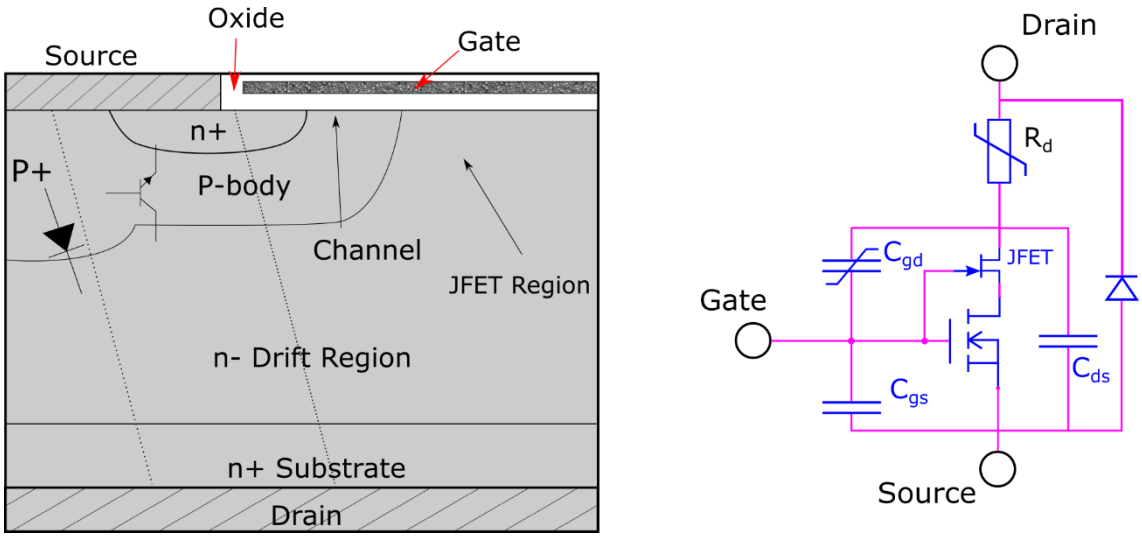


Figure 2.3: Vertical Diffusion MOSFET structure.

For a MOSFET to turn on, the applied gate voltage needs to be greater than the threshold voltage which is defined as:

$$V_{TH} = \frac{t_{OX}}{\varepsilon_{OX}} \sqrt{4\varepsilon_s kTN_A \ln(\frac{N_A}{n_i})} + \frac{2kT}{q} \ln\left(\frac{N_A}{n_i}\right) \tag{2.11}$$

where t_{OX} is the thickness of the gate oxide, ε_{OX} is the oxide dielectric constant, ε_s is the semiconductor dielectric constant, k is the Boltzmann's constant, N_A is the doping concentration in the p-base region and n_i is the intrinsic carrier concentration. Technically, the threshold voltage is defined as the gate voltage at which the surface potential of the semiconductor is twice the bulk potential and thus sufficient to invert the semiconductor from p-type to n-type. The on-state channel resistance for a VD-MOSFET is thus controllable by the gate voltage according to:

$$R_{CH} = \frac{L_{CH} \cdot W_{cell}}{2 \cdot \mu_{ni} \cdot C_{OX} \cdot (V_G - V_{TH})} \tag{2.12}$$

where L_{CH} is the channel length, W_{cell} is the cell pitch width, μ_{ni} is the inversion layer mobility, C_{OX} is the specific capacitance of gate oxide which is specified as:

$$C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}} \tag{2.13}$$

In addition to the channel resistance, there is a JFET resistance, drift region resistance and terminal contact resistance. The JFET resistance is given as:

$$R_{JFET} = \frac{x_{JP} W_{Cell}}{q\mu_n N_{DJ} (W_G - 2x_P - 2W_0)} \tag{2.14}$$

where x_{JP} is the P-base junction depth, μ_n is the bulk mobility appropriate to the doping level of the JFET region, N_{DJ} is the doping concentration in the JFET region, W_0 is the

zero-bias depletion width for the JFET region and W_G is the gate width. The drift region resistance is given as:

$$R_D = \frac{\rho_D \cdot W_{Cell}}{2} \ln\left(\frac{W_{Cell}}{a}\right) + \rho_D \left(t + \frac{a}{2} - \frac{W_{Cell}}{2}\right) \tag{2.15}$$

where ρ_D is resistivity of the drift region, a is the JFET region width. The MOSFET is able to control the drain-source current through the induced channel in the p-body under the gate terminal. When the gate source is forward biased with the threshold voltage, the electric field across the gate oxide inverts the p-body and creates a channel. This channel connects the source n+ source with the drift region, thus the source terminal is connected with the drain through the n+ channel and drift region. The gate oxide is generally very thin (<50 nm) to control the threshold voltage and maintain the high transconductance [26, 74]. The transconductance of the MOSFET is given by:

$$g_{mL} = \frac{W \mu_{ni} C_{OX}}{L_{CH}} V_D \tag{2.16}$$

where W is the channel width, C_{OX} is capacitance density of the gate oxide and μ_{ni} is the inversion layer mobility for electrons. Hence the MOSFET has a saturated drain current for a given gate voltage as:

$$I_{D,sat} = \frac{W \mu_{ni} C_{OX}}{2 \cdot L_{CH}} \cdot \left(V_{GS} - V_{TH}\right)^2 \tag{2.17}$$

With different assumptions, accurate and reliable compact models have been proposed for either silicon or SiC devices [75-83].

Power MOSFETs exhibit inter-terminal parasitic capacitances that charge and discharge during switching transients thereby contributing to switching losses. The three capacitances are the gate-source (C_{GS}), drain-source (C_{DS}) and gate-drain (C_{GD})

capacitances. The sum of the gate-source and gate-drain capacitances is the input capacitance. This capacitance must be charged before the transistor is switched on.

$$C_{ISS} = C_{GS} + C_{GD} \tag{2.18}$$

The gate-source capacitance is due to the overlap between the MOSFET gate and source and depends on the area of overlap as well as the gate oxide thickness

$$C_{GS} = \frac{2x_{PL}}{W_{Cell}}\left(\frac{\varepsilon_{OX}}{t_{OX}}\right) + \frac{W_G}{W_{Cell}}\left(\frac{\varepsilon_{OX}}{t_{IEOX}}\right) \tag{2.19}$$

$$C_{GD} = \frac{W_G - 2x_{PL}}{W_{Cell}} \cdot \sqrt{\frac{qN_D\varepsilon_S}{2\left(V_D + V_{bi}\right)}} \tag{2.20}$$

where W_G is the gate width, x_{PL} is the overlap length of gate oxide and p-body region, t_{OX} is the oxide thickness between the gate and semiconductor and and t_{IEOX} is the oxide thickness between the gate and the source metal respectively. The gate-drain capacitance, also referred to as the Miller capacitance is due to the overlap between the gate and drain. It is a series combination of an oxide capacitance and a depletion capacitance. The oxide capacitance is fixed while the depletion capacitance depends on the drain voltage. Hence, the gate-drain capacitance is a non-linear capacitance that changes during switching. The output capacitance (C_{OSS}) is the sum of the gate-drain and drain-source capacitance. Both capacitances are voltage dependent; hence, the output capacitance also exhibits non-linear behaviour during the switching transient.

$$C_{oss} = \left(\frac{W_{PW} + 2x_{PL}}{W_{Cell}}\right) \cdot \sqrt{\frac{q \cdot N_D \cdot \varepsilon_S}{2\left(V_D + V_{bi}\right)}} \tag{2.21}$$

where $W_{PW} + x_{PL}$ is the area of the junction within the cell and V_D is the drain voltage.

The switching waveforms due to the charging and discharging of this parasitic capacitances cause an overlap between the output voltages and currents according to the Figure 2.4 shown below. The charging of the gate-drain capacitance causes the drain voltage to fall from the supply voltage to the on-state voltage during turn on. Likewise, during turn off, the discharge of the gate-drain capacitance causes the drain voltage of the MOSFET to rise from the on-state voltage to the supply voltage.

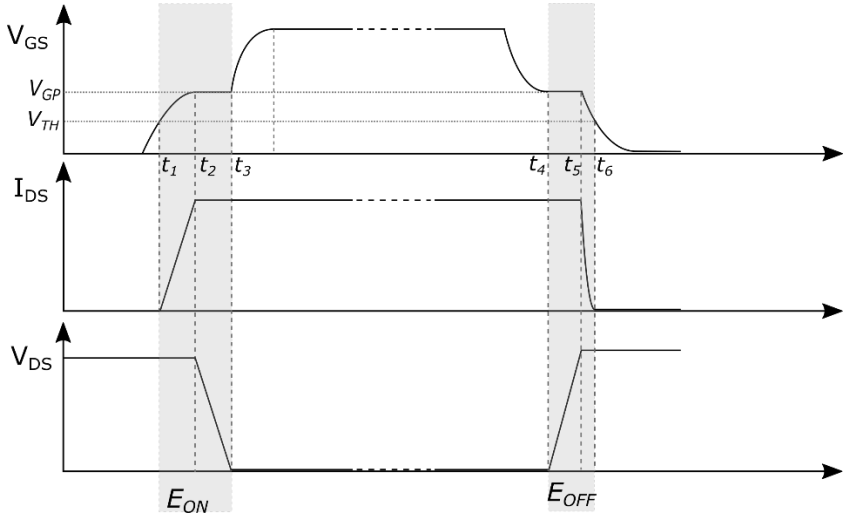


Figure 2.4: Switching characteristic waveforms for the MOSFET with clamped inductive load.

Super Junction MOSFET

MOSFETs exhibit high on-state resistance and conduction losses as the blocking voltage increases. This is due to the fact that thicker and more resistance epitaxial layers are needed to block higher voltages. This is why MOSFETs are limited to lower voltage applications. However, super-junction MOSFETs use the principle of charge balance from vertical p-n junctions in the drift region to break this limit. By using these p-pillars in the drift region, higher voltages can be blocked without using thick and resistive epitaxial layers. This vertical junction in the drift region distributes the electric field

uniformly across the drift layer and since the breakdown voltage is the integral of the electric field over distance, higher breakdown voltages are achieved using 2 dimensional depletion. CoolMOS is an alternative name for super junction MOSFETs and was first commercialized by Infineon in 1999 [57]. Figure 2.5 shows a comparison of the electric field distribution at breakdown voltage for a conventional MOSFET and a CoolMOS device with similar drift region thickness and doping level.

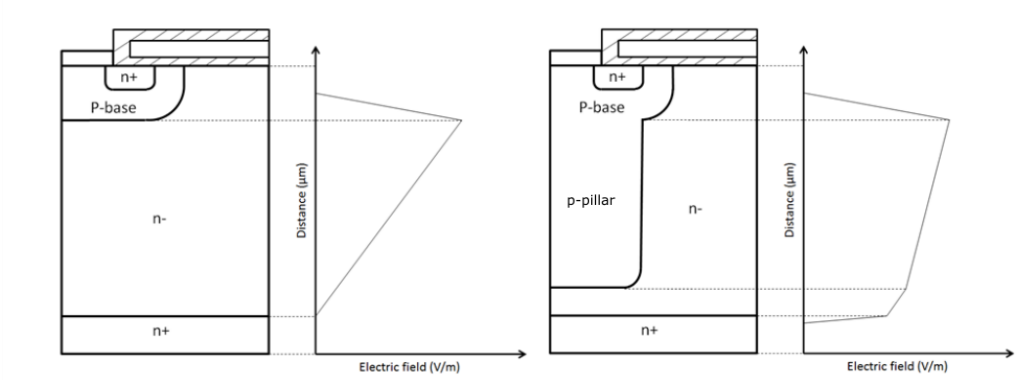


Figure 2.5: A Comparison of electric field distribution for the MOSFET and CoolMOS.

It can be seen that the electric field has a larger area for the CoolMOS device which means that it has a higher breakdown voltage. For super-junction devices, the breakdown voltage is not only dependent on the doping concentration and drift region thickness, but is also dependent on the doping balancing between the n stripe and p stripe pillars in the drift region. Figure 2.6 shows the breakdown voltage as a function of doping balance between the n and p pillars 5 µm width for the n stripe and p stripe. It can be seen from Figure 2.6 that the breakdown voltage reduces with larger doping unbalance. It can be seen that the breakdown voltage reduces from 600 V to 440 V for a 20 % difference in doping. Commercial CoolMOS devices are generally rated from 600V to 900V and is competitive with silicon IGBTs at this voltage level.

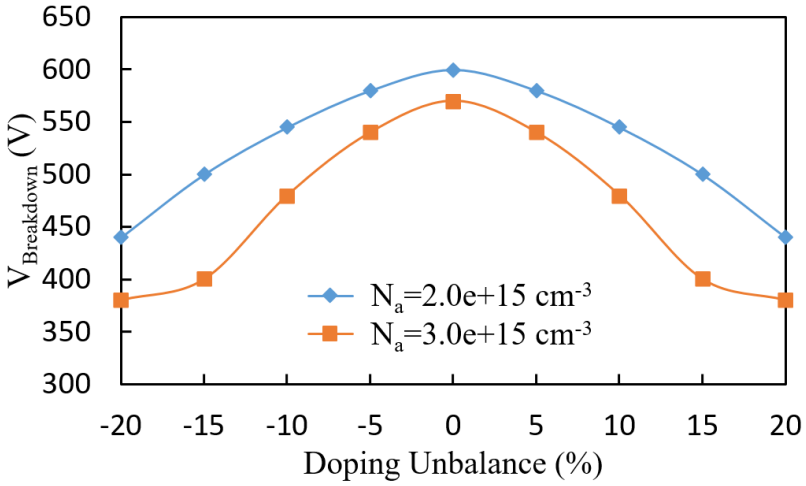


Figure 2.6: The breakdown voltage as a function of doping balance for CoolMOS.

Insulated Gate Bipolar Transistors (IGBTs)

As has been mentioned previously, MOSFETs are limited in high voltage applications because of the conduction losses associated with the thick and resistive epitaxial layers needed to block the higher voltages. The on-state resistance increases in relation to the breakdown voltage according to the well-known silicon limit expressed by [26] as

$$R_{ON} \approx 8.3\times10^{-9} V_B^{2.5}\ \Omega\cdot cm^2 \qquad (2.22)$$

Although CoolMOS and SiC devices have pushed MOSFETs into the 1 kV and even 1.7 kV blocking voltage application space, the dominant technology in medium voltage application is the IGBT. The IGBT is very similar to the MOSFET because both transistors have an insulated gate input formed by a MOS structure. However, the IGBT differs from the MOSFET in that it has an additional p layer after the n- drift and n+ layer. This additional p+ layer enhances the on-state conduction losses by injecting holes into the voltage blocking drift region as electrons are injected into the same region from the MOS channel. Hence, IGBTs have the advantage of a MOS input since the device is

voltage driven and combines this with the advantage of a BJT output, since there is conductivity modulation. Hence, the conduction losses of IGBTs outperform that of MOSFETs since the drift region during the on-state is saturated by electrons injected from the MOS channel and holes injected from the p+ cathode.

IGBTs can be punch-through IGBTs and non-punch-through (NPT) IGBTs. Figure 2.7 shows the pictures of both IGBTs. The primary difference between the PT-IGBT and the NPT-IGBT is the fact that the PT-IGBT has an additional N+ buffer layer between the n-drift layer and the p+ collector as shown in Figure 2.7. The NPT IGBT does not have this additional buffer layer. Due to the low resistance of this buffer layer, PT IGBTs typically have lower conduction losses since the buffer layer is effective is minimizing the depletion width at high voltages. Hence, PT-IGBTs have better conduction and switching losses compared to NPT IGBTs, however, the on-state voltage is sometimes negatively correlated with temperature due to increased carrier injection from the buffer layer as temperature increases. Hence, NPT-IGBTs are preferred in high current power modules where several IGBT chips are connected in parallel.

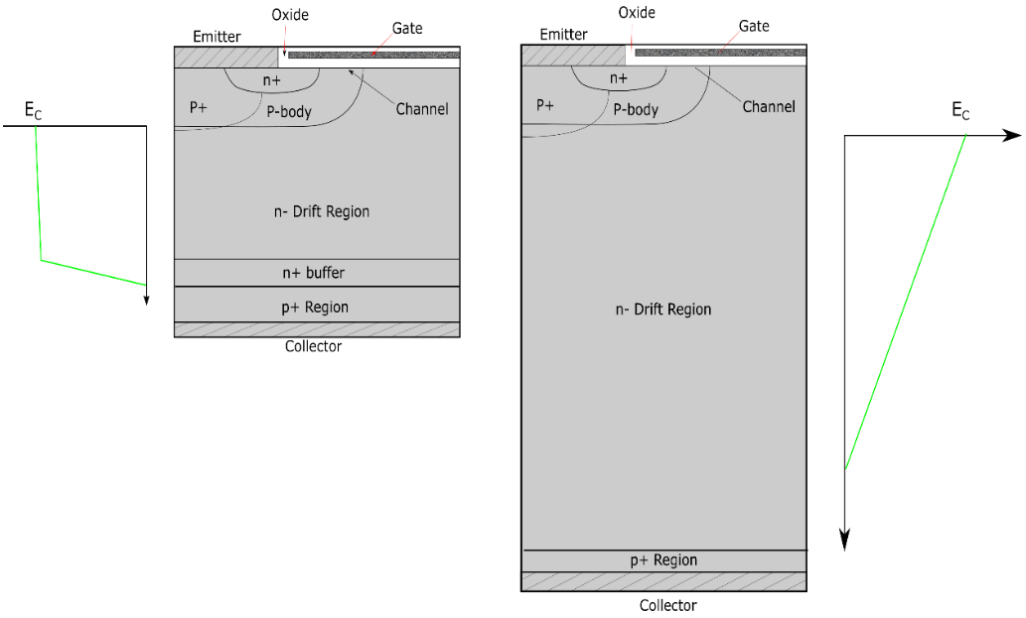


Figure 2.7: PT and NPT IGBT structure.

One of the main disadvantages of PT-IGBTs is the snappiness of the turn-OFF current transient i.e. the high *dI/dt* that occurs during punch-through when the drift layer becomes fully depleted, the device capacitance drops precipitously and all the minority hole carriers are swept into the N+ buffer layer. The snappiness occurs because the N+ buffer layer causes high recombination rates for holes since the increased electron concentration reduces the minority carrier lifetime. This snappiness does not occur in NPT-IGBTs because of the absence of the N+ buffer between the p+ collector and the voltage blocking drift layer. This is why NPT-IGBTs exhibit long tail currents from minority carrier recombination during turn-OFF. The snappiness in the turn-OFF current of PT-IGBTs can cause severe over-voltages since the combination of high dI/dt and parasitic inductances cause voltage overshoots. To mitigate this effect, manufacturers like ABB have developed a Field-Stop IGBT (FS-IGBT) where a gentle grading in the N+ buffer doping is introduced to reduce the rate of punch-through [48, 84]. Both the PT-IGBT and the FS-IGBT make use of the N+ buffer layer to create a trapezoidal electric field thereby minimizing the drift layer thickness by minimizing the maximum depletion at the full blocking voltage. However, the major difference between the PT-IGBT and the FS-IGBT arises from the fact that the FS-IGBT uses an N+ doping profile with a lower rate of change of doping with distance in the direction of epitaxial growth The reduced rate at which punch-through occurs reduces the snappiness of the current turn-OFF transient, hence, this IGBT is sometimes called the Soft-Punch-through IGBT (SPT-IGBT). Another major difference between the FS-IGBT and the PT-IGBT is that the P+ collector in the FS-IGBT is formed by ion implantation while the P+ collector in the PT-IGBT is formed by in-situ doping during epitaxial growth of the wafer.

It is important in such power modules that the IGBTs have an on-state voltage drop that increases with temperature since this is a requirement for electrothermal stability and

good current sharing between parallel transistors. The on-state voltage drop for the IGBT can be obtained as:

$$V_{ON} = V_{P+N} + V_{NB} + V_{MOSFET} \tag{2.23}$$

where V_{P+N} is the voltage drop across the bottom p+ collector/n-drift region junction. For NPT IGBT it can be obtained as:

$$V_{P+N} = \frac{kT}{q}\ln\left(\frac{p_0 N_D}{n_i^2}\right) \tag{2.24}$$

where p_0 is the increase in the hole concentration at the junction. The V_{MOSFET} is equivalent to the channel resistance which is defined as:

$$V_{MOSFET} = \frac{J_C L_{CH} W_{Cell}}{2\mu_{ni} C_{OX}\left(V_G - V_{TH}\right)} \tag{2.25}$$

where J_C is the collector current flow. The voltage drop across the n-drift region is rather complex due to the minority carrier injection. However it still can be obtained by integrating the vertical electric field as:

$$\begin{aligned} V_{NB} = {} & \frac{2L_a J_C \sinh\left(\frac{W_N}{L_a}\right)}{qp_0\left(\mu_n + \mu_p\right)}\left\{tanh^{-1}\left[e^{-\left(\frac{W_{ON}}{L_a}\right)}\right] - tanh^{-1}\left[e^{-\left(\frac{W_N}{L_a}\right)}\right]\right. \\ & \left. + \frac{kT}{q}\left(\frac{\mu_n - \mu_p}{\mu_n + \mu_p}\right)\ln\left[\frac{\tanh\left(\frac{W_{ON}}{L_a}\right)\cosh\left(\frac{W_{ON}}{L_a}\right)}{\tanh\left(\frac{W_N}{L_a}\right)\cosh\left(\frac{W_N}{L_a}\right)}\right]\right. \end{aligned} \tag{2.26}$$

where W_N is the width of the lightly doped N-drift region, W_{ON} is the depletion width, L_a is the ambipolar diffusion length. Since, the IGBT is a bipolar device, there is charge

stored in the drift region that needs to be extracted during turn off and formed up during turn on. The charge quantity in the drift region is defined as:

$$\boldsymbol{Q_{ds}} = \begin{cases} \boldsymbol{A_{device}\sqrt{2\varepsilon_{si}(V_{ce}+0.6)q\cdot N_{scl}}} & \boldsymbol{for} \quad \boldsymbol{V_{ce} \le V_{rt}} \\ \boldsymbol{qA_{device}W_L N_{scl} + \frac{A_{ds}\varepsilon_{si}(V_{ce}-V_{rt})}{W_L}} & \boldsymbol{for} \quad \boldsymbol{V_{ce} > V_{rt}} \end{cases} \tag{2.27}$$

where N_{scl} is the collector-base space charge concentration, V_{rt} is reach through voltage of the p+collector/N-base junction. Again, based on different assumptions, these equations can be simplified and taken in consideration with more practical conditions like parasitic inductance which has been proposed in [47, 48, 52, 85-88].

IGBTs, MOSFET and CoolMOS devices have operation losses that can be classified into conduction losses, switching losses, output capacitance losses, reverse charge losses and gate drive losses. The proportion of these losses will depend on the application, switching frequency and operating temperature. Advanced transistors have been engineered to minimise energy conversion losses. These losses can be summarised as the equations below [89]:

Power Loss Category	Corresponding Equation
Conduction Losses	$P_{COND} = I^2 R_{DS\,ON}$
Switching Losses	$P_{SW} = V_{IN}(Q_{GD} + Q_{GS}) f_{Switch}$
Output Capacitance Losses	$P_{OSS} = \frac{1}{2} V_{IN} Q_{OSS} f_{Switch}$
Reverse Charge Recovery Losses	$P_{QRR} = V_{IN} Q_{QRR} f_{Switch}$
Gate Drive Losses	$P_{GD} = V_G Q_G f_{Switch}$

Table 2-1: Loss classification and corresponding equations.

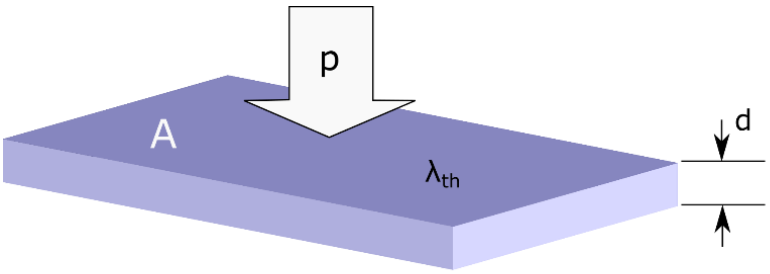
2.3 Transient Thermal Impedance Characteristics and Thermal Modelling of Power devices

It is important to be able to calculate the junction temperature of a power semiconductor device given the instantaneous power dissipation. The junction temperature can be most accurately modelled using finite element techniques since that method can account for temperature non-uniformity within the device. However, using a compact thermal model based on lumped thermal resistances and capacitances can suffice for estimating the average junction temperature. Junction-to-case transient thermal impedance characteristics are normally given on datasheet for the purpose of estimating the junction temperature. This transient thermal characteristic can be used to create a thermal impedance network comprised of thermal resistances and capacitances.

The heat flow equation for a homogeneous isotropic material is given by

$$\frac{\partial^2 T}{\partial x^2} = \frac{c \cdot \rho}{\lambda_{th}} \cdot \frac{\partial T}{\partial t} \tag{2.28}$$

where λ_{th} is the specific heat conductance, c is the thermal capacitance, ρ is the density of material and x is the coordinate distance in the direction of heat transfer. The 3 dimensional solution for this equation for a system comprised of different materials and interfaces can become very complicated. Hence, for the sake of simplification, the thermal network of the power semiconductor device is assumed to be a one-dimensional heat flow problem which consists of several thermal resistances and thermal capacitances. This is not an unreasonable assumption since the primary direction of heat flow is from the junction to the case and from the case to the heatsink. A simple 1-dimensional thermal system is shown below in Figure 2.8.



$$R_{th} = \frac{d}{A \cdot \lambda_{th}}$$

$$C_{th} = c \cdot \rho \cdot d \cdot A$$

Figure 2.8: The schematic of thermal equivalent elements.

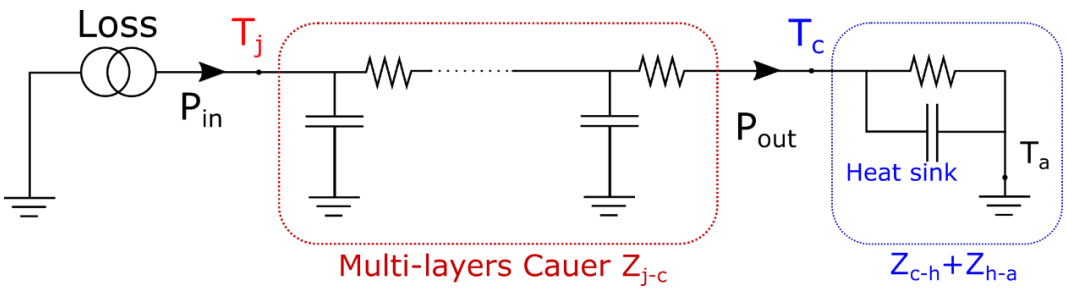
There are two commonly used equivalent circuit models namely the continued fraction circuit (Cauer model as shown in Figure 2.9(a)) and partial fraction circuit (Foster model as shown in Figure 2.9(b)). The Cauer network models the thermal capacitance of each layer with an intermediary thermal resistance. Shown alongside the Cauer network is a cross-section of a typical power electronic assembly comprised of a semiconductor die connected to a heatsink through a multi-layer arrangement of solder, copper base plate and a thermal contact which can be aluminium nitride (AlN) or ceramic (Al_2O_3). The value of each connecting node in the Cauer network represents the temperature in the corresponding layer of the power semiconductor assembly. Hence the dynamic temperature gradient along the direction of heat flow can be extracted from this model. However, it is quite difficult to determine the exact thermal property of each layer due to 3-dimensional heat spreading.

The transient thermal impedance characteristic can be generated for a power semiconductor device by applying some input electrical power sufficient to raise the junction temperature of the device to a predefined value via self-heating. This temperature is typically determined using a temperature sensitive electrical parameter (TSEP) like the forward voltage of a diode or the on-state voltage drop of a transistor. Therefore, the real-time junction temperature can be extracted using the TSEP while the real-time case

temperature can be monitored using a fast response thermocouple. The thermal resistance can be measured by supplying constant power to the device until it reaches steady state junction and case temperature while the thermal capacitance can be measured from the transient between the application of the input power and the steady-state temperature. Furthermore, by switching off the applied power and monitoring the cooling curve, the transient thermal impedance characteristics together with the lumped thermal parameters (thermal capacitances and resistances) can be extracted [90-94]. The transient thermal impedance from the cooling curve is given by:

$$Z_{th}(t) = \frac{T_{j1} - T_j(t)}{P_1} \tag{2.29}$$

where T_{j1} is the steady state junction temperature due to the self-heating and P_1 is the steady state input power. The heating curve is more difficult to use because the heating current and sensing current have to be applied simultaneously to the device which makes the junction temperature determination difficult. Since the heating current is absent during the cooling of the device, the sensing current can be used to determine the junction temperature easily.



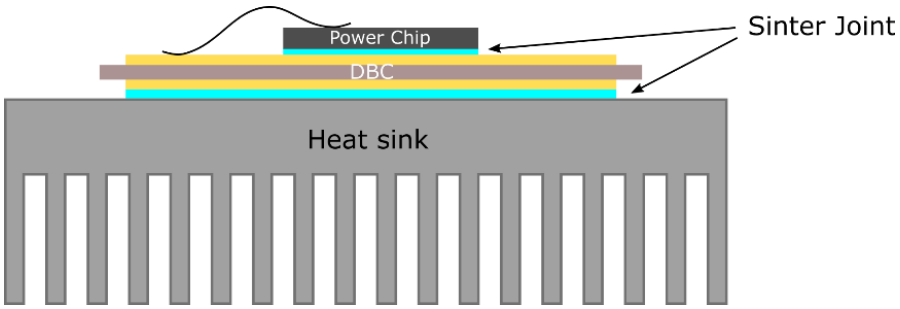


Figure 2.9(a): The Cauer thermal network schematic.

The Cauer thermal network shown in Figure 2.9(a), based on the transmission line model, is more closely correlated with the physical arrangement of the power electronic assembly shown. A more mathematically simpler, however physically uncorrelated thermal network that can be derived from the transient thermal impedance characteristic is the Foster network shown in Figure 2.9(b):

$$Z_{th}(t) = \sum_{v=1}^{n} R_v \left(1 - e^{-\frac{t}{R_v C_v}} \right) \tag{2.30}$$

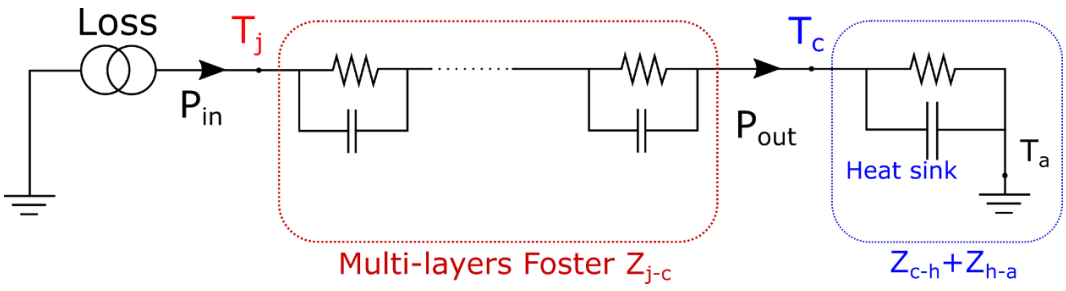


Figure 2.9(b): The Foster thermal network schematic.

The Foster network shown in Figure 2.9(b) is useful for estimating the junction temperature of a device on the assumption that there is no physical meaning that can be attached to the lumped thermal resistances and capacitance, hence, the power device assembly at the terminal of interest can be treated as a black box.

2.3.1 Thermal network in finite element modelling

The choice of the thermal resistance and thermal capacitance values used in the finite element models is critical for ensuring that the simulator predicts the correct thermal response. The size of the mesh will determine the thermal resistance and capacitance of the semiconductor chip being simulated. However, the power devices measured and characterised in this thesis are typically discrete power semiconductors in three-lead packages like TO-247 and TO-220, which means that there are additional thermal resistances and capacitances due to the solder, the copper base and the lead-frame. Hence, the simulator will have to account for the junction to case thermal resistance and the total thermal capacitance of the device and package. To enable this, the finite element simulator provides a choice of connecting lumped thermal resistances and capacitances to the power device being simulated. These lumped thermal components are chosen to emulate the effects of the solder layer, the copper base plate and the lead-frame. The choice of the components is guided by the transient thermal impedance characteristics taken from the device datasheet where the steady-state thermal impedance is equal to the junction to case thermal resistance and the rate of change of the transient thermal impedance with time determines the junction capacitance. There are generally 3 methods of determining the values of these lumped thermal components. These are briefly explained below.

i. **Foster Network Characterisation**: This method uses a multiple layer Foster network to generate a curve that replicates the datasheet transient thermal impedance characteristic. The R_{TH} and C_{TH} values are iteratively tested for curve fitting. The values arrived at have no physical meaning since the Foster network is a mathematical construct that is not directly derived from the device structure.

ii. **Cauer Network Characterisation**: Here, the physical thermal resistance and capacitance of each layer is calculated from the physical dimensions (thickness and area) and the known thermal properties (density and thermal conductivity) of the materials. This method relies on intimate design knowledge of the packaging process and materials including solder thickness, chemistry as well as base-plate and lead-frame dimensions.

iii. **Experimental Characterisation with Specialised Equipment**: This method relies on injecting power into the device using a constant current source and measuring the junction and case temperatures at different power levels. The non-trivial task of simultaneously measuring the junction and case temperature requires dedicated and specialised equipment that can be bought from specific vendors.

In this thesis, the first method. Figure 2.10 below shows a single layer Foster network. The thermal network can be analysed in a similar manner to an electrical network where the thermal resistance behaves like an electrical resistance, the thermal capacitance behaves like an electrical capacitance, the dissipated power from the conduction and switching losses of the device emulates the current source and the temperature response is analogous to the voltage drop across the components.

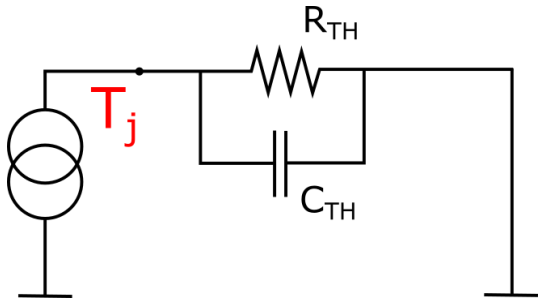


Figure 2.10: The thermal model of device in FEM model.

The lumped thermal impedance in Laplace domain is given by:

$$Z_{TH} = R_{TH} \parallel \frac{1}{sC_{TH}}$$

$$Z_{TH} = \frac{\frac{R_{TH}}{sC_{TH}}}{R_{TH} + \frac{1}{sC_{TH}}} = \frac{R_{TH}}{sR_{TH}C_{TH} + 1}$$

The inverse Laplace transform of the lumped thermal impedance becomes

$$Z_{TH} = R_{TH}(1 - e^{-\tau/R_{TH}C_{TH}}) \tag{2.31}$$

A 4-layer Foster network is used to account for the device, the solder, the copper base and the lead-frame. The equation for this 4-layer Foster network is shown below as equation 2.32.

$$Z_{TH} = R_{th1} \cdot \left(1 - e^{-\frac{\tau}{R_{th1} \cdot C_{th1}}}\right) + R_{th2} \cdot \left(1 - e^{-\frac{\tau}{R_{th2} \cdot C_{th2}}}\right) + R_{th3} \cdot \left(1 - e^{-\frac{\tau}{R_{th3} \cdot C_{th3}}}\right) +$$

$$R_{th4} \cdot \left(1 - e^{-\frac{\tau}{R_{th4} \cdot C_{th4}}}\right) \tag{2.32}$$

The values of R_{TH1} to R_{TH4} and C_{TH1} to C_{TH4} are chosen so that the thermal response of this network normalised to 1 W of input power replicates that datasheet accurately. Figure 2.10(a) shows the datasheet copy of the transient thermal impedance characteristic of the 1.2 kV/10 A SiC power MOSFET while Figure 2.10(b) shows the characteristic generated by the 4-layer network modelled in equation 2.32. The long pulse characteristic from the datasheet is used for the curve-fitting. Table 2-2 shows the values of the thermal impedances and capacitances used to achieve this matching. These values are input to the simulator and the generated thermal transients for test cases are compared with the ones derived from circuit simulators. Good agreement is achieved between both, hence, there is confidence that thermal network used in the finite element simulator is accurate.

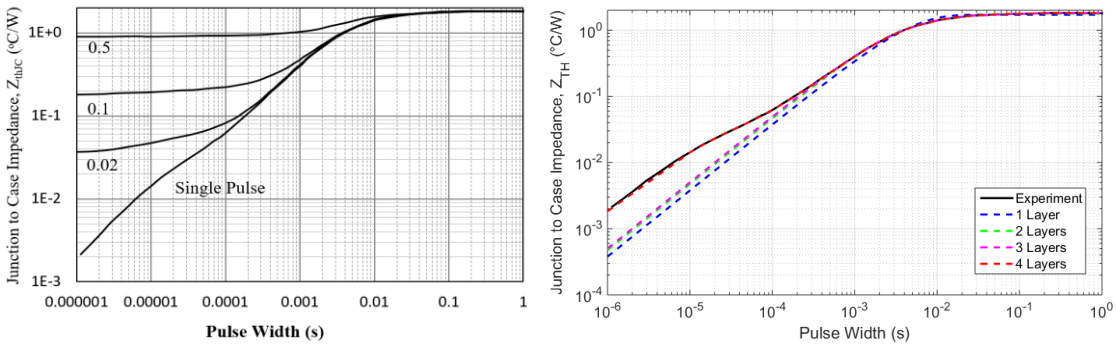


Figure 2.10(a): Transient thermal impedance with duty cycle for 10A/1.2 kV SiC MOSFET, (b) The matching curve of foster networks with different layers with the experiment result.

R_{th1}	7.852×10^{-1} K/W
C_{th1}	8.797×10^{-3} J/K
R_{th2}	1.73×10^{-2} K/W
C_{th2}	1.205×10^{-5} J/K
R_{th3}	8.351×10^{-1} K/W
C_{th3}	2.264×10^{-3} J/K
R_{th4}	1.789×10^{-1} K/W
C_{th4}	7.617×10^{-2} J/K

Table 2-2: The value of the thermal resistance and thermal capacitance in the matched foster network.

2.4 Finite Element Modelling of Power Semiconductor Devices

The mathematical model for any semiconductor device is based on fundamental physical equations that calculate the electrostatic potential and the carrier densities. These equations have been derived from Maxwell's electromagnetic laws and consist of the continuity equations, the transport equations and Poisson's Equation [26, 95]. The continuity and the transport equations calculate the evolution of electron and hole densities during the transport, generation and recombination processes.

2.4.1 Continuity equation

The continuity equations for electrons and holes are defined by:

$$\frac{\partial n}{\partial t} = \frac{1}{q} div\overrightarrow{J_n} + G_n - R_n \tag{2.33}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} div\overrightarrow{J_p} + G_p - R_p \tag{2.34}$$

where n and p are the electron and hole concentration, $\overrightarrow{J_n}$ and $\overrightarrow{J_p}$ are the electron and hole current densities, G_n and G_p are the generation rates for electrons and holes, R_n and R_p are the recombination rates for electrons and holes, and q is the magnitude of the charge on electron.

2.4.2 The Transport Equations

The charge transport models are obtained by applying approximations and simplifications to the Boltzmann Transport Equation. These assumptions can lead to several different transport models such as the drift-diffusion model, the energy balance transport model or the hydrodynamic model. The simplest and most useful model of charge transport is drift-diffusion model. This model has the attractive feature that it does not introduce other independent variables in addition to potential ψ, n and p. Until recently, the drift-diffusion model was adequate for nearly all devices that were technologically feasible.

2.4.3 Drift-diffusion Transport Model

The Boltzmann transport equation can be used to show that the drift-diffusion equations are an approximation of the current densities in the continuity equations [26]. The current densities in this case are expressed in terms of quasi-Fermi levels ϕ_n and ϕ_p as:

$$\overrightarrow{J_n} = -q\mu_n n \nabla \phi_n \tag{2.35}$$

$$\overrightarrow{J_p} = -q\mu_p p \nabla \phi_p \tag{2.36}$$

where μ_n and μ_p are the electron and hole mobilities. The quasi-Fermi levels are then linked to the carrier concentrations and the potential through the two Boltzmann approximations:

$$n = n_{ie} e^{\left[\frac{q(\psi - \phi_n)}{kT_L}\right]} \tag{2.37}$$

$$p = n_{ie} e^{\left[\frac{-q(\psi - \phi_p)}{kT_L}\right]} \tag{2.38}$$

where n_{ie} is the effective intrinsic concentration, ψ is electrostatic potential and T_L is the lattice temperature. Hence the quasi-Fermi potentials can be defined by re-writing these two equations as:

$$\phi_n = \psi - \frac{kT_L}{q} \ln \frac{n}{n_{ie}} \tag{2.39}$$

$$\phi_p = \psi + \frac{kT_L}{q} \ln \frac{p}{n_{ie}} \tag{2.40}$$

The current density equations can be obtained by substituting these equations into the expressions of current density for electrons and holes as shown:

$$\vec{j}_n = qD_n \nabla n - qn\mu_n \nabla \psi - \mu_n n\left(kT_L \nabla\left(\ln n_{ie}\right)\right) \tag{2.41}$$

$$\vec{j}_p = -qD_p \nabla p - qp\mu_p \nabla \psi + \mu_p p\left(kT_L \nabla\left(\ln n_{ie}\right)\right) \tag{2.42}$$

The final term accounts for the gradient in the effective intrinsic carrier concentration, which takes account of bandgap narrowing effects. Effective electric field are normally defined as:

$$\vec{E}_n = -\nabla\left(\psi + \frac{kT_L}{q}\ln n_{ie}\right) \tag{2.43}$$

$$\vec{E}_p = -\nabla\left(\psi - \frac{kT_L}{q}\ln n_{ie}\right) \tag{2.44}$$

hence the formulation of drift-diffusion equations can be re-written as:

$$\vec{J}_n = qn\mu_n \vec{E}_n + qD_n \nabla n \tag{2.45}$$

$$\vec{J}_p = qn\mu_p \vec{E}_p - qD_p \nabla p \tag{2.46}$$

This derivation of drift-diffusion model is based on the assumption that Einstein relationship holds. In the case of Boltzmann statistics it corresponds to:

$$D_n = \frac{kT_L}{q}\mu_n \tag{2.47}$$

$$D_p = \frac{kT_L}{q}\mu_p \tag{2.48}$$

The displacement current takes an important role in device switching or reverse biasing. The expression for displacement current is given as:

$$\overrightarrow{j_{dis}} = \varepsilon\left(\frac{\partial \bar{E}}{\partial t}\right) \tag{2.49}$$

2.4.4 Poission's Equation

In semiconductor devices, the electrostatic potential is related to space charge density by Poisson's equation:

$$div\left(\varepsilon \nabla \psi\right) = -\rho \tag{2.50}$$

where ε is the local permittivity, ψ is the electrostatic potential, and ρ is the local space charge density (sum of all mobile and fixed charges). The electric field is obtained from the gradient of the potential as:

$$\vec{E} = -\nabla \psi \tag{2.51}$$

2.4.5 Carrier Generation-recombination models

Intrinsic Carrier Concentration

The thermal generation of electron-hole pairs across the semiconductor energy bandgap determines the intrinsic carrier concentration. It can be calculated as expression:

$$n_{ie} = \sqrt{N_C N_V}\, e^{-E_G/2kT} \tag{2.52}$$

where E_G is the bandgap energy. N_C is the effective density of state in the conduction band, N_V is the effective density of state in the valence band, k is the Boltzmann's constant ($1.38\times10^{-23}\ J\cdot K^{-1}$) and T is absolute temperature in Kelvin. The carrier generation and recombination process is continuous and tends to balance under thermal equilibrium

conditions. This balance can be disturbed by external physical changes such as light, electric field and etc. However, the semiconductor will re-establish balanced generation-recombination rates when the external stimulus is removed. The rate at which generation-recombination equilibrium is re-established depends on the minority carrier lifetime in the semiconductor. The transition during the recombination process falls into main categories namely: i) Photon transitions; ii) phonon transitions; iii) Auger transitions.

Shockley-Read-Hall (SRH) Recombination

The SRH recombination model is given by:

$$U = \frac{np - n_i^2}{\tau_{p0}\left(n + N_c e^{\left(\frac{E_t - E_c}{kT}\right)}\right) + \tau_{n0}\left(p + N_V e^{\left(\frac{E_V - E_t}{kT}\right)}\right)} \tag{2.53}$$

where U is the recombination rate, n and p are the electron and hole concentration respectively, E_t is the trapping energy level, N_C is the effective density of states in conduction band, N_V is the effective density of states in valence band, k is the Boltzmann's constant ($1.38\times10^{-23}\ J\cdot K^{-1}$) and T is absolute temperature in Kelvin. τ_{p0} and τ_{n0} are the carrier lifetimes for the holes and electrons respectively which depends on impurity concentration. Hence the SRH recombination rate is concentration dependent.

Auger Recombination

The carrier density within the semiconductor increases with the on-state current density. At high current density, the auger recombination process occurs. Auger recombination occurs when electrons and holes recombine in a manner that the energy or momentum is

transferred to another mobile particle (electron or hole) by collision. The rate of standard auger recombination is given by:

$$R = \frac{n(x)}{\tau_{HL}} + C_{A\Delta n}\left[n(x)\right]^2 \tag{2.54}$$

where $C_{A\Delta n}$ is the high-level injection Auger coefficient.

2.4.6 Mobility models

As the carrier within the semiconductor is accelerated by an external electric field, it will lose momentum in various scattering processes as a result of the interaction with the steady lattice, electromagnetic interaction from ionized donors and other scattering mechanisms like surface scattering [26]. Hence, the velocity of the carrier depends on the electric field and the scattering process. At low electric fields, the carrier mobility of the semiconductor is defined as the average carrier velocity under the electric field. The mobility as a function of electric field (E) and average carrier velocity v_D is given as:

$$\mu = E / v_D \tag{2.55}$$

The energy that the accelerated carrier loses during the scattering process is transferred to other forms of energy such as thermal or light. The effective mobility relates to resistivity according to:

$$\rho = \frac{1}{q\mu N} \tag{2.56}$$

where ρ is the resistivity of a semiconductor region, μ is the majority carrier mobility (electrons in n-type region/holes in p-type region), N is doping concentration of the region

and q is the electron charge (1.6×10^{-19} C). In semiconductors, since the carrier velocity results from the electric field coupled with the different scattering mechanisms, the mobility of a carrier is a non-linear parameter. Hence, the carrier mobility is typically temperature and concentration dependent. For instance, the mobility of electrons reduces from 1350 $cm^2/V\cdot s$ to 960 $cm^2/V\cdot s$ as the doping concentration increases from 1.0×10^{14} cm^{-3} to 2.0×10^{16} cm^{-3}. While for the holes, the mobility is reduced from 495.0 $cm^2/V\cdot s$ to 434.8 $cm^2/V\cdot s$. On the other hand, the mobility generally reduces as temperature increases. Hence the resistivity of the semiconductor is a non-linear parameter that depends on the lattice temperature and doping concentration. The TCAD simulator ATLAS offers different types of mobility models based on different functions for different scenarios. For simulating low-field mobility, there are two commonly used models namely (i) constant low-field mobility model for electrons and holes and (ii) low field mobility model with lattice temperature and concentration dependency. The simulations presented in this thesis uses the latter model.

2.4.7 Impact ionization models

Impact ionization occurs when the applied reverse bias to any space charge region is sufficiently high to accelerate free carriers to a kinetic energy that exceeds the bandgap of the semiconductor. As the accelerated carriers collide with the semiconductor crystal lattice with a force greater than the bandgap, they will liberate the electron-hole pairs which will subsequently accelerate under the electric field to continue the process as in a chain reaction. This is called avalanche breakdown via impact ionisation and is the primary mechanism that limits the voltage a semiconductor can block. The general impact ionization process is described as:

$$G = \alpha_n \left|\vec{J}\right|_n n + \alpha_p \left|\vec{J}\right|_p \tag{2.57}$$

where G is the local generation rate for the electron-hole pairs, J_n and J_p are the current density for the electron and hole current, α_n and α_p are the ionization coefficients for the electron and hole respectively. The impact ionization rate is a measure of the generated carriers by each free carrier that has travelled a distance of 1 cm. The impact ionization coefficient for the semiconductor is given as [26, 96]:

$$\boldsymbol{\alpha = ae^{-b/E}} \tag{2.58}$$

where E is electric field in the same direction as current flow. The parameter a and b are constant values which are semiconductor material and temperature dependent. Due to the wider bandgap in silicon carbide, higher electric fields are needed to induce impact ionisation since a greater magnitude of kinetic energy is needed to generate the electron-hole pair. Hence, SiC devices have a higher critical electric field, which is defined as the minimum electric field applied across a semiconductor that is sufficient to induce impact ionisation. It is this greater electric field that enables high voltage blocking MOSFETs in SiC technology.

2.4.8 Heat flow equations in semiconductors

Power semiconductor devices dissipate electric power during operation thereby causing a rise in the junction temperature. Since most critical power device parameters like the threshold voltage, leakage currents, breakdown voltage and carrier mobility are all temperature dependent, this causes a coupled feedback loop between temperature and device performance. The electrical switching and on-state performance of the semiconductor coupled with the transient thermal impedance determines the junction

temperature, which in turn affects the losses. The ATLAS simulator from SILVACO offers a self-heating simulation function for circuit and device simulations. The heat flow equation for the semiconductor is given as:

$$C\frac{\partial T_L}{\partial \mathrm{t}} = \nabla\left(k\nabla T_L\right) + H \tag{2.59}$$

where C is the heat capacitance of the material (unit is $J/K/cm^3$), k is the thermal conductivity ($W/K/cm$), H is the heat generation from self-heating (W) and T_L is the transient local temperature (^oC).

2.4.9 Contact model

The power semiconductor device is interfaced with the external circuit through metallic contact materials. These contact materials are usually ohmic contacts formed between the semiconductor and a metal (usually aluminium). There are two major types of contact between a metal and a semiconductor namely (i) an Ohmic contact and (ii) a Schottky contact. The Ohmic contact is non-rectifying junction between the metal and semiconductor with fixed resistance that is usually designed to be as low as possible. This contact satisfies Ohm's law by having a linear current-voltage relationship. The Schottky contact is a rectifying junction between a metal and a semiconductor. It is able to block voltage from one direction while conducting current in another direction. In a Schottky junction contact, the electrons require energy to transit from conduction band of the semiconductor across the Schottky barrier to the metal. The Schottky barrier results from the difference between the work-function of the metal and fermi level of the semiconductor. The Schottky barrier height is defined as:

$$\Phi_{BN} = \mathrm{q}V_{bi} + \left(E_C - E_{FS}\right) \tag{2.60}$$

where Φ_{BN} is the Schottky barrier height, q is the electron charge, V_{bi} is the built-in potential, E_C is the conduction band of semiconductor and E_{FS} is the Fermi level position in the semiconductor.

2.5 Finite Element Modelling of Power Devices

2.5.1 Clamped Inductive Switching Circuit

ATLAS enables not just device simulations but also circuit simulations. Since the operational characteristics of the power devices are not just determined by the internal physics and design characteristics of the device but also on the terminal characteristics imposed by the circuit, all of the simulations in the thesis have been performed in the context of the circuit. The simulation test circuit, which is the similar to the experimental test set-up used to verify the simulations, is the clamped inductive switching circuit shown in Figure 2.11below.

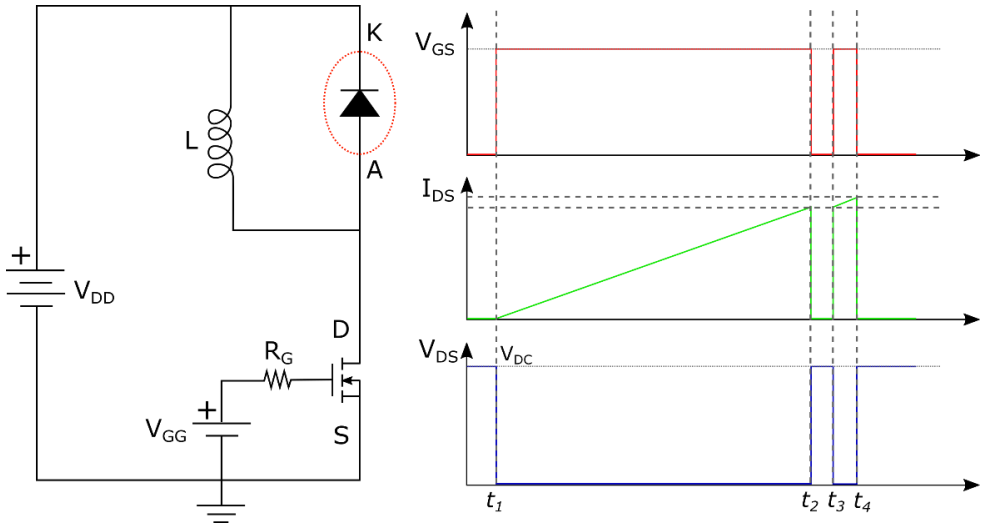


Figure 2.11: The schematic of clamped inductive switching circuit and waveforms.

Shown with the clamped inductive switching test circuit are the waveforms of the double pulse test. The clamped inductive switching circuit is comprised of a high side diode and a low side transistor. This circuit emulates a phase leg of a typical 3 phase 2 level voltage source converter in which current is commutated away from a diode by a complimenting transistor. In the double pulse test, the low side transistor is switched on between time t_1 and t_2 where the inductor is charged to a predefined current value. When the low side transistor is turned off at time t_2, current commutates to the high side diode between time t_2 and t_3. At time t_3, the low side transistor is switched on again, thereby commutating current away from the high side diode to the low side transistor. At time t_4, the low side transistor is turned OFF. During the 2nd turn-ON gate pulse on the low side transistor, the turn-ON and turn-OFF characteristics of the low side transistor and high side diode can be analysed. This simple circuit is used to analyse power transistors and diodes both from the simulations and from experimental measurements.

2.5.2 PiN Rectifier

A PiN diode model has been developed in the finite element simulator ATLAS. Figure 2.12(a) shows the PiN diode structure rated at 1.4 kV breakdown voltage. The diode has 3 regions with different doping. The P-type region is degenerately doped to inject carriers into the drift region thereby optimising high forward current conductivity. Figure 2.12(b) shows the electric field distribution along the vertical direction when the cathode voltage is at the breakdown voltage. It can be seen from Figure 2.12(b) that the electric field is highest at the P-N junction and linearly reduces with distance away from the junction. It can also be seen that the n-drift is blocking the majority of the reverse voltage (area covered by the electric field).

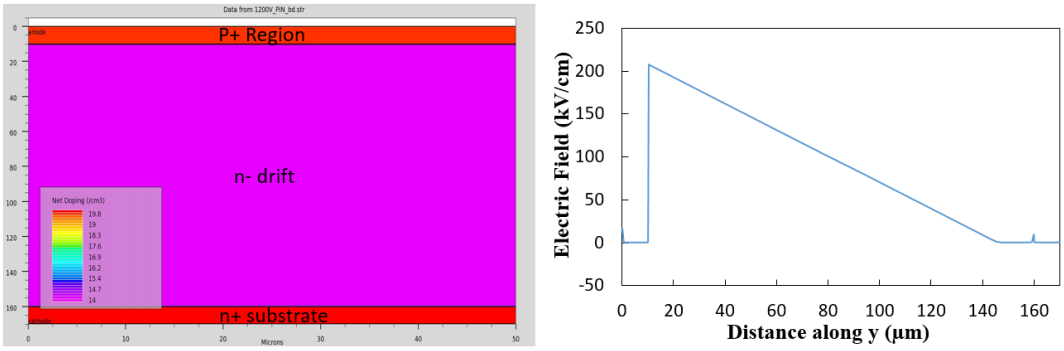


Figure 2.12: (a) the 2-D structure plot for the PiN diode and (b) Electric field distribution at breakdown voltage.

Figure 2.13 shows the carrier distribution within the drift region for different forward current. It can be seen that the carrier density within the drift region increases with the on-state current. With an increase in the carrier density in the drift region, the forward conductivity of the PiN diode increases and the on-state resistance reduces. On the other hand, the increasing carrier density will result in increased minority carrier storage which results in increased reverse recovery charge.

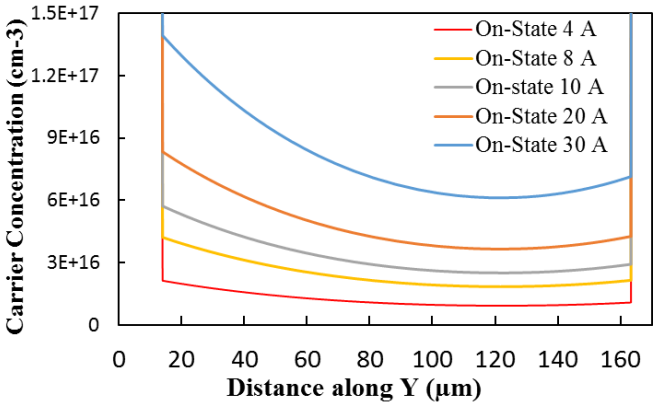


Figure 2.13: The carrier distribution for different on-state current density.

The carrier distribution profile in the drift region of the PiN diode changes during the turn-ON transient. Figure 2.14(a) shows the simulated turn-ON transient current waveform of the PiN diode with 5 time instants marked (V, W, X, Y and Z). The transient

carrier distribution profile in the drift region is extracted from the simulator and as shown in Figure 2.14(b). It can be seen from Figure 2.14(b) that the carrier concentration at the terminals of the diode increases as the current rises from point V to point Z. Figure 2.15 shows the simulated electric field across the PiN diode extracted from the simulator during the corresponding time instants during turn-ON.

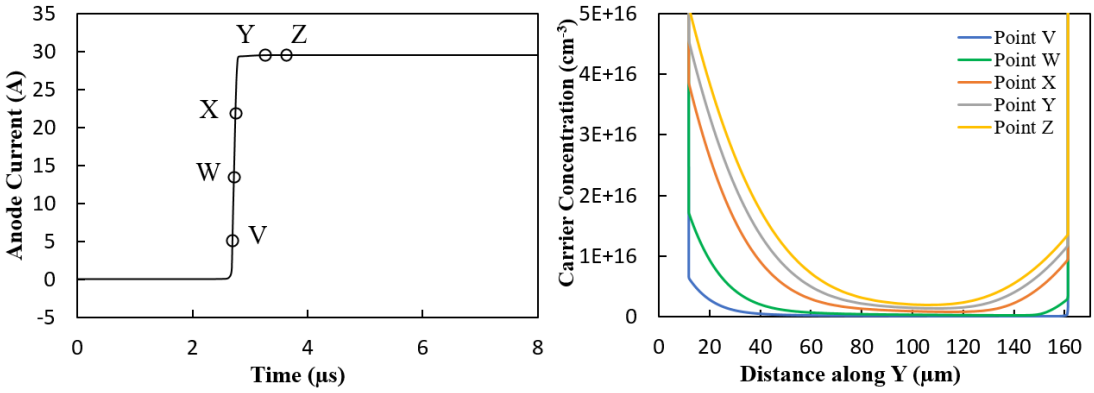


Figure 2.14: (a) The turn-On current transient waveform for the PiN diode. (b) The carrier distribution in the drift region corresponding to point V to Z in 2.14(a).

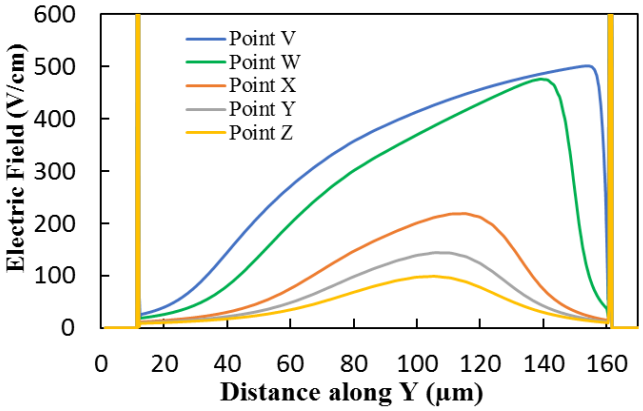


Figure 2.15: The electric field distribution in the drift region corresponding to point V to Z in Figure 2.14(a).

The reverse recovery characteristics of the diode in the clamped inductive switching circuit have been simulated using ATLAS. The reverse recovery has been simulated for different turn-OFF current commutation rates. The current commutation rate is set by the gate resistance of the low side transistor. It has been observed experimentally, that the

peak reverse recovery current increases with the turn-OFF current commutation rate (*dI/dt*) and the recombination current exhibits a snappier characteristic i.e. rapid recombination rates. This is potentially detrimental to device reliability since high recombination current rates coupled with parasitic inductance can cause dangerous over-voltages across the diode and complimenting transistor. This characteristic has been simulated in ATLAS as shown in Figure 2.16(a). Also shown in Figure 2.16(b) is the reverse recovery characteristics of the simulated PiN diode during turn-OFF of different forward currents. In these simulations, the turn-OFF current rate was held constant while the forward current was varied. It can be seen from this figure that the reverse charge increases with the forward current as was expected since the stored charge during the ON-state increases with the forward current.

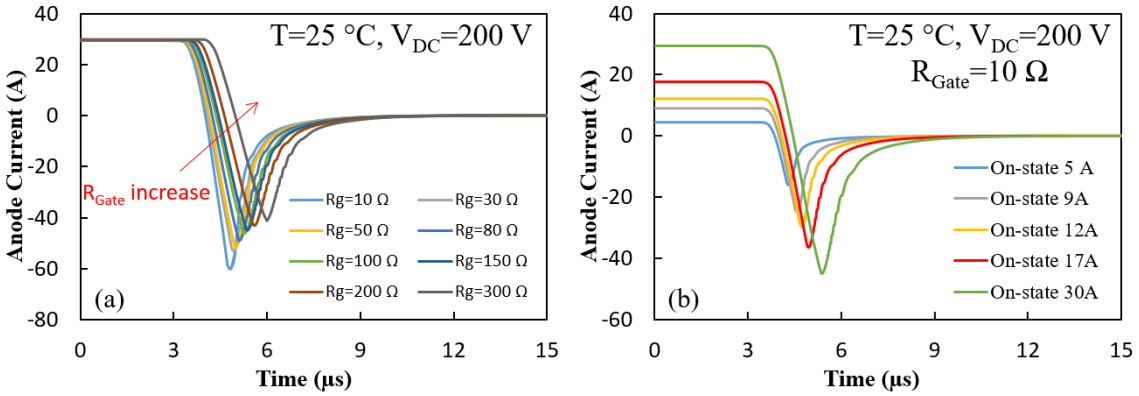


Figure 2.16: Diode reverser recovery waveform as a function of (a) switching rate and (b) forward current rating.

Shown in Figure 2.17(a) is the simulated reverse recovery characteristics of the PiN diode at different temperatures but with a fixed turn-OFF current commutation rate and fixed forward current. It can be seen that the total reverse charge increases with temperature due to the positive temperature coefficient of the minority carrier lifetime. This is a disadvantage of PiN diode rectifiers because it means that they exhibit higher losses as the junction temperature increases. Shown in Figure 2.17(b) is the reverse

recovery characteristics of the simulated PiN diode with different supply voltages. It can be seen that the reverse recovery characteristics become snappier as the supply voltage increases. This is due to the fact that increasing the supply voltage increases the extension of the depletion width into the PiN diode, thereby causing faster charge extraction and recombination.

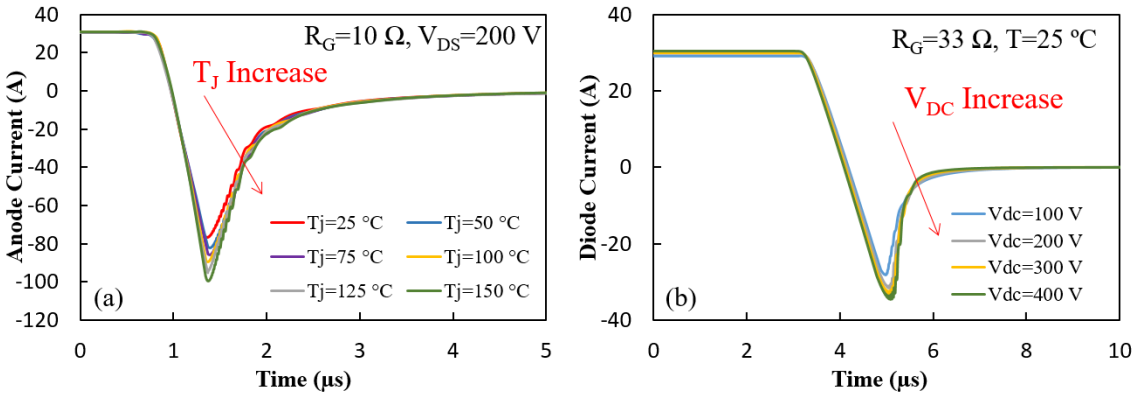


Figure 2.17: Diode reverser recovery waveform as a function of temperature and supply voltage.

The dynamic behaviour of the minority carrier distribution profile in the drift layer of the PiN diode during turn-OFF has also been modelled. Mathematical and physics-based compact models have been proposed for modelling the minority carrier distribution changes within the drift region during turn-Off, however, this is most accurately done using finite element models [97-99]. Figure 2.18(a) shows the simulated transient waveform for the PiN diode during turn-OFF with 5 time instants labelled A to E. At each of these time instants, the minority carrier distribution profile within the PiN diode has been extracted from the simulator. Figure 2.18(b) shows the carrier distribution profile corresponding to points A to E in Figure 2.18(a) where it can be seen that the carrier density is reducing during the turn-OFF. It can be seen from these plots that the catenary shape of the distribution profile at points A and B changes with the rate of change of carrier concentration with distance changing polarity at the junctions at point C. This is

due to the fact that the voltage across the PiN diode is rising at the depletion widths formed at the junctions cut-off minority carrier supply into the drift region. At points D and E, the minority carrier concentration at the anode junction becomes effectively zero. The remaining charge in the PiN diode at this point depends on the minority carrier lifetime and needs to be recombined. The rate at which this occurs will determine the snappiness of the recovery current.

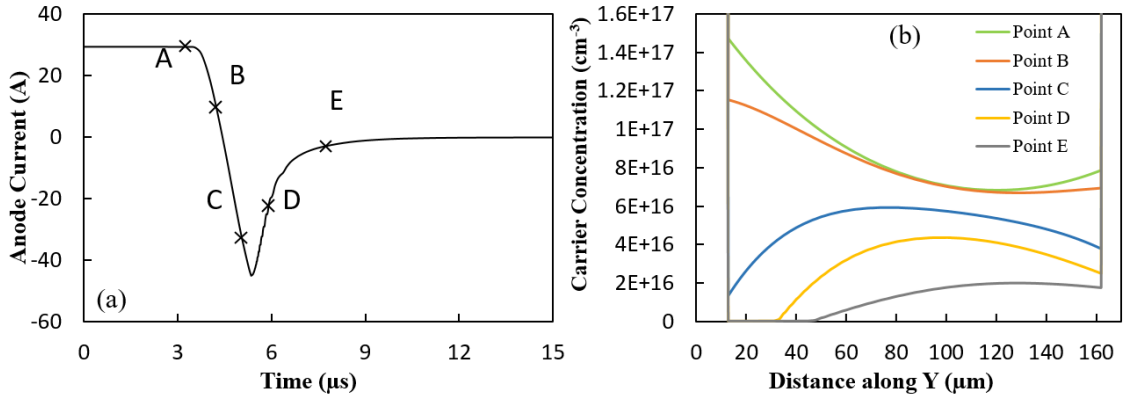


Figure 2.18: (a) Simulated Reverse recovery waveform for the PiN diode. (b) The carrier distribution within the drift region for the PiN diode corresponding to point A, B, C, D and E.

2.5.3 SiC Schottky diodes

The Schottky diode is a unipolar diode formed by a rectifying contact between a metal and a semiconductor. The difference between the work-function of the metal and the Fermi level of the semiconductor forms a barrier height that is analogous to the depletion width of a PN junction. Because there are no minority carriers in the PiN diode it does not exhibit stored charge and reverse recovery current. As a result, it is a fast switching device that exhibits small switching losses compared to PiN diodes. However, since conductivity modulation is not used during the on-state, Schottky diodes can exhibit large conduction losses resulting from the voltage blocking drift layer. As a result,

Schottky diodes are typically fabricated out of SiC and not silicon for high voltage since the wide bandgap and large critical field means that significantly thinner drift regions have can be used for blocking high voltages. The experimental evaluation of SiC Schottky barrier diodes will be described in Chapter 3. Figure 2.19(a) shows an example of a finite element simulated 900 V SiC SBD with a drift layer thickness of 5.5 µm and a drift layer n-type doping level of 1.2×10^{16} cm^{-3}. To match this breakdown voltage rating in a silicon Schottky barrier diode, a drift layer with a thickness of 50 µm and a doping of 2×10^{14} cm^{-3} is required. This will result in unacceptably high conduction losses, hence, high voltage silicon Schottky diodes are virtually non-existent. Figure 2.19(b) shows the electric field distribution of a SiC SBD reverse biased at its breakdown voltage. It can be seen that the electric field is higher close the Schottky contact and gradually reduces with increasing distance from the Schottky barrier.

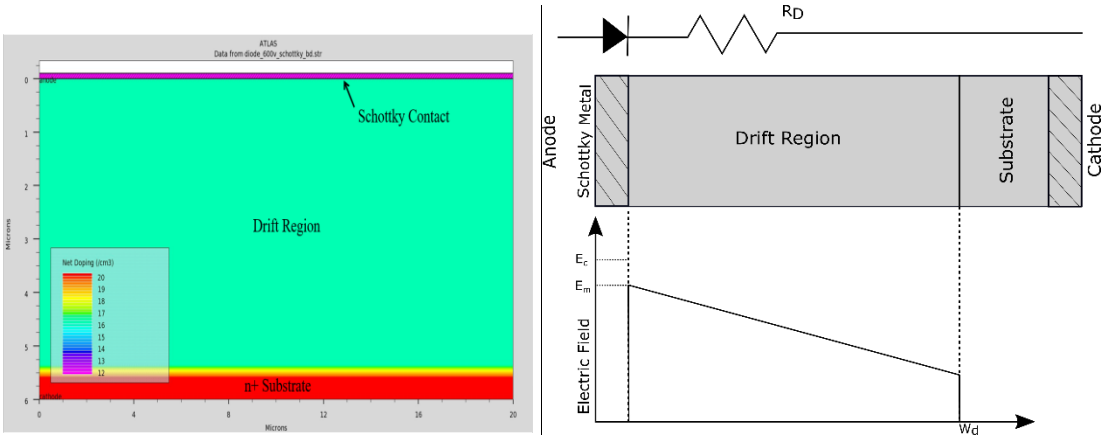


Figure 2.19: (a) The SiC Schottky diode model rated at 600V. (b) The electric field distribution at its breakdown voltage.

Since the SiC SBD is a unipolar device, it is capable of high current commutation rates (*dI/dt*) since there are no minority carriers. This gives SiC SBDs a unique advantage of operation in applications with high switching frequencies where low switching losses are required. However, this high dI/dt coupled with parasitic inductance can induce

electromagnetic oscillations (ringing) resulting from RLC resonance. This can cause additional switching losses, known as ringing losses, and may have reliability and EMI implications [58, 100-103]. This RLC resonance is formed between the parasitic inductance and the depletion capacitance formed at the Schottky junction. The Schottky junction capacitance is given by:

$$C_{AK} = A\sqrt{\frac{qN_D\varepsilon_S}{2(V_{bi} - V_{AK})}} \tag{2.61}$$

where A is the active area of the diode, V_{bi} is the build-in voltage and V_{AK} is the reverse biased voltage across the diode. Ringing in SiC Schottky diodes is a well-known problem that is exacerbated by high switching rates in the complimenting transistor. In a clamped inductive switching circuit where current commutation occurs between a transistor and a diode, the switching rate of the transistor will affect the ringing characteristics of the diode. This characteristic has been simulated by the circuit simulator in ATLAS, where a 15 *nH* inductor is connected in series with the SiC Schottky diode in the clamped inductive switching circuit shown previously in Figure 2.11. The clamped inductive switching circuit used for the double pulse test shown in Figure 2.11 is redrawn with the parasitic inductances and capacitances as shown in Figure 2.20(b) below. The parasitic capacitances are the inter-terminal capacitances of the MOSFET (C_{GS}, C_{DS} and C_{GD}) while the parasitic inductance is due to packaging. Figure 20(a) below shows finite element simulations of a SiC SBD switched with different *dI/dt* where it can be seen that the peak amplitude of the diode voltage overshoot increases as the gate resistance on the low side MOSFET is reduced, implying that the RLC resonance is less damped. Figure 2.21(a) shows actual experimental measurements performed on a 1.2 kV SiC SBD switched with a low side 1.2 kV SiC MOSFET. Both devices are from CREE with datasheet reference C2M0160120D and C4D10120A (datasheet attached in Appendix).

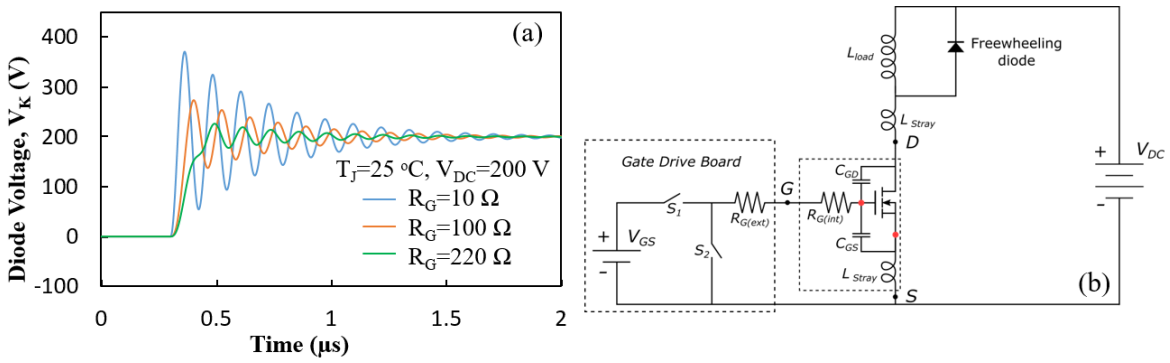


Figure 2.20: The (a) simulated turn-Off voltage and (b) simulation circuit.

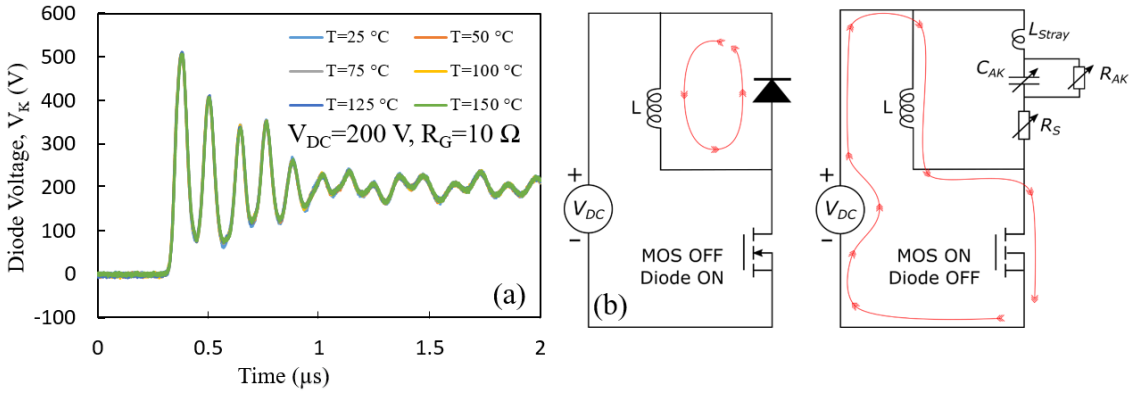


Figure 2.21: The (a) measured turn-Off voltage for the SiC SBD and (b) equivalent circuit.

It can be seen from the experimental measurements of the diode voltage that it is temperature invariant. Shown alongside the experimental measurements is the redrawn circuit diagrams of the clamped inductive switching test-rig under 2 conditions, (i) high side diode ON and low side MOSFET OFF and (ii) high side diode OFF and low side MOSFET ON. As the MOSFET is turned ON and high side diode is turned OFF, the *dV/dt* imposed across the diode sets the circuit into resonance between the diode depletion capacitance and parasitic (stray) inductance.

Figure 2.22 shows the measured turn ON and turn OFF characteristics of the SiC MOSFET illustrating the drain-source voltage (V_{DS}), drain-source current (I_{DS}), gate-source voltage (V_{GS}) and gate-source current (I_{GS}). Figure 2.23 shows the ATLAS simulated characteristics where good agreement can be seen with the measurements.

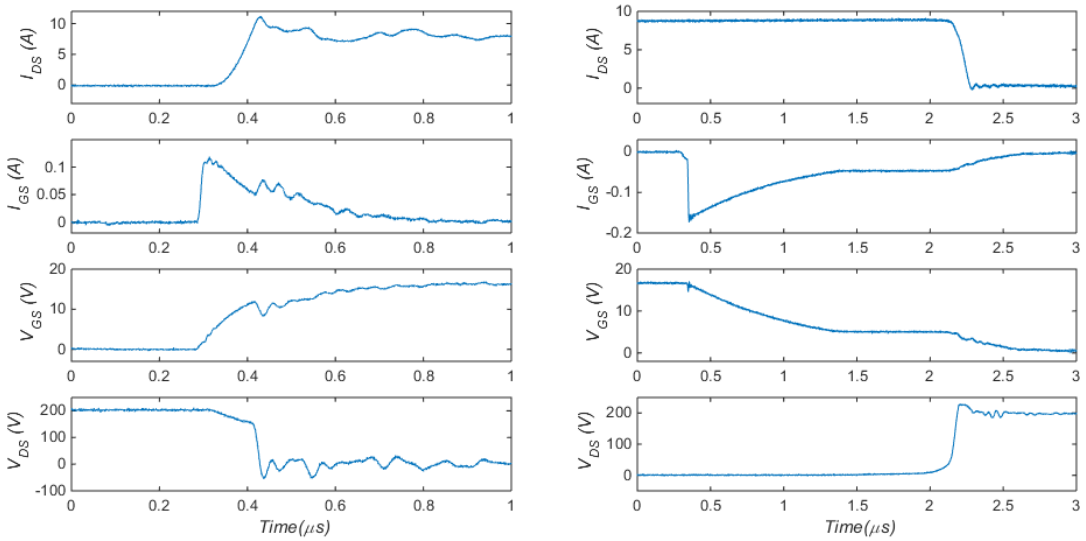


Figure 2.22: The measured (a) turn-On and (b) turn-Off transient characteristics for the SiC MOSFET.

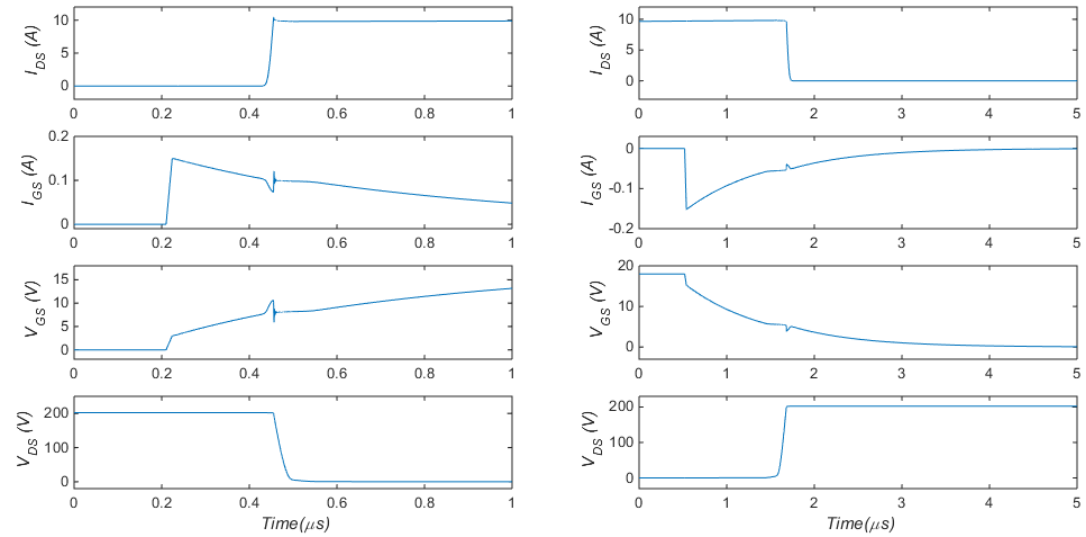


Figure 2.23: The simulated (a) turn-On and (b) turn-Off transient characteristics for the SiC MOSFET.

2.5.4 Avalanche Ruggedness under Unclamped Inductive Switching

Avalanche mode conduction is not a normal mode of operation and occurs when current is forced through a device that is turned OFF. This current is usually from an

inductor that is demagnetising itself. It can be an inductance from a machine stator winding or stray inductance resulting in voltage overshoots. When the device conducts under these conditions, it is referred to as Unclamped Inductive Switching (UIS). UIS switching is particularly stressful for the device because of the high instantaneous power dissipation resulting from simultaneously high currents through the device and voltages across the device. Hence, it can be electrothermally destructive. UIS switching of power MOSFETs is an important ruggedness concern and various innovations have improved the avalanche ruggedness of power MOSFETs under UIS [104-110]. These previous work identify the failure mode of power MOSFETs under UIS is parasitic NPN BJT latch-up. The emitter, base and collector of the parasitic NPN BJT corresponds to the source, body and drain of the MOSFET respectively as shown in Figure 2.24. The anode of the body diode is also the MOSFET source and BJT emitter while the cathode is the MOSFET drain and BJT collector.

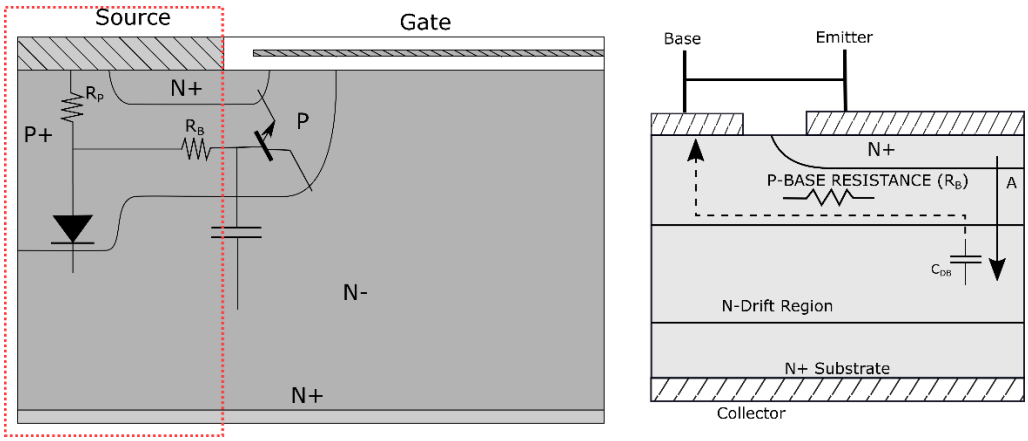


Figure 2.24: Shorted base-emitter BJT within the VD-MOSFET structure.

Since the MOSFET is OFF when current is forced through it by a de-magnetising inductance, there is no source-drain channel, hence, the current is not a drift-diffusion current. Instead, the current flows as an avalanche current via impact ionisation. As the current flows through the anti-parallel body diode, a p-body current resulting from the

liberated carriers during impact ionisation may flow across this parasitic p-body resistance. If the voltage drop arising from this p-body current is high enough to forward bias the emitter base junction of the parasitic NPN BJT, then the power MOSFET may latch with destructive consequences.

Experimental measurements and finite element simulations have been performed to further understand UIS in power MOSFETs. Figure 2.25 below shows the clamped inductive switching test rig with experimental measurements taken from a 1.2 kV/24 A SiC power MOSFET from CREE. It can be seen that the test rig is similar to the clamped inductive switching test rig except that the free-wheeling diode has been removed.

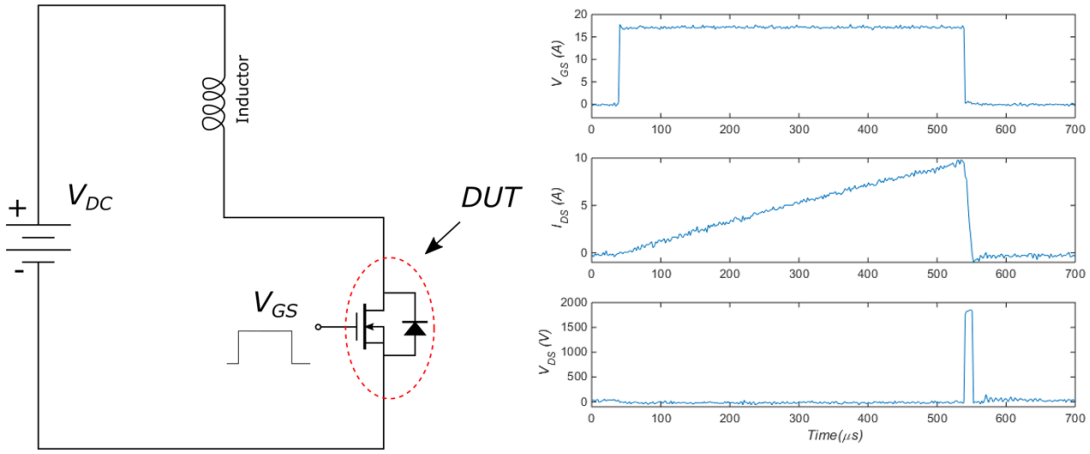


Figure 2.25: UIS test rig and avalanche measurements on a SiC Power MOSFET.

The measurements in Figure 2.25 show an initial ramping phase in the current as the low side MOSFET is switched ON and the inductor is charged. The duration of the MOSFET gate pulse determines the peak avalanche current. As the MOSFET is switched OFF, the current stored in the inductor is dissipated in the MOSFET as it conducts via avalanche mode. During avalanche mode conduction, the drain-source voltage of the MOSFET is at its breakdown voltage and the avalanche power is several kW. In the measurements shown, the peak avalanche power is approximately 40 kW.

Figure 2.26(a) below show different avalanche measurements performed on the SiC power MOSFET at different temperatures. If the device survives the avalanche pulse, the drain source current returns to zero. However, if the BJT latches and thermally destroys the MOSFET, the drain-source current rises uncontrollably as seen in Figure 2.26(a) for the higher temperatures.

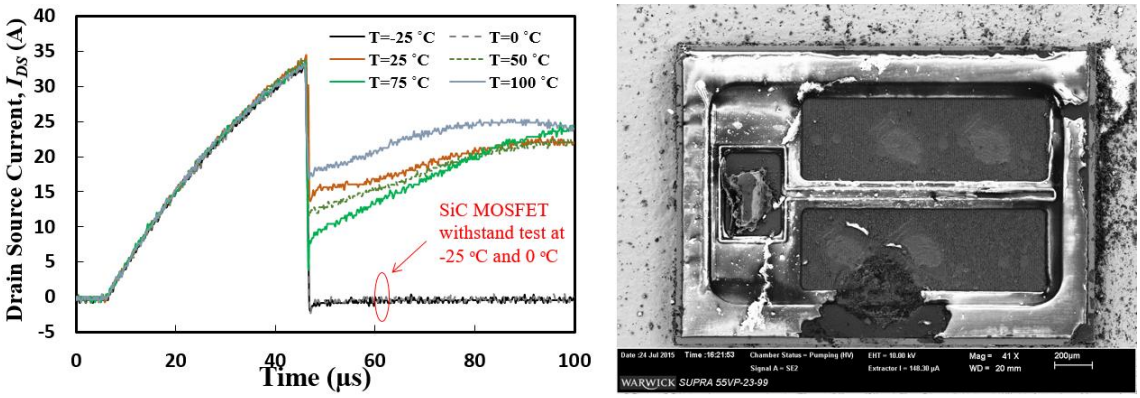


Figure 2.26: (a) UIS Measurements for a SiC Power MOSFET at different temperatures. (b) Picture of the device after BJT latch-up.

Finite element modelling has been performed for power MOSFETs under UIS in an effort to probe the internal carrier dynamics during avalanche mode conduction. Using the mixed mode circuit simulation package in SILVACO, the unclamped inductive switching test rig in Figure 2.25 has been simulated. The avalanche characteristic of the TCAD simulated both silicon and SiC power MOSFET that has failed under UIS similar to Figure 2.26 has been performed where Figure 2.27 to 2.29 shows the characteristic for the silicon MOSFET and the characteristic for the SiC is shown in chapter 5. Figure 2.27(b) shows the corresponding simulated drain-source voltage where it can be seen that it rises to the breakdown voltage during UIS. Figure 2.28(a) and 2.29(b) shows the avalanche power and highest lattice temperature of the silicon power MOSFET during the UIS event. Different points in the characteristic have been marked with point A marking the time instant when the MOSFET is in normal forward conduction mode, point

B marking the time instant when it is under UIS, point C marking the time instant when it is about to fail under UIS and point D marking the time instant when the parasitic BJT has latched and the MOSFET is failing. Figure 2.29 shows the 2-D current density contour plot and the 2-D lattice temperature plot extracted from the device simulator at point A when the MOSFET is in forward mode conduction. Figure 2.29(c) and Figure 2.29(d) shows the 2-D current density contour and lattice temperature plot for the MOSFET corresponding to point B in Figure 2.27, where it can be seen that the entire avalanche is conducting through the MOSFET body diode after the channel cuts off. Figure 2.29(e) and Figure 2.29(f) shows the 2-D current density and lattice temperature plots corresponding to point C in Figure 2.27. It can be seen here that the avalanche current starts diverting towards the NPN BJT away from the body diode. This is an indication that the NPN BJT is about the latch and the MOSFET is about to fail. Figure 2.29(g) and Figure 2.29(h) shows the 2-D current density and lattice temperature plot corresponding to point D in Figure 2.27 when the device is in full BJT latch-up. It can be seen that the current flows entirely through the NPN BJT and the lattice temperature is uncontrollably high.

The 2-D current density and temperature plots extracted from the simulator are critical for understanding the internal carrier dynamics of the device. It was observed from such Figures that the avalanche current path in the device determines whether the device fails or survives the UIS event. The 2-D lattice temperature plots show that the peak temperatures within the device occurs where the current density is highest and hence, moves from the body diode of the MOSFET to the NPN BJT.

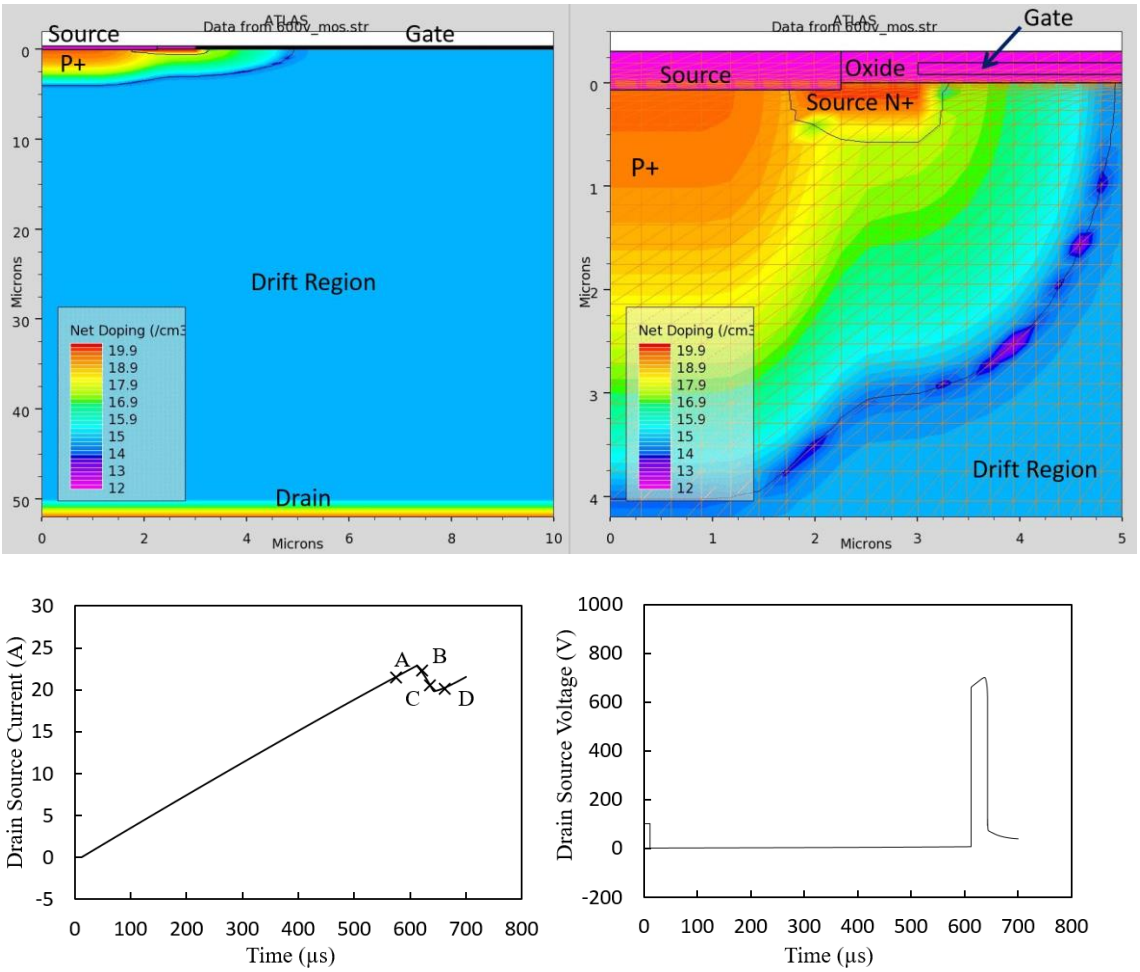


Figure 2.27: (a) The layout of the simulated 600V silicon MOSFET, (b) the simulated avalanche current for the SiC MOSFET which failed in UIS and (c) Corresponding drain voltage characteristics.

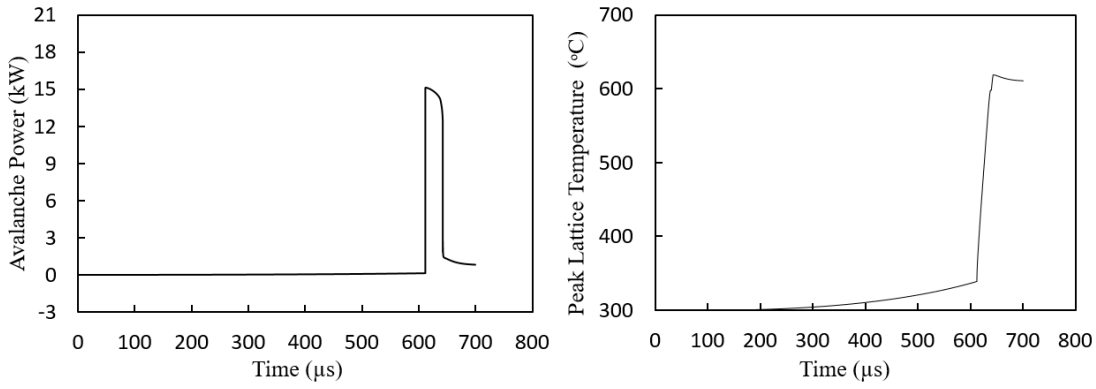


Figure 2.28: Simulated (a) Avalanche Power and (b) Highest Lattice Temperature of the Power MOSFET under UIS.

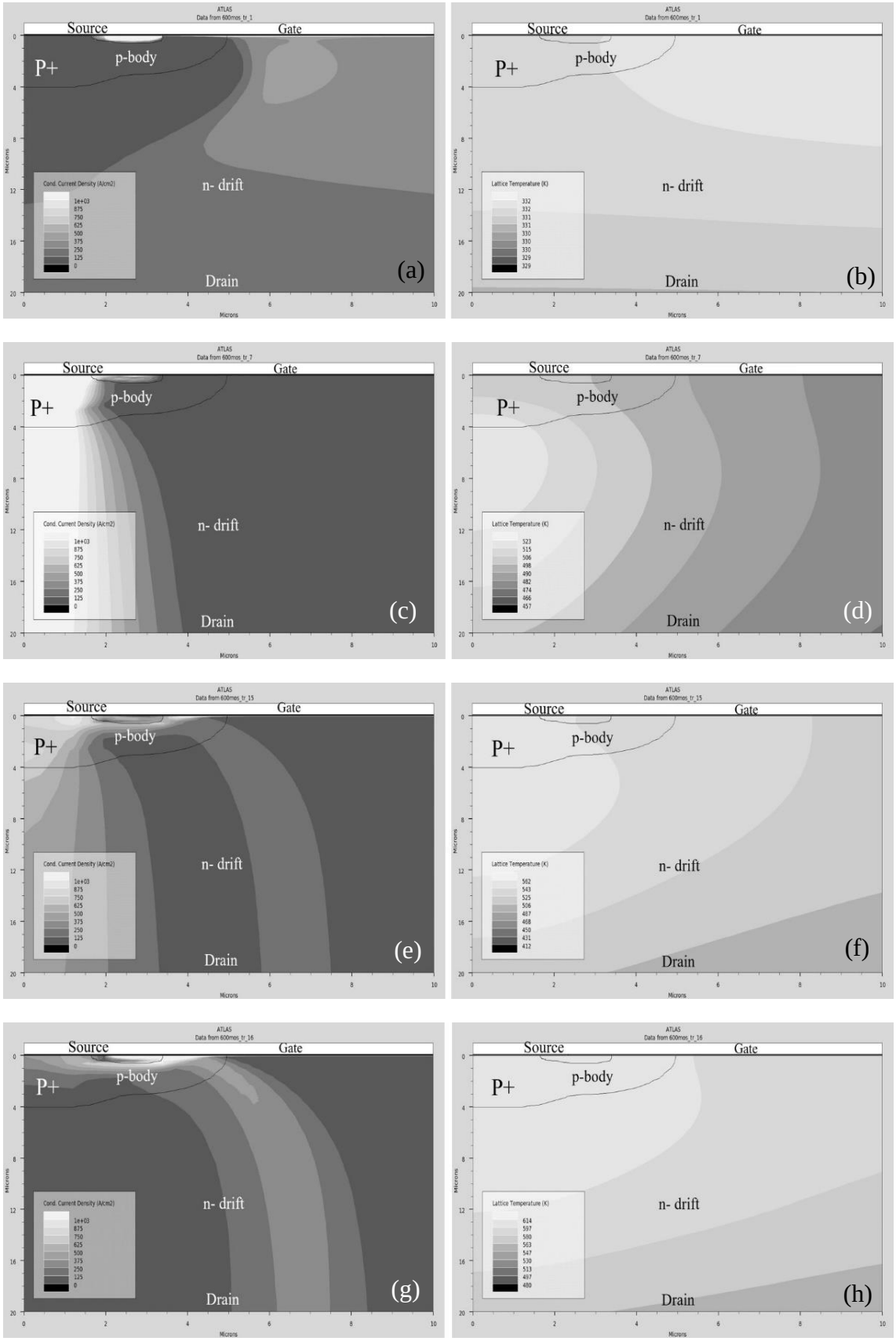


Figure 2.29: The simulated 2-D current density contour plot for the 600V silicon MOSFET corresponding to point A, B, C and D in Figure 2.27(b).

2.5.5 Unclamped Inductive Switching of CoolMOS Device

Similar finite element models where performed for the CoolMOS device. The goal is to investigate the impact of the vertical p-pillars on the avalanche ruggedness of the device. Experiments have been performed comparing the avalanche ruggedness of 600 V/20 A silicon power MOSFETs with 600 V/20 A CoolMOS devices with the same current rating. The power MOSFETs were from TOSHIBA with datasheet reference TK20E60U while the CoolMOS devices are from Infineon with datasheet reference SPW20N60S5. Previous analysis [53, 57, 111] has shown that CoolMOS devices are more avalanche rugged resulting from the additional p-pillar. The measurements here, shown in Figure 2.30 support this since the CoolMOS device survives a UIS test at a higher peak avalanche current compared to the silicon power MOSFET. The reason for this is due to the fact that there is a smaller p-body resistance in CoolMOS devices. The super-junction architecture allows for a higher p-body doping while blocking the same voltage since the electric field is spread over a wider area. Similar to the power MOSFET, 2-D current density and lattice temperature plots have been extracted from SILVACO showing the internal carrier dynamics of the device during normal forward conduction, avalanche mode and BJT latch-up mode. The simulated avalanche current and voltage characteristics are shown in Figure 2.31. Figures 2.32(a) to 2.32(f) show the 2-D current density and corresponding lattice temperature plots of the CoolMOS device. The movement of the carriers away from the body diode to the NPN BJT just before latch-up is also evident in the CoolMOS device. The higher avalanche ruggedness is due to the higher p-body doping, hence, low p-body resistance.

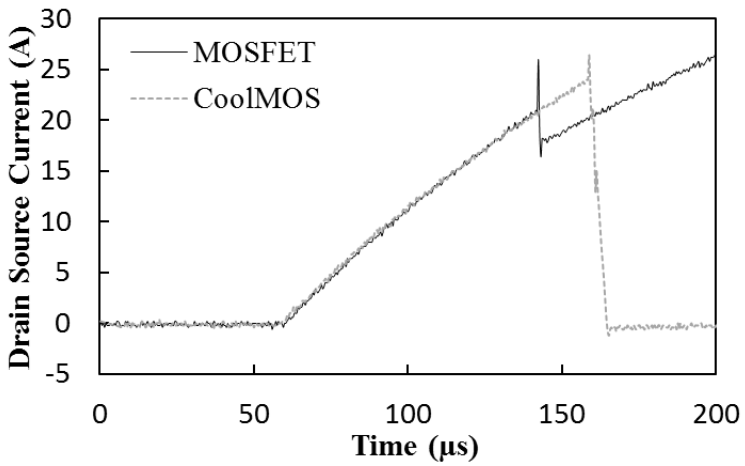


Figure 2.30: The measured UIS waveform for the CoolMOS and conventional MOSFET at room temperature.

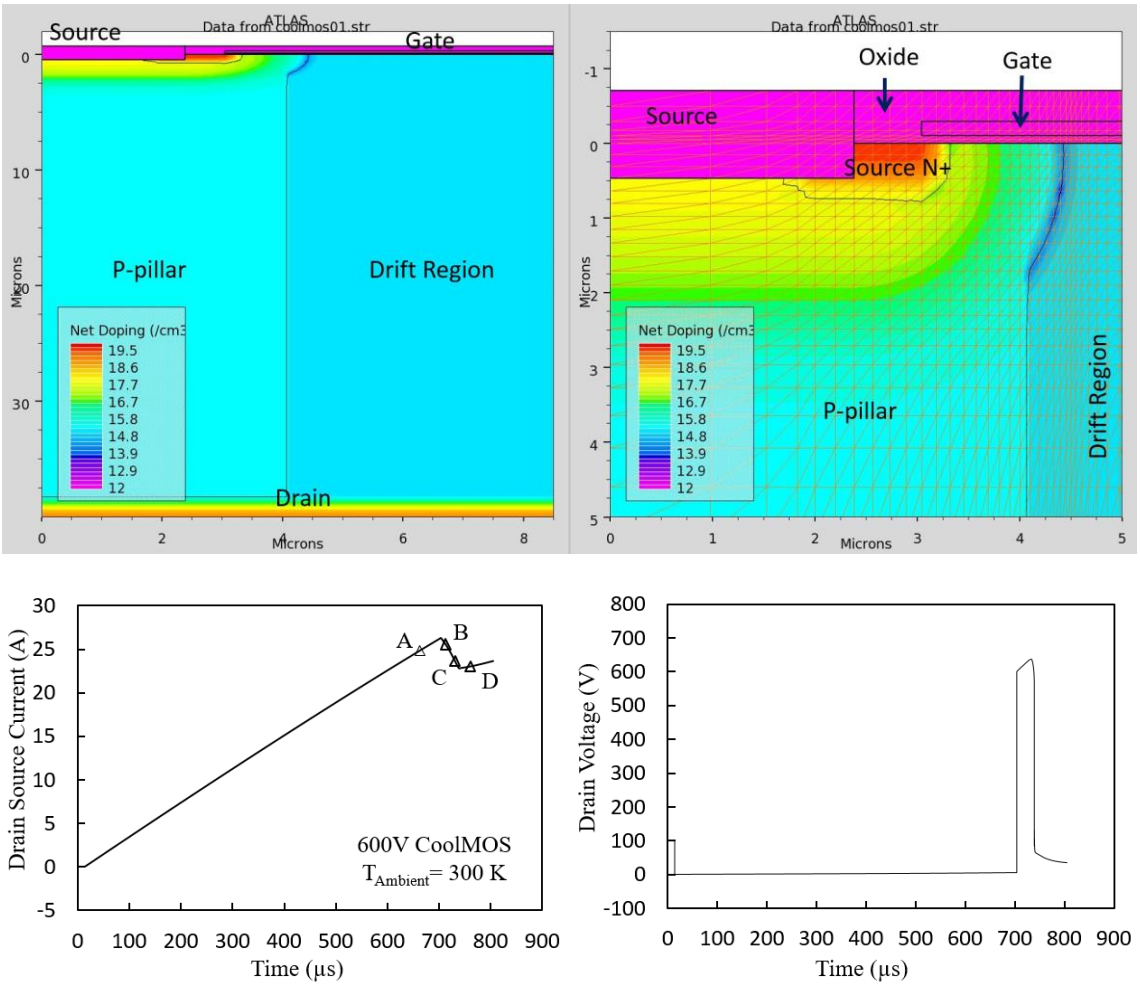


Figure 2.31: (a) The layout of the simulated 600 V silicon CoolMOS device, (b) the simulated avalanche current and (c) voltage characteristics of the CoolMOS device.

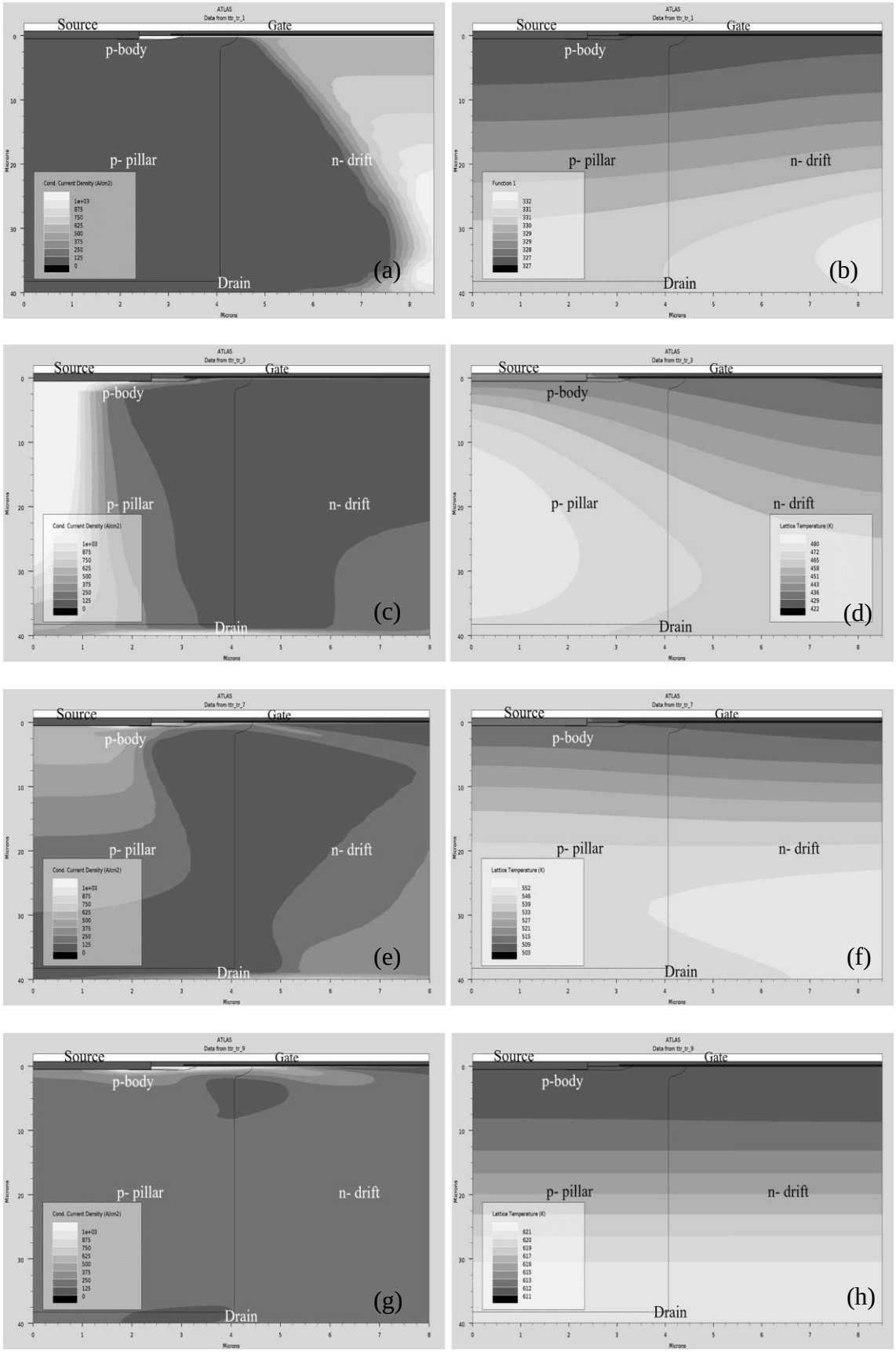


Figure 2.32: The simulated avalanche characteristic for the CoolMOS under in UIS corresponding to point A, B, C and D in Figure 2.31(b).

Chapter 3.

ANALYSIS OF ELECTROTHERMAL BALANCE IN SiC SCHOTTKY AND PiN DIODES

3.0 Introduction

In order to deliver higher current ratings, power modules are usually comprised of several parallel-connected dies. On a smaller scale, single power devices are comprised of several cells in parallel thereby sharing common terminals and delivering the rated current of the device. One method available for delivering high current rating is to use large active area dies, since the current rating is proportional to die area. However, two major problems that result from having larger die area are the higher cost resulting from lower yield (functioning devices produced per wafer) and the thermomechanical fatigue related issues exacerbated by larger dies [102, 112]. Larger die area leads to lower yield resulting from less efficient area management on the wafer. Therefore the overall cost is higher for manufacturing the larger die. Furthermore, the alternative of larger die areas is not always available in alternative semiconductor materials like SiC and GaN, where the epitaxial

growth technology, defect density control techniques and cost are still critical factors [113-115]. Thermomechanical fatigue is one of the main reliability concerns in power electronic devices and converters. In power electronic devices, the die is bonded onto a copper/ceramic substrate which thermally connects the device to the heatsink while simultaneously maintaining electrical isolation. A typical power device integrated into a power module consists of an assembly of different material interfaces for example, silicon is soldered onto a copper baseplate which sits on Al_2O_3 or aluminium nitride. These materials have different coefficients of thermal expansion (CTE), hence, will expand and contract at different rates as the conduction and switching losses of the device are dissipated. The CTE differences will cause thermo-mechanical stresses at the interfaces which ultimately result in solder joint delamination, voiding and/or cracking [112, 116]. Degradation in the solder/die attach leads to increased thermal resistance between the die and the heatsink which results in higher junction temperature since heat extraction rate is impeded. Since the stress increases with the distance from the centre of the die, larger die are prone to higher failure rate than smaller dies [102, 117]. Hence, in some cases, it may be more desirable to have smaller dies connected in parallel rather than having a single larger chip.

When connecting power devices in parallel, the temperature characteristics of each device is critical in determining how well the parallel connection can maintain electrothermal equilibrium. Generally, it is desirable for devices to exhibit an electrical conductivity with a negative temperature coefficient so that less current is conducted as temperature increases. If the electrical conductivity of the device decreases with temperature, then the device is inherently electrothermally stable in so far as it is not conducting current from a constant current source. On the other hand, if the electrical conductivity of a power device increases with temperature, then it is prone to thermal

runaway since the device conducts more current as the junction temperature increases i.e. positive feedback loops are inherently less stable than negative feedback loops. The temperature coefficient of a power diodes electrical conductivity depends on where in the output characteristic the device is operating. The equation for the forward voltage of the Schottky diode is the sum of the Schottky contact junction voltage (determined by the metal-semiconductor barrier height) and the voltage drop along the total series parasitic resistance comprising of the drift resistance, substrate resistance and contact resistance. The forward voltage is given by [26]

$$V_F = \frac{KT}{q}\ln\left(\frac{J_F}{J_S}\right) + (R_{drfit} + R_{SUB} + R_C)J_F \qquad (3.1)$$

The 1st term in equation (3.1) has a negative temperature coefficient while the 2nd term has a positive temperature coefficient. At low forward current densities, the first term in equation (3.1) dominates meaning that the forward voltage decreases with increasing temperature. However, as the current density increases, the 2nd term dominates meaning that the temperature coefficient of the forward voltage changes from negative to positive. The zero-temperature coefficient in the output characteristics is the current at which forward voltage becomes temperature invariant. PiN diodes also exhibit similar temperature dependent characteristics with the temperature coefficient of the forward voltage changing from negative to positive as the forward current density increases. PiN diodes are minority carrier bipolar devices that rely on conductivity modulation from minority carrier injection to achieve low conduction losses [97]. For this reason, slow switching transients and reverse recovery currents due to stored charge are characteristic disadvantages of PiN diodes. On the contrary, Schottky diodes are majority carrier unipolar device that rely on the drift of majority carriers under the influence of an electric field. Hence, Schottky diodes are usually implemented in SiC technology so as to

minimize the thickness and resistivity of the drift layer [26]. Over the years, the switching performance of PiN diodes have been improved by minority carrier lifetime engineering [118]. This is achieved by introducing recombination centres in the drift region of the diode thereby minimizing the reverse recovery characteristics by reducing minority carrier lifetime. Based on this, fast recovery diodes have been designed and released.

Due to the fact that both devices operate under different physical principles, the electrothermal performance of each device is different with respect to the other. Because the energy bandgap of the semiconductor reduces and minority carrier lifetime of the diffusing carriers increases with temperature, the carrier density in the drift region plasma increases with temperature thereby causing a negative temperature coefficient between the on-state resistance and temperature. In Schottky diodes, the on-state voltage decreases with temperature initially (due to thermally induced bandgap narrowing) but later increases with temperature because of the resistance of the drift region. The zero-temperature coefficient (ZTC) point is the drain current at which the reduction in the energy bandgap is exactly counter balanced by the resistance of the drift region i.e. the forward voltage is temperature invariant. As a result of conductivity modulation in the PiN diodes, there is a higher ZTC point in the output characteristics compared to SiC Schottky diodes. The ZTC point is important when paralleling devices so as to ensure stable electrothermal operation.

It is also important to investigate the impact of electrothermal imbalance on the robustness of parallel-connected diodes under unclamped inductive switching (UIS) conditions. Under UIS conditions, the current through the diode and the voltage across the diode are simultaneously high thereby causing very significant instantaneous power dissipation capable of thermally destroying the devices. In this case, the diode conducts an avalanche current under reverse bias conditions when it is blocking voltage.

Differences in the initial junction temperature of the parallel-connected diodes will likely degrade the overall electrothermal ruggedness of the parallel pair, however, this has yet to be quantified. These differences can arise as a result of different thermal resistances due to different stages of thermo-mechanical degradation.

In this chapter, the impact of electrothermal imbalance between parallel-connected silicon PiN and SiC Schottky diodes is investigated under clamped and unclamped inductive switching conditions. The impact of the diode technology on the complimenting transistor is assessed together with a comparative electrothermal analysis of both diodes. In this chapter, the impact of the diode on the thermal stresses of the complimenting transistor is analysed. The impact of electrothermal balance is investigated for both SiC Schottky and silicon PiN diode technologies by introducing temperature variation as well as thermal resistance variation. The impact of the diode's electrothermal performance on the complimenting transistor is assessed by double pulse and repetitive switching in a clamped inductive switching test rig with a low side SiC MOSFET. Section 3.1 presents the experimental measurements and a comparison of steady state and dynamic electrothermal performance of standalone PiN and SiC Schottky diodes in clamped inductive switching circuit. Section 3.2 to Section 3.4 presents the experimental measurements of parallel-connected silicon PiN and SiC Schottky diodes in a clamped inductive switching circuit with balanced and unbalanced electrothermal conditions. Section 3.5 presents the experimental measurements of silicon PiN diodes and SiC Schottky diodes in an unclamped inductive switching circuit (UIS) again with balanced and unbalanced electrothermal conditions. Section 3.5(d) introduces the finite element simulation of the standalone silicon PiN diode as well as parallel-connected PiN diodes in an unbalanced parallel connection. Similar finite element simulations for a SiC

Schottky diode were done so as to understand the physics behind device failure and the impact of electrothermal imbalance under unclamped inductive switching.

3.1 The experimental set-up

The experimental circuit schematic and set-up is shown in Figure 3.1(a) for the clamped inductive switching experiments and Figure 3.1(b) for the unclamped inductive switching experiments. The clamped inductive switching test set-up consists of 2 parallel diodes acting as the free-wheeling diodes. The diodes under investigation in this chapter are 600V/15A silicon PiN diodes from International Rectifier with datasheet reference 15ETH06 and 600V/9A SiC CREE Schottky diodes with datasheet reference C3D06060. The low side conducting device is a 1.2 kV SiC MOSFET from CREE with datasheet reference CMF20120D. Electric-hot plates are available so that the diode junction temperatures can be varied and pre-set at different temperatures. Steady state behaviour is evaluated by the double pulse measurement while the transient thermal behaviour is measured by repetitive switching until steady-state temperature is reached. In the double pulse measurement, the MOSFET initially switched on so as to charge the inductor to a pre-defined current which is determined by the duration of the gate pulse. When the MOSFET is turned off, the current in the inductor commutates to the free-wheeling diodes which are the devices under test (DUTs). When the MOSFET is switched on for the second time, the diodes turn-off and the switching characteristics can be assessed.

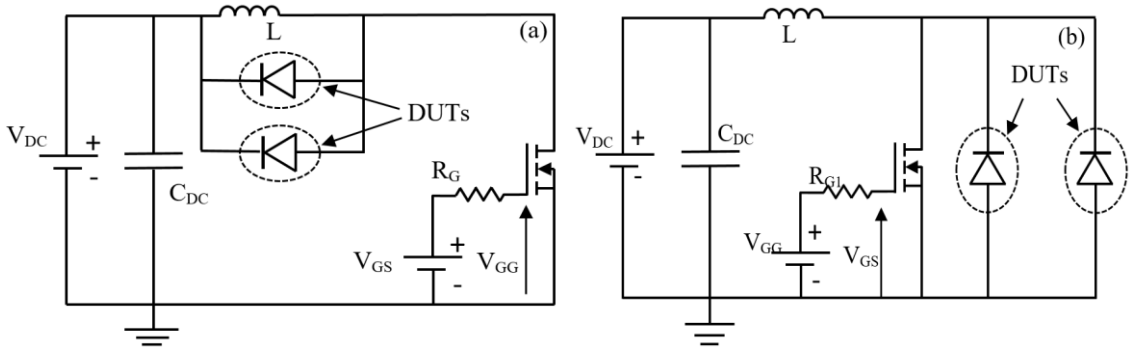


Figure 3.1: (a) the clamped inductive switching schematic and (b) unclamped inductive switching schematic.

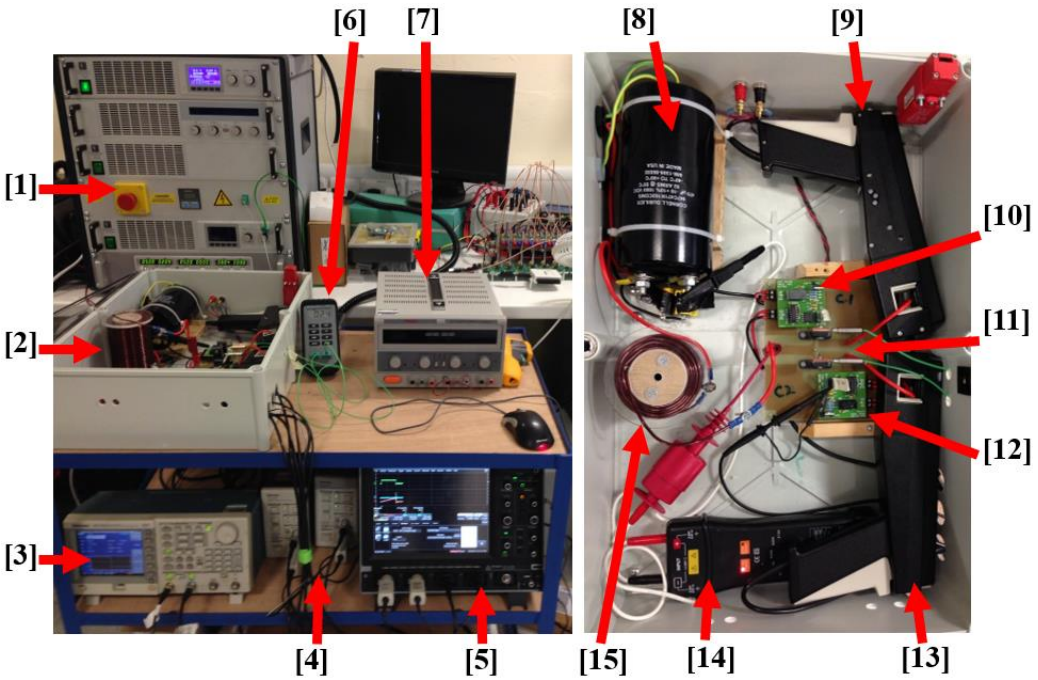


Figure 3.1(c): A photograph of the experimental set-up with [1] DC Power Supply. [2] Test Chamber. [3] Function Generator. [4] Current probe Amplifier. [5] Oscilloscope. [6] Inductor. [7] Differential voltage probe. [8] Voltage probe. [9] and [14] Current Probes. [10] and [11] Device Under Test (DUT). [12] Drive MOSFET. [13] Gate Drives. [15] DC capacitor. [16] DC power supply for heater. [17] Thermometer.

Electrothermal imbalance between the parallel-connected DUTs can be introduced by using different heatsinks or by using the electric heaters to set different initial junction temperatures. The heatsinks are used to test the impact of electrothermal imbalance on the transient/steady state thermal response of the diodes under repetitive switching. As an

advantage of fixed plug-in sockets on print circuit board (PCB), the DUTs are fixed in mounted, thereby the stray inductance in the circuit is the same for DUTs with or without additional heatsinks.

Figure 3.1(b) shows the test circuit and picture for the unclamped inductive switching test rig comprising of the driving transistor connected in parallel with the DUTs. In this circuit, the transistor is a high voltage (1.7 kV) device that is used to drive current through the inductor. The duration of the gate pulse of the driving transistor is used to set the peak avalanche current. The parallel connected DUTs (diodes) have a lower breakdown voltage rating (600 V) than the driving transistor. This is done to ensure that the inductor dissipates the current through the diodes and the driving transistor does not conduct any of the avalanche current i.e. the current always flows through the device with the lower breakdown voltage. When the transistor is switched ON, current flows through the inductor from the power supply and the current ramps up linearly in so far as the inductor is not saturated. When the transistor is switched OFF, the current stored in the magnetic field of the inductor is dissipated through the parallel-connected diodes since they have a lower breakdown voltage rating than the transistor. The maximum avalanche current capable of causing thermal destruction of the diodes is determined by varying the gate pulse of the driving transistor. This is done incrementally until the DUTs conducting current in avalanche are thermally destroyed. The experiment is repeated at least 3 times so as to remove statistical anomalies.

3.2 Silicon PiN diodes and SiC Schottky diodes under Clamped Inductive Switching Measurements

a. Silicon PiN diodes in CIS measurements

PiN diodes typically have lower-conduction energy dissipation but higher switching losses at higher temperatures. PiN diode is a bipolar device that relies on the conductivity modulation from minority carrier injection into the depletion region of the device to increase the on-state conductivity. The on-state conductivity of the PiN diode improves with the temperature rise as a result of increased carrier lifetime. Although carrier lifetime has a positive coefficient of temperature, however, the switching energy loss increases as the reverse recovery charge increases with an increase in the carrier lifetime. When the diode turns off, the reverse recovery charge is extracted as a negative current before the diode starts blocking.

The switching behaviour of PiN diodes were measured by the previously described double pulse testing scheme, in which the anode cathode current (I_{AK}), anode cathode voltage (V_{AK}), current passing through the 1200V/10A MOSFET (I_{DS}) and voltage across the MOSFET (V_{DS}) are measured during the switching. A heater with thermocouple is attached to the backside of the device in order to set the initial operation temperature of the device. Figure 3.2 shows the transient switching waveforms of a single diode switched at junction temperature of 50 °C where (a) shows the turn on transient of the diode and (b) shows the turn off transient of the diode. As can be seen from Figure 3.2 (a), it takes approximate 0.5 µs for the diode current to reach the steady state during the turn on thus the energy loss during this period is considered as the turn on energy loss. Figure 3.2 (b) indicates that the reverse recovery of PiN diode significantly contributes to the switching energy loss compared with the turn-ON waveforms. This is due to the overlap between

the voltage and the current waveforms which shows a significant power loss during the turn-off. This power loss contributes to temperature rise in both the diode and the MOSFET.

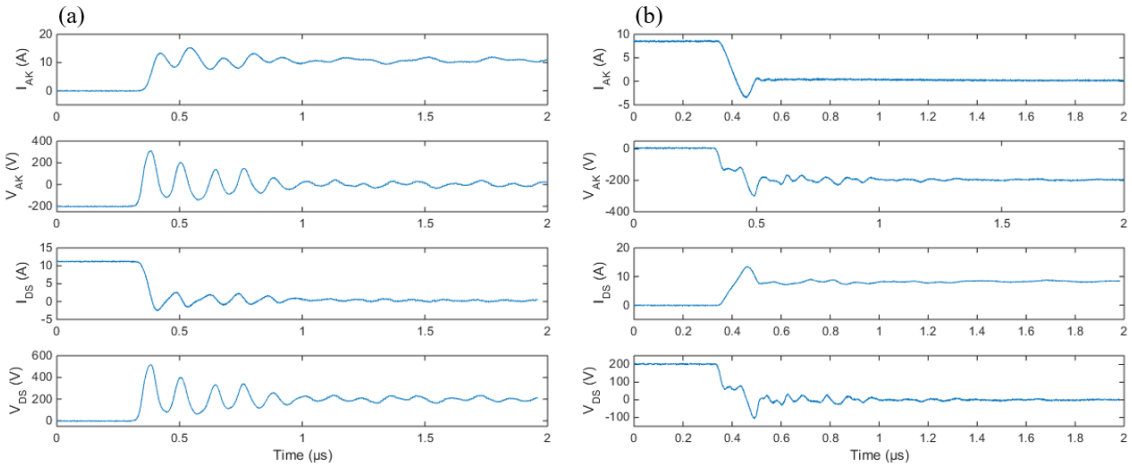


Figure 3.2: The measured (a) turn-ON and (b) turn-OFF transient waveform of power PiN diode in a clamped inductive switching measurement.

It can be seen from the PiN diode turn-off transient characteristics in Figure 3.2(b) that the reverse recovery current in the PiN diode contributes to turn-on switching energy of the MOSFET since the drain-source current increases in proportion to the reverse recovery current. Figure 3.3 shows the transient waveforms of the (a) diode current I_{AK}, (b) diode voltage V_{AK} (V_{ANODE}-$V_{CATHODE}$), (c) the gate source voltage of MOSFET V_{GS} and (d) the gate current during MOSFET turn-ON which is diode turn-OFF. Figure 3.3(a) shows that the peak reverse recovery current increases with temperature as a result of the increase in the minority carrier lifetime with temperature. This leads to higher reverse recovery charge during turn-off. Figure 3.3(b) shows the voltage across the diode at different junction temperatures, where it can be seen that the peak voltage overshoot increases with temperature in a similar fashion as the peak reverse recovery current increasing with temperature in Figure 3.3(a). It can also be observed that the voltage overshoots during the diode turn-OFF occurs at approximately 0.5 μs. As shown in Figure

3.3(c), the gate source voltage experiences oscillations at 0.5 μs during turn-ON which occurs at the same time instant that the reverse recovery current in the diode shown in Figure 3.3(a) decreases rapidly from its peak value to zero. In Figure 3.3(d), it can be seen that the gate current experiences a sudden rise followed by damped oscillations.

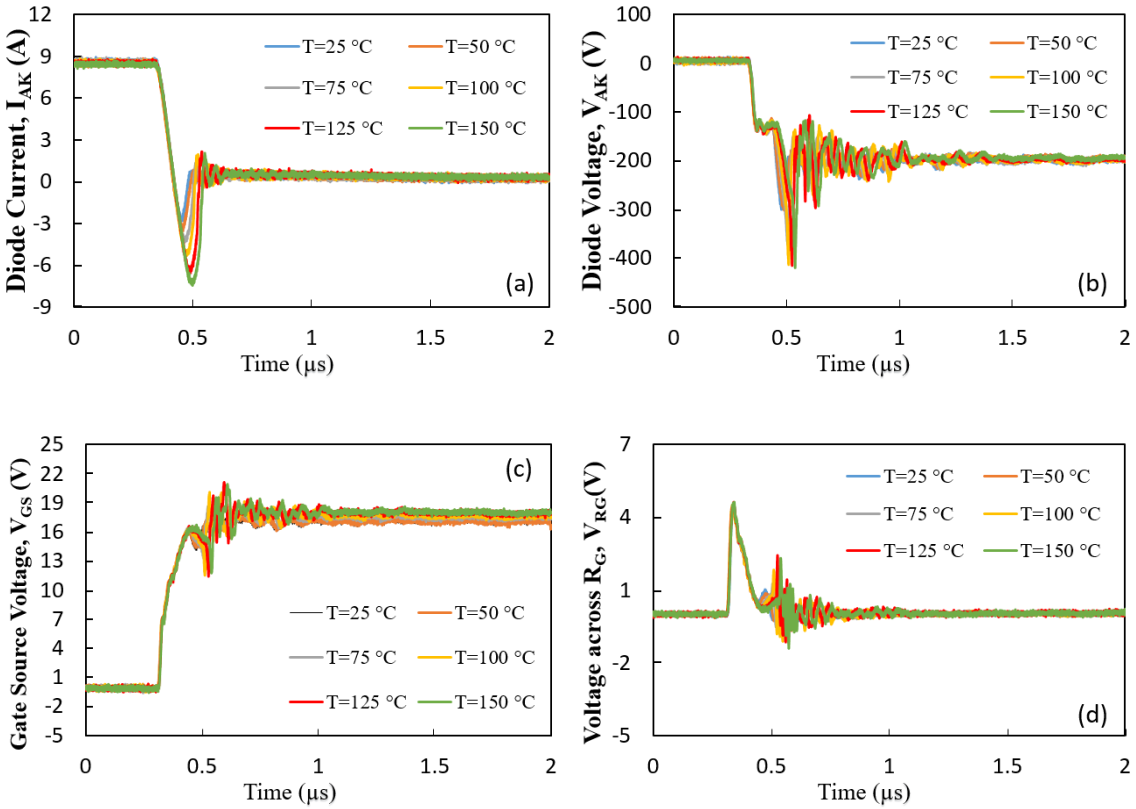


Figure 3.3: The measured turn-OFF transient waveform of Silicon PiN diode showing the Transient Characteristics of the (a) I_{AK}, (b) V_{AK}, (c) V_{GS} and (d) I_G.

The diode voltage overshoot in Figure 3.3(b), gate voltage oscillation in Figure 3.3(c) and the gate current oscillations in Figure 3.3(d) all result from the high dI_{AK}/dt of the recombination current in Figure 3.3(a). As the temperature is increased, the peak reverse recovery current increases, which results in faster carrier extraction through higher recombination rates. This high dI_{AK}/dt combines with the parasitic series source inductance from the MOSFET wire-bonds and results in a high source voltage that temporarily rises beyond the threshold voltage of the MOSFET thereby turning it OFF

unintentionally. As the MOSFET is parasitically turned-OFF, the changing dV_{DS}/dt across the MOSFET coupled with the Miller capacitance causes a gate current which is evident in Figure 3.3(b). This temperature induced parasitic turn-OFF is unique to PiN diodes because of the reverse recovery characteristics and can be detrimental to the reliability of the complimenting driving transistor.

b. SiC Schottky diode in CIS measurement

Similar measurements have been carried out for SiC Schottky diodes. Figure 3.4 shows the measured transient waveforms for diode current (I_{AK}), diode voltage (V_{AK}), complimenting driving MOSFET current (I_{DS}) and voltage (V_{DS}). The measurements were performed at a diode junction temperature of 50 °C. The SiC Schottky diode has similar turn-on waveform to the silicon PiN diode as can be seen in Figure 3.4(a). By comparing the turn-off waveform shown in Figure 3.4(b) for the SiC Schottky diode and Figure 3.2(b) for the silicon PiN diode, the reverse recovery current and the voltage oscillation is significantly smaller for the SiC Schottky diode. This consequently induces less losses during turn-on of the lower side MOSFET. It also can be seen from Figure 3.4 that there exist a voltage plateau during turn-Off which is caused by the high stray inductance of the SiC Schottky diode.

Figure 3.5 illustrates the measured transient waveform of I_{AK}, V_{AK}, V_{GS} and I_G during the turn-ON transient of the driving MOSFET. As can be seen in Figure 3.5(a) to (d), the switching waveforms are temperature invariant. This is due to the previously discussed wide bandgap characteristics of SiC From the perspective of the complimenting driving transistor, there is less of a reliability concern when the free-wheeling diodes are Schottky diodes instead of silicon PiN diodes.

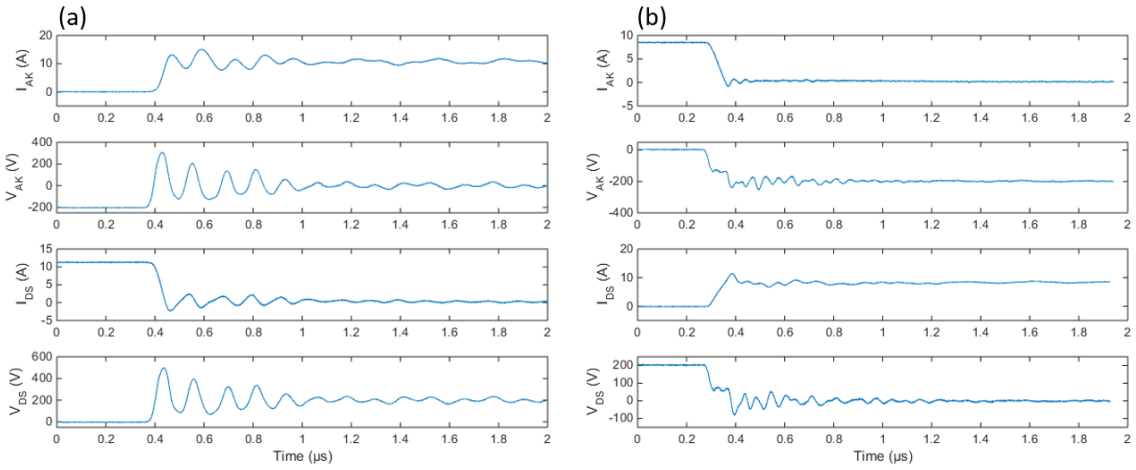


Figure 3.4: The measured (a) turn-ON and (b) turn-OFF transient waveforms of SiC Schottky diode in clamped inductive switching measurement.

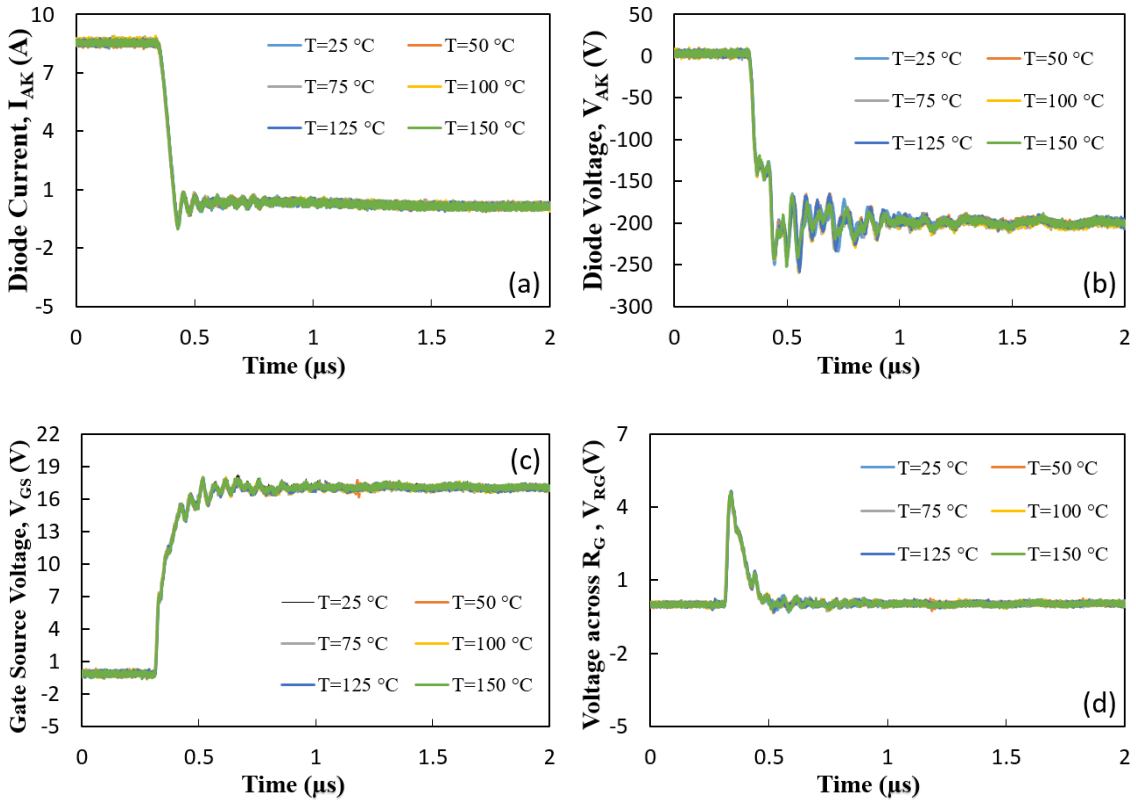


Figure 3.5: The measured turn-OFF transient waveform of the SiC Schottky diode showing (a) I_{AK}, (b) V_{AK}, (c) V_{GS} and (d) I_G.

c. Comparisons of Thermal Transients in Silicon PiN and SiC Schottky Diodes under Repetitive Clamped Switching

Figure 3.6 shows the measured low side SiC MOSFET current when the diode is operating at different junction temperatures for the (a) silicon PiN diode and (b) SiC Schottky diode. Figure 3.6(a) shows that the current overshoot in the SiC MOSFET increases with temperature while Figure 3.6(b) shows that the SiC MOSFET switched with the SiC Schottky diode shows no significant change with temperature. It is clear from Figure 3.6(a) that the PiN diode reverse recovery current contributes to the turn-ON current overshoot in the SiC MOSFET and the positive temperature coefficient of the reverse recovery charge makes this overshoot worse. This is responsible for the higher steady-state case temperatures in the SiC MOSFET in the PiN diode test compared with the Schottky diode test. Figure 3.7(a) shows the turn-ON switching energy while Figure 3.7(b) shows the turn-OFF switching energy of the SiC MOSFET as a function of the diode temperature for both the silicon PiN diode and the SiC Schottky diode. It should be noted that the temperature of the driving SiC MOSFET is held constant while the temperature of the diode is varied. It can be seen from Figure 3.7(a) that the turn-ON switching energy of the SiC MOSFET is 34.4% higher when switched with the PiN diode than when switched with the Schottky diode at 25 °C. As the diode temperature is increased to 150 °C, the turn-ON energy of the SiC MOSFET with the PiN diode becomes 229.2% higher than when the SiC MOSFET is switched with the Schottky diode. Figure 3.7(b) shows that this is also the case for the turn-OFF switching energy. However, the difference in the switching energy is not as much as the case of the MOSFET turn-ON because of the absence of the reverse recovery characteristic of the diode.

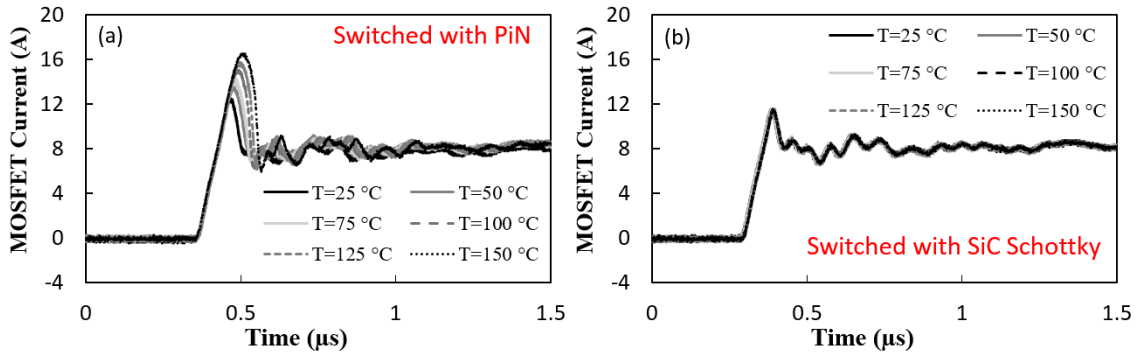


Figure 3.6: The measured turn-on waveform of the driver MOSFET switched with (a) PiN diode operating at different temperatures. (b) Similar measurement for the MOSFET switched with SiC Schottky diode.

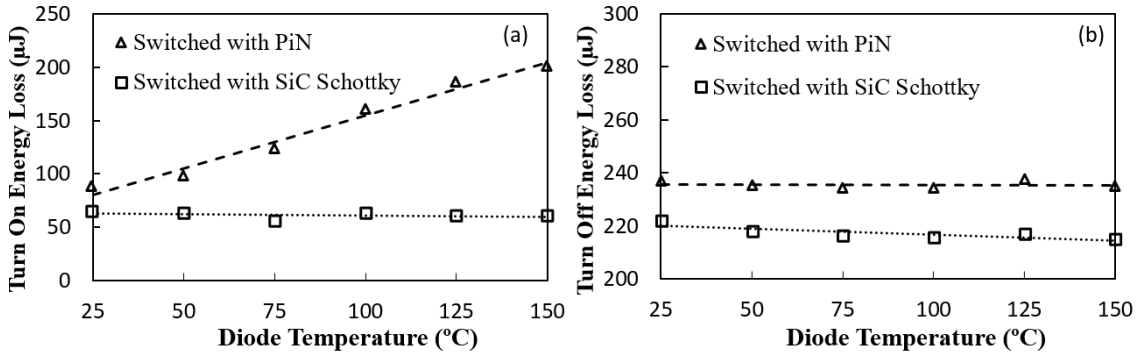


Figure 3.7: The measured (a) turn-on and (b) turn-off switching energy of the MOSFET as a function of diode operation temperature.

Figure 3.8 shows transient thermal response of the case temperature of a single silicon PiN (a) and SiC Schottky diode (b) switched with different duty cycles on the low side SiC MOSFET. As expected, the steady state case temperature increases with the diode duty cycle for both technologies however, the SiC Schottky diode on average has higher case temperatures and shows more thermal sensitivity to the duty cycle.

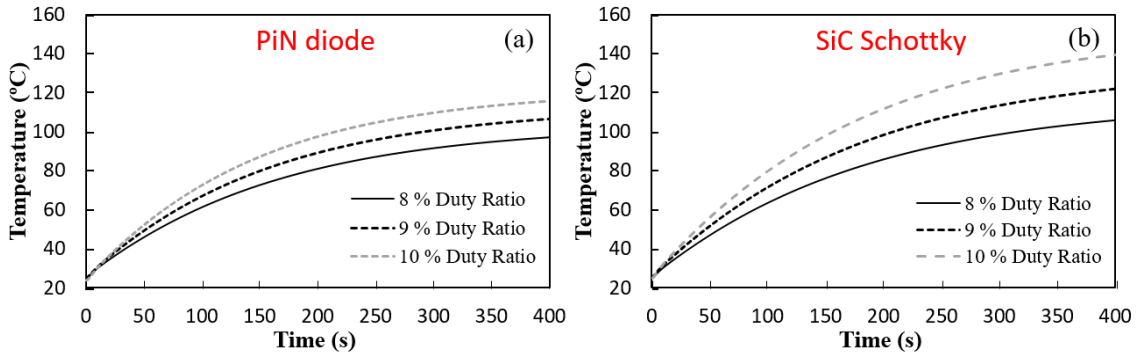


Figure 3.8: The measured case temperature rise for the (a) PiN diode switched with different duty ratios. (b) Similar measurement for the SiC Schottky diodes.

Figure 3.9 shows the diode temperature rise as a function of the switching frequency of the low side driving SiC MOSFET. The repetitive switching is performed with the same duty ratio, DC supply voltage and initial ambient temperature.

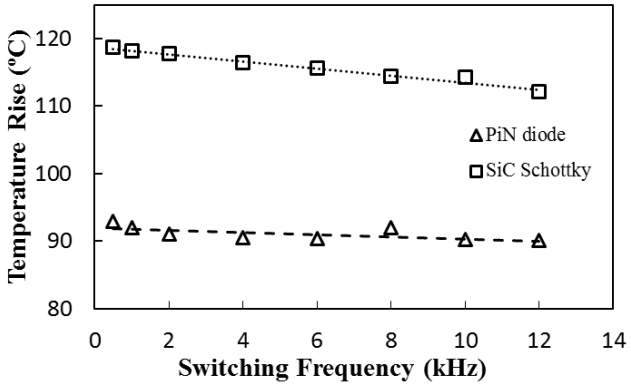


Figure 3.9: The case temperature rise as a function of switching frequency for both the silicon PiN and SiC Schottky diodes.

The case temperature is measured after 400 seconds when the diode is in steady state. As can be seen from Figure 3.9, the case temperatures for both diodes decreases with increasing switching frequency. This is due to the fact that the diode is on for 90% according to the duty cycle as a result of limited current rating of the test rig, hence, is dominated by the conduction losses. The SiC Schottky diode has a higher case temperature rise over the range of switching frequencies, however, the negative slope

with respect to temperature is higher compared to the PiN diode. In other words, at very high switching frequencies (10s of kHz), the SiC Schottky diode is expected to have a lower case temperature rise than the silicon PiN diode.

3.3 Electrothermal Balance in Parallel Connected Diodes

a. Temperature Imbalance

The parallel-connected silicon PiN diodes are heated to different initial junction temperatures using the electric heaters and the double pulse measurement is performed in order to assess the impact of the different junction temperatures on the diode's switching and conduction characteristics. Figure 3.10 shows the turn-on and turn-off current waveforms of two unbalanced diodes operating with DUT1 at 25 °C and DUT2 at 100 °C with a V_{DC} of 200V. Such an extreme mismatch is not a common issue in real applications but it is nonetheless studied as a worst case. As can be seen, the device operating at lower junction temperature conducts less current than the device operating at higher junction temperature. Moreover, this device switches off significantly faster than the device with higher junction temperature. This is due to the fact that the device at the lower junction temperature exhibits smaller minority carrier lifetime in the drift region and as a result, higher resistance in the drift region i.e. the PiN diodes are operating below the ZTC. In contrast the hotter device has a larger carrier lifetime and therefore more conductivity modulation. According to the current divider rule, it therefore conducts a higher current. It can also be seen from Figure 3.10 that the hotter Si PiN diode exhibits significantly larger reverse recovery charge. This larger reverse recovery will contribute to additional switching energy which increases the temperature of the hotter device and causes it to

take more current since it operates below ZTC. What is also important to note in the silicon PiN diode waveforms shown in Figure 3.10 is the fact that the diode currents diverge over time with the hotter PiN diode continually taking more current than the cooler PiN diode. This indicates thermal instability and possible thermal runaway in the absence of adequate cooling.

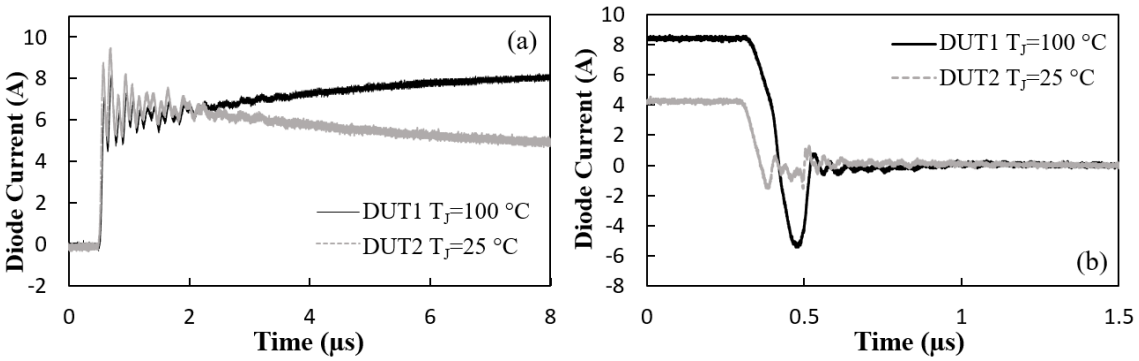


Figure 3.10: The measured (a) turn-ON and (b) turn-OFF current waveforms of parallel connected PiN diodes with junction temperatures of 25 °C and 100 °C.

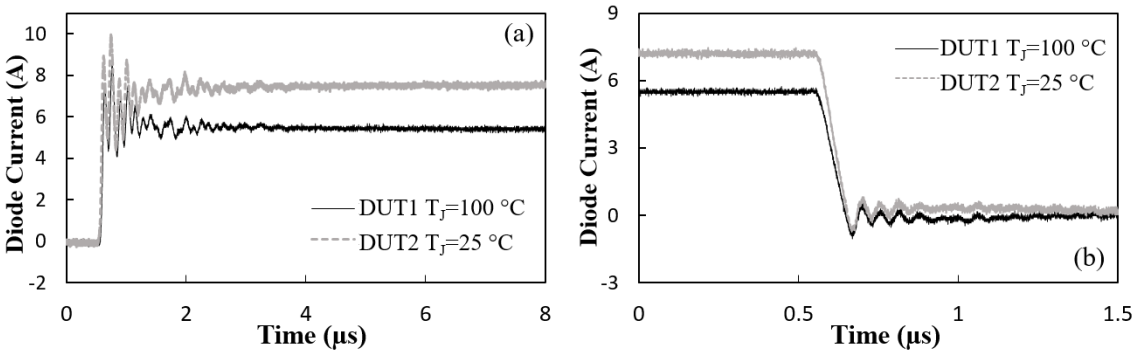


Figure 3.11: The measured (a) turn on and (b) turn off current waveform of the parallel connected SiC Schottky diodes with junction temperatures of 25 °C and 100 °C respectively.

The turn-ON and turn-OFF current switching transient of the parallel connected SiC Schottky diodes operating at different initial junction temperature is shown in Figure 3.11. As can be seen, the hotter device conducts less current thereby indicating that the diodes are operating above the ZTC point. Furthermore, the current through the parallel SiC

diodes is constant over time thereby indicating thermal stability. It should be noted that the diodes under investigation are conducting currents within the rated specification.

Figure 3.12(a) shows the turn-on and Figure 3.12(b) shows the measured turn-OFF switching energy of the unbalanced parallel-connected silicon PiN diodes. In Figure 3.12(a) and 3.12(b), one diode is held constant at 25 °C while the junction temperature of the other diode is varied from 25 °C to 150 °C. Hence, the plots show the switching energies as a function of the difference between the temperatures of the parallel diodes. As can be observed from the Figure 3.12, the turn-ON energy is higher for the cooler device while the turn-OFF energy is higher for the hotter device as a result of greater reverse recovery charge at high temperature. The difference between the switching energies of the parallel devices increases with the difference in the junction/case temperature.

Figure 3.13(a) and Figure 3.13(b) show the similar measurements for the unbalanced parallel-connected SiC Schottky diodes at different junction temperatures. By comparing Figure 3.12 and Figure 3.13, it can be seen that difference in switching energy between the parallel diodes are smaller for the SiC Schottky diodes than for the PiN diodes. In other words, the variation in the switching energy as a function of temperature is lower for the SiC Schottky diodes than for the silicon PiN diodes. As the temperature difference between the parallel connected diodes is increased from 0 to 125 °C, the switching energy difference between the parallel pair increases by 44.3% for the silicon PiN diodes and 13.5% for the SiC Schottky diodes. This is due to the temperature dependence of reverse recovery charge in silicon PiN diodes.

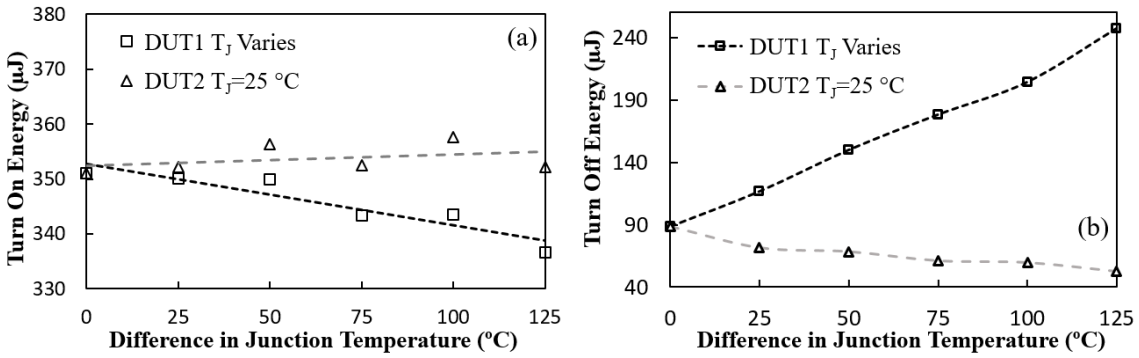


Figure 3.12: The measured (a) turn-ON and (b) turn-OFF switching energies of the parallel connected PiN diodes as a function of the difference in junction temperature.

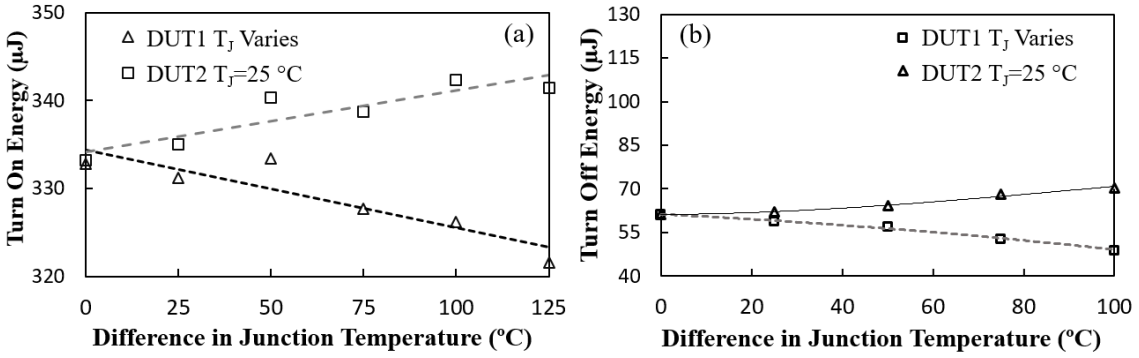


Figure 3.13: The measured (a) turn-ON and (b) turn-OFF switching energies of the parallel-connected SiC Schottky diodes as a function of the difference in junction temperature.

b. Dynamic behaviour evaluation

The thermal transient measurements are performed by repetitive switching over several minutes until steady state case temperature is reached. Hence, the case-temperature rise of continuously switched parallel-connected silicon PiN diodes has been measured and shown in Figure 3.14(a) and for the SiC Schottky diodes shown in Figure 3.14(b). Electrothermal imbalance between the parallel-connected diodes was introduced by setting different initial case temperatures. The difference in the initial case/junction temperature between the parallel-connected diodes was set to 3 °C. The parallel-

connected diodes have identical heatsinks and are switched at a frequency of 2 kHz with a duty ratio of 90% so that the conduction losses are dominant.

As can be seen from Figure 3.14(a), the measured case temperature difference between the two silicon PiN diodes diverge with time and is 13.5% after 600 seconds. This correlates with the double pulse measurements presented for the PiN diodes in Figure 3.10. Figure 3.14(b) shows that the case temperature difference for the SiC Schottky diodes converges and is only 2.3% after 600 seconds. However, the steady-state average case temperature rise for both PiN diode pair is 27.9% smaller than that of the Schottky diode pair after 600 seconds. Also shown in Figure 3.14, is the case temperature of the low side conducting SiC MOSFETs used to commutate current in both diodes. As can be observed from the comparison of Figure 3.14(a) and Figure 3.14(b), the temperature rise of the bottom SiC MOSFET is higher for the parallel PiN diode pair compared to the Schottky diode pair. This higher temperature rise in the MOSFET is due to the reverse recovery of PiN diodes inducing higher switching losses in the low side SiC MOSFET.

Figure 3.15 shows the parallel diode pair switched with different sizes of heatsinks, which in this case, simulates different thermal resistances and capacitances. Figure 3.15(a) shows the case temperature transient for the PiN diode pair, while Figure 3.15(b) shows that of the SiC Schottky diode pair. As can be seen from Figure 3.15(a) and 3.15(b), the diode with the smaller heatsink (higher thermal resistance) operates at a higher case temperature compared to that with the larger heat-sink (smaller thermal resistance). However, in the case of the unbalanced SiC diode pair, the difference in case temperature is smaller and appears to be converging after 600 seconds. For the unbalanced silicon PiN diode pair, the case temperature difference is larger and appears to be diverging after 600 seconds. Again, the low side SiC MOSFET used for switching current into the PiN diodes exhibits a higher case temperature compared to when the same device is used for the SiC

Schottky diodes. Hence, although the overall average case temperature is 27.9% lower for the PiN diode pair compared to the SiC Schottky diode pair, the case temperature rise of the low side MOSFET is 53.5% higher for the PiN diode pair.

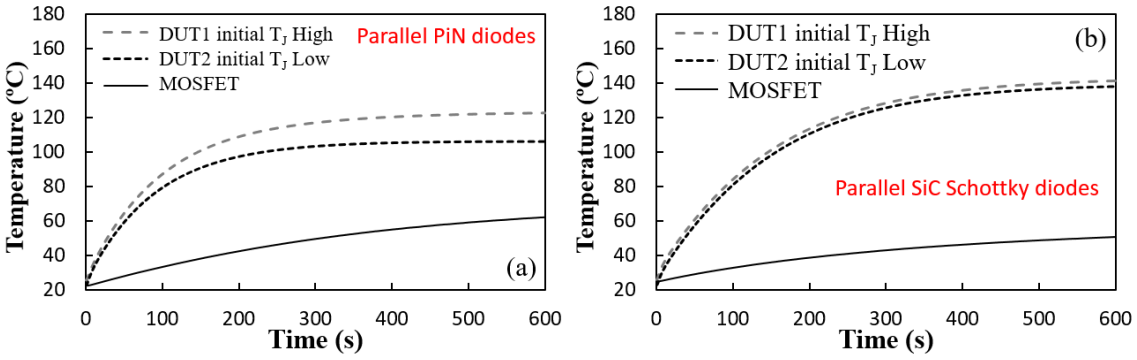


Figure 3.14: The measured case temperature rise for the (a) parallel-connected PiN diodes switched with same heatsink but with 3 °C difference in initial temperature. (b) Similar measurement for the parallel connected SiC Schottky diodes.

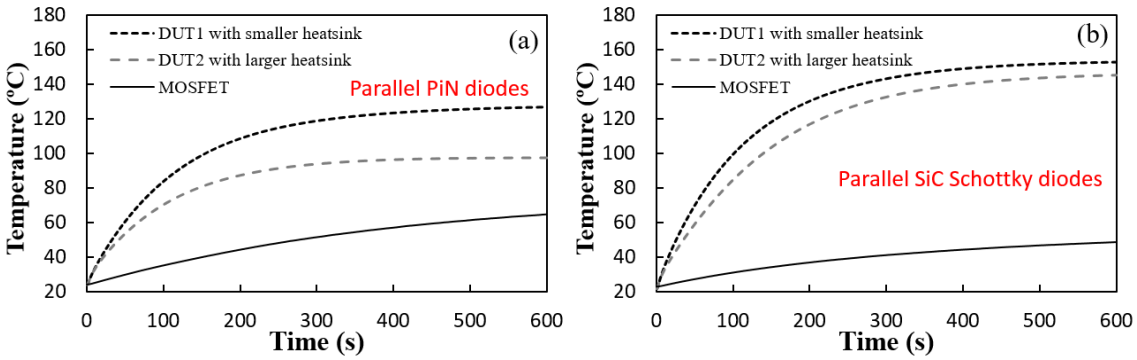


Figure 3.15: The measured case temperature rise for the (a) parallel-connected PiN diodes switched with different size heatsinks. (b) Similar measurement for the parallel connected SiC Schottky diodes.

3.4 Electrothermal evaluation of Silicon PiN and SiC Schottky Diodes under Unclamped Inductive Switching

Diodes are usually connected in anti-parallel with semiconductor switches in power converter applications. They can come in the form of external discrete diodes or internal body diodes with MOSFETs. Thus, the diode is able to block voltage in the same direction as the transistor switch while conducting the current in the opposite direction. Hence, when transistor switches undergo unclamped inductive switching, the anti-parallel connected diode is stressed especially if it is a body diode or an external discrete diode connected in anti-parallel with an IGBT. Stray inductances in circuits can also cause UIS in diodes since the inductances are de-energised by passing current into the diode while it is blocking voltage. It is therefore important to assess the electrothermal ruggedness of the diodes to evaluate the overall robustness of the converter.

Figure 3.16(a) shows the avalanche measurements taken from a 9A/600V SiC diode using the experimental test-rig introduced in Figure 3.1(b). When the diode goes into avalanche mode conduction, the voltage across the diode is equal to its intrinsic breakdown voltage which is typically higher than the stated breakdown voltage on the datasheet. It can be seen that for the 600 V rated SiC diode in Figure 3.16(a), the voltage across the diode during UIS is approximately 1000 V. As discussed previously, the high voltage MOSFET turns ON and charges the inductor which subsequently discharges the current into the diode under test since the latter has a lower breakdown voltage. It can be seen from Figure 3.16(a) that no current passes through the high voltage MOSFET when it is turned OFF. Figure 3.16(b) shows how increasing the gate pulse on the driving MOSFET is used to increase the avalanche current conducted by the diode. The peak avalanche current is increased gradually until the diode fails under thermal runaway. The current successfully conducted by the diode just before thermal destruction under UIS is

designated as the maximum avalanche current that the diode can sustain. Figure 3.17 shows examples of a silicon PiN diode and a SiC Schottky diode that has failed under UIS. The indication of thermal failure is a rapidly rising uncontrolled current that results from the fact that the diode has internally been short circuited. The current through the diode is eventually limited by the power supply.

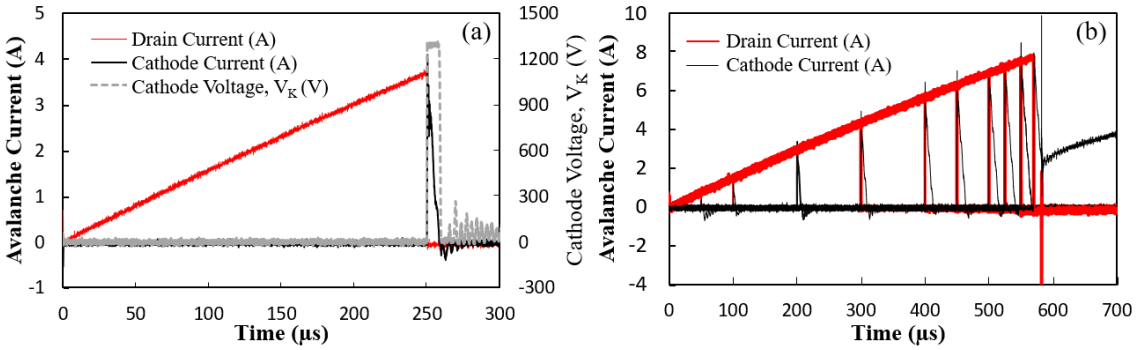


Figure 3.16: (a) UIS characteristics of a 600 V SiC Schottky diode and (b) UIS test with different pulse width.

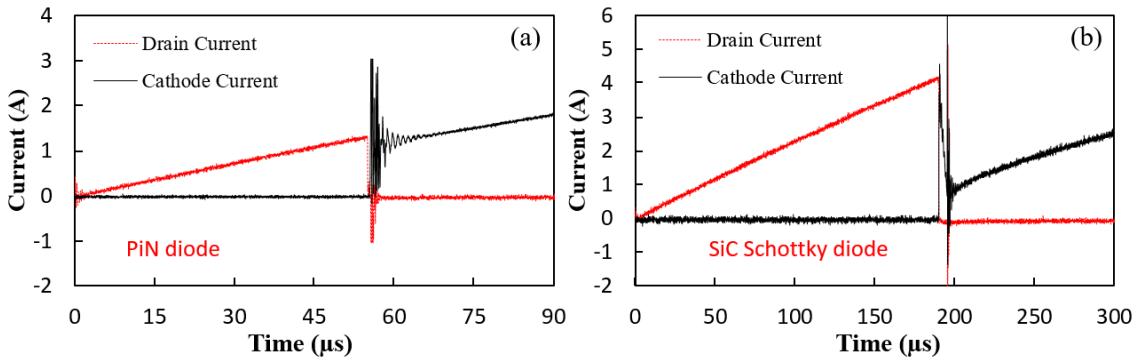


Figure 3.17: UIS Current waveform of (a) PiN diode and (b) SiC Schottky diode failure under avalanche mode conduction.

UIS measurements have been performed on SiC Schottky diodes and silicon PiN diodes in order to determine the maximum avalanche current and energy of both device technologies. Figure 3.17 shows the UIS test waveforms of (a) PiN diode and (b) SiC Schottky that have failed under UIS. The test is performed with a 4A/600V silicon PiN diode from international rectifier with the datasheet reference number of HFA04TB60 and 4A/600V SiC Schottky diode from CREE with the datasheet reference of C3D04060

with the inductor size of 2 mH. Figure 3.18 shows the peak avalanche current conducted by the diodes before failure for the (a) PiN diode and (b) SiC Schottky diode tested with 3 mH inductor.

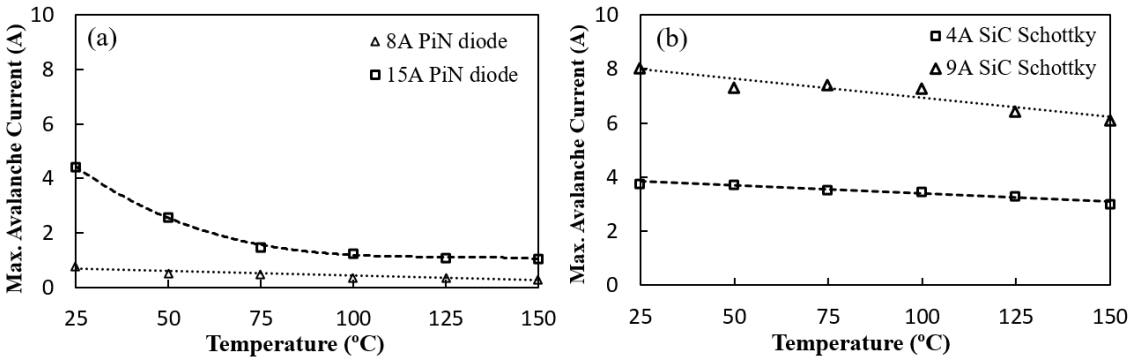


Figure 3.18: The maximum avalanche current for different current rated (a) PiN diodes and (b) SiC Schottky diodes at different junction temperatures.

The maximum avalanche current was measured for different initial junction temperatures for both technologies by setting the electric heater. For the silicon PiN diode, this was done for an 8 A and 15 A current rated device whereas for the SiC Schottky diodes, this was done for a 4 A and a 9 A current rated device. As can be seen from Figure 3.18, the higher current rated device exhibits a higher maximum avalanche current for both device technologies. This is expected since the current rating of the diode increases with the active area while the thermal resistance reduces with increasing active area. The current density is higher for the smaller active area diodes and coupled with the higher thermal resistance, the small current rated diodes will be less avalanche rugged. For both device technologies at both current ratings, the maximum avalanche current reduces with increasing junction temperature. The temperature coefficient of the maximum avalanche current is higher for the PiN diodes compared with the SiC Schottky diodes. The improved avalanche ruggedness of SiC Schottky diode benefits from better material property of SiC than silicon. Due to the energy band gap is three times higher for the SiC than silicon, the SiC device has higher doping concentration and thinner depletion region

compared to same voltage rating silicon device. Therefore, smaller active area is required for the SiC Schottky since depletion region is less resistivity. This is approved with the de-capsulated diodes which has been shown in the appendix. In addition, the thermal conductivity of SiC is 2.5 times higher than silicon, enabling superior heat extraction from the hotter cell, leading to less temperature imbalance between the cells within the device.

The avalanche characteristics of the devices are evaluated for different avalanche durations by using different inductor sizes. The avalanche energy dissipated in the device is equal to the energy stored in the magnetic field of the inductor, and this energy is calculated by $0.5 \cdot L \cdot I^2$. Consequently, the DUT can possibly fail in two ways: (1) long avalanche durations (using a large inductor) with small peak avalanche current and (2) short avalanche durations (using a small inductor) size with large avalanche current. Figure 3.19(a) shows the peak avalanche current before failure as a function of junction temperature for 2 different inductor sizes and Figure 3.19(b) shows the measured avalanche energy.

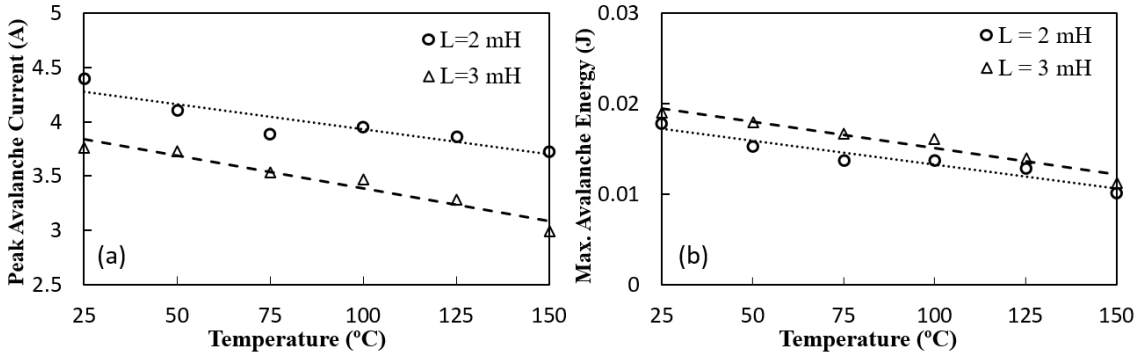


Figure 3.19: (a) The measured peak avalanche current and (b) calculated avalanche energy for the 4A SiC Schottky diode as a function of junction temperature for different avalanche durations.

The results show that the peak avalanche current reduces with the size of the inductor since the currents measured with a 2 mH inductor are larger than those measured with the

3 mH inductor. Furthermore, the maximum avalanche energy dissipated by the diode before thermal failure increases with the avalanche duration (inductor).

3.5 UIS measurements and Simulations for Parallel Connected Diodes

Parallel connected silicon PiN and SiC Schottky diodes have been subjected to UIS tests so as to investigate the impact of electrothermal imbalance on the avalanche ruggedness of the parallel pair. Before the parallel devices are set at different junction temperatures, first, the avalanche current sharing capability of the parallel connected devices when set at the same junction temperature is evaluated. Figure 3.20 shows the measured avalanche waveform of the parallel connected SiC Schottky diode pairs at the same junction temperature 25 ºC. As can be seen from Figure 3.20, the voltage across the DUT increases slightly during avalanche conduction. This is due to the fact that the breakdown voltage has a positive temperature coefficient, hence, it increases as the junction heats up. Figure 3.20 shows that the devices are matched since both conduct equal magnitudes of the avalanche current.

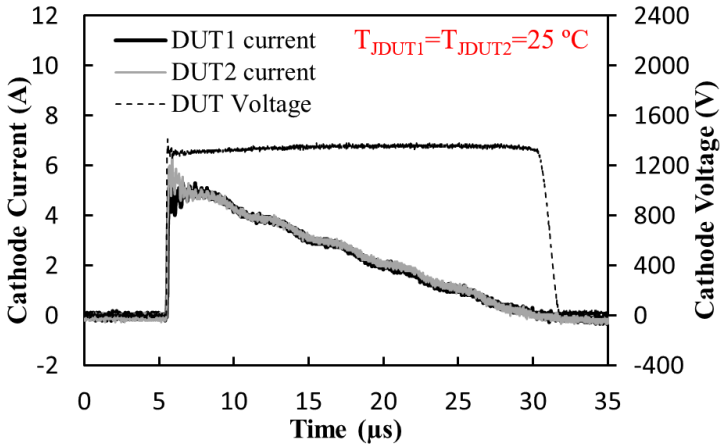


Figure 3.20: Avalanche current characteristics for the parallel SiC Schottky diodes with equal junction temperatures between the DUTs (T_{J1}=T_{J2}=25 ºC).

a. UIS measurements on parallel Silicon PiN diodes

The silicon PiN diode under test is a 15A/600V hyper-fast PiN diode from International Rectifier. In this experimental setup, the electrothermal non-uniformity between the PiN diode pairs is introduced by keeping one of the PiN diodes at 25 ºC while the other is heated to higher pre-defined temperature using an electric heater. Figure 3.21(a) shows the measured waveforms of the parallel connected PiN diodes with different junction temperatures (DUT1 was set at 25 °C and DUT2 was set at 100 °C). It can be seen from Figure 3.21 that the diodes both successfully conduct the avalanche current without thermal destruction. However, the PiN diode set at the lower junction temperature conducts the bulk of the total avalanche current. This is due to the positive temperature coefficient of the breakdown voltage which means that the device with the lower junction temperature has a lower breakdown voltage and thus conducts the bulk of the avalanche current. The peak avalanche current conducted by the parallel diodes was increased until thermal runaway occurred. This was done for different magnitudes of temperature difference between the parallel DUTs.

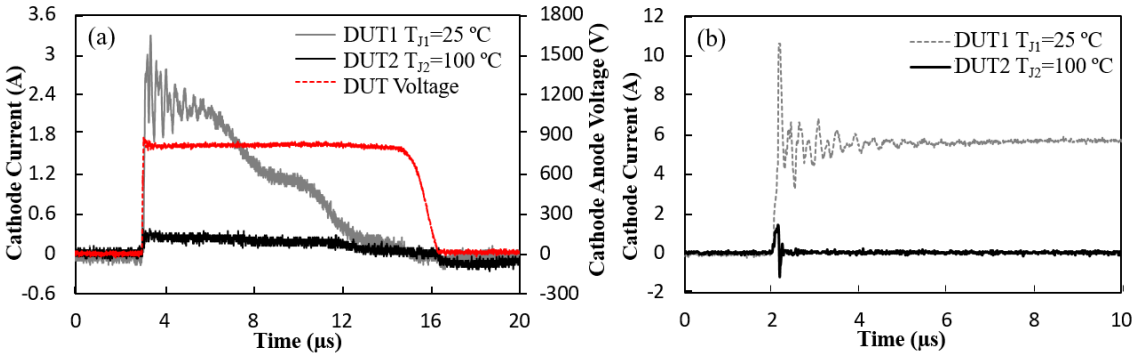


Figure 3.21: (a) Avalanche current waveforms for the parallel PiN diodes with different junction temperatures showing (a) no thermal runaway at 3 A peak current (b) thermal runaway at 10 A peak current.

Figure 3.21(b) shows measured waveforms of the avalanche currents when thermal runaway occurred in the cooler device. As can be seen, the diode with T_J=100 °C conducts approximately 1.5 A of avalanche current and recovers while the device with T_J=25 °C conducts a peak avalanche current of 10 A and undergoes thermal runaway.

b. UIS measurements on parallel SiC Schottky diodes

The SiC Schottky diode under test is a 600V/9A device from CREE. The avalanche measurements are performed under identical conditions as the experiments carried out with the PiN diodes. Figure 3.22 shows the measured waveforms of the parallel connected SiC Schottky diodes with the junction temperatures set at 25 ºC and 100 ºC. Similar to the measurements on the PiN didoes, the hotter device conducts less avalanche current which is again due to the positive temperature coefficient of the breakdown voltage. However, for the same temperature difference between the parallel pairs, the difference in avalanche current is smaller for the SiC Schottky diodes. The hotter SiC diode on average conducts almost the same current as the cooler SiC diode unlike the case of the parallel silicon PiN diodes where the ratio of avalanche current between the cooler and the hotter was over 9:1. Figure 3.22(b) shows the avalanche current characteristics of the parallel connected SiC Schottky diodes where failure has occurred. Unlike the parallel silicon PiN diodes where the cooler device failed, in the parallel SiC Schottky diodes, the hotter device failed.

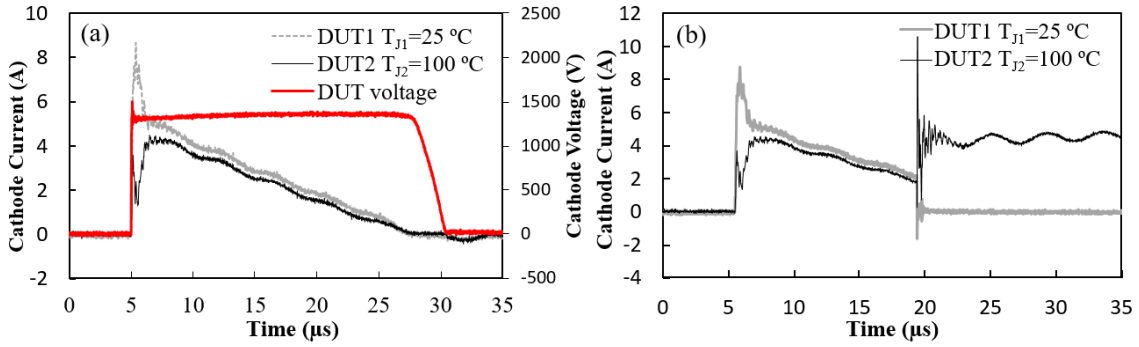


Figure 3.22: (a) Avalanche current waveforms for the parallel SiC Schottky diodes with different junction temperatures showing (a) no thermal runaway at 8 A peak current (b) thermal runaway at 8.5 A peak current.

c. Avalanche Ruggedness of the Parallel Pairs with different ΔT_J

The duration of the UIS pulse is determined by the inductor size since the voltage characteristic of the inductor is given by V=L·dI/dt, hence the avalanche duration can be defined as t=L·I/V. UIS stress tests on parallel connected diode pairs at different initial junction temperatures have been done for different avalanche durations corresponding to 1 mH and 3 mH inductors. Figure 3.23(a) shows the measurements for the parallel connected SiC Schottky diodes while Figure 3.23(b) shows the measurements for the silicon PiN diodes. It can clearly be seen that the wide bandgap characteristics and high thermal conductivity of SiC means that the diodes are able to sustain higher peak avalanche currents without going into thermal runaway. However, what can also be seen is that parallel connected SiC diodes with different initial junction temperatures are more electrothermally rugged also because there is better current sharing even when imbalance is introduced. For example, as the difference in the initial junction temperature between the parallel DUTs (ΔT_J) is increased from 0 to 125 °C, with a 1 mH inductance, the peak avalanche current sustainable by the parallel SiC Schottky diodes falls by only 20.7%

whereas for the PiN diode is falls by 35.7%. As the inductance is increased to 3 mH, the change in the maximum avalanche current is 11.4% for the parallel SiC Schottky diodes and 44.5% for the parallel PiN diodes.

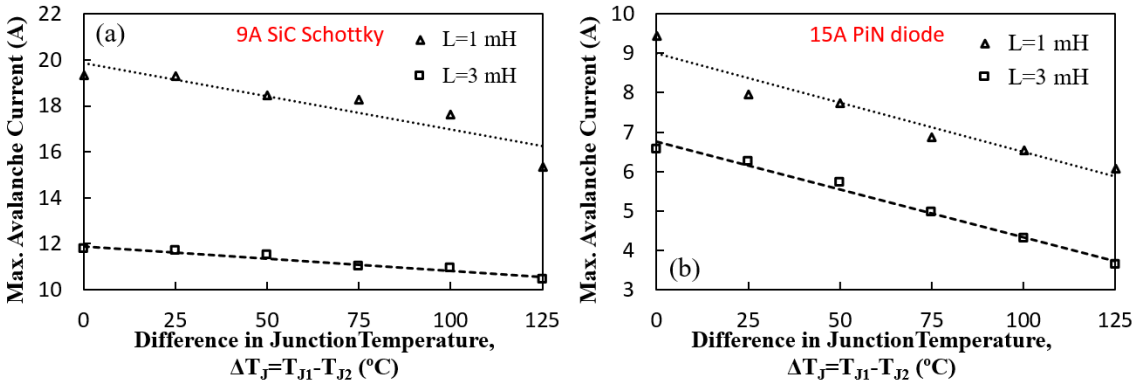


Figure 3.23: The peak avalanche current as a function of temperature difference between the parallel connected (a) silicon PiN diodes and (b) SiC Schottky diodes for two inductor sizes: 1 mH and 3 mH.

Figure 3.24(a) shows the measured maximum avalanche energy before thermal failure for the parallel SiC Schottky diodes as a function of ΔT_J (the initial junction temperature difference between the parallel connected DUTs) with 1 mH and 3 mH inductance. Figure 3.24(b) shows a similar plot for the silicon PiN diodes. Both plots show that the maximum avalanche energy increases with the avalanche duration. The parallel SiC diodes conduct significantly more avalanche energy compared to the parallel PiN diodes (0.2 J compared with 0.07 J) in spite of the fact that they have lower current ratings than the PiN diodes. Again, the decrease in the maximum avalanche energy corresponding to a given ΔT_J between the parallel devices is more for the PiN diodes than the Schottky diodes. This means that the SiC Schottky diodes are not only more electrothermally rugged but can cope with electrothermal imbalance better than PiN diodes.

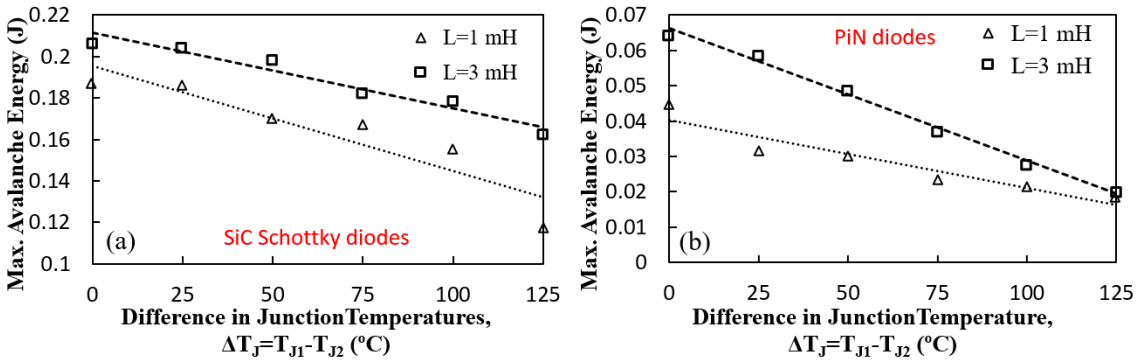


Figure 3.24: The measured avalanche energy dissipated in the (a) SiC parallel Schottky pairs and (b) Silicon PiN diode pairs as a function of temperature difference between the DUTs. Measurements for 1 mH and 3 mH inductance.

By comparing Figure 3.21(b) with Figure 3.22(b), it can be seen that when unbalanced parallel connected diodes fail under UIS, the cooler diode fails in the case of silicon PiN diodes whereas the hotter diode fails for in the case of the SiC Schottky diodes. When diodes fail under UIS, the failure mechanism is thermal runaway resulting from a self-sustaining avalanche multiplication (or impact ionisation) process. For this to happen, the thermally generated carriers resulting from temperature induced bandgap narrowing must overcome the background doping of the semiconductor. Normally, parallel-connected MOSFETs conducting avalanche current should be electrothermally stable. This is due to the fact that the positive temperature coefficient of the breakdown voltage should self-regulate the avalanche current. Hence, as the initially cooler device conducts more avalanche current and increases its junction temperature, the breakdown voltage should also increase thereby diverting current to the parallel connected device with the smaller junction temperature. Hence, like parallel MOSFETs conducting on-state current, the positive temperature coefficient of the breakdown voltage should regulate the avalanche current. But this depends on the device having sufficient time to reach thermal equilibrium as well as the difference in the initial breakdown voltages between the parallel

connected devices i.e. the greater the difference in breakdown voltage, the more time is required to reach thermal equilibrium between them.

The rate at which the breakdown voltage changes with temperature is important in understanding why the cooler device fails in the PiN diode case and the hotter device fails in the SiC Schottky diode case. Figure 3.25(a) shows the measured breakdown voltages of the silicon PiN and SiC Schottky diodes as functions of temperature while Figure 3.25(b) shows the normalised version of Figure 3.25(a). It can be seen from both plots that the breakdown voltage increases with temperature. This is due to increased phonon scattering reducing the carrier mean-free-path thus delaying impact ionisation and reducing avalanche multiplication. However, it can be seen from Figure 3.25(b) that the temperature coefficient of the breakdown voltage is higher for the silicon PiN diode than it is for the SiC Schottky diode. Hence, the result is that the temperature difference between the parallel-connected DUTs leads to a much higher difference in breakdown voltage between the PiN diodes compared to the Schottky diodes. As a result, a greater fraction of the avalanche current flows through the cooler device in PiN diodes which causes a sudden rise in temperature in the cooler diode thereby taking the initially cooler diode to its thermal limit. There is no time for the breakdown voltages to self-correct as the device is thermally destroyed in a few microseconds.

In the case of the Schottky diode, the lower temperature coefficient of the breakdown voltage means that the difference between the breakdown voltages of the unbalanced parallel-connected diodes is lower compared to the PiN diode pair. As a result, the hotter diode is pushed to its thermal limit faster since there is no time for the breakdown voltages to regulate the avalanche current.

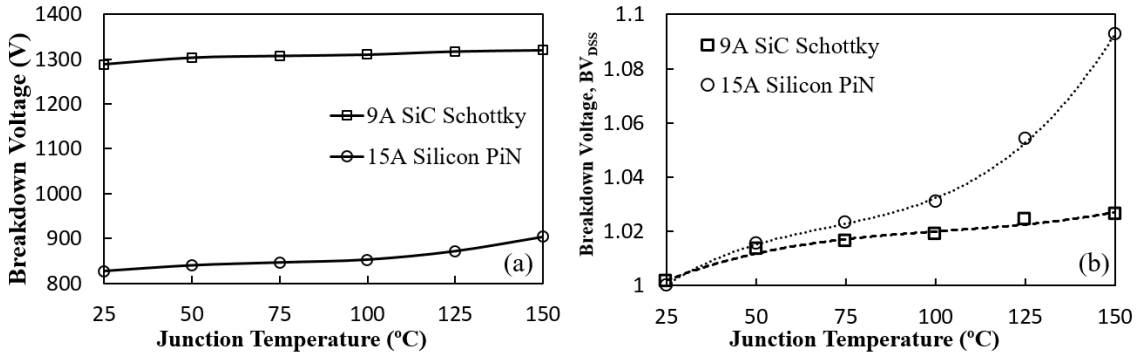


Figure 3.25: (a) The measured breakdown voltages of the silicon PiN and SiC Schottky diodes as functions of temperature (b) Normalised breakdown voltages.

d. Finite Element Modelling

Finite Element Models for the Silicon PiN Diode Pair

Finite element models have been developed to describe the characteristics of the silicon PiN diodes and SiC Schottky diodes under avalanche mode condition. The PiN diode in the simulation was optimized to yield a breakdown voltage of 700 V by using a 55 µm depletion layer with a doping of $3x10^{14}$ cm^{-3}. The p-region doping and n substrate was $1x10^{19}$ cm^{-3} and $5x10^{19}$ cm^{-3} respectively. Two identical PiN diodes were simulated under the same conditions as the experimental measurements and the initial junction temperature of the devices were set to 25 ºC and 100 ºC. Figure 3.26 shows the simulated avalanche waveform for the parallel-connected PiN diodes with different junction temperature. Figure 3.26 shows the MOSFET charging current in red dashed lines and the diode avalanche currents in black. In Figure 3.26, it can be seen that the parallel diodes fail during avalanche since the current rises uncontrollably during UIS conduction. In order to understand the internal current distribution within the devices during the UIS test, two-dimensional current density contour plots at various points in time has been extracted from the simulator. These 2-D plots have been extracted at points X, Y and Z

corresponding to Figure 3.26. Figure 3.27 shows the 2-D current density contour plots of the parallel-connected PiN diodes at point X where the MOSFET is turning off and the avalanche current starts to flow through the parallel-connected PiN diodes. As can be seen from the Figure 3.27, the cooler device conducts more current than the hotter diode since the cooler device is less resistive as a result of lower breakdown voltage. Figure 3.28 shows the 2-D current density contour plot at point Y corresponding to Figure 3.26 where the current density can be seen to be much higher for the cooler device. Figure 3.29 shows the 2-D current density contour plot corresponding to point Z in Figure 3.26 where the cooler PiN diode failed in conducting the avalanche current.

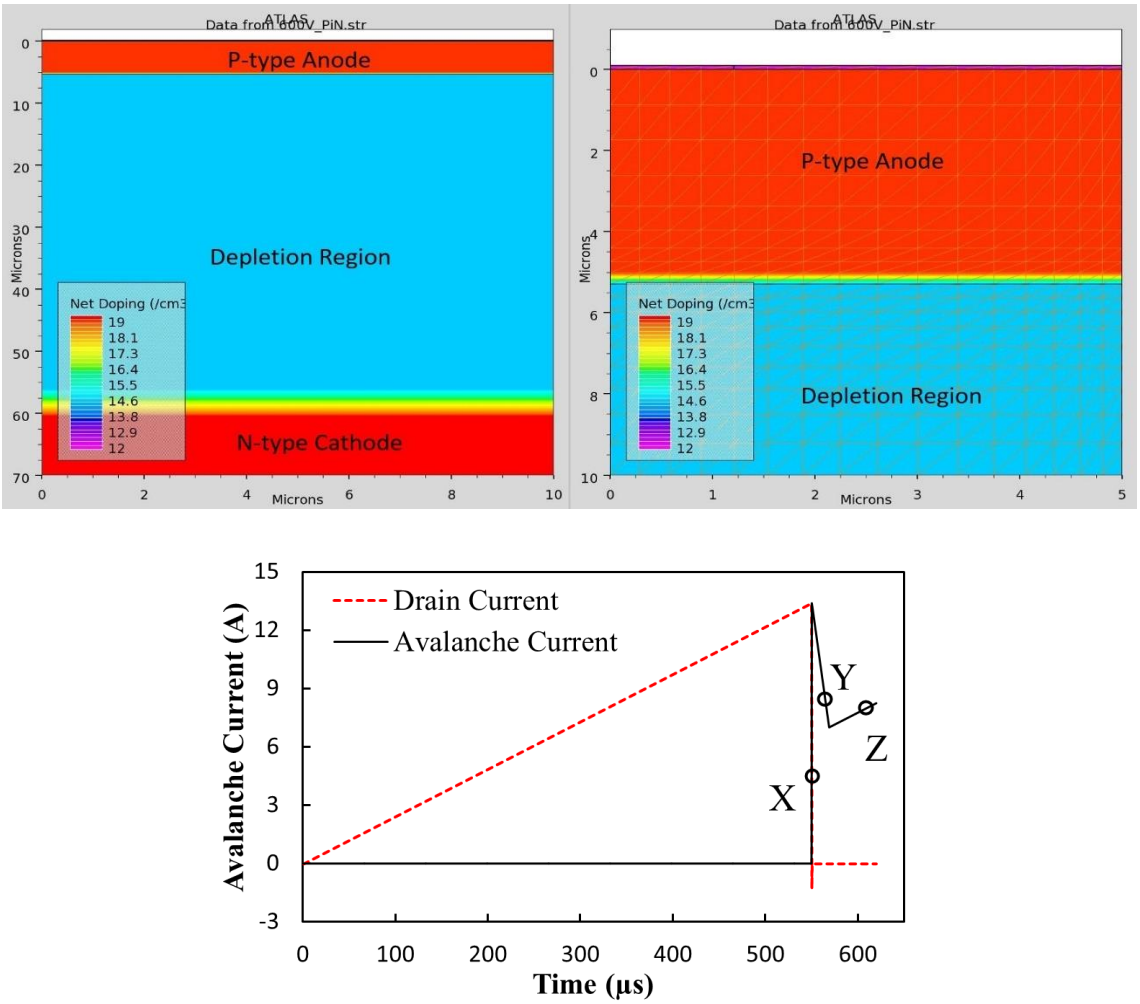


Figure 3.26: (a) The layout of the simulated 600 V silicon PiN diode, and (b) the simulated avalanche current for the parallel connected PiN diodes with different junction temperatures.

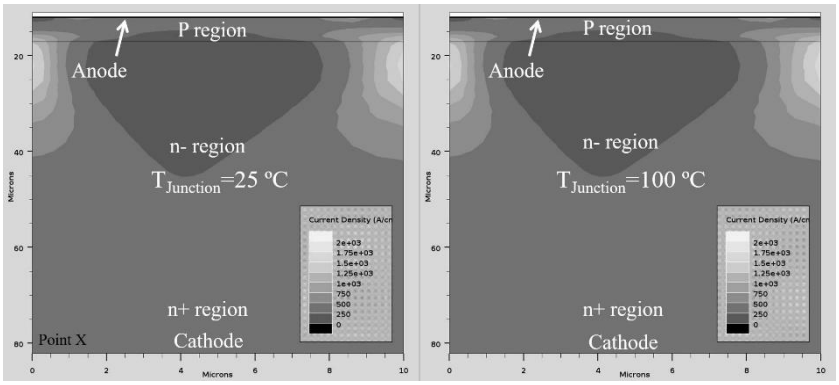


Figure 3.27: 2-D current density plots for parallel connected PiN diodes with different junction temperatures under UIS. This corresponds to point X in Figure 3.26.

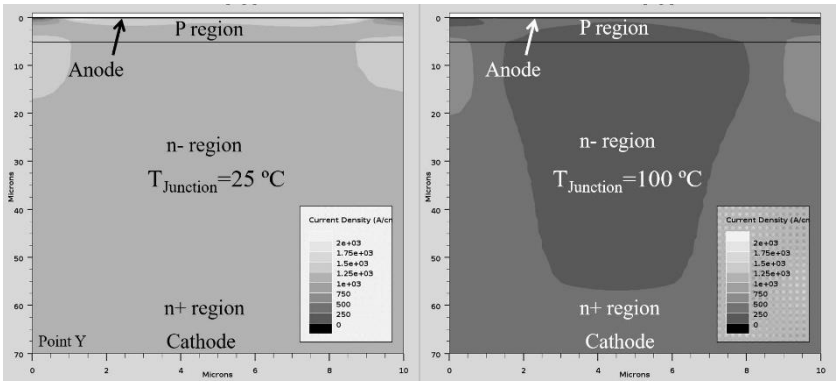


Figure 3.28: 2-D current density plots for parallel connected PiN diodes with different junction temperature under UIS. This corresponds to point Y in Figure 3.26.

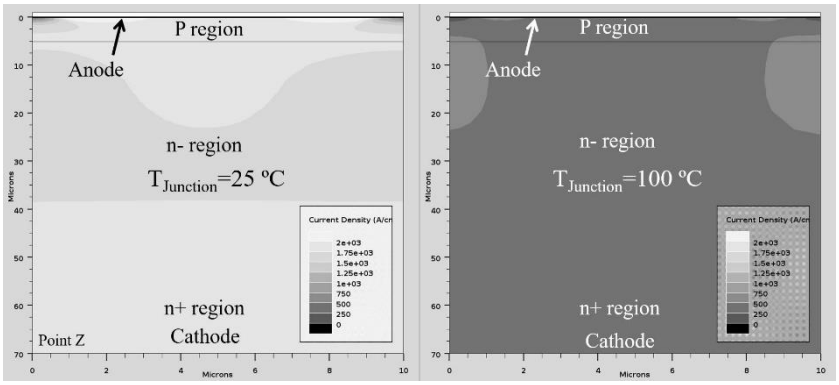


Figure 3.29: 2-D current density plots for parallel connected PiN diodes with different junction temperature under UIS. This corresponds to point Z in Figure 3.26 where the cooler PiN diode fails to dissipate the avalanche current.

Finite Element Models for the SiC Schottky Diode Pair

Similar finite element models have been simulated for the SiC Schottky diode parallel pair in order to explain the experimental performance. The SiC Schottky diode in the model was optimized to 800 V by using a 3.5 μm depletion layer with a doping of $8.5x10^{15}$ cm^{-3}. Similar avalanche simulations were performed for the SiC Schottky diode pair producing similar breakdown characteristics as shown in Figure 3.26. In the simulations of the Schottky diode pair, one diode was set at a junction temperature of 25 °C while the other was set at 100 °C. Figure 3.30 shows the layout of the simulated SiC Schottky model in ATLAS. Figure 3.31 shows the 2-D current density contour plot for parallel SiC diodes at point Y corresponding to point Y in Figure 3.26. As can be seen from Figure 3.31, the current density is higher in the cooler diode compared to the hotter one when both diodes conduct in avalanche. Figure 3.32 shows the 2-D current density plots of the parallel SiC Schottky diode pair at point Z when thermal runaway sets in. By comparing Figure 3.32 to Figure 3.29, it can be seen that the avalanche current flows through the hotter diode in the SiC Schottky diode pair unlike the silicon PiN diode pair where the cooler diode undergoes thermal runaway. The simulation results confirm the experimental observations which show that the hotter SiC diode fails in thermal runaway.

The simulation results confirm that the lower temperature coefficient of the breakdown voltage in SiC means that the avalanche current disparity between the diodes is smaller compared to the PiN diode pair. Hence, as a result, the hotter diode reaches the maximum temperature before the diode with the lower junction temperature has time to reach runaway temperature.

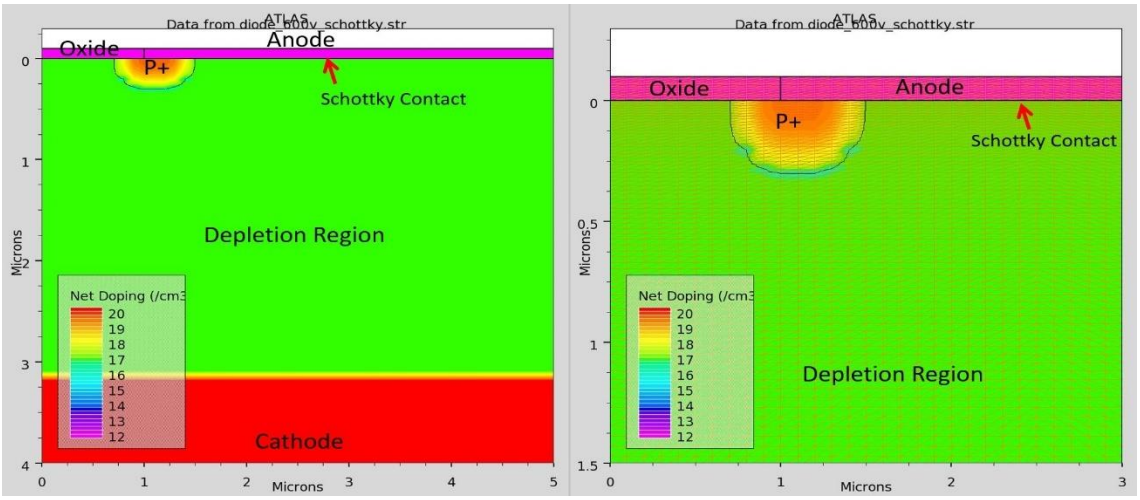


Figure 3.30: The layout of simulated 600 V SiC Schottky diode.

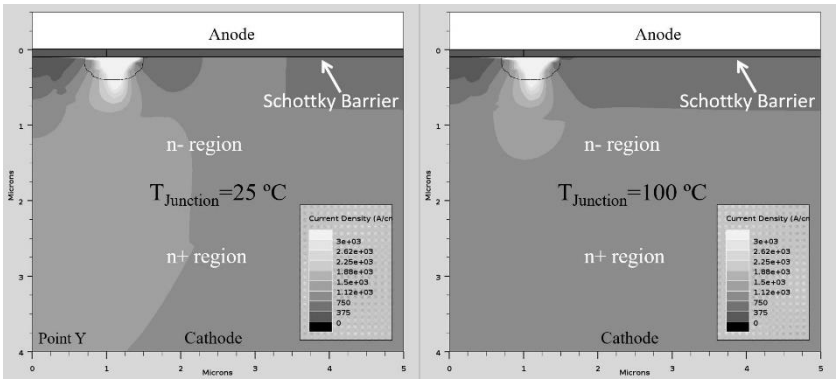


Figure 3.31: 2-D current density plots for parallel SiC Schottky diodes with different junction temperature under UIS. This corresponds to point Y in Figure 3.26.

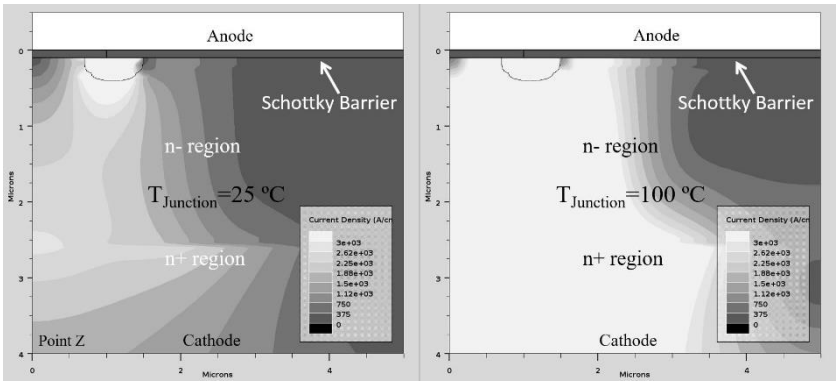


Figure 3.32: 2-D current density plots for parallel SiC Schottky diodes with different junction temperature under UIS. This corresponds to point Z in Figure 3.26 where the SiC Schottky diode pair fails to dissipate the avalanche current.

3.6 Conclusion

In this chapter, clamped inductive switching test has shown that although PiN diodes exhibit lower junction/case temperatures than SiC Schottky diodes for a given switching frequency, duty cycle and switching rate, however, the complimenting transistor exhibits a higher junction/case temperature i.e. the electrothermal stress is transferred from the diode to the complimenting transistor. It is also shown that SiC Schottky diodes exhibit more stable operation under electrothermal imbalance when connected in parallel. The higher ZTC point in silicon PiN diodes typically results in lower junction/case temperatures under repetitive switching conditions compared with SiC Schottky diodes. However, the reverse recovery characteristics causes higher switching losses, hence, higher junction temperatures, in the low side driving MOSFET. The positive temperature coefficient of the PiN diode's current conductivity causes thermal instability as evidenced through the diverging case temperatures between the parallel connected devices. This is not the case with Schottky diodes where converging temperature characteristics in the parallel connected diodes is evident.

UIS measurements have shown that SiC Schottky diodes are more electrothermally rugged than silicon PiN diodes regardless of the current rating. When there is temperature imbalance between parallel connected diodes in avalanche, the total electrothermal ruggedness of the parallel connected pair reduces. The maximum avalanche current and energy of the parallel connected diode pairs have been shown to reduce with increasing difference in the initial junction temperature. This reduction is significantly smaller for the SiC Schottky diodes compared to the silicon PiN diodes. Furthermore, in parallel SiC Schottky diode pairs, the hotter device fails under UIS whereas in the case of the parallel silicon PiN diode pairs, the cooler device fails. This is due to the smaller temperature coefficient of the breakdown voltage in SiC Schottky diodes compared with silicon PiN

diodes. Hence, Schottky diodes are not only more electrothermally rugged than silicon PiN diodes, but they perform better under parallel connections and can balance energy more equally.

Chapter 4.

MODELLING AND EXPERIMENTAL CHARACTERIZATION OF PARALLEL CONNECTED POWER DEVICES UNDER CLAMPED INDUCTIVE SWITCHING

4.0 Introduction

The ability of power semiconductor devices to share current and temperature in parallel is a very important feature because parallel connected devices are often required to deliver higher current ratings [8, 119-123]. Although solder fatigue and wire-bond damage are the dominant failure mechanisms in power modules [112, 124-128], it is nevertheless important to study the impact of possible electrothermal variations between parallel connected devices on the overall robustness of the power module. Differences in the electrical and thermal parameters of the individual devices can trigger other failure

mechanisms [129, 130]. If parallel connected power devices are subject to different load currents, they will undergo different thermal cycles and hence, different degrees of thermo-mechanical fatigue from stress cycling due to CTE mismatch. This means the thermal resistance will degrade at different rates and the devices will thus operate at different junction temperatures. Hence, while thermo-mechanical fatigue may degrade the health of the module, the single event failure mechanism may be electrothermal overloading from the degraded safe-operating-area. Although devices may begin the application mission profile with minimal variation between the electrothermal parameters, over the course of operation in the field, this variation may increase due to the position dependency of the device or application related field fails. Electrothermal variations between parallel connected devices can also accelerate short circuit failure since the current is not shared equally between the parallel devices. The short circuit performance of SiC power devices has been studied in [131, 132] and advanced gate drivers with short circuit protection features capable of turning off the device instantly when the short circuits occurs has been presented in [133, 134].

Under normal operation such as motor driving and/or power conversion in clamped inductive switching (CIS) conditions, the positive temperature coefficient of the on-state resistance of power MOSFETs makes them ideal for parallel operation since temperature limits the current [122, 135]. IGBT devices have an extra $p+$ layer after the voltage blocking drift layer compared to the standard MOSFET so as to reduce the on-state resistance through conductivity modulation. On the other hand, CoolMOS devices are basically MOSFETs that use the principle of super-junctions to deliver low conduction losses by using alternate p and n columns in the voltage blocking drift layer [136-138]. CoolMOS transistors competes with conventional silicon MOSFETs and IGBTs in the sub 1200 V application space, while the wide bandgap SiC devices are expected to take

to compete with IGBTs in applications above 1200V. In high current applications where several dies are required in parallel, the ability of the devices to share current and temperature equally is important. High current applications with IGBT/SiC have been presented in [8, 123, 139-141] and the impact of electrothermal imbalance between the parallel connected IGBTs have been investigated in [142-144]. However, a systematic investigation of how SiC MOSFETs, silicon IGBTs and CoolMOS devices comparatively perform under electrothermal imbalance between parallel connected devices has not systematically been investigated.

Differences in the thermal and electrical switching time constants between parallel-connected devices cause imbalances in the power and temperature distribution thereby accelerating the aging of power module. In this chapter, the impact of electro-thermal variations between parallel-connected devices on module balancing is investigated for 900V-CoolMOS, 1.2kV-SiC MOSFETs and 1.2kV-IGBTs under clamped inductive switching (CIS). The electro-thermal variations are introduced by switching parallel-connected transistors with different gate resistances (to emulate different electrical time constants) and different cooling conditions (to emulate different thermal time constants). Under CIS, the difference in the steady-state junction temperature (ΔT_J) and switching energy (ΔE_{SW}) between the parallel connected devices for a given difference in the gate and thermal resistance (ΔR_G & ΔR_{TH}) is used as the metric for determining robustness to electrothermal variations i.e. how well the devices maintain uniform temperature in-spite of switching with different rates and thermal resistances. Hence, for every electrical and thermal mismatch introduced between the parallel-connected devices, the impact on the measured switching energy and steady-state case temperature is ascertained. Hence, this chapter studies the impact of variation in electrothermal parameters between parallel-connected devices for the different technologies. The two principal parameters under

investigation in this chapter are electrical switching rates and the thermal resistance. Variations in the electrical switching time are set by the gate resistances which determine the *dI/dt* while variation in the thermal resistance is emulated by setting different initial junction temperatures between the parallel devices and using different heat-sinks. Section 4.1 describes the experimental set-up used in this chapter. Section 4.2 to Section 4.8 shows the results obtained from clamped inductive switching measurements and finite element modelling while Section 4.9 concludes the chapter.

4.1 Experimental Set-up

The circuit diagram and picture of the experimental test rig is shown in Figure 4.1(a) and Figure 4.1(b) respectively. The parallel connected Devices under Test (DUTs) are driven by separate gate drives, a common 470 µF DC link capacitance, the same free-wheeling diodes and a DC power supply. The switching energies were also measured under identical conditions, and it was confirmed that the devices are identical in switching characteristics and the separate gate drivers have not introduced variations between the parallel devices.

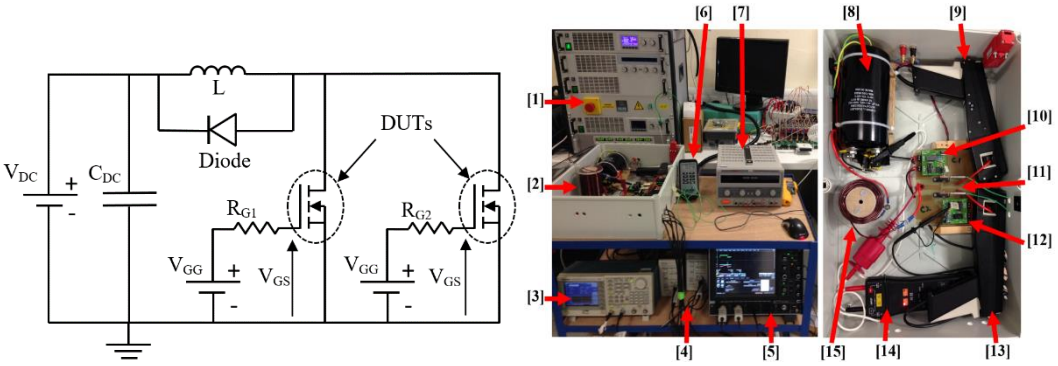


Figure 4.1: (a) Circuit schematic for the experimental set-up. (b) shows the picture of the experimental set-up with [1] Power Supply. [2] Test Chamber. [3] Function Generator. [4] Current probe Amplifier. [5] Oscilloscope. [6] Thermometer. [7] DC power supply for heater. [8] DC capacitor. [9] and [13] Current Probes. [10] and [12] Gate Drives. [11] DUTs. [14] Voltage probe. [15] Inductor.

The SiC power MOSFETs are 1.2kV/10A devices from CREE with datasheet reference C2M0280120D, the CoolMOS devices are from Infineon and rated at 900V/15A with datasheet reference IPW90R340C3 and the IGBT devices are from International Rectifier and rated at 1.2kV/11A with datasheet reference IRG4PH20KPbF. The IGBT is standalone version that has no internally integrated anti-parallel connected diode. Differences in the electrical response between parallel-connected devices are set by ensuring $R_{G1} \neq R_{G2}$ and in the case of thermal response, $T_{J1} \neq T_{J2}$.The gate capacitance is an inherent characteristic of power semiconductor switches. Similar to an ordinary capacitor, this capacitance depends on the area and thickness of the dielectric. When several dies are connected in parallel, the overall gate capacitance becomes the sum of each gate capacitance. This increases the demand of the power handling capability of the gate driver [144]. Previous work in [145] has shown that the track distance on the DBC can lead to mismatch in current sharing between the parallel-connected SiC MOSFETs due to different electrical switching time constants arising from the different gate resistances. Although the gate drivers are separate, they are identical circuits driven from the same signal generator and have thus been synchronized. Proper current/temperature sharing between the devices under identical conditions have been guaranteed before electrothermal variations are introduced. Hence, under repetitive clamped inductive switching, the case temperatures of 2 parallel connected devices identically driven by the 2 gate drives were within 1 °C of each other.

When the parallel connected devices were driven with the same gate resistance and at the same temperature, the measured switching energy was very similar thereby indicating that the gate drivers were properly synchronised and did not inject any variation into the analysis. This is also true for the case temperatures under repetitive switching which were equal for both devices, again, indicating that the devices are properly

synchronised. Figure 4.2(a) shows the synchronised current waveform characteristics of the parallel SiC MOSFETs at turn-ON while Figure 4.2(b) shows the characteristics at turn-OFF. Figure 4.3(a) shows the turn-ON switching transient for parallel devices switched with a 2 ns delay introduced between the gate drivers. It can be seen that DUT1 turn-On and turn-Off later than DUT2 compared with Figure 4.2, this delay translates into the current switching transients proportionally.

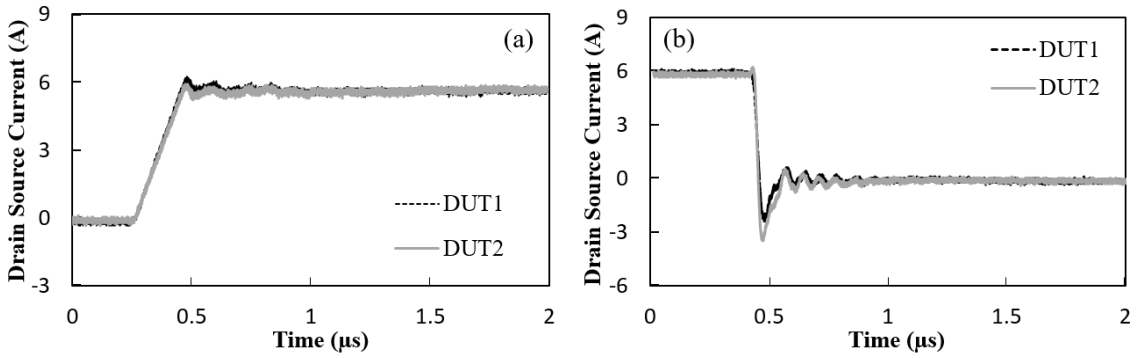


Figure 4.2: (a) Current switching transient characteristics for the parallel connected SiC power MOSFETs at turn-ON under balanced conditions (b) Similar measurements for turn-OFF.

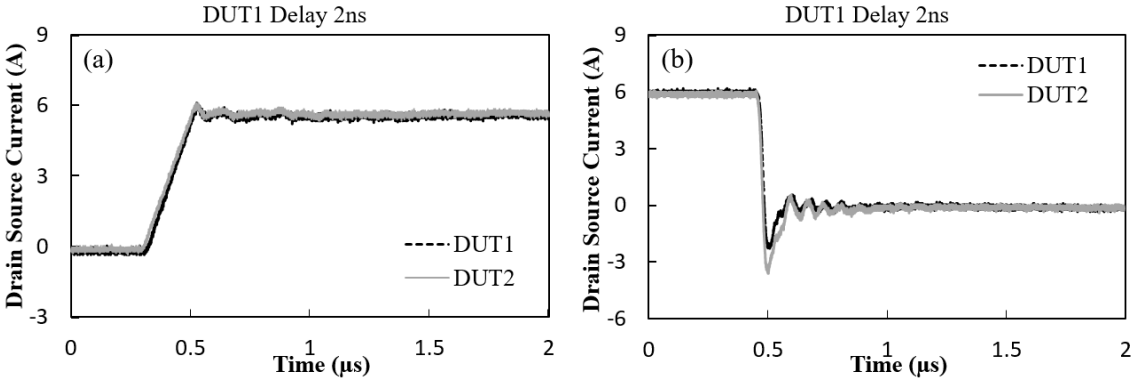


Figure 4.3: (a) Current switching transient characteristics for the parallel connected SiC power MOSFETs at turn-ON driven with 2 ns delay between the gate drivers (b) Similar measurements for turn-OFF.

As was mentioned previsouly, electrothermal variations were introduced by switching with different electrical time constants, different initial junction temperatures

and different cooling conditions. This has been done for SiC MOSFETs, silicon CoolMOS devices and silicon IGBTs.

4.2 The Impact of Switching Rate Mismatch

Figure 4.4(a) shows the turn-on current transient waveforms for the parallel connected SiC MOSFETs driven with different gate resistances while Figure 4.4(b) shows the same characteristics for the CoolMOS device. The supply voltage during the clamped inductive switching measurement was 300 V. It can be seen from Figure 4.4(a) and Figure 4.4(b) that the device with the smaller gate resistance switches faster thereby conducting more of the load current compared to the slower switching device during turn-ON. However, the difference between the currents in both devices is higher for the CoolMOS device compared to the SiC device in spite of the fact that the parallel pairs are driven with the same mismatch in gate resistance. This is due to the factor that the input capacitance of the CoolMOS device is larger than that of SiC MOSFET (datasheet shown in Appendix), leading to larger mismatch in switching speed. Figure 4.5(a) shows the measured turn-off characteristics for the parallel connected SiC MOSFETs switched with different rates while Figure 4.5(b) shows similar characteristics for the parallel CoolMOS devices. It can be seen in Figure 4.5, that contrary to Figure 4.4, the slower switching device conducts the bulk of the turn-off current because the entirety of the load current is diverted to it after the faster switching device is turned-off. Hence, at turn on, the faster switching devices experience higher power losses compared to the slower switching devices and at turn off, the converse is true.

The gate driving circuit typically consists an optocoupler which creates the isolation between the gate drive power supply and the power device. Since the optocoupler has a limited output current, therefore, there is need for a gate resistance connected between

the optocoupler and the power device to limit the current supplied. In addition, the gate resistance can be used to control the switching rate of the power device, ie, reduced switching rate for limiting peak reverse recovery currents in PiN diodes and controlling EMI in SiC MOSFETs. The switching rate of a power device is not only determined by the gate resistance used but also by the input capacitance of the device, the stray inductance in the gate connection as well as the parasitic source inductance amongst other factors. When power devices switch in parallel, variation in the gate resistance as well as the parasitic inductances can cause unsynchronised switching and a resulting electrothermal imbalance. In this thesis, variation in the gate resistance between parallel-connected devices is used since this is the most direct way of controlling the switching rate. Variation in the parasitic inductances and input capacitances will have the same resultant effect but to varying degrees depending on the magnitude of the variation.

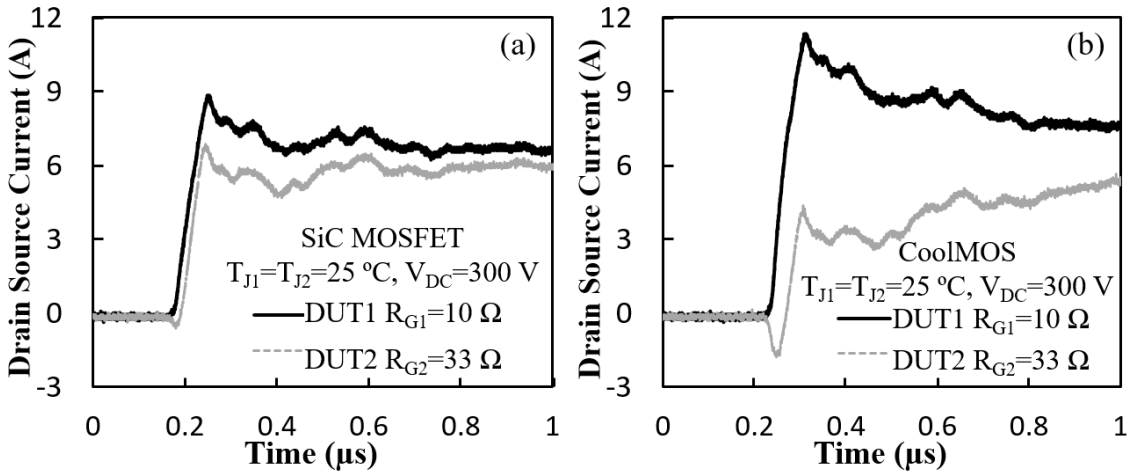


Figure 4.4: (a) Turn-ON current waveforms for parallel connected SiC MOSFETs with different switching rates. (b) Similar characteristics for the CoolMOS device.

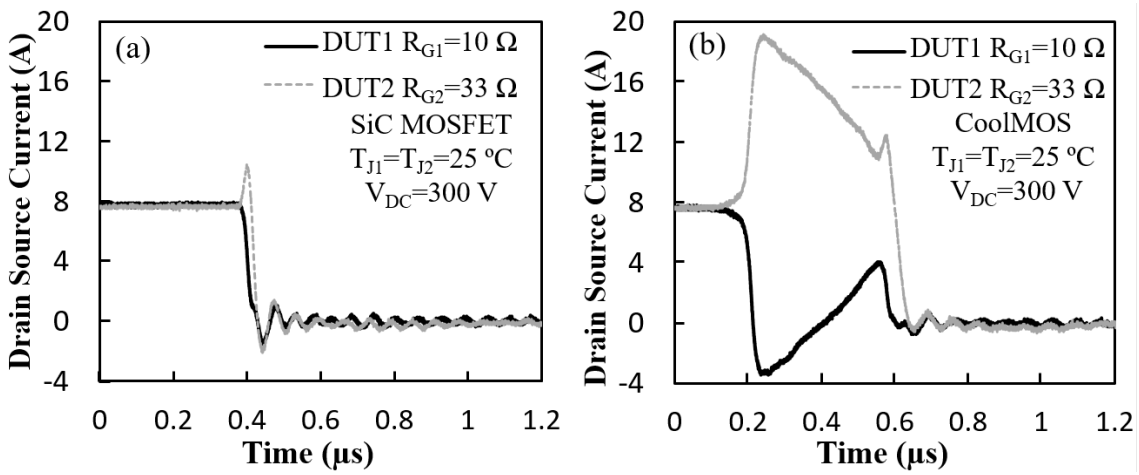


Figure 4.5: (a) Turn-OFF current waveforms for parallel connected SiC MOSFETs with different switching rates. (b) Similar characteristics for the CoolMOS device.

The measured switching energy is calculated by integrating the dissipated power (I_{DS}·V_{DS}) over the duration of the switching transients at turn-ON and turn-OFF. Figure 4.6 shows the measured turn-on switching energy for the parallel-connected SiC MOSFETs switched with different variations in switching rates i.e. $R_{G2} - R_{G1}$ where R_{G2} is the gate resistance of DUT2 and R_{G1} is the gate resistance of DUT1. The switching rate of DUT1 is held constant with a gate resistance R_{G1}=10 Ω while the switching rate of DUT2 is varied over a wide range of resistances.

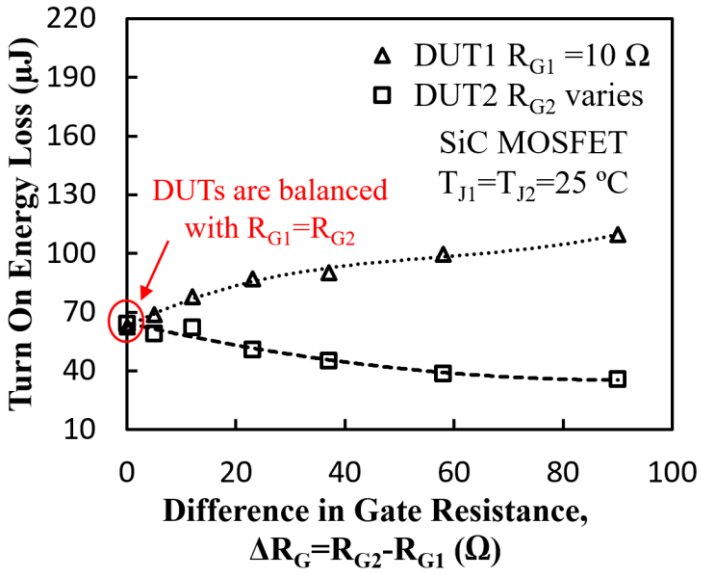


Figure 4.6: The measured turn-ON switching energies of the parallel connected SiC MOSFET as a function of the difference in gate resistance.

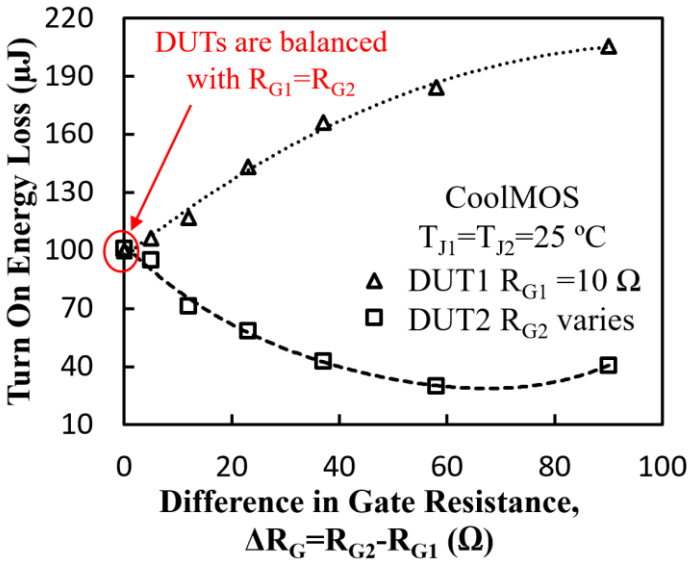


Figure 4.7: The measured turn-ON switching energies of the parallel connected CoolMOS devices as a function of the difference in gate resistance.

Figure 4.7 shows similar characteristics for the CoolMOS devices where the switching energies have been measured for each of the parallel DUTs switched at different rates. It is clear from Figure 4.6 and Figure 4.7 that, not only do the SiC MOSFETs have smaller switching losses than the CoolMOS devices, but that the devices can cope with imbalances in the switching rates better. The maximum change in switching energies between the parallel connected DUTs is 40% higher for the CoolMOS devices under the same variation in switching rates i.e. $\Delta R_G = R_{G2}-R_{G1}$. It can also be seen that this variation in switching energy (ΔE_{SW}) increases with the difference in switching rate (ΔR_G) for the CoolMOS while it is relatively more stable for the SiC devices i.e. $\Delta E_{SW}/\Delta R_G$ is higher for the CoolMOS than for the SiC device.

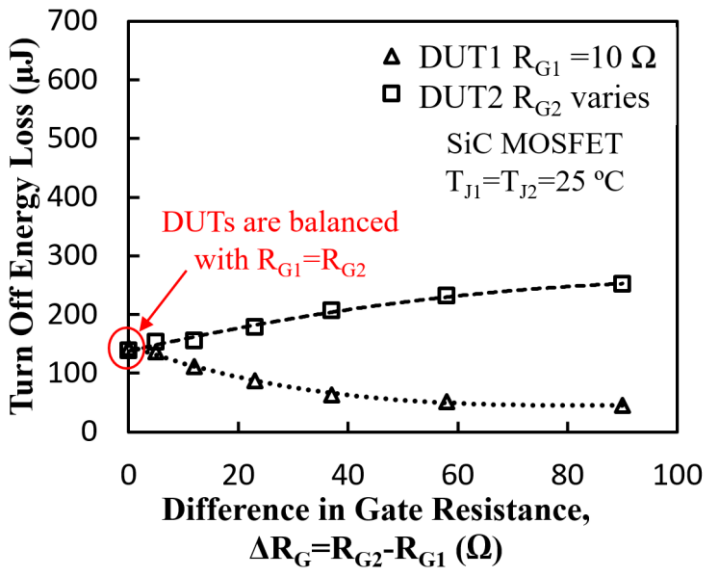


Figure 4.8: The measured turn-off switching energies of the parallel connected SiC MOSFET as a function of the difference in gate resistance.

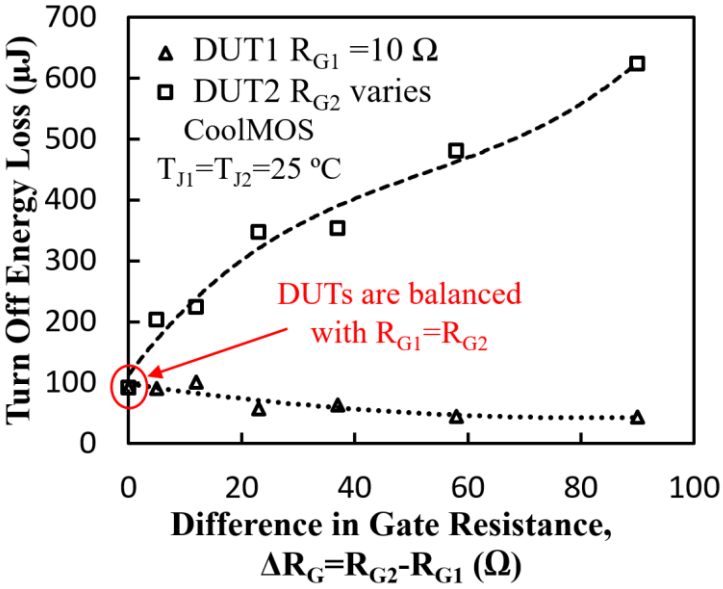


Figure 4.9: The measured turn-off switching energies of the parallel connected CoolMOS devices as a function of the difference in gate resistance.

Figure 4.8 shows the measured turn-OFF switching energy for the parallel connected SiC MOSFETs while Figure 4.9 shows that of the CoolMOS devices. Unlike the turn-ON characteristics shown in Figure 4.6 and Figure 4.7, the slower switching DUT exhibits higher switching energy. This is due to the current overshoots in the slower switching

device during turn-OFF as shown in Figure 4.5. It can also be seen from Figure 4.8 and Figure 4.9 that ΔE_{SW} at a given ΔR_G is smaller for SiC compared to the CoolMOS device. This correlates well with Figure 4.5, where the current overshoot in the slower switching CoolMOS device is much higher than that in the SiC MOSFET.

The case temperatures have also been measured for each of the parallel DUTs so as to ascertain how the variation in switching rates (ΔR_G) impacts the respective junction/case temperatures of the individual DUTs. Due to the smaller die size in SiC MOSFETs, the junction-to-case thermal resistance for the SiC MOSFET is 1.8 °C/W while that of the CoolMOS device is 0.6 °C/W. Figure 4.10(a) shows the measured case temperature rise for the parallel connected SiC MOSFETs with repetitive switching at a frequency of 2 kHz with DUT1 switched at 10 Ω and DUT2 switched at 33 Ω. Figure 4.10(b) shows similar characteristics for the CoolMOS devices. It can be seen in Figure 4.10 that the variation in the case temperature between the parallel-connected DUTs is higher for the CoolMOS device than for the SiC MOSFETs.

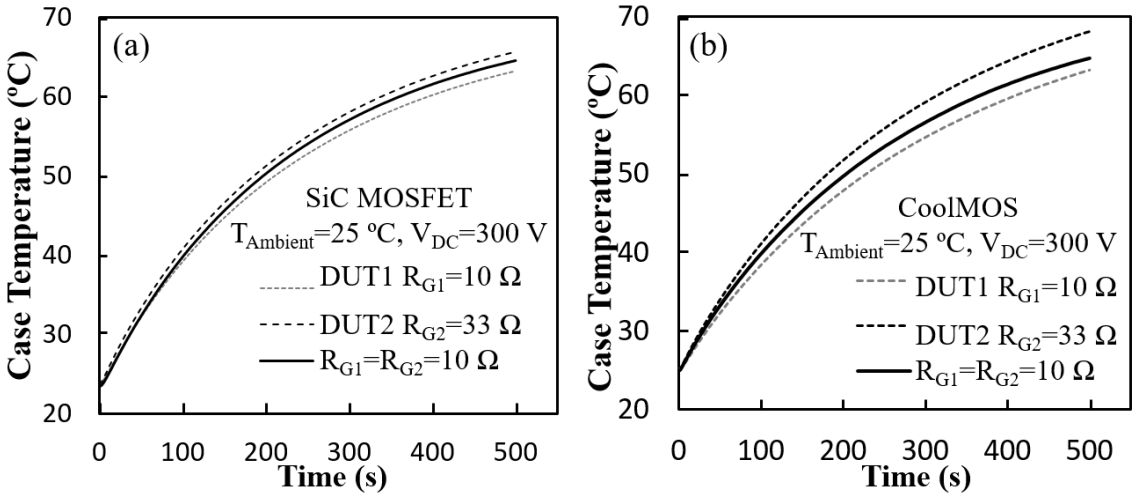


Figure 4.10: (a) The measured case temperature rise for the parallel connected SiC MOSFETs switched with R_G of DUT1 and DUT2 as 10 Ω and 33 Ω respectively. (b) Similar measurements for the CoolMOS device.

Figure 4.11 shows the measured steady state case temperatures for the parallel connected SiC MOSFETs repetitively switched at 2 kHz with different magnitudes of $\Delta R_G=R_{G2}-R_{G1}$. Figure 4.12 shows the same plot for the CoolMOS device. By comparing Figure 4.11 and Figure 4.12, it can be seen that the SiC MOSFETs show less temperature variation (ΔT_J) between the respective DUTs compared with the CoolMOS devices. Hence, the impact of mismatch in the switching rate of the parallel-connected devices results in less temperature mismatch for the SiC MOSFETs compared with the CoolMOS devices. The smaller die sizes and less temperature sensitive electrical parameters in SiC mean that variations in temperature and switching rate between the parallel connected DUTs result in less mismatch in switching energy and dissipated power. Though the R_G difference between parallel connected device may be minimal, the switching time constant ($\tau = RC$) could be enlarged as the input capacitance of MOS is proportion to the current rating. As a result, for high current rating application, the temperature difference can be serious though with a small difference in R_G.

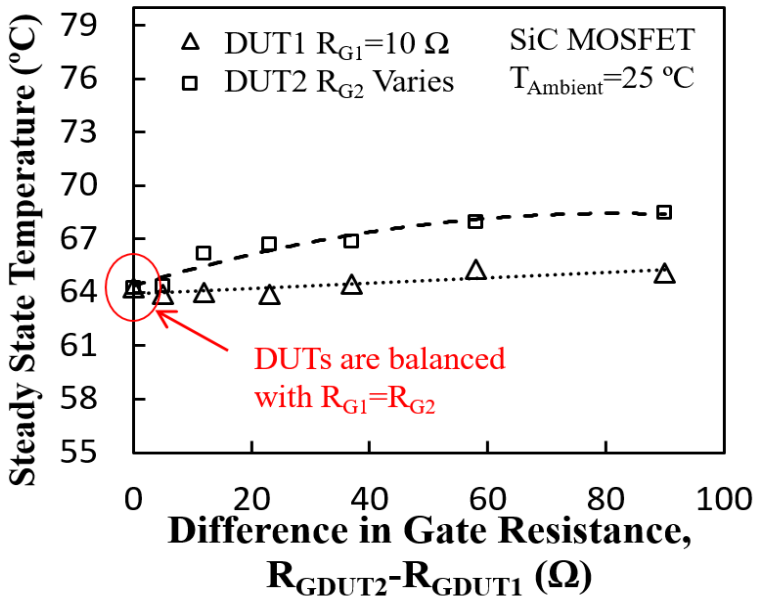


Figure 4.11: The measured case temperature rise for the parallel connected SiC MOSFETs switched at different rates.

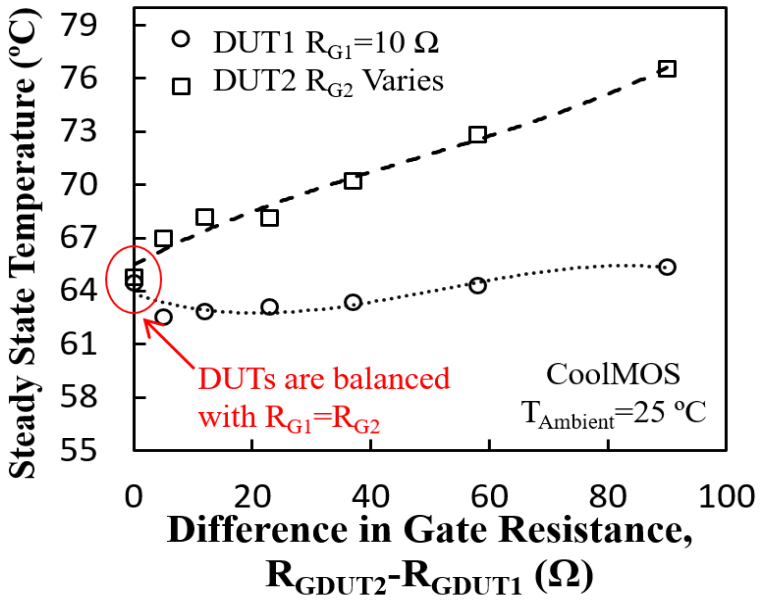


Figure 4.12: The measured case temperature rise for the parallel-connected CoolMOS devices switched at different rates.

Tables 4-1 and 4-2 show the measured temperature difference between the parallel-connected devices driven with different switching rates in the case of the SiC MOSFETs and the CoolMOS devices respectively. In the 3D graphs, both axes represent the gate resistances of the parallel pair and the temperature difference is simply the difference between the measured junction temperatures of both devices.

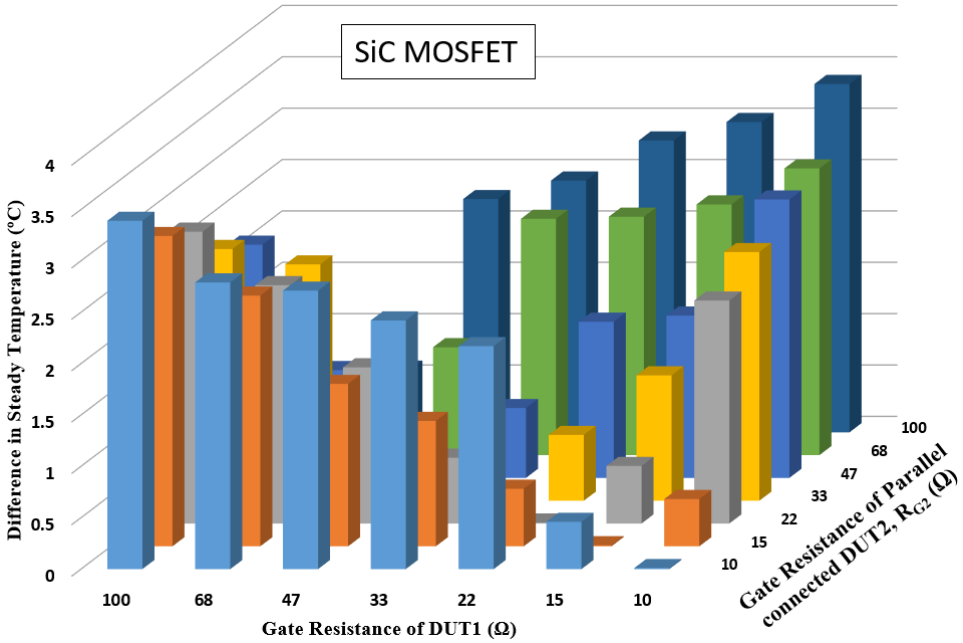


Table 4-1: Temperature Rise look up table for parallel-connected SiC MOSFETs switched with different gate resistance.

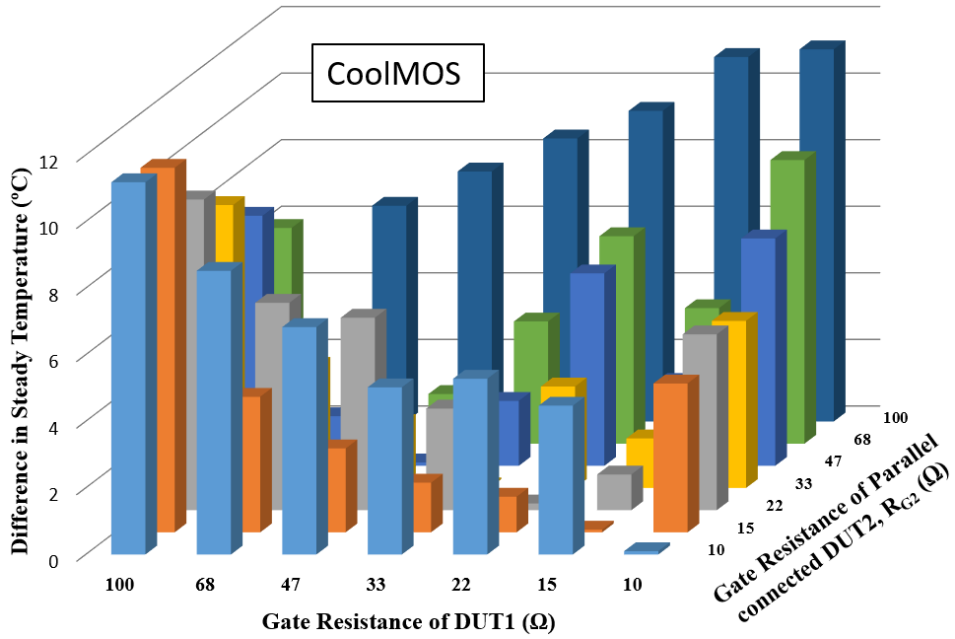


Table 4-2: Temperature Rise look up table for parallel-connected CoolMOS devices switched with different gate resistance.

4.3 Finite Element Simulations of Switching Rate Mismatch between Parallel DUTs

The experimental observations have been confirmed by the Finite Element simulator ATLAS. Table 4.3 shows the parameters used in the simulation of the devices. Lattice temperature heating was activated to make the simulation electrothermal. SRH and Auger recombination models were activated to properly account for minority carrier lifetime in the power devices. Temperature, surface field and ionised impurity scattering mobility models were activated in the simulator to account for the mobility degradation due to ionised dopants, phonon scattering at elevated temperatures as well as surface roughness scattering at the gate dielectric interface.

Parameter	**Value (SiC)**	**Value (CoolMOS)**	**Units**	**Source**
Gate-Source Oxide Thickness	50.0	80.0	nm	Literature
Gate-Drain Oxide Thickness	50.0	80.0	nm	Literature
Source doping	5×10^{19}	5.0×10^{20}	cm^{-3}	Literature
P-Body doping	1.0×10^{18}	1.0×10^{17}	cm^{-3}	Literature
P+ doping	1.0×10^{19}	N/A	cm^{-3}	Literature
N-drift layer doping	1.0×10^{16}	1.05×10^{15}	cm^{-3}	Calculated
N-drift layer thickness	7.0	58.0	µm	Calculated
N+ drain doping	2×10^{19}	5×10^{19}	cm^{-3}	Literature
N+ thickness	2.0	5.0	µm	Literature
Gate Resistance	10	10	Ω	Data Sheet
Junction-Case R_{TH}	1.8	0.6	K/W	Data Sheet
Die Area	1.5	10.5	mm^2	Experiment
p-pillar doping	N/A	1.05×10^{15}	cm^{-3}	Literature

Table 4-3: Parameters of the simulated finite element model.

Figure 4.13 and 4.14 show the simulated SiC MOSFET and CoolMOS devices with the mesh definition and doping profile around the channel area. Subsequent TCAD figures presented in this thesis are intended to show the direction of current flow and the temperature distribution within the device at different stages of the device switching.

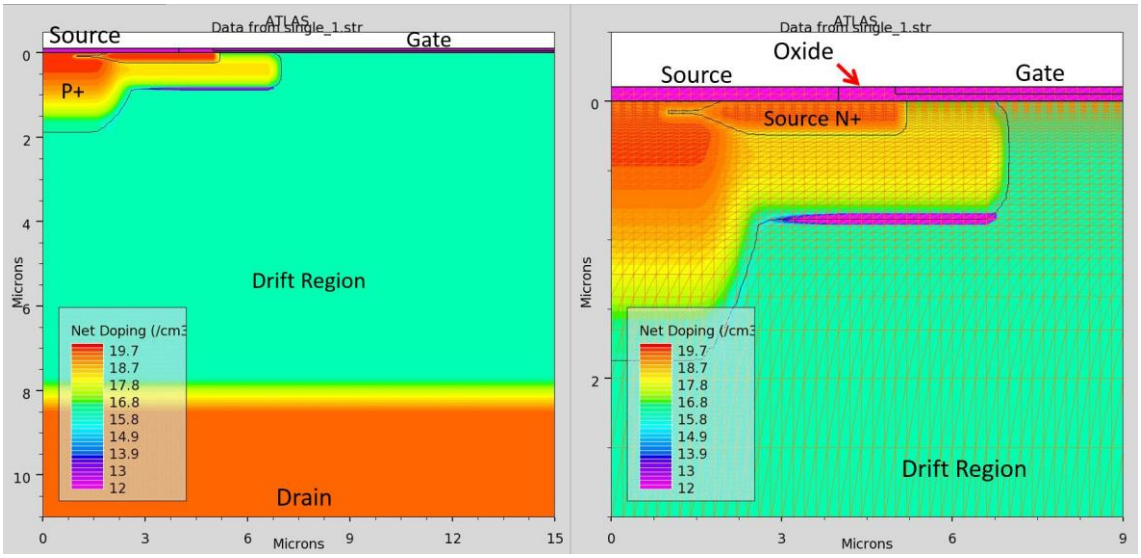


Figure 4.13: SiC MOSFET TCAD Model showing the doping profile and the meshes.

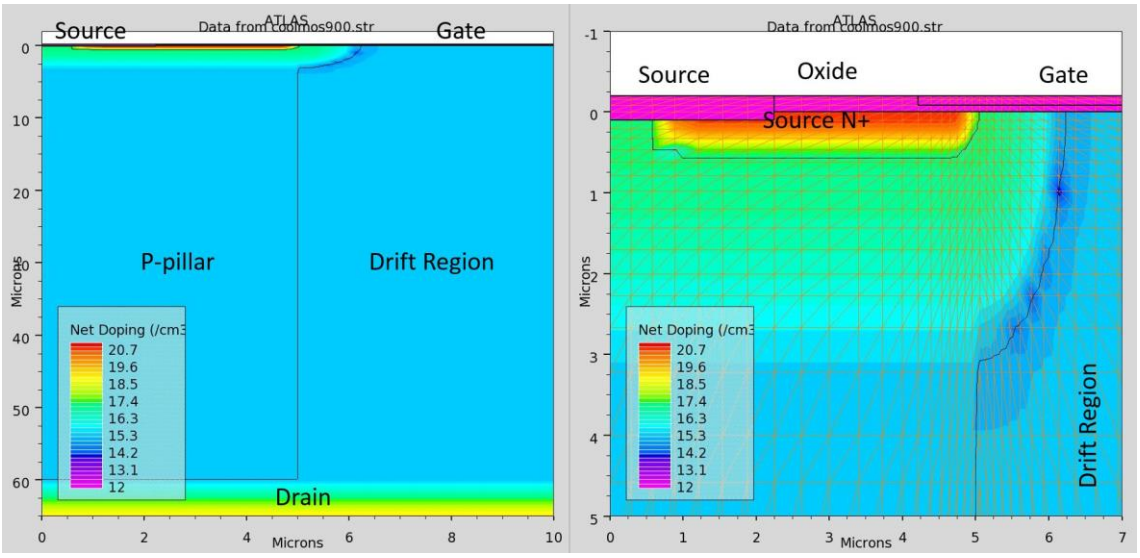


Figure 4.14: CoolMOS TCAD Model showing the doping profile and the meshes.

Figure 4.15 shows the simulated switching waveforms of the double pulse test consisting of the inductor charging phase as well as the turn-OFF and turn-ON transients for the

parallel connected SiC MOSFETs with different gate resistance. Figure 4.16(a) shows the simulated turn-ON waveforms for the parallel SiC MOSFETs while Figure 4.16(b) show the simulated turn-OFF waveforms. The peak overshoot in DUT1 during turn-ON and in DUT 2 during turn-OFF can be observed as was the case in the measurements. Figure 4.17 shows the 2-D current density contour plots of the parallel-connected SiC MOSFETs corresponding to point X in the turn-ON transient in Figure 4.16(a). It can be seen that the simulated MOSFET with smaller gate resistance has a higher current density in the channel. Figure 4.18 shows the 2-D current density contour plot corresponding to point Y in the turn-OFF transient in Figure 4.16(b). As the DUT on the RHS of Figure 4.18 turns-OFF quicker, the voltage across the DUTs increases and as a result, the current is more concentrated in pinch-OFF ($V_{DS} > V_{GS} - V_{TH}$) rather than a disperse current within the drift region for both DUTs when in linear mode ($V_{DS} < V_{GS} - V_{TH}$).

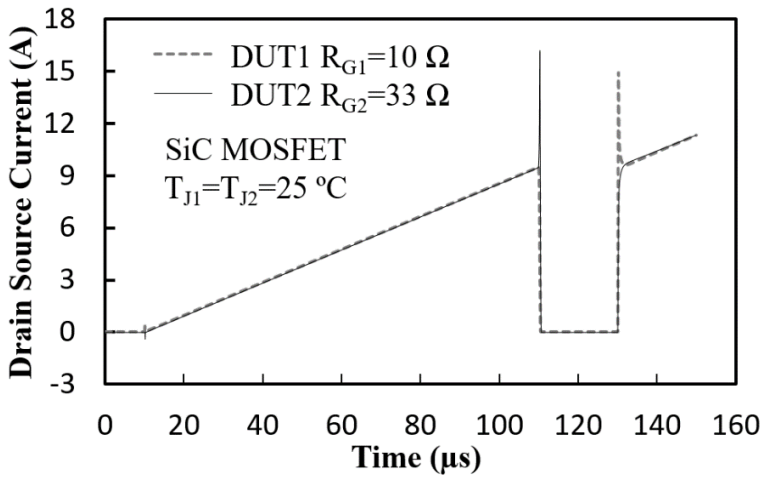


Figure 4.15: The simulated current waveforms for the parallel connected SiC MOSFETs switched with different gate resistance.

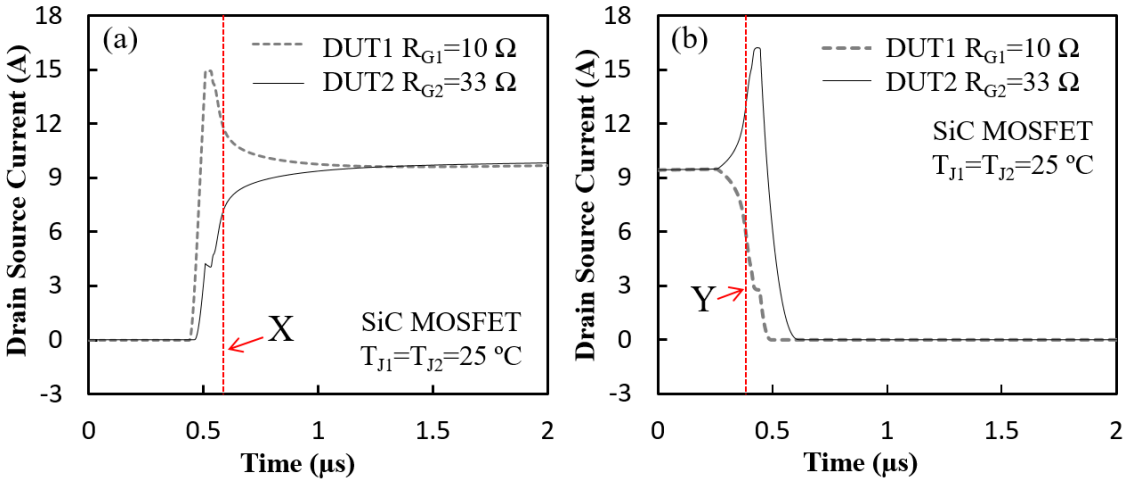


Figure 4.16: The simulated (a) turn-ON and (b) turn-OFF current waveforms for the parallel connected SiC MOSFET switched with different gate resistance.

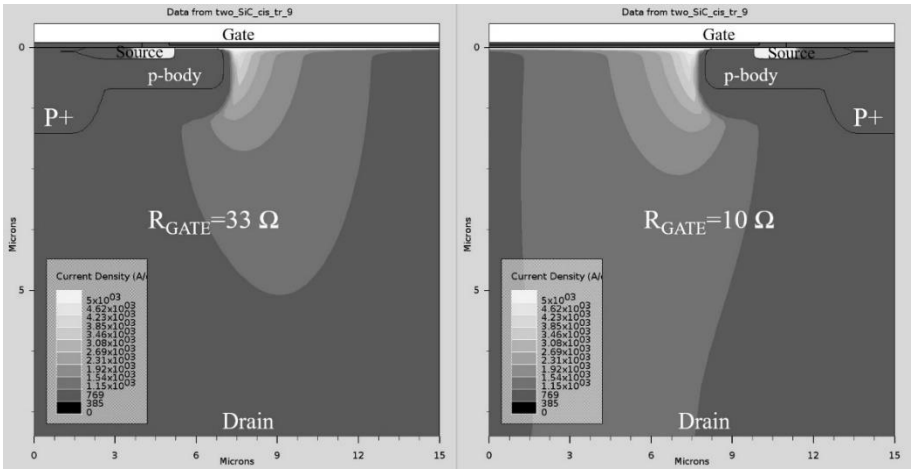


Figure 4.17: The 2-D current density contour plot for the parallel connected SiC MOSFETs with different switching rate corresponding to point X in Figure 4.16(a).

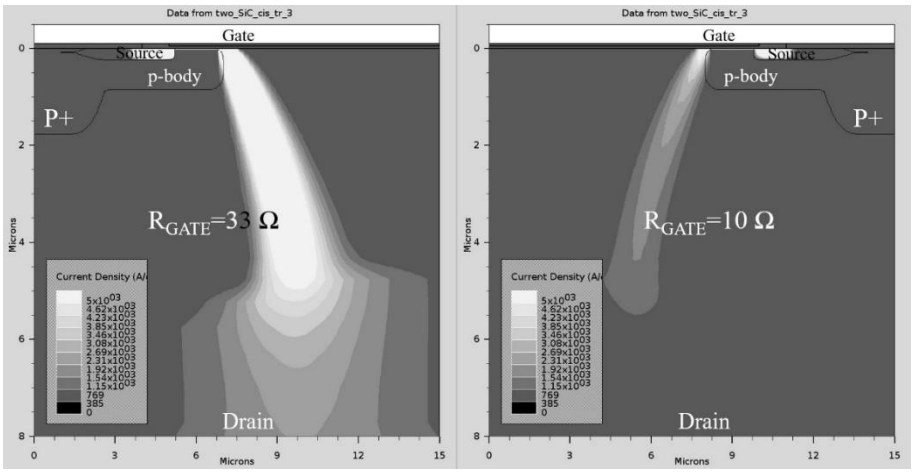


Figure 4.18: The 2-D current density contour plot for the parallel connected SiC MOSFETs with different switching rate corresponding to point Y in Figure 4.16(b).

Similar finite element simulations have been done for the CoolMOS devices using the parameters in Table 4-3. Figure 4.19 shows the simulated switching transient for the parallel connected CoolMOS devices switched with different gate resistance. It can be seen by comparing Figure 4.19(a) with 4.16(a) that the CoolMOS device exhibits larger current difference during the turn-ON compared to the SiC MOSFETs. By comparing the CoolMOS simulations with the SiC simulations, it can be seen that the time-lag between the turn-ON and turn-OFF of the parallel DUTs is larger for the CoolMOS. This is due to the larger gate-source and Miller capacitances which means the CoolMOS devices switch slower and have higher switching losses compared to the SiC MOSFETs. Figure 4.20 and Figure 4.21 show the 2-D current density contour plots at turn-ON and turn-OFF respectively for the parallel connected CoolMOS devices switched with different gate resistance. Also, the current densities in the CoolMOS devices are lower because the current is spread over a larger area within the device. This is due to the p-pillar in the CoolMOS device that causes lateral depletion in addition to the vertical depletion.

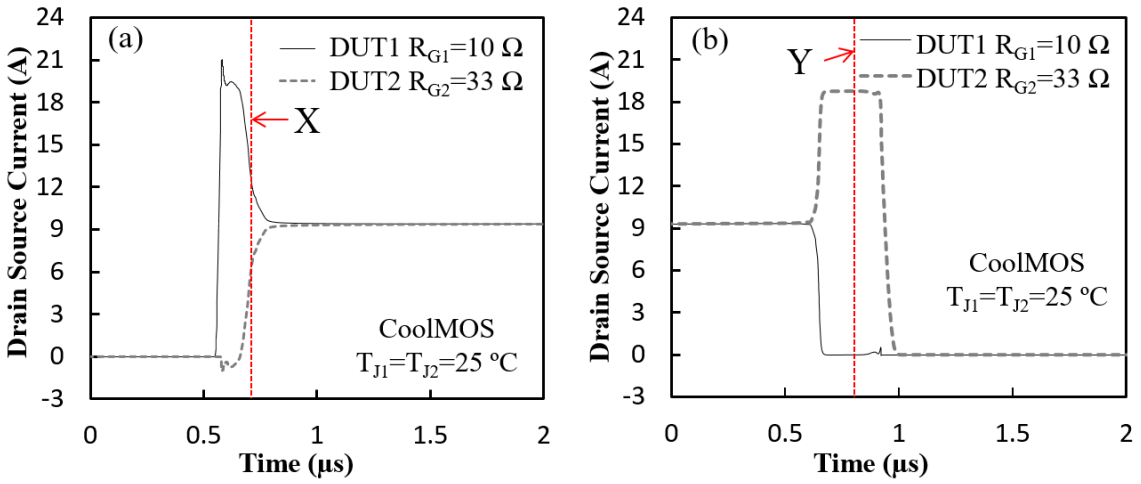


Figure 4.19: (a) turn-ON and (b) turn-OFF current waveforms for the parallel-connected CoolMOS devices switched with different gate resistance.

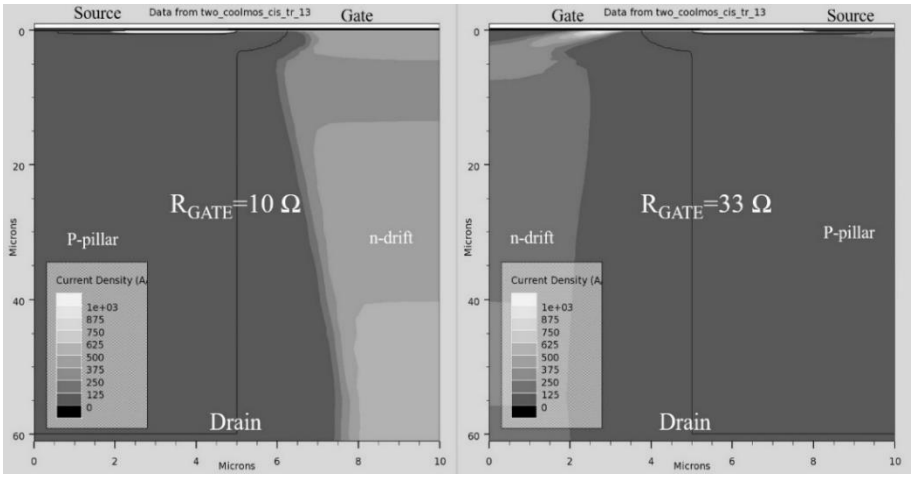


Figure 4.20: The 2-D current density contour plot for the parallel connected CoolMOS devices with different switching rate corresponding to point X in Figure 4.19(a).

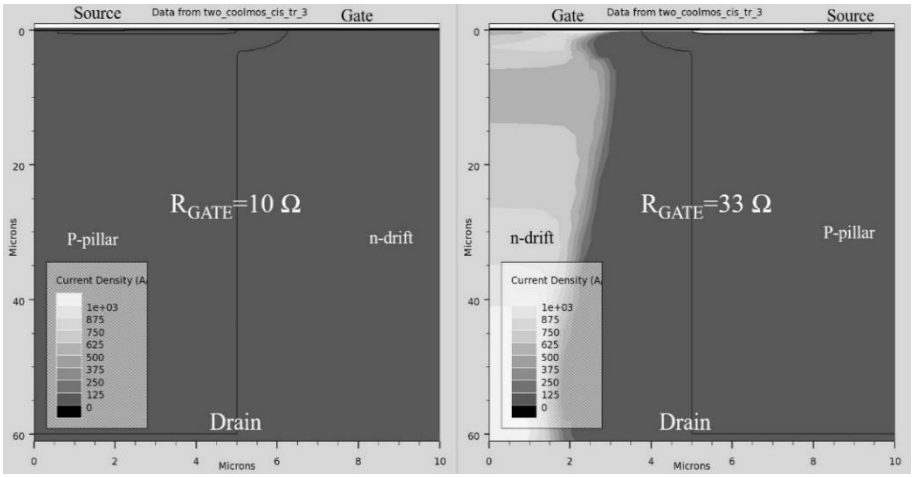


Figure 4.21: The 2-D current density contour plot for the parallel connected CoolMOS devices with different switching rate corresponding to point Y in Figure 4.19(b).

4.4 Impact of Initial Junction Temperature Mismatch

Similar measurements have been performed for parallel-connected devices, however, with different initial junction temperatures. The initial junction temperatures are set by electric hot-plates connected to the base of the device. Since the system is at steady-state, it can be assumed that the case temperature is equal to the junction temperature. Figure 4.22(a) shows the turn-ON current for the parallel connected SiC MOSFETs with different junction temperatures set by the heaters. Again, V_{DS}=300 V. Figure 4.22(b)

shows a similar plot for the CoolMOS devices. Figure 4.22 shows that the hotter device takes less current as expected because of the positive temperature coefficient of the on-state resistance and the current divider rule which stipulates that the more current flows through the more conductive device. By comparing the SiC and CoolMOS characteristics it can be seen that the steady state current mismatch is less for the SiC device compared with the CoolMOS device. This is due to the fact that SiC is more temperature resilient since its wide bandgap ensures that thermally generated carriers for any given temperature are smaller compared to those in silicon devices.

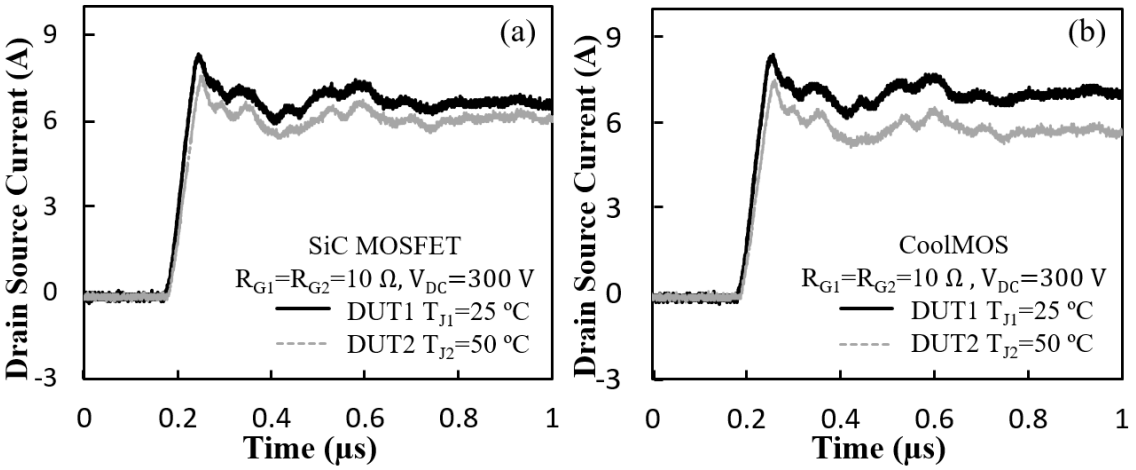


Figure 4.22: (a) The measured turn-ON current for the parallel connected SiC MOSFETs driven at 2 different junction temperatures. (b) Similar measurements for the CoolMOS device.

Figure 4.23 shows the measured turn-on energy of the parallel connected SiC MOSFETs with different magnitudes of initial junction temperature mismatch between the DUTs i.e. DUTs set at different $\Delta T_J = T_{J2} - T_{J1}$ where T_{J2} is the junction temperature of DUT2 and T_{J1} is the junction temperature of DUT1. In Figure 4.23, the junction temperature of DUT1 is held constant at 25 °C while the junction temperature of DUT2 is varied over a wide temperature range. Figure 4.24 shows similar characteristics for the CoolMOS device. It can be seen from Figure 4.23 and Figure 4.24 that the turn-on energy of the device at the higher junction temperature is lower. This is expected in MOSFETs

because the turn-on dI_{DS}/dt decreases with temperature as a result of the negative temperature coefficient of the MOSFET threshold voltage.

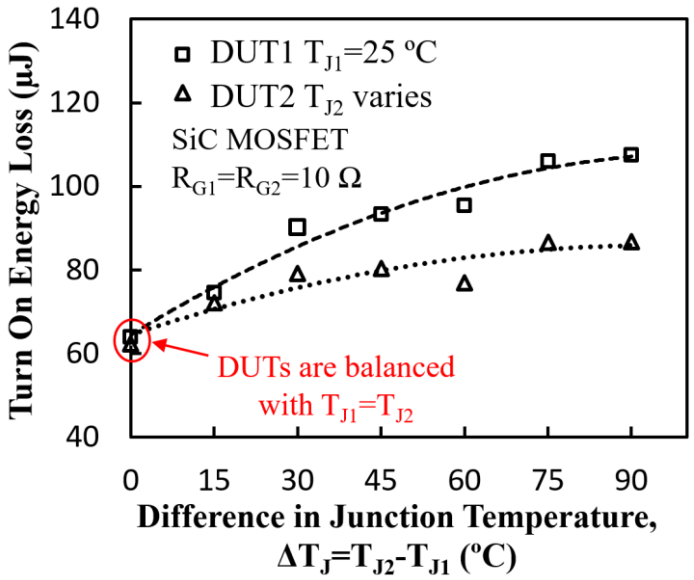


Figure 4.23: Measured turn-ON switching energy for the parallel connected SiC MOSFETs with the DUTs set at different junction temperatures.

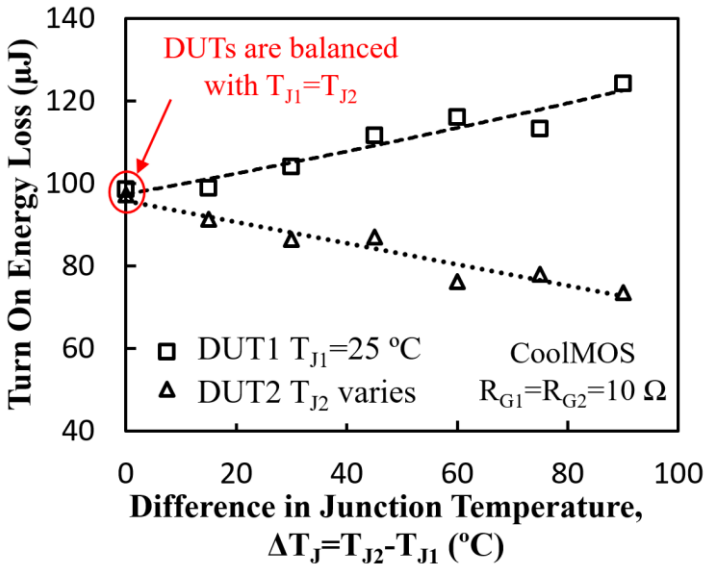


Figure 4.24: Measured turn-on switching energy for the parallel-connected CoolMOS devices with the DUTs set at different junction temperatures.

It can also be seen by comparing Figure 4.23 with Figure 4.24 that the difference in turn-on energy loss ($\Delta E_{SW\,ON}$) between the parallel-connected DUTs is smaller in SiC and remains more stable as ΔT_J is increased. Hence, it is demonstrated that parallel-connected

SiC MOSFETs perform better than CoolMOS devices under both temperature and switching rate imbalances. As can be seen from the CoolMOS measurements in Figure 4.24, increasing the temperature difference (ΔT_J) between the parallel DUTs results in much higher switching energy variation ($\Delta E_{SW\,ON}$) compared with the SiC MOSFETs.

Figure 4.25 shows the measured turn-OFF switching energy for the parallel connected SiC MOSFETs while Figure 4.26 shows that of the CoolMOS device. By comparing Figure 4.25 with Figure 4.26, it can be seen that the turn-OFF energy loss is again more stable than the CoolMOS device. For the SiC MOSFET, the turn-OFF energy is reducing the temperature difference (ΔT_J), this is due to the factor that the hotter device conducts less current before it turns off. However for the CoolMOS devices, both turn-Off energy loss increases with temperature difference. This result from two factors, one is the current conducts through the cooler DUT1 before turn off increases with temperature difference, hence it has more turn-OFF switching loss. The second is as the junction temperature of DUT2 increase, it has more current oscillation after the turn-Off, and this amount of loss has been counted into the turn-Off switching loss ($E_{SW\,OFF}$).

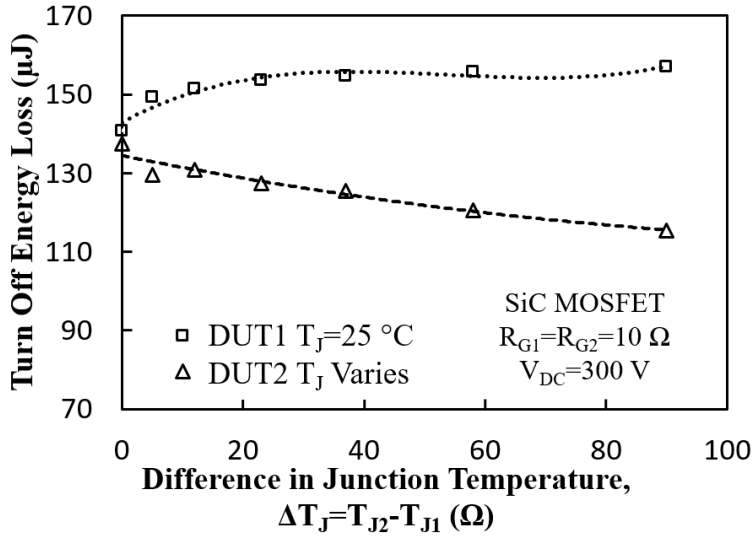


Figure 4.25: Measured turn-OFF switching energy for the parallel connected SiC MOSFETs with the DUTs set at different junction temperatures.

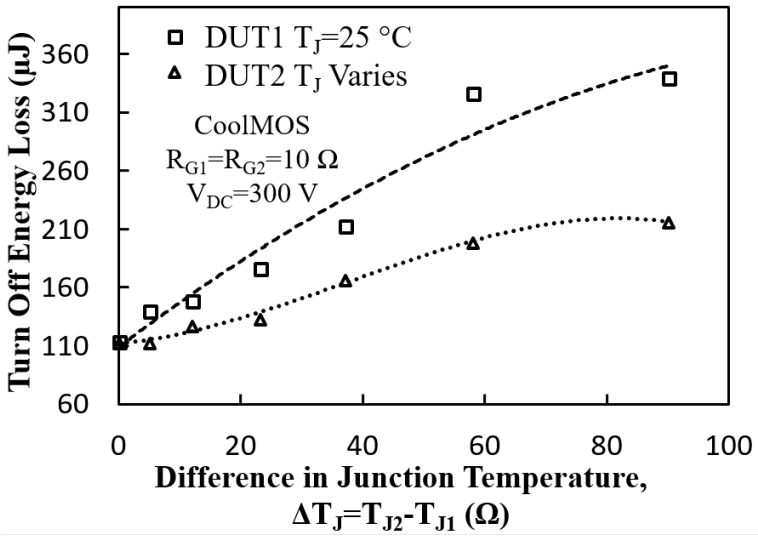


Figure 4.26: Measured turn-Off switching energy for the parallel-connected CoolMOS devices with the DUTs set at different junction temperatures.

4.5 Finite Element Simulations of Initial Junction Temperature Mismatch

The variations in the initial junction temperature for the parallel-connected SiC MOSFET and CoolMOS devices have been modelled by ATLAS. Figure 4.27 shows the simulated waveform for the parallel-connected SiC MOSFETs switched at different initial junction temperature. It can be seen that the cooler DUT conducts more current therefore having a larger dI/dt during the inductor charging phase.

Figure 4.28 shows the turn-ON and turn-OFF transient for the parallel-connected SiC MOSFETs switched at different junction temperature. Figure 4.29 and Figure 4.30 shows the 2-D current density contour plot during turn-ON and turn-OFF respectively for the SiC MOSFETs. It can be seen that the DUT switched with the lower junction temperature conducts more steady state current than the DUT at higher initial junction temperature. The simulations show that the switching transients are well synchronised since the gate resistance is not affected by temperature although on closer inspection, the DUT with the higher junction temperature will switch marginally sooner than the DUT with the lower

junction temperature because of the negative temperature coefficient of the threshold voltage. Therefore, there is current spike for the hotter DUT as shown in Figure 4.28. However, the 2-D plots show an increased current spreading in the drift region of the DUT with the lower junction temperature.

Figure 4.31 shows the similar simulation characteristics for the parallel-connected CoolMOS devices. By comparing Figure 4.31 with Figure 4.28, it is clear to see that the SiC MOSFETs have a smaller current difference between the parallel DUTs than the CoolMOS devices for the same difference in junction temperature. Figure 4.32 and 4.33 show the 2-D current density contour plots for the parallel-connected CoolMOS devices during turn-ON and turn-OFF respectively. Again, it can be seen that current only flows in the N-pillar of the super-junction layer. It can also be seen that the current density is higher in the CoolMOS device simulated with the lower junction temperature.

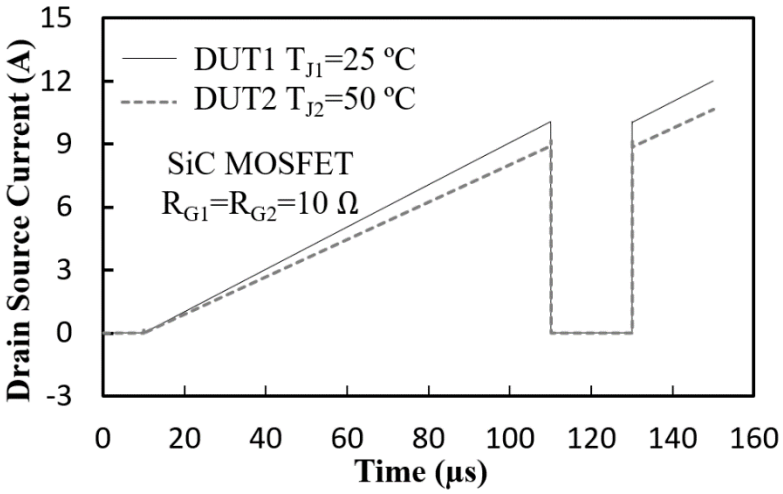


Figure 4.27: The simulated current waveforms for the parallel connected SiC MOSFETs switched at different initial junction temperatures.

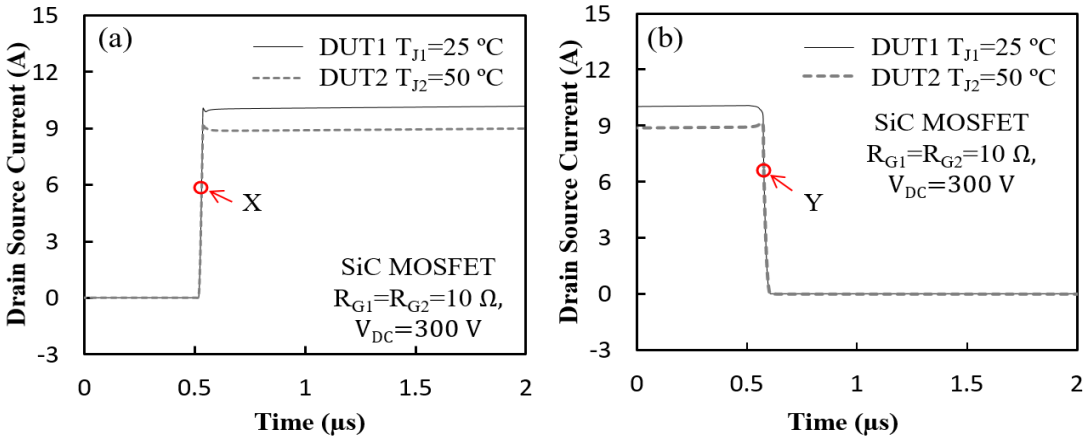


Figure 4.28: The simulated (a) turn-ON and (b) turn-OFF current waveforms for the parallel connected SiC MOSFETs switched with different initial junction temperatures.

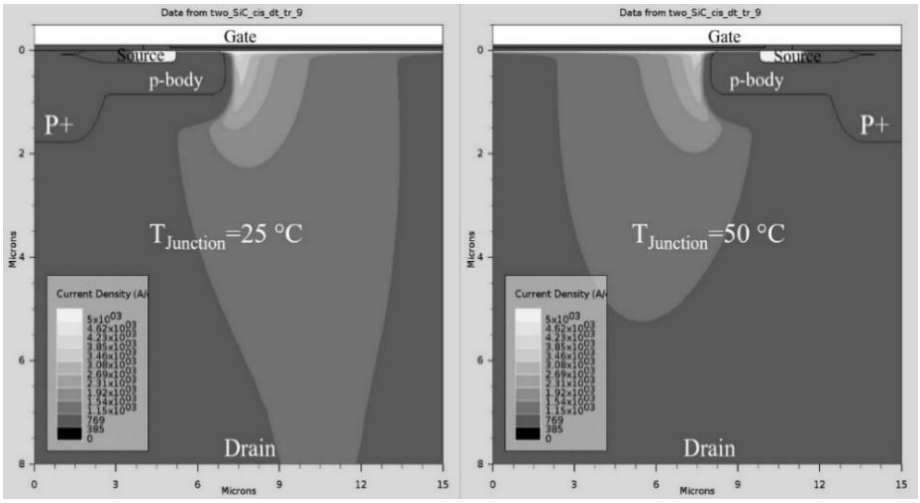


Figure 4.29: The 2-D current density contour plot for the parallel connected SiC MOSFETs switched at different junction temperature corresponding to point X in Figure 4.26(a).

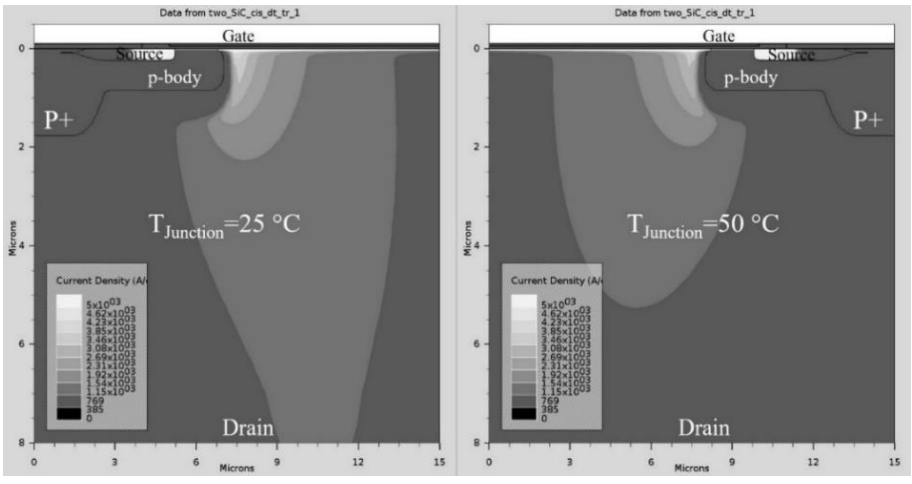


Figure 4.30: The 2-D current density contour plots for the parallel connected SiC MOSFETs switched at different junction temperature corresponding to point Y in Figure 4.26(b).

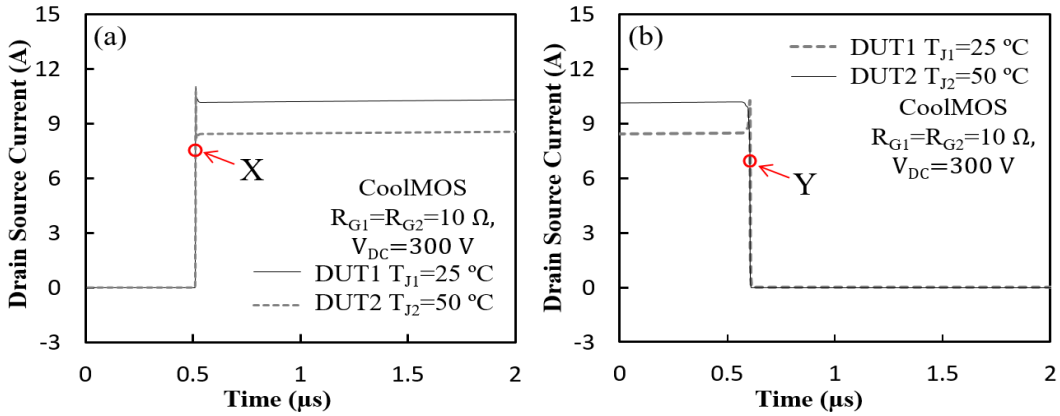


Figure 4.31: The simulated (a) turn-ON and turn-OFF currents for the parallel connected CoolMOS devices switched at different initial junction temperatures.

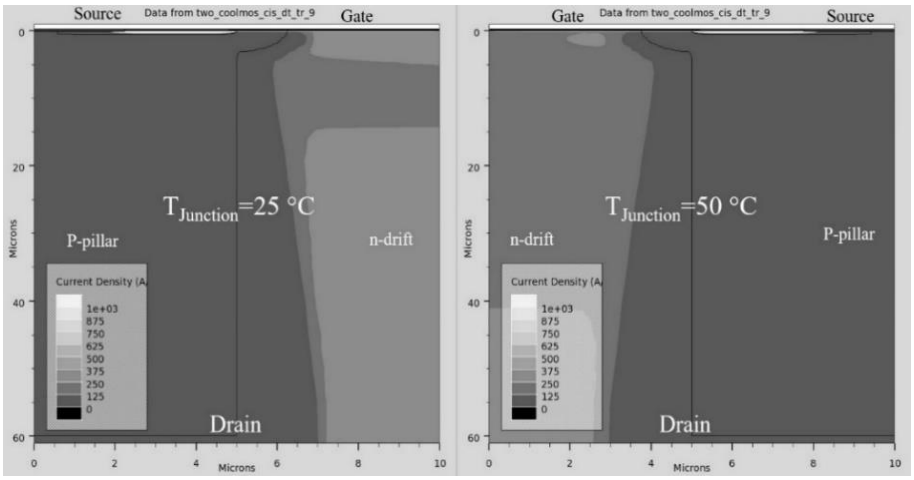


Figure 4.32: 2-D current density contour plot for the parallel connected CoolMOS devices switched at different junction temperatures corresponding to point X in Figure 4.31(a).

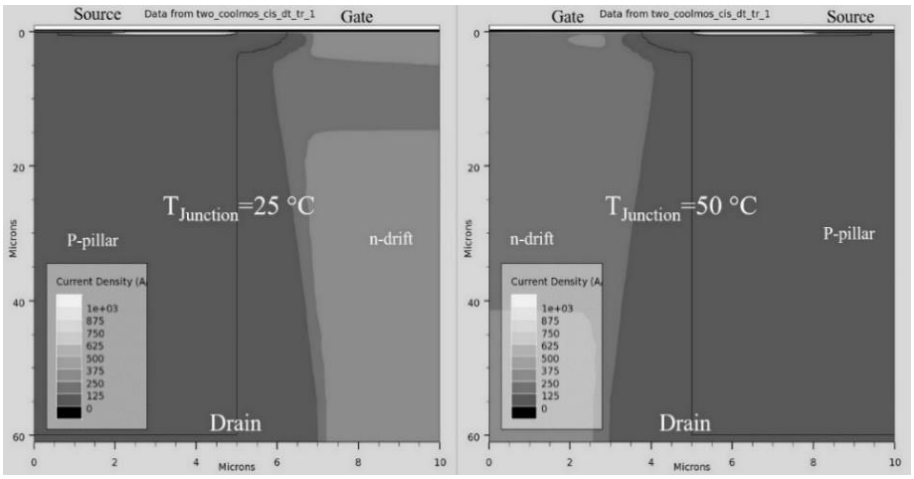


Figure 4.33: 2-D current density contour plots for the parallel connected CoolMOS devices switched at different junction temperatures corresponding to point Y in Figure 4.31(b).

4.6 Impact of Temperature Variations on Parallel Connected NPT IGBTs

In this section, the impact of electrothermal variations on parallel conducting IGBTs are investigated experimentally. With trench gate and field stop technologies, the latest IGBTs are able to block higher voltages with less conduction (V_{CEsat}) and switching losses (Esw_{off}). IGBTs, depending on the epitaxial layer architecture, can be classified as Punch-Through (*PT*) or Non-Punch-Through (*NPT*) IGBTs. While PT IGBTs exhibit lower conduction and switching losses as a result of the additional n+ buffer layer between the n-drift layer and the p+ collector, however, the on-state resistance of PT IGBT has a negative temperature coefficient. This makes parallel connection of PT-IGBTs a reliability risk since the probability of thermal runaway is high i.e. the hotter IGBT conducts more current which causes a positive feedback loop between current and temperature. On the other hand, the on-state resistance of the NPT IGBT has a positive temperature coefficient, which makes it better suited for high current applications where parallel dies are required. In this case, the hotter device conducts less current which cools it down thereby resulting in a stable negative feedback loop between current and temperature.

In this section, parallel-connected NPT IGBTs have been measured with electrothermal variation between the devices. An example of the results is presented in Figure 4.34 where two IGBTs are connected in parallel and are switching current with different initial junction temperatures. Figure 4.34 shows the collector current of the 2 IGBTs during the initial inductor charging phase and the clamped inductive switching phase. It can be seen that the hotter IGBT (with initial T_J=55 °C) initially exhibits a higher turn-ON *dI/dt* due to the lower threshold voltage. However, as the DUTs are properly turned ON, the cooler device with T_J=25 °C conducts more current. Hence, during the initial inductor charging phase the negative temperature coefficient of the threshold

voltage dominates at low collector currents while the positive temperature coefficient of the ON-state resistance dominates at high currents. The second pulse of the double pulse test is the more important one since this more closely emulates actual switching conditions in power converters.

Figure 4.35 shows the waveforms of the second pulse for the parallel-connected IGBTs switched with different initial junction temperatures for (a) a junction temperature difference of 20 °C and (b) a junction temperature difference of 80 °C. It can be seen that in both cases, the cooler device conducts more current thereby indicating that the positive temperature coefficient of the ON-state resistance dominates. However, the electrical current difference between the 2 parallel DUTs does not increase with temperature. This is due to 2 conflicting effects in temperature dependence of the IGBTs ON-state resistance.

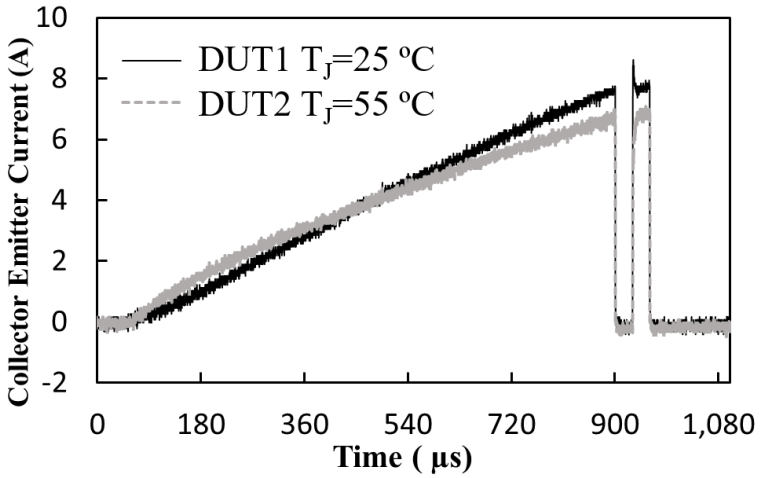


Figure 4.34: The measured current waveform of parallel-connected IGBTs switched with different initial junction temperatures (25 ºC and 55 ºC).

These effects are (i) The effective mobility of the carriers in the MOS channel decrease with increasing resistance as a result of increased phonon-scattering and (ii) the minority carrier lifetime in the voltage blocking drift layer increases with temperature i.e. as the minority carrier lifetime increases, the plasma in the drift region becomes less resistive. Depending on the IGBT, these competing effects will have different manifestations. In

the case of this IGBT, there is some initial increase with the ON-state resistance with temperature, however, after a certain temperature, the increase in the minority carrier lifetime becomes dominant and cancels out the lower mobility.

Figure 4.36 shows the current turn-ON and turn-OFF transients of the parallel connected IGBTs driven with different initial junction temperatures. It can be seen from Figure 4.36, that the turn-ON *dI/dt* is higher for the IGBT with the cooler junction temperature (25 °C) compared to the hotter junction temperature (55 °C).

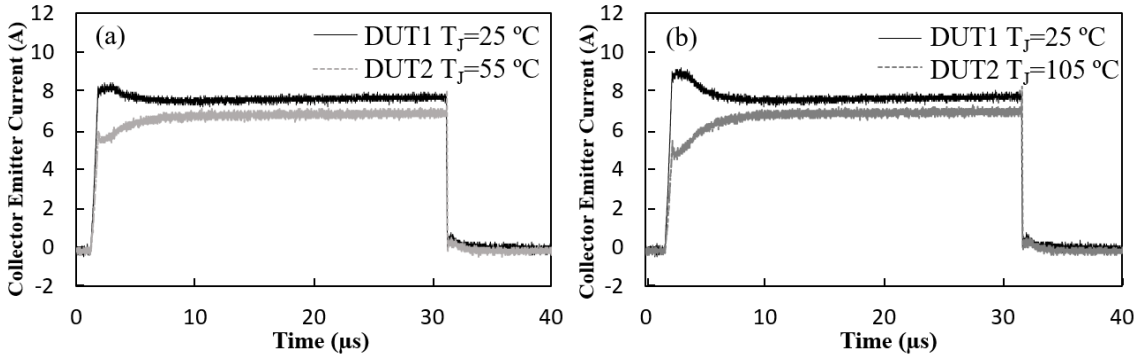


Figure 4.35: The measured current waveform of parallel connected IGBTs switched with different junction temperatures (a) Junction temperature of DUT1=25 ºC and DUT2=55 ºC. (b) Junction temperature of DUT1=25 ºC and DUT2=105 ºC.

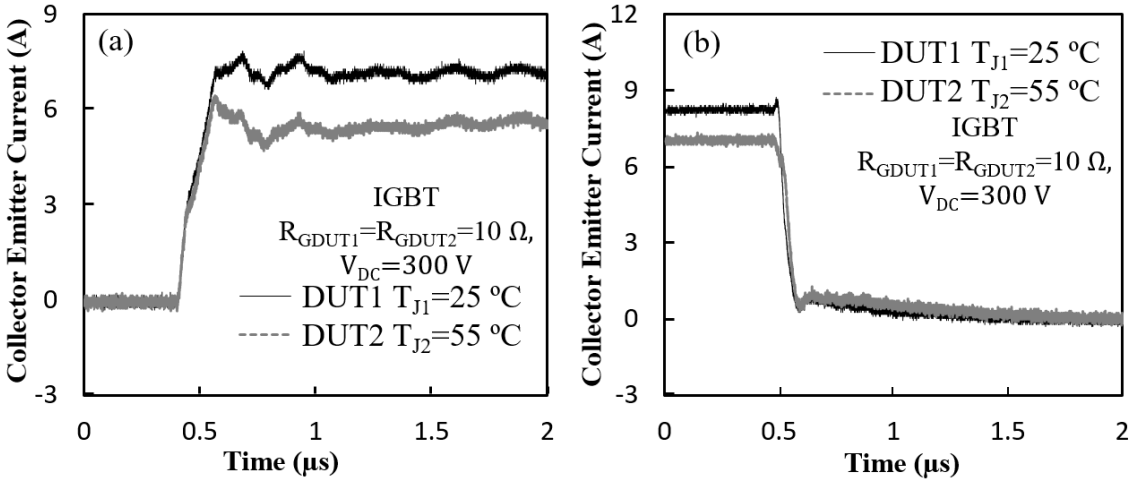


Figure 4.36: The measured (a) turn on and (b) turn off waveform of parallel connected IGBTs switched at different initial junction temperature.

This is a result of the increased carrier lifetime causing a higher forward reverse recovery charge in the hotter IGBT, thereby resulting in a lower *dI/dt* since the forward charge must first be formed in the drift region before the device can conduct the current.

Figure 4.37 shows the measured turn-ON energy as a function of initial junction temperature difference for the parallel-connected devices with different junction temperatures. It can be seen from Figure 4.37 that the cooler IGBT, which is DUT1, with the initial junction temperature of 25 ºC, has a higher switching loss compared to the hotter IGBT. It can also be seen that the switching energy difference between the parallel connected IGBTs increases with the difference in the initial junction temperature. As the difference in the junction temperature between the parallel DUTs increases, the magnitude of the difference of the current conducted increases correspondingly because of the increase in the difference between the ON-state resistances. The cooler IGBT is forced to conduct the bulk of the load current since it has a smaller forward recovery charge i.e. it takes less time for plasma formation in the drift region since the minority carrier lifetime is smaller.

Figure 4.38 shows the measured turn-OFF switching energies between the parallel connected IGBTs with different initial junction temperatures as a function of the junction temperature difference. It can be seen that unlike the unipolar device, the hotter IGBT (DUT2) exhibits larger switching energy and it increases with the junction temperature. And as the junction temperature difference increases, the turn-Off energy loss ($E_{SW\,OFF}$) of the cooler IGBT (DUT1) is constant likely. This is due to the factor, as shown in Figure 4.35, the current conduct by the cooler DUT1 before turn-Off is not changing much with the junction temperature of DUT2 therefore the turn-Off energy loss is not changing with difference in junction temperature. On the other hand, the junction temperature increase

result in longer turn-off time due to the current tail as a result of recombination, thereby the turn-Off energy loss is increasing with junction temperature for the DUT2.

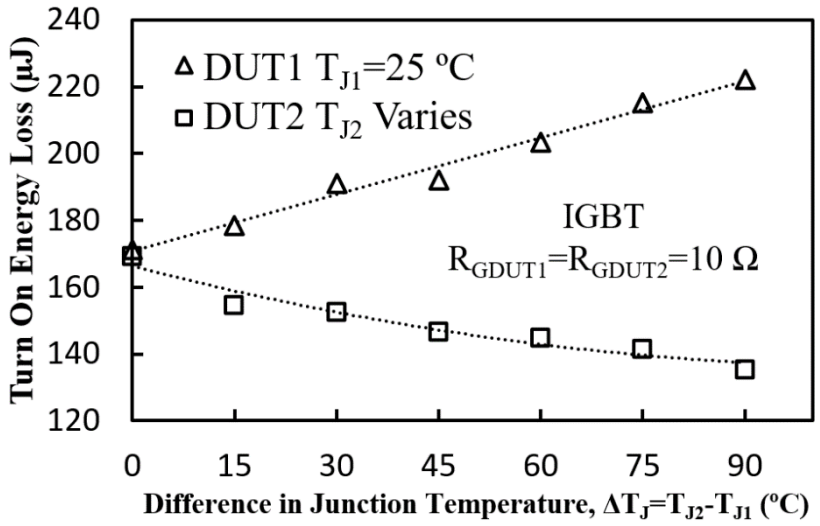


Figure 4.37: The measured turn-ON switching energies of the parallel-connected IGBT devices with the DUTs set at different junction temperatures.

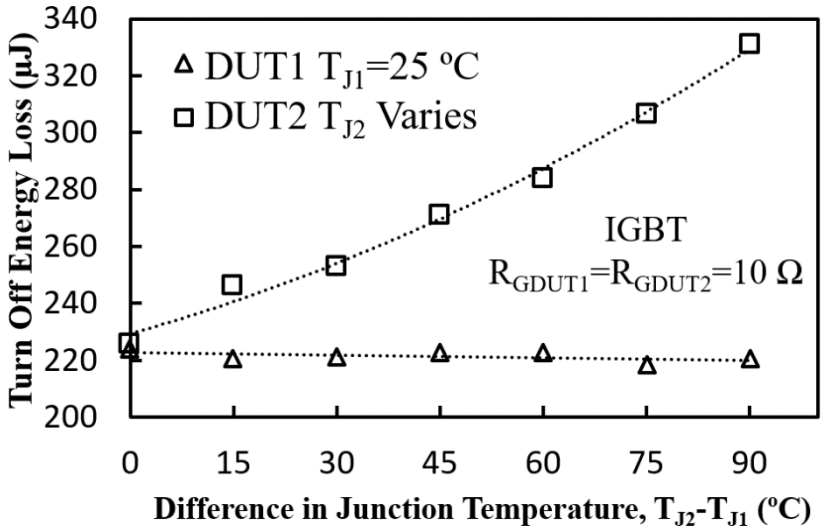


Figure 4.38: The measured turn-off switching energies of the parallel-connected IGBT devices with the DUTs set at different junction temperatures.

4.7 Impact of Switching Rate Variations on Parallel Connected NPT IGBTs

The parallel-connected IGBTs have also been switched with different switching rates at the same junction temperature. Figure 4.39 shows the turn-ON and turn-OFF current transient waveforms for the parallel connected IGBTs driven with different gate resistance (DUT1 is switched with R_G=10 Ω while DUT2 is switched with R_G=33 Ω). Similar to the parallel-connected CoolMOS and SiC MOSFETs, the device with the smaller gate resistance conducts more of the load current compared to the device with larger gate resistance. In the turn-ON characteristics shown in Figure 4.39(a), the faster switching device experiences a higher turn-On current overshoot. In the turn-OFF characteristics shown in Figure 4.39(b), the slower switching device experiences a significantly higher current overshoot. However, when in steady-state, both DUTs conduct the same load current unlike the case when driven with different initial junction temperatures.

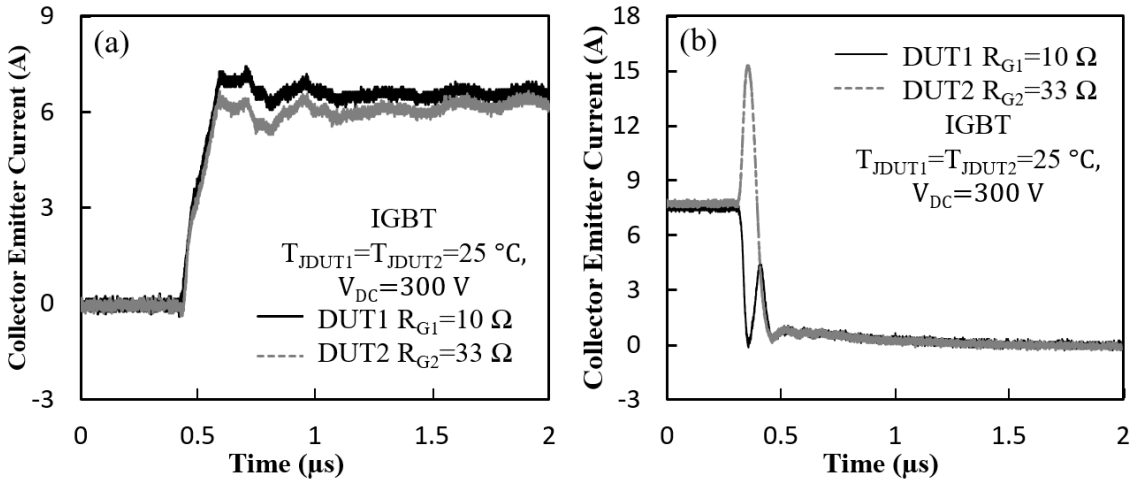


Figure 4.39: Measured (a) turn-on and (b) turn-off current waveform for parallel connected IGBTs with different switching rates.

Figure 4.40 shows the measured turn-ON switching energy for the parallel-connected IGBTs driven with different switching rates. The plot shows the measured turn-ON switching energy as a function of the difference in the gate resistances between the DUTs. DUT1 is driven with a fixed R_G=10 Ω while DUT2 is driven with higher gate resistances so as to ascertain the impact of the different switching rates on the switching energies. It can be seen that the difference in the turn-ON switching energy increases with the difference in the gate resistance with the faster switching device exhibiting a higher turn-ON energy.

Figure 4.41 shows the measured turn-OFF switching energies of the parallel connected IGBTs as a function of the difference in the gate resistances. It can be seen that the DUT driven at the lower rate exhibits a higher turn-OFF switching energy. However, the difference in the turn-OFF switching energy is much higher than the turn-ON switching energy (160 μJ vs 50 μJ), hence, the turn-OFF losses dominate. Figure 4.42 shows the case temperature after 500 seconds of repetitive switching of the parallel IGBTs with different rates. The slower switching IGBT exhibits a higher case temperature thereby indicating that the turn-OFF energy dominates.

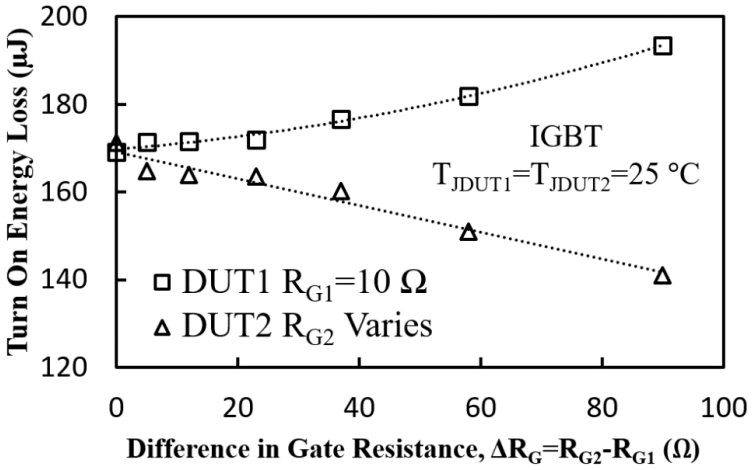


Figure 4.40: Measured turn-ON switching energy for the parallel connected IGBT devices with the DUTs driven at different switching rates.

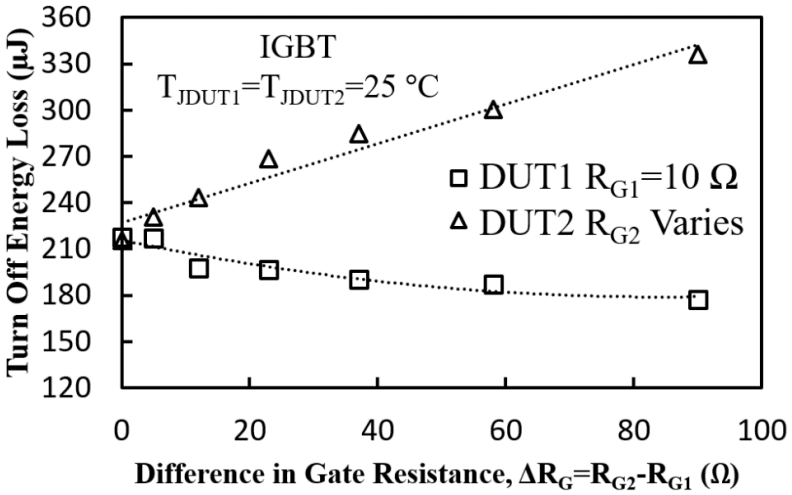


Figure 4.41: Measured turn-off switching energy for the parallel-connected IGBT devices with the DUTs driven at different switching rates.

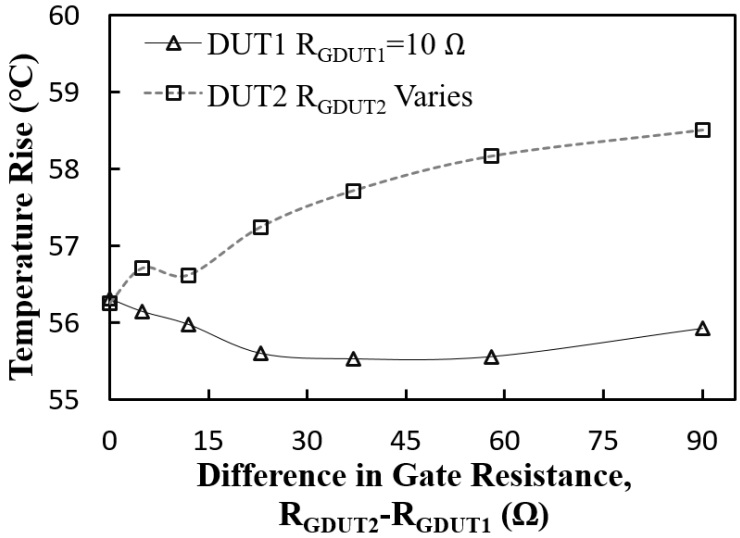


Figure 4.42: The measured case temperature rise for the parallel-connected IGBTs switched at different rates.

4.8 Impact of Variations in Case-to-Ambient Thermal Resistances and Capacitances (Different Heatsink Thermal Transients)

There are 2 thermal resistances critical to heat extraction in power devices. The first is the junction to case thermal resistance which is determined by the physical/material properties of the semiconductor chip. The second is the case to ambient thermal resistance,

which is determined by the thermal parameters of the heatsink including its physical geometry, density, fan speed and flow rate of the cooling liquid. Parallel-connected devices may operate with different case-to-ambient thermal resistances and capacitances as a result of variations in the cooling conditions. This is true for parallel-connected devices in the same module or parallel modules in the same system. This can result from thermal conduction material degradation or mechanical failure such as reduced flow rate of the cooling liquid or fan failure. In this case, the parallel devices will operate at different case/junction temperatures and will therefore exhibit switching energy mismatch as shown in section 4.2.

In this section, the parallel-connected DUTs are mounted on 2 separate natural convection heatsinks with thermal resistances of 6.4 °C/W and 7.6 °C/W respectively. A thin copper piece machined with a pin hole is mounted between the device and heat sink so as to enable the thermocouple to measure the case temperature. The electrical switching of the parallel DUTs in the clamped switching test rig is performed with 10 % duty ratio on the DUTs at 2 kHz switching frequency for 500 seconds, the supply voltage is 200 V. Figure 4.43 shows the measured temperature rise for the parallel-connected CoolMOS devices switched with different heatsinks emulating different case-to-ambient thermal resistances. The measurements were performed with the parallel DUTs switched with the same gate resistance ($R_{GDUT1} = R_{GDUT2}$) over a range of gate resistances. Hence, the initial switching losses, before the temperature rise of the heatsink, are the same. However, since the heat is extracted at different rates, as the devices reach steady-state electrothermal conditions, different case and average junction temperatures will emerge between the DUTs. The smaller heatsink has a quicker thermal response and therefore reaches a higher steady-state temperature than the larger heatsink. It can be seen from Figure 4.43, that the case temperatures of both DUTs increase with the gate resistances

which is expected since switching losses increase with the gate resistance. It can also be seen from Figure 4.43, that the smaller heatsink has a larger steady-state case temperature compared to the larger heatsink. This is also expected since the smaller heatsink has a smaller thermal mass and therefore requires a smaller amount of energy to achieve the same temperature rise as the larger heatsink.

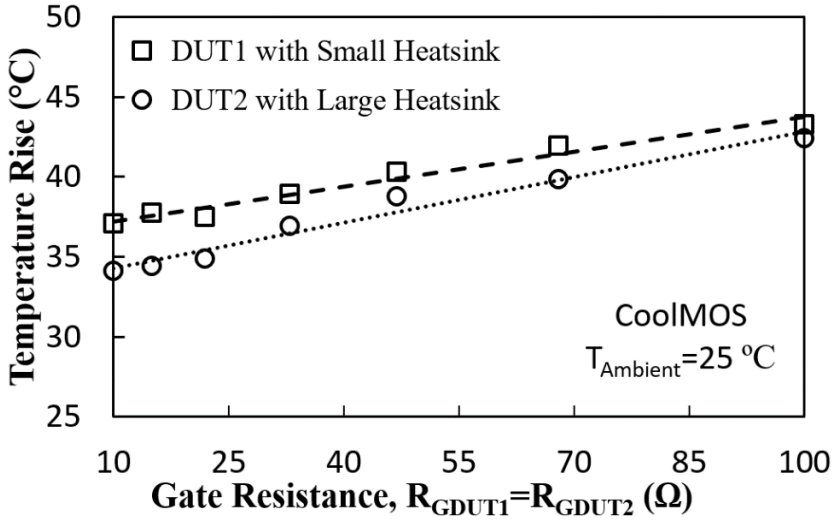


Figure 4.43: The measured case temperature rise for the parallel connected CoolMOS devices switched with different heatsinks.

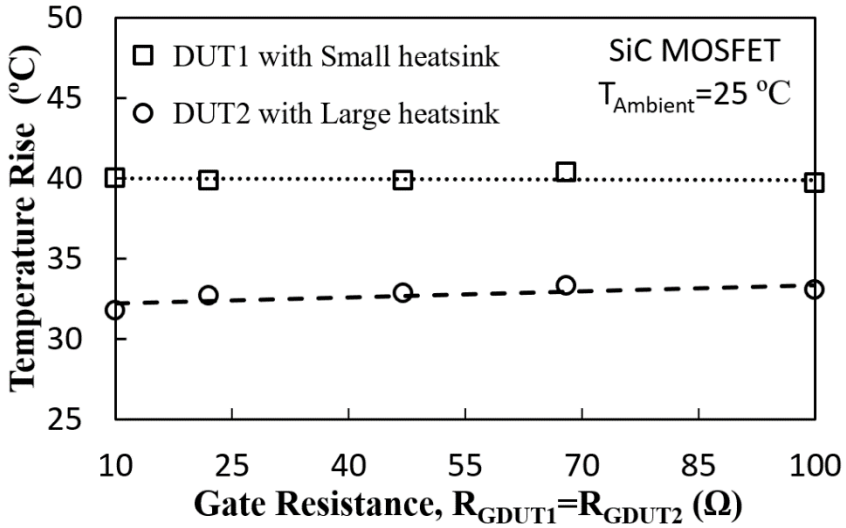


Figure 4.44: The measured case temperature rise for the parallel connected SiC MOSFETs switched with different heatsinks.

Figure 4.44 shows similar measurements for the parallel SiC MOSFETs switched with different case-to-ambient thermal resistances emulated by using different heatsinks. As, in Figure 4.43, the smaller heatsink reaches a higher steady-state case temperature and the case temperature increases with the gate resistance for both DUTs. However, the rate at which the steady state case temperature rises with respect to the switching losses (gate resistance) is slower for the SiC MOSFET. What is interesting to note in comparing the CoolMOS measurements (in Figure 4.43) with the SiC MOSFET measurements (in Figure 4.44) is that the temperature difference between the DUTs is higher for SiC compared with CoolMOS. This may initially seem to contradict earlier measurements in Figure 4.23 to 4.26 which show that parallel SiC MOSFETs with different initial junction temperatures have smaller variations in switching energy compared to parallel CoolMOS devices (with the same variations) due to less thermal sensitivity of the switching transients. However, it is due to the smaller thermal sensitivity of the losses in SiC that a larger variation in steady-state case temperature emerges from differences in case-to-ambient thermal resistance between parallel DUTs. As the case temperatures rise to different values during repetitive switching, the losses in the CoolMOS DUT with the higher case temperature increases significantly more than the CoolMOS DUT with the lower case temperature. As a result, the hotter CoolMOS DUT becomes more resistive and takes less current due to the positive temperature coefficient of the ON-state resistance in CoolMOS. Hence, the temperature between the 2 heatsinks narrow since more current flows through the CoolMOS DUT on the larger heatsink. Because, the temperature sensitivity of the conduction and switching losses is smaller in SiC MOSFETs, the temperature between the 2 heatsinks do not become smaller as is the case for CoolMOS.

Hence, although SiC MOSFETs introduce smaller temperature variations between parallel connected DUTs resulting from the fact that the losses in SiC are less temperature dependent, however, if the thermal variation is introduced by an external factor like the case-to-ambient thermal resistance, parallel SiC devices exhibit a larger temperature variation. Hence, for device-related variations like switching rates and initial junction temperatures, parallel SiC MOSFETs show better electrothermal stability however, for external variations like heatsinks, parallel SiC MOSFETs show less electrothermal stability.

Figure 4.45 shows the measured steady-state case temperature rise for parallel-connected IGBTs. The average temperatures are higher for the silicon IGBTs compared with the SiC MOSFETs and CoolMOS devices because of higher switching losses. It can be seen that the temperature of the IGBT pair is relatively constant as the gate resistance of the IGBT pair is increased from 10 Ω to 100 Ω. This is due to the fact that the IGBT switching transients depend as much on the forward recovery and long current tail transients as they do on the switching rate of the current through the MOS channel of the IGBT. As IGBT's turn-OFF, the long tail currents resulting from minority carrier recombination in the drift region have a significant impact on the switching losses. Since the tail currents depend on the minority carrier lifetime much more that the current commutation rate set by the gate resistance, there is less dependence of the steady state case temperature on the gate resistance for both heatsinks.

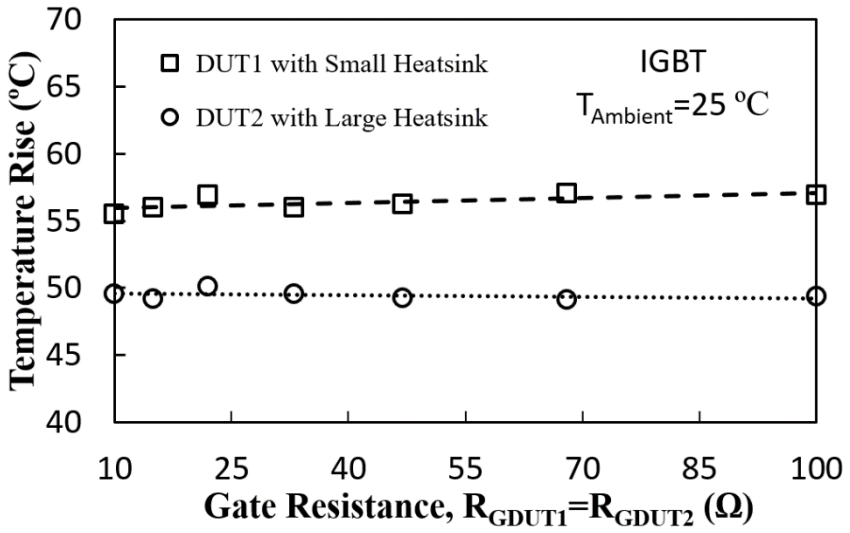


Figure 4.45: The measured case temperature rise for the parallel connected SiC MOSFETs switched with different heatsink.

4.9 Conclusions

Electrothermal balancing of parallel connected SiC MOSFETs, CoolMOS and silicon IGBTs have been studied in this chapter. Variations have been introduced between the parallel-connected DUTs through varying (i) the switching rate (ii) the initial junction temperature and (iii) The case-to-ambient thermal resistance. This has been done for single switching measurements so as to evaluate the impact of variations in the initial junction temperature and switching rates on the switching energy of the parallel DUTs and also, repetitive switching measurements to evaluate the impact of the variations on steady state temperature differences between the parallel DUTs.

Figure 4.46 shows the percentage change in the turn-ON switching energy as a function of the variation in the switching rate (ΔR_G) while Figure 4.47 shows a similar plot for the turn-OFF switching energy. The SiC MOSFETs perform better than the CoolMOS since the variation in the switching energy is less for a given magnitude of ΔR_G between the parallel-connected DUTs. However, the IGBTs show the most insensitivity

to differences in R_G. This is due to the fact that the current commutation rate (dI/dt) of the IGBT is smaller than the MOSFETs (SiC and CoolMOS) because of conductivity modulation. As the IGBT is switched ON and OFF, the forward recovery and recombination of the minority carriers in the drift region determines the current commutation rate more than the gate resistance. The gate resistance determines the rate at which the MOS channel in the IGBT is switched, however, the minority carrier lifetime is the most dominant factor. Similar characteristic plots are shown in Figure 4.48 and Figure 4.49 for parallel-connected devices set at different junction temperatures. It can be seen that the percentage change in the switching energy for a given ΔT_J is smaller for the SiC MOSFETs than for the CoolMOS devices or IGBTs. For silicon IGBTs, the minority carrier lifetime is temperature dependent, hence, changes in the temperature between the parallel DUTs will impact energy and temperature balancing.

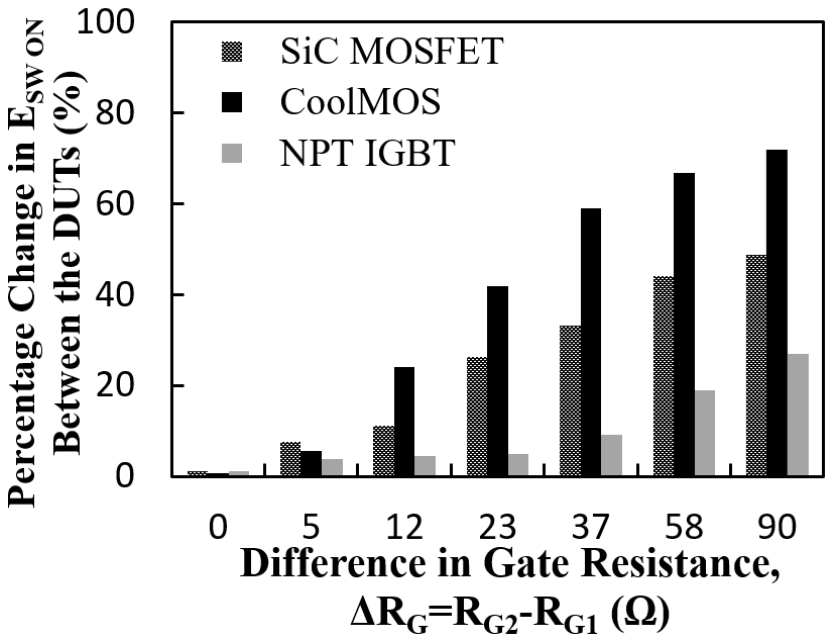


Figure 4.46: Percentage change in the turn-ON switching energy ($E_{SW\,ON}$) as a function of the switching rate difference (ΔR_G) between the parallel DUTs.

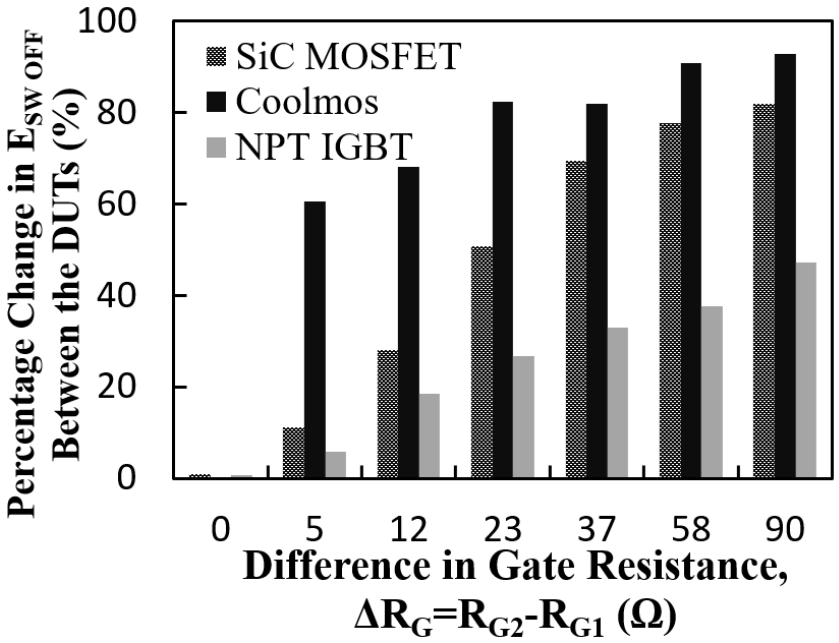


Figure 4.47: Percentage change in the turn-OFF switching energy ($E_{SW\ OFF}$) as a function of the switching rate difference (ΔR_G) between the parallel DUTs.

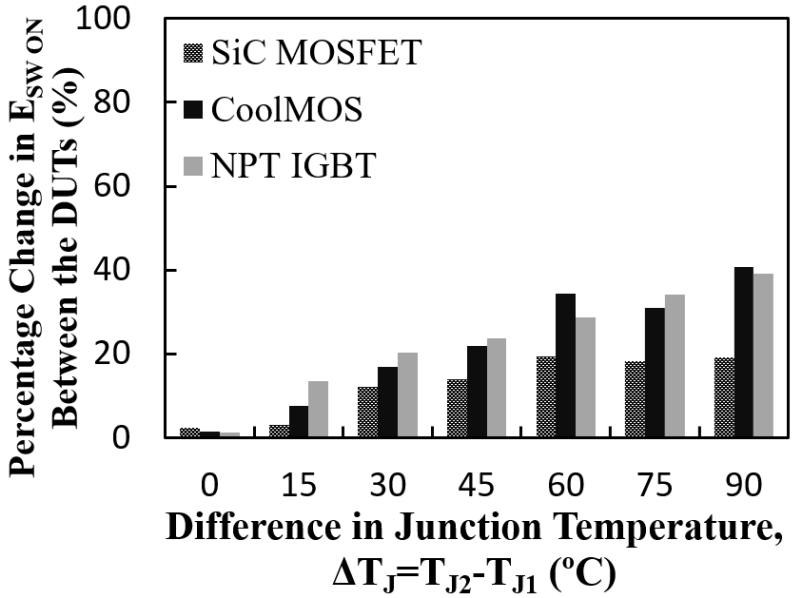


Figure 4.48: Percentage change in the turn-ON switching energy ($E_{SW\ ON}$) as a function of the junction temperature difference (ΔT_J) between the parallel DUTs.

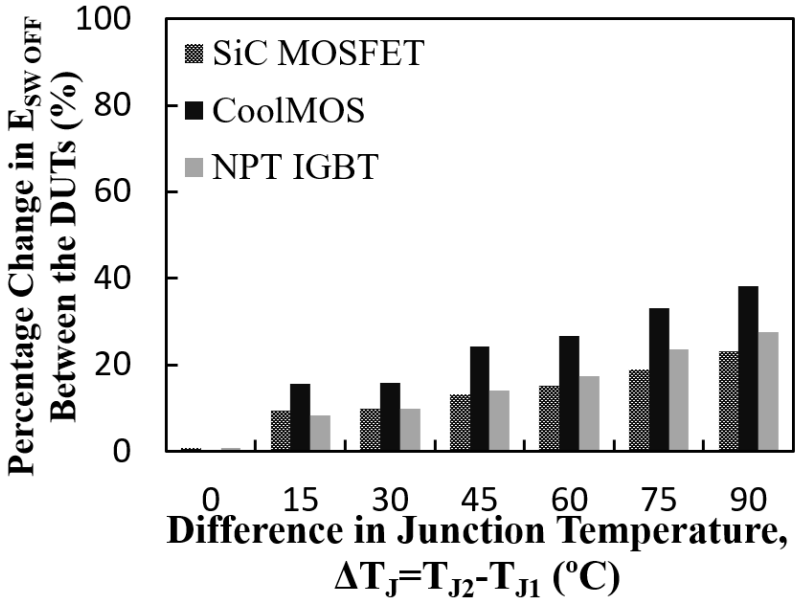


Figure 4.49: Percentage change in the turn-OFF switching energy ($E_{SW\ OFF}$) as a function of the junction temperature difference (ΔT_J) between the parallel DUTs.

4.10 Implications for Power Electronic Applications

Power electronic modules are typically comprised of power semiconductor devices paralleled together for delivering high current capability. These power devices should ideally be electrothermally identical thereby minimising power and temperature variation across the module. However, variations in switching rate and parasitic components can introduce electrothermal variation between the parallel devices. The results in this chapter show that SiC power modules are more capable of maintaining electrothermal stability given with variations between the different devices. These results are important especially given that SiC power modules will typically comprise of more parallel power devices than IGBT modules since the current ratings of SiC power devices are lower than that of silicon IGBTs. These results are useful for power electronic engineers designing converter modules and for reliability engineers seeking to implement SiC power devices in the next generation of high power density converters.

Chapter 5.

ELECTROTHERMAL RUGGEDNESS OF PARALLEL CONNECTED SIC MOSFET AND COOLMOS

5.1 Introduction

Power modules are usually comprised of a number of dies connected in parallel for the purpose of delivering higher current ratings. Likewise, power devices are comprised of several cells internally connected in parallel thereby sharing common terminals and delivering the rated current of the device. Process variations mean that the electrical and thermal parameters of the switching device may not always be exactly uniform. This can be true of separate discrete power devices as well as the internal FET cells of a single power device. Since commercial semiconductor fabrication processes are often designed to tightly limit the variation in the electrical parameters across the wafer from which the devices are derived, there are limits to the variation of these electrical parameters e.g. breakdown voltage, on-state resistance, threshold voltage etc. However, operational degradation of the devices does not usually occur at the same rate. Devices connected in

parallel may begin the operational mission profile with almost identical thermal and electrical parameters, however, over time, may develop variations resulting from non-uniform rates of degradation. For instance, the thermal resistances of the power devices typically increase as a result of solder joint degradation due to thermo-mechanical stresses arising from coefficient of thermal expansion (CTE) mismatch between the die and the substrate [106, 127, 146, 147]. Depending on the position of the device on the heat-sink, this effect of mechanical degradation may not occur at the same rate. Parallel-connected devices with different degrees of solder joint delamination will have different thermal resistances and therefore different electro-thermal properties arising from different junction temperatures. Another source of possible variation is the electrical switching time constant, which is determined by the gate resistance and internal capacitances. Over the operating life of the power device, thermo-mechanical stresses from temperature and power cycles mean that the gate resistance is likely to increase as a result of wire-bond mechanical degradation [86, 127]. If this degradation occurs at a non-uniform rate between parallel-connected devices, then a situation can arise whereby parallel connected devices have significantly different gate resistances and therefore switch at different rates. Although less likely, the gate capacitance can increase as a result if higher interface and fixed oxide charges from the adjacent channel. This can cause variation in the electrical switching time constant between the parallel-connected devices. This problem is all the more pertinent to high current applications where small die areas mean several devices are often required to meet defined current ratings. Furthermore, during operation at higher switching frequencies, which is seen to be the unique advantage of unipolar power devices like CoolMOS and SiC power devices, variations in electrothermal switching characteristics constitute more of a reliability concern.

Power device failure from electrothermal runaway can result from (i) Package-related failure, (ii) Safe operating area (SOA) failure and (iii) Avalanche breakdown. The package-related failure mechanism is typically degradation occurring in the soldering layer and/or wire bond from thermo-mechanical stresses resulting from CTE mismatch between the different materials. SOA failure typical results from the rate of heat generation in the device exceeding the rate of heat extraction/dissipation thereby leading to a temperature surge at the junction. This can result from the device operating in the liner mode where there is high instantaneous power resulting from simultaneously high current and voltage. Some applications require device operation in the linear mode while switch mode devices can drift into linear mode operation as a result of de-saturation. Avalanche breakdown of power devices can occur under a number of conditions namely

(i). Unclamped inductive switching where the device interrupt current through an inductive load and the load de-magnetises itself by dissipating current through the device in its OFF-state.

(ii). Hard commutation of the body diode. If the device's internal body diode is commutated with a high enough *dV/dt*, the discharge current of the internal depletion capacitance can latch the internal BJT of the device resulting in simultaneously high current through the device and voltage across the device. This becomes destructive if the heat generated from the latching of the internal BJT surpasses the heat dissipated in sufficient time for the BJT collector current to become positively correlated with temperature.

(iii). Hard turn-OFF with high *dI/dt*. If a device is turned-OFF while high *dI/dt* in the presence of parasitic collector/drain inductance, the voltage overshoot resulting from the $L \cdot dI/dt$ can exceed the breakdown voltage of the device and cause avalanche mode conduction.

It is well understood that the failure mode of power devices under unclamped inductive switching (UIS) are of 2 categories which are (i) parasitic bipolar latch-up for UIS pulses with high currents and low durations [104, 148, 149] and (ii) intrinsic temperature limitations for lower current pulses over a long avalanche duration [26, 104, 107]. The wider bandgap, higher critical electric field and higher thermal conductivity of SiC means that the devices are more robust under UIS compared to similarly rated technologies as has already been demonstrated in [102, 105, 107, 109, 150-152]. However, the impact of electro-thermal variations in parallel-connected devices under UIS has yet to be investigated for the different technologies. Furthermore, how these electro-thermal variations impact the overall reliability of parallel connected devices for high power avalanche pulses with short durations compared to smaller power avalanche pulses over longer avalanche durations is interesting to consider.

Non-uniformities in the electrothermal characteristics of parallel-connected devices reduce the overall reliability since power is not equally dissipated between the devices. Furthermore, a non-uniform rate of operational degradation induces electrothermal variations thereby accelerating the development of failure. This chapter uses simulations and experiments to quantitatively and qualitatively investigate the impact of electrothermal variations on the reliability of parallel-connected power devices under unclamped inductive switching (UIS) conditions. This is especially pertinent to SiC where small die areas mean devices are often connected in parallel for higher current capability and high thermal resistances mean high junction temperatures. Like the previous chapter, the performance of CoolMOS devices is considered alongside the SiC devices and finite element simulations have been used to investigate the electrothermal dynamics of parallel-connected devices. Because avalanche mode conduction occurs through the body diode and IGBTs do not have a body diode, IGBTs have not been

considered in this chapter since they usually do not have avalanche ratings. Measurements and simulations show that, for both the SiC MOSFETs and the CoolMOS devices, increasing the variation in the initial junction temperatures and switching rates between parallel-connected devices under UIS reduces the total sustainable avalanche current. It is seen that the device with the lower junction temperature and lower switching rate fails. This observation occurs both for the parallel-connected CoolMOS and parallel connected SiC devices. The measurements also show that the maximum sustainable avalanche energy for a given variation in junction temperature and switching rate increases with the avalanche duration, meaning that the effect of electro-thermal variation is more critical with high power (high current & low inductor) UIS pulses compared with high energy (low current & high inductance) pulses. These results are important for condition monitoring and reliability analysis.

This chapter uses experimental measurements and simulations of parallel connected SiC power devices to understand the impact of electro-thermal variation on module reliability. The impact of variations in the junction temperature and gate resistance between parallel-connected SiC MOSFETs and CoolMOS devices on overall avalanche ruggedness is analysed using a dedicated test rig and a finite element solver.

5.2 Electrothermal Ruggedness of Power MOSFETs under Unclamped Inductive Switching

Power semiconductor devices have steadily improved in energy efficiency over the decades. By optimizing device design and processing, lower conduction and switching losses have been achieved. This has usually been at the cost of increased thermal resistance and higher power densities thus translating to higher average junction

temperatures. Shrinking die sizes as a result of improved specific ON resistance, results in lower parasitic capacitances and lower switching losses, however, with higher current and voltage commutation rates. The higher current commutation rate (*dI/dt*) in the presence of parasitic inductances will cause electromagnetic instability via oscillations and ringing. Severe over-voltages resulting from fast turn-OFF can cause drain voltages far exceeding the breakdown voltage. This is more so the case in automotive applications where inductive loads like motors are driven and controlled by power devices. These voltage overshoots force the device to operate under avalanche mode conduction where very high instantaneous power can easily force the device beyond its rated junction temperature.

The ability of a power MOSFET to dissipate this avalanche energy without electrothermal destruction is usually referred to as electrothermal ruggedness and depends on whether the internal parasitic BJT is properly controlled. Inherent in every MOSFET is a parasitic npn BJT with the BJT collector corresponding to the MOSFET drain, the BJT emitter corresponding to the MOSFET source and the BJT base corresponding to the MOSFET p-body. Figure 5.1 shows the single cell of a power MOSFET with the corresponding npn BJT.

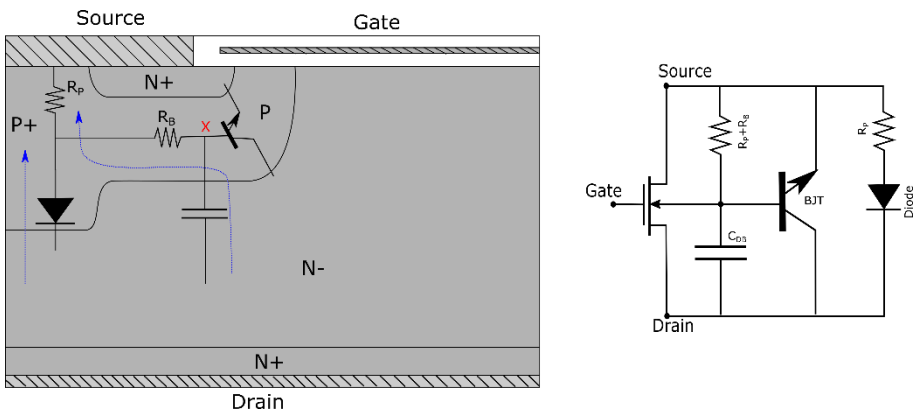


Figure 5.1: MOSFET structure with parasitic components and equivalent circuit.

For the parasitic BJT to turn-ON, the emitter base voltage must exceed the inbuilt junction voltage of the PN diode while the base-collector junction is reverse biased. The equation for the in-built voltage of the emitter (source) to base (p-body) junction voltage is given by:

$$\Phi_{bi} = \frac{K_B T_{(t)}}{q} \ln\left(\frac{N_E N_B}{n_i^2}\right) \tag{5.1}$$

where K_B is the Boltzmann constant, n_i is the intrinsic carrier concentration of the semiconductor, N_E is the emitter (source) doping and N_B is the base (p-body) doping.

For this to happen, there must be a base current flowing across the p-body of the MOSFET with a sufficient magnitude to cause a voltage drop along the parasitic base resistance. If this voltage drop exceeds the in-built junction voltage of the source-to-body PN junction, then the parasitic BJT may be activated. This voltage drop may be expressed as

$$V_A = R_B I_B \tag{5.2}$$

where R_B is the lateral resistance of the P-body as shown in Figure 5.1, the parasitic BJT base current (I_B) which is generated by impact ionisation from the avalanche current is given by

$$I_B = I_C - I_E \tag{5.3}$$

where I_E is the emitter current of the BJT and the parasitic BJT collector current I_C is given by

$$I_C = \alpha I_E = \gamma_E \alpha_T M I_E \tag{5.4}$$

In the equation above, α is the parasitic BJT gain factor, γ_E is the emitter injection efficiency, α_T is the base transport factor and M is the multiplication coefficient. The emitter injection efficiency is measure of the electron current through the parasitic NPN BJT that is due to the electrons injected from the emitter (source) into the base (body) while the base transport factor is a measure of what fraction of the minority carriers (in the case electrons in the p-base) reaches the collector-to-base junction. The parasitic BJT emitter current increases as the base current increases and the junction voltage between the MOSFET source and body increases. This emitter current I_E is given by

$$I_E = I_0 \exp\left[\frac{qI_B R_{PB}}{K_B T}\right] = I_0 \exp\left[\frac{qR_{PB}}{K_B T}(M-1)I_E\right] \tag{5.5}$$

During UIS, the increasing voltage across the DUT increases the current gain (multiplication coefficient) of the BJT. In addition, the increased junction temperature causes higher carrier injection from the emitter, which leads to less resistivity of the BJT.

$$M = \frac{1}{1-\left(\frac{V_D}{BV}\right)^6} \tag{5.6}$$

$$V_{D,SB} = \frac{BV}{\left[\frac{qR_{PB}I_0}{kT}\right]^{\frac{1}{6}}} \tag{5.7}$$

where V_D is the applied drain voltage, BV is the breakdown voltage and I_0 is the base current of the parasitic BJT at point A. The impact ionisation coefficient of a semiconductor is critical in determining the avalanche ruggedness of the power device. It is defined as the number of electron-hole pairs generated by a carrier (electron or hole) traversing through a fixed distance (defined as 1 cm) within the depletion layer along the direction of the electric field. Hence, the lower the impact ionisation coefficient, the less likely avalanche breakdown will occur. The impact ionisation coefficients are determined

empirically by measurements and have been reported for silicon and SiC to be given by [26] as:

$$\alpha_n(Si) = 7.03 \times 10^5 \cdot \{1 + 0.588[\left(\frac{T}{300}\right)^{0.85} - 1] \cdot e^{-1.23 \times \frac{10^6}{E}}$$
$$\alpha_p(Si) = 1.58 \times 10^6 \cdot \{1 + 0.588[\left(\frac{T}{300}\right)^{0.85} - 1] \cdot e^{-2.0 \times \frac{10^6}{E}} \quad (5.8)$$

$$\alpha(4H - SiC) = (6.46 \times 10^6 - 1.07 \times 10^4 \cdot T) e^{-1.75 \times \frac{10^7}{E}} \quad (5.9)$$

It can be seen from the equations above that SiC as a material has a lower impact ionisation coefficient. This is due to the wide bandgap which requires significantly higher energy to generate electron-hole pairs, since the minimum collision energy needed to generate an electron-hole pair is the bandgap.

Power MOSFET designers are well aware of parasitic BJT latch-up and have therefore designed a new generation of avalanche rugged power MOSFETs with improved safety features. This includes deep p-body implants with very low resistivity and with the source metal shorting n+ source and the p+ body. This deep p-body implant zone is spatially separated from the nominal p-body implant that is used to set the threshold voltage of the device and is normally done after the nominal p-body implant. This is referred to as the deep p-body implant and has two purposes. Firstly, to ensure that the avalanche breakdown occurs at that junction since the high dose p-body implant ensures that the highest electric field occurs away from the channel region and secondly, to minimize the parasitic p-body resistance thereby supressing the possibility of triggering the parasitic BJT. The deep p-body implant causes the body diode of the power MOSFET to have a low breakdown voltage, hence, the objective is to ensure that the body-diode conducts the avalanche current, since this diverts current away from the parasitic BJT.

Figure 5.2 shows the single cell schematic of a power MOSFET with the deep p-body implant.

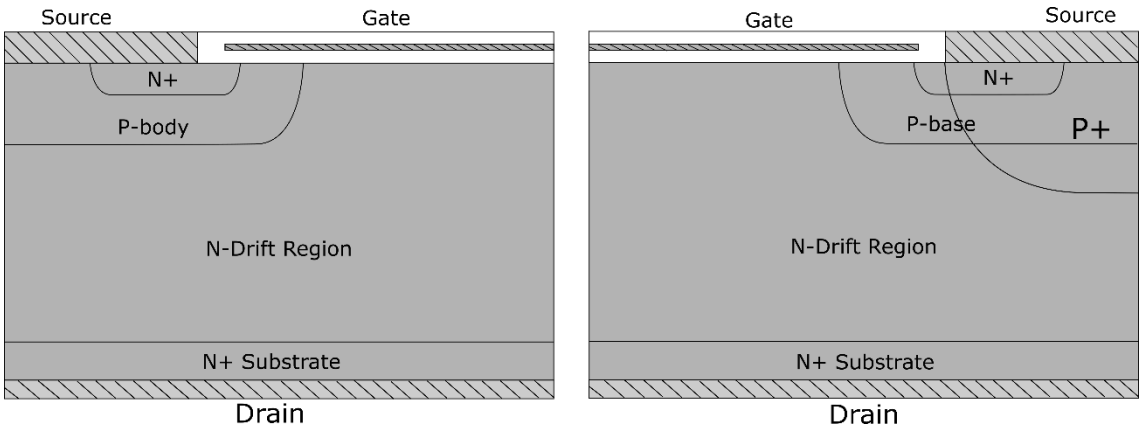


Figure 5.2: Power MOSFET cell (a) without and (b) with deep-body implant.

There is still a finite probability of BJT latch-up even with the deep p implant. The power MOSFET goes into avalanche when it conducts current in the OFF state i.e. no channel between the source and drain. If the avalanche current is high enough, there will be two factors contributing towards BJT latch-up. The first is increased p-body resistance from higher junction temperatures and the second is a MOSFET body current generated from impact ionisation. This MOSFET body current, if large enough, becomes the base current of the parasitic BJT. The increased p-body resistance comes from increased phonon scattering impeding the flow of carriers. It should be noted that failure in the power MOSFET is usually localised to a single cell within the device. A power MOSFET is comprised of numerous cells depending on the cell pitch and the size of the power MOSFET. Hence, if the parasitic BJT is latched in a single cell, current crowding will occur and if the BJT current is positively correlated with temperature, then thermal runaway and device destruction happens.

Power MOSFET failure under UIS depends on how the avalanche energy is dissipated through the device. The failure mechanism is parasitic BJT latch-up if the avalanche energy comes in the form of high power density over a short avalanche duration. Under avalanche pulses with high power density, the inductor (avalanche duration) is small and the peak avalanche current is large. Due to the fast nature of the electrical transient, only a small section of the device attains a high junction temperature thereby resulting in hot spots or current filaments. The parasitic BJT in a single cell is triggered and when latched, the positive temperature coefficient of the avalanche current leads to thermal runaway i.e. a single hot-spot destroys the device.

The other failure mechanism occurs when the avalanche energy comes in the form of low power density over a long avalanche duration [106, 148, 153-156]. This failure mechanism is associated with long avalanche duration and low peak avalanche current pulses, occurs when the electrical power transient is long enough to allow the global temperature of the device is rise to its temperature limit. When the device junction temperature reaches the point at which the thermally generated carrier concentration becomes comparable to the background doping, the semiconductor becomes more like a metal and loses the capability to turn-OFF. The thermally generated carrier concentration for the silicon and SiC can be calculated as [26]:

$$n_i(Si) = 3.87 \times 10^{16} T^{\frac{3}{2}} e^{-\frac{7.02\times10^3}{T}} \tag{5.10}$$

$$n_i(SiC) = 1.70 \times 10^{16} T^{\frac{3}{2}} e^{-\frac{2.08\times10^4}{T}} \tag{5.11}$$

where the T is temperature in Kelvin. For a CoolMOS device rated at 900V, the doping concentration for the drift region is approximately 1×10^{15} cm^{-3} while for the 4H-SiC MOSFET rated at 1.2 kV, the background doping is approximately 1×10^{16} cm^{-3}. The table

below shows that at any given temperature, due to the wide bandgap of SiC, the thermally generated carrier concentration for the SiC MOSFET is always significantly lower than that of a silicon device. This makes SiC inherently rugged under avalanche conditions.

Temperature (ºC)	Intrinsic Carrier Concentration of Silicon (cm^{-3})	Intrinsic Carrier Concentration of 4H-SiC (cm^{-3})
300	2.5367×10^{15}	4.006×10^{4}
600	3.2134×10^{17}	1.9702×10^{10}
1000	7.0798×10^{18}	6.1887×10^{13}

Table 5-1: The intrinsic carrier concentration as a function of temperature for silicon and SiC.

5.3 Experimental Test-Rig

Figure 5.3(a) shows the circuit schematic of the experimental set-up used for the investigations. This test set-up is similar to the test rig shown in chapter 4, except for the removed free-wheeling diode. Since the diode is not there to allow the de-magnetisation of the inductor by free-wheeling the current, the inductor is de-magnetised by forcing the low side DUT into avalanche. The parallel-connected devices are thus subjected to unclamped inductive switching with an avalanche power that depends on the peak avalanche current and the avalanche duration. Again, the gate drive has been pre-synchronized before starting the test. The devices under investigation are 1.2kV/10A CREE SiC MOSFETs with datasheet reference C2M0280120D and 900V/15A Infineon CoolMOS^{TM} devices with datasheet reference IPW90R340C3. Although these two devices have differences in blocking voltage and current rating, they have similar power rating. The avalanche current is determined by the duration of the gate pulse which charges the inductor. The turn-ON and turn-OFF gate voltages were set as 18 V and 0 V respectively. The voltage of DC power supply is constantly 50V. The negative

temperature coefficient of the threshold voltage means that the V_{TH} reduces as the temperature increases. However, for the temperature range that will be examined in this chapter (between 25 and 110 °C), the threshold voltage reduction is not sufficient to affect avalanche current sharing between the parallel connected DUTs since the avalanche duration will be much longer than the turn-OFF time. According to the temperature dependency of the threshold voltage presented on the datasheet of the device, the maximum difference in threshold voltage between the parallel-connected devices will be limited to 0.5 V corresponding to a temperature difference of 85°C between the DUTs. Figure 5.3(c) shows typical avalanche characteristics for a 1.2 kV SiC MOSFET under UIS. In Figure 5.3(c), the current ramp up phase can be seen while the gate voltage is high. It can also be seen that the drain-source voltage rises abruptly to the breakdown voltage as the gate voltage is turned-OFF and the device conducts in avalanche.

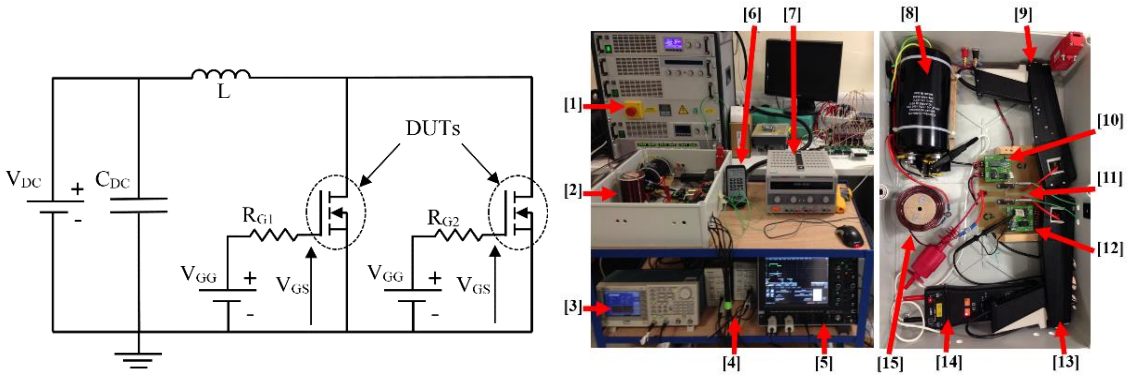


Figure 5.3: (a) The circuit schematic for the experimental set-up. (b) Photograph of the test Rig.

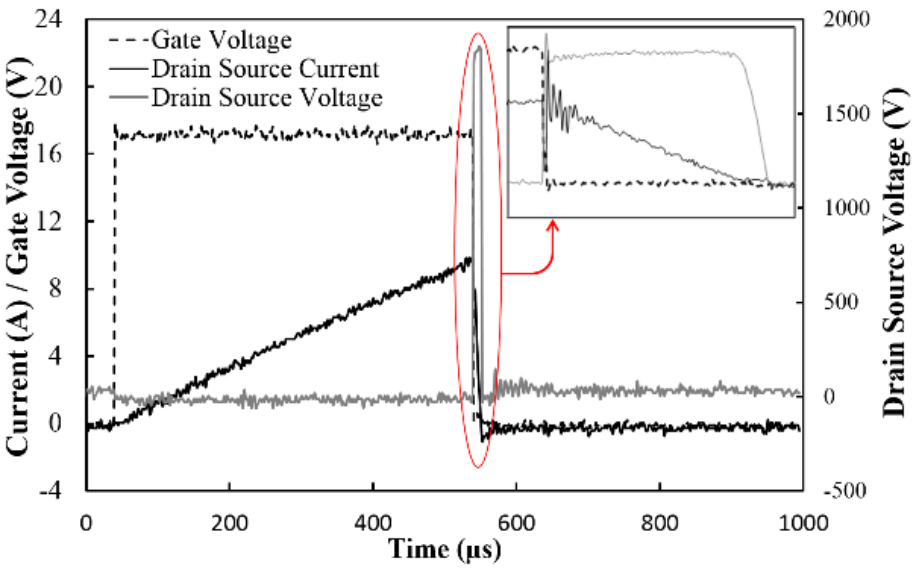


Figure 5.3: (c) Typical avalanche characteristics showing the gate voltage, drain voltage and drain-source current during the charging and avalanche conduction phases.

Figure 5.4(a) shows how the maximum avalanche current sustainable by the DUT before failure under UIS is determined by progressively increasing the peak avalanche current through the duration of the charging gate pulse. Figure 5.4(b) shows the peak avalanche current characteristics of the SiC MOSFET that has failed under UIS for 2 different avalanche durations. It can be seen that the peak avalanche current sustainable by the device decreases with increasing avalanche duration i.e. when a larger inductor is used, a smaller peak current is needed to destroy the device. Figure 5.5 shows pictures of de-capsulated 1.2kV/24A and 1.2kV/10A SiC power MOSFETs that have failed under UIS with the burn marks due to thermal runaway showing. The de-capsulation was done destructively using mechanical force while ensuring that the process did not alter the die surface. The burn marks occur just underneath the source wire-bonds where high current densities are likely to occur due to the proximity of the source wires. Figure 5.6 shows the measured maximum sustainable energy successfully dissipated by the DUT prior to failure under UIS for different avalanche durations and temperatures. It can be seen that

the device can dissipate higher avalanche energies if it comes in the form of lower peak avalanche currents over longer durations [152, 157].

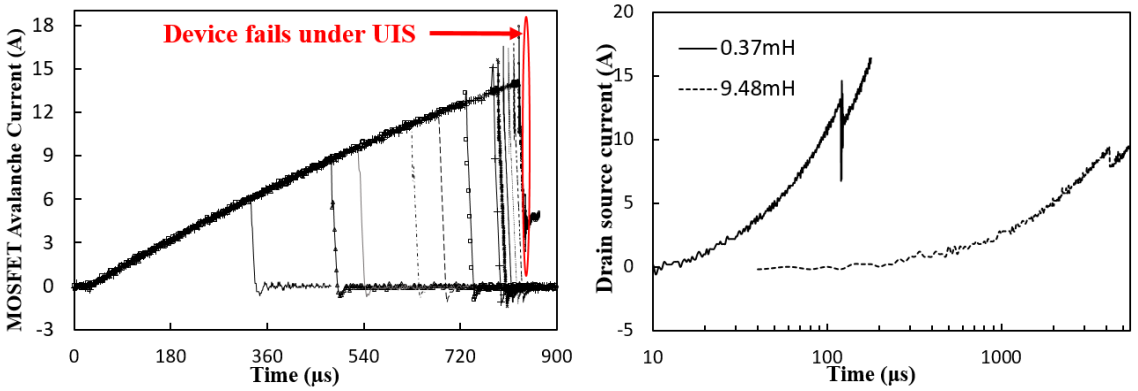


Figure 5.4: (a) UIS measurements of a 1.2kV/10A SiC MOSFET drain-source currents during the inductor charging and avalanche phases with different gate pulse durations. (b) The peak avalanche current characteristics of a SiC MOSFET for 2 different inductor sizes.

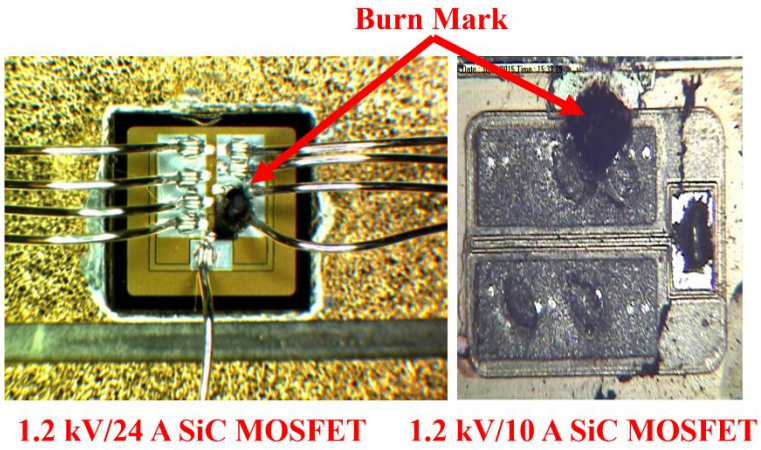


Figure 5.5: Picture of the de-capsulated SiC MOSFETs showing burn mark resulting from failure under UIS.

It can also be observed from Figure 5.6 that increasing the ambient temperature of the UIS experiment decreases the overall sustainable energy as expected. In the next phase of the experiments, the impact of electro-thermal variations in parallel-connected devices on the maximum sustainable avalanche energies sustainable without failure will be investigated. Specifically, the impact of different initial junction temperatures (which

result from different thermal resistances) and the impact of different switching rates set by different gate resistances will be investigated.

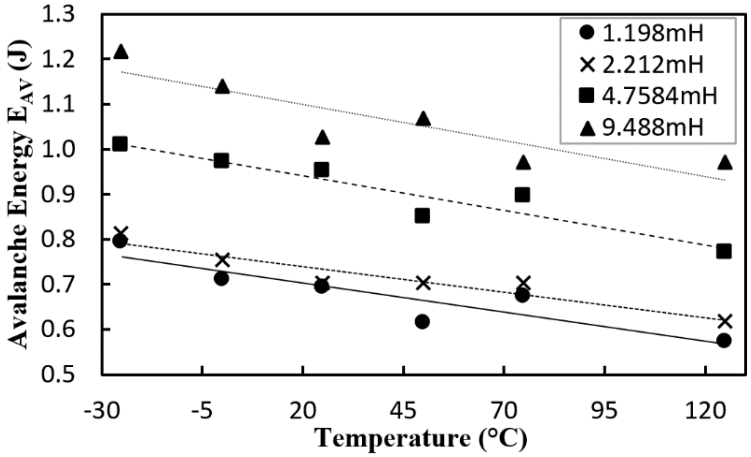


Figure 5.6: The measured maximum sustainable avalanche energy before failure under UIS for different inductors as a function of temperatures. The device tested was a 1.2kV/24A SiC power MOSFET.

5.4 Compact Model Estimation for Junction Temperature of Power MOSFETs under UIS

Using compact models and parameters derived from device datasheets, it is possible to estimate the device junction temperature as a result of avalanche mode conduction in unclamped inductive switching. This method of estimating the junction temperature is computationally inexpensive, however, is not as accurate as using finite element methods as will be shown in the next section of this chapter. The junction temperature is estimated using the transient thermal impedance characteristics, which are usually provided by the device manufacturers. The junction to case transient thermal impedance coupled with the avalanche power is sufficient in estimating the junction temperature. Due to the fact that the avalanche power is dissipated in the power device in approximately tens of microseconds, the entirety of the temperature rise occurs within the junction-to-case

thermal resistance. This is due to the fact that the electrical time constant is significantly shorter than the thermal time constant, hence, the avalanche pulse is over before there is time for the heat to diffuse into the case-to-ambient thermal impedance.

This method, since it is based on lumped thermal resistances and capacitances, assumes that the heat is uniformly dissipated within the power device, hence, cannot account for hot-spots within the device. It cannot also predict and explain how mismatched parallel devices will fail under UIS and what impact the mismatch will have. The peak junction temperature of device under UIS can be calculated since the temperature rise is a function of the transient impedance (Z_{TH}) and power dissipation (P_{AV}) according to [26]:

$$\Delta T = Z_{TH} \times P_{AV} \tag{5.12}$$

Hence the junction temperature can be calculated as

$$T_J = T_{Initial} + \Delta T \tag{5.13}$$

The conducting current during avalanche is calculated as

$$I_{AV}(t) = I_{AV}(peak) - \frac{V_{AV} \cdot (t - t_0)}{L} \tag{5.14}$$

where $I_{AV}(peak)$ is the peak avalanche current before turn-OFF; t_0 is the start time of the avalanche pulse and L is the inductance. Since the drain-source voltage during avalanche is invariant as was observed experimentally, it can be assumed to be constant through out the UIS pulse. Hence the average power dissipated as a function of time during the avalanche can be calculated as

$$P_{AV}(t) = \frac{\int_{t_0}^{t} V_{AV} \cdot I_{AV}(t)dt}{t - t_0} \cong \frac{(I_{AV}(t) + I_{AV}(peak)) \cdot V_{AV}}{2} \tag{5.15}$$

Figure 5.7(a) shows the transient junction-to-case thermal impedance as a function of power pulse width for the 1200V SiC MOSFET used in the experiments. The thermal impedance of the power devices consists of two components namely the intrinsic thermal capacitance and the thermal resistance. In the self-heating process, the intrinsic thermal capacitance is charged initially, after which the heat is conducted to the case through the thermal resistance. Hence, for long pulse durations, the thermal impedance is the same for pulses with different duty ratios. Figure 5.7(b) shows the calculated transient junction temperature during the avalanche pulse for avalanche durations corresponding to the 1 mH and 3 mH inductors. The avalanche current conducted is the maximum current successfully dissipated by the device before electrothermal failure for both inductors. The calculated junction temperature is higher in the case of the 3 mH avalanche measurement since the avalanche duration is longer. The 1 mH inductor causes a shorter thermal transient compared to the 3 mH inductor.

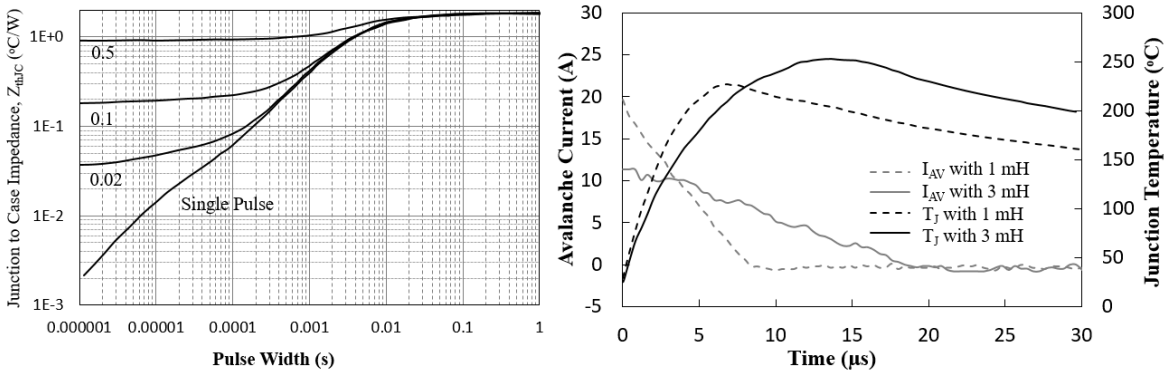


Figure 5.7: (a) The transient thermal impedance of 1200V SiC MOSFET as a function of power pulse width; (b) The power dissipated and calculated junction temperature as a function of time during the avalanche test.

5.5 Finite Element Simulation of UIS in Parallel Connected DUTs

The circuit shown in Figure 5.3(a) has been simulated in ATLAS from SILVACO using the mixed mode circuit application to solve the switching transients with the finite element model. Finite element simulations have been performed on SiC power MOSFETs and CoolMOS device under avalanche mode conduction so as to gain a deeper insight into the physics of device failure with 2 parallel devices. The model included lattice-heating and temperature dependent impact ionization together with the continuity/Poisson equations for carrier transport. The drift layer doping and thickness was optimized to achieve the desired breakdown voltage in SiC. To correctly model the on-state current, Shockley-Read-Hall (SRH) recombination was used together with concentration dependent mobility for the electrons in the MOSFET channel. For the SiC MOSFETs, a p-body doping of 1.0×10^{18} cm^{-3} was used in combination with a 1.0×10^{19} cm^{-3} $p+$ doping for the body diode shorting the source to the body. The source and drain regions were degenerately doped with n+ and an oxide thickness of 50 nm was used for the gate dielectric. The thickness and doping of the voltage blocking drift layer in the device was set to achieve a breakdown voltage of 1.5 kV. A drain current density of 60 A/cm^2 was achieved in the simulation based on the simulated active area of 3.5 mm^2.

Firstly, electro-thermally identical MOSFFETs have been simulated in order to understand the internal physics of the device under ideal conditions. The results are shown in Figure 5.8(a) where the inductor charging current and avalanche current characteristics of the device are shown. Different points in the avalanche characteristics have been labelled (A, B and C). Device cross-sections of the DUT have been extracted from the simulator at the time instants corresponding to points A, B and C. Figure 5.8(b) shows the drain voltage characteristics during avalanche mode conduction while Figure 5.8(c) shows the avalanche power versus time profiles of the SiC MOSFET under UIS.

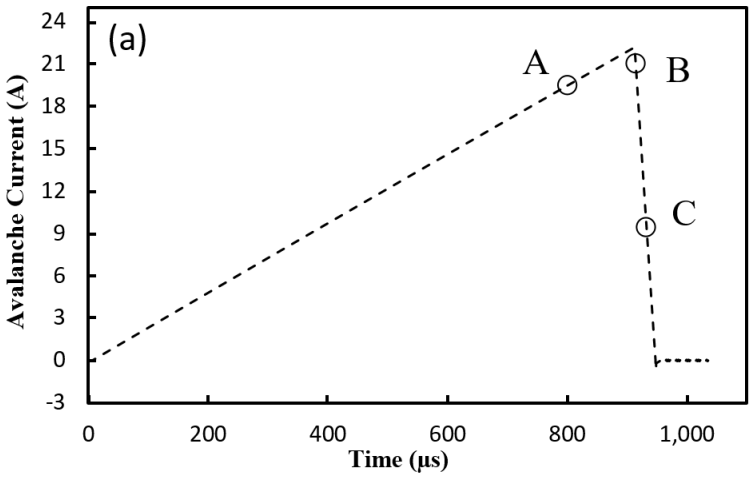


Figure 5.8: (a) The simulated avalanche current characteristics for parallel connect SiC MOSFETs with identical electrothermal conditions. CoolMOS has similar characteristic.

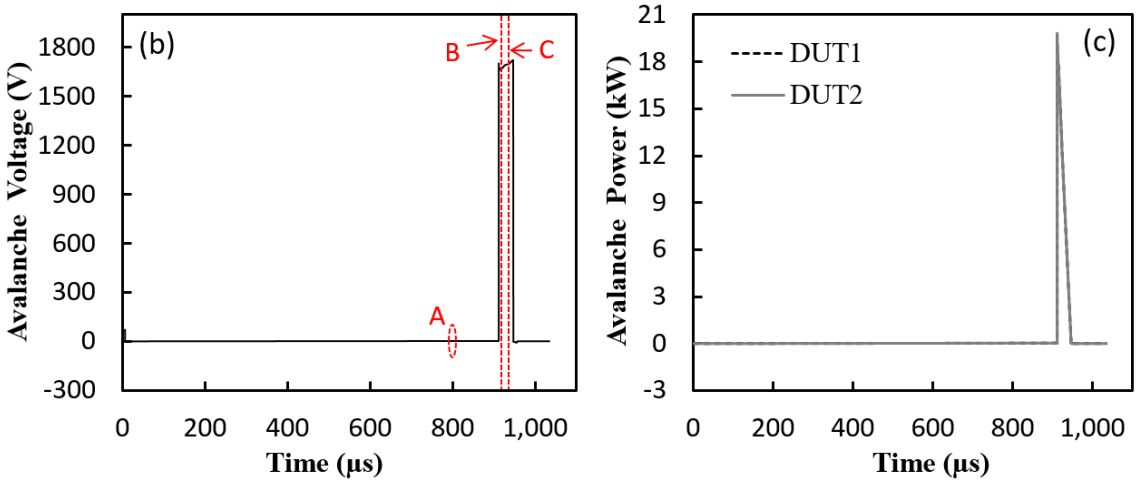


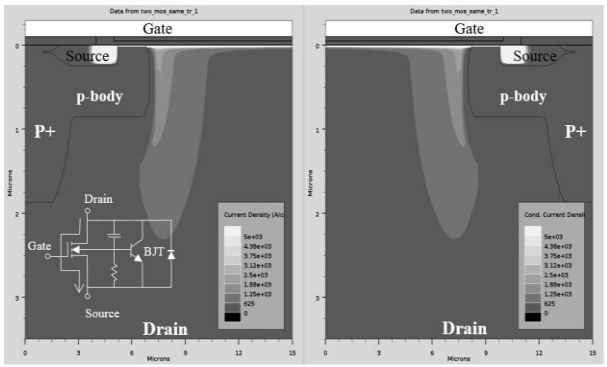
Figure 5.8: (b) the drain voltage and (c) Avalanche power characteristics of 2 parallel connected DUTs with identical electro-thermal parameters under UIS.

Figure 5.9 shows the 2-D current density plot and transient lattice temperature corresponding to point A, B and C marked in Figure 5.8(a). Figure 5.9(a) shows the 2-dimensional current density contour plots of the identical devices corresponding to point A in Figure 5.8(a). At this point, the MOSFETs conduct normally through the channel under drift-diffusion mechanisms. It can be seen that the highest current densities occur in the source, channel and drain regions of the device as expected. Figure 5.9(b) shows the lattice temperature corresponding to point A in Figure 5.8(a) when the channel is

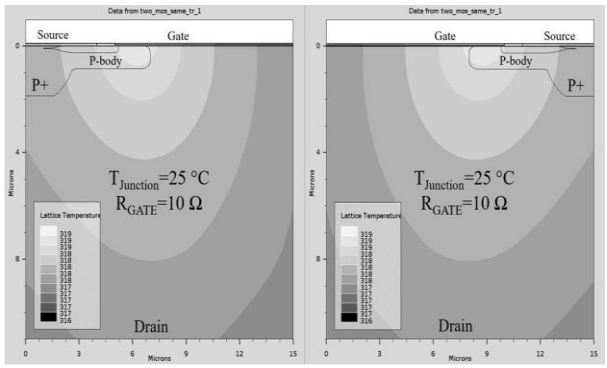
uniformly inverted and conducting the ON-state current. It can be seen from Figure 5.9(b) that the junction between the channel and the lightly doped drift region exhibits the highest temperature within the device. This is due to the fact that the electric field is highest at this point and hence, joule heating is also highest at this point. Figure 5.9(c) shows the 2-dimensional current density contour plot of identical DUTs corresponding to point B in Figure 5.8(a) where avalanche conduction is occurring. It can be seen that, as the uniformly inverted channel cuts off, the current density is more concentrated in the drift region compared to Figure 5.9(a). This is similar to the drain current characteristics when the MOSFET is in saturation. This is due to the fact that the drain voltage across the DUTs increases and the channel becomes pinched-off, the electric field accelerates the electrons in the drift region, thereby resulting in concentrated currents in the drift region. Figure 5.9(d) shows the internal temperature distribution within the SiC device when the channel is cut-off and the device goes into avalanche mode conduction. When the channel pinches off after the device is turned-OFF, the avalanche current is diverted to the anti-parallel body diode, and hence, the temperature distribution reflects this with the highest temperatures occurring at the drain end of the channel. Figure 5.9(e) shows the 2-dimensional current density contour plots of the identical devices at point C corresponding to Figure 5.8(a). At this point, the devices have been switched OFF and the inductor dissipates the current stored in its magnetic field through the devices which are conducting in avalanche.

It can be seen from the current density contour plots in Figure 5.9(e) that the peak avalanche flowing through the device is not through the channel but through the reverse biased body diode comprised of the deep P+ body and the drain. This is how a power device reliably conducts current through the body diode and not through the internal npn BJT. Subsequent 2-D current density plots obtained from the simulator for devices that

have failed under UIS will show high current densities through the npn BJT thereby indicating latch-up. As shown in Figure 5.9(f) that the temperature in the body diode is highest within the device since this is where the bulk of the avalanche current is conducted.

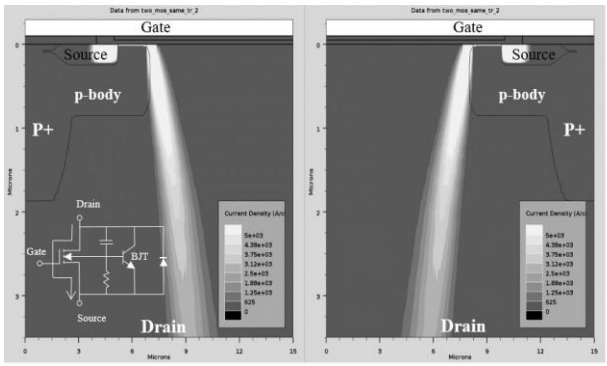


(a) Simulated 2D Avalanche Current Density

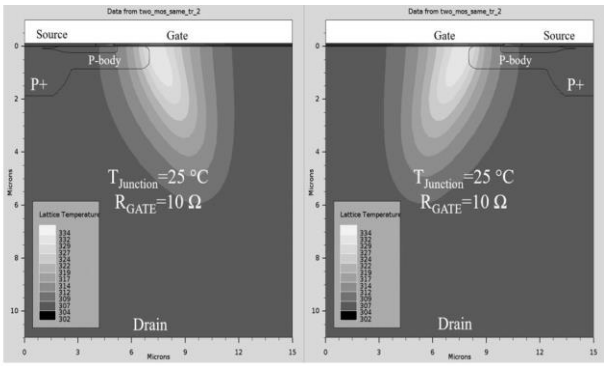


(b) Simulated 2D Temperature Plot

Figure 5.9: The Simulated 2-D (a) current density and (b) lattice temperature contour plots of the parallel connected SiC DUTs at point A corresponding to Figure 5.8(a).

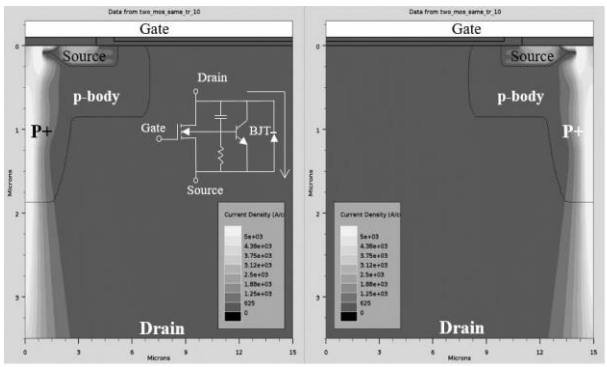


(c) Simulated 2D Avalanche Current Density

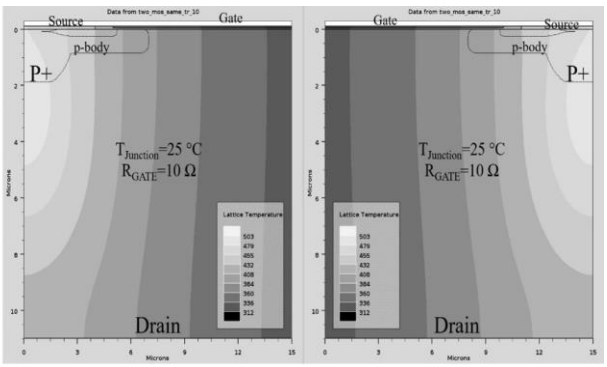


(d) Simulated 2D Temperature Plot

Figure 5.9: The Simulated 2-D (c) current density and (d) lattice temperature contour plots of the parallel connected SiC DUTs at point B corresponding to Figure 5.8(a).



(e) Simulated 2D Avalanche Current Density

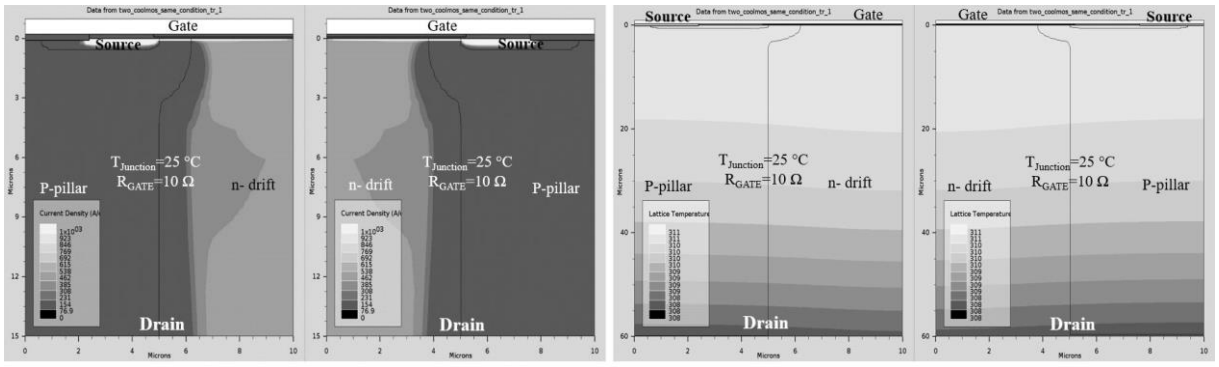


(f) Simulated 2D Temperature Plot

Figure 5.9: The simulated 2-D (e) current density and (f) lattice temperature contour plots of the parallel connected SiC DUTs at point C corresponding to Figure 5.8(a).

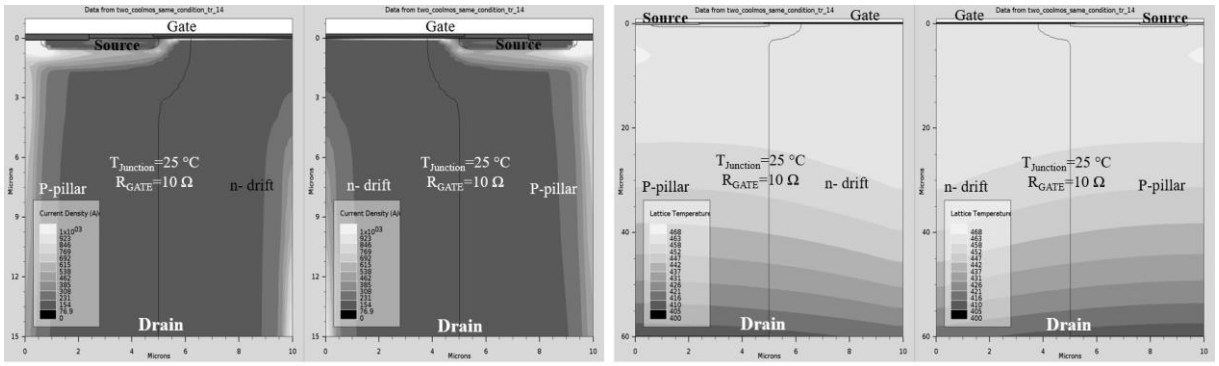
Similar simulations for the parallel-connected CoolMOS devices have been shown in Figure 5.10. The super-junctions in the voltage blocking drift layer is simulated with a balanced doping of 1.05×10^{15} cm^{-3} and the drift layer is simulated with a thickness of 60 µm which results in a breakdown voltage of 1.1 kV. A p-body doping of 1×10^{17} cm^{-3} was used in combination with a 1×10^{19} cm^{-3} p+ doping for the body diode shorting the source to the body. The source and drain regions were degenerately doped with n+ implants and an oxide thickness of 80 nm was used for the gate dielectric. The CoolMOS has similar avalanche characteristic as SiC MOSFET shown in Figure 5.8, Figure 5.10(a), 5.10(c) and 5.10(e) shows the simulated 2-D current density plots for the parallel-connected CoolMOS devices corresponding the point A, B and C in Figure 5.8(a). Figure 5.10(b) 5.10(d) and 5.10(f) shows the simulated 2-D transient lattice temperature plots for the CoolMOS devices corresponding to points A, B and C in Figure 5.8(a). It can be seen that current is initially being conducted through the channel and the n-pillar drift region as shown in Figure 5.10(a). Figure 5.10(b) shows that the highest temperature within the CoolMOS device occurs closest to the channel of the device. After the channel turned-OFF, the current is diverted into the body diode as shown in Figure 5.10(c). As can be seen in Figure 5.10(c), the current density in the CoolMOS p-pillar is less concentrated and unlike the case of the SiC MOSFET, there are considerable lateral currents. These simulations show that the p-pillar and hence, the body diode is more conductive. Figure 5.10(e) shows that there are 2 current flow paths for the avalanche current. These are the body diode p-pillar and the parasitic npn transistor formed in the CoolMOS device. The CoolMOS device has significantly larger area internal PN junctions compared to the SiC MOSFET. This is due to the super-junctions that are required for charge balancing. Hence, the internal parasitic BJT has a larger area and thus exhibits lower current densities as can be seen in Figure 5.10. These current densities are

significantly lower than the SiC MOSFET current densities because the currents are less concentrated in the internal body diodes.



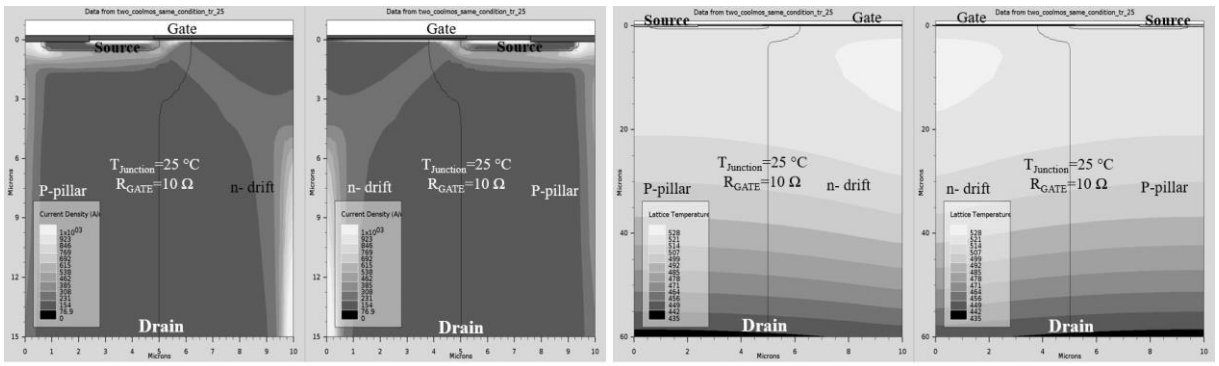
(a) Simulated 2D Avalanche Current Density (b) Simulated 2D Temperature Plot

Figure 5.10: The simulated 2-D (a) current density and (b) lattice temperature contour plots of the parallel connected CoolMOS DUTs at point A corresponding to Figure 5.8(a).



(c) Simulated 2D Avalanche Current Density (d) Simulated 2D Temperature Plot

Figure 5.10: The simulated (c) 2-D current density and (d) lattice temperature contour plots of the parallel connected CoolMOS DUTs at point B corresponding to Figure 5.8(a).



(e) Simulated 2D Avalanche Current Density (f) Simulated 2D Temperature Plot

Figure 5.10: The simulated (e) 2-D current density and (f) lattice temperature contour plots of the parallel connected DUTs at point C corresponding to Figure 5.8(a).

5.6 Unclamped Inductive Switching Measurements on Parallel Connected DUTs (Impact of Junction Temperature Variation).

The junction temperature of the DUT is determined by using an electric hot-plate shown in Figure 5.3(b) which is set individually for each DUT. Figure 5.11 shows the experimental measurements performed with DUT1 and DUT2 with initial junction temperatures of 25 ^{0}C and 50 ^{0}C respectively where it can be seen that DUT1 fails under UIS induced latch-up while DUT2 does not. These measurements were repeated to ensure statistical integrity of the analysis. The reason for the failure in the cooler device is twofold. First, the DUT with the lower junction temperature conducts more current during the inductor charging phase which is due to lower on-state resistance [19]. This can be seen in Figure 5.11 where the DUT with the lower junction temperature has a higher current slope (dI_{DS}/dt) because of the lower on-state resistance. Secondly, the higher junction temperature in DUT2 means the device has a higher breakdown voltage. Breakdown voltage increases with temperature as a result of the reduced carrier mean free path from increased phonon scattering delaying the on-set of impact ionization. Hence, the bulk of the avalanche current flows through DUT1 because it has a lower breakdown voltage thereby resulting in failure under UIS in DUT1. The measurement was repeated for a range of temperature differences between the DUTs and it was seen that the DUT with the lower junction temperature always failed. It can also be seen from Figure 5.11(a) and (b) that the difference in the peak avalanche current between the parallel connected DUTs is higher for the CoolMOS than for the SiC MOSFET. This is due to the lower temperature coefficient of the on-state current in SiC compared to the CoolMOS device; hence, the imbalance in peak avalanche current between the parallel connected DUTs is lower in SiC than in CoolMOS.

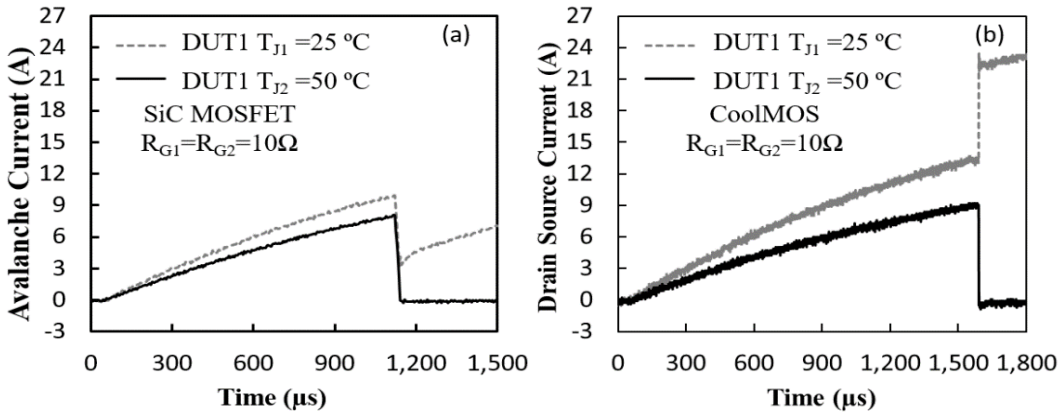


Figure 5.11: (a) The measured inductor charging and avalanche characteristics for the parallel connected SiC MOSFETs with different initial junction temperatures. (b)Similar characteristics for the CoolMOS.

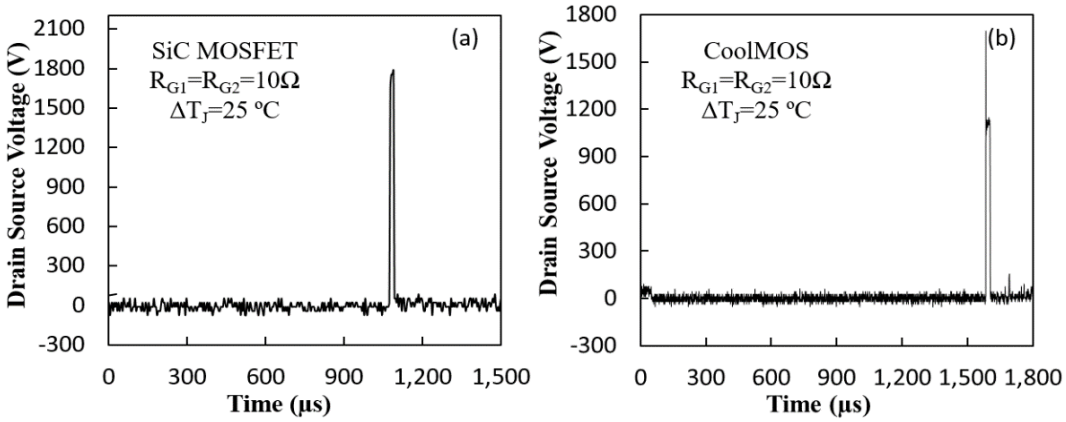


Figure 5.12: (a) The measured drain source voltage during the charging and avalanche conduction for the parallel connected SiC MOSFETs with different initial junction temperatures. (b). Similar characteristics for the CoolMOS.

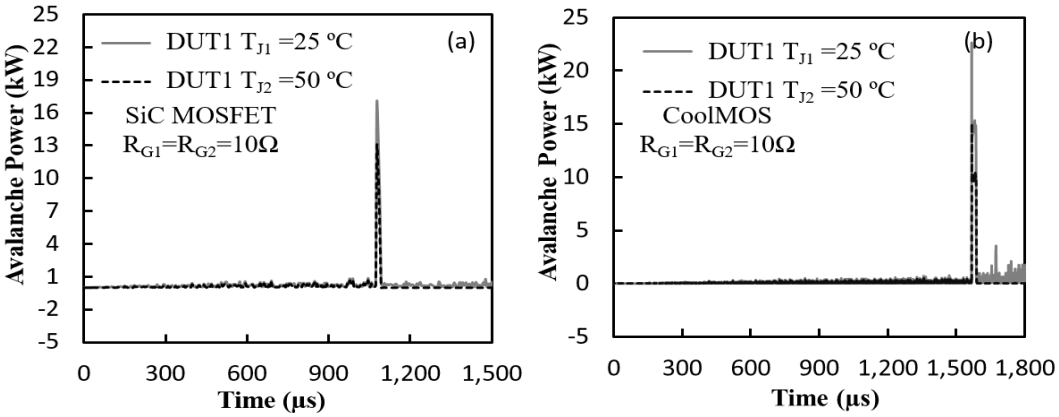


Figure 5.13: (a) The measured power loss during charging and avalanche conduction for the parallel connected SiC MOSFETs with different initial junction temperatures. (b). Similar characteristics for the CoolMOS.

Figure 5.14 shows the peak avalanche current successfully dissipated as a function of the temperature difference between DUT1 and DUT2 for the parallel-connected SiC MOSFETs and CoolMOS devices respectively. These measurements have been performed with 3 different avalanche durations which have been set by 3 different inductors (1, 2 and 3 mH). It can be seen from Figure 5.14 that the peak avalanche current sustainable by the device decreases as the avalanche duration (inductor) increases as expected. It can also be seen that the maximum combined avalanche currents of both DUTs marginally reduce as the temperature difference between the DUTs increases. This is due to increased current crowding in the lower temperature DUT as the temperature difference rises. For the SiC devices in Figure 5.14(a), the peak avalanche current sustainable by the parallel pair reduces marginally as the temperature difference between the parallel DUTs increases i.e. when $\Delta T_J = T_{JDUT2} - T_{JDUT1} = 0\ °C$ (the same initial junction temperature), the peak avalanche current is 27.12 A, 20.96 A and 17.54 A at 1 mH, 2 mH and 3 mH respectively for the SiC DUTs. As the temperature difference between the parallel SiC DUTs is increased to $\Delta T_J = T_{JDUT2} - T_{JDUT1} = 80\ °C$, the peak avalanche current reduces to 25.02 A, 19.41 A and 16.3 A for the 3 inductors. This represents a change of 7.74%, 7.39% and 7.06% for the 1 mH, 2 mH and 3 mH inductors respectively. In the case of the parallel CoolMOS DUTs under avalanche, the peak avalanche current dropped from 32.95 A, 27.9 A and 23.75 A to 21.44 A, 21.15 A and 18.06 A for the 1 mH, 2 mH and 3 mH inductor respectively, therefore the percentage change in the peak sustainable avalanche current decreases by 34.95%, 24.19% and 23.96% as $\Delta T_J = T_{JDUT2} - T_{JDUT1}$ is increased from 0 to 80 °C. Hence, although the peak avalanche current is higher for the parallel CoolMOS devices at $\Delta T_J = T_{JDUT2} - T_{JDUT1} = 0\ °C$, the rate of change of this parameter is higher as more electrothermal balance is introduced in the initial conditions. Hence, SiC devices are more capable of balanced electrothermal operation between

parallel DUTs under avalanche.

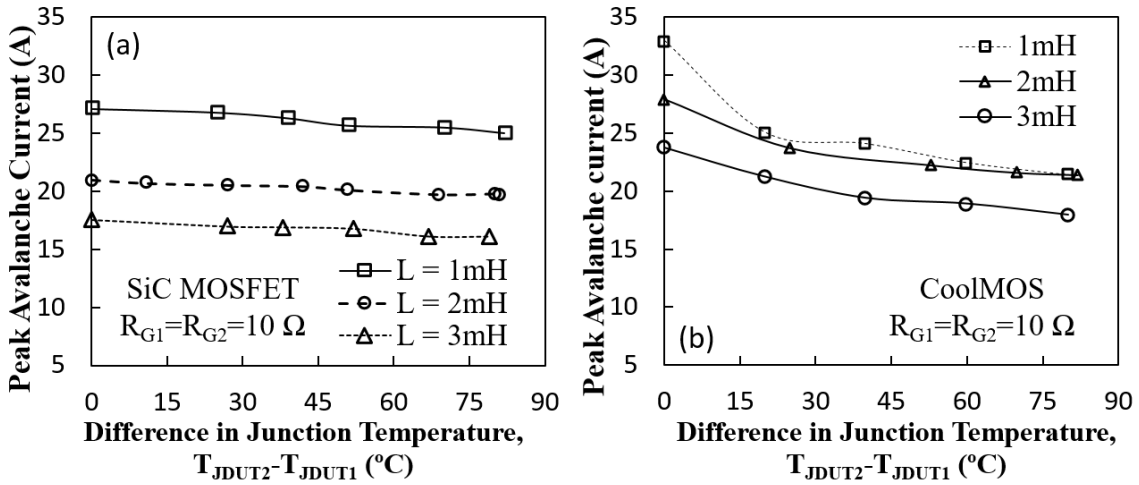


Figure 5.14: (a) The measured peak avalanche currents conducted by the DUTs as a function of the temperature difference between the parallel connected SiC MOSFETs for 3 avalanche durations (inductance sizes). (b) Similar characteristic for the CoolMOS.

Figure 5.15 shows the maximum measured avalanche energy successfully dissipated by the DUTs before failure under UIS for the 3 avalanche durations. It can be seen from Figure 5.15 that the energy is higher when the avalanche duration is increased since the DUTs sustain the highest avalanche energies for the case of the 3 mH inductor. This implies that the mismatch in junction temperature is more detrimental to the overall avalanche ruggedness of the parallel-connected devices when the UIS event occurs with high current and low inductance. This is expected since failure under UIS is triggered by current crowding which is aggravated by higher current densities. It can be seen that the parallel connected SiC MOSFET perform better under temperature imbalance. Although the peak avalanche energy reduces with increasing temperature mismatch (ΔT_J) between the parallel connected DUTs, the reduction is quite small for the SiC MOSFETs compared with CoolMOS devices.

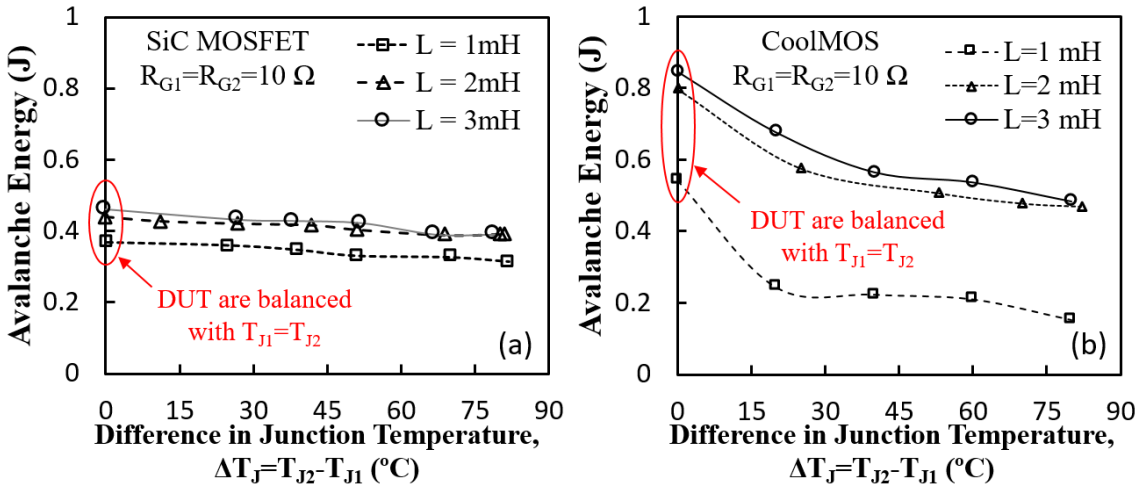


Figure 5.15: (a) The measured avalanche energy successfully dissipated by the combined SiC MOSFETs as a function of the temperature difference between the DUTs for 3 avalanche durations (inductor sizes). (b) Similar characteristic for the CoolMOS devices.

Figure 5.16 shows the comparison of the percentage change in the measured peak avalanche energy (E_{AV}) for different temperature variation ΔT_J between the parallel SiC and CoolMOS devices. It can be seen that the parallel connected SiC MOSFETs exhibits smaller variation in the avalanche characteristics. This is due to the fact that it is a wide bandgap material and therefore exhibits lower temperature sensitivity since higher temperatures are required for generating carriers.

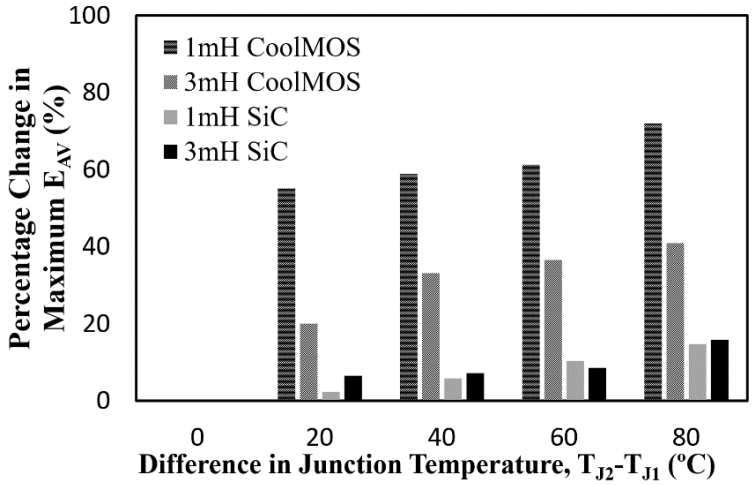


Figure 5.16: Percentage change in the peak avalanche energy (E_{AV}) as a function of the temperature difference between the parallel DUTs.

5.7 Finite Element Simulation of UIS in Parallel Connected DUTs (Impact of Junction Temperature Variation)

Similar to the experiments, the impact of different initial junction temperatures on the avalanche mode conduction of parallel connected devices has been investigated. The results are shown in Figure 5.17, where the transient UIS characteristics can be seen for the devices with the same and with different initial junction temperatures. It can be seen from Figure 5.17 that the devices with $T_{J1}=T_{J2}$ pass the UIS test while those with $T_{J1}\neq T_{J2}$ undergo parasitic bipolar latch-up.

Figure 5.18(a) shows the simulated current waveforms conducted through each parallel DUT for the SiC MOSFETs switched with different initial junction temperature. Figure 5.18(b) shows the simulated drain voltage characteristics of the parallel-connected devices. It can be seen from Figure 5.18(a) that, similar to the experimental measurements, the DUT simulated with the higher initial junction temperature does not undergo thermal runaway through BJT latch-up, while the DUT with the lower junction temperature does. Avalanche mode conduction results in high instantaneous power dissipated in the DUTs since there is simultaneously high voltage across the device as the current flows through the DUTs. For instance, as shown in Figure 5.3(c), the voltage across the DUT reaches approximately 1.8 kV as the avalanche current starts gradually falling from a peak of 9 A, which results in approximately 16.2 kW of instant power dissipated in the DUTs. Figure 5.18(c) shows the simulated avalanche power dissipated within the parallel DUTs where it can be seen that DUT1 exhibits a higher avalanche energy. This high instantaneous avalanche power results in a rapid temperature rise within the device. Figure 5.18(d) shows the simulated peak temperature within the DUT for the parallel-connected SiC MOSFETs switched at different initial junction temperatures.

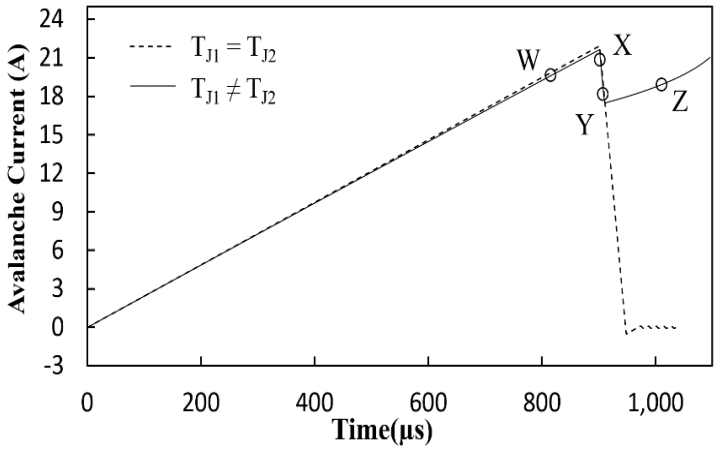


Figure 5.17: The simulated UIS characteristics of 2 parallel connected DUTs at identical and different initial junction temperatures.

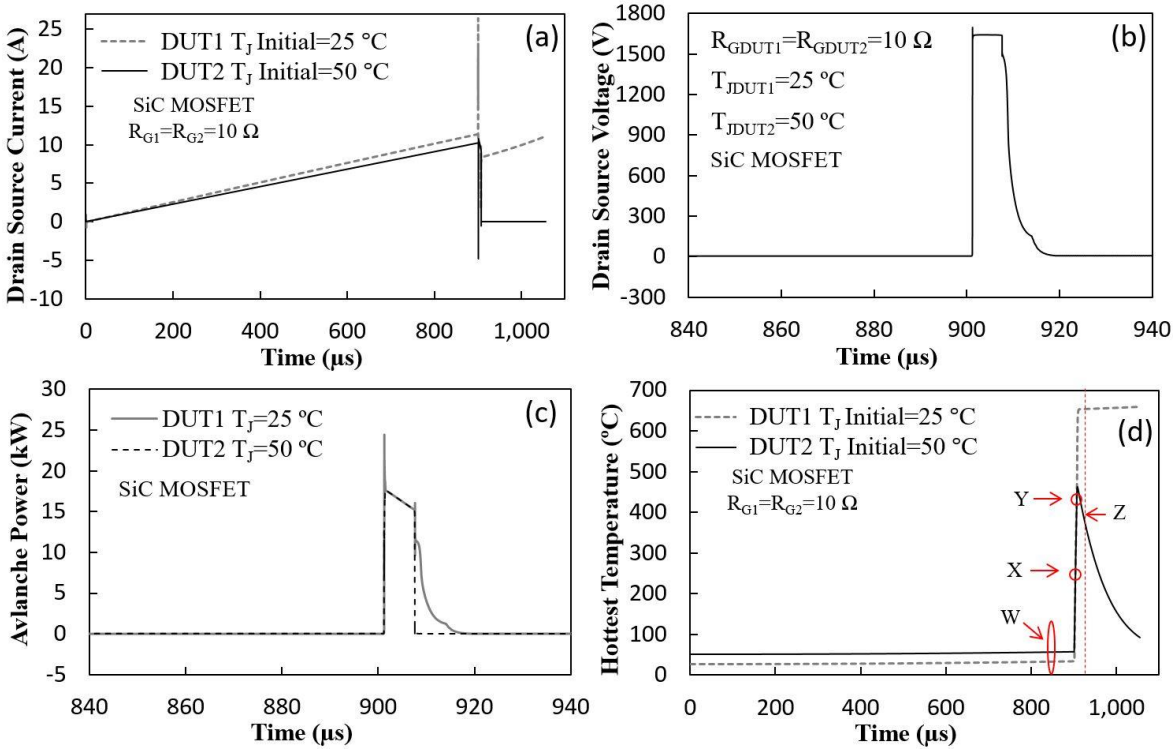
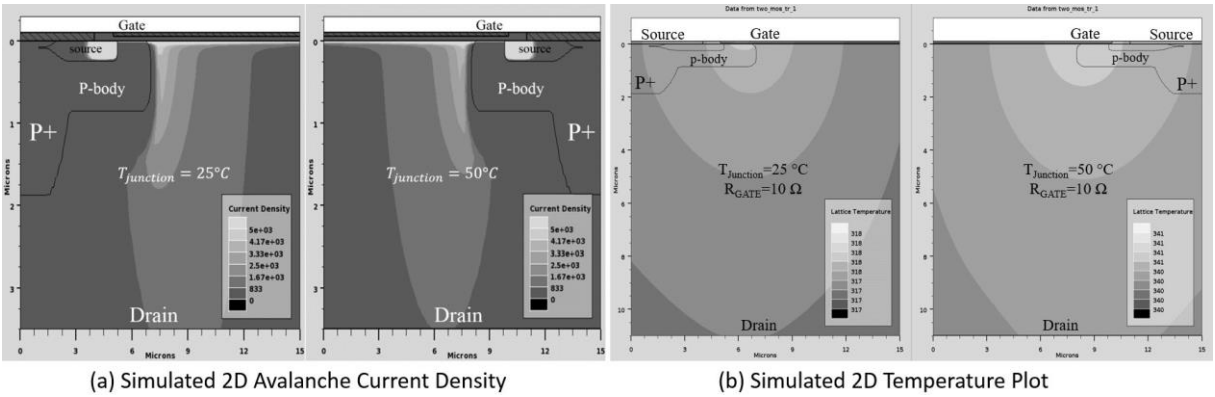


Figure 5.18: The Simulated (a) Avalanche current; (b) Drain Voltage; (c) Power and (d) Temperature of the parallel connected DUTs respectively during the UIS.

Figure 5.19(a) and (b) show the simulated 2-D current density and lattice temperature contour plots for the simulated SiC MOSFET at the time instant corresponding to point W in Figure 5.17 where the SiC DUTs are in conduction mode. Figure 5.19(c) and (d) show the 2-D current density and lattice temperature contour plots corresponding to the

time instant X in Figure 5.17 where the DUTs are in avalanche mode conduction. Figure 5.19(e) and (f) show the 2-D current density and lattice temperature contour plots corresponding to the time instant Y in Figure 5.17 where the lower initial temperature DUT starts undergoing BJT latch-up while the higher initial temperature DUT continues in avalanche. Figure 5.19(g) and (h) show the 2-D current density and lattice temperature contour plots corresponding to the time instant Z in Figure 5.17 where one DUT is in thermal runaway while the other DUT is OFF.

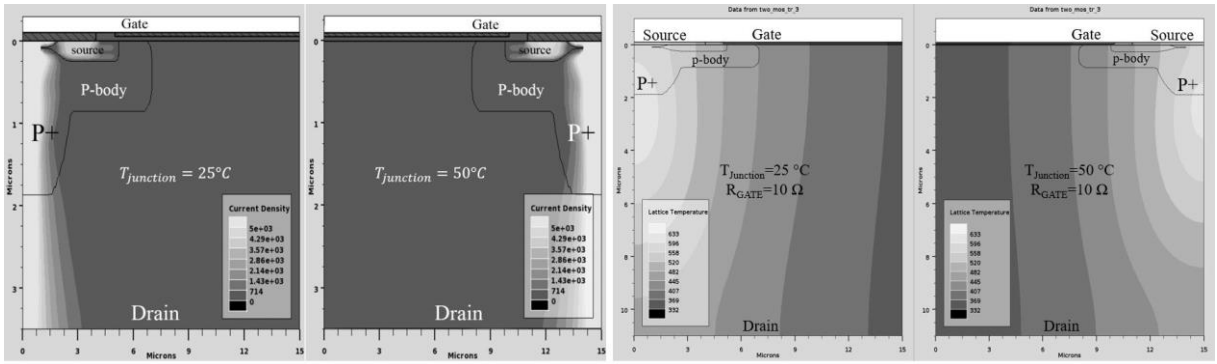
Figure 5.19(a) shows the 2-D current plot at point W when both channels are conducting normally. On closer inspection, it can be seen that the lower temperature device on the LHS has a slightly higher current density because the reduced on-state resistance. Figure 5.19(b) shows the 2-D lattice temperature plots of the parallel SiC DUTs conducting current in the normal ON-state mode corresponding to point W in Figure 5.17. It can be seen from Figure 5.19(b) that the highest temperature point within the SiC MOSFET is at the channel to drain junction because that is where the electric field is highest.



(a) Simulated 2D Avalanche Current Density (b) Simulated 2D Temperature Plot

Figure 5.19: The simulated (a) 2-D current density and (b) lattice temperature contour plots for devices with different initial junction temperatures at point W corresponding to Figure 5.17.

Figure 5.19(c) shows the current density plot corresponding to point X in Figure 5.17 when both devices go into avalanche mode conduction. It can be seen from Figure 5.19 that both devices go safely into avalanche by conducting the current through the body diode. Figure 5.19(d) shows the 2-D lattice temperature contour plot corresponding to X. At this point, the DUTs have been switched OFF and avalanche current starts flowing through the anti-parallel body diode, hence the highest temperature point moves to the body diode.

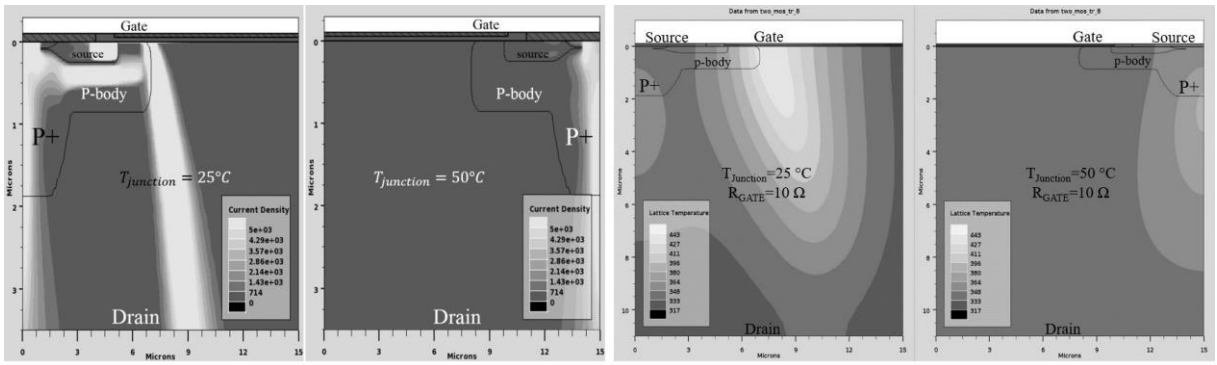


(c) Simulated 2D Avalanche Current Density (d) Simulated 2D Temperature Plot

Figure 5.19: The simulated 2-D (c) current density and (d) lattice temperature contour plots for devices with different initial junction temperatures at point X corresponding to Figure 5.17.

Figure 5.19(e) corresponds to the point Y in Figure 5.17 where the DUT with the lower junction temperature is going into thermal runaway due to BJT latch-up. It can be seen that the current is moving away from the antiparallel body diode towards the intrinsic NPN BJT. At this point, the current through the antiparallel body diode of the device simulated with the higher junction temperature is diminishing because the device simulated with the lower initial junction temperature is taking all of the current. Figure 5.19(f) shows the 2-D lattice temperature contour plots at point Y corresponding to Figure 5.17. It can be seen here, that the DUT on the LHS with the initial junction temperature of 25 °C, exhibits significantly higher temperatures compared to the DUT on the RHS. It

can also be noticed that the highest temperature point has moved from the anti-parallel body diode to the bulk of the device where the parasitic BJT is. As the temperature rises, the in-built junction voltage between the emitter and base of the BJT reduces and the p-body resistance increases therefore increasing the possibility that the internal BJT will be triggered.



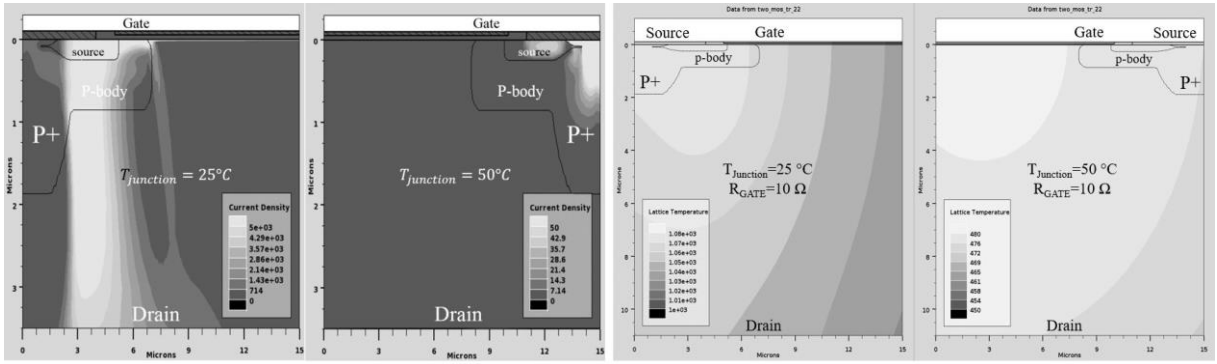
(e) Simulated 2D Avalanche Current Density (f) Simulated 2D Temperature Plot

Figure 5.19: The simulated 2-D (e) current density and (f) lattice temperature contour plots for devices with different initial junction temperatures at point Y corresponding to Figure 5.17.

Figure 5.19(g) shows the 2D current density plot of the parallel DUTs at the time instant corresponding to point Z in Figure 5.17. It can be seen that lower temperature device on the LHS in full BJT latch-up while the higher temperature device stops taking any current. The path of current flow shown in the LHS device in Figure 5.19(g) is through the NPN BJT in the body and not through the anti-parallel diode. Figure 5.19(h) shows the 2D lattice temperature contour plots corresponding to point Z in Figure 5.17 where the DUT on the LHS has failed due to the BJT latch up. The temperature plots show that the hotspots are less concentrated compared to the previous plots which indicates that the heat radiates through the device.

These plots fully explain and agree with the experimental measurements shown in Figure 5.8. The breakdown voltage of the simulated device shows a positive temperature

coefficient. Since avalanche current always flows through the device with the smallest breakdown voltage, the bulk of the avalanche current flows through the device simulated with the lower junction temperature. Using the simulations, it was also confirmed that increasing the difference between the junction temperatures of the parallel-connected devices reduces the total avalanche current the devices can sustain without the cooler device initiating BJT latch-up.



(g) Simulated 2D Avalanche Current Density (h) Simulated 2D Temperature Plot

Figure 5.19: The simulated 2-D (g) current density and (h) lattice temperature contour plots for devices with different initial junction temperatures at point Z corresponding to Figure 5.17.

Similar simulations have been done for the parallel-connected CoolMOS devices, the results of which are shown in Figure 5.20. It can be seen in Figure 5.20(a) that the DUT with the lower initial junction temperature (DUT1), undergoes thermal runaway during the UIS of the parallel pair. Figure 5.20(b) shows the simulated drain voltage characteristics of the parallel-connected CoolMOS devices under UIS. Figure 5.20(c) shows the simulated transient peak temperature within the DUTs. By comparing the thermal runaway temperature for the parallel CoolMOS devices with that of the SiC MOSFETs presented earlier, it can be seen that BJT latch-up occurs at a lower junction temperature for the CoolMOS devices. This is due to the fact that silicon is not as

thermally rugged as SiC. The wide bandgap of SiC means that significantly higher junction temperatures are needed to take the semiconductor into thermal runaway.

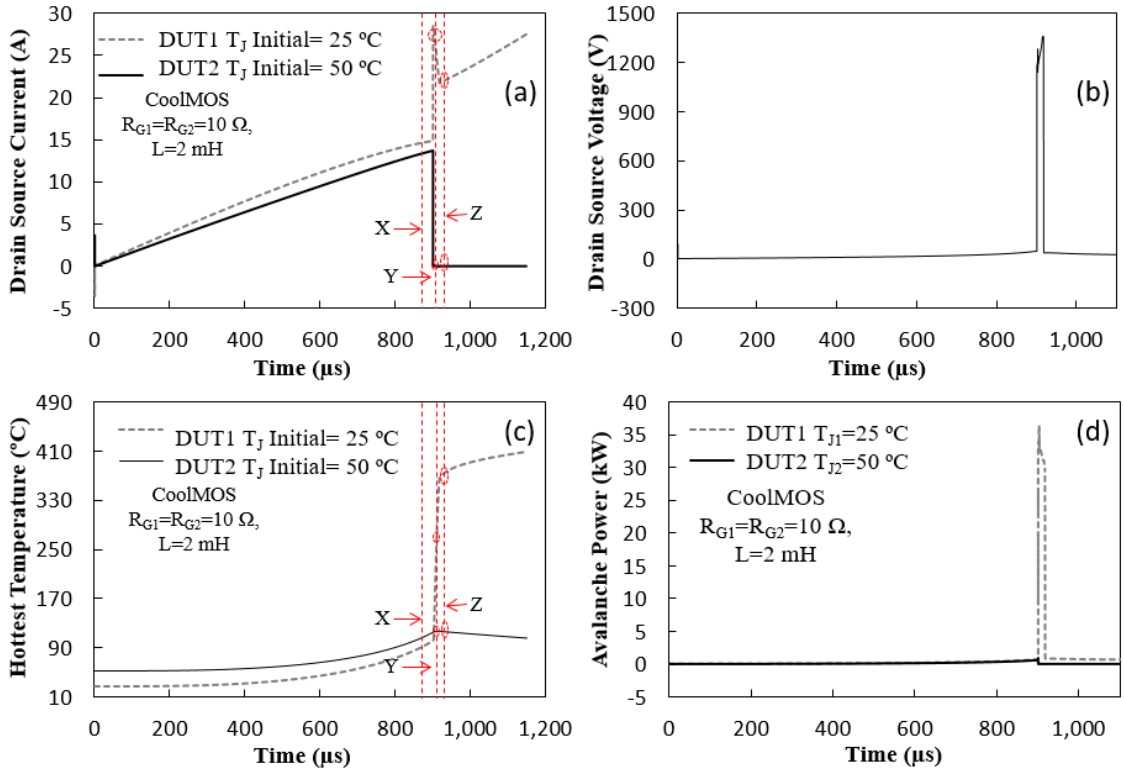
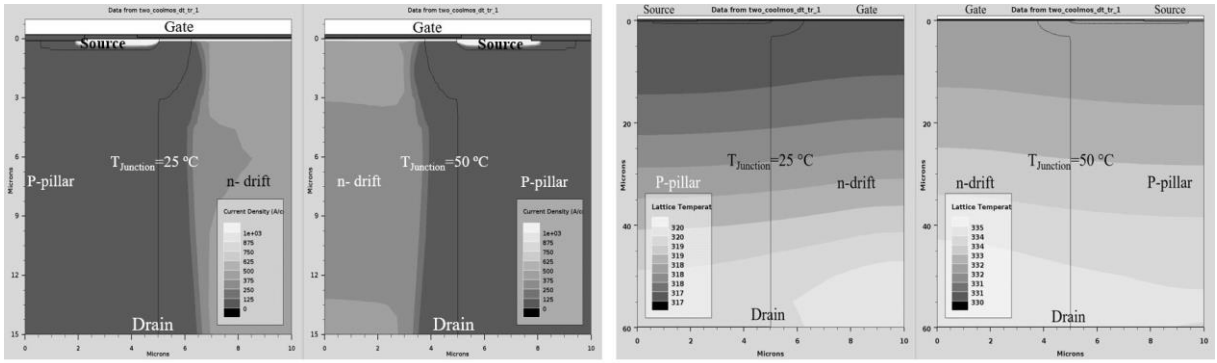


Figure 5.20: The simulated (a) avalanche current, (b) drain voltage (c) Lattice temperature and (d) Avalanche power characteristics for parallel connected CoolMOS devices under UIS at different temperature.

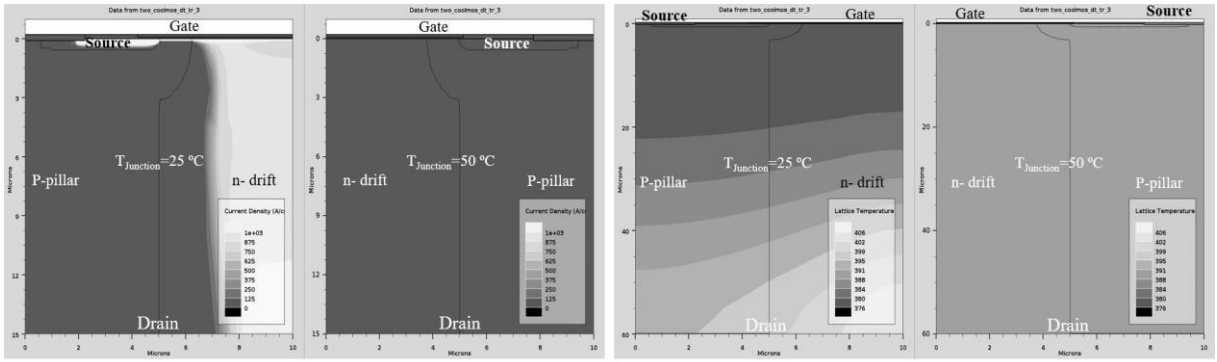
Figure 5.21(a) shows the 2-D current density contour plots at point X (conduction mode) while Figure 5.21(b) shows lattice temperature at the same time instant. Figure 5.21(c) shows the 2-D current density contour plots at point Y (avalanche conduction mode) while Figure 5.21(d) shows the transient lattice temperature at the same time instant when the parallel CoolMOS devices are in avalanche. Figure 5.21(e) and Figure 5.21(f) shows the current density and lattice temperature respectively at point Z corresponding to Figure 5.20(a) where the parallel-connected CoolMOS devices are in BJT latch-up and/or failure mode. As can be seen from Figure 5.21(a), current conducts through the n- drift region within the CoolMOS devices and is slightly higher for the cooler device. It can be seen

that the current density in the simulated CoolMOS DUT with the lower junction temperature on the LHS is higher due to reduced phonon scattering, hence, lower channel and drift resistance. The extracted temperatures from the simulator shown in Figure 5.21(b) are consistent with the temperatures set i.e. heat spreads from the base to the channel as was input in the code.



(a) Simulated 2D Avalanche Current Density (b) Simulated 2D Temperature Plot

Figure 5.21: The simulated 2-D (a) current density and (b) lattice temperature contour plots for parallel connected CoolMOS devices with different initial junction temperatures at point X corresponding to Figure 5.20(a).



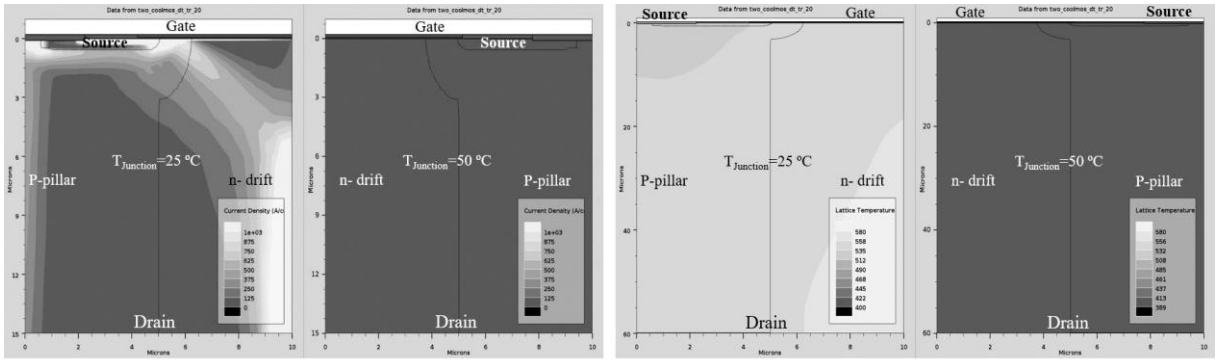
(c) Simulated 2D Avalanche Current Density (d) Simulated 2D Temperature Plot

Figure 5.21: The simulated 2-D (a) current density and (d) lattice temperature contour plots for parallel connected CoolMOS devices with different initial junction temperatures at point Y corresponding to Figure 5.20(a).

Figure 5.21(c) and Figure 5.21(d) show the current density plots and the lattice temperature corresponding to the time instant at point Y with respect to Figure 5.20(a). It can be seen from Figure 5.21(c) that the initially cooler device conducts the entirety of

the avalanche current and the CoolMOS DUT on the RHS does not conduct any current. At this time instant, the DUT with initially lower junction temperature has a higher peak temperature as well as a higher temperature gradient within the device.

Figure 5.21(e) and 5.21(f) show the 2-D current density and lattice temperature extracted from the simulator at time instant Z where the DUT on the LHS is in BJT latch-up while the RHS device is OFF. It can be seen from Figure 5.21(e) that the current flows in the simulated LHS CoolMOS DUT through the parasitic NPN BJT. It can also be seen from Figure 5.21(e) that, unlike the SiC MOSFET DUT, there are significant lateral currents in the CoolMOS device undergoing BJT latch-up. Figure 5.21(f) shows the 2-D lattice temperature contour plot for the simulated parallel-connected CoolMOS DUTs where significantly higher temperatures can be seen in the LHS DUT that has undergone BJT latch-up. Similar to the experimental measurements, the initially cooler device fails under UIS for both the SiC MOSFETs and the CoolMOS devices. The simulations also show that the SiC MOSFETs are more thermally rugged under electrothermal variations between the parallel DUTs.



(e) Simulated 2D Avalanche Current Density (f) Simulated 2D Temperature Plot

Figure 5.21: The simulated (e) Current density and (f) Lattice temperature 2-D contour plots for parallel connected CoolMOS with different junction temperatures corresponding to point Z in Figure 5.20(a).

5.8 Impact of Variation in Switching Rates between the Parallel DUTs on Avalanche Ruggedness

The switching rate of the DUTs is set by simply changing the gate resistances. Figure 5.22(a) shows the measurement results for the UIS experiments with the parallel-connected SiC MOSFETs switched with different gate resistances. Here DUT1 is switched with R_G=10 Ω while DUT2 is switched with R_G=33 Ω. Figure 5.22(b) shows similar measurements for the parallel-connected CoolMOS devices. Figure 5.23 and 5.24 show the measured drain-source voltage characteristics and avalanche power dissipation during avalanche mode conduction for the parallel connected DUTs. In both figures, (a) shows the parallel-connected SiC MOSFET characteristics while (b) shows the CoolMOS characteristics. It can be seen from Figure 5.22 that DUT2, which is the slower switching device with R_G=33 Ω, fails while DUT1 does not. The test has been repeated for different combination of gate resistances and on all occasions the slower switching device fails under UIS while the faster switching device does not. The reason for this, as subsequent finite element models will show, is that the slower switching device is more conductive during UIS since there is a residual channel due to the slower turn-OFF transient. Since the DUT with the larger gate resistance (lower dI_{DS}/dt) switches off more slowly, the channel is more conductive, thereby exacerbating current crowding within the device. Figure 5.25 shows the peak combined avalanche current for both DUTs (before the failure of either under UIS) as a function of the difference between the gate resistances between the DUTs. The measurements in Figure 5.25 have been performed for 3 different avalanche durations i.e. 3 different inductors namely 1, 2 and 3 mH. It can be seen from Figure 5.25 that the peak combined avalanche current of both DUTs before failure decreases as the difference between the gate resistances of DUT1 and DUT2 increases.

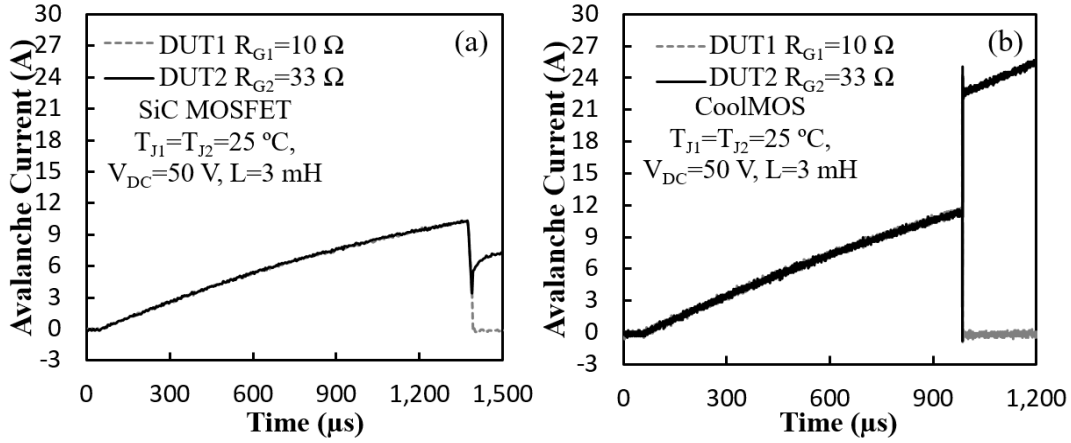


Figure 5.22: (a) Avalanche current characteristics for the parallel connected SiC MOSFETs with different R_G. (b) Similar characteristics for CoolMOS.

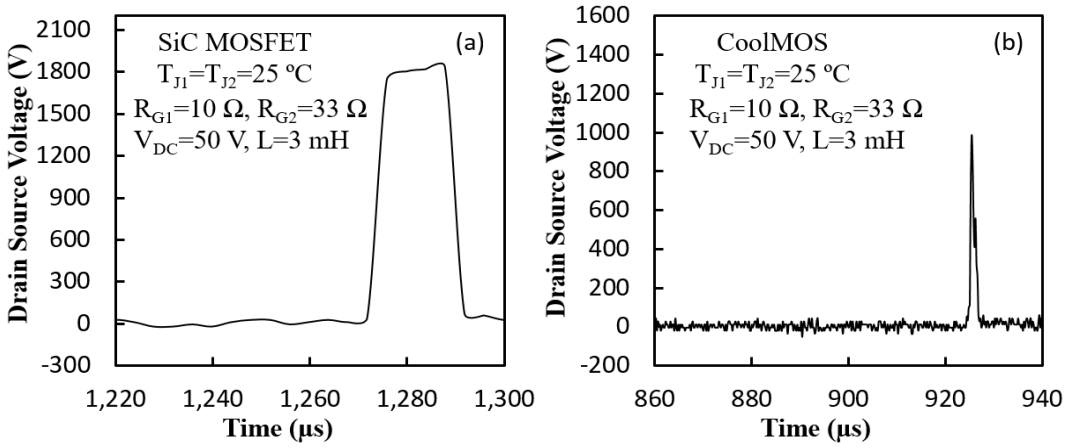


Figure 5.23: (a) The measured drain voltage for parallel connected SiC MOSFETs with different R_G. (b) Similar characteristics for CoolMOS.

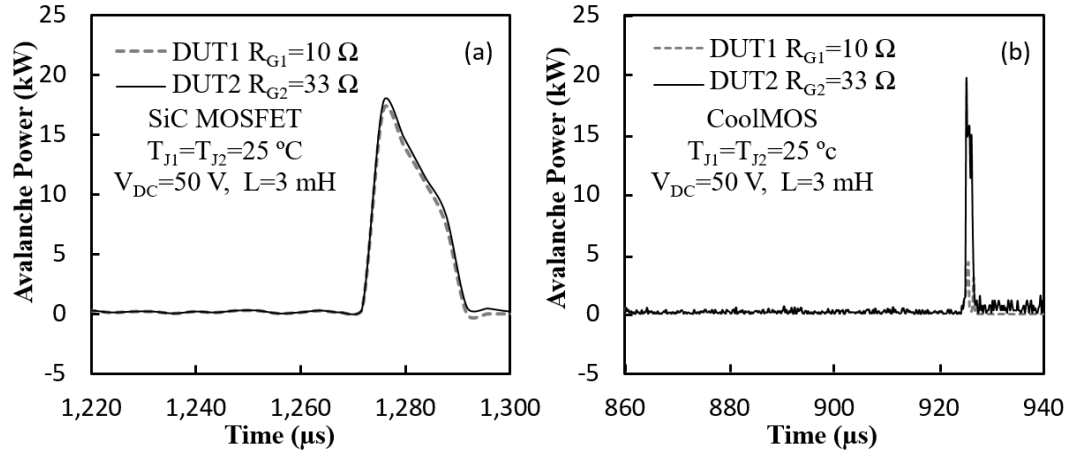


Figure 5.24: (a) The measured avalanche power for parallel connected SiC MOSFETs with different R_G. (b) Similar characteristics for CoolMOS.

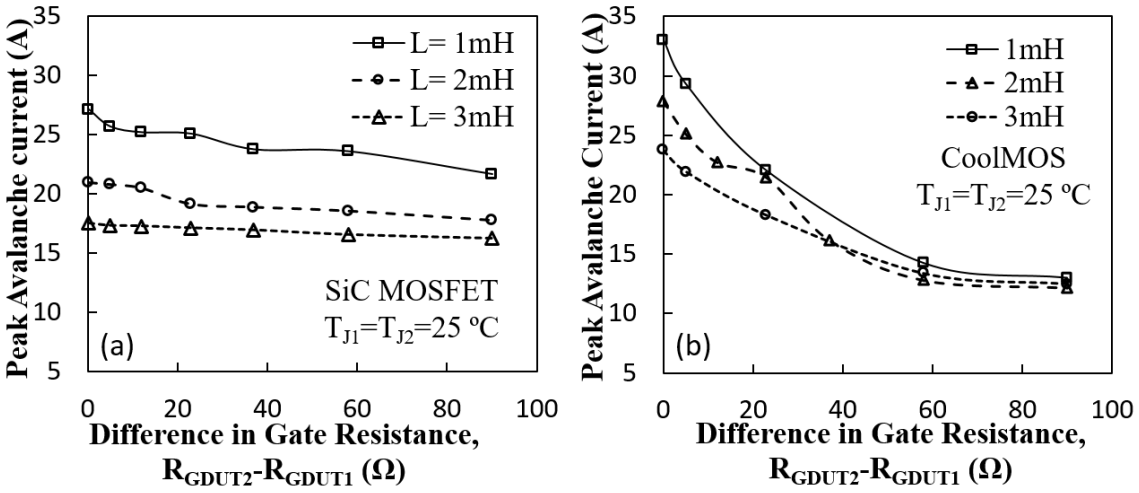


Figure 5.25: The measured peak combined avalanche currents conducted by the DUTs as a function of the switching rate difference between the DUTs for 3 avalanche durations (inductance sizes) for parallel (a) SiC MOSFETs and (b) CoolMOS devices.

This is expected since further increment in the difference between the switching rates of the DUTs will exacerbate current crowding in the slower switching DUT. Figure 5.26 shows the measured maximum avalanche energy successfully dissipated in both DUTs as a function of the difference between the gate resistances (and dI_{DS}/dt) in the DUTs. Again, the measurements have been performed with different inductors (1, 2 and 3 mH) to investigate the impact of avalanche duration on the reliability of the DUTs switching with different rates. It can be seen from Figure 5.26 that the avalanche energy sustainable by the combined DUTs increases with the avalanche duration for a given mismatch in the switching rate. In other words, differences in the switching rates of parallel connected DUTs degrades the overall avalanche ruggedness of the device faster for high current low inductance UIS pulses compared with low current high inductance UIS pulses. Hence, similar to the case of variation of junction temperatures between the DUTs, the effect is exacerbated by higher current densities. Figure 5.27 shows the comparison of the percentage change in the measured peak avalanche energy (E_{AV}) for different ΔR_G in the parallel SiC and CoolMOS devices. It can be seen that the percentage change in the

maximum avalanche energy is significantly smaller in the SiC MOSFETs than in the CoolMOS devices.

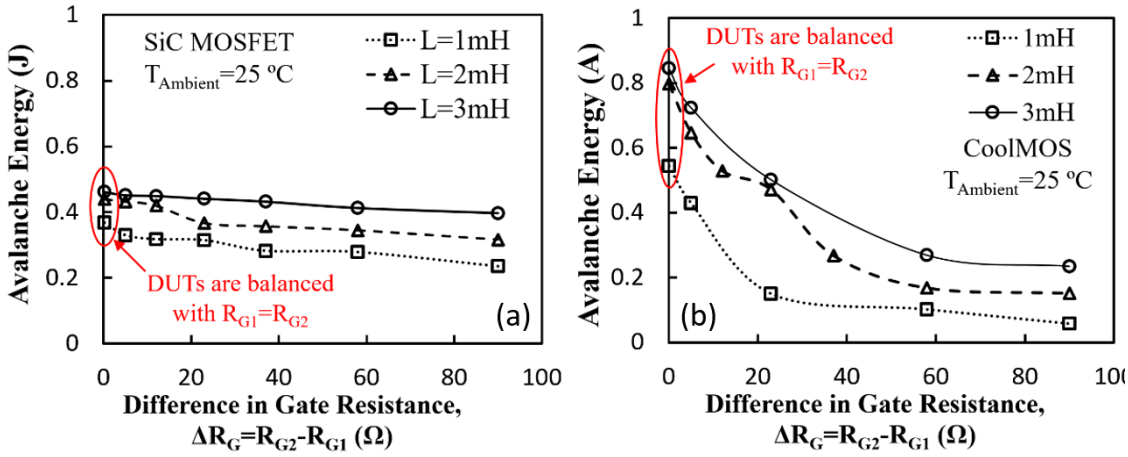


Figure 5.26: The measured avalanche energy safely dissipated by the combined DUTs as a function of the switching rate difference between the DUTs for 3 avalanche durations (inductor sizes).

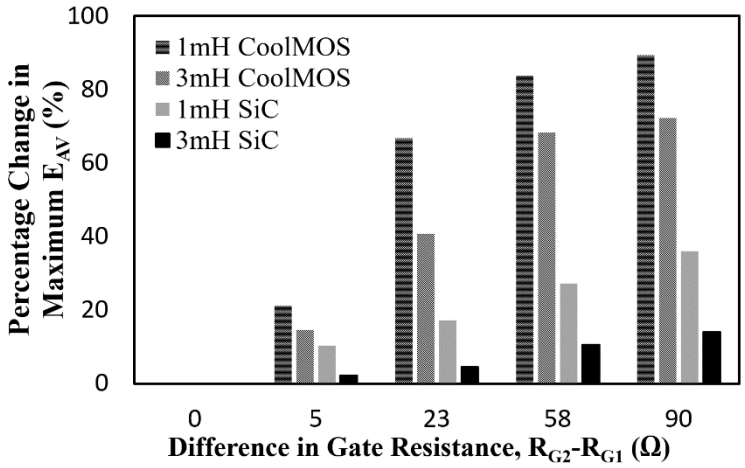


Figure 5.27: Percentage change in the peak avalanche energy (E_{AV}) as a function of the switching rate difference between the parallel DUTs.

5.9 Finite Element Simulations of the Impact of Different Switching Rates

Similar simulations have been performed to investigate the impact of different switching rates on parallel-connected DUTs under UIS. Figure 5.28(a) and 5.28(b) show the simulated UIS current and voltage characteristics for parallel connected SiC MOSFETs switched at same and different rates with different gate resistances. It can be seen in Figure 5.28(a) that similar to the experimental measurements presented earlier, the devices simulated with $R_{G1}=R_{G2}$ successfully dissipate the avalanche current while the devices with $R_{G1}\neq R_{G2}$ undergo thermal runaway during UIS.

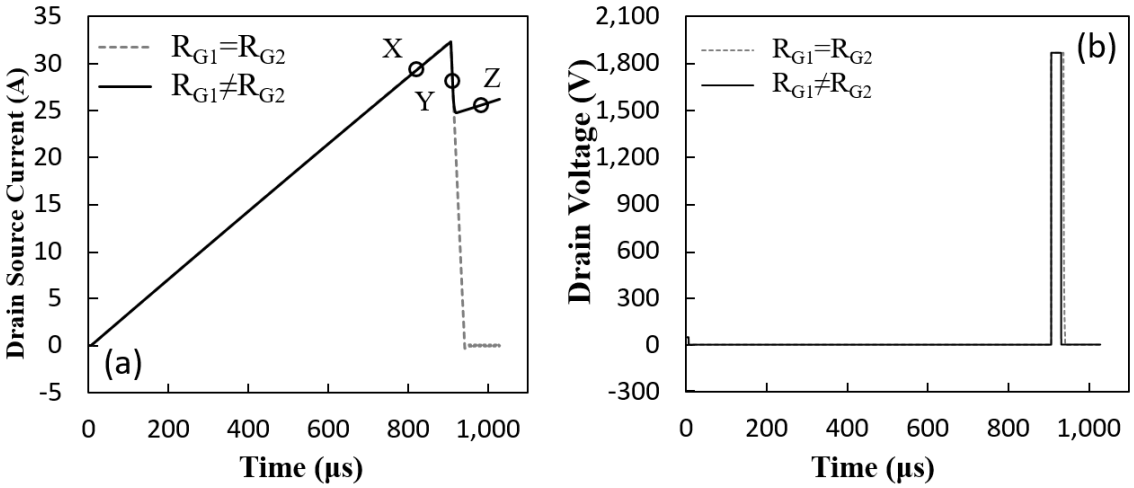
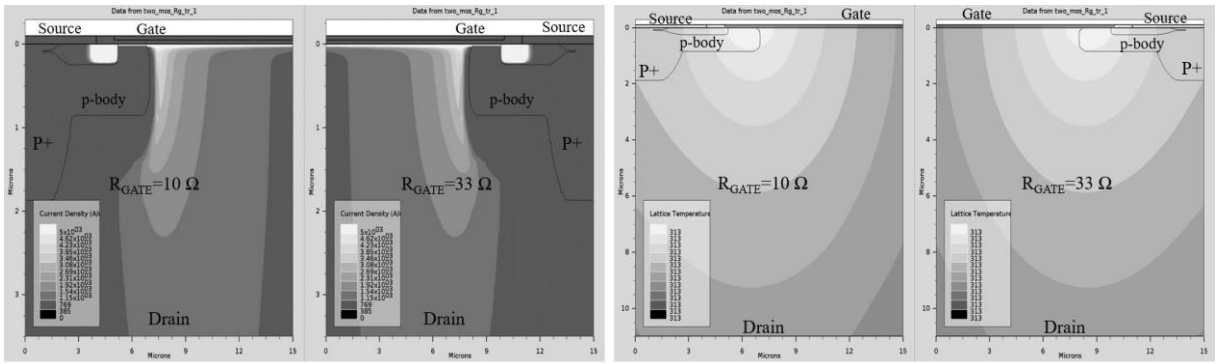


Figure 5.28: Simulated UIS characteristics of 2 parallel connected DUTs at the same and different switching rates.

Figure 5.29(a) shows the 2-D current density contour plots in the simulated parallel connected SiC MOSFETs at point X where it can be seen that both devices conduct current normally. The devices share the current equally during the steady state since differences in the switching time will cause differences only during switching transients. Figure 5.29(b) shows the simulated transient lattice temperature 2-D plot where it can be seen that the MOSFET channel exhibits the highest temperature. Under steady state

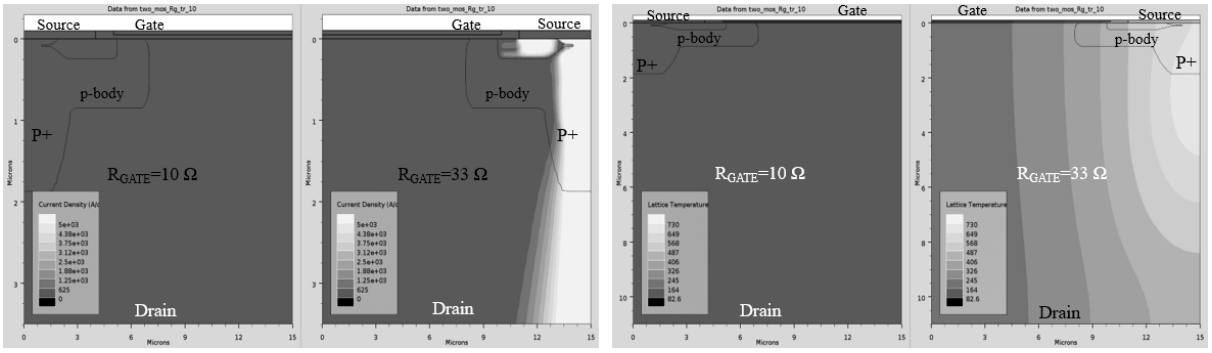
conditions, differences in the switching rate have no effect on the thermal and current distribution between the parallel DUTs.



(a) Simulated 2D Avalanche Current Density (b) Simulated 2D Temperature Plot

Figure 5.29: The simulated 2-D (a) current density and (b) lattice temperature contour plots for the parallel-connected devices with different switching rates at point X corresponding to Figure 5.28(a).

Figure 5.29(c) shows the 2-D current density contour plots of the simulated parallel connected DUTs at point Y during avalanche mode conduction after the devices have been switched-OFF. Figure 5.29(d) shows the corresponding 2-D lattice temperature plots for the simulated parallel-connected SiC DUTs.

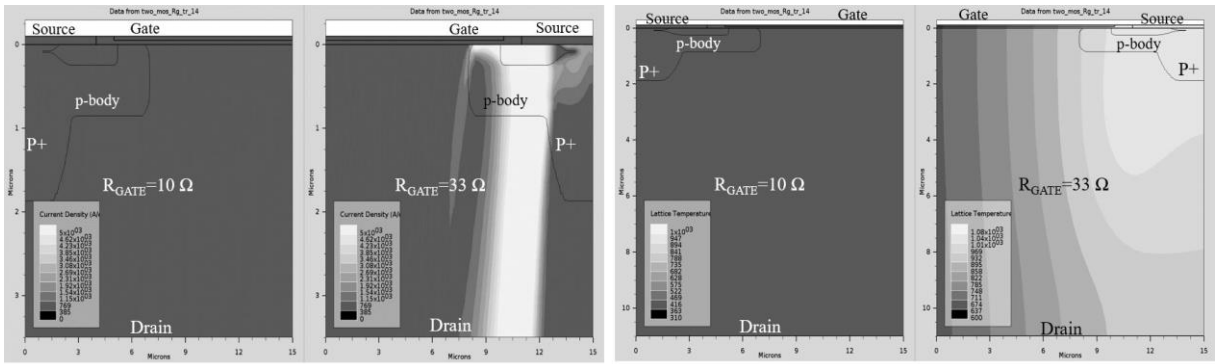


(c) Simulated 2D Avalanche Current Density (d) Simulated 2D Temperature Plot

Figure 5.29: The simulated 2-D (c) current density and (d) lattice temperature contour plots for the parallel-connected devices with different switching rates at point Y corresponding to Figure 5.28(a).

It can be seen in Figure 5.29(c) that the slower switching DUT on the RHS exhibits a considerably high current density through the NPN BJT as well as through the body diode. Because the device switches slower, the channel is still conductive at the point that the avalanche current starts to flow, hence, the significant current density through the p-body under the source. The faster switching device with the lower gate resistance conducts the avalanche current normally through the antiparallel body diode. As a result, the simulated SiC MOSFET DUT with larger gate resistance has a higher junction temperature because it conducts the bulk of the avalanche current as shown in Figure 5.29(d).

Figure 5.29(e) shows the 2-D current density contour plots at point Z corresponding to Figure 5.28(a) where full BJT latch-up is evident in the slower switching device (on the RHS) with the higher gate resistance. The faster switching device does not conduct any current since thermal runaway in the slower switching device has diverted the entire avalanche current away. This leads to a much higher internal device temperature in the DUT with the smaller gate resistance which is shown in Figure 5.29(f). These simulations correspond to and very well explain the experimental measurements presented in Figure 5.22 where the slower switching device failed during the UIS test.



(e) Simulated 2D Avalanche Current Density (f) Simulated 2D Temperature Plot

Figure 5.29: The simulated 2-D (e) current density and (f) lattice temperature contour plots for the parallel-connected devices with different switching rates at point Z corresponding to Figure 5.21(a).

Similar simulations are shown in Figure 5.30 for the CoolMOS devices switched with different gate resistances where Figure 5.30(a) shows the avalanche current characteristics and Figure 5.30(b) shows the drain voltage characteristic during avalanche mode conduction. Figure 5.30(c) shows the transient peak temperature within the DUTs during charging and avalanche while Figure 5.30(d) shows the avalanche power transient. It can be seen in Figure 5.30(a) that the slower switching simulated CoolMOS device undergoes BJT latch-up with significantly higher peak avalanche current.

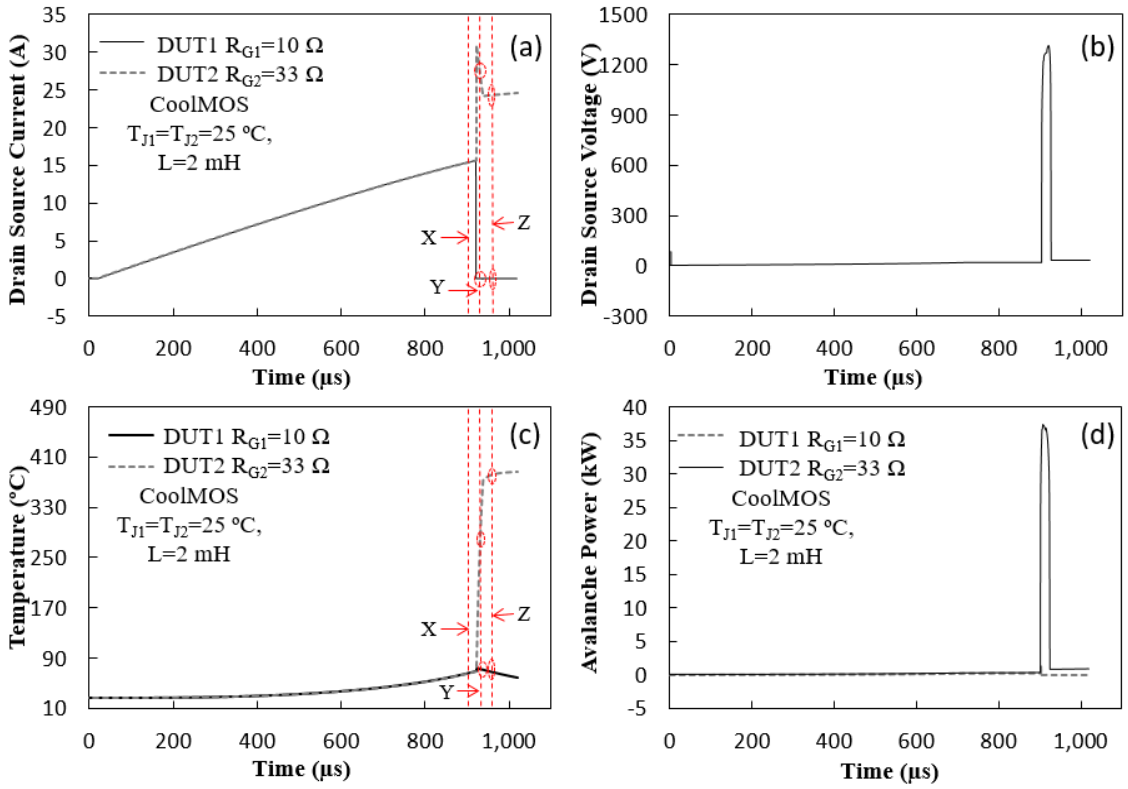
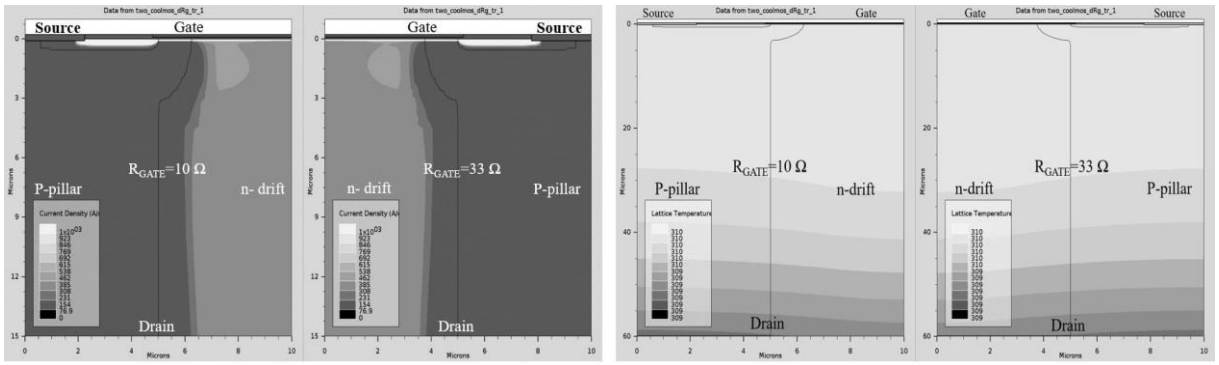


Figure 5.30: The (a) simulated avalanche current (b) drain voltage (c) Temperature and (d) dissipated power for the parallel connected CoolMOS devices switched with different gate resistance.

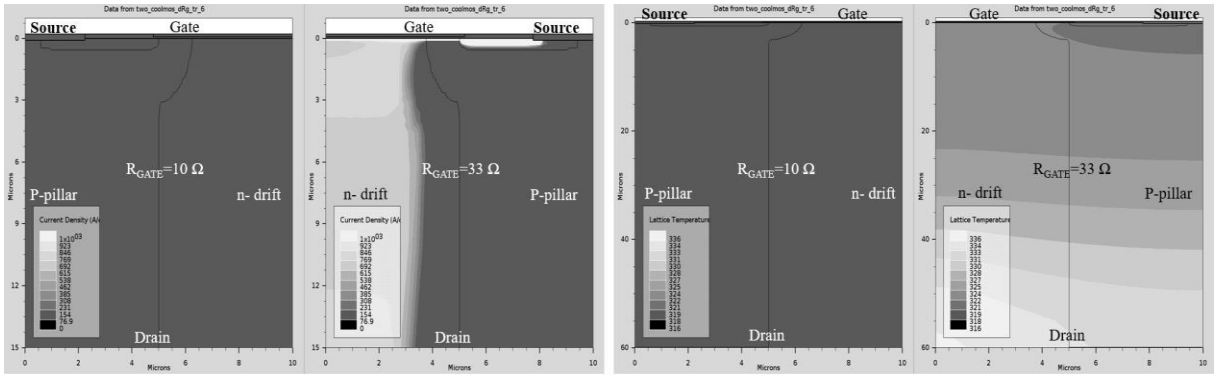
Figure 5.31(a) shows the 2D current density contour plots at point X (conduction mode) while Figure 5.31(b) shows the corresponding simulated lattice temperature at the same point. The DUTs are identical in terms of current and temperature distribution since the CoolMOS DUTs are in steady-state. Figure 5.31(c) and 5.31(d) show the 2D current

density and lattice temperature contour plots at point Y (avalanche mode) where the slower switching CoolMOS DUT on the RHS is in BJT latch-up. The faster switching simulated CoolMOS DUT on the LHS is turned OFF with no current flowing through it.



(a) Simulated 2D Avalanche Current Density (b) Simulated 2D Temperature Plot

Figure 5.31: The simulated (a) 2-D current density and (b) lattice temperature contour plots of the parallel connected CoolMOS with different gate resistances under UIS. This corresponds to point X in Figure 5.30 where the DUTs are under normal conduction mode.

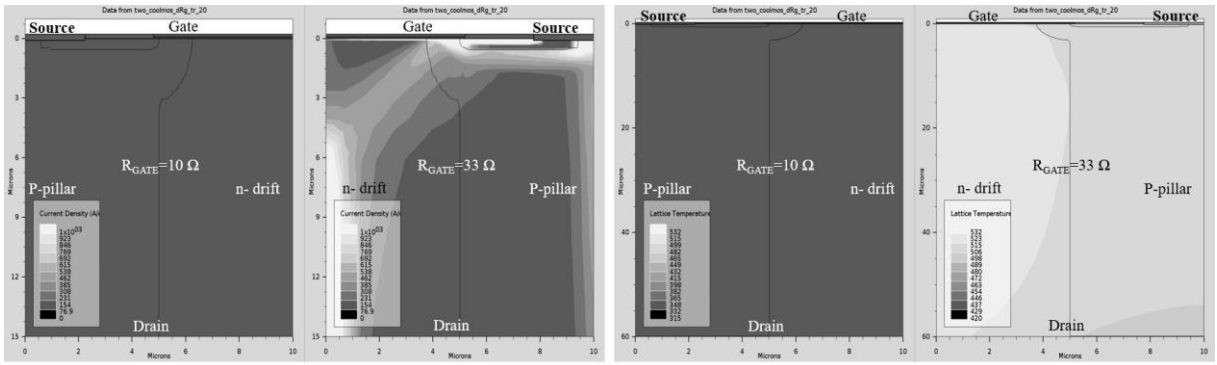


(c) Simulated 2D Avalanche Current Density (d) Simulated 2D Temperature Plot

Figure 5.31: The simulated (c) 2-D current density and (d) lattice temperature contour plots for parallel connected CoolMOS with different gate resistances under UIS. This corresponds to point Y in Figure 5.30 where the DUTs are in avalanche mode conduction.

Figure 5.31(e) and 5.31(f) shows the simulated 2D current density and lattice temperature contour plots corresponding to point Z in Figure 5.30 where the slower switching CoolMOS DUT is in full BJT latch-up and the faster switching DUT on the LHS is fully turned OFF. The CoolMOS devices exhibit different latch-up characteristics than the SiC MOSFETs. By comparing Figure 5.29(e) to Figure 5.31(e), it can be seen

that under BJT latch-up, the CoolMOS device exhibits more lateral currents due to presence of the p-pillar in the drift region. Figure 5.31(f) shows the 2D lattice temperature plot where it can be seen that the slower switching CoolMOS DUT on the RHS exhibits higher temperature compared to the DUT on the LHS.



(e) Simulated 2D Avalanche Current Density (f) Simulated 2D Temperature Plot

Figure 5.31: The simulated (e) 2-D current density and (f) lattice temperature plots for the parallel connected CoolMOS with different gate resistances under UIS. This corresponds to point Z in Figure 5.30 where the slower switching DUT fails under BJT latch-up.

5.10 Conclusions

In this chapter, both experimental measurements and simulations have been used to reach the following conclusions about parallel-connected SiC MOSFETs and parallel connected CoolMOS devices conducting under avalanche mode conditions in UIS

i) Both CoolMOS devices and SiC MOSFETs can dissipate higher avalanche energies in the form of lower avalanche power densities over longer avalanche durations compared to higher peak avalanche currents over shorter durations.

ii) Differences in the initial junction temperature reduce the overall maximum avalanche energy the combined devices can conduct without failure in either technology. A junction temperature difference of 85°C between the parallel-connected SiC MOSFETs causes the maximum sustainable avalanche current to

reduce by 10% while a gate resistance difference of 90 Ω causes the maximum sustainable avalanche current to reduce by 14%. On the other hand, same junction temperature difference between parallel-connected CoolMOS devices reduces the maximum sustainable avalanche current by 37% while same gate resistance difference reduces the maximum sustainable avalanche current by 75%. In other words, parallel-connected SiC MOSFETs are more electro-thermally rugged under mismatched conditions and can cope with electro-thermal variations better than parallel-connected CoolMOS DUTs.

iii) For parallel SiC MOSFETs and CoolMOS devices, the device with the lower initial junction temperature fails under UIS while the device with the higher initial junction temperature does not. This is primarily due to the positive temperature coefficient of the breakdown voltage, which ensures that the avalanche current flows through the initially cooler DUT. The fast nature of the avalanche power transient (a few microseconds) ensures that the initially cooler DUT reaches it electro-thermal limit and thus undergoes thermal runaway via BJT latch-up before the heat can flow out to the case.

iv) For parallel SiC MOSFETs and CoolMOS devices, the device switching with the higher gate resistance (lower dI_{DS}/dt) fails because the channel is more conductive during UIS compared to the device switching with the lower gate resistance (higher dI_{DS}/dt). Similarly, the fast nature of the avalanche transient ensures that there is insufficient time for heat-flow to reduce the junction temperature.

v) The impact of different junction temperatures and switching rates on the overall avalanche ruggedness of the parallel-connected devices is less effective when the avalanche energy is dissipated in the form of a lower power density over a longer avalanche duration. In other words, electro-thermal mismatch between the parallel-

connected DUTs is less critical as the power density of the UIS pulse reduces. Again, parallel-connected SiC MOSFETs exhibit better electro-thermal ruggedness over the entire range of avalanche durations compared to parallel-connected CoolMOS devices.

5.11 Implications for Power Electronic Applications

The reliability of power devices under unclamped inductive switching is a very important consideration in the design of power converters. The results in this chapter are important for such industrial applications where the power devices may undergo such stressful mission profiles. Since degradation of the power devices will not occur uniformly between the parallel devices, it is important to understand how degradation in single devices affects the ruggedness of the parallel combination. This analysis helps to understand single event failures that result from excessive electrothermal stresses and can assist in developing a reliability user manual for the devices. Applications include power dense high voltage automotive systems of the future where power devices may be used in different converter configurations.

Chapter 6.

CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

This thesis has used finite element simulations in conjunction with experimental measurements to investigate the electrothermal performance of single and parallel connected power devices. Systematic investigations of clamped and unclamped inductive switching was performed on silicon and SiC power devices. In the analysis of power diodes, clamped inductive switching tests showed that although PiN diodes exhibit lower junction/case temperatures than SiC Schottky diodes for a given switching frequency, duty cycle and switching rate, however, the complimenting transistor exhibits a higher junction/case temperature i.e. the electrothermal stress is transferred from the diode to the complimenting transistor. It was also shown that SiC Schottky diodes exhibit more stable operation under electrothermal imbalance when connected in parallel compared with PiN diodes. The higher ZTC point in silicon PiN diodes typically results in lower junction/case temperatures under repetitive switching conditions compared with SiC Schottky diodes.

However, the reverse recovery characteristics causes higher switching losses, hence, higher junction temperatures, in the low side driving transistor. The positive temperature coefficient of the PiN diode's current conductivity causes thermal instability as evidenced through the diverging case temperatures between the parallel connected devices. This is not the case with the Schottky diodes where converging temperature characteristics in the parallel connected diodes is evident. Despite the fact that SiC Schottky diodes have a lower current rating, it has been shown that the SiC Schottky diode is more electrothermally rugged under UIS conditions and can withstand higher temperature surges. It has been shown that the cooler PiN diode fails for the parallel connected PiN pairs while the hotter SiC Schottky diode fails for the parallel connected SiC Schottky pairs. Finite element modelling has matched with the experiment and it has been shown that the avalanche current is higher density beneath the terminal edge, and the SiC Schottky diode shows the same behaviour.

In the investigations of parallel transistors under clamped inductive switching, this thesis has demonstrated the impact of electrothermal unbalance in parallel connected devices for three different technologies: CoolMOS, SiC MOSFET and PT IGBT. The SiC MOSFETs are more resilient to electrothermal imbalance than CoolMOS device. Given the same variations in switching rates and thermal resistance (junction temperature), SiC MOSFETs will exhibit less variations in the switching energy, steady state operating temperatures and output characteristics. On the other hand, the parallel connected IGBT with electrothermal variations between the DUTs has been demonstrated, due to the zero temperature coefficient located within the operation temperature range, the two opposite part of temperature coefficient of on-state resistance leads to that PT IGBT devices can operate in parallel-connection without easy goes into thermal runaway.

This thesis also used experimental measurements and simulations to reach the following conclusions about parallel-connected SiC MOSFETs and parallel connected CoolMOS devices conducting in avalanche mode conduction under UIS

i) Both CoolMOS devices and SiC MOSFETs can dissipate higher avalanche energies in the form of lower avalanche power densities over longer avalanche durations compared to higher peak avalanche currents over shorter durations.

ii) Differences in the initial junction temperature reduce the overall maximum avalanche energy the combined devices can conduct without failure in either technology. A junction temperature difference of 85°C between the parallel-connected SiC MOSFETs causes the maximum sustainable avalanche current to reduce by 10% while a gate resistance difference of 90 Ω causes the maximum sustainable avalanche current to reduce by 14%. On the other hand, same junction temperature difference between parallel-connected CoolMOS devices reduces the maximum sustainable avalanche current by 37% while same gate resistance difference reduces the maximum sustainable avalanche current by 75%. In other words, parallel-connected SiC MOSFETs are more electro-thermally rugged under mismatched conditions and can cope with electro-thermal variations better than parallel-connected CoolMOS DUTs.

iii) For parallel SiC MOSFETs and CoolMOS devices, the device with the lower initial junction temperature fails under UIS while the device with the higher initial junction temperature does not. This is primarily due to the positive temperature coefficient of the breakdown voltage, which ensures that the avalanche current flows through the initially cooler DUT. The fast nature of the avalanche power transient (a few microseconds) ensures that the initially cooler DUT reaches it

electro-thermal limit and thus undergoes thermal runaway via BJT latch-up before the heat can flow out to the case.

iv) For parallel SiC MOSFETs and CoolMOS devices, the device switching with the higher gate resistance (lower dI_{DS}/dt) fails because the channel is more conductive during UIS compared to the device switching with the lower gate resistance (higher dI_{DS}/dt). Similarly, the fast nature of the avalanche transient ensures that there is insufficient time for heat-flow to reduce the junction temperature.

v) The impact of different junction temperatures and switching rates on the overall avalanche ruggedness of the parallel-connected devices is less effective when the avalanche energy is dissipated in the form of a lower power density over a longer avalanche duration. In other words, electro-thermal mismatch between the parallel-connected DUTs is less critical as the power density of the UIS pulse reduces. Again, parallel-connected SiC MOSFETs exhibit better electrothermal ruggedness over the entire range of avalanche durations compared to parallel-connected CoolMOS devices.

6.2 Implications of the Thesis Findings for The Industrial Applications of Power Electronic Devices

This thesis has systematically investigated the impact of variations in the switching transients of parallel-connected SiC Schottky diodes and SiC MOSFETs. This has been benchmarked against comparatively rated contemporary power semiconductor technologies like CoolMOS devices and silicon IGBTs. The electrothermal variation was introduced in the form of varied switching rates, varied case temperatures and varied case to ambient thermal resistances. The test conditions of the set-up were varied between mild

and high imbalance in order to investigate the linearity between imbalance in the input variables (switching rate, case temperature and thermal resistances) and the out variables for all technologies (switching energy and junction temperature). Case temperature variation of between 50 °C and 100 °C can occur between parallel-connected devices under different aging conditions i.e. parallel-connected MOSFETs/diodes with different degrees of solder voiding and die attach degradation [112, 158, 159]. Hence, the variation in junction temperature explored by the thesis is realistic since aged modules can easily exhibit such internal variation between the parallel devices. Switching rate variation between 40 and 200 A/µs corresponding to effective gate drive resistances between 10 and 90 Ω can easily occur as a result of varying degrees of increased gate contact resistance resulting from wire-bond lift-off [160]. Hence, the range of gate resistance variation has been selected to investigate the impact of non-uniform aging of the gate bond-wire contact in parallel-connected power devices.

The findings are relevant because future industrial applications of power devices will rely on increasingly high current ratings of power modules. In the case of SiC power MOSFETs, the paralleling considerations are even more critical since the current rating of the individual MOSFETs are lower, hence, more parallel-connected devices are required. Figure 6.1 shows a CREE 1.2 kV/150 A half bridge power module implemented by 5 parallel SiC MOSFETs and Schottky diodes. Figure 6.2 shows a similarly rated Si-IGBT half-bridge power module implemented using a single 150 A rated IGBT and PiN diode for each switching cell. It is plain to see that paralleling and electrothermal imbalance from variations of critical parameters is more important for SiC power modules than silicon power modules.

Future medium voltage multi-MW electric drivetrains will demand higher current ratings, hence, module design to ensure synchronised switching of power MOSFETs and

diodes will become even more important in the future. Also, the impact of non-uniform aging between the parallel-connected MOSFET and diodes on the electrothermal ruggedness and reliability is equally important.

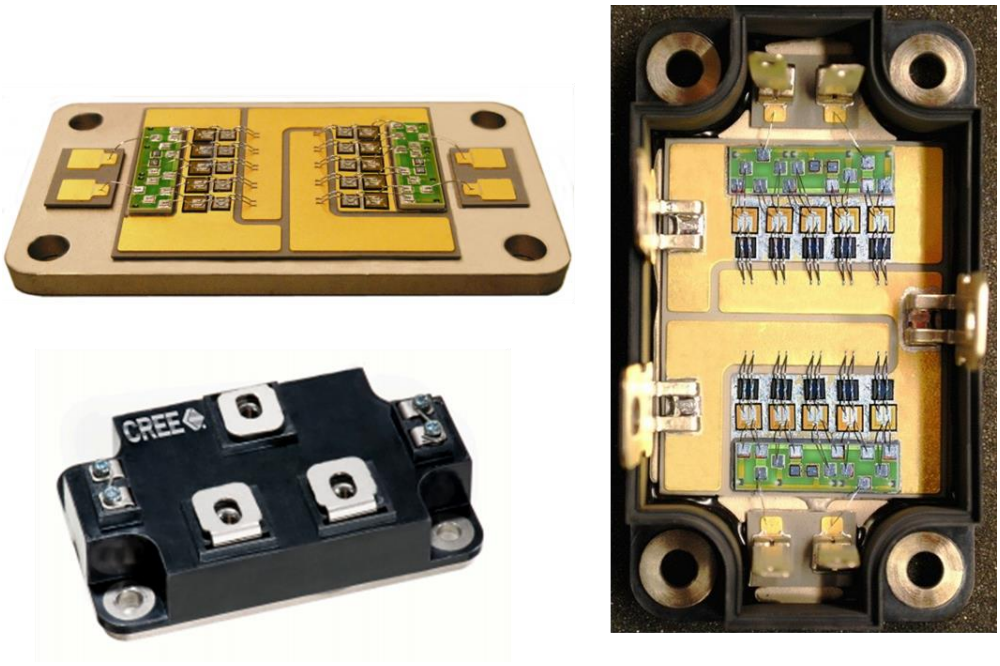


Figure 6.1: 1.2 kV/150 A CREE half-bride Power Module implemented in SiC power MOSFETs and Schottky Barrier Diodes.

Figure 6.2: 1.2 kV/150 A Fairchild half-bride Power Module implemented in a silicon IGBT and PiN diode for each switching cell.

The thesis findings can be applied in industrial applications in the following ways

a) **Design of Snubber-less Power Converters**: Currently, in some applications, output snubbers are used to ensure uniform and balanced switching between all parallel-connected and series-connected power modules. Output snubbers are costly, bulky and difficult to implement in applications where weight and volume is critical for delivering high power densities. Hence, snubber-less design of power converters is an active research topic. In the design of such power converters, the results in Chapters 3 and 4 can be used for to ascertain the required tolerances for the design of the gate drivers required for highly synchronised electrical switching. In such converters, the ability of the converter to operate seamlessly under electrothermal imbalance between the switching devices is important, hence, the dependency of the junction temperature imbalance on the imbalance of switching rate and thermal resistance is an important contribution of the thesis.

b) **Reliability Estimation for Converter Power Modules**: Currently, power converter modules are known to be implemented as multi-die designs. From physical inspection of the 1.2 kV/150 A SiC module shown in Figure 6.1, it can be seen that gate path for the 5 devices are not symmetrical. As the module ages under thermos-mechanical stress cycling, the variation in the electrical gate resistance will increase due to varying degrees of increased gate bond-wire contact resistance. This is a well-known failure mechanism in power modules [161]. Furthermore, differences in the heat-flow path between the parallel MOSFETs/diodes will increase with the aging of the module. Die attach delamination, solder voiding and thermal resistance degradation are very well-known reliability issues for power modules [112]. Hence, the findings in chapters 3 and 5 can be used to ascertain the impact of aging on the electro-thermal ruggedness under UIS. In general, although

SiC modules will have more parallel devices, the electrothermal properties of the WBG material ensures that the module is better capable of handling imbalance compared to silicon. Module designers can use the results together with the mission profile of the intended application to reliability predict the reliability of multi-chip power modules.

c) **Maximisation of Power Density**: Maximising power density usually involves switching with the highest possible PWM carrier frequency so as to reduce the size and volume of the output filters required for harmonic management. When each switching cell is comprised of several connected power devices as shown in Figure 6.1 for the SiC MOSFET power module, the impact of electrothermal imbalance is aggravated since the switching losses and average junction temperature will be higher as the switching frequency is increased. This will have significant implications for the reliability of the module. The trade-off analysis between power density and reliability will derive benefit from the results of chapters 3, 4 and 5. The contributions of these results provide module designers with more understanding of how imbalance is aggravated between switching cells and how the degree of aggravation depends on the technology used.

6.3 Future Work

The experiments of electrothermal imbalance between parallel devices in this thesis was limited to 2 parallel devices, hence, the next step would be multiple devices i.e. greater than 2. This evaluation is more valuable for high current applications where multiple dies are used for high current ratings for example, the Infineon 1000A/1700V half bridge module consists of six identical smaller modules connected in parallel. A generalised

model for power device failure and switching energy/junction temperature mismatch can then be generated and applied to any arbitrary number of parallel devices. Since these studies are geared towards understanding the impact of electrothermal mismatch between parallel connected devices on the reliability of the power module, future work should focus on the use of condition monitoring of parallel devices. This will be useful in detecting junction temperature mismatch and coupled with signal processing and intelligent gate driving, can be a method of diagnosing the health of the module and ultimately predicting lifetime. Condition monitoring will usually involve the use of a temperature sensitive electrical parameter (TSEP) for ascertaining the junction temperature thereby gaining insight into the thermal resistance and health of the power module. The finite element modelling package will be useful in the understanding of the TSEP. Recently, hybrid structure devices such as reverse conducting IGBTs [140], merged PiN Schottky (MPS) diode [162], junction barrier Schottky (JBS) diode and the HUBFET [163-165] have been proposed. Investigating electrothermal imbalance between these devices and understanding how device ruggedness is impacted will also be important here.

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APPENDIX

V_{DS}	1200 V
$I_{D\ @\ 25°C}$	10 A
$R_{DS(on)}$	280 mΩ

C2M0280120D

Silicon Carbide Power MOSFET
C2M™ MOSFET Technology

N-Channel Enhancement Mode

Features

- New C2M SiC MOSFET technlogy
- High Blocking Voltage with Low On-Resistance
- High Speed Switching with Low Capacitances
- Easy to Parallel and Simple to Drive
- Avalanche Ruggedness
- Resistant to Latch-Up
- Halogen Free, RoHS Compliant

Benefits

- Higher System Efficiency
- Reduced Cooling Requirements
- Increased Power Density
- Increased System Switching Frequency

Applications

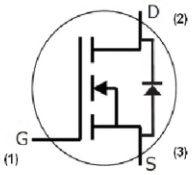
- LED Lighting Power Supplies
- High Voltage DC/DC Converters
- Industrial Power Supplies
- HVAC

Package

TO-247-3

Halogen-Free

RoHS



Part Number	Package
C2M0280120D	TO-247-3

Maximum Ratings (T_C = 25 °C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DSmax}	Drain - Source Voltage	1200	V	V_{GS} = 0 V, I_D = 100 µA	
V_{GSmax}	Gate - Source Voltage	-10/+25	V	Absolute maximum values	
V_{GSop}	Gate - Source Voltage	-5/+20	V	Recommended operational values	
I_D	Continuous Drain Current	10	A	V_{GS} = 20 V, T_C = 25 °C	Fig. 19
		6		V_{GS} = 20 V, T_C = 100 °C	
$I_{D(pulse)}$	Pulsed Drain Current	20	A	Pulse width t_P limited by T_{jmax}	Fig. 22
P_D	Power Dissipation	62.5	W	T_C=25 °C, T_J = 150 °C	Fig. 20
T_J , T_{stg}	Operating Junction and Storage Temperature	-55 to +150	°C		
T_L	Solder Temperature	260	°C	1.6 mm (0.063") from case for 10s	
M_d	Mounting Torque	1 8.8	Nm lbf-in	M3 or 6-32 screw	

Electrical Characteristics (T_C = 25°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	V_{GS} = 0 V, I_D = 100 µA	
$V_{GS(th)}$	Gate Threshold Voltage	2.4	2.8		V	V_{DS} = 10 V, I_D = 1.25mA	Fig. 11
		1.8	2.1		V	V_{DS} = 10 V, I_D = 1.25mA, T_J = 150 °C	
I_{DSS}	Zero Gate Voltage Drain Current		1	100	µA	V_{DS} = 1200 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current			250	nA	V_{GS} = 20 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance		280	370	mΩ	V_{GS} = 20 V, I_D = 6 A	Fig. 4,5,6
			530			V_{GS} = 20 V, I_D = 6 A, T_J = 150 °C	
g_{fs}	Transconductance		2.8		S	V_{DS}= 20 V, I_{DS}= 6 A	Fig. 7
			2.4			V_{DS}= 20 V, I_{DS}= 6 A, T_J = 150 °C	
C_{iss}	Input Capacitance		259		pF	V_{GS} = 0 V V_{DS} = 1000 V f = 1 MHz V_{AC} = 25 mV	Fig. 17,18
C_{oss}	Output Capacitance		23				
C_{rss}	Reverse Transfer Capacitance		3				
E_{oss}	C_{oss} Stored Energy		12.5		µJ		Fig 16
E_{AS}	Avalanche Energy, Single Pluse		280		mJ	I_D = 6A, V_{DD} = 50V	Fig. 29
E_{ON}	Turn-On Switching Energy		32		µJ	V_{DS} = 800 V, V_{GS} = -5/20 V, I_D = 6A, $R_{G(ext)}$ = 2.5Ω, L= 412 µH	Fig. 25
E_{OFF}	Turn Off Switching Energy		37				
$t_{d(on)}$	Turn-On Delay Time		5.2		ns	V_{DD} = 800 V, V_{GS} = -5/20 V I_D = 6 A, $R_{G(ext)}$ = 2.5 Ω, R_L = 133 Ω Timing relative to V_{DS} Per IEC60747-8-4 pg 83	Fig. 27
t_r	Rise Time		7.6				
$t_{d(off)}$	Turn-Off Delay Time		10.8				
t_f	Fall Time		9.9				
$R_{G(int)}$	Internal Gate Resistance		11.4		Ω	f = 1 MHz, V_{AC} = 25 mV, ESR of C_{iss}	
Q_{gs}	Gate to Source Charge		5.6		nC	V_{DS} = 800 V, V_{GS} = -5/20 V I_D = 6 A Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		7.6				
Q_g	Gate Charge Total		20.4				

Reverse Diode Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	3.3		V	V_{GS} = - 5 V, I_{SD} = 3 A	Fig. 8, 9, 10
		3.1		V	V_{GS} = - 5 V, I_{SD} = 3 A, T_J = 150 °C	
I_S	Continuous Diode Forward Current		10	A	T_C = 25°C	Note 1
t_{rr}	Reverse Recovery time	24		ns	V_{GS} = - 5 V, I_{SD} = 6 A, V_R = 800 V dif/dt = 1000 A/µs	Note 1
Q_{rr}	Reverse Recovery Charge	70		nC		
I_{rrm}	Peak Reverse Recovery Current	4		A		

Note (1): When using SiC Body Diode the maximum recommended V_{GS} = -5V

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	1.8	2.0	°C/W		Fig. 21
$R_{\theta JC}$	Thermal Resistance from Junction to Ambient		40			

Typical Performance

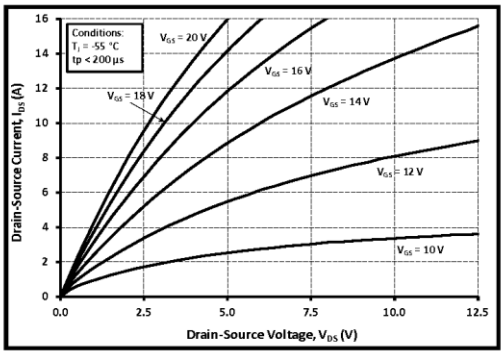


Figure 1. Output Characteristics T_J = -55 °C

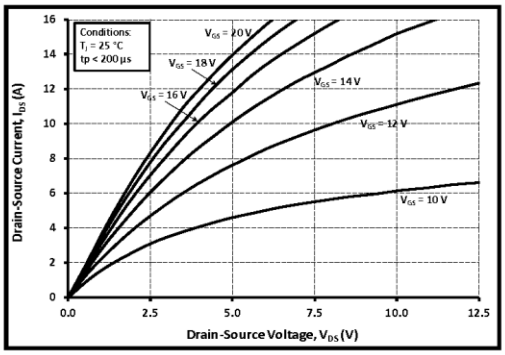


Figure 2. Output Characteristics T_J = 25 °C

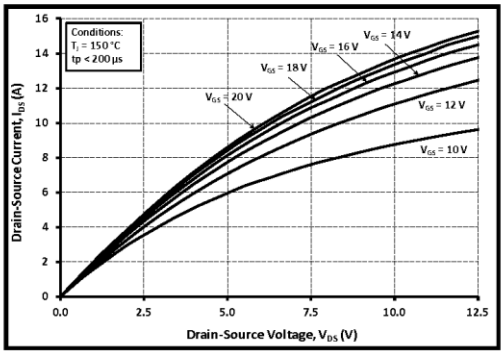


Figure 3. Output Characteristics T_J = 150 °C

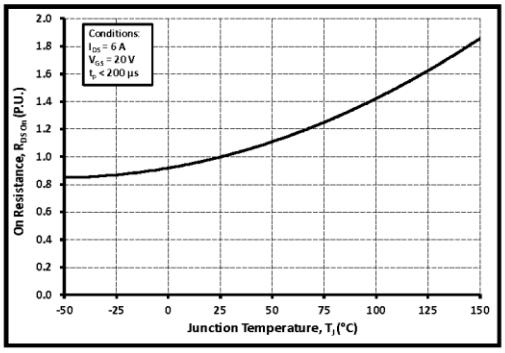


Figure 4. Normalized On-Resistance vs. Temperature

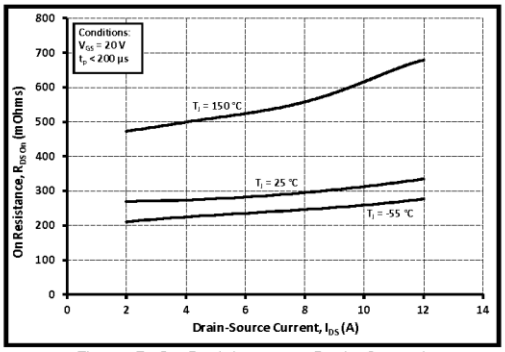


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

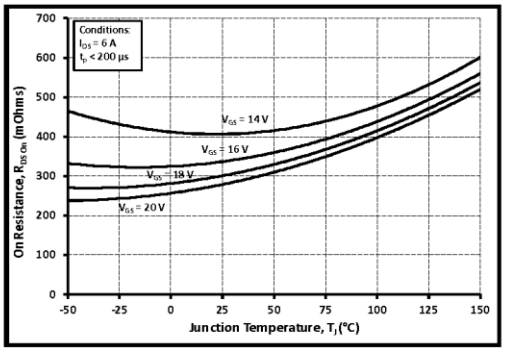
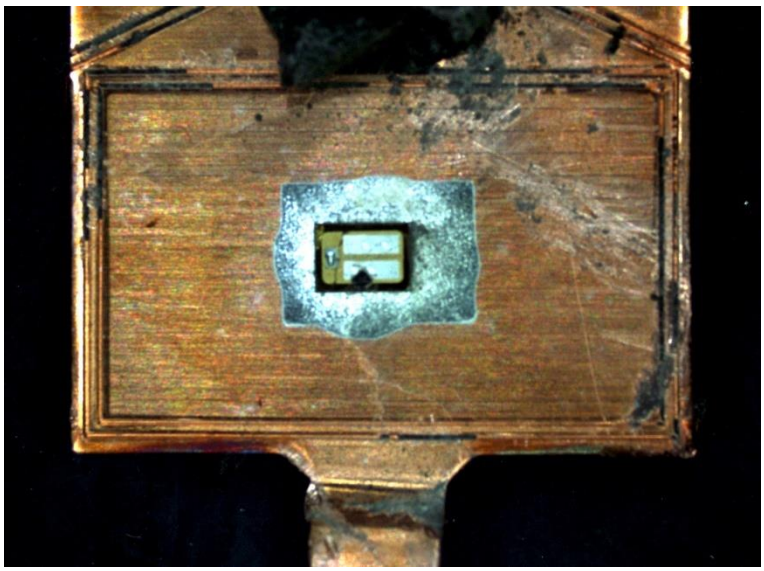
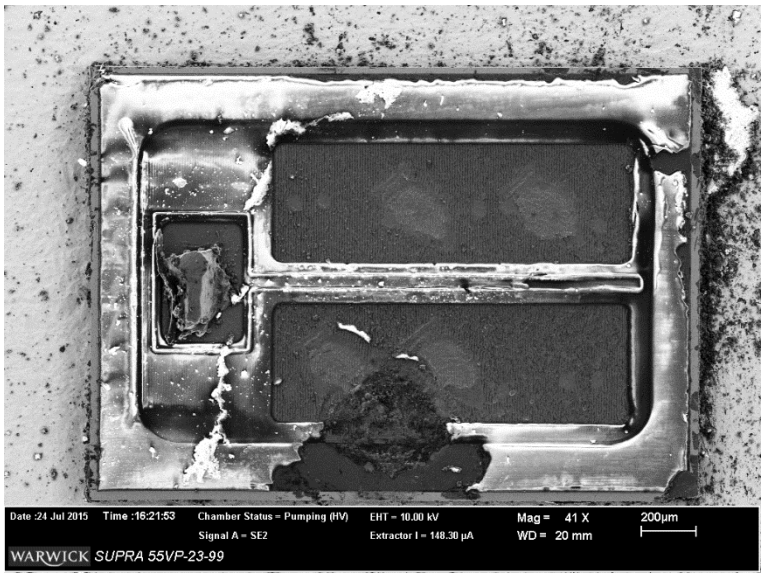


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage





C2M0280120D 10 A/1200 V SiC MOSFET, the die area is 2.2 mm ×1.5 mm

CoolMOS™ Power Transistor

Features

- Lowest figure-of-merit $R_{ON} \times Q_g$
- Extreme dv/dt rated
- High peak current capability
- Qualified for industrial grade applications according to JEDEC[1)]
- Pb-free lead plating; RoHS compliant
- Ultra low gate charge

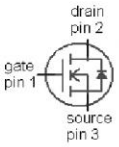
Product Summary

V_{DS} @ T_J = 25°C	900	V
$R_{DS(on),max}$ @ T_J=25°C	0.34	Ω
$Q_{g,typ}$	94	nC

PG-TO247

CoolMOS™ 900V is designed for:

- Quasi Resonant Flyback / Forward topologies
- PC Silverbox and consumer applications
- Industrial SMPS



Type	Package	Marking
IPW90R340C3	PG-TO247	9R340C

Maximum ratings, at T_J=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C	15	A
		T_C=100 °C	9.5	
Pulsed drain current [2)]	$I_{D,pulse}$	T_C=25 °C	34	
Avalanche energy, single pulse	E_{AS}	I_D=3.1 A, V_{DD}=50 V	678	mJ
Avalanche energy, repetitive t_{AR}[2),3)]	E_{AR}	I_D=3.1 A, V_{DD}=50 V	1	
Avalanche current, repetitive t_{AR}[2),3)]	I_{AR}		3.1	A
MOSFET dv/dt ruggedness	dv/dt	V_{DS}=0...400 V	50	V/ns
Gate source voltage	V_{GS}	static	±20	V
		AC (f>1 Hz)	±30	
Power dissipation	P_{tot}	T_C=25 °C	208	W
Operating and storage temperature	T_J, T_{stg}		-55 ... 150	°C
Mounting torque		M3 and M3.5 screws	60	Ncm

Please note the new package dimensions arccording to PCN 2009-134-A

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous diode forward current	I_S	T_C=25 °C	9.2	A
Diode pulse current [2]	$I_{S,pulse}$		34	
Reverse diode dv/dt [4]	dv/dt		4	V/ns

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	0.6	K/W
Thermal resistance, junction - ambient	R_{thJA}	leaded	-	-	62	
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	1.6 mm (0.063 in.) from case for 10 s	-	-	260	°C
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=250 µA	900	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=1 mA	2.5	3	3.5	
Zero gate voltage drain current	I_{DSS}	V_{DS}=900 V, V_{GS}=0 V, T_j=25 °C	-	-	2	µA
		V_{DS}=900 V, V_{GS}=0 V, T_j=150 °C	-	20	-	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=9.2 A, T_j=25 °C	-	0.28	0.34	Ω
		V_{GS}=10 V, I_D=9.2 A, T_j=150 °C	-	0.76	-	
Gate resistance	R_G	f=1 MHz, open drain	-	1.3	-	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz	-	2400	-	pF
Output capacitance	C_{oss}		-	120	-	
Effective output capacitance, energy related [5]	$C_{o(er)}$	V_{GS}=0 V, V_{DS}=0 V to 500 V	-	71	-	
Effective output capacitance, time related [6]	$C_{o(tr)}$		-	280	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=400 V, V_{GS}=10 V, I_D=9.2A, R_G=23.1 Ω	-	70	-	ns
Rise time	t_r		-	20	-	
Turn-off delay time	$t_{d(off)}$		-	400	-	
Fall time	t_f		-	25	-	
Gate Charge Characteristics						
Gate to source charge	Q_{gs}	V_{DD}=400 V, I_D=9.2 A, V_{GS}=0 to 10 V	-	11	-	nC
Gate to drain charge	Q_{gd}		-	41	-	
Gate charge total	Q_g		-	94	tbd	
Gate plateau voltage	$V_{plateau}$		-	4.6	-	V
Reverse Diode						
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=9.2 A, T_J=25 °C	-	0.8	1.2	V
Reverse recovery time	t_{rr}	V_R=400 V, I_F=I_S, di_F/dt=100 A/µs	-	510	-	ns
Reverse recovery charge	Q_{rr}		-	11	-	µC
Peak reverse recovery current	I_{rrm}		-	41	-	A

[1] J-STD20 and JESD22

[2] Pulse width t_p limited by $T_{J,max}$

[3] Repetitive avalanche causes additional power losses that can be calculated as P_{AV}=E_{AR}*f.

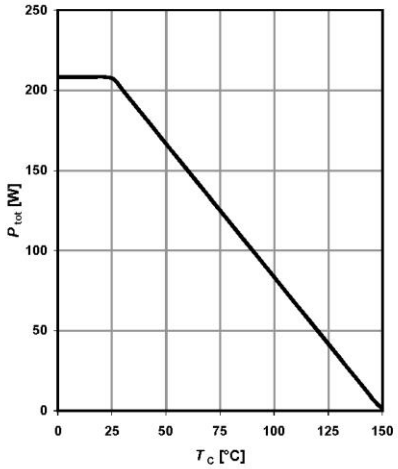
[4] I_{SD}≤I_D, di/dt≤200A/µs, V_{DClink}=400V, V_{peak}<$V_{(BR)DSS}$, T_J<$T_{J,max}$, identical low side and high side switch

[5] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 50% V_{DSS}.

[6] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 50% V_{DSS}.

1 Power dissipation

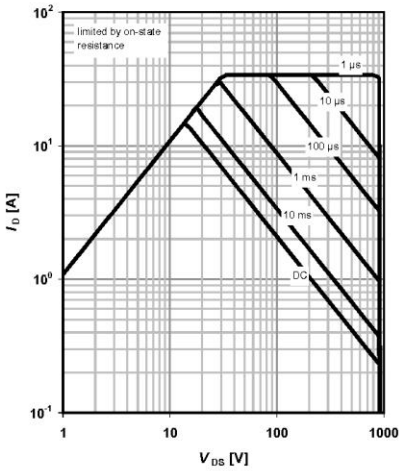
$P_{tot}=f(T_C)$



2 Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$

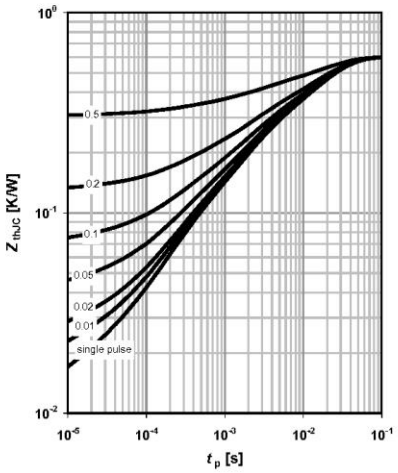
parameter: t_p



3 Max. transient thermal impedance

$Z_{thJC}=f(t_P)$

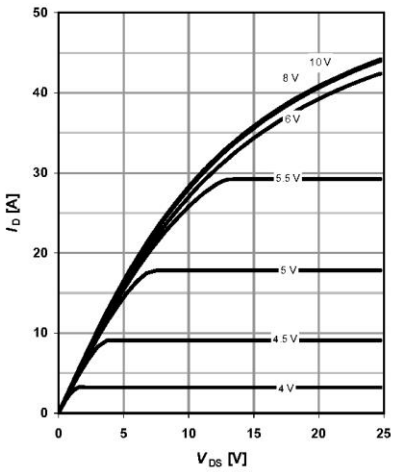
parameter: $D=t_p/T$



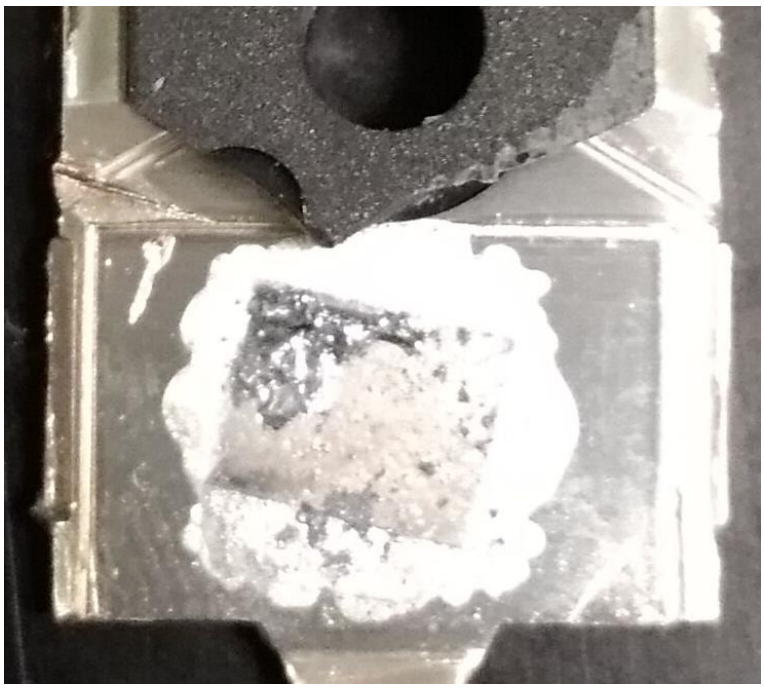
4 Typ. output characteristics

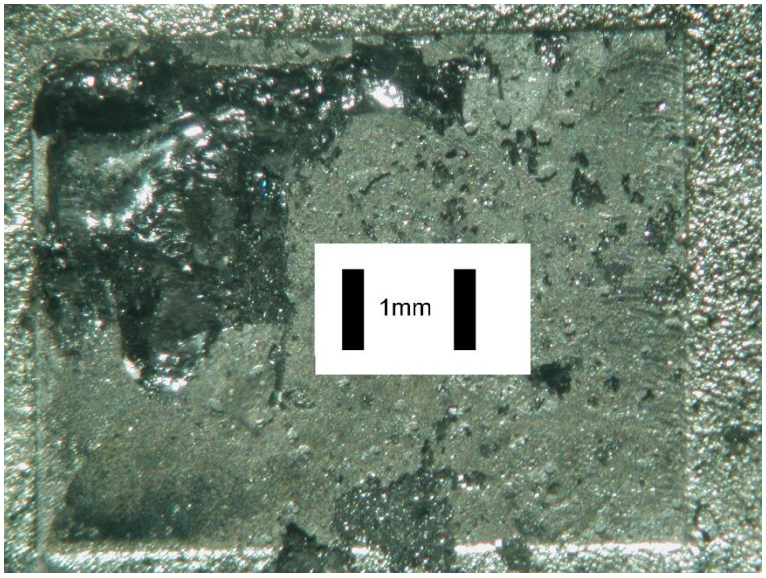
$I_D=f(V_{DS})$; $T_J=25$ °C

parameter: V_{GS}



Please note the new package dimensions arccording to PCN 2009-134-A





IPW90R340 15 A/900 V CoolMOS, The die area is 5.6 mm×4.5 mm

Bulletin PD-20749 rev. E 10/06

International
IOR Rectifier

15ETH06
15ETH06S
15ETH06-1

Hyperfast Rectifier

Features

- Hyperfastfast Recovery Time
- Low Forward Voltage Drop
- Low Leakage Current
- 175°C Operating Junction Temperature
- Single Die Center Tap Module

t_{rr} = 22ns typ.
$I_{F(AV)}$ = 15Amp
V_R = 600V

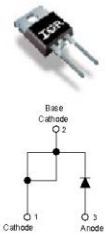
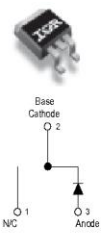
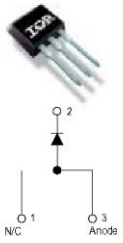
Description/ Applications

State of the art Hyperfast recovery rectifiers designed with optimized performance of forward voltage drop, Hyperfast recover time, and soft recovery.
The planar structure and the platinum doped life time control guarantee the best overall performance, ruggedness and reliability characteristics.
These devices are intended for use in PFC Boost stage in the AC-DC section of SMPS, inverters or as freewheeling diodes.
The IR extremely optimized stored charge and low recovery current minimize the switching losses and reduce over dissipation in the switching element and snubbers.

Absolute Maximum Ratings

	Parameters		Max	Units
V_{RRM}	Peak Repetitive Peak Reverse Voltage		600	V
$I_{F(AV)}$	Average Rectified Forward Current	@ T_C = 140°C	15	A
I_{FSM}	Non Repetitive Peak Surge Current	@ T_J = 25°C	120	
I_{FM}	Peak Repetitive Forward Current		30	
T_J, T_{STG}	Operating Junction and Storage Temperatures		- 65 to 175	°C

Case Styles

15ETH06	15ETH06S	15ETH06-1
		
TO-220AC	D^2PAK	TO-262

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameters	Min	Typ	Max	Units	Test Conditions
V_{BR}, V_r	Breakdown Voltage, Blocking Voltage	600	-	-	V	I_R = 100µA
V_F	Forward Voltage	-	1.8	2.2	V	I_F = 15A, T_J = 25°C
		-	1.3	1.6	V	I_F = 15A, T_J = 150°C
I_R	Reverse Leakage Current	-	0.2	50	µA	V_R = V_R Rated
		-	30	500	µA	T_J = 150°C, V_R = V_R Rated
C_T	Junction Capacitance	-	20	-	pF	V_R = 600V
L_S	Series Inductance	-	8.0	-	nH	Measured lead to lead 5mm from package body

Dynamic Recovery Characteristics @ T_C = 25°C (unless otherwise specified)

	Parameters	Min	Typ	Max	Units	Test Conditions	
t_{rr}	Reverse Recovery Time	-	22	30	ns	I_F = 1A, di_F/dt = 100A/µs, V_R = 30V	
		-	28	35		I_F = 15A, di_F/dt = 100A/µs, V_R = 30V	
		-	29	-		T_J = 25°C	I_F = 15A di_F/dt = 200A/µs V_R = 390V
		-	75	-		T_J = 125°C	
I_{RRM}	Peak Recovery Current	-	3.5	-	A	T_J = 25°C	
		-	7	-		T_J = 125°C	
Q_{rr}	Reverse Recovery Charge	-	57	-	nC	T_J = 25°C	
		-	300	-		T_J = 125°C	
t_{rr}	Reverse Recovery Time	-	51	-	ns	T_J = 125°C	I_F = 15A di_F/dt = 800A/µs V_R = 390V
I_{RRM}	Peak Recovery Current	-	20	-	A		
Q_{rr}	Reverse Recovery Charge	-	580	-	nC		

Thermal - Mechanical Characteristics

	Parameters		Min	Typ	Max	Units
T_J	Max. Junction Temperature Range		-	-	175	°C
T_{Stg}	Max. Storage Temperature Range		- 65	-	175	
R_{thJC}	Thermal Resistance, Junction to Case	Per Leg	-	1.0	1.3	°C/W
R_{thJA} ①	Thermal Resistance, Junction to Ambient	Per Leg	-	-	70	
R_{thCS} ②	Thermal Resistance, Case to Heatsink		-	0.5	-	
	Weight		-	2.0	-	g
			-	0.07	-	(oz)
	Mounting Torque		6.0	-	12	Kg-cm
			5.0	-	10	lbf.in

① Typical Socket Mount
② Mounting Surface, Flat, Smooth and Greased

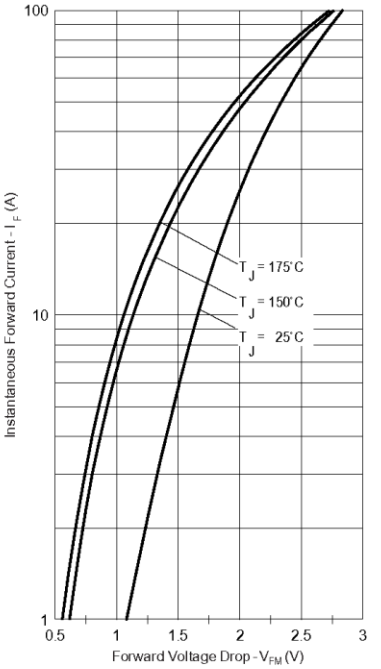


Fig. 1 - Typical Forward Voltage Drop Characteristics

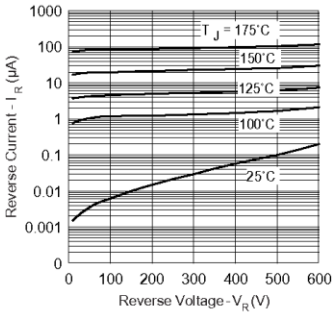


Fig. 2 - Typical Values Of Reverse Current Vs. Reverse Voltage

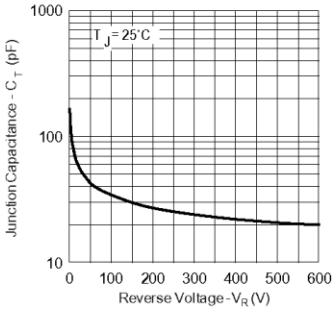


Fig. 3 - Typical Junction Capacitance Vs. Reverse Voltage

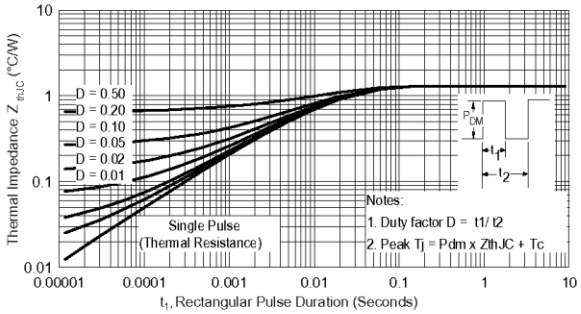
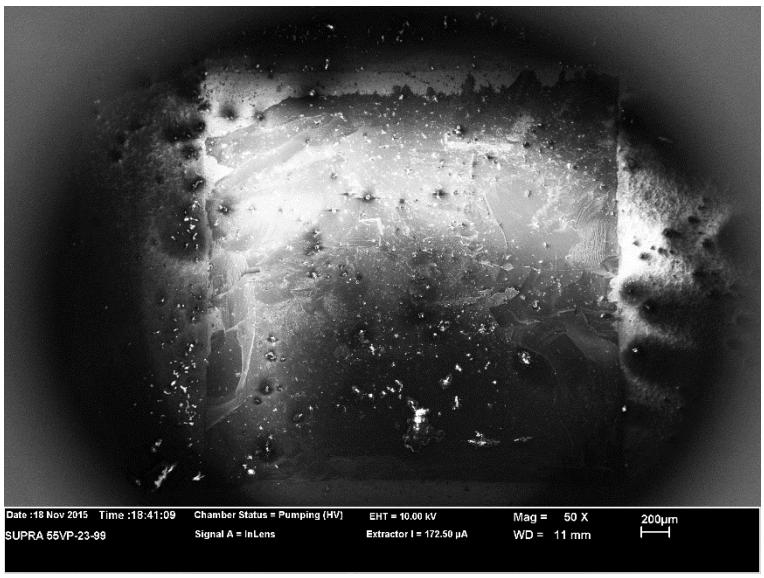


Fig. 4 - Max. Thermal Impedance Z_{thJC} Characteristics



15ETH06 15 A/600 V silicon PiN diode, the die area is 3.15 mm×3.15 mm

C3D06060A–Silicon Carbide Schottky Diode

Z-REC™ RECTIFIER

V_{RRM} = 600 V
$I_{F(AVG)}$ = 6 A
(T_C < 150°C)
Q_c = 16 nC

Features

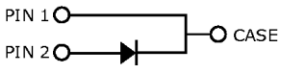
- 600-Volt Schottky Rectifier
- Zero Reverse Recovery Current
- Zero Forward Recovery Voltage
- High-Frequency Operation
- Temperature-Independent Switching Behavior
- Extremely Fast Switching
- Positive Temperature Coefficient on V_F

Package

TO-220-2

Benefits

- Replace Bipolar with Unipolar Rectifiers
- Essentially No Switching Losses
- Higher Efficiency
- Reduction of Heat Sink Requirements
- Parallel Devices Without Thermal Runaway



Applications

- Switch Mode Power Supplies
- Power Factor Correction
  - Typical PFC P_{out} : 600W-1200W
- Motor Drives
  - Typical Power : 2HP-3HP

Part Number	Package	Marking
C3D06060A	TO-220-2	C3D06060

Maximum Ratings

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{RRM}	Repetitive Peak Reverse Voltage	600	V		
V_{RSM}	Surge Peak Reverse Voltage	600	V		
V_{DC}	DC Blocking Voltage	600	V		
$I_{F(AVG)}$	Average Forward Current	6 8	A	T_C<150°C T_C<135°C	See Fig. 3
I_{FRM}	Repetitive Peak Forward Surge Current	41 27	A	T_C=25°C, t_p = 10 ms, Half Sine Wave, D=0.3 T_C=110°C, t_p=10 ms, Half Sine Wave, D=0.3	
I_{FSM}	Non-Repetitive Peak Forward Surge Current	70 55	A	T_C=25°C, t_p = 10 mS, Half Sine Wave, D=0.3 T_C=110°C, t_p = 10 mS, Half Sine Wave, D=0.3	
I_{FSM}	Non-Repetitive Peak Forward Surge Current	200	A	T_C=25°C, t_p = 10 µs, Pulse	
P_{tot}	Power Dissipation	79 34	W	T_C=25°C T_C=110°C	
T_J , T_{stg}	Operating Junction and Storage Temperature	-55 to +175	°C		
	TO-220 Mounting Torque	1 8.8	Nm lbf-in	M3 Screw 6-32 Screw	

Electrical Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_F	Forward Voltage	1.6 1.9	1.8 2.4	V	I_F = 6 A T_J=25°C I_F = 6 A T_J=175°C	
I_R	Reverse Current	10 20	50 200	μA	V_R = 600 V T_J=25°C V_R = 600 V T_J=175°C	
Q_C	Total Capacitive Charge	16		nC	V_R = 600 V, I_F = 6A di/dt = 500 A/μs T_J = 25°C	
C	Total Capacitance	294 27 26		pF	V_R = 0 V, T_J = 25°C, f = 1 MHz V_R = 200 V, T_J = 25°C, f = 1 MHz V_R = 400 V, T_J = 25°C, f = 1 MHz	

Note:
1. This is a majority carrier diode, so there is no reverse recovery charge.

Thermal Characteristics

Symbol	Parameter	Typ.	Unit
$R_{\theta JC}$	Thermal Resistance from Junction to Case	1.9	°C/W

Typical Performance

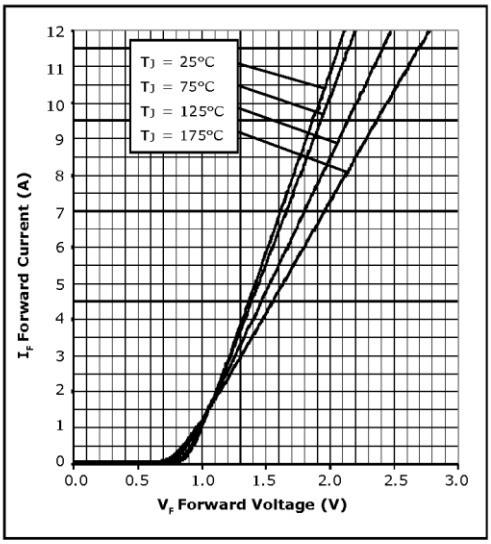


Figure 1. Forward Characteristics

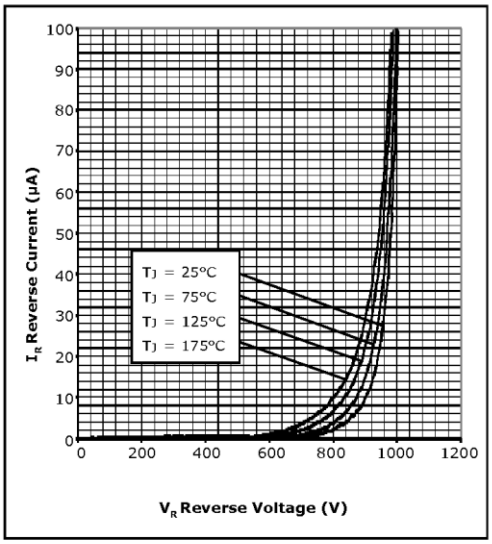


Figure 2. Reverse Characteristics

Typical Performance

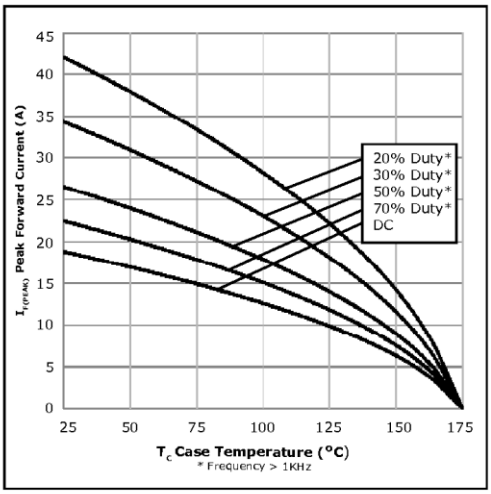


Figure 3. Current Derating

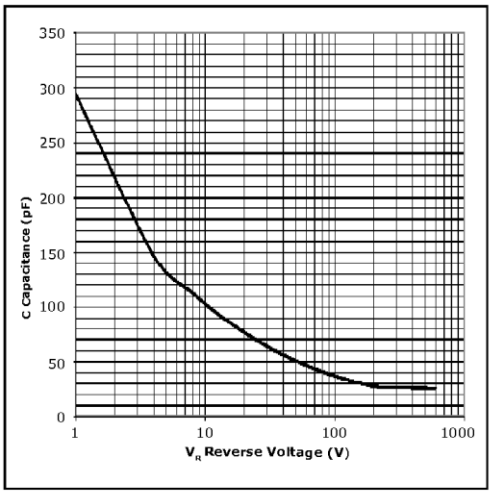


Figure 4. Capacitance vs. Reverse Voltage

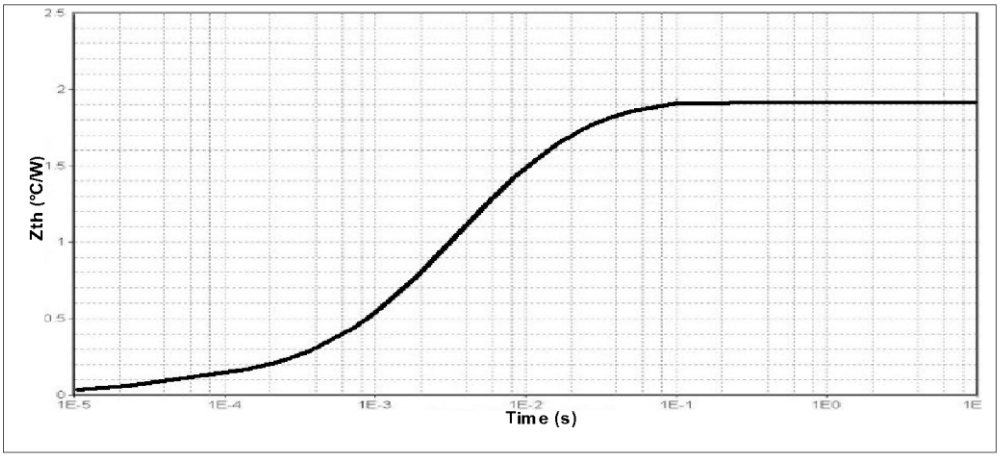
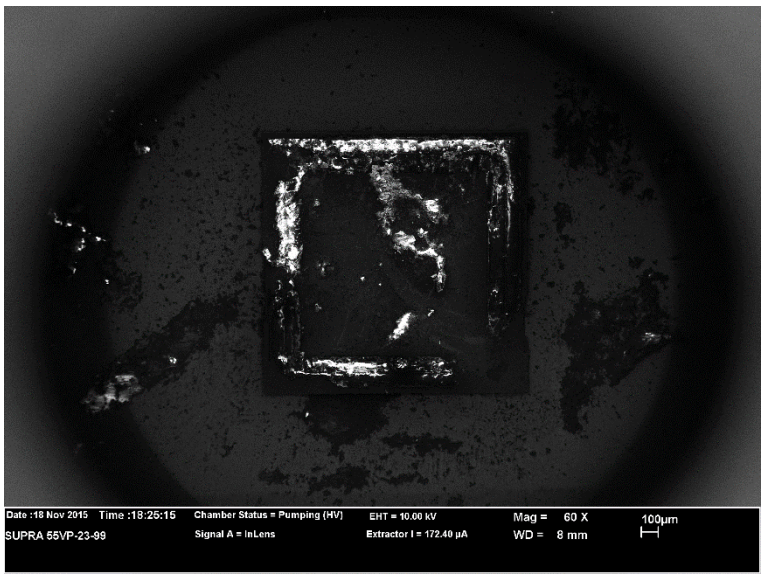


Figure 5. Transient Thermal Impedance



C3D06060A 9 A/ SiC Schottky diode, 1.6 mm×1.6 mm

Gate Driver Design

The schematic of the logic and gate driver circuit is represented in Figure g-1 below. (This is the schematic used for the calculations, for the final layout design, check the Figure g-3)

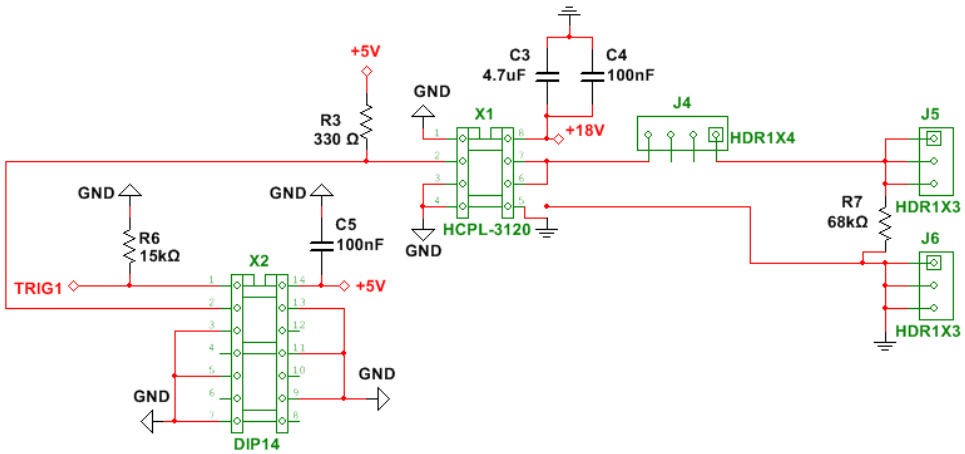


Figure g-1: Logic and gate driver circuit

The main element of the logic circuit is the IC X2. The IC selected is the open collector non-inverting buffer SN74ALS1035N. This circuit is used to bias the emitting LED of the gate driver with the suitable current value. This configuration is recommended in the manufacturer's data sheet in order to improve the CMR. The resistor R3 (15 kΩ) is a pull-down resistor used to keep the output of the driver off when no signal is used to drive the circuit. The connection between the open collector output and the LED can be seen in the Figure g-.

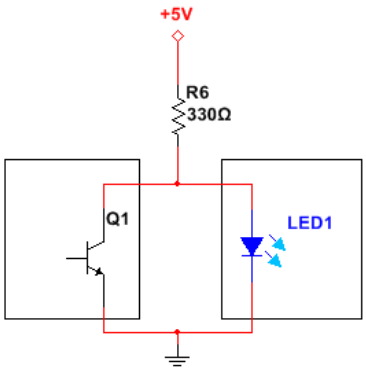


Figure g-2: Connection between the open collector buffer and the gate driver LED

The SN74ALS1035N is a non-inverting buffer, so when the input is a logic 1, the output will be 5 V and when the input is a logic 0, the output will be 0 V. From the point of view of the LED, when the output is 5 V, the current will circulate through the LED and when the output of the buffer is 0 V, the current will flow through the output of the buffer. The gate driver IC (HCPL-3120) is non-inverting, so the operating truth table is:

Input PWM Signal (Logic levels)	LED	Driver output
H	ON	H
L	OFF	L

Table g-1: Gate driver board truth table

The schematic that has been used for the layout design is represented on Figure g-3.

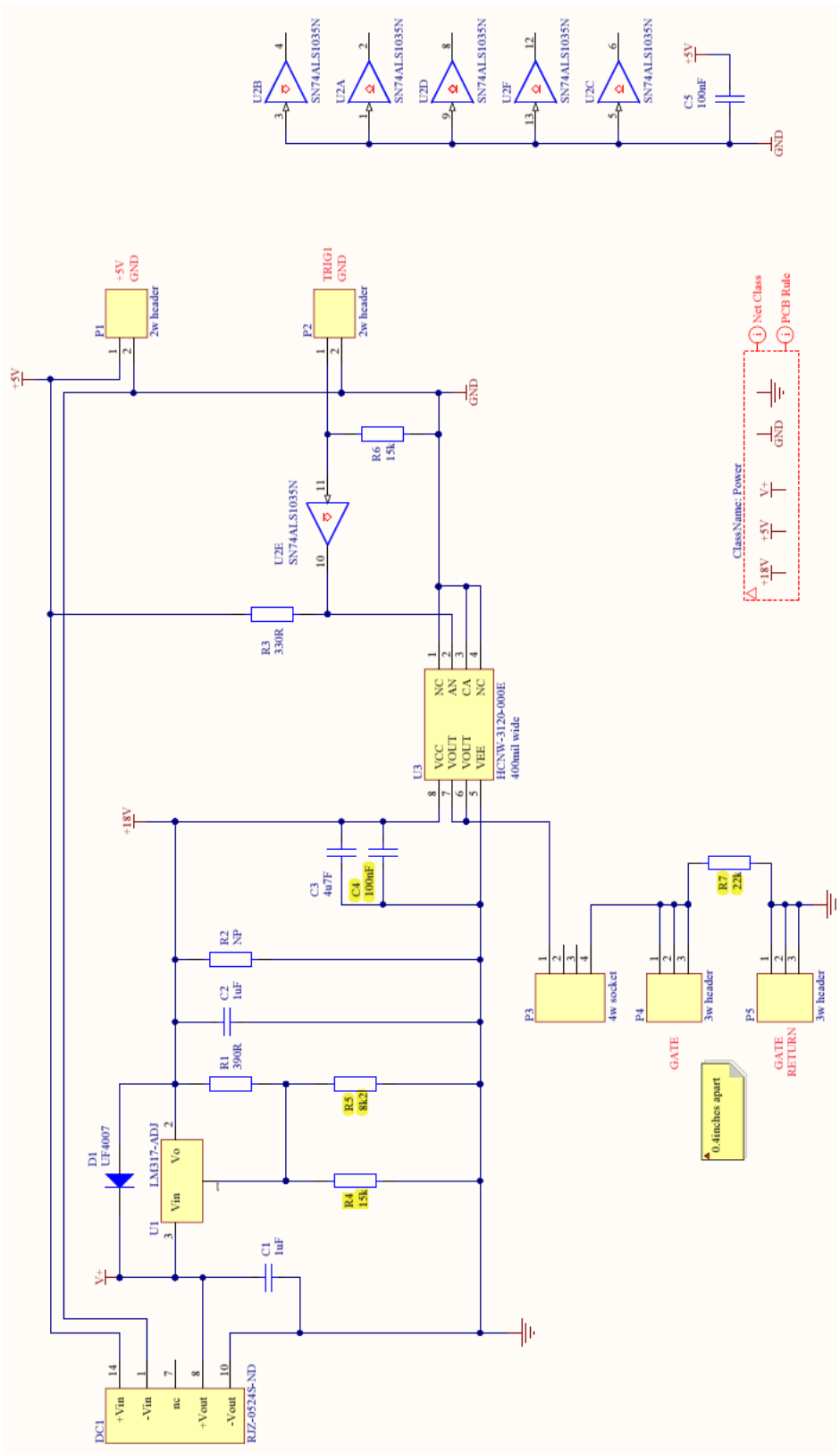


Figure g-3: Schematic of the E10778A2 gate driver board.