



Gurpinar, Emre and Castellazzi, Alberto (2016) Novel multilevel hybrid inverter topology with power scalability. In: 42nd Annual Conference of the IEEE Industrial Electronics Society (IECON 2016), 24-27 October 2016, Florence, Italy. (In Press)

Access from the University of Nottingham repository:

<http://eprints.nottingham.ac.uk/35839/1/A%20novel%20multilevel%20hybrid%20inverter%20topology%20with%20power%20scalability.pdf>

Copyright and reuse:

The Nottingham ePrints service makes this work by researchers of the University of Nottingham available open access under the following conditions.

This article is made available under the University of Nottingham End User licence and may be reused according to the conditions of the licence. For more details see: http://eprints.nottingham.ac.uk/end_user_agreement.pdf

A note on versions:

The version presented here may differ from the published version or from the version of record. If you wish to cite this item you are advised to consult the publisher's version. Please see the repository url above for details on accessing the published version and note that access may require a subscription.

For more information, please contact eprints@nottingham.ac.uk

Novel Multilevel Hybrid Inverter Topology with Power Scalability

Emre Gurpinar, Alberto Castellazzi
Power Electronics, Machines and Control Group
University of Nottingham
Nottingham, UK
Email: emre.gurpinar@nottingham.ac.uk

Abstract—In this paper, a novel multilevel hybrid inverter is presented. The inverter is based on 2 floating capacitors and 16 active switches for five-level voltage waveform between the output of the inverter and neutral point of DC link. The proposed inverter structure, switching states and commutation scheme for different output voltage levels are presented. The proposed topology is simulated and verified experimentally. The simulation results show that proposed topology can achieve higher efficiency in comparison to state-of-the-art hybrid topologies due to reduced conduction and switching losses at low modulation index and light load conditions. Experimental results show that the converter is successfully operated up to 1 kV DC link voltage and 12 kW output power.

Index Terms—Renewable energy, single-phase inverters, ANPC, active neutral point clamped inverter, stacked multicell converter, SMC, hybrid multilevel inverter

I. INTRODUCTION

Electricity generation from renewable energy sources such as wind, tidal, wave and solar has been one of the trending topics in power conversion research in order to reduce carbon emissions and dependency to limited fossil fuel supplies. Generating electricity by using photovoltaic panels and wind turbines has been one of the most studied topics. One of the main aims of the research in this area is increasing efficiency of the power electronics system that delivers the generated power from renewable sources to the grid.

Multilevel inverters have been discussed in literature as good candidates for high power conversion systems due to improved output voltage distortion, reduced voltage stress across power semiconductors and reduced filtering requirements [1], [2]. The first multilevel converter designs were based on neutral point clamped (NPC) and flying capacitor (FC) based topologies. These two approaches have been proposed for three and higher number of voltage levels. At high number of voltage levels (five and more), NPC based inverters suffer from high semiconductor count, high conduction losses and asymmetrical semiconductor switching loss. On the other hand, FC based topologies require complex control schemes for balancing flying capacitors and high energy storage in floating capacitors [1], [3].

Due to the limitations of NPC and FC based topologies for high number voltage levels (five and above), various hybrid topologies have been introduced [4]. One of the most popular hybrid topologies is five-level active neutral point clamped

(ANPC) inverter. ANPC is a member of half-bridge neutral point clamped inverter family and it was introduced in [5] as an alternative to three-level NPC inverter for improved loss balancing and better utilization of semiconductor chip areas in the inverter. Replacing diodes in NPC inverters with active switches provides additional zero states, and at the same time different modulation strategies can be applied with a flexible utilization of the redundant switching states. The three-level ANPC topology is extended to five-level ANPC (5L-ANPC) in [6]–[8] and presented in Fig. 1. 5L-ANPC is formed by 12 active switches and a floating capacitor C_{f_1} , where C_{f_1} voltage is fixed to E . By using the floating capacitor and neutral point, five voltage levels ($+2E$, $+E$, 0 , $-E$, $-2E$) can be achieved between the output (OUT) and neutral point (N). Similar hybrid five-level topology based on two floating capacitors $C_{f_{1-2}}$ and 14 active switches has been introduced in literature [9]. The topology is presented in Fig. 2. The floating capacitor voltages are kept at one fourth of DC link voltage and the inductor L_{f_1} is used for limiting inrush current between DC link capacitors and floating capacitors due to voltage variation across floating capacitors. Another hybrid multilevel inverter concept called "Stacked Multicell Converter" (SMC) is discussed in [10], [11]. The concept is based on increasing number of voltage levels at the output of the converter by introducing floating capacitor and active switch based cells. Five-level inverter based on SMC approach is presented in Fig. 3. In all three inverters presented in Fig. 1, 2 and 3, active devices are rated at one fourth of DC link voltage E .

In this paper, a new five-level hybrid inverter is presented. The details of the proposed topology including switching states and commutation scheme are presented in Section II. The simulation results including efficiency comparison with respect to 5L-ANPC is presented in Section III. Finally, the experimental results based on 12 kW prototype are presented in Section IV and discussed.

II. PROPOSED INVERTER TOPOLOGY

The proposed five-level inverter topology in this paper is based on a hybrid configuration of neutral-point-clamp and floating capacitors. The topology is named as "Efficiency and Dense Architecture: EDA5" and filed for patent application [12]. The topology is formed by 16 active switches S_1 – S_{10} , two floating capacitors $C_{f_{1-2}}$ and two DC-link capacitors

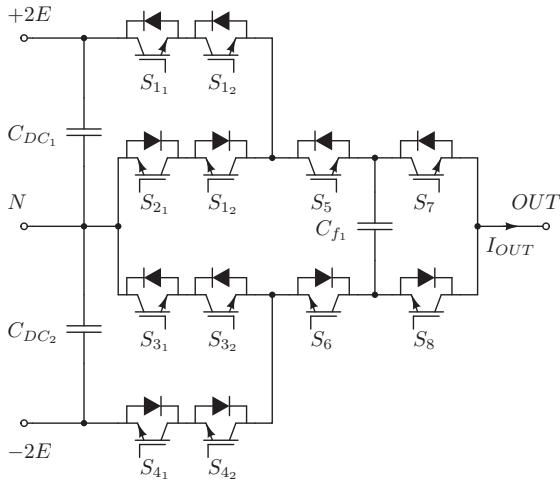


Fig. 1. 5L-ANPC inverter.

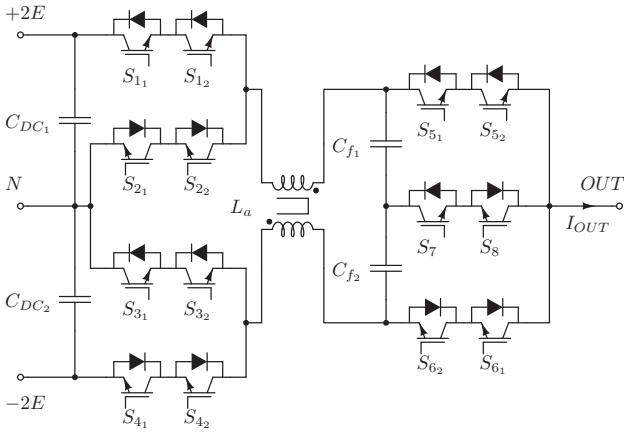


Fig. 2. FUJI five-level inverter.

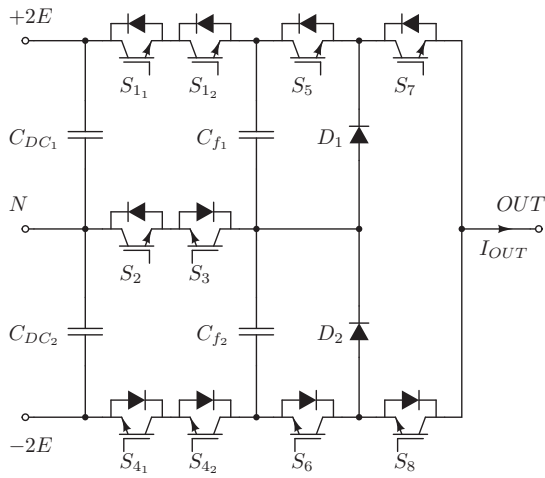


Fig. 3. Five-level stacked multicell inverter.

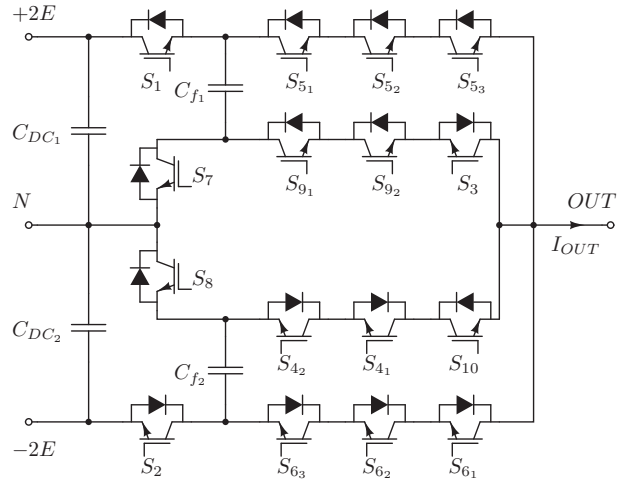


Fig. 4. Proposed five-level inverter topology: EDA5

C_{DC1-2} . The schematic of EDA5 is presented in Fig. 4. Each switch in the converter is rated at E , one-fourth of the total DC link voltage $4E$. The charge state of floating capacitors C_{f1-2} is controlled by utilizing redundant states in order to keep capacitor voltages at E for five-level voltage waveform ($2E$, E , 0 , $-E$ and $-2E$) between output of the converter (OUT) and neutral point (N) of input DC-link capacitors C_{DC1-2} .

A. Switching States

The switching states of the converter based on unity power factor operation are presented in Table I. Series connected switches such as S_{X1} and S_{X2} are switched on and off simultaneously, and therefore are represented as a single switch S_X in the switching state table. Single state is available for $+2E$ and $-2E$ output voltage levels while two states are available for $+E$ and $-E$ output voltage levels and three states are available for zero output state. The two switching states for $+E$ and $-E$ levels are achieved by introducing floating capacitors to the path of output current I_{OUT} . Depending on the polarity of output current and voltage, the floating capacitors are charged or discharged. In Table I, the switching states E_C and E_D define the charging and discharging states respectively for floating capacitors at unity power factor operation and inverter mode. For zero output voltage, three possible paths can be used: 1) upper path 0_P formed by S_3 , S_7 and S_9 , 2) lower path 0_N formed by S_4 , S_8 and S_{10} , 3) parallel path 0_X formed by simultaneous conduction of upper path 0_P and lower path 0_N . The main benefit parallel zero state path 0_X is the reduction of conduction losses in the power cell during low modulation indexes or higher DC link voltages, where zero state conduction is dominant.

The current paths for four different switching states during positive half of output voltage for inverter mode are presented in Fig. 5. It can be seen from Figs. 4 and 5 that four devices are in conduction during all switching states except zero state 0_X where the output current is divided into two zero state branches. Charge or discharge state can be selected during $+E$

TABLE I
SWITCHING STATES

State	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}
$+2E$	1	0	0	0	1	0	0	0	0	0
$+E_C$	1	0	1	0	0	0	0	0	1	0
$+E_D$	0	0	0	0	1	0	1	0	0	0
0_P	0	0	1	0	0	0	1	0	1	0
0_N	0	0	0	1	0	0	0	1	0	1
0_X	0	0	1	1	0	0	1	1	1	1
$-E_D$	0	0	0	0	0	1	0	1	0	0
$-E_C$	0	1	0	1	0	0	0	0	0	1
$-2E$	0	1	0	0	0	1	0	0	0	0

and $-E$ states in order to fix the floating capacitor voltage to the half of DC link capacitor voltage. For example, during unity power factor operation for inverter mode, at $+E_C$ state, switches S_1 , S_3 and S_9 are turned-on in order to apply $+E$ state to the output by subtracting floating capacitor voltage E from DC link capacitor voltage $+2E$ while charging the floating capacitor. During $+E_D$ state, the voltage across floating capacitor is applied to the output of the converter by turning-on S_5 and S_7 switches. The "charging" or "discharging" status of a switching state can be defined by polarity of output voltage and direction of output current.

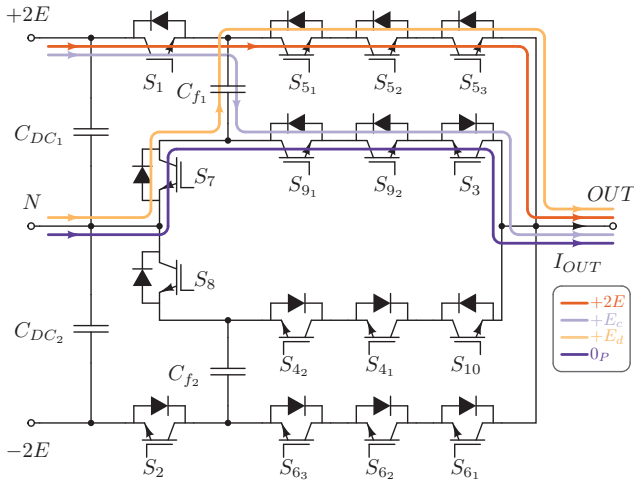


Fig. 5. Current paths for $+2E$, $+E_C$, $+E_D$ and 0_P states during positive half of output voltage.

B. Commutation Scheme

The commutation procedure between switching states, which are presented in Table I, has to be determined for transition of continuous output current from one state to another. The possible commutation schemes for the positive half of the output voltage for positive and negative output current are presented in Fig. 6. The blue and red curves for V_{OUT} represents output voltage with positive and negative output currents respectively. Due to the nature of the topology, suitable commutations can be realised between $+2E$ and $+E_{C-D}$ or $+E_{C-D}$ and 0_P states. The commutation between $+E_C$ and $+E_D$ is not possible without clamping the output to

another voltage state. In the first commutation scenario from $+2E$ to $+E_C$ in Fig. 6 (a), S_9 switch is turned-on first, and after the dead-time period t_{dt} , S_5 is switched-off and finally S_3 switch is turned-on. Depending on the direction of output current, the output voltage changes from $+2E$ to $+E_C$ state after t_{dt} or $2t_{dt}$. Commutation schemes in Fig. 6 (b), (c) and (d) have similar structure with Fig. 6 (a), and all of the schemes can be realised by applying logic gates to PWM signals coming from the controller.

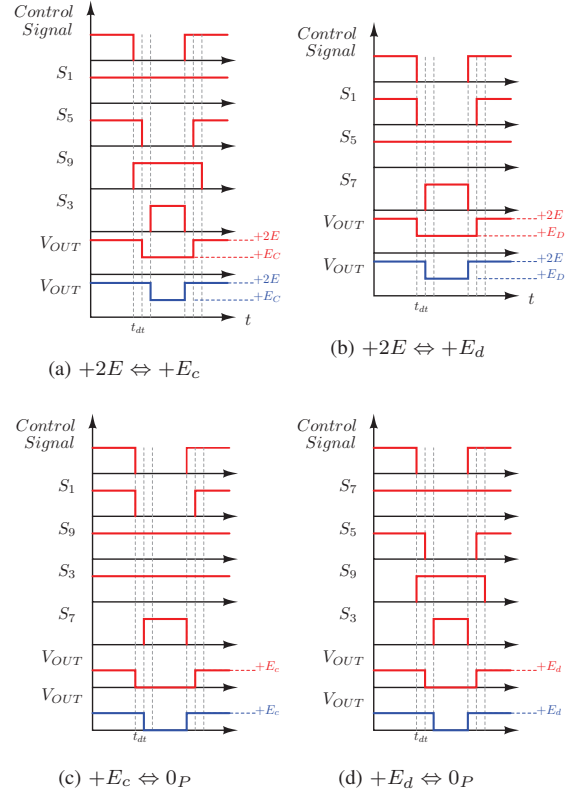


Fig. 6. Commutation schemes for the positive half of the output voltage.

III. SIMULATION RESULTS

The proposed topology is simulated in PLECS at inverter mode for evaluation of functionality and efficiency comparison with 5L-ANPC topology. The simulation conditions and converter parameters are presented in Table II. Medium voltage drive systems have been considered as the case study for the evaluation of the topology. Therefore commercial 1.7 kV, 800 A IGBT has been used in order to achieve 4.8 kV DC link voltage with 1.06 MVA output power [13]. Switching and conduction losses of switches at various operating conditions are calculated based on datasheet parameters at 125 °C junction temperature. Switching frequency is fixed to 2.5 kHz and current source is used in order to mimic continuous load current. The output voltage and current waveforms at 750 kW output power with 0.707 power factor are presented in Fig. 7. Modulation index is set to 0.9. It is proven that the converter can achieve five-level output waveform successfully by controlling floating capacitor voltages.

TABLE II
SIMULATION AND CONVERTER PARAMETERS

Parameter	Symbol	Value
Input Voltage	V_{DC}	4.8 kV
Output Power	P_{OUT}	750 kW
Output Power Factor	pf	0.707
Output Voltage	V_{OUT}	1.5 kV
Switching Frequency	f_{sw}	2.5 kHz
Switching Device	S_{1-10}	1.7 kV, 800 A IGBT
Junction Temperature	T_j	125 °C
Total Floating Capacitance	C_f	10 mF

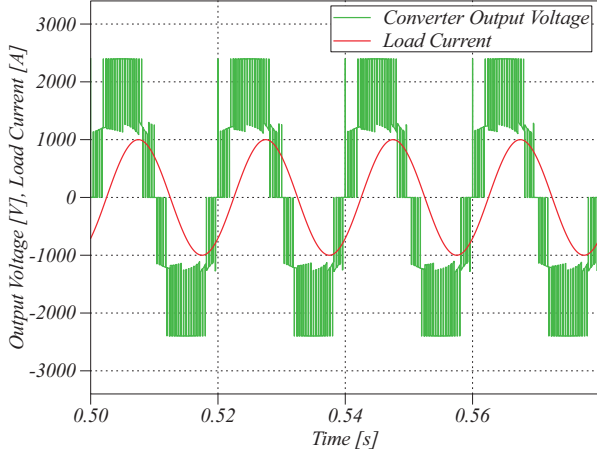


Fig. 7. Output voltage and current waveforms.

Under same operating conditions, floating capacitor voltages for C_{f1} and C_{f2} capacitors are presented in Fig. 4. The floating capacitor voltages are controlled by individual hysteresis controllers for each capacitor where main DC link and floating capacitor voltages are measured and compared. The upper and lower band of hysteresis control are set as 26.25% and 23.75% of total DC link voltage respectively in order to provide 10% control margin. Floating capacitor voltages with respect to hysteresis band limits are presented in Fig. 8. It can be seen that the capacitor voltages are exceeding hysteresis limits at certain time of operation. The reason for that is the hysteresis controller is forcing the output control signal, which determines charge or discharge state for each capacitor, to be changed during $2E$, 0 or opposite half of output signal with respect to each floating capacitor. As it is mentioned in commutation scheme section, the commutation of output current cannot happen between charging and discharging states and this approach prevents commutation between these two E states. The state of charge of each floating capacitor is dependent on load current and switching frequency. Therefore, the control of floating capacitor voltage with the hysteresis controller can be improved by increasing switching and increase of capacitance for same load conditions.

In order to evaluate efficiency performance of proposed topology, 5L-ANPC is simulated under same operating conditions in Table II. Two operation scenarios for the converters are considered: 1) voltage source operation where modulation index is fixed and output current is varied, 2) current source

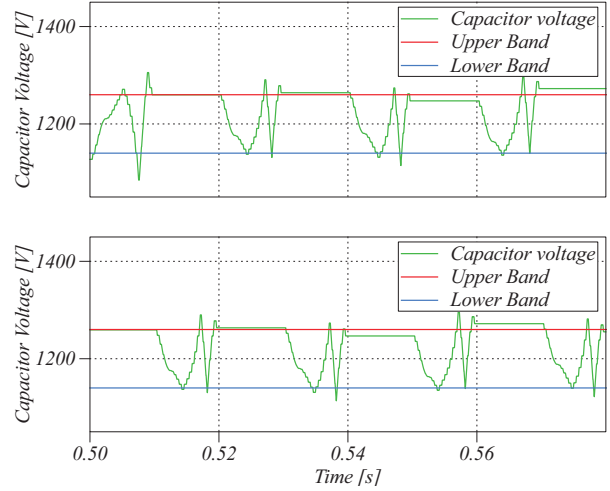


Fig. 8. C_{f1} and C_{f2} floating capacitor voltages.

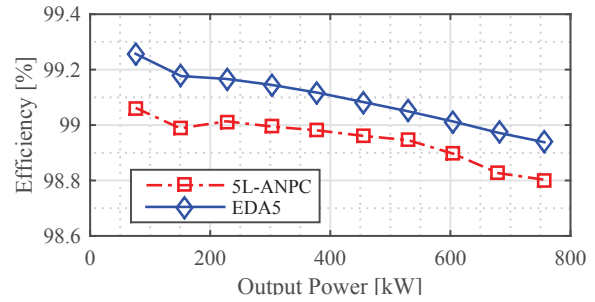


Fig. 9. Efficiency comparison with voltage source operation.

operation where output current is fixed and modulation index is varied. The efficiency results of single phase power cells for voltage source and current source operation are presented in Figs. 9 and 10 respectively. The results in Fig. 9 for voltage source operation show that proposed topology has approximately 0.2% higher efficiency under wide load range due to reduced conduction losses at zero voltage states. As presented in Fig. 10, during current source operation, the performance gap between proposed topology and 5L-ANPC is increased at light load conditions due to reduced conduction and switching losses at lower modulation index.

Switching and conduction losses for both operation modes have been analysed and presented in Figs. 11 and 12 for voltage source and current source operation respectively. With

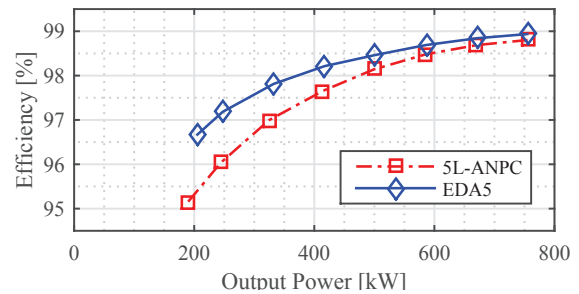


Fig. 10. Efficiency comparison with current source operation.

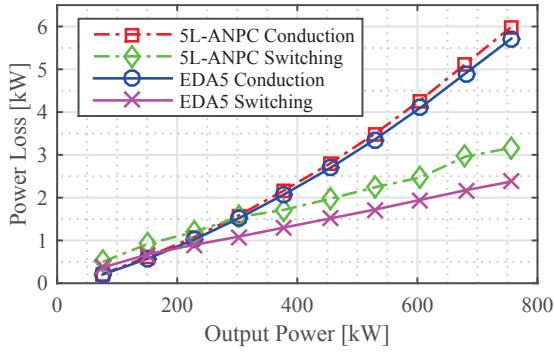


Fig. 11. Switching and conduction loss comparison with voltage source operation.

voltage source mode, the switching and conduction losses increase linearly and exponentially with respect to output power for both topologies. Although the conduction losses are similar, proposed topology has better switching performance in comparison to 5L-ANPC. The difference between switching losses is the reason for the efficiency difference between two topologies shown in Fig. 9. In current source mode, proposed topology has a significant advantage over 5L-ANPC under light load conditions due to reduced conduction and switching losses. This shows that proposed topology can operate with higher efficiency at higher DC link voltage and lower modulation index conditions.

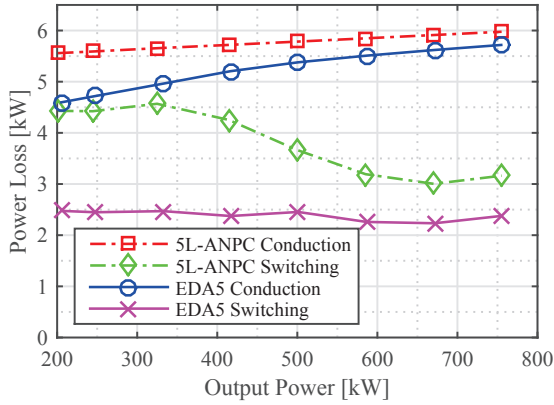


Fig. 12. Switching and conduction loss comparison with current source operation.

IV. EXPERIMENTAL RESULTS

Experimental validation of the proposed hybrid inverter topology is completed by a 12 kW single phase prototype. The prototype test parameters are presented in Table III and photo of the prototype can be seen in Fig. 13. The system can be extended to three phase by stacking single phase building blocks. Single phase building block consist of DC link film capacitors, floating capacitors, DC link and floating capacitor voltage sensors, gate drivers, switches and turn-off snubbers. DC link voltage sensors are used to control the

TABLE III
PROTOTYPE PARAMETERS

Parameter	Symbol	Value
Input Voltage	V_{DC}	1 kV
Output Power	P_{OUT}	12 kW
Switching Frequency	f_{sw}	10 kHz
Switching Device	S_{1-10}	600 V, 75 A IGBT
Output Filter Inductor	L_f	1.5 mH

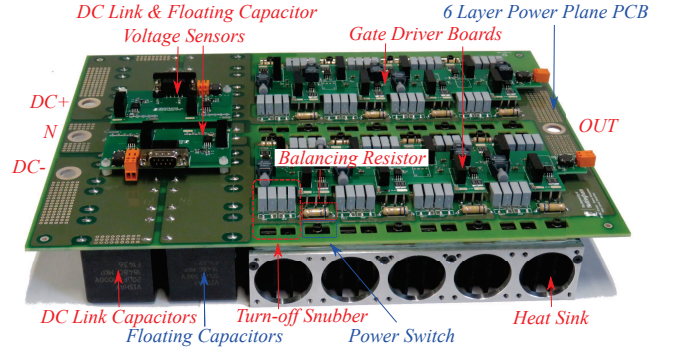


Fig. 13. Single phase 12 kW prototype.

floating capacitor voltage by hysteresis control implemented in DSP+FPGA control platform. Discrete IGBTs with anti-parallel diodes are implemented with RCD turn-off snubbers in order to achieve dynamic and static voltage sharing between series connected IGBTs presented in Fig. 4. Power plane is formed by 6-layer PCB with 140 μm copper on each layer for minimum parasitic inductance between commutating switches and minimum conduction losses.

The inverter output voltage and current waveforms at 2 kW and 12 kW output power conditions are presented in Figs. 14 and 15 respectively. The experimental results show that proposed topology successfully operates with an inductive load up to 12 kW output power. At 12 kW output power, it can be seen that output current is distorted due to the voltage variation at E and -E level (250 V, -250 V) due to voltage variation across floating capacitors C_{f1} and C_{f2} . The floating capacitor voltage with respect to DC link capacitor voltage is presented in Figs. 16a and 16b at 2 kW and 12 kW output power conditions. Although the average voltage of floating capacitor is fixed to half of DC link capacitor voltage 250 V for both load conditions, the peak-to-peak voltage variation across floating capacitor is increased from 30 V to 180 V with the increase of output current. The reason for the large variation at high output power is the sensor accuracy and limitations of control board. Due to control board limitations, the update rate for floating capacitor control is limited to 1 kHz and the effect of low update frequency makes voltage fluctuation more severe at higher output current conditions. This can be solved by improving accuracy of the sensors and also implementing the hysteresis control in the FPGA rather than DSP.

Finally, efficiency figures of the prototype power cell and total converter at 1 kV DC link voltage and 0.72 modulation

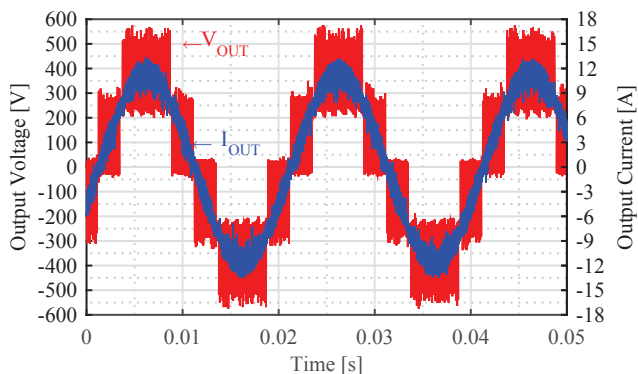


Fig. 14. Experimental output voltage and current waveforms at 2 kW output power.

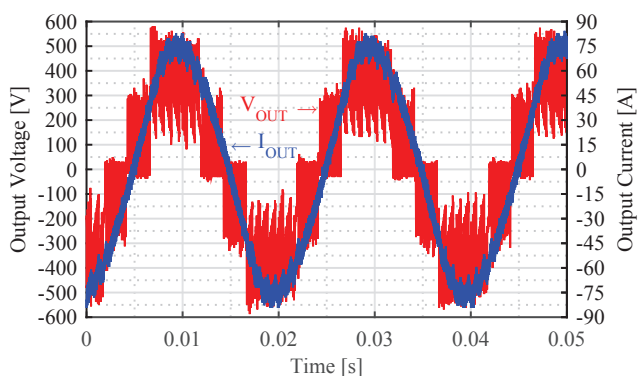


Fig. 15. Experimental output voltage and current waveforms at 12 kW output power.

index are presented in Fig. 17. The power cell efficiency curve includes DC link capacitor and power switch losses; and total efficiency curve includes power cell losses and output inductor losses. It can be seen that the prototype power cell can achieve 96% peak efficiency with Si IGBTs. The main objective of the prototype is demonstration of the functionality of EDA5 topology at high voltage and high power conditions. The efficiency of the prototype can be further improved by increasing the current capability of Si IGBT gate drivers and optimising RCD snubbers to minimise switching loss.

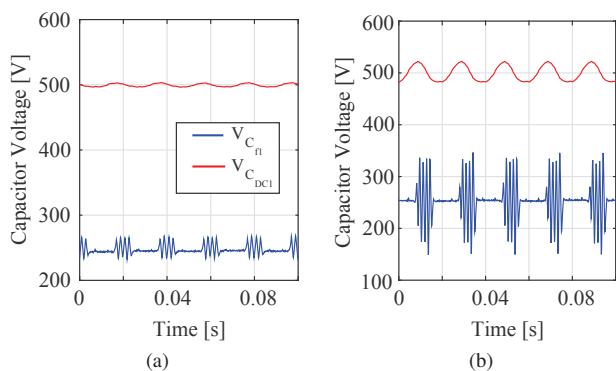


Fig. 16. DC link and floating capacitor voltage at (a) 2 kW and (b) 14 kW output power.

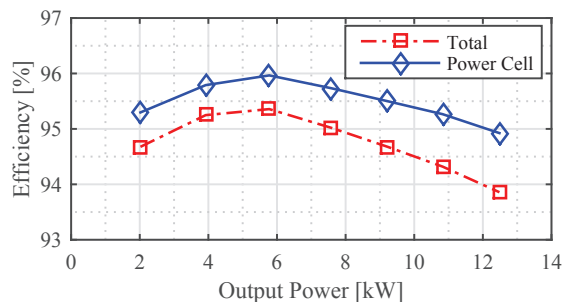


Fig. 17. Efficiency of the prototype at 1 kV DC link voltage and 0.72 modulation index.

V. CONCLUSION

In this paper, a novel five-level hybrid inverter topology for renewable energy systems and high power applications has been presented including description switching states and commutation scheme. The proposed topology is compared with state-of-the-art hybrid multilevel topologies in simulation. Simulation results show that EDA5 provides higher efficiency in comparison to 5L-ANPC, especially at lighter load conditions. The functionality of the topology has been verified experimentally with a 12 kW single phase prototype.

REFERENCES

- [1] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug 2002.
- [2] J.-S. Lai and F. Z. Peng, "Multilevel converters—a new breed of power converters," *IEEE Trans. Ind. App.*, vol. 32, no. 3, pp. 509–517, May 1996.
- [3] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped pwm inverter," *IEEE Trans. Ind. App.*, vol. IA-17, no. 5, pp. 518–523, Sept 1981.
- [4] M. D. Manjrekar, P. K. Steimer, and T. A. Lipo, "Hybrid multilevel power conversion system: a competitive solution for high-power applications," *IEEE Trans. Ind. App.*, vol. 36, no. 3, pp. 834–841, May 2000.
- [5] T. Bruckner, S. Bernet, and H. Guldner, "The active npc converter and its loss-balancing control," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 855–868, June 2005.
- [6] P. Barbosa, P. Steimer, J. Steinke, M. WinkeInkemper, and N. Celanovic, "Active-neutral-point-clamped (anpc) multilevel converter technology," in *Proc. of EPE*, Sept 2005, pp. 10 pp.–P.10.
- [7] F. Kieferndorf, M. Basler, L. A. Serpa, J. H. Fabian, A. Coccia, and G. A. Scheuer, "A new medium voltage drive system based on anpc-5l technology," in *Proc. of ICIT*, March 2010, pp. 643–649.
- [8] P. Barbosa, P. Steimer, and T. Chaudhuri, "Converter circuit for switching a large number of switching voltage levels," Sep. 17 2009, US Patent App. 12/421,660. [Online]. Available: <http://www.google.ch/patents/US20090231896>
- [9] M. Yatsu and K. Yoda, "Five-level converter," Apr. 6 2011, EP Patent App. EP20,100,177,221. [Online]. Available: <http://google.com/patents/EP2306629A2?cl=fi>
- [10] S. Dargahi, E. Babaei, S. Eskandari, V. Dargahi, and M. Sabahi, "Flying-capacitor stacked multicell multilevel voltage source inverters: analysis and modelling," *IET Power Electron.*, vol. 7, no. 12, pp. 2969–2987, 2014.
- [11] G. Gateau, T. A. Meynard, and H. Foch, "Stacked multicell converter (smc): properties and design," in *Proc. of PESC*, vol. 3, 2001, pp. 1583–1588 vol. 3.
- [12] E. Gurpinar, D. De, and A. Castellazzi, "Power converter," Patent Application GB 1 520 961.2, 11 27, 2015.
- [13] 5SND 0800M170100 Hi PAK IGBT Module, ABB Switzerland Ltd, Semiconductors, Apr. 2014, doc. No. 5SYA1589-01.