A High-Efficiency GaN Doherty Power Amplifier with Blended Class-EF Mode and Load-Pull Technique

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A High-Efficiency GaN Doherty Power Amplifier With Blended Class-EF Mode and Load-Pull Technique

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Abstract—**This paper presents a new Doherty power amplifier (DPA) configuration that employs high-efficiency switched-mode Class EF as its Main and Auxiliary cells. A blended approach is proposed to design the load network of the PA cells, in which the fundamental-frequency load impedance is obtained through load-pull analysis whereas the harmonic load impedances are set according to the Class-EF requirements. Realized using GaN HEMTs, the DPA prototype exhibits a drain efficiency (DE) of 81% at 45-dBm peak power and 68% at 6-dB back-off power, i.e. when excited using a 2.4 GHz continuous-wave signal. The proposed DPA has a 3-dB bandwidth of nearly 300 MHz within which the DE can be maintained above 68.5%. Using 16-QAM signal with 5-MHz bandwidth and 6-dB peak-to-average power ratio, the DPA shows a DE of 69.7% and an ACLR1 of -26.6 dBc at an average output power of 39.2 dBm.**

Index Terms—**Class-EF, Doherty, GaN HEMT, load pull, power amplifier, transmission line.**

Fig. 1. Constant PAE and output power contours resulted from the load-pull simulation at 2.4 GHz (P_{in} = 29 dBm, V_{DD} = 28 V, and V_{GG} = -2.7 V).

I. INTRODUCTION

IN THE classical Doherty power amplifier (DPA), the Main and Auxiliary cells are typically biased in Class AB and C modes, respectively, where the gate bias voltage of the Auxiliary cell is set below that of the Main cell in order to turn on the Auxiliary cell at 6-dB back-off power (BOP). Switched-mode Class-E DPAs and harmonically tuned DPAs wherein Class F, F^{-1} or J is employed as the Main and/or Auxiliary cells, have been shown to exhibit higher drain efficiencies compared to the traditional DPAs, [1]-[8].

The Class-EF PA introduced in [9]-[10] takes advantage of soft-switching operation offered by the Class E and low peak switch voltage of the Class F i.e. $2 \times V_{DC}$. However, when operated at high frequency to deliver high output power, the theoretical value of the capacitance shunting the ideal switch in the Class-EF topology is typically lower than the actual transistor's equivalent output capacitance. To address this problem, the so-called Fifth-Harmonic-Peaking (FHP) Class-EF PA was proposed in [11]. This new PA variant specifically satisfies the Class-EF load-impedance requirements at fundamental frequency (f_0), all even harmonics, and the first two odd harmonics, i.e. $3f_0$ and $5f_0$. In addition, the FHP Class-EF PA load network provides a means for simultaneous impedance matching to a typical 50-Ω load resistance, thus dispensing the need for an additional output matching circuit
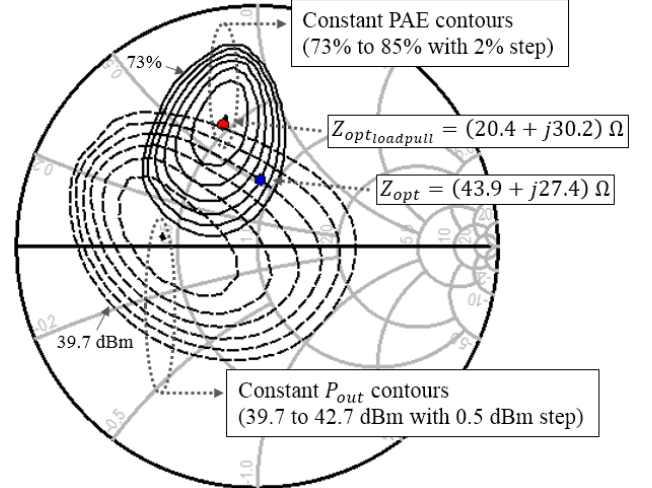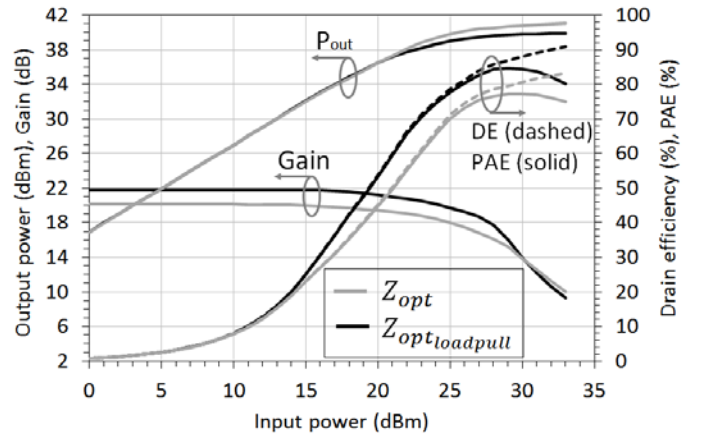
Fig. 2. Simulated PA performance at 2.4 GHz for Z_{opt} = $(43.9 + j27.4)$ Ω and $Z_{opt_{loadpull}}$ = $(20.4 + j30.2)$ Ω.

which would otherwise increase the overall loss.

The optimum fundamental-frequency load-impedance of Class EF (Z_{opt}) is derived using Fourier analysis by treating the active device as an ideal switch [9], but neglecting the presence of bond-wire inductances and package parasitics in the actual transistors. Because of this, the theoretical Z_{opt} will not provide best efficiency, and consequently, the load network's component values need to be tuned heavily in a practical design, hence increasing simulation time. In order to bridge the gap between the theory and practice, we propose a blended Class-EF mode and load-pull technique. Here the optimum fundamental-frequency load-impedance is obtained through load-pull simulations, whereas the load impedances presented to the output node of the transistor (i.e. drain) at harmonic frequencies will follow those in the Class EF. This load-pull

FHP Class-EF PA will then be employed as the Main and Auxiliary cells of the DPA.

The paper is organized as follows. Section II will present the design and implementation of the load-pull FHP Class-EF PA cell. Section III will explain how the PA cell treated in Section II is incorporated in the proposed DPA configuration, and describe the procedure to calculate the output combiner's transmission-line parameters, the DPA realization and the measurement results. Conclusions will be provided at the end.

II. LOAD-PULL FHP CLASS-EF POWER AMPLIFIER CELL: THEORY, DESIGN, AND IMPLEMENTATION

To obtain the optimum fundamental-frequency load impedance which gives best power added efficiency (PAE) ($Z_{opt_{loadpull}}$), a load-pull simulation was performed on a Cree's 10-W CGH40010F GaN HEMT device. Here the 2nd and 4th harmonic load impedances were set to zero whereas the 3rd and 5th harmonic load impedances were set to a large value (in this case, 50 kΩ), i.e. similar to that in the Class-EF mode. The gate and drain bias voltages were set to V_{GG} = -2.7 V and V_{DD} = 28 V. This arrangement resulted in $Z_{opt_{loadpull}}$ = $(20.4 + j30.2)$ Ω at the required operating frequency f_0 = 2.4 GHz. Fig. 1 shows the locus of this impedance on the Smith chart with respect to the constant output power and PAE contours generated from the simulation. For comparison, the theoretical Class-EF's optimum fundamental-frequency load-impedance (Z_{opt}) is also plotted in Fig. 1. For a given dead time τ_D = 48.5°, V_{DD} = 28 V, and output power P_{out} = 10 W, Z_{opt} is $(43.9 + j27.4)$ Ω, calculated using (1).

$$Z_{opt} = \frac{2\left(1+\cos\tau_D\right)^2}{\pi^2}\frac{V_{DD}^2}{P_{out}}\left\{1+j\frac{\tau_D - 0.5\sin\left(2\tau_D\right)}{\sin^2\tau_D}\right\} \quad (1)$$

Fig. 2 shows the simulated PA performance for Z_{opt} and $Z_{opt_{loadpull}}$. A PAE of 84.6% (drain efficiency DE = 86.8%) at 39.7 dBm output power and 16.1 dB gain was achieved for $Z_{opt_{loadpull}}$, showing a 7.4% improvement in PAE and a 2.2 dB improvement in the transducer gain (i.e. from 13.9 to 16.1 dB) compared to the case of Z_{opt}. The next challenging step is to design the PA's load network that presents $Z_{opt_{loadpull}}$ at f_0, a short circuit at $2f_0$ and $4f_0$, and an open circuit at $3f_0$ and $5f_0$. This can be accomplished by using the FHP Class-EF PA topology, Fig. 3. Note that C_B is a dc blocking capacitance. To find the electrical lengths and characteristic impedances of the idealized transmission lines TL$_1$-TL$_8$ shown in Fig. 3, we have followed the same circuit design methodology for the FHP Class-EF PA reported in [11].

Subsequently, the electrical parameters of these transmission lines were converted to the corresponding microstrip widths (W) and lengths (L), which were then optimized in the simulations to provide best efficiency. Both theoretical and optimized circuit component values are given in Table I. The complete circuit schematic of the load-pull FHP Class-EF PA is depicted in Fig. 4, and the simulated PA performance is shown in Fig. 5 where a maximum PAE of 81.3% (DE = 84.8%) was achieved at 41.4-dBm output power and 13.8-dB
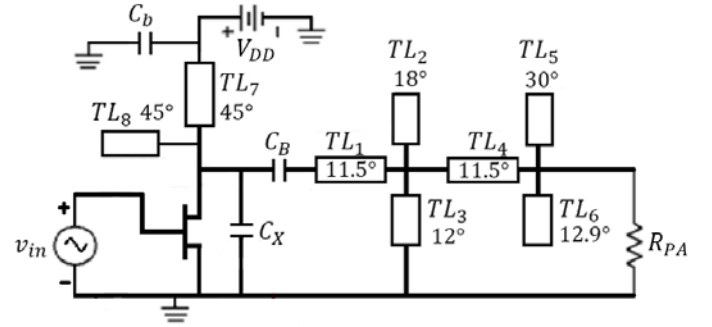

Fig. 3. Circuit schematic of the load-pull FHP Class-EF PA [11].

TABLE I
TRANSMISSION-LINE PARAMETER VALUES OF THE 2.4-GHz 28-V 10-W LOAD-PULL FHP CLASS-EF PA

Parameter	Theoretical Value (in mm)	Optimized Value (in mm)
$W_1 = W_4$	1.56	1.56
$L_1 = L_4$	2.28	2.28
$W_2 = W_3$	0.38	0.38
L_2	3.76	3.86
L_3	2.51	2.31
$W_5 = W_6$	0.73	2.00
L_5	6.12	6.22
L_6	2.62	2.52
$W_7 = W_8$	0.46	0.46
L_7	9.34	8.24
L_8	9.34	9.60

this simulation result and that presented in Fig. 2 wherein the PAE is slightly higher (i.e. 84.6%) and output power is lower (i.e. 39.7 dBm). This is chiefly because the circuit used to generate the result presented in Fig. 2 employs an equation-based component, the so-called "S1P_Eqn", to set different load impedances at the fundamental and harmonic frequencies, whereas the result presented in Fig. 5 was produced using the transmission-line load-network arrangement shown in Fig. 3.

To verify the aforementioned design concepts and simulation results, a PA prototype was constructed on a 0.508-mm thick Rogers RO4003C substrate with a dielectric constant of 3.55 and a loss tangent of 0.0027 (Fig. 6). The CGH40010F GaN HEMT was biased with V_{GG} = -2.5 V, and the PA was excited using a continuous wave (CW) signal at 2.4 GHz. Measured output power, gain, DE, and PAE were plotted in Fig. 7. A maximum DE of 84.4% (PAE = 80.8%) was achieved at 40.4-dBm output power and 13.8-dB gain. Fig. 8 shows the PA performance across a frequency range from 2 to 2.8 GHz within which the DE is higher than 61%.

III. CLASS-EF DOHERTY POWER AMPLIFIER: THEORY, DESIGN, AND IMPLEMENTATION

Shown in Fig. 9 is the block diagram of the proposed Doherty PA in which the load-pull FHP Class-EF PA described in Section II is employed as the Main and Auxiliary PA cells. Compared with the classical Class-B DPA [12], the new Class-EF DPA offers higher instantaneous drain efficiencies at both peak power and BOP levels, Fig. 10,
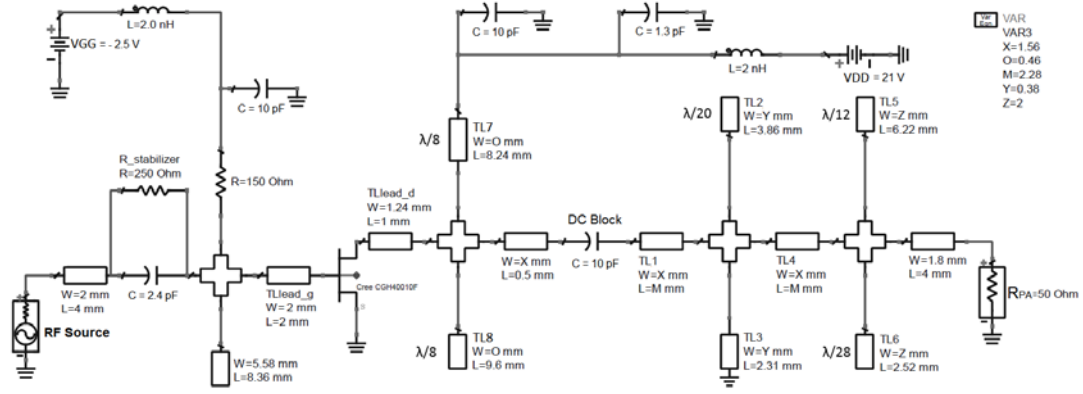
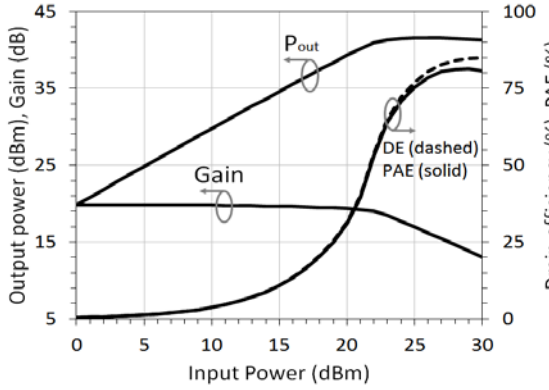Fig. 4. Complete circuit schematic of the load-pull FHP Class-EF PA.

Fig. 5. Simulated output power, gain, DE and PAE versus input power of the load-pull FHP Class-EF PA ($f_0 = 2.4$ GHz and $V_{GG} = -2.5$ V).
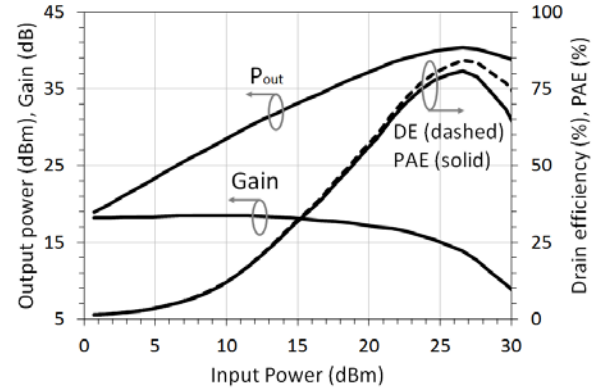

Fig. 7. Measured output power, gain, DE and PAE versus input power of the load-pull FHP Class-EF PA ($f_0 = 2.4$ GHz and $V_{GG} = -2.5$ V).
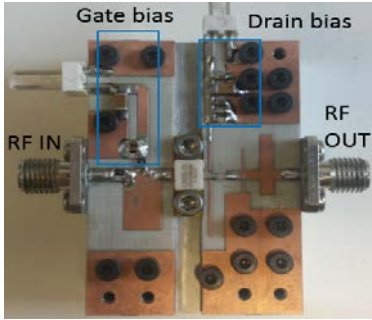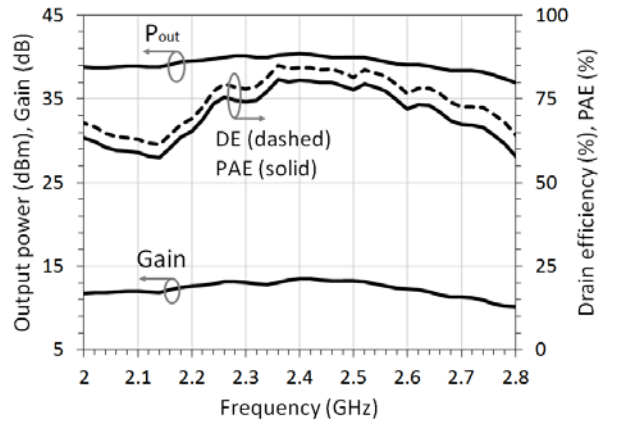

Fig. 6. The fabricated load-pull FHP Class-EF PA.

Fig. 8. Measured output power, gain, DE and PAE versus frequency of the load-pull FHP Class-EF PA ($P_{in} = 27$ dBm and $V_{GG} = -2.5$ V).

leading to a higher average efficiency (defined as a product of instantaneous efficiency and probability density function, e.g., Gaussian, Rayleigh, etc.). When the input drive voltage v_{in} is reduced from v_{max} to $v_{max}/2$, the impedances that the Main and Auxiliary PA cells present to the output combiner are modulated accordingly from R_{PA} to $2R_{PA}$ and from R_{PA} to infinity, respectively. Through this active load modulation, high efficiency across the back-off region as illustrated in Fig. 10 is achieved. The output combiner of the proposed DPA is comprised of three quarter-wave transmission lines, one at the Main branch (TL$_A$) and two at the Auxiliary branch (TL$_B$ and TL$_C$). A 90° hybrid coupler is required to evenly split the input power and provide a 90° phase shift at the input of the Main PA cell in order to compensate for the 90° phase difference between the Main and Auxiliary paths. For a given $R_{PA} = 50 \ \Omega$ and standard load $R_L = 50 \ \Omega$, the output-combiner transmission-line parameters can be calculated using the formulae given in Table II [13].

At peak power i.e. when the input drive voltage $v_{in} = v_{max}$, both Main and Auxiliary PAs are ON, presenting a load impedance of R_{PA} to the output combiner. The transmission line TL$_A$ transforms the Main PA's impedance R_{PA} to $R_{PA}/\alpha^2 = 2R_{PA}$. On the other hand, the transmission line TL$_B$ transforms the Auxiliary PA's impedance R_{PA} to $R_{PA}/\alpha = \sqrt{2}R_{PA}$ which is subsequently transformed by TL$_C$ to $R_{PA}/\alpha^2 = 2R_{PA}$. Since $R_{PA} = R_L$, the two parallel $2R_{PA}$ will provide a perfect match to R_L. At 6-dB BOP i.e. when the input drive voltage $v_{in} = v_{max}/2$, the Main PA is ON, presenting a load impedance of $2R_{PA}$ to the output combiner, whereas the Auxiliary PA is OFF, presenting an infinity load impedance to the output combiner. The transmission line TL$_A$ transforms the Main PA's impedance $2R_{PA}$ to $R_{PA}/(2\alpha^2) = R_{PA}$ which is matched to R_L.
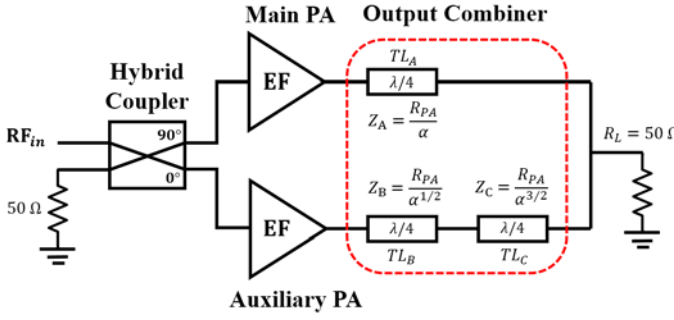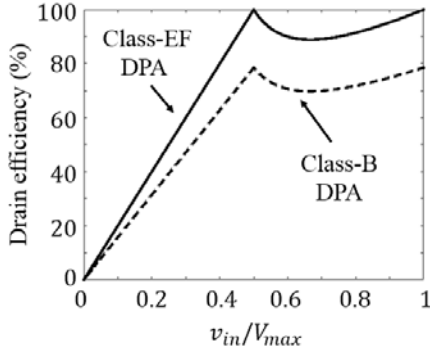
Fig. 9. Class-EF DPA block diagram.

Fig. 10. Idealized drain efficiency versus normalized input voltage for Class-B and Class-EF DPAs.

TABLE II
OUTPUT COMBINER PARAMETERS

Parameter	Equivalent to	Value
α	$\sqrt{R_{PA}/(2R_L)}$	0.707
Z_A	R_{PA}/α	70.7 Ω
Z_B	$R_{PA}/\sqrt{\alpha}$	59.5 Ω
Z_C	$R_{PA}/\alpha^{3/2}$	84.1 Ω

The DPA circuit was realized on Rogers RO4003C substrate (Fig. 11). It employed two 10-W CGH40010F GaN HEMTs with drain and gate bias voltages optimized for best efficiency, resulting in $V_{DD} = 28$ V, $V_{GG_{MAIN}} = -2.7$ V and $V_{GG_{AUX}} = -11.5$ V. A driver was connected to the input of the DPA to extend the input power range up to 37 dBm. Measurements using CW signal were performed with input power swept at 2.4 GHz. As shown in Fig. 12, the DPA exhibits a maximum DE of 81.3% at an output power of 45.3 dBm and a 3.1-dB compressed gain of 9.3 dB. Drain efficiencies of 82.8% and 68% were recorded at 4 and 6 dB output BOP, respectively. Here, a 6-dB input BOP corresponds only to 4-dB output BOP due to the compression of the Main PA. Also shown in Fig. 12 is the DPA performance when $V_{GG_{AUX}}$ was increased to -9.5 V while other bias voltages remained as before. Here, the transducer gain decreased to 11.8 dB from 12.4 dB, and a maximum DE of 78.9% occurred at 45.2-dBm peak power at which point the gain was compressed by 2.6 dB.
The frequency behavior of the DPA at both peak power and 6-dB output BOP levels is shown in Fig. 13. At peak power level, a maximum DE of 87.4% was obtained at 2.52 GHz, and the DE was maintained above 68.5% across the 2.3-2.6 GHz frequency range. At 6-dB BOP level, a maximum DE of 71% was achieved at 2.38 GHz. The DE was maintained above 40%
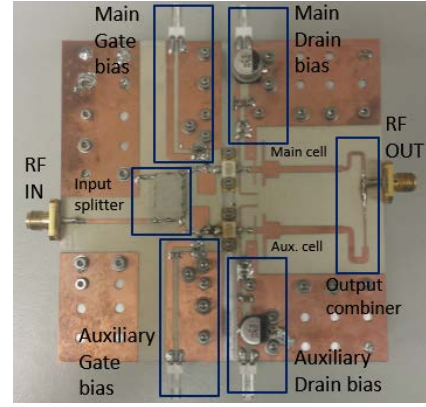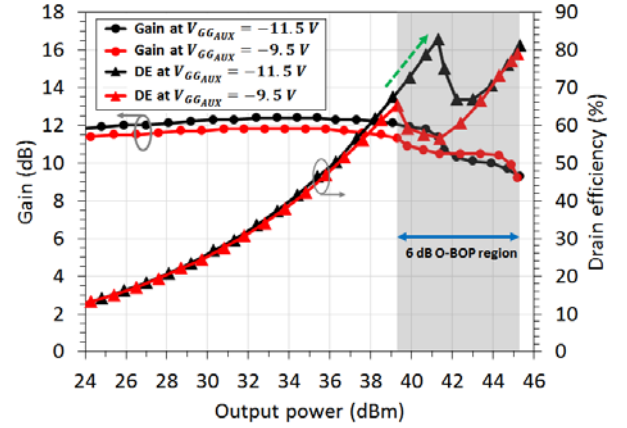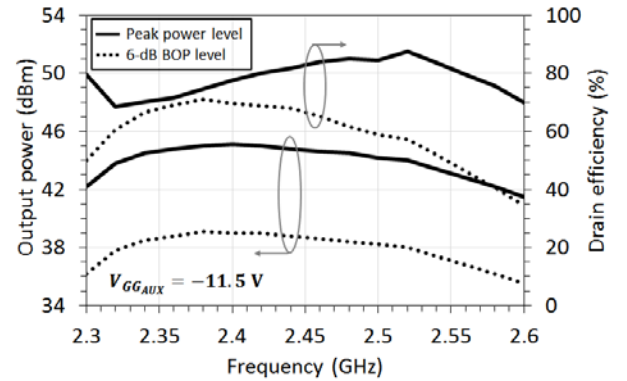

Fig. 11. The fabricated Class-EF DPA prototype (10 cm × 10 cm).

Fig. 12 Measured gain and DE versus output power of the Class-EF DPA ($f_0 = 2.4$ GHz, $V_{DD} = 28$ V, and $V_{GG_{MAIN}} = -2.7$ V).

Fig. 13. Measured output power and DE versus frequency at both peak power and 6-dB output BOP of the Class-EF DPA.

within 280-MHz frequency range, i.e., from 2.3 to 2.58 GHz.

To examine the performance of the DPA with modulated signals, the DPA was excited by two modulated signals that were individually generated from Rohde & Schwarz SMU200A signal generator, centered at 2.4 GHz, and analyzed by Rohde & Schwarz FSQ40 spectrum analyzer. The first signal is a single carrier wideband code division multiple access (W-CDMA) 3GPP signal with 45°-quadrature phase shift keying (QPSK) modulation scheme, 5-MHz bandwidth, and 4.8-dB peak-to-average power ratio (PAPR). Whereas the second signal is a 16-state quadrature amplitude modulated (16-QAM) signal with 5-MHz bandwidth and 6-dB PAPR.

Figs. 14 and 15 show the measured adjacent channel leakage ratios (ACLRs) and DE using the aforementioned modulated signals. With the W-CDMA signal, a maximum DE of 73.4%
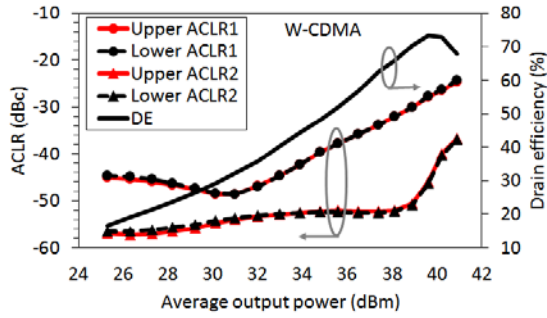
Fig. 14. Measured DE and ACLRs against the average output power with single carrier W-CDMA signal. $ACLR_1$ and $ACLR_2$ are at 5- and 10-MHz offsets from the carrier frequency, respectively.
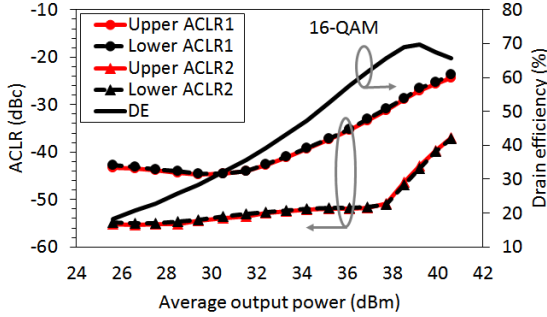

Fig. 15. Measured DE and ACLRs against the average output power with single carrier 16-QAM signal.

TABLE III
PERFORMANCE SUMMARY AND COMPARISON WITH OTHER PUBLISHED DOHERTY POWER AMPLIFIERS

Ref.	Class	Freq. (GHz)	P_{SAT} (dBm)	Instantaneous DE (%)	
				Peak power	6-dB BOP
[1]	F	0.85	43	67	58
[2]	F	2.14	35.1	54.7	43.7
[3]	E	2.14	46	72.5 (PAE)	61.2
[4]	F^{-1}	2.14	50	77	N/A
[5]	E	2.14	52.3	54	58.4
[6]	F^{-1}	2.6	57.3	N/A	53
[7]	J	2.7	45	79	60
[8]	F	3.5	46.8	64	53
[14]	AB-C	2.14	44	68.2	51.5
[15]	-	0.85	48.8	64.7	63.8
[16]	AB-C	1.8	40	45	28
This work	**EF**	**2.4**	**45.3**	**81.3**	**68**

with an $ACLR_1$ of -27.8 dBc was achieved at an average output power of 39.6 dBm. Whereas using the 16-QAM signal the DPA exhibits a maximum DE of 69.7% with an $ACLR_1$ of -26.6 dBc at an average output power of 39.2 dBm. When comparing between the two signals we find that the DPA shows, at high power operation, lower DE values when using the 16-QAM signal due to its higher PAPR. To sum up, the modulated wave measurements have shown an exceptional efficiency with quite good linearity performance that could be enhanced using the familiar linearization techniques such as digital pre-distortion.

The performance of the DPA prototype is summarized in Table III, and when compared with other published DPAs the proposed Class-EF DPA offers superior drain efficiencies at both peak power and 6-dB BOP levels.

IV. CONCLUSION

The Fifth-Harmonic-Peaking Class-EF PA has been, for the first time, employed as Main and Auxiliary cells of the Doherty PA. The optimum fundamental-frequency load impedance of the FHP Class-EF cell was obtained using load-pull technique to give best PAE. The fabricated and tested PA cell delivered a peak output power of 40.4-dBm at 84.4% DE. Continuous-wave measurements of the DPA prototype at 2.4 GHz have shown an excellent DE of 81.3% and 68% at peak power (45.3 dBm) and 6-dB back-off power, respectively. The proposed DPA exhibits a 3-dB bandwidth close to 300 MHz within which the DE is maintained above 68.5%. Using modulated wave signals with 5-6 PAPR, the DPA exhibits $ACLR_1$ levels below -26.5 dBc with drain efficiencies higher than 69.5%.

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