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Reduction of oscillations in a GaN bridge leg using active gate driving with sub-ns resolution, arbitrary gate-resistance patterns

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***Abstract*—Active gate driving provides an opportunity to reduce EMI in power electronic circuits. Whilst it has been demonstrated for MOS-gated silicon power semiconductor devices, reported advanced gate driving in wide-bandgap devices has been limited to a single impedance change during the device switching transitions. For the first time, this paper shows multi-point gate signal profiling at the sub-ns resolution required for GaN devices. A high-speed, programmable active gate driver is implemented with an integrated high-speed memory and output stage to realise arbitrary gate pull-up and pull-down resistance profiles. The nominal resistance range is 120 mΩ to 64 Ω, and the timing resolution of impedance changes is 150 ps. This driver is used in a 1 MHz GaN bridge leg that represents a synchronous buck converter. It is demonstrated that the gate voltage profile can be manipulated aggressively in nanosecond scale. It is observed that by profiling the first 5 ns of the control device's gate voltage transient, a reduction in switch-node voltage oscillations is observed, resulting in an 8-16 dB reduction in spectral power between 400 MHz and 1.8 GHz. This occurs without an increase in switching loss. A small increase in spectral power is seen below 320 MHz. As a baseline for comparison, the GaN bridge leg is operated with a fixed gate drive strength. It is concluded that p-type gate GaN HFETs are actively controllable, and that EMI can be reduced without increasing switching loss. (*Abstract*)**

Keywords— GaN; active gate driver; oscillation; electromagnetic interference (EMI); gate signal profiling; arbitrary gate impedance (*key words*)

I. Introduction

Active gate driving adjusts a power device's switching waveforms during the switching transient by shaping the gate voltage signal, as opposed to conventional gate drives that apply a voltage step-function to the gate via a fixed resistance. Active gate driving has been demonstrated with all types of MOS-gated silicon devices, usually with the intention of controlling di/dt and dv/dt [1], for example to allow dynamic voltage sharing of seriesed devices [2], and to reduce voltage overshoots [3] or EMI [1], [4]-[7]. It has been shown that by applying carefully shaped waveforms to the gate of silicon IGBTs, EMI is reduced without increasing switching loss [5]. In [6], the gate driver is an analogue amplifier with feedback, controlling high-power IGBTs, and in [7] a gate driver consisting of 8 digitally enabled parallel output stages reduces EMI of a power MOSFET circuit. Other methods exist to control di/dt and dv/dt, overshoots and EMI, such as adding snubbers [8] and non-linear damping integrated into the circuit board [9].

With the move to faster-switching wide-bandgap power devices, the need for waveform control increases. However, it remains unclear to what extent active gate control is possible emerging SiC and GaN devices. Two particular challenges arise: First, the control time resolution of the active gate driver must be small enough so as to be commensurate with the ns-level switching time of GaN devices; second, the delicate nature and the narrow gate voltage headroom of p-type GaN gates [12], make it harder to deliver a shaped gate signal through the low-pass filter composed of driver package, PCB tracks and parasitic elements of GaN HFET. In [10], 20 MHz switching with 40 V GaN HEMTs is presented using a gate drive with two fixed impedance levels to combine fast driving and mitigation of gate voltage overshoot. Reference [11] demonstrates the reduction of gate voltage overshoot in an 800 kHz buck converter using 1200 V SiC JFETs. A two-stage driver with programmable impedance levels allows the switchover between impedances to occur at a single chosen point in the switching transient.

In this paper, the first multi-point profiling of GaN gate signals is demonstrated, as illustrated in Fig. 1.

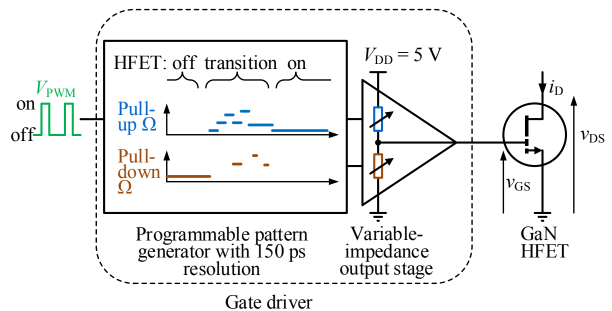

Fig. 1. Gate driver for multi-point resistance profiling.

For the first time, this driving method permits previously reported complex active gate driving methods for slower silicon devices to be translated to high-speed, wide-bandgap device switching transients. The chief objective is to establish whether enhancement-mode GaN devices are controllable via the gate during the switching transient, in a manner that would permit the control of switching waveforms. A GaN-based bridge-leg is selected as an evaluation platform for multi-point gate waveform profiling, as it incorporates a hard-switched control device and a soft-switched synchronous device in one circuit. Active gate driving can be applied to either or both devices. Since the driving of the control device actually determines the current and voltage commutations of both devices, the active gate driver is used to drive the control device only as a starting point. Here, the focus lies on shaping the switch-node voltage v_{SW} of a buck converter, Fig. 2, where high frequency oscillations of v_{SW} need to be attenuated as these can be a source of EMI. In this circuit, active gate driving is attractive, since a reduction in oscillations at the source of the electromagnetic emissions reduces the cost of subsequent filtering and shielding.

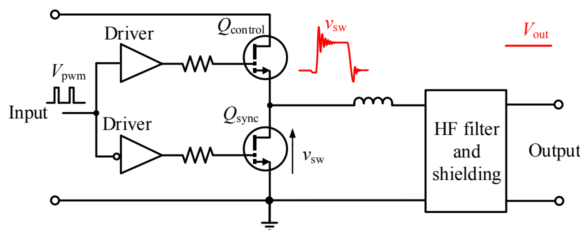

Fig. 2. Synchronous buck converter with conventional step-function gate driving with fixed drive resistances (sometimes incorporated into the drivers as shown here).

In this paper, Section II presents the method of multi-point gate waveform profiling, Section III describes the hardware implementation, and Section IV shows measured waveforms for constant-strength gate driving contrasted against active profiling that targets the reduction of oscillations. The driving patterns and the corresponding spectra are also provided, showing that the power in the spectrum of v_{SW} can be reduced without an increase in switching loss. In Section V, conclusions are drawn on the potential and limitations of the presented method of gate profiling.

II. Multi-Point Gate Waveform Profiling

A. Test Circuit

The clamped inductive switching circuit of Fig. 3 is employed to test gate voltage profiling in GaN-based converters. This circuit replicates the device interaction and hard-switching transitions in a synchronous buck converter. In contrast to the synchronous buck converter in Fig. 3, the bottom GaN HFET is driven by the programmable gate driver as the control device $Q_{control}$. It facilitates a ground-referenced gate drive interface. For simplicity, the gate and source terminals of the top GaN HFET Q_{sync} are shorted, resulting in the equivalent behaviour of a body diode. It is reasonable to hold the gate of Q_{sync} off as both turn-on and turn-off hard-switching commutations occur between $Q_{control}$ and the equivalent body diode of Q_{sync}.

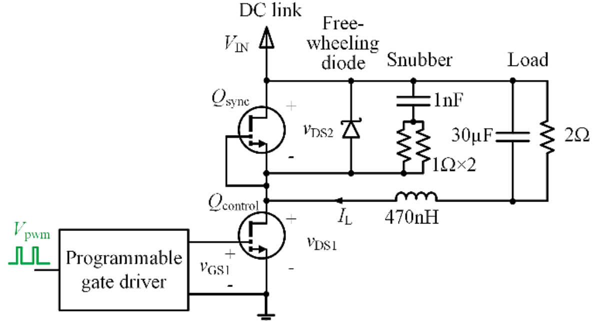

Fig. 3. High-side referenced buck converter test circuit used to generate results of Fig. 8 and Fig. 9.

One concern about GaN HFETs is the much higher source-drain voltage drop during self-commutated reverse conduction compared to Si MOSFETs. The conduction loss of Q_{sync} can thereby be a major loss component. An anti-parallel Schottky diode is placed across Q_{sync} to reduce the conduction loss [13]. However, the parasitic inductances of the diode together with the additional parasitic capacitance it adds to Q_{sync} may lead to more oscillation in the rising edge of v_{DS2} [14]. An RC snubber is one option to damp the oscillation observed on the rising edge of v_{DS2}, however efficiency is reduced as a result.

B. Transition of Interest

The transition of interest, highlighted in Fig. 4, is when the control device $Q_{control}$ turns on. Without multi-point profiling, this transition generates the most EMI: At fast switching speeds, a high displacement current flows through the synchronous device Q_{sync} and its anti-parallel diode, limited only by the parasitic circuit inductance. This current triggers oscillations in the underdamped resonant tank consisting of the parasitic capacitance of the synchronous device Q_{sync} and its anti-parallel diode, and the parasitic inductance of the bridge leg and DC-link bypass network. The resulting voltage oscillations in the drain-source voltage v_{DS2} of the synchronous device, illustrated in Fig. 5, are an important source of EMI. v_{DS2} is the equivalent of the switch-node voltage v_{SW} of the synchronous buck converter, which, in turn, is applied to the LC filter. Spectral components of this signal at frequencies above the self-resonance of the filter inductor can propagate to the output causing conducted and radiated electromagnetic emissions.

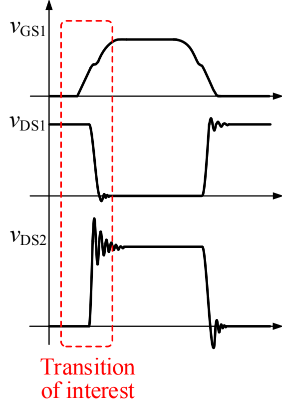

Fig. 4. Conceptual waveforms and the switching transition of interest to be shaped.

C. Gate Driving Strategy

The objective of multi-point waveform profiling at the transition of interest is to reduce the oscillation at v_{DS2} with little or no increase in switching loss. This transition, as shown in Fig. 5, can be divided into four consecutive stages: turn-on delay time t_d, current rise time t_{ir}, voltage fall time t_{vf} and oscillation time t_{osc}. The overlap loss is determined by the duration of current rise time and voltage fall time. In principle, a strong gate driving strength is needed for both intervals to reduce the switching loss, however, during the voltage fall, this increases the displacement current flowing through Q_{sync} and thereby exacerbates oscillation in the final stage. This illustrates the limitations of a constant strength driver. In contrast, multi-point gate profiling enables the choice of the best strength in each of the phases with an aim of striking a better compromise between oscillation reduction and switching loss. The gate driving strategy used here is described as follows.

$\boldsymbol{t_d}$ Turn-on delay time: As $Q_{control}$ remains off in this stage, a strong gate driving strength is applied to reduce the delay time.

$\boldsymbol{t_{ir}}$ Current rise time: A strong gate driving strength is used at the beginning to reduce the overlap loss. As the drain current slew rate determines the current overshoot and oscillation in the next stage, when drain current i_{D1} approaches load current I_L, the gate driving strength is reduced to slow down the rate of change of current.

$\boldsymbol{t_{vf}}$ Voltage fall time: A weak gate driving strength is applied at the beginning to reduce the voltage slew rate and the resultant displacement current flowing through $Q_{control}$. In order not to greatly increase the overlap loss, the gate driving strength is increased when v_{DS1} approaches zero.

$\boldsymbol{t_{osc}}$ Oscillation time: After v_{DS1} reaches steady-state, gate driving strength does not affect the oscillation in i_{D1} and v_{DS2}. A strong gate driving strength is applied to hold the device on.

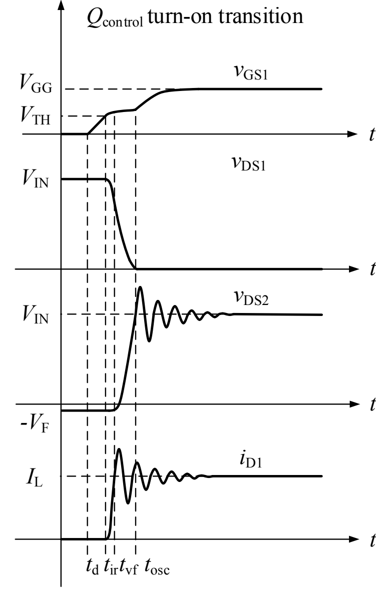

Fig. 5. Typical $Q_{control}$ turn-on switching waveforms.

III. Hardware Implementation And Testing Procedure

The programmable gate driver, whose main performance specifications are provided in Table 1, is fabricated in AMS HVCMOS 180 nm technology. It features a timing resolution of 150 ps, and spans an impedance range of 120 mΩ to 64 Ω. The sub-clock 150 ps timing resolution is achieved by digitally-selectable delay elements. This timing resolution and the low-impedance capabilities of this gate driver surpass any gate driver or arbitrary waveform generator known to the authors.

Table 1: Integrated gate driver specification.

Impedance range	0.12 – 64 Ω
Impedance levels	2^{15}
Time steps	88
Time resolution	150 ps
Architecture	Simultaneous operation of parallel pull-up and pull down drivers

This integrated driver consists of high-speed memory, control logic and a digitally-controlled gate drive output stage. The output stage consists of independently-controllable pull-up and pull-down networks with variable impedance. Once programmed with the desired strength and timing patterns, the chip is fully autonomous. The relevant desired resistance and timing values stored in the high-speed memory are applied to the output stages by the integrated control logic whenever the input PWM demand signal changes logic state. A change in logic state of the PWM signal triggers a gate-drive sequence that is 8 internal clock cycles long or approx. 13 ns (f_{clock} ≈ 620 MHz).

During each 13 ns transition, the pull-up and pull-down gate drives execute their respective stored patterns.

Fig. 6 shows the power circuit containing two EPC2015 GaN transistors and the programmable gate driver. PCB layout was optimised following recommendations in [15] to minimise parasitic inductances. The simulated in-circuit power loop inductance value is 0.57 nH. Near-constant DC link and gate-drive supply voltages are provided by carefully designed bypass networks incorporating high-frequency damping. An RC snubber is designed to provide damping at the frequency of the oscillations observed during the transition of interest. The values are carefully selected, with the aid of circuit simulation, to balance reduction in the amplitude of the oscillations against increased losses. The snubber is implemented with 0603-sized resistors and a 0402-sized capacitor, connected directly across the Schottky diode. However, its effectiveness is still limited by its parasitic inductance. The effectiveness of the snubber against that of profiled gate driving are shown in Section IV.

Fig. 6. Detailed view of the power board layout and 8 GHz RT-ZZ80 probe connections measuring the high-side device voltage v_{DS2} and low-side gate voltage v_{GS1}. Not shown is the 2 GHz RT-ZD30 probe connected to the underside of the board to measure v_{DS2}. Also on the underside are the anti-parallel diode and the snubber.

The power circuit is operated in continuous mode, rather than double-pulsed, in order to obtain periodic switching waveforms for frequency-domain analysis. Constant-resistance driving is carried out with the programmable driver rather than using a conventional driver and discrete gate resistor, which would alter the layout and thereby complicate the comparison.

The test hardware is implemented as shown in Fig. 7. A Digilent Zedboard with a Xilinx Zync 7000 series FPGA and ARM CPU system-on-chip programs the gate driver and generates the PWM switching waveform. Prior to testing, the host computer sends the desired gate drive patterns to the Xilinx system, which in turn programs the gate driver. During operation, the Xilinx system also provides the PWM demand signal. MATLAB, running on the host PC, configures the 4 GHz, 10 GSa/s Rhode & Schwarz RTO1044 oscilloscope to trigger on v_{DS2} rising edges, and capture and average 8,192 consecutive waveforms in order to lower the measurement noise floor [4]. The process is repeated for v_{DS2} falling edges. A complete pulse train is reconstructed in MATLAB for analysis and calculation of the spectra shown in Section IV. A pair of 8 GHz Rhode & Schwarz RT-ZZ80 transmission-line probes measure v_{GS1} and v_{DS1} respectively while a 2 GHz Rhode & Schwarz RT-ZD30 active differential probe with RT-ZA15 attenuator captures v_{DS2}.

Fig. 7. Overview of the test system hardware structure.

Input power (P_{IN}) is calculated from the input voltage and current, respectively measured using TT*i* 1604 and Fluke 8845A multimeters. Output power P_{OUT} is calculated from the output voltage and current, respectively measured using Fluke 8845A and Agilent U1273A multimeters. Although the absolute accuracy of the input and output power measurements is subject to significant measurement tolerances of the instrumentation, these are due to temperature-dependent offsets and thus repeatable. The data presented here is taken during the same hour with constant temperatures. Therefore, whilst the absolute power measurements quoted here may be inaccurate (up to +/- 100mW), the relative changes are accurate (+/- units of mW) allowing comparisons between different operating modes of this circuit.

IV. Experimental Results

A. Reduction of High-Frequency v_{DS2} Oscillations

The GaN converter described in Sections II and III is switched at 1 MHz, with a 10 V DC link, a 4 A load, and with a control-device duty cycle of around 94.8%. Fig. 8 shows the effect of two gate driving regimes on the high-side device voltage v_{DS2} (top), and the gate voltages v_{GS1} of the control device (middle). The pull-up and pull-down impedance patterns for the profiled regime are shown in Fig. 5 (bottom). First, 5.8 Ω fixed-resistance driving is seen to cause significant high-frequency oscillation (≈ 800 MHz) in v_{DS2}. Second, a gate pattern is formulated according to the gate driving strategy given in Sec. II. The profiling of the low-side gate is seen to significantly reduce the oscillations in v_{DS2}, without slowing down the switching transient. It is thereby demonstrated, for the first time, that aggressive sub-nanosecond manipulation of the gate impedance can be transmitted through the parasitic impedances of gate-driver packaging, PCB tracks, and GaN device gates, to result in beneficial changes to power circuit waveforms of a GaN-based converter.

The observable delay between the low-side gate and its effect on the high-side switch-node oscillation, is due to the low-side device controlling the drain current pulse in the high-side device, which, in turn, affects the drain-source voltage of this switch.

B. Spectra of v_{DS2} Voltage and Switching Loss

The high-side device voltage v_{DS2} spectral envelopes, calculated from the measured time-domain data, for the two driving regimes of Fig. 8 are shown in Fig. 9, alongside the measured total power-circuit loss. The total loss remains constant, indicating that switching loss has not significantly changed. With fixed-strength driving, two spectral peaks are present at approximately 800 MHz and 1.1 GHz. Changing to the profiled drive regime reduces these peaks by 8 and 16 dB (by 60% and 84%) respectively, whilst increasing the power in the spectrum between 210 and 320 MHz. At these lower frequencies, a cm-scale circuit does not radiate and filtering is effective. At frequencies of around 1 GHz however, a cm-scale circuit could create radiated EMI, and the effectiveness of a typical output LC filter is low due to parasitic impedances, especially the choke's parasitic capacitance. Approaches to addressing this include e.g. designing the choke in Fig. 2 with a high-self-resonant frequency. However, core geometries are restricted ([16], [17]) and windings costs may be increased. Alternatively, a second choke may be added in series with that in Fig. 2. Whilst the inductance of the first choke is set to control di/dt, the second choke has a lower inductance and consequently a higher self-resonant frequency. These solutions add cost and losses, hence the desirability of addressing EMI at source. It follows that the gate profiling regime has resulted in a valuable reduction and redistribution of spectral power.

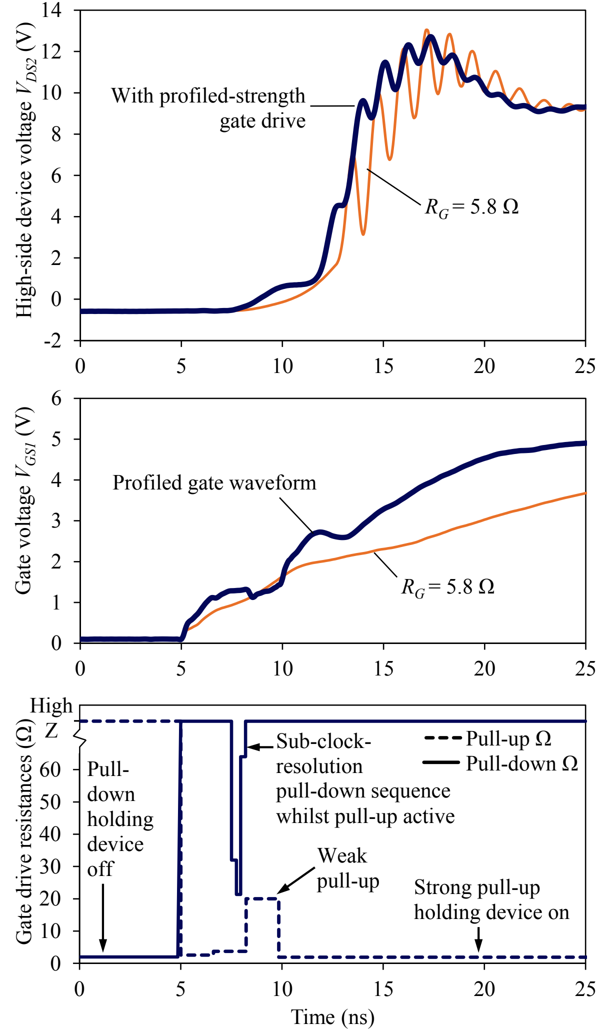

Fig. 8. Measured high-side device voltage v_{DS2} and low-side gate voltages v_{GS1} for two gate drive regimes: Standard gate drive with $R_G = 5.8$ Ω, and profiled gate driving. Top: v_{DS2} waveforms. Middle: v_{GS1} waveforms of control switch. Bottom: gate impedance profile for the profiled waveforms.

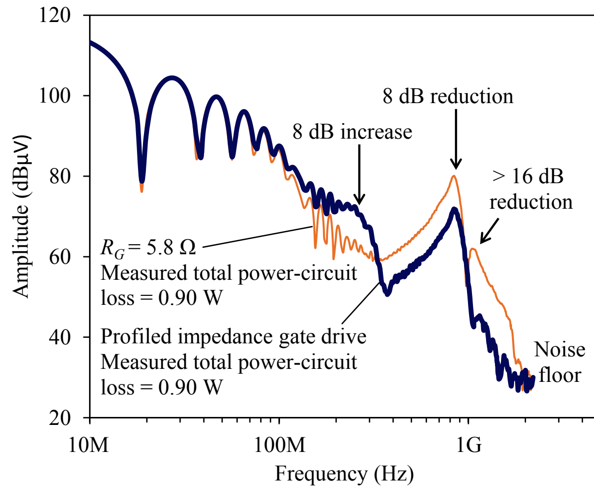

Fig. 9. High-side device voltage v_{DS2} spectral envelopes for two drive regimes: Standard gate drive with $R_G = 5.8\ \Omega$, and profiled gate driving.

V. Conclusions and Further Work

Sub-nanosecond-resolution, multi-point profiling of GaN gate signals has been presented. Applied to a GaN bridge leg, experimental results show that, when compared with the use of a fixed gate resistance, 8-16 dB reductions in the spectrum of the switch-node voltage of a buck converter are attained in the band from 400 MHz to 1.8 GHz, with negligible increase in switching loss. There is an 8 dB increase in spectral power from 200 MHz to 320 MHz where filtering is more effective and radiative transmission paths are unlikely to exist.

This work shows that aggressive active driving at wide-bandgap speeds is possible without the integration of the driver onto the GaN device. It also shows that the p-type GaN gate is actively controllable. We are aware that complex gate driving may not be viable in many low-power, low voltage applications, and therefore the transition to larger and higher voltage devices is being investigated. However, in the experiments shown in this paper, the driver is using only 18 of its 319 output transistors, and thus the implementation of a gate driver for this specific circuit would use only a fraction of the 5mm^2 silicon area of the presented integrated arbitrary waveform generator. We anticipate that active gate driving could be viable, not only for high-cost-of-failure systems, but also for lower cost mains voltage applications. In addition, arbitrary gate resistance driving could be valuable at the design stage of low-power applications.

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