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Four-Leg Converters with Improved Common Current Sharing and Selective Voltage Quality Enhancement for Islanded Microgrids

Xiao Zhou, Fen Tang, Poh Chiang Loh, Ximin Jin, Wenping Cao, *Senior Member*, *IEEE*

***Abstract*—Four-leg DC-AC power converters are widely used for the power grids to manage grid voltage unbalance caused by the interconnection of single-phase or three-phase unbalanced loads. These converters can further be connected in parallel to increase the overall power rating. The control of these converters poses a particular challenge if they are placed far apart with no links between them (e.g. in islanded microgrids). This challenge is studied in this paper with each four-leg converter designed to have improved common current sharing and selective voltage quality enhancement. The common current sharing, including zero sequence component, is necessary since loads are spread over the microgrid and they are hence the common responsibility of all converters. The voltage quality enhancement consideration should however be more selective since different loads have different sensitivity levels towards voltage disturbances. Converters connected to the more sensitive load buses should therefore be selectively triggered for compensation when voltage unbalances at their protected buses exceed the predefined thresholds. The proposed scheme is therefore different from conventional centralized schemes protecting only a common bus. Simulation and experimental results obtained have verified the effectiveness of the proposed scheme when applied to a four-wire islanded microgrid.**

***Index Terms*—Four-leg converter, microgrid, virtual impedance, voltage quality, unbalance.**

I. Introduction

INCREASING concern with fossil fuel consumption has led to the development of new and renewable energy, and the introduction of distributed generators (DGs) [1], [2]. Multiple DGs can then be integrated to form a microgrid with better shared advantages and more flexible operation. Controllability of the formed microgrid is also enormous because of the many power converters used for interfacing the DGs [3]-[6]. A microgrid is therefore self-contained, allowing it to operate in either the grid-connected or islanded mode. Its supply-demand requirement is less restrictive in the grid-connected mode with any surplus channeled to the grid and any shortfall drawn from it. The grid therefore behaves as a large energy reservoir for buffering any mismatches between supply and demand. The buffering effect is however not available in islanded operation which requires a strict supply-demand balance. Besides this, a load power sharing function among the DGs is needed to avoid stressing a particular DG. As a result, the control of DGs needs a decentralized technique (i.e. droop control) which is tuned according to the individual DG ratings. The operation of DGs relies only on locally measured quantities, and hence does not require communication links (named as wireless control in [7]-[9]).

Droop control was first developed for large synchronous generators and directed at balanced three-phase systems. Their active and reactive powers can be regulated by varying the system frequency and their respective terminal voltages. The same principle can be applied to power converters but does not work well when single-phase or three-phase unbalanced loads exist [10], [11]. Typically, the unbalanced load currents flow through the line and converter impedances, giving rise to unbalanced terminal voltages which can trip off sensitive loads. This problem is solved by employing active power filters (APFs) [12]-[14], static synchronous compensators (STATCOMs), dynamic voltage restorers (DVRs) [15], [16] or the unified power quality conditioners (UPQCs) [17]. However, these additions are costly. They are hence not attractive.

A less costly alternative is to oversize the existing DG converters slightly, and to modify their control algorithms to include some compensation functions [18]. For example, in [19] and [20], voltage unbalance was mitigated by injecting negative-sequence currents through the current-controlled DG converters. This method is however not applicable to voltage-controlled DGs. In [21], voltage unbalance was compensated by using multiple DGs. In order to achieve negative-sequence reactive power sharing, each DG is controlled as a negative-sequence conductor with its conductance drooping with the negative-sequence reactive power flow. However, the negative-sequence current sharing performance is affected by line impedance and droop coefficient mismatches. Another approach can be found in [22], where negative-sequence reactive power and compensation gain were used for

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correcting voltage unbalance in an islanded microgrid. The compensation gain is however load-dependent, and hence difficult to optimize. A modified virtual impedance loop for improving voltage quality is presented in [23], but it does not consider unbalanced load power sharing. It is thus more suitable for a single DG operation.

Moreover, most existing techniques focus on three-phase three-leg converters, where only positive- and negative-sequence currents can flow. This is certainly not the case for a three-phase four-wire microgrid, where four-leg DG converters are used for supplying single- and three-phase loads with an additional zero-sequence current return path [24]-[27]. Therefore, sharing unbalanced load current among those four-leg DG converters also needs to take account of zero-sequence component. The sharing should also be shouldered by all DGs, since powering dispersed loads in a microgrid should rightfully be the common responsibility of all DGs. Nonetheless, the voltage unbalance caused by unbalanced currents would impact individual loads differently, depending on their sensitivity levels. In this sense, each DG converter should have selective voltage compensation capability, while sharing the common load with the others.

This is a decentralized voltage compensation approach, which no doubt, is different from the centralized schemes discussed in [31] and [34] for unbalanced voltage compensation. Moreover, critical loads in these references are assumed to be connected to a single common bus, which is far away from the DGs. Therefore, their centralized schemes should have communication links. Ideally, the loads, storage and sources should all be spread. In addition, critical loads should be placed close to converters with the compensation ability like in the case of uninterruptible power supplies. It is therefore more appropriate to have a decentralized scheme with only DG converters near to critical buses enabled for compensation whenever their voltage unbalances exceed certain thresholds. Such a decentralized scheme is proposed and achieved in this paper with its effectiveness validated experimentally with a three-phase four-wire islanded microgrid. Comparing with the typical centralized compensation method, the proposed control scheme can better match with the concept of distributed generation and some issues including transmitting time delay and signal loss, which are introduced by communication links may be avoided.

II. Common Current Sharing

An illustrative islanded microgrid with two DGs is shown in Fig. 1. Each DG is tied to its local bus by a three-phase four-leg converter, where L and L_n[1] denote the filter inductances, C_f is the filter capacitance, Z_L is the line impedance, u_{inv} and u_o are the unfiltered and filtered output voltages, respectively. The four-leg converters must regulate their respective bus

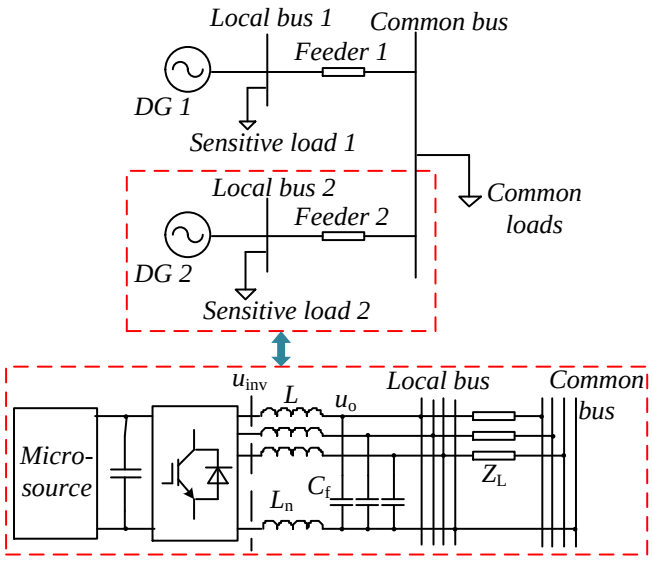


Fig. 1. Example of the three-phase four-wire islanded microgrid.

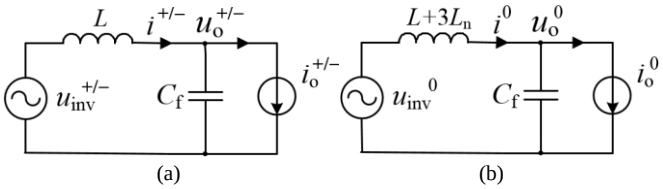


Fig. 2. Equivalent (a) positive- / negative- and (b) zero- sequence circuits of each four-leg DG converter.

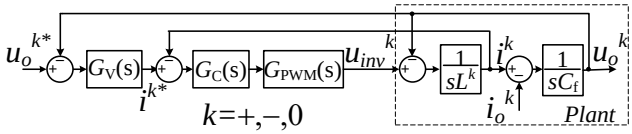


Fig. 3. Inner voltage and current control of each four-leg DG converter.

voltages and share the loads by applying droop control [7]-[9] if a decentralized scheme is preferred. Since the droop scheme works well only with balanced loads, only the positive-sequence current component in the three-phase four-wire microgrid is regulated. In reality, negative- and zero-sequence current components do exist as a result of unbalanced loads and they need to be addressed separately.

A. Control of individual four-leg converters

According to the symmetrical component theory, any phasor variables of the DG converter can be resolved into positive-, negative- and zero-sequence components, as shown in Fig. 2 [20], [28]. In this figure, i represents the instantaneous output current of the converter, while i_o represents the current after the LC filter. The superscripts +, –, and 0 denote positive-, negative- and zero-sequence components, respectively. It is not surprising that the two equivalent circuits look almost the same except for the inductance where $L^+ = L^- = L$ in Fig. 2(a) and $L^0 = L + 3L_n$ in Fig. 2(b). Ideally, the positive-sequence voltage u_o^+ should be set to a finite stable value, while u_o^- and u_o^0 should be nullified regardless of the amount of unbalanced currents drawn by the loads. This can be ensured by regulating each voltage

[1] Inductance L_n in Fig. 1 is for reducing switching frequency ripple in zero-sequence current along the common return line without influencing positive- and negative-sequence currents along the other three lines. Omitting L_n and increasing L alone will change all sequence currents. The effect of neutral line inductance can be found in [27].

component separately using the control scheme shown in Fig. 3 [28], where the superscript k = +, − or 0 denotes the sequence components, and the superscript * indicates the command reference.

Also shown in Fig. 3 are controllers $G_V(s)$ and $G_C(s)$ for regulating the terminal voltage and converter current, respectively. Modulator $G_{PWM}(s)$ is represented by a proportional gain. The output voltages can then be derived as

$$\begin{cases} u_o^+ = H^+(s)u_o^{+*} - Z_o^+(s)i_o^+ \\ u_o^- = H^-(s)u_o^{-*} - Z_o^-(s)i_o^- \\ u_o^0 = H^0(s)u_o^{0*} - Z_o^0(s)i_o^0 \end{cases} \quad (1)$$

where $H^+(s)$, $H^-(s)$ and $H^0(s)$ are the positive-, negative- and zero-sequence closed-loop gains, and $Z_o^+(s)$, $Z_o^-(s)$ and $Z_o^0(s)$ are the positive-, negative- and zero-sequence closed-loop output impedances, respectively.

Under balanced output voltage tracking, the demanded voltage references are set as $u_o^{+*} = u_{ref}$ and $u_o^{-*} = u_o^{0*} = 0$. Substituting these to (1) then leads to (2),

$$\begin{cases} u_o^- = -Z_o^-(s)i_o^- \\ u_o^0 = -Z_o^0(s)i_o^0 \end{cases} \quad (2)$$

where

$$Z_o^0(s) = \frac{L^0 s + G_C(s)G_{PWM}(s)}{L^0 C_f s^2 + (C_f s + G_V(s))G_C(s)G_{PWM}(s) + 1} \quad (3)$$

Equation (3) can also be used to represent $Z_o^+(s)$ and $Z_o^-(s)$ upon replacing L^0 with $L^+ = L^-$. Transfer function analyses for all sequence impedances are therefore the same even though only $Z_o^-(s)$ is considered in (3). Ideally, (3) should be zero in order to prevent the load current components i_o^+, i_o^- and i_o^0 from affecting the output voltages u_o^+, u_o^- and u_o^0 according to (1). This can be ensured by choosing a large $G_V(s)$, at least, at the frequency of interest. In terms of unbalance control with a four-leg converter, a large $G_V(s)$ implies that the system fundamental frequency f (or ω in angular notation) should be considered for all three sequence components if the control scheme is implemented in the stationary frame. However, if the positive-sequence synchronous *dq0* frame is preferred to merge with the accompanied droop control, three frequencies of interest must be specified. They are 0 Hz for positive-sequence, ω for zero-sequence and 2ω for negative-sequence regulation when all sequence components are referred to the same positive-sequence synchronous frame.

High gains at these frequencies can be obtained by using an integral term in $G_V(s)$ for the positive-sequence regulation and a resonant term at 2ω for the negative-sequence regulation. The resulting transfer function is given in (4),

$$G_{PIR}(s) = k_p + \frac{k_i}{s} + \frac{2k_r\omega_c s}{s^2 + 2\omega_c s + (2\omega)^2} \quad (4)$$

where k_p, k_i and k_r are the controller gains, and ω_c is the cutoff frequency of the third resonant term. The same resonant term, but with its resonant peak shifted to ω, can be used for regulating the zero-sequence component. The required transfer function is given in (5),

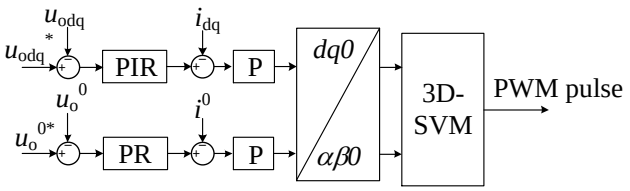


Fig. 4. Illustration of controller types for the inner voltage and current control of each four-leg DG converter.

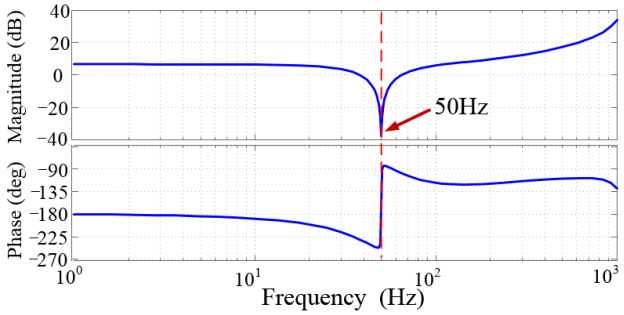


Fig. 5. Bode plot of the zero-sequence output impedance.

$$G_{PR}(s) = k_{p0} + \frac{2k_{r0}\omega_c s}{s^2 + 2\omega_c s + \omega^2} \quad (5)$$

where k_{p0} and k_{r0} are the accompanied controller gains.

The placement of (4) and (5) in the control scheme can be seen in Fig. 4, where only a proportional term (*P*) is used as $G_C(s)$ (= k_c) for all sequence components. Higher order terms such as an integral or resonant term can be included in $G_C(s)$ too, but is generally not necessary. To demonstrate this, (3) can be simplified as (6) if only a large $G_C(s)$ is assumed.

$$Z_o^0(s) \approx \frac{G_C(s)G_{PWM}(s)}{(C_f s + G_V(s))G_C(s)G_{PWM}(s)} \approx \frac{1}{C_f s + G_V(s)} \quad (6)$$

Clearly, $Z_o^0(s)$ will not approach zero if $G_V(s)$ is not large enough, regardless of the order of $G_C(s)$. Therefore, $G_C(s)$ can merely be a proportional term to simplify the controller design. For verification, Bode diagram of $Z_o^0(s)$ is plotted using parameters listed in Table I. This plot clearly shows a very low impedance (−40 dB or 0.01 Ω) at the frequency of interest (ω = 2π × 50 rad/s). Therefore, it is sufficient to use a proportional term as $G_C(s)$ with its output fed to a three-dimensional space vector modulator (3D-SVM) described in [27].

B. Common current sharing based on virtual impedances

The control scheme in Fig. 3 requires a voltage command notated as u_o^{k*} (k = +, − or 0). For a single converter, this command can be set to a fixed system voltage designed for the microgrid. The fixed voltage command will however not function well when two or more converters are interconnected. This is because $G_V(s)$, consisting of (4) and (5), will make the converters behave as ideal voltage sources with zero output impedances. The current or power combination from these ideal voltage sources is then not uniquely defined. It is thus possible for a lower rated converter to supply more power than a higher rated converter provided that the microgrid is stable. This is certainly not desired since the lower rated converter

will be stressed unfairly. To avoid the problem in a decentralized manner, droop control is implemented by using those linear expressions in (7),

$$\begin{cases} \omega = \omega^* - mP \\ E = E^* - nQ \end{cases} \tag{7}$$

where P and Q are active and reactive powers controlled by the converter, m and n are the frequency and voltage droop coefficients, and ω and E are the operating frequency and voltage magnitude, respectively.

In effect, (7) creates an effective frequency range for ω and a voltage range for E those are linearly mapped to the converter P and Q ranges by the droop coefficients m and n. Ideally, m and n should be tuned inversely proportional to the converter power ratings. Using ω and E then results in a variable voltage command for the converter, whose value is uniquely mapped to a defined set of P and Q. The unequal power flows through the converters are therefore avoided at the expense of a slight variation of terminal voltage. The droop scheme is however effective only for balanced systems where P and Q are predominantly constant in the steady state. In case of an unbalanced microgrid, the same droop expressions in (7) can be used, but only for its positive-sequence balanced components. Otherwise, it would give rise to oscillation because of power ripples introduced by the unbalanced components. Negative- and zero-sequence power sharing must hence be managed separately in a four-wire microgrid, where single- and three-phase unbalanced loads exist.

The unbalanced sharing principles can be explained by referring to Fig. 6, where Thévenin equivalent circuits of two four-leg converters connected in parallel are illustrated. Included in the figure are Z_{L1}^-, Z_{L2}^-, Z_{L1}^0 and Z_{L2}^0 for representing sequence components of line impedances between the DGs and common bus, and Z_{o1}^-, Z_{o2}^-, Z_{o1}^0 and Z_{o2}^0 for representing closed-loop control impedances of the DG converters. The latter four impedances will be zero if (4) and (5) are used as $G_V(s)$ in Fig. 3. Sharing of sequence load currents i_o^- and i_o^0 will then be determined by the line impedances, rather than controlled by the DG converters. To regain controllability, a simple technique is to insert negative- and zero-sequence virtual impedances by modifying the sequence control schemes of the converters. The added virtual impedances will be in series with the line impedances, and if they are chosen sufficiently large, the line impedances can be ignored.

Similarly, positive-sequence virtual impedances can be inserted, but their purposes are mainly for improving reactive power sharing or power decoupling in a low-voltage microgrid, where resistance dominates inductance [29], [30]. These purposes are well explained in the literature, and hence not further discussed in the paper. For the inserted negative- and zero-sequence virtual impedances, their corresponding control modifications are relatively simple, involving only minor changes to u_o^{-*} and u_o^{0*} in Fig. 3. These references are no longer zero. Instead, they are equal to the voltage drops ($u_o^{-*} = -u_{zv}^-$ and $u_o^{0*} = -u_{zv}^0$) across the resistive virtual impedances

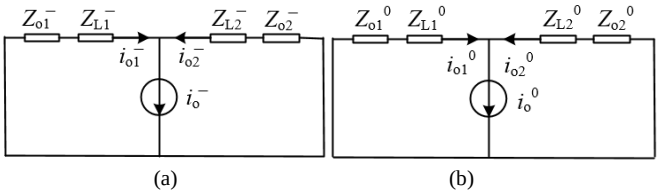


Fig. 6. Thévenin equivalent circuits of two four-leg DG converters connected in parallel. (a) Negative- sequence circuit. (b) Zero-sequence circuit.

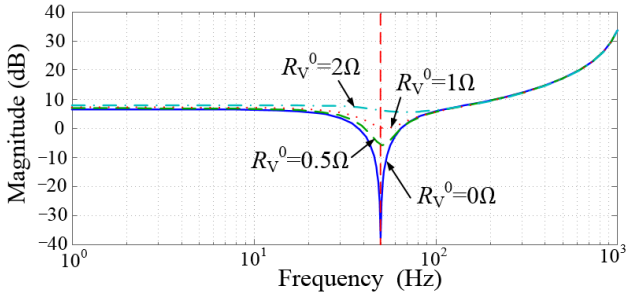


Fig. 7. Bode plot of zero-sequence output impedance after the insertion of zero sequence virtual impedances.

expressed in (8). Alternatively, reactive virtual impedances can be considered, but they are not encouraged because of possible derivative noise amplification at high frequency. This is especially true along the zero-sequence return path, where common switching noises from all three phases sum together.

$$\begin{cases} u_{ZV}^- = R_V^- i_o^- \\ u_{ZV}^0 = R_V^0 i_o^0 \end{cases} \tag{8}$$

With the inserted virtual impedances, zero-sequence output voltage of each DG converter then changes to

$$u_o^0 = H^0(s)u_o^{0*} - (H^0(s)R_V^0 + Z_o^0(s))i_o^0 \tag{9}$$

Equation (9) can similarly be used for representing positive- and negative-sequence output voltages after replacing the superscript 0 with + and –, respectively. They are hence not explicitly shown. From (9), the new output impedance of the converter can then be written as $Z_{oV}^0(s) = H^0(s)R_V^0 + Z_o^0(s)$, which upon expanded, leads to (10),

$$Z_{oV}^0(s) = \frac{L^0 s + (R_V^0 G_V(s)+1)G_C(s)G_{PWM}(s)}{L^0 C_f s^2 + (C_f s + G_V(s))G_C(s)G_{PWM}(s)+1} \tag{10}$$

Bode diagram of $Z_{oV}^0(s)$ after the addition of virtual impedances is shown in Fig. 7, where it is noted that its magnitude increases with R_V^0 at the system frequency of 50 Hz. The converter output impedance is therefore controllable, and is almost equal to R_V^0 if R_V^0 is large (e.g. $|Z_{oV}^0|$ = 0.0784 dB = 1.009 Ω when R_V^0 = 1 Ω). Indirectly, that also means the sequence current sharing can be controlled, as viewed from those sequence equivalent circuits in Fig. 6, where Z_{ox}^- and Z_{ox}^0 are now replaced by Z_{oVx}^- and Z_{oVx}^0, respectively (x = 1 or 2 for distinguishing the two DGs). When $|Z_{oV}^0| >> |Z_L^0|$, the zero-sequence current i_{o1}^0 flowing through DG1 can then be derived as

$$i_{o1}^0 = \frac{Z_{oV2}^0}{Z_{oV1}^0 + Z_{oV2}^0} i_o^0 \tag{11}$$

Obviously, $i_{o1}{}^0$ can be controlled proportional to the DG rating of S_1, if $Z_{oVx}{}^0 \approx R_{Vx}{}^0 \propto 1 / S_x$ or $Z_{oV1}{}^0 S_1 = Z_{oV2}{}^0 S_2$ for the two-DG example shown in Fig. 1. The same sharing principle can equally be applied to the negative-sequence current, as mentioned earlier.

III. Selective Bus Voltage Enhancement

It has been demonstrated that the common load current sharing among the DGs can be achieved by inserting large sequence virtual impedances. However, the insertion of large sequence impedances will induce large voltage unbalances at most system buses. The buses with sensitive loads may trip when the bus unbalances exceed certain thresholds. Ideally, these buses should have DG converters tied to them, whose controllability can be tapped for improving the bus voltage quality. To illustrate this, the example four-wire microgrid shown in Fig. 1 is considered, whose local buses are assumed to have sensitive loads tied to them. These loads are thus respectively protected by DG1 and DG2. Assuming next that only voltage unbalance at bus 1 has exceeded its threshold, only DG1 should then be selectively enabled to perform the proposed voltage compensation. This is conducted by lowering its sequence virtual impedances since they are the main causes of voltage unbalance.

On the other hand, DG2 and its protected loads will remain undisturbed since their unbalanced thresholds are not exceeded. Despite that, the voltage quality at bus 2 and the common bus are also improved slightly because of the propagating effect from bus 1. The only tradeoff according to (11) is a larger unbalanced current flowing through DG1, which must be capped. It should also be emphasized that the proposed selective scheme is decentralized with each DG detecting its own bus terminal variables for protecting its own sensitive loads against incoming disturbances. It is therefore different from the common centralized schemes [34], which detect terminal variables at the common bus and then transmit the information to the DGs through communication links.

In principle, the decentralized voltage compensation scheme can be realized by modifying the sequence virtual impedances in (12), where $R_{Vf}{}^k$ is the fixed resistance for achieving common load current sharing, and $\Delta R_V{}^k$ is the adjustable resistance for restoring voltage quality (k = − or 0).

$$\begin{cases} R_V^- = R_{Vf}^- + \Delta R_V^- \\ R_V^0 = R_{Vf}^0 + \Delta R_V^0 \end{cases} \text{ and } \begin{cases} -R_{Vf}^- \le \Delta R_V^- \le 0 \\ -R_{Vf}^0 \le \Delta R_V^0 \le 0 \end{cases} \tag{12}$$

The adjustable sequence resistances can then be regulated by detecting the voltage unbalance factors (VUFs) which are defined in [32].

$$\begin{cases} \text{VUF}^- = \dfrac{|u_o^-|}{|u_o^+|} \times 100\% \\ \text{VUF}^0 = \dfrac{|u_o^0|}{|u_o^+|} \times 100\% \end{cases} \tag{13}$$

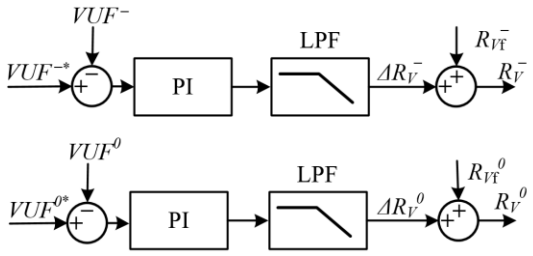


Fig. 8. Computation of sequence virtual impedances.

When the pre-defined VUF threshold at bus 1 is exceeded, the voltage compensation scheme of DG1 shown in Fig. 8 will immediately be triggered, which in the steady state, will regulate the sequence VUFs to their specified thresholds (notated with superscript *), rather than reducing them to a value lower than the thresholds. This avoids an unnecessary increase of unbalanced current through DG1, while still retaining proper operation of its sensitive loads at the specified thresholds. In this paper, the thresholds have been set to 1%~2%, which are lower than the maximum of 2%~3% permitted by IEC and ANSI C84.1-2006 [32] for electrical power systems. The outputs of Proportional-Integral (PI) controllers are then low-pass filtered to remove noise, and to intentionally slow down the computation. This is to ensure that its response time matches that of the positive-sequence droop scheme, where low-pass filters (LPFs) are also used for filtering out the average active and reactive powers. The adjustable resistances obtained from the LPFs in Fig. 8 are finally summed with the fixed resistances according to (12).

IV. Simulation Results

The overall proposed control scheme is shown in Fig. 9. It consists of a positive-sequence droop controller, a sequence virtual impedance insertion loop, and two inner (voltage and current) control loops. The inner control loops and positive-sequence droop controller are described in Section II-A and B, respectively, while the sequence virtual impedance insertion loop is described in both Section II-B and Section III. Also included in Fig. 9 is a block for extracting sequence components based on the second-order generalized integrators [33]. The control scheme is implemented in the *dq0* synchronous reference frame, and duplicated for controlling the four DGs shown in Fig. 10.

All DGs are set to have the same power ratings. This is theoretically fair since DGs with different ratings will still share the same per-unit powers after normalized with their respective ratings. As for the buses, local bus 1 is dedicated as the critical bus with a common threshold of 1% set for its negative- and zero-sequence VUFs. The other buses are less sensitive, and hence have a higher threshold of 2%. The resulting four-wire islanded microgrid is tested in Matlab/Simulink using parameters listed in Table I and a single-phase load of 6 Ω and 25.7 mH connected to the common bus.

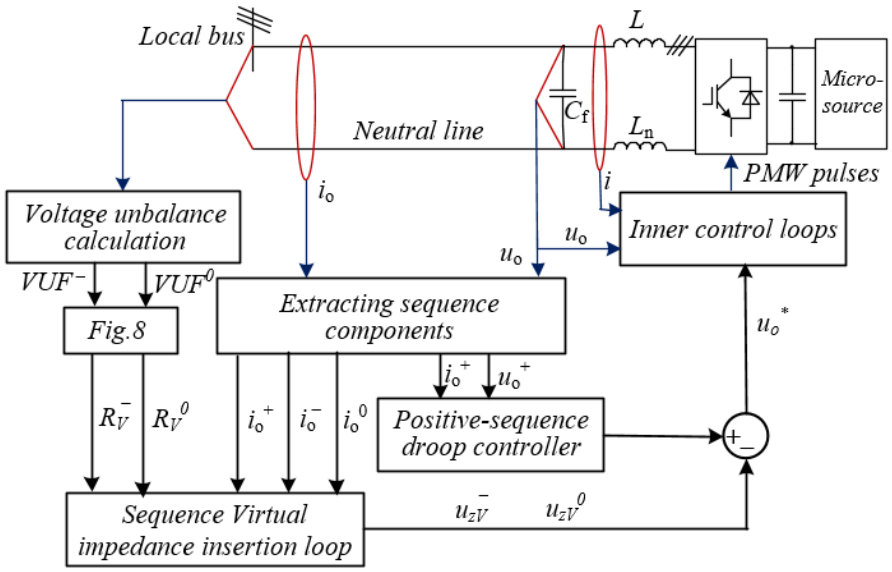


Fig. 9. Overall control of the four-leg DG converter.

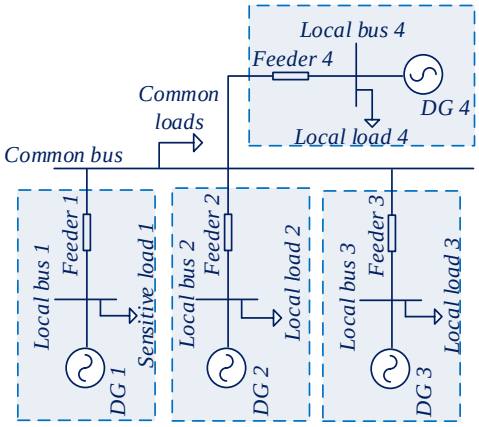


Fig. 10. Simulation diagram with proposed distributed compensation scheme.

TABLE I
SYSTEM PARAMETERS

Parameters	Symbol	Value
Nominal output voltage	E^*	220 V
Nominal output angular frequency	ω^*	100π rad/s
Filter inductance	L, L_n	2 mH, 1.2mH
Filter capacitance	C_f	12 μF
Line impedance of DG1	Z_{L1}	1 mH, 0.1 Ω
Line impedance of DG2	Z_{L2}	0.8 mH, 0.1 Ω
Line impedance of DG3	Z_{L3}	1.2 mH, 0.15 Ω
Line impedance of DG4	Z_{L4}	1.6 mH, 0.2 Ω
Voltage closed-loop	k_p, k_r	0.12, 50
	k_p^0, k_r^0	0. 2, 100
	k_i	100
	ω_c	1 rad/s
Current closed-loop	k_C	20
	k_C^0	20
Droop coefficient	m	3.14×10^{-4} rad /(W·s)
	n	0.0062 V/Var
Virtual impedance	R_v^+, L_v^+	1 Ω, 4 mH
	R_{vf}^-,	1 Ω
	R_{vf}^0	1 Ω

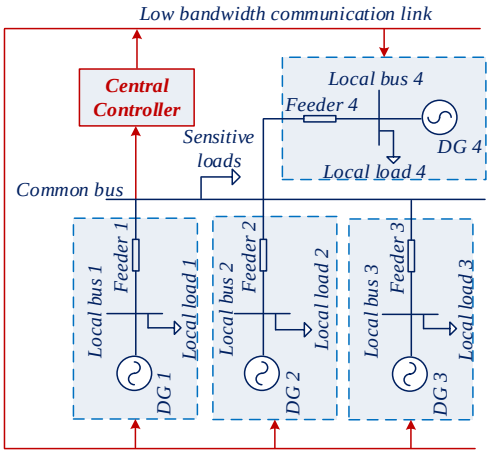
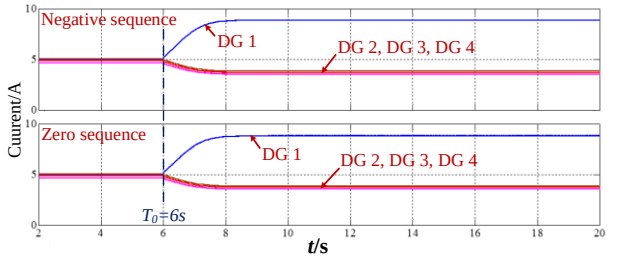


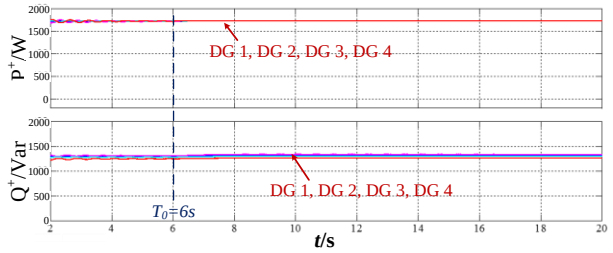
Fig. 11. Simulation diagram with existing centralized compensation scheme.

For comparison, the centralized voltage compensation scheme from [34] is also simulated. Its overview is shown in Fig. 11, where a centralized controller can clearly be seen. The centralized controller measures voltage of the common bus, and then transmits the compensation references to the DGs. Communication links are therefore needed since the DGs are located far apart. Although the DGs are still realizing the compensation, the main decision management has been dedicated to the centralized controller. Each DG is also not selectively enabled for protecting its local bus. Instead, they are jointly enabled for protecting the common bus monitored by the centralized controller. The proposed decentralized scheme is thus different from the most existing centralized schemes including that in [34].

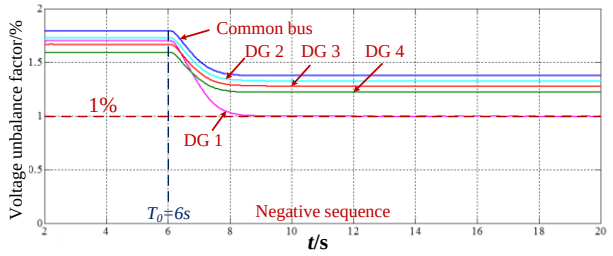
With the proposed scheme first simulated, results obtained from it are presented in Fig. 12. In particular, Fig. 12(a) shows all DGs in the common current sharing mode before T_0 = 6 s. Their generated currents are thus equal at the expense of voltage unbalance detected in Fig. 12(c) and (d). As previously explained, this is created by the large inserted sequence impedances as shown in Fig. 12(e). After T_0 = 6 s, the conditions change with DG1 now activated to perform voltage



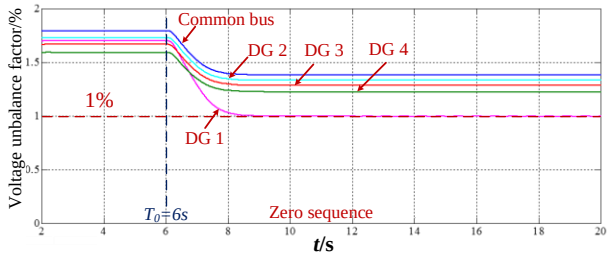
(a)



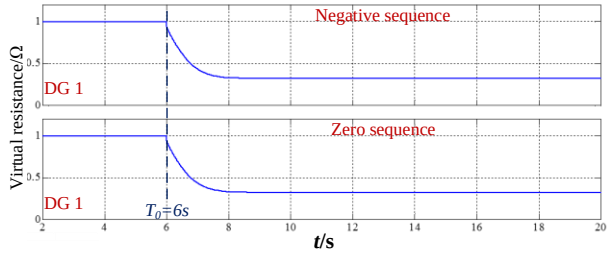
(b)



(c)



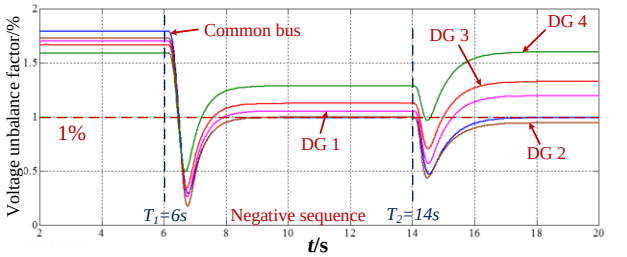
(d)



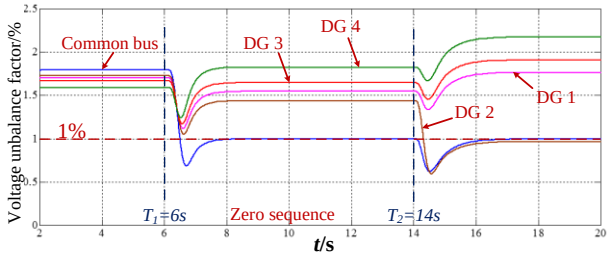
(e)

Fig. 12. Simulation results for four DGs using the proposed control scheme. (a) negative- and zero-sequence components of output currents, (b) positive sequence active and reactive powers, (c) negative-sequence VUFs of all buses, (d) zero-sequence VUFs of all buses, and (e) virtual impedance values.

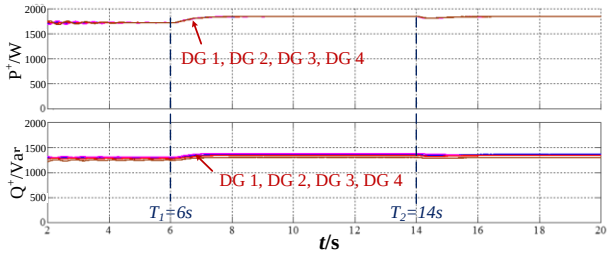
compensation. As seen from Fig. 12(a), DG1 now carries more sequence currents with the remaining shared equally among the other DGs. The bus voltage quality of DG1 has therefore improved, as verified by the regulation of VUFs at 1% from T_0 = 6 s onwards. This can clearly be seen in Fig. 12(c) and (d),



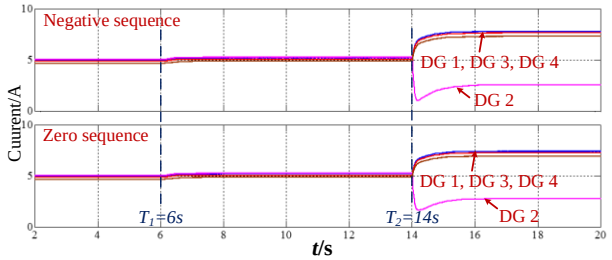
(a)



(b)



(c)



(d)

Fig. 13. Simulation results for four DGs using existing centralized control scheme. (a) negative-sequence VUFs of all buses, (b) zero-sequence VUFs of all buses, (c) positive-sequence active and reactive powers, and (d) negative- and zero-sequence output currents.

and is caused by the intentional lowering of sequence virtual impedances shown in Fig. 12(e).

Although not intentional, voltage qualities of the common and other local buses are also improved because of the lower negative- and zero-sequence currents flowing through lines connecting them. Moreover, during the simulated time, all DGs share the positive-sequence active and reactive powers equally, as shown in Fig. 12(b). This is expected since they use the same P^+–f and Q^+–V droop controllers and positive-sequence virtual impedances. The effect of unbalance compensation on positive-sequence power sharing is therefore negligible or fully decoupled.

Simulation results for the centralized scheme are next presented in Fig. 13 using the same parameters and enabling conditions as Fig. 12. The latter means the centralized voltage

compensation only begins from T_1 = 6 s onwards. Fig. 13(a) and (b) show the VUFs captured for the common and local buses. It can clearly be seen that the VUFs of the common bus have been lowered to 1%, but not those of the local buses since they are not directly controlled. The local VUFs are, in fact, higher due to voltage drops across lines connecting the common and local buses. Equal power sharing feature of the DGs is not affected as shown in Fig. 13(c). The same uniform sharing can also be observed with the negative- and zero-sequence currents in Fig. 13(d), which certainly, is expected since all DGs have been enabled for voltage compensation, rather than selectively.

Another feature of the centralized scheme is its reliance on communication links, which can usually be burdened by time delays. Effects of this reliance are illustrated in Fig. 13(a) and (b), where large transient overshoots of VUFs can be seen even though the same settling time as Fig. 12 has been used. The impact is even greater after communication signals to DG2 are lost from T_2 = 14 s onwards in Fig. 13. When that happens, DG2 carries lesser negative- and zero-sequence currents, and its VUFs have been lowered. However, the VUFs of the other local buses have risen noticeably with zero-sequence VUF of DG4 rising above 2% in Fig. 13(b) (highest local threshold set for the decentralized scheme).

In contrast to the centralized control methods, the proposed decentralized scheme is thus less prone to unexpected conditions caused by communication faults. The regulation is smoother and voltage quality of all the buses can be improved to some extent. It also offers more selective voltage compensation to the loads, which like the DGs, should mostly be distributed rather than concentrated at the common bus.

V. Experimental Results

Following the simulation study, an experimental setup is developed for validating the proposed control scheme shown in Fig. 9. It has two 12-kVA four-leg converters with *LCL* filters for emulating the two DGs in Fig. 1. Their control schemes are implemented with two *TMS320F28335* digital signal processors (DSPs), whose control parameters and other system parameters are in accordance with the previous simulation, as listed in Table I. The experiment setup has a single-phase 12-Ω resistive load connected, which will definitely cause unbalanced currents to flow. To share these unbalanced currents effectively, both negative- and zero-sequence virtual resistances inserted have been set to 1 Ω. Corresponding results obtained are shown from Figs. 15 to 17.

In particular, it can be observed from Fig. 15 that output currents of both DGs are similar before the time instant of *T1* (only two phase currents from each DG are shown in Fig. 15(a) and (c) since the third phase current is the same as the smaller phase current shown in each of the figures). This is expected since both DGs are in their common current sharing mode. After *T1*, DG1 carries more current than DG2 since its voltage compensation functionality has been activated as shown in Fig. 15. Phase A and B currents generated by the DGs are also no longer zero even though no load has been connected to these two phases. In terms of their sequence components, Fig. 15(b) and (d) show an increase in negative- and zero-sequence currents through DG1, while those through DG2 decrease. Carrying lesser sequence currents, phase currents of DG2 will then have closer magnitudes, which certainly, is the case observed from Fig. 15(a) and (c) after *T1*.

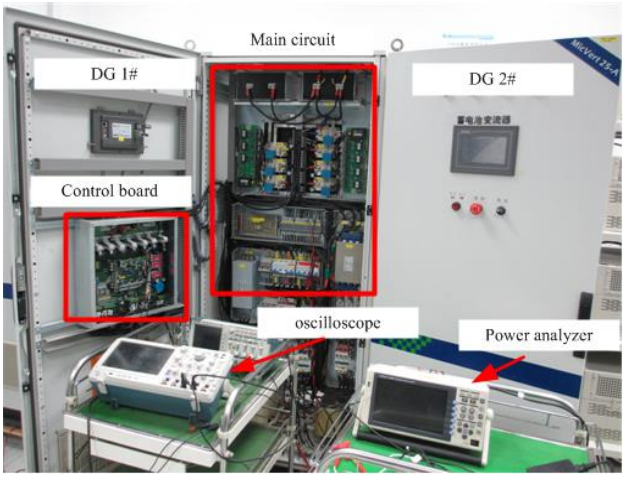


Fig. 14. Photograph of the experimental setup.

The voltage quality improvement can be seen by comparing Fig. 16(a) with the unbalanced RMS bus voltages of 223 V, 223.7 V and 210.3 V before *T1*, and Fig. 16(b) with the improved RMS bus voltages of 220 V, 220.7 V and 214.7 V after *T1*. The improvement in bus voltages can also be seen in Fig. 17(a), where the computed VUF^- and VUF^0 have dropped from 1.5% to 1% and 2.6% to 1%, respectively, after *T1*. Again, the voltage quality improvement is achieved by lowering sequence virtual impedances of DG1 selectively, as shown in Fig. 17(b).

VI. Conclusion

A control scheme with common load current sharing and selective bus voltage enhancement has been presented for regulating the four-leg DGs used in an islanded four-wire microgrid. The control scheme achieves common current sharing by inserting negative- and zero-sequence virtual impedances, in addition to the usual positive-sequence impedance inserted with a droop controller. Making these sequence impedances tunable further allows the DGs to perform selective voltage compensation when the VUF thresholds of local buses have been exceeded. Instead of nullifying the VUFs of the concerned buses, the enabled DGs maintain them at their thresholds, which can help to limit currents passing through the enabled DGs, while protecting their sensitive loads. Simulation and experimental results have verified the effectiveness of the proposed scheme when compared with an existing centralized scheme.

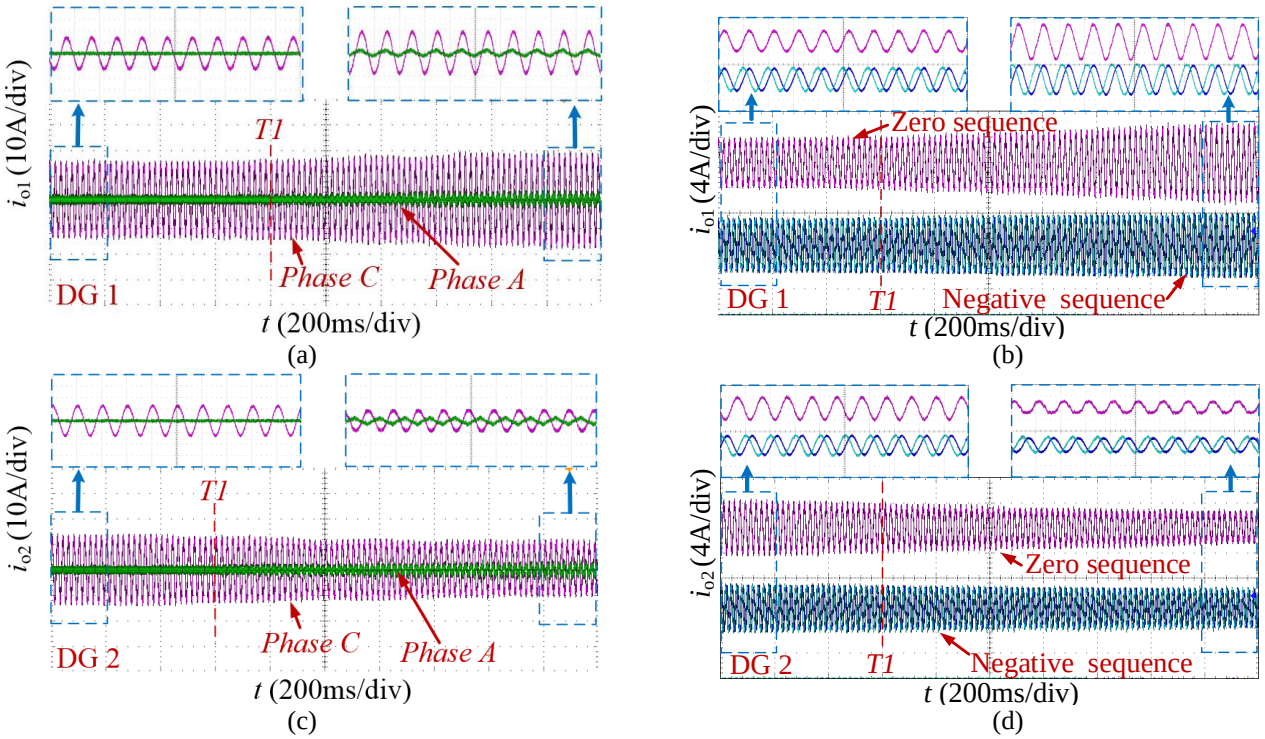


Fig. 15. Experimental (a) phase output currents of DG1, (b) negative- and zero-sequence output currents of DG1, (c) phase output currents of DG2, and (d) negative- and zero-sequence output currents of DG2.

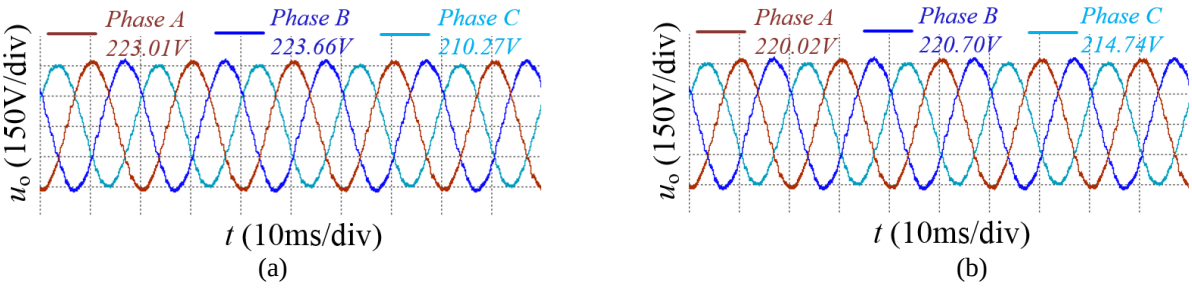


Fig. 16. Experimental bus voltages (a) before and (b) after voltage compensation.

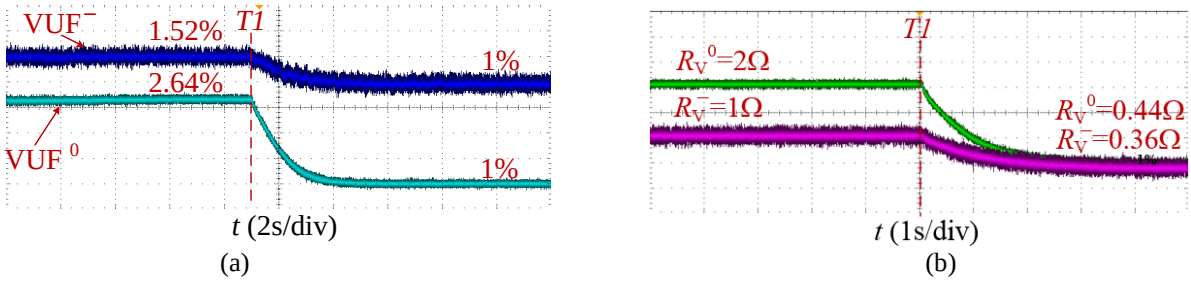


Fig. 17. Experimental results for DG1. (a) VUFs, (b) Virtual impedances.

VII. References

[1] H. Farhangi, "The path of the smart grid," *IEEE Power Energy Mag.*, vol. 8, no. 1, pp. 18-28, Jan./Feb. 2010.

[2] H. Nikkhajoei and R. H. Lasseter, "Distributed generation interface to the CERTS microgrid," *IEEE Trans. Power Del.*, vol. 24, no. 3, pp. 1598 - 1608, Jul. 2009.

[3] J. Rocabert, A. Luna, F. Blaabjerg, P. Rodriguez, "Control of power converters in ac microgrid," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4734-4749, Nov. 2012.

[4] Y. W. Li, D. M. Vilathgamuwa, P. C. Loh, "Microgrid power quality enhancement using a three-phase four-wire grid-interfacing compensator," *IEEE Trans. Ind. Appl.*, vol. 41, no. 6, pp. 1707-1719, Nov./Dec. 2005.

[5] F. Wang, J. L. Duarte and M. A. M. Hendrix, "Grid-interfacing converter systems with enhanced voltage quality for microgrid application-concept and implementation," *IEEE Trans. Power Electron.*, vol. 26, no.12, pp. 3501-3513, Dec. 2011.

[6] C. K. Sao and P. W. Lehn, "Autonomous load sharing of voltage source converters," *IEEE Trans. Power Del.*, vol. 20, no. 2, pp. 1009-1016, Apr. 2005.

[7] R. Majumder, G. Ledwich, A. Ghosh, S. Chakrabarti and F. Zare, "Droop control of converter-Interfaced microsources in rural distributed generation," *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 2768-2778, Oct. 2010.

[8] J. M. Guerrero, J. Matas, X. F. de Vicu, L. G. A, M. Castilla, J. Miret, "Wireless-control strategy for parallel operation of distributed-generation inverters," *IEEE Trans. Ind. Electron.*, vol. 26, no.5, pp. 1461-1470, Oct. 2006.

[9] Q. C. Zhong, "Robust droop controller for accurate proportional load sharing among inverters operated in parallel," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1281-1290, Apr. 2013.

[10] X. Wang, F. Blaabjerg and Z. Chen, "An improved design of virtual output impedance loop for droop-controlled parallel three-phase voltage source inverters," *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2012 pp. 2466-2473.

[11] D. De, V. Ramanarayanan, "Decentralized parallel operation of inverters sharing unbalanced and nonlinear loads," *IEEE Trans. Power Electron*., vol. 25, no. 12, pp. 3015-3025, Dec. 2010.

[12] P. Lohia, M. K. Mishra, K. Karthikeyan, and K. Vasudevan, "A minimally switched control algorithm for three-phase four-leg VSI topology to compensate unbalanced and nonlinear load," *IEEE Trans. Power Electron*., vol. 23, no. 4, pp. 1935-1944, Jul. 2008.

[13] A. Garcia-Cerrada, O. Pinzon-Ardila, V. Feliu-Batlle, P. Roncero-Sanchez, P. Garcia-Gonzalez, "Application of a repetitive controller for a three-phase active power filter," *IEEE Trans. Power Electron*., vol. 22, no.1 pp. 237-246, Jan. 2007.

[14] F. Barrero, S. Martínez, F. Yeves, F. Mur, P. M. Martínez, "Universal and reconfigurable to UPS active power filter for line conditioning," *IEEE Trans. Power Del*., vol. 18, no. 1, pp. 283-290, Jan. 2003.

[15] T. L. Li, S. H. Hu, Y. H. Chan, "D-STATCOM with positive-sequence admittance and negative-sequence conductance to mitigate voltage fluctuations in high-level penetration of distributed-generation systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4 pp. 1417-1428, 2013.

[16] G. Chen, M. Zhu, X. Cai, "Medium-voltage level dynamic voltage restorer compensation strategy by positive and negative sequence extractions in multiple reference frames," *IET Power Electron*., vol. 7, no. 7, pp. 1747-1758, 2014.

[17] I. Axente, J. N. Ganesh, M. Basu, M. F. Conlon, K. Gaughan, "A 12-kVA DSP-controlled laboratory prototype UPQC capable of mitigating unbalance in source voltage and load current," *IEEE Trans. Power Electron*., vol. 25, no. 6, pp. 1471-1479, Jun. 2010.

[18] G. Joos, B. T. Ooi, D. McGillis, F. D. Galiana, R. Marceau, "The potential of distributed generation to provide ancillary services," *IEEE Power Eng. Soc. Summer Meeting*, Jun., 2000, pp. 1762-1767.

[19] G. Azevedo, P. Rodriguez, J. Rocabert, M. Cavalcanti, F. Neves, "Voltage quality improvement of microgrids under islanding mode," *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2010, pp. 3169-3173.

[20] F. Wang, H. Mao, D. Xu, Y. Ruan, "Negative-sequence admittance control scheme for distributed compensation of grid voltage unbalance," *Control and Modeling for Power Electronics (COMPEL)*, 2012, pp. 1-8.

[21] P. T. Cheng, C. A. Chen, T. L. Lee, S. Y. Kuo, "A cooperative imbalance compensation method for distributed-generation interface converters," *IEEE Trans. Ind. Appl.*, vol. 45, no. 2, pp. 805-815, Feb. 2009.

[22] M. Savaghebi, A. Jalilian, J. C. Vasquez. J. M. Guerrero, "Autonomous voltage unbalance compensation in an islanded droop-controlled microgrid," *IEEE Trans. Ind. Appl.*, vol. 60, no. 4, pp. 1390-1402, Apr. 2013.

[23] Q. W. Liu, Y. Tao, X. H. Liu, Y. Deng, X. N. He, "Voltage unbalance and harmonics compensation for islanded microgrid inverters," *IET Power Electron*., vol. 7, no. 5, pp. 1055-1063, 2014.

[24] M. Rivera, V. Yaramasu, A. Llor, J. Rodriguez, B. Wu, M. Fadel, "Digital predictive current control of a three-phase four-leg inverter," *IEEE Trans. Ind. Appl.*, vol. 60, no. 11, pp. 4903-4912, Nov. 2013.

[25] A. Lidozzi, G. L. Calzo, L. Solero, F. Crescimbini, "Integral-resonant control for stand-alone voltage source inverters, " *IET Power Electron*., vol. 7, no. 2, pp. 271-278, Feb. 2014.

[26] B. Singh, S. Sharma, "Design and implementation of four-leg voltage-source-converter-based VFC for autonomous wind energy conversion system," *IEEE Trans. Ind. Electron.*, vol. 59, no. 12, pp. 4694-4703, Dec. 2012.

[27] R. Zhang, V. H. Prasad, D. Boroyevich, F. C. Lee, "Three-dimensional space vector modulation for four-leg voltage-source converter," *IEEE Trans. Power Electron*., vol. 17, no. 3, pp. 314-326, May 2002.

[28] I. Vechiu, O. Curea, H. Camblong, "Transient operation of a four-leg inverter for autonomous applications with unbalanced load," *IEEE Trans. Power Electron.*, vol. 25, no. 2, pp. 399-407, Feb. 2010.

[29] J. Matas, M. Castilla, X. F. de Vicu, L. G. A, J. Miret, J. C. Vasquez, "Virtual impedance loop for droop-controlled single-phase parallel inverters using a second-order general-integrator scheme," *IEEE Trans. Power Electron*., vol. 25, no. 12, pp. 2993-3002, Dec. 2010.

[30] J. W. He, Y. W. Li, "Analysis, design, and implementation of virtual impedance for power electronics interfaced distributed generation," *IEEE Trans. Ind. Appl.*, vol. 47, no. 6, pp. 2525-2538, Nov./Dec. 2011.

[31] M. Savaghebi, A. Jalilian, J. C. Vasquez, J. M. Guerrero, "Secondary control scheme for voltage unbalance compensation in an islanded droop-controlled microgrid," *IEEE Trans. Smart Grid*, vol. 3, no.2 pp. 797-807, Jun. 2012.

[32] A. V. Jouanne, B. Banerjee, "Assessment of voltage unbalance," *IEEE Trans. Power Del*., vol. 16, no. 4, pp. 782-790, Oct. 2001.

[33] P. Rodriguez, A. V. Timbus, R. Teodorescu, M. Liserre, F. Blaabjerg, "Flexible active power control of distributed power generation systems during grid faults," *IEEE Trans. Ind. Electron.*, vol. 54 no. 5, 2583-2592, Oct. 2007.

[34] F.Tang, X. Zhou, L. X. Meng, Josep M. Guerrero and J. C. Vasquez, "Secondary Voltage Unbalance Compensation for Three-Phase Four-Wire Islanded Microgrids," IEEE 11th International Multi-Conference on Systems, Signals & Devices (SSD), 2014 pp.1-5.