# Ultrahigh Step-up DC-DC Converter for Distributed Generation by Three Degrees of Freedom (3DoF) Approach 

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#### Abstract

This paper proposes a novel dc-dc converter topology to achieve an ultrahigh step-up ratio while maintaining a high conversion efficiency. It adopts a three degree of freedom approach in the circuit design. It also demonstrates the flexibility of the proposed converter to combine with the features of modularity, electrical isolation, soft-switching, low voltage stress on switching devices, and is thus considered to be an improved topology over traditional dc-dc converters. New control strategies including the two-section output voltage control and cell idle control are also developed to improve the converter performance. With the cell idle control, the secondary winding inductance of the idle module is bypassed to decrease its power loss. A 400-W dc-dc converter is prototyped and tested to verify the proposed techniques, in addition to a simulation study. The step-up conversion ratio can reach 1:14 with a peak efficiency of $\mathbf{9 4 \%}$ and the proposed techniques can be applied to a wide range of high voltage and high power distributed generation and dc power transmission.


Index Terms-Boost converter, control strategy, dc-dc power conversion, degrees of freedom (DoF), high step-up converter, modularization.

## I. Introduction

DISTRIBUTED generation is playing an increasingly important role in reducing greenhouse gas emissions and improving the quality of human lives. In these systems, power converters are a key component to control power flow within the system. In particular, high step-up dc-dc converters are widely used in solar power generation, fuel cells, electric vehicles and uninterrupted power supplies [1]-[13]. The features of dc-dc conversion are also essential to off-shore wind power transmission through high voltage dc (HVDC) power systems [14], [15].

[^0]In these applications, high voltage gain and high conversion efficiency of dc-dc converters are highly desirable.

When isolated topologies are utilized, a high voltage gain is traditionally achieved by manipulating the transformer's turns ratio, the pulse width modulation duty ratio or phase-angle shift. The duty ratio of high-frequency switching devices is often considered as one design freedom while the turns ratio of transformers is another [16]-[28]. When both are employed to achieve a high voltage conversion ratio, it is termed the two degrees of freedom (2DoF) design [17], [21], [23]. Furthermore, soft switching can also be a useful feature when an active or passive clamping circuit is implemented [4]-[6]. An active clamping circuit consists of one active switching device and one clamping capacitor, while a passive clamping circuit uses some passive switching devices (e.g., diodes) for the same purpose. In theory, the leakage inductance is proportional to the square of the turns ratio [29]. As a result, a very high turns ratio is generally avoided in the transformer design since it can reduce the efficiency of the transformer. A typical topology of high step-up converters uses only one switching device [30], [31] while their converter ratings are low. Due to the size of capacitors, the power density of these converters decreases as the voltage gain increases [32]-[34]. In the literature, some high step-up conversion ratios are also reported by combining the features of turns ratio, multilevel and duty ratio in the converter design [35]-[41]. For instance, paper [41] integrates a coupled inductor with a switching capacitor in the high step-up converter using one switching device. The input-parallel output-series structure can also provide a high voltage gain and a high power level [42], [43]. In paper [42], coupled inductors are used to achieve a high voltage gain but electrical isolation is absent. Alternatively, the use of a cascaded converter structure can provide a high voltage gain [44], [45]. However, the topology in [44] is limited in converter power ratings due to the high current in the switching devices. In order to increase the power level, a modular multilevel converter is presented in [45] but it can only regulate the duty ratio and cell number (i.e., 2DoF). Clearly, these reported topologies do not provide electrical isolation and sufficient flexibility for further expansion.

The voltage gain of a typical 2DoF converter is expressed as follows:

$$
\begin{equation*}
G=\frac{2 N}{1-D} \tag{1}
\end{equation*}
$$

where $N$ is the turns ratio and $D$ is the duty ratio.


Fig. 1. DC-DC converter topologies with flyback-forward cells. (a) Typical flyback-forward converter [6]. (b) Proposed flyback-forward dc-dc converter (using two cells).

Obviously, a small change in the duty ratio can lead to a significant change in the voltage gain. This poses a challenge to the converter control so that the accurate regulation of the output voltage becomes difficult. To tackle the problem, this paper proposes a novel ultrahigh step-up dc-dc converter, which utilizes the features of modularity, multilevels and electrical isolation. In effect, this is a three degree of freedom (3DoF) design of dc-dc converters.

## II. Proposed 3DoF Converter Topology

A conventional interleaved flyback-forward dc-dc converter is presented in Fig. 1(a). The voltage gain can be found by

$$
\begin{equation*}
G=\frac{V_{\text {out }}}{V_{\text {in }}}=\frac{2 N}{1-D} \cdot \frac{1}{1+\sqrt{\frac{2 L_{\mathrm{LK}} \cdot f_{s}}{(1-D)^{2} R}}} \tag{2}
\end{equation*}
$$

where $L_{\mathrm{LK}}$ is the leakage inductance, $f_{s}$ is the switching frequency, and $R$ is the load resistance. Clearly, the voltage gain is determined by the leakage inductance of the coupled inductor, switching frequency, load resistance, in additional to turns ratio and duty ratio.

If the secondary side of the flyback-forward dc-dc converter is seen as a cell, more cells can be added up in series, as shown in Fig. 1(b). By doing so, a multilevel output voltage can be obtained. The corresponding voltage gain in an idea condition is given by

$$
\begin{equation*}
G=\frac{2 m \cdot N}{1-D} \tag{3}
\end{equation*}
$$

where $m$ denotes the number of voltage levels.
This paper develops a two-cell high step-up dc-dc converter as an example and its topology is shown in Fig. 1(b), where $S_{1}-S_{4}$ are four main switches. Active clamping circuits including clamp switches $S_{c 1}-S_{c 4}$ and clamping capacitors $C_{c 1}-C_{c 4}$ are employed to limit the voltage stress on the main switches.


Fig. 2. Waveforms of the proposed converter.
Four coupled inductors $L_{1}-L_{4}$ are used to form two power cells ( $L_{1}$ and $L_{2}$ for cell-1, $L_{3}$ and $L_{4}$ for cell-2). The primary and secondary winding turns for the four coupled inductors are represented by $n_{1}$ and $n_{2}$, respectively, and their turns ratio is $N=$ $n_{2} / n_{1}$. The coupling references are remarked with "*", "O", "I" and "■". $L_{\mathrm{LK} 1}-L_{\mathrm{LK} 4}$ are the leakage inductances for coupled inductors $L_{1}-L_{4}$, respectively. In this figure, the rectifier diodes $D_{o 1}-D_{o 2}$ and the output capacitors $C_{1}-C_{2}$ also form a voltage-doubling rectifier circuit.

The proposed converter is built on basic cells; each of them consists of two coupled inductors and a power switch. Typical steady-state waveforms of this converter are shown in Fig. 2. The active clamping switches $S_{C 1}-S_{C 4}$ are complementary to the main switches $S_{1}-S_{4}$, respectively. The outputs of cell-1 and cell-2 are $V_{\text {cell-1 }}$ and $V_{\text {cell-2 }}$, respectively. The switches $S_{1}-S_{4}$ can be regulated by earthier duty ratio control or phase angle shift control. The waveforms of $V_{\text {cell-1 }}$ and $V_{\text {cell-2 }}$ are identical.

The proposed converter has eight operational stages, as shown in Fig. 3.

State $1\left[t_{0}-t_{1}\right]$ : During this stage, $S_{1} \sim S_{4}$ are turned on and the corresponding clamping switches are OFF. All the coupled inductors operate in flyback mode to store energy. The outputs of cell-1 and cell-2 are zero and the output rectifier diodes are both reverse-biased. The output capacitors $C_{01}$ and $C_{02}$ supply the energy to the load.
State $2\left[t_{1}-t_{2}\right]$ : At $t_{1}, S_{2}$ and $S_{4}$ receive a turn-off gate signal, increasing their drain-source voltage across the parasitic capacitor of the main switches in an approximate linear manner.

(d)

(e)

(f)

(g)

(h)

Fig. 3. Eight operational stages of the proposed converter (using two cells). (a) State $1\left[t_{0}-t_{1}\right]$. (b) State $2\left[t_{1}-t_{2}\right]$. (c) State $3\left[t_{2}-t_{3}\right]$. (d) State $4\left[t_{3}-t_{4}\right]$. (e) State $5\left[t_{4}-t_{5}\right]$. (f) State $6\left[t_{5}-t_{6}\right]$. (g) State $7\left[t_{6}-t_{7}\right]$. (h) State $8\left[t_{7}-t_{8}\right]$.


Fig. 4. Phase-angle shift control.

(a)

(b)

Fig. 5. Output voltage with the phase-angle shift control. (a) 0.66 duty ratio. (b) 0.33 duty ratio.

Due to the low parasitic capacitance and the large current in the primary coupled inductor, this period is very short.
State $3\left[t_{2}-t_{3}\right]$ : At $t_{2}$, the drain-source voltage of $S_{2}$ and $S_{4}$ increases to conduct the output rectifier diodes $D_{o 2}$. During this interval, $L_{1}$ (in cell-1) and $L_{3}$ (in cell-2) operate in forward mode while $L_{2}$ and $L_{4}$ in a flyback mode to transfer energy to the load.
State $4\left[t_{3}-t_{4}\right]$ : In this stage, the voltage across the parasitic capacitor of $S_{2}$ and $S_{4}$ increases to the corresponding voltage of clamp capacitors $C_{c 2}$ and $C_{c 4}$, the antiparallel diodes of $S_{c 2}$ and $S_{c 4}$ begin to conduct.


Fig. 6. Schematic diagram of the proposed control strategy.

State $5\left[t_{4}-t_{5}\right]$ : At $t_{4}, S_{c 2}$ and $S_{c 4}$ are switched on with zerovoltage switching (ZVS). Then, a current flows in the antiparallel diode. During this interval, cell-1 and cell-2 provide a continuous current to the load, i.e.,

$$
\begin{equation*}
i_{\mathrm{LK} 1}(t)=\frac{N \cdot V_{C c 2}+N \cdot V_{C c 4}-V_{C o 1}}{L_{\mathrm{LK} 1}+L_{\mathrm{LK} 2}+L_{\mathrm{LK} 3}+L_{\mathrm{LK} 4}} \cdot\left(t-t_{4}\right) \tag{4}
\end{equation*}
$$

where $V_{C c 2}$ and $V_{C c 4}$ are the voltage across capacitors $C_{c 2}$ and $C_{c 4}$, respectively.
State $6\left[t_{5}-t_{6}\right]$ : At $t_{5}, S_{c 2}$ and $S_{c 4}$ receive a turn-off signal. Because of the parallel capacitors $C_{s 2}$ and $C_{s 4}$, the voltage across $S_{2}$ and $S_{4}$ decreases in an approximately linear manner and that in $S_{c 2}$ and $S_{c 4}$ increases nearly linearly. Over this period, $S_{c 2}$ and $S_{c 4}$ are turned off with ZVS.
State $7\left[t_{6}-t_{7}\right]$ : At $t_{6}$, the drain-source voltage of $S_{2}$ and $S_{4}$ decrease to zero owing to the capacitor-inductance resonant. Then, the corresponding antiparallel diode conducts.
State $8\left[t_{7}-t_{8}\right]$ : At $t_{7}, S_{2}$ and $S_{4}$ turn on with ZVS. The leakage currents of cell-1 and cell-2 decrease to zero and $D_{02}$ turns off with zero-current switching (ZCS). The following equations can be obtained:
$i_{\mathrm{LK} 1}(t)=I_{\mathrm{LK}}\left(t_{5}\right)-\frac{V_{C o 1}}{L_{\mathrm{LK} 1}+L_{\mathrm{LK} 2}+L_{\mathrm{LK} 3}+L_{\mathrm{LK} 4}}\left(t-t_{5}\right)$
$I_{\mathrm{LK}}\left(t_{5}\right)=\frac{N \cdot V_{C c 2}+N \cdot V_{C c 4}-V_{C o 1}}{L_{\mathrm{LK} 1}+L_{\mathrm{LK} 2}+L_{\mathrm{LK} 3}+L_{\mathrm{LK} 4}}(1-D) T_{s}$
$t_{8}-t_{5}=\frac{N \cdot V_{C c 2}+N \cdot V_{C c 4}-V_{C o 1}}{V_{C o 1}}(1-D) T_{s}$.
During the period $t_{2}-t_{8}$, the electrical charge on the secondary side of cell-1 and cell-2 is given by

$$
\begin{align*}
Q_{C o 1} & =\frac{1}{2} \cdot I_{\mathrm{LK} 1}\left(t_{5}\right) \cdot\left(t_{8}-t_{2}\right) \\
& =\frac{\left(N \cdot V_{C c 2}+N \cdot V_{C c 4}-V_{C o 1}\right)^{2}}{2 \cdot V_{C o 1} \cdot\left(L_{\mathrm{LK} 1}+L_{\mathrm{LK} 2}+L_{\mathrm{LK} 3}+L_{\mathrm{LK} 4}\right)}(1-D)^{2} \cdot T_{s}^{2} . \tag{8}
\end{align*}
$$

Because of the symmetrical structure, the charging and discharging processes during $t_{8}-t_{16}$ are identical to these during $t_{0}-t_{8}$.

## III. Steady-State Analysis

In order to simplify the analysis of the proposed converter, the following assumptions are made: 1) all the four coupled


Fig. 7. Waveforms of the shielding control under modular power cell idle conditions.


Fig. 8. Equivalent circuit of the idle modular power cell.
inductors are identical; 2) all the clamping capacitors are identi$\mathrm{cal} ; 3$ ) the voltage of the clamping capacitors is constant; and 4) the dead-time between the main switches and clamping switches is neglected.

## A. Voltage Stress

The voltage stress on switching devices is equal to the voltage across the clamping capacitors

$$
\begin{equation*}
V_{D S i}=V_{C c i}=\frac{V_{\mathrm{in}}}{1-D} \tag{9}
\end{equation*}
$$

where $V_{C c i}$ is the voltage of the active clamping switch, $V_{D S i}$ is the voltage of the main switch, and $V_{\mathrm{in}}$ is the input voltage. According to the symmetrical waveforms of $V_{\mathrm{ab}}$, the voltage stress on the output diodes can be found by

$$
\begin{equation*}
V_{c o 1}=V_{c o 2}=V_{\text {out }} \tag{10}
\end{equation*}
$$

## B. Voltage Gain

However, the leakage inductance of the coupled inductor can also impact on the voltage gain. In a two-level high step-up converter, the electrical charge of $C_{o 1}$ is half of the total electrical charge due to the symmetry of the rectifier circuit

$$
\begin{equation*}
Q_{C o 1}=\frac{1}{2} \cdot \frac{V_{\text {out }}}{R} \cdot T_{s} \tag{11}
\end{equation*}
$$



Fig. 9. Simulation results for the cell idle control.


Fig. 10. Three DoF converter with the interleaved structure.

From (8), (9), and (11), the voltage gain can be expressed as

$$
\begin{equation*}
G=\frac{4 \cdot N}{1-D+\sqrt{\frac{2 \cdot f_{s} \cdot\left(L_{\mathrm{LK} 1}+L_{\mathrm{LK} 2}+L_{\mathrm{LK} 3}+L_{\mathrm{LK} 4}\right)}{R}}} \tag{12}
\end{equation*}
$$

where $R$ is the load resistance.
Due to the series connection of the secondary side of the high step-up power cells, the turns ratios of the coupled inductors in power cells can be different. Under normal conditions, the total voltage gain of $M$ cells is

$$
\begin{equation*}
G=\frac{2 \cdot\left(\sum_{i=1}^{m} N_{i}\right)}{1-D+\sqrt{\frac{2 \cdot f_{s} \cdot\left(\sum_{i=1}^{m} L_{L K i}\right)}{R}}} \tag{13}
\end{equation*}
$$

where $N_{i}$ is the turns ratio of the $i$ th cell and $L_{L k i}$ is the leakage inductance of the $i$ th cell.

## C. Soft Switching

Soft switching of power devices can reduce the switching power loss and thus improve the energy efficiency of the converter. In order to realize ZVS for the clamp switches, the antiparallel diodes of clamp switches should conduct prior to


Fig. 11. Simulation results for the 3 DoF with the interleaved structure. (a) Output voltage and winding arm output. (b) Voltage and current of the primary switching devices.
the turn-on of the switches. For the main switches, the energy stored in parasitic capacitors should be lower than that stored in the leakage inductor. The ZVS turn-on condition for the main switches is

$$
\begin{equation*}
\frac{1}{2} \frac{L_{L K i}}{N_{i}^{2}} I_{i}^{2} \geq \frac{1}{2} C_{D S i} V_{D S i}^{2} \tag{14}
\end{equation*}
$$

where $I_{i}$ is the primary input current of the power step-up cell and $C_{D S i}$ is the parasitic capacitor voltage.


Fig. 12. Three DoF converter with the input-parallel output-series structure.

Owing to the series connection of the secondary side of high step-up power cells, the leakage inductance can be easily increased for soft switching at the expense of the voltage gain, as presented in (12).

## IV. Control Strategies for the Proposed Converter

There are two control strategies developed to control the output voltage of the proposed converter: the two-section output voltage control and the module idle control.

## A. Two-Section Output Voltage Control

In the proposed converter, the output voltage is built up by connecting several voltage sources in series, similar to Fig. 1(b). Therefore, the total voltage gain is the sum of individual cells. The output voltage of $m$ cells includes two parts: the output voltage of $m-1$ cells, and power cell $m$ (used for minor adjustment of the output voltage to limit the duty ratio change).

Moreover, the phase-angle shift with respect to the turn-on signal of $S_{1}$ (see Fig. 2) can be employed to adjust the output voltage of each cell. This has two conditions: controllable and uncontrollable, as illustrated in Fig. 4. The output voltage control under $D \geq 0.5$ and $D<0.5$ is further presented in Fig. 5. At a shift angle of $180^{\circ}$, the output voltage peaks. In the power cell,


Fig. 13. Proposed 3DoF converter for high power and high voltage-gain output.
the two main switches are usually of $180^{\circ}$ shift angle, which is in an uncontrollable range, as shown in Figs. 4 and 5. When all cells use the same duty ratio, the phase-angle shift can be employed to control the converter output voltage.

Fig. 6 illustrates the proposed converter control strategy. $\Delta V_{\mathrm{ref}}$ is the threshold value of voltage error. For a given voltage error, major and minor adjustments can be decided. If a major adjustment is needed, all the high step-up power cells are involved and a new duty ratio is assigned. In a minor adjustment, only the $m$ th power cell is involved. If the voltage error is positive, the duty ratio of associated main switches needs to be increased. When the voltage error is negative, the phase-angle shift is employed to control the output voltage.

## B. Cell Idle Control

In the proposed topology, power cell idle conditions can be employed to adjust the voltage gain. If the primary main switching devices are idle, the secondary winding inductor changes from an alternating square voltage source to an inductor. Since the secondary windings of the coupled inductor are series connected; the winding inductance of the idle power cell blocks the current, which is generated from other cells. In this paper, a shielding control strategy is developed for idle power cells by controlling the coupled inductor output with reverse polarity. It is needed to send a turn-off signal to the main switching devices and a turn-on signal to the idle power cells, as presented in Fig. 7. The output of $V_{\text {cell-2 }}$ is zero during $\left[t_{1}-t_{2}\right.$ ] and [ $t_{3}-$ $t_{4}$ ] that ensures the energy flow from $V_{\text {cell }-1}$ to the load. The

TABLE I
Performance Comparison

| Topology | Converter in [42] | Converter in [47] | Converter in [48] | Proposed converter |
| :--- | :---: | :---: | :---: | :---: |
| Modular structure | No | Yes | No | Yes |
| Power density | Medium | Low | Medium | High |
| Stressed devices | No | Transformer | Main switching devices | Secondary-side diode |
| Switching devices voltage stress | $\frac{V_{\text {in }}}{1-D}$ | Depending on cell voltage | $\frac{2}{1-D} V_{\text {in }}$ | $\frac{V_{\text {in }}}{1-D}$ |
| Expandability | No | Yes | No | Yes |
| Soft switching | Yes | No | No | Yes |
| Electrical isolation | No | Yes | No | Yes |
| Power rating | Low | High | Low | High |

equivalent circuit of the idle power cell is shown in Fig. 8. Both $L_{3}$ and $L_{4}$ operate in flyback mode, and the secondary side voltage sources are effectively reverse connected. At this condition, the secondary inductor of the idle module is bypassed. In the idle cells, the power losses (associated with the wire resistance and on-state conducting loss of clamp switches) are very low. In effect, cell-1 can operate at the rated output power so as to improve the converter efficiency.

In order to study the mechanism of the cell idle mode, the PSIM simulation software is employed to model the converter. In Fig. 9, a two-cell topology is used as an example. The input voltage is 15 V and the turn ratio is 2 . One cell is idle and the other cell is operational. The output voltage of the operating cell is 60 V while the peak output voltage of the idle cell is 3 V , which is associated with the leakage inductance.

## V. Expandable Characteristic and PERFORMANCE COMPARISON

The proposed 3DoF topology is flexible and expandable. First, it can combine with the interleaved structure to expand the power level, as shown in Fig. 10. Furthermore, with the development of high voltage silicon carbine ( SiC ) devices [46], the topology can be applied to HVDC power transmission for offshore wind power. In the simulation, the input voltage is 100 V , converter power is 100 kW , switching frequency is 50 kHz , each winding arm has four cells. Simulation results are shown in Fig. 11. The output voltage reaches 6.35 kV (the voltage gain is 63.5). The voltage stress on the primary switching devices is only 200 V and the peak current is 125 A . Furthermore, more diode bridges and winding arms can be added up for a higher output power.

Currently, the input-parallel output-series structure is widely used to achieve a high voltage output. However, it needs a large number of diodes and capacitors to connect the secondary sides of all cells in series after the rectifier circuit, increasing connection complexity and fault possibilities. Furthermore, the structure cannot be used to achieve a high power output. In this paper, a new solution is to combine with the input-parallel output-series structure, as shown in Fig. 12. In this case, the 3DoF topology can be seen as a cell in the traditional input-parallel output-series topology to build up a high-voltage gain converter. Clearly, the features of interleaved structure and input-parallel outputseries structure can be used in the proposed 3DoF to increase both power and voltage, as shown in Fig. 13. Therefore, by

TABLE II
Specifications of the Proposed Converter

| Component/Parameter | Value |
| :--- | :---: |
| Power level $\left(P_{\text {out }}\right)$ | 400 W |
| Input voltage $\left(V_{\text {in }}\right)$ | $5 \sim 10 \mathrm{~V}$ |
| Load resistance $(R)$ | $44 \Omega$ |
| Output voltage $\left(V_{\text {out }}\right)$ | $50 \sim 100 \mathrm{~V}$ |
| Switching frequency $\left(f_{s}\right)$ | 50 kHz |
| Main switches $\left(S_{1} \sim S_{4}\right)$ | FDP047AN |
| Clamp switches $\left(S_{c 1} \sim S_{c 4}\right)$ | FDP047AN |
| Rectifier diodes $\left(D_{o 1}, D_{o 2}\right)$ | FEP30DP |
| Clamp capacitors $\left(C_{c 1} \sim C_{c 4}\right)$ | $4.7 \mu \mathrm{~F}$ |
| Output capacitor $\left(C_{o 1}\right.$ and $\left.C_{o 2}\right)$ | $470 \mu \mathrm{~F}$ |
| Turns ratio $\left(N=n_{2} / n_{1}\right)$ | $40: 10$ |

TABLE III
Specifications of the Coupled Inductors

|  | Primary <br> inductance | Primary leakage <br> inductance | Secondary <br> inductance | Secondary leakage <br> inductance |
| :--- | :---: | :---: | :---: | :---: |
| $L_{1}$ | $28.65 \mu \mathrm{H}$ | $1.041 \mu \mathrm{H}$ | $442.9 \mu \mathrm{H}$ | $7.651 \mu \mathrm{H}$ |
| $L_{2}$ | $29.27 \mu \mathrm{H}$ | $0.991 \mu \mathrm{H}$ | $453.5 \mu \mathrm{H}$ | $7.684 \mu \mathrm{H}$ |
| $L_{3}$ | $28.88 \mu \mathrm{H}$ | $1.002 \mu \mathrm{H}$ | $447.3 \mu \mathrm{H}$ | $7.684 \mu \mathrm{H}$ |
| $L_{4}$ | $28.81 \mu \mathrm{H}$ | $0.980 \mu \mathrm{H}$ | $446.5 \mu \mathrm{H}$ | $7.886 \mu \mathrm{H}$ |

introducing a new design freedom, the proposed topology can incorporate features of traditional input-parallel output-series converters to increase voltage (via series-connection) and power (via parallel-connection) to meet the requirements.

Based on the previous analysis, a performance comparison of different dc-dc converter topologies is presented in Table I. Compared with the topologies in [42] and [47], the proposed topology has a higher power density. Compared with the converter in [48], the proposed topology can provide electrical isolation and soft switching. Furthermore, the secondary diodes can be achieved by connecting low-voltage diodes in series and parallel connections [49]-[50].

## VI. Experimental Verification

A converter with two cells is designed and fabricated to verify the effectiveness of the proposed converter. The system parameters are tabulated in Table II. The coupled inductor is constructed from a Koolmu magnetic core (0077109A7). Table III lists the parameters of four coupled inductors.


Fig. 14. Experimental results of the proposed converter. (a) Cell output voltage under normal conditions. (b) Without the shielding control. (c) With the shielding control. (d) Gate signal with the phase-angle control. (e) Output voltage of the main switch with the phase-angle control. (f) Voltage and current of the output rectifier diode.

Experimental results are presented in Fig. 14 for a 5 V input voltage, 0.5 duty ratio, and $180^{\circ}$ shift angle. Fig. 14(a) presents the cell output voltage under normal conditions using the same duty ratio and phase angle shift for cell-1 and cell-2 where each cell generates half of the output voltage. Fig. 14(b) and (c) shows test results for cell-2 idle, without and with the shielding control, respectively. In Fig. 14(b), the input current is limited so that the converter cannot transfer energy to the load. The power generated from the operating module cell is largely absorbed by the idle power cell so that little power is transferred to the load.

With the shielding control strategy [see Fig. 14(c)], the energy can be transferred to the secondary side without incurring a voltage drop across the idle windings and the input current increases dramatically. Fig. 14(d) presents the gate signal with the two-section output voltage control where the phase-angle shift control is employed to realize minor voltage adjustment. In cell-1 of Fig. 14(d), $S_{1}$ and $S_{2}$ are with a $50 \%$ duty ratio and an $180^{\circ}$ phase angle shift. In cell- $2, S_{3}$ and $S_{4}$ are with also with a $50 \%$ duty ratio but a $150^{\circ}$ phase angle shift. Compared with $S_{1}$, there is a $30^{\circ}$ delay for $S_{3} . S_{2}$ and $S_{4}$ have the same phase


Fig. 15. Soft-switching performance. (a) Main switch $S_{1}$. (b) Active clamp switch $S_{C 1}$.
shift angle and their output voltage is 72 V . Fig. 14(e) shows the output voltage of main switch $S_{3}$ with a shift angle of $30^{\circ}$, $60^{\circ}$, and $90^{\circ}$; the corresponding output voltage are 72,70 , and 67 V , respectively. The output voltage is fairly smooth with the phase-angle control. Fig. 14(f) presents the voltage and current waveforms for the output rectifier diode. Clearly, the rectifier diode reverse-recovery problem is alleviated.

The soft-switching performance of the main switch $\left(S_{1}\right)$ and clamping switch $\left(S_{C 1}\right)$ is demonstrated in Fig. 15. Due to the symmetry of the topology, all the switches have the same current and voltage profiles. Experimental results from the load transient tests are shown in Fig. 16. Fig. 16(a) shows the response to a step load change from 44 to $24 \Omega$ and Fig. 16(b), step load increase from 24 to $44 \Omega$. With the closed-loop control, the output voltage can quickly return to the set voltage, showing excellent robustness of the system. The single cell efficiency, one-cell-operating one-cell-idle efficiency and overall converter efficiency are calculated and presented in Fig. 17. In the power cell idle condition, due to the parasitic resistance in the primaryside capacitors and inductors and secondary winding resistance of the idle cell, the converter efficiency is lower than that for a single cell working condition, but is higher than the two-cell operating condition. By using power cells in an idle mode, the converter can maintain a relatively high efficiency over a wide output power range.


Fig. 16. Load transient tests. (a) Soft switching of the main switch. (b) Step load change from 24 to $44 \Omega$.


Fig. 17. Measured efficiency of the proposed converter at different conditions.

## VII. CONCLUSION

This paper has presented an ultrahigh step-up dc-dc topology based on a 3DoF topology. Through theoretical analysis and experimental tests, the proposed converter is proven to be advantageous.

1) A 3 DoF design is achieved to improve the converter performance. The electrical isolation and modular structure
of high step-up power cells are combined to increase the output voltage.
2) The voltage stress on primary switching devices of the coupled inductors is limited and soft switching of primaryside switches is achieved. The proposed 3DoF converter can use low-voltage power devices to generate a high output voltage. In addition, the reverse-recovery issue with secondary rectifier diodes is also alleviated.
3) The two-section output voltage control and module idle control are developed to improve the controllability of the output voltage and converter efficiency over a wide power range.
In summary, the proposed converter is featured with electrical isolation, modularity, multilevel structure, controllable turns ratio and duty ratio, and flexible control strategies to provide high system performance. The developed techniques can be applied widely to high-voltage and high-power dc systems.

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