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A Multi-modular Second Life Hybrid Battery Energy Storage System for Utility Grid Applications

NILANJAN MUKHERJEE

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ASTON UNIVERSITY

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Abstract

The modern grid system or the smart grid is likely to be populated with multiple distributed energy sources, e.g. wind power, PV power, Plug-in Electric Vehicle (PEV). It will also include a variety of linear and nonlinear loads. The intermittent nature of renewable energies like PV, wind turbine and increased penetration of Electric Vehicle (EV) makes the stable operation of utility grid system challenging. In order to ensure a stable operation of the utility grid system and to support smart grid functionalities such as, fault ride-through, frequency response, reactive power support, and mitigation of power quality issues, an energy storage system (ESS) could play an important role. A fast acting bidirectional energy storage system which can rapidly provide and absorb power and/or VARs for a sufficient time is a potentially valuable tool to support this functionality.

Battery energy storage systems (BESS) are one of a range suitable energy storage system because it can provide and absorb power for sufficient time as well as able to respond reasonably fast. Conventional BESS already exist on the grid system are made up primarily of new batteries. The cost of these batteries can be high which makes most BESS an expensive solution. In order to assist moving towards a low carbon economy and to reduce battery cost this work aims to research the opportunities for the re-use of batteries after their primary use in low and ultra-low carbon vehicles (EV/HEV) on the electricity grid system. This research aims to develop a new generation of second life battery energy storage systems (SLBESS) which could interface to the low/medium voltage network to provide necessary grid support in a reliable and in cost-effective manner.

The reliability/performance of these batteries is not clear, but is almost certainly worse than a new battery. Manufacturers indicate that a mixture of gradual degradation and sudden failure are both possible and failure mechanisms are likely to be related to how hard the batteries were driven inside the vehicle. There are several figures from a number of sources including the DECC (Department of Energy and Climate Control) and Arup and Cenex reports indicate anything from 70,000 to 2.6 million electric and hybrid vehicles on the road by 2020. Once the vehicle battery has degraded to around 70-80% of its capacity it is considered to be at the end of its first life application. This leaves capacity available for a second life at a much cheaper cost than a new BESS Assuming a battery capability of around 5-18kWhr (MHEV 5kWh - BEV 18kWh battery) and approximate 10 year life span, this equates to a projection of battery storage capability available for second life of >1GWhrs by 2025. Moreover, each vehicle manufacturer has different specifications for battery chemistry, number and arrangement of battery cells, capacity, voltage, size etc. To enable research and investment in this area and to maximize the remaining life of these batteries, one of the design challenges is to combine these hybrid batteries into a grid-tie converter where their different performance characteristics, and parameter variation can be catered for and a hot swapping mechanism is available so that as a battery ends its second life, it can be replaced without affecting the overall system operation. This integration of either single types of batteries with vastly different performance capability or a hybrid battery system to a grid-tie

energy storage system is different to currently existing work on battery energy storage systems (BESS) which deals with a single type of battery with common characteristics. This thesis addresses and solves the power electronic design challenges in integrating second life hybrid batteries into a grid-tie energy storage unit for the first time.

This study details a suitable multi-modular power electronic converter and its various switching strategies which can integrate widely different batteries to a grid-tie inverter irrespective of their characteristics, voltage levels and reliability. The proposed converter provides a high efficiency, enhanced control flexibility and has the capability to operate in different operational modes from the input to output.

Designing an appropriate control system for this kind of hybrid battery storage system is also important because of the variation of battery types, differences in characteristics and different levels of degradations. This thesis proposes a generalised distributed power sharing strategy based on weighting function aims to optimally use a set of hybrid batteries according to their relative characteristics while providing the necessary grid support by distributing the power between the batteries. The strategy is adaptive in nature and varies as the individual battery characteristics change in real time as a result of degradation for example. A suitable bidirectional distributed control strategy or a module independent control technique has been developed corresponding to each mode of operation of the proposed modular converter.

Stability is an important consideration in control of all power converters and as such this thesis investigates the control stability of the multi-modular converter in detailed. Many controllers use PI/PID based techniques with fixed control parameters. However, this is not found to be suitable from a stability point-of-view. Issues of control stability using this controller type under one of the operating modes has led to the development of an alternative adaptive and nonlinear Lyapunov based control for the modular power converter.

Finally, a detailed simulation and experimental validation of the proposed power converter operation, power sharing strategy, proposed control structures and control stability issue have been undertaken using a grid connected laboratory based multi-modular hybrid battery energy storage system prototype. The experimental validation has demonstrated the feasibility of this new energy storage system operation for use in future grid applications.

To my Beloved Mother

Bharati Mukherjee

To My Brother

Debanjan Mukherjee

To my Friend

Dr. Runa

To My Uncle and Aunty

Debabrata Bhattacharya and Anima Bhattacharya

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Contents

Abstract.....2

Acknowledgment5

List of Figures10

List of Tables.....16

List of Symbols18

1 Introduction.....20

 1.1 Smart grid system and challenges20

 1.2 Importance of energy storage system in the smart grid21

 1.3 Types of energy storage systems23

 1.4 Battery technology25

 1.5 Battery Energy Storage Systems (BESS) components28

 1.5.1 Battery management systems (BMS) and its operation28

 1.5.2 Power converter topologies.....32

 1.5.3 Dc-dc converters40

 1.5.4 Dc-ac Converters45

 1.5.5 Power converter control.....48

 1.6 Introduction to second life battery energy storage system (SLBESS).....52

 1.6.1 Key Advantages52

 1.6.2 Challenges of SLBESS53

 1.7 Research summary57

 1.8 Thesis Structure58

2 Power Converter Topology for SLBESS60

 2.1 Introduction.....60

 2.2 Reliability issues of Second Life Batteries and the effect of converter topologies.....60

 2.2.1 Reliability calculation background60

 2.2.2 Component failure rates.....62

 2.2.3 Reliability Estimation of Different Topologies.....63

 2.3 Multi-modular Topologies68

 2.3.1 Different Multi-modular Topologies.....68

 2.3.2 Topology Optimisation71

 2.3.3 Numerical Analysis.....74

 2.3.4 Conclusion82

3 Proposed Topology: Operational Modes.....83

 3.1 Introduction.....83

 3.2 Different modes of operation of the Converter.....83

 3.3 Design of module inductor and capacitors.....87

 3.3.1 Design of module inductor.....88

3.3.2	Design of module capacitor in boost mode.....	89
3.3.3	Design of module capacitor in buck/boost-buck mode.....	89
3.3.4	Capacitor ripple current and life expectancy.....	90
3.4	Power loss/efficiency.....	91
3.4.1	Theoretical calculation of Mode – 1 (boost Mode).....	92
3.4.2	Theoretical calculation of Mode – 2 (buck mode).....	94
3.4.3	Theoretical calculation of Mode – 3 (boost-buck mode).....	95
3.5	Validation of different modes of operation.....	96
3.5.1	Boost Mode.....	96
3.5.2	Boost-buck Mode.....	99
3.6	Validation of Power loss/efficiency.....	100
3.6.1	Switching Loss Measurement.....	101
3.6.2	Conduction loss measurement.....	101
3.6.3	Inductor Loss Measurement.....	101
3.6.4	Overall loss.....	102
3.7	Conclusion.....	103
4	Distributed Power Sharing Strategy for Second Life Hybrid Batteries.....	104
4.1	Introduction.....	104
4.2	Preliminary characterisation.....	105
4.2.1	Capacity.....	105
4.2.2	SOC-OCV relationship.....	106
4.2.3	Initial impedance.....	107
4.3	Proposed distributed sharing strategy.....	108
4.4	Online Battery Parameter Tracking.....	113
4.4.1	Internal impedance estimation.....	113
4.4.2	Capacity or charge estimation.....	115
4.5	Modelling and validation.....	117
4.5.1	Battery modelling.....	117
4.5.2	Modelling of estimation.....	117
4.5.3	Modelling of modular dc-dc converter and inverter.....	120
4.5.4	Validation in grid connected mode under normal operation.....	121
4.5.5	Validation in grid connected mode under abnormal conditions.....	123
4.5.6	Validation under parameter variation.....	124
4.5.7	Validation with sudden power change.....	126
4.6	Conclusion.....	127
5	Distributed Control Architecture.....	129
5.1	Introduction.....	129
5.2	Modelling of different control modes.....	130
5.3	Modelling in boost mode.....	130

5.4	Control in boost mode.....	132
5.4.1	Proposed DC-side control structure	132
5.4.2	Controller design.....	133
5.4.3	Dynamic response.....	135
5.4.4	Proposed overall control structure including the line side inverter.....	138
5.5	Modelling in buck mode	142
5.6	Control in buck mode.....	143
5.6.1	Proposed DC-side control structure	145
5.6.2	Controller design.....	145
5.7	Modelling in boost-buck mode	147
5.8	Control in boost-buck mode.....	147
5.8.1	Case – 1: All the modules in boost-buck mode.....	148
5.8.2	Case – 2: Boost- k -out-of- n modules only in buck mode.....	148
5.8.3	Control structure	149
5.9	Experimental validation	151
5.9.1	Boost mode	151
5.9.2	Boost-buck mode	155
5.9.3	Charging and discharging trajectory	159
5.10	Comparison between different control modes	160
5.10.1	Overall comparison and Selection of control mode.....	166
5.11	Conclusion	166
6	Stability Investigation of Distributed Control.....	167
6.1	Introduction.....	167
6.2	Stability of boost mode	168
6.2.1	Analysis.....	168
6.2.2	Other effects.....	174
6.2.3	Validation of fixed controller stability issues.....	175
6.3	Mitigation of stability problem – an adaptive PI approach.....	177
6.3.1	Adaptive tuning.....	177
6.3.2	Validation of adaptive PI-controller based approach	178
6.4	Mitigation of stability problem – Lyapunov Approach	179
6.4.1	Background.....	180
6.4.2	Lyapunov based control for cascaded dc-dc converters.....	181
6.4.3	Control architecture development.....	185
6.5	Simulation and experimental validation	188
6.5.1	Lyapunov based control approach.....	188
6.6	Stability of boost-buck mode	193
6.6.1	Boost converter analysis	193
6.6.2	Multilevel buck converter analysis	194

6.7	Conclusion	195
7	Hardware Implementation	197
7.1	Introduction.....	197
7.2	Converter design	199
7.2.1	Dc-dc Converter module design.....	199
7.2.2	Grid-tie Inverter design.....	200
7.3	Protection	205
7.3.1	Battery side protection	206
7.3.2	Protection of modular dc-dc converter.....	207
7.3.3	Protection of line side inverter	208
7.3.4	Shielding and fusing protections.....	209
7.3.5	Sensors	209
7.4	Interfacing digital controller	210
7.5	Implementation issues.....	211
7.6	Overall prototype	211
7.7	Conclusion	213
8	Conclusions and Future Work.....	214
8.1	Introduction.....	214
8.2	SLBESS system summary	214
8.3	Summary on converter topology.....	214
8.4	Summary on control strategy	215
8.4.1	Power sharing strategy	215
8.4.2	Control structure	216
8.4.3	Summary Control stability	216
8.5	Scope for additional and future Work.....	217
9	Appendix – 1: Circuit Schematics	221
10	Appendix – 2: Sample Programs and Codes.....	224
10.1	Sample numerical program for the topology optimisation	224
10.2	Sample OPAL-RT code	225
11	Appendix – 3: List of Publications	226
	References.....	227

List of Figures

Fig. 1.1 A Smart grid concept with multiple embedded generations	20
Fig. 1.2 Typical renewable energy and load demand: a) wind power case [32], b) PV power case [19]	21
Fig. 1.3 Uses of energy storage system in smart grid	22
Fig. 1.4 Power versus energy density characteristics of different energy storage systems [19]	25
Fig. 1.5 Comparison on energy density and cost [128]	26
Fig. 1.6 Typical grid connected BESS	28
Fig. 1.7 A typical battery management system	29
Fig. 1.8 Classification of different charge equalisation methods	31
Fig. 1.9 An example of active SOC balancing control structure	31
Fig. 1.10 Effect of equalisation or balancing control during discharging	32
Fig. 1.11 Classification of different converter topologies bidirectional energy storage system	33
Fig. 1.12 Single stage BESS	34
Fig. 1.13 Two-stage BESS	35
Fig. 1.14 Three-stage BESS based on high frequency-link transformer	35
Fig. 1.15 Two-stage BESS with cell bypassing functionality	36
Fig. 1.16 Dc-side modular converters: a) parallel type, b) cascaded or series type	37
Fig. 1.17 AC-side modular: Cascaded H-bridge converter	38
Fig. 1.18 AC-side modular: Cascaded H-bridge converter with integrated dc-dc converter	39
Fig. 1.19 AC-side modular configuration: parallel dc-ac topology	39
Fig. 1.20 Family of bidirectional dc-dc converters: a) boost, b) buck, c) buck-boost	41
Fig. 1.21 Classification of different dc-dc boost converter topologies	41
Fig. 1.22 Two-stage dc-dc converter	42
Fig. 1.23 Quadratic boost dc-dc converter	42
Fig. 1.24 Two-phase dc-dc converter	43
Fig. 1.25 An example of multilevel dc/dc converter	44
Fig. 1.26 Classification of different inverter topologies	45
Fig. 1.27 Diode-clamped or NPC multilevel converter	47
Fig. 1.28 Capacitor-clamped multilevel inverter	47
Fig. 1.29 Second life battery supply chain	53
Fig. 2.1 Reliability diagram of a conventional BESS	61
Fig. 2.2 Reliability diagram of modular BESS	61
Fig. 2.3 Overall cost comparison of different topologies at 10MW power level meeting 96% reliability	68
Fig. 2.4 Different possible multi-modular topologies for SLBESS : a) cascaded dc-ac, b) parallel dc-ac, c) cascaded dc-ac with integrated dc-dc, d) parallel dc-ac with integrated dc-dc, e) cascaded dc-dc with inverter, f) parallel dc-dc with inverter	70
Fig. 2.5 Ways to handle the battery failure: a) direct battery bypassing, b) bypassing through converter	70
Fig. 2.6 Cost of components: a) power electronic switches, b) drivers, c) inductors, d) capacitors	72
Fig. 2.7 Solutions for cascaded dc-side modular topology at $\lambda_{batt} = 0.2 \times 10^{-6}$: a) excluding power converter reliability, b) including power converter reliability	78
Fig. 2.8 Range of solutions for cascaded dc-side modular topology at $\lambda_{batt} = 7.7 \times 10^{-6}$: a)	

excluding power converter reliability, b) including power converter reliability	79
Fig. 2.9 Range of solutions for cascaded dc-side modular topology at $\lambda_{batt} = 60 \times 10^{-6}$: excluding power converter reliability	79
Fig. 2.10 2D-plot showing the variation of cost with n/k and x at $\lambda_{batt} = 0.2 \times 10^{-6}$ a) variation with n/k , b) variation with x	80
Fig. 2.11 Range of solutions for parallel dc-side modular topology at $\lambda_{batt} = 0.2 \times 10^{-6}$: a) excluding power converter reliability, b) including power converter reliability	81
Fig. 2.12 2D-plot showing the variation of cost with n/k and x for parallel topology at $\lambda_{batt} =$ 0.2×10^{-6} a) variation with n/k , b) variation with x	81
Fig. 3.1 Power circuit of the proposed topology	84
Fig. 3.2 Multiple modes of the proposed converter from the input to output: a) Cascaded boost mode, b) multilevel buck mode, c) Boost-multilevel buck mode	86
Fig. 3.3 Operational diagram for each mode: a) control range of boost mode, b) control range of buck mode, c) control range of boost-buck mode	87
Fig. 3.4 Block diagram of the Proposed Configuration	87
Fig. 3.5 Nature of load current in module capacitor design: a) boost-mode, b) boost-buck mode	90
Fig. 3.6 Approximate variation of on-state resistance of commercially available MOSEFTs with their voltage rating [331]	92
Fig. 3.7 Cascaded boost mode of operation: Simulation result – 1	97
Fig. 3.8 Cascaded boost mode of operation: Experimental result – 1 (time scale 20ms/div, voltage scale 20V/div)	98
Fig. 3.9 Cascaded boost mode of operation: Simulation result – 2	98
Fig. 3.10 Cascaded boost mode of operation: Experimental result – 2 (time scale 20ms/div, voltage scale 50V/div, current scale 5A/div)	99
Fig. 3.11 Boost-buck mode of operation: Simulation result	100
Fig. 3.12 Boost-buck mode of operation: Experimental result (time scale 20ms/div, voltage scale 100V/div, current scale 2A/div)	100
Fig. 3.13 Switching transients of FDPF085N10A: a) Turn ON transient b) Turn OFF transient (scale time 200ns/div, voltage 40V/div, current 10A/div)	101
Fig. 3.14 Experimental efficiency comparison of different modes of operation	102
Fig. 4.1 SOC-OCV relationship for Lead acid and NiMH batteries	106
Fig. 4.2 Pulse load test to find initial internal impedance using a dc-dc converter control ..	107
Fig. 4.3 Impedance based battery model	109
Fig. 4.4 Proposed strategy to deal with the hybrid batteries trajectory	109
Fig. 4.5 Proposed trajectory during discharging at $t = \Delta T$	112
Fig. 4.6 Ripple based impedance estimation	114
Fig. 4.7 Validation of ripple based impedance estimation method using external impedance	114
Fig. 4.8 Experimental validation of impedance estimation method for 24V battery ($Z_{nom} =$ 0.02Ω) at 10 kHz switching frequency: a) measured current ripple, b) measured voltage ripple, c) estimated impedance	115
Fig. 4.9 Validation of capacity estimation method using two identical batteries in parallel .	116
Fig. 4.10 Experimental validation of capacity estimation process using two 12V, 10Ah batteries and dynamic change in capacity	117
Fig. 4.11 Battery Model in Matlab/Simulink during discharging	118
Fig. 4.12 Matlab/Simulink model for the online capacity estimation	118
Fig. 4.13 Matlab/Simulink model for the online impedance estimation	118
Fig. 4.14 Overall Matlab/Simulink model of the bi-directional hybrid battery energy storage system	119

Fig. 4.15 Current sharing while connecting to grid during charging: a) simulation, b) experimental results	121
Fig. 4.16 Current sharing while connecting to grid during discharging: a) simulation, b) experimental results	122
Fig. 4.17 Simulated and experimental charging trajectory using the distributed power sharing strategy.....	122
Fig. 4.18 Simulated and experimental discharging trajectory using the distributed power sharing strategy	122
Fig. 4.19 Distributed sharing under module bypassing in charging mode: a) simulation, b) experimental.....	123
Fig. 4.20 Distributed sharing under module bypassing in discharging: a) simulation, b) experimental.....	123
Fig. 4.21 Simulated and experimental charging trajectory of the hybrid batteries: module bypassing.....	124
Fig. 4.22 Simulated and experimental discharging trajectory of the hybrid batteries: module bypassing.....	124
Fig. 4.23 Power sharing under capacity fade during discharging: a) simulated, b) experimental result.....	125
Fig. 4.24 Power sharing under capacity fade during charging: a) simulated, b) experimental result.....	125
Fig. 4.25 Discharging trajectory under capacity fade: a) simulation, b) experimental result	126
Fig. 4.26 Charging trajectory under capacity fade: a) simulation, b) experimental result	126
Fig. 4.27 Simulated discharging trajectory with a step change in power	127
Fig. 4.28 Simulated charging trajectory with a step change in power	127
Fig. 5.1 Considered converter topology for hybrid second life batteries.....	130
Fig. 5.2 Proposed distributed control architecture in boost mode: a) module dc-link voltage reference generation, b) module based voltage control structure	133
Fig. 5.3 Control loops per module: a) module voltage loop, b) current control loop.....	134
Fig. 5.4 Matlab/Simulink model of the control loops in boost mode	136
Fig. 5.5 Frequency response plot of the module voltage control loop.....	137
Fig. 5.6 Adaptive PI-tuning and controller parameter determination for three modules.....	137
Fig. 5.7 Frequency response plot of the module inner current control loop.....	138
Fig. 5.8 Proposed overall control architecture in boost mode: dc-side distributed control ..	139
Fig. 5.9 Rotating frame for the line side inverter control	139
Fig. 5.10 Single phase PLL structure	140
Fig. 5.11 Simplified block diagram of the PLL control.....	140
Fig. 5.12 Rotating frame based integrated control strategy for the line side inverter.....	140
Fig. 5.13 Rotating frame based inverter control structure for grid support applications.....	141
Fig. 5.14 Multilevel operation per switching cycle using distributed duty ratio	145
Fig. 5.15 Proposed DC-side control architecture in buck mode	146
Fig. 5.16 DC-link control loops: a) dc-link voltage control loop, b) dc-link current control loop	147
Fig. 5.17 Proposed dc-side control architecture in boost-buck control mode	149
Fig. 5.18 Matlab/Simulink model of the boost-buck control mode	150
Fig. 5.19 Distributed sharing (current dynamics): a) zero to discharging in simulation, b) zero to discharging in experiment (scale: current 5A/div, time 20ms/div).....	152
Fig. 5.20 Distributed sharing (current dynamics): a) zero to charging in simulation, b) zero to charging in experiment (scale: current 5A/div, time 20ms/div).....	152
Fig. 5.21 Distributed sharing (current dynamics): a) charging to discharging in simulation, b) charging to discharging in experiment (scale: current 5A/div, time 20ms/div).....	153

Fig. 5.22 Distributed sharing (current dynamics): a) discharging to charging in simulation, b) discharging to charging in experiment (scale: current 5A/div, time 20ms/div).....	153
Fig. 5.23 Distributed power sharing under module bypassing in charging mode: a) simulation, b) experimental result	153
Fig. 5.24 Distributed power sharing under module bypassing in discharging mode: a) simulation, b) experimental result.....	154
Fig. 5.25 Distributed sharing (voltage dynamics): a) charging to discharging in simulation, b) charging to discharging in experiment (scale: voltage 50V/div, time 20ms/div)	154
Fig. 5.26 Laboratory built multi-modular converter based hybrid battery energy storage system	156
Fig. 5.27 Distributed current sharing: a) zero to discharging in simulation, b) zero to discharging in experiment (scale: current 5A/div, time 20ms/div).....	157
Fig. 5.28 Distributed current sharing: a) zero to charging in simulation, b) zero to charging in experiment (scale: current 5A/div, time 20ms/div).....	157
Fig. 5.29 Distributed current sharing: a) charging to discharging in simulation, b) charging to discharging in experiment (scale: current 5A/div, time 20ms/div).....	157
Fig. 5.30 Distributed current sharing: a) discharging to charging in simulation, b) discharging to charging in experiment (scale: current 5A/div, time 20ms/div)	158
Fig. 5.31 Module bypassing during simulation: a) in simulation, b) in experiment (scale: current 5A/div, time 20ms/div)	158
Fig. 5.32 Experimental results of charging trajectory.....	160
Fig. 5.33 Experimental results of discharging trajectory	160
Fig. 5.34 Simulation comparison in discharging mode: a) boost mode, b) boost-buck mode	162
Fig. 5.35 Experimental comparison in discharging mode: a) boost mode, b) boost-buck mode (scale: current 5A/div, time 20ms/div).....	162
Fig. 5.36 Simulation comparison in charging mode: a) boost mode, b) boost-buck mode ..	163
Fig. 5.37 Experimental comparison in charging mode: a) boost mode, b) boost-buck mode (scale: current 5A/div, time 20ms/div).....	163
Fig. 5.38 Simulation comparison in charging to discharging mode: a) boost mode, b) boost-buck mode.....	163
Fig. 5.39 Experimental comparison in charging to discharging mode: a) boost mode, b) boost-buck mode (scale: current 5A/div, time 20ms/div).....	164
Fig. 5.40 Simulation comparison in discharging to charging mode: a) boost mode, b) boost-buck mode.....	164
Fig. 5.41 Experimental comparison in discharging to charging mode: a) boost mode, b) boost-buck mode (scale: current 5A/div, time 20ms/div).....	164
Fig. 6.1 Range of variation of module dc-link voltage reference and actual voltage with weighting factor: a) range of $V_{dc,i}^*$, b) range of $V_{dc,i}$	171
Fig. 6.2 Variation of gain crossover frequency or closed loop BW with SOC for 7.2V battery module.....	171
Fig. 6.3 Effect of initial SOC variation on outer voltage loop stability margin for a 7.2V, 6.5Ah module during discharging mode: a) $SOC = 70\%$, b) $SOC = 33.3\%$, c) $SOC = 10\%$	173
Fig. 6.4 Effect of SOC variation on inner loop using a modulated carrier gain (variable G) for a 7.2V, 6.5Ah module during discharging mode: a) $SOC = 70\%$, b) $SOC = 33.3\%$, c) $SOC = 10\%$	173
Fig. 6.5 Effect of SOC variation on inner current loop using a fixed carrier gain (fixed G) for a 12V, 10Ah module during discharging mode: a) $SOC = 80\%$, b) $SOC = 20\%$	174
Fig. 6.6 Variation of control stability margin with initial SOC for a 7.2V battery module ..	174

Fig. 6.7 Variation of control stability margin for capacity fade: a 7.2V battery module	174
Fig. 6.8 Fixed PI-controller in discharging condition in grid-tie mode: a) simulation study, b) experimental study: $OCV_{o,1} = 9.75V$, $OCV_{o,2} = 19V$, $OCV_{o,3} = 6.8V$: scale 50ms/div, grid current 10A/div, module currents 5A/div	176
Fig. 6.9 Fixed PI-controller in charging condition before connecting to the grid: a) simulation study, b) experimental study: $OCV_{o,1} = 13.6V$, $OCV_{o,2} = 27V$, $OCV_{o,3} = 8.3V$: scale 50ms/div, module current 5A/div	176
Fig. 6.10 Fixed PI-controller in charging condition after connecting to the grid: a) simulation study, b) experimental study: scale 5s/div, module current 5A/div, grid current 10A/div.....	176
Fig. 6.11 Comparison of non-adaptive and adaptive controller performance during discharging mode: a) non-adaptive controller, b) adaptive controller: Operating condition $OCV_1 = 9.8V(SOC_1 = 4.5\%)$, $OCV_2 = 19V(SOC_2 = 10\%)$, c) $OCV_3 = 7.8V(SOC_3 = 76\%)$.	178
Fig. 6.12 Adaptive PI-controller in discharging: a) simulation study, b) experimental study $OCV_{o,1} = 10V$, $OCV_{o,2} = 22.2V$, $OCV_{o,3} = 6V$: scale 100ms/div, grid current 10A/div, module currents 5A/div.....	179
Fig. 6.13 Adaptive PI-controller in charging: a) simulation study, b) experimental study $OCV_{o,1} = 13.4V$, $OCV_{o,2} = 26.2V$, $OCV_{o,3} = 8V$: scale 100ms/div, grid current 10A/div, module currents 5A/div.....	179
Fig. 6.14 Proposed distributed control approach for the cascaded dc-dc converter	186
Fig. 6.15 Proposed distributed control structure for the cascaded dc-dc converter: a) voltage reference generation, b) current reference generation, c) duty ratio reference generation, d) actual control logic.....	187
Fig. 6.16 Matlab/Simulink Model of module Lyapunov based control.....	188
Fig. 6.17 Matlab/Simulink model of central dc-link control loop and reference generation.	188
Fig. 6.18 Lyapunov controller in discharging: a) simulation study, b) experimental study $OCV_{o,1} = 9.9V$, $OCV_{o,2} = 20.2V$, $OCV_{o,3} = 5.9V$: scale 100ms/div, grid current 10A/div, module currents 5A/div.....	189
Fig. 6.19 Lyapunov controller in charging: a) simulation study, b) experimental study $OCV_{o,1} = 13.4V$, $OCV_{o,2} = 26.2V$, $OCV_{o,3} = 8V$: scale 100ms/div, grid current 10A/div, module currents 5A/div.....	190
Fig. 6.20 Lyapunov controller during charging to discharging: a) simulation study, b) experimental study $OCV_{o,1} = 9.8V$, $OCV_{o,2} = 22.0V$, $OCV_{o,3} = 6.1V$: scale 20ms/div, grid current 10A/div, module currents 5A/div	190
Fig. 6.21 Lyapunov controller during discharging to charging: a) simulation study, b) experimental study $OCV_{o,1} = 13.8V$, $OCV_{o,2} = 27.2V$, $OCV_{o,3} = 8.3V$: scale 20ms/div, grid current 10A/div, module currents 5A/div	190
Fig. 6.22 Effect of very high value of K: a) simulation study, b) experimental study of variation of K for module – 3: scale 500ms/div, grid current 10A/div, module currents 5A/div	191
Fig. 6.23 Effect of very low value of K: a) simulation study, b) experimental study of variation of K for module – 3: scale 500ms/div, grid current 10A/div, module currents 5A/div	192
Fig. 6.24 Test of dynamic response – 1: a) simulation study, b) experimental study scale 20ms/div, grid current 10A/div, module currents 5A/div	192
Fig. 6.25 Test of dynamic response – 2: a) simulation study, b) experimental study scale 20ms/div, grid current 10A/div, module currents 5A/div	193
Fig. 6.26 Module voltage control loop in boost-buck mode.....	193
Fig. 6.27 Module current control loop in boost-buck mode	194
Fig. 6.28 Control loop for the multilevel buck converter: a) outer dc-link voltage loop, b) inner current loop.....	195

Fig. 7.1 System architecture implemented.....	198
Fig. 7.2 Operational envelope for 1kW prototype: a) input side region, b) output side region	198
Fig. 7.3 One converter module	199
Fig. 7.4 Laboratory built converter module with integrated driver	199
Fig. 7.5 Grid-tie single phase inverter	200
Fig. 7.6 Line side current ripple.....	202
Fig. 7.7 Variation of output current ripple with the duty ratio of inverter leg	202
Fig. 7.8 Electrical equivalent circuit to design a common heat-sink for the inverter	204
Fig. 7.9 Laboratory built line side inverter	205
Fig. 7.10 Crowbar protection	207
Fig. 7.11 logic circuit protection	207
Fig. 7.12 Protection logic for each converter module.....	208
Fig. 7.13 Laboratory built protection card for one converter module	208
Fig. 7.14 Protection logic for the line side inverter	209
Fig. 7.15 Overall laboratory experimental set-up	212
Fig. 7.16 hybrid batteries used in the experimental implementation.....	212
Fig. 7.17 Detailed overall set-up: a) overall set-up, b) power converter part.....	213

List of Tables

Table 1-1 Comparison among different energy storage systems	24
Table 1-2 Comparison of different SOC estimation methods [134]	30
Table 1-3 Comparison of different configuration in BESS.....	40
Table 1-4 Comparison of different types of dc-dc boost converter	44
Table 1-5 Comparison of different dc-ac converter topologies	48
Table 1-6 Comparison of different controller	51
Table 1-7 Revenue stream.....	54
Table 1-8 Range of inferred failure rates of batteries	55
Table 2-1 Range of failure rate and average failure rate of different components	63
Table 2-2 Reliability comparison of different topologies for transformerless grid connection	66
Table 2-3 Reliability and voltage functions for different multi-modular topologies	73
Table 2-4 Expression of cost indicators for different multi-modular topologies	73
Table 2-5 Optimisation result for different topologies – 1.....	75
Table 2-6 Optimisation result for different topologies – 2.....	76
Table 3-1 Boost inductor values with a considered range of input voltages	93
Table 3-2 Efficiency/power loss calculation in boost mode (equal module) at 1kW power level.....	93
Table 3-3 An example calculation in boost mode (unequal module) at 1kW power level	94
Table 3-4 Efficiency/power loss calculation in buck mode at 1kW power level.....	95
Table 3-5 Efficiency/power loss calculation in boost-buck mode (equal modules)	96
Table 3-6 Efficiency/power loss calculation in boost-buck mode (unequal modules)	96
Table 3-7 Components specifications used in experimental validations	97
Table 3-8 Theoretical and experimental efficiency using different modes at a particular operating point	102
Table 3-9 Detailed Loss distribution in the converter.....	103
Table 3-10 Measured case temperature of the module switches under real operating condition	103
Table 4-1 Component specifications used in simulation and/or experimental validation	120
Table 5-1 Operating condition in boost mode.....	155
Table 5-2 Theoretical and experimental comparison of module currents at an instant in boost mode.....	155
Table 5-3 Operating condition in boost-buck mode	158
Table 5-4 Theoretical and experimental comparison of module currents in boost mode.....	159
Table 5-5 Comparison of theoretical and experimental values of module currents in boost mode.....	165
Table 5-6 Comparison of theoretical and experimental values of module currents in boost-buck mode.....	165
Table 5-7 Overall comparison.....	166
Table 6-1 Stability comparison between the boost and boost-buck mode of operation	195
Table 7-1 Rating specification for maximum 1kW laboratory prototype.....	198
Table 7-2 Components used per H-bridge dc-dc module	200
Table 7-3 Components used in the inverter	205
Table 7-4 Different types of fault and proposed actions.....	206
Table 7-5 Fusing and shielding protection.....	209
Table 7-6 Specification of OPAL-RT based digital controller.....	210

Table 7-7 Controller interface with the converter210

List of Symbols

SLBESS	Second Life Battery Energy Storage Systems	
$V_{batt,i}$	Steady state terminal voltage of i^{th} module	V
$V_{max,i}$	Maximum allowable voltage of i^{th} module	V
$V_{min,i}$	Minimum allowable voltage of i^{th} module	V
$i_{batt,i}^*$	Current reference of i^{th} battery module	
$I_{batt,i}$	Steady state current of i^{th} battery module	A
$V_{dc,i}$	Steady state capacitor voltage of i^{th} module	V
$V_{dc,i}^*$	Capacitor voltage reference of i^{th} module	
$\widehat{i}_{batt,i}$	Small signal value of i^{th} module current	
$\widehat{V}_{dc,i}$	Small signal i^{th} module dc-link voltage	
V_{dc}	Total DC-link capacitor voltage	V
V_{dc}^*	Total DC-link capacitor voltage reference	
$\Delta V_{batt,i}$	Battery voltage ripple of i^{th} module	V
$\Delta i_{batt,i}$	Battery current ripple of i^{th} module	A
I_{dc}	Steady state DC-link current	A
d_i	Instantaneous duty cycle of i^{th} boost converter module	
$d_{i i}$	Instantaneous duty cycle of i^{th} buck converter module	
d_{av}	overall duty cycle of multilevel buck converter module	
D_i	Average duty cycle of i^{th} boost converter module	
D_{ii}	Average duty cycle of i^{th} buck converter module	
$d_{max,i}$	Maximum duty cycle of i^{th} converter module	
C	Module dc-link capacitance	F
L	Module boost inductance	H
R	Leakage resistance of module boost inductance	Ω
$R_{ds(on)}$	On-state resistance of the switches	Ω
L_s	Line side filter inductance	H
C_s	Line side filter capacitance	F
V_s	RMS grid voltage	V
I_s	RMS grid current	A
V_{sw}	Maximum switch voltage rating of a dc-dc module	V
$Q_{max,i}$	Maximum charge (capacity) of i^{th} module	C
$SOC_{0,i}$	Initial state-of-charge of i^{th} battery module	p.u.
SOC_i	Instantaneous state-of-charge of i^{th} battery module	p.u.
$OCV_{0,i}$	Initial open circuit voltage of i^{th} module	V
OCV_i	Instantaneous open circuit voltage of i^{th} module	V
$OCV_{min,i}$	Minimum open circuit voltage of i^{th} module	V
$OCV_{max,i}$	Maximum open circuit voltage of i^{th} module	V
Z_i	Impedance of i^{th} battery module	Ω
ω_i	Weighting factor of i^{th} module currents	
BW	Bandwidth	
ω_{gc}	Gain crossover frequency	
$K_{v,i}$	Proportional gain for voltage controller of i^{th} module	A/V
T_v	Integral gain for module voltage controller	
T_d	Current controller delay	s
K_c	Proportional gain for inner module current controller	A/V

K_{cd}	Proportional gain for inner dc-link current controller	A/V
$K_{v,d}$	Proportional gain for central dc-link voltage controller	A/V
i_s^{dq}	Rotating frame line side currents	A
V_s^{dq}	Rotating frame line side voltage side	V
λ_{batt}	Battery failure rate	$10^{-6}/h$
λ_{sw}	Switch failure rate	$10^{-6}/h$
$\lambda_{DC/DC}$	Dc-dc converter failure rate	$10^{-6}/h$
$\lambda_{DC/AC}$	Dc-Ac converter failure rate	$10^{-6}/h$
λ_{DAB}	Dual active bridge failure rate	$10^{-6}/h$
λ_{HFT}	High frequency transformer failure rate	$10^{-6}/h$
λ_{filter}	Converter filter failure rate	$10^{-6}/h$
λ_b	Basic failure rate of an electronic component	$10^{-6}/h$
R_m	Converter module reliability	p.u.
R_T	Total converter reliability	p.u.
V_{cell}	Battery cell voltage	V
x	Total number of battery cells/module	
<i>DUOS</i>	Distribution use of system	
<i>STOR</i>	Short term operating reserve	
<i>FCDM</i>	Frequency control by demand management	
<i>FFR</i>	Firm frequency response	

1 Introduction

1.1 Smart grid system and challenges

Due to the increasing shortage of fossil fuels and the impending issues from environmental pressure, new generation sources with higher efficiency such as fuel cells, micro-gas turbines, and renewable energy sources (RESs) such as wind and solar power, are becoming more important as distributed energy resources (DERs). The distributed and renewable energy sources are set to take an increasing portion in the market at electric power generation in coming years as summarised in [1] – [4] which discusses the economic benefits of DER into the grid system. Today, the most prolific renewable energy sources are wind and PV systems as discussed in [5] – [10]. The proliferation of current and planned distributed generation along with future concepts such as Vehicle-to-Grid (V2G) interfacing [11] – [12] is leading to the push for a better co-ordinated, better monitored smart grid. Some of the key review papers on topic are [13] – [17] which act as examples of proposed smart grids of the future around in the literature. Many researchers agree that the key features are shown in Fig. 1.1 [18].

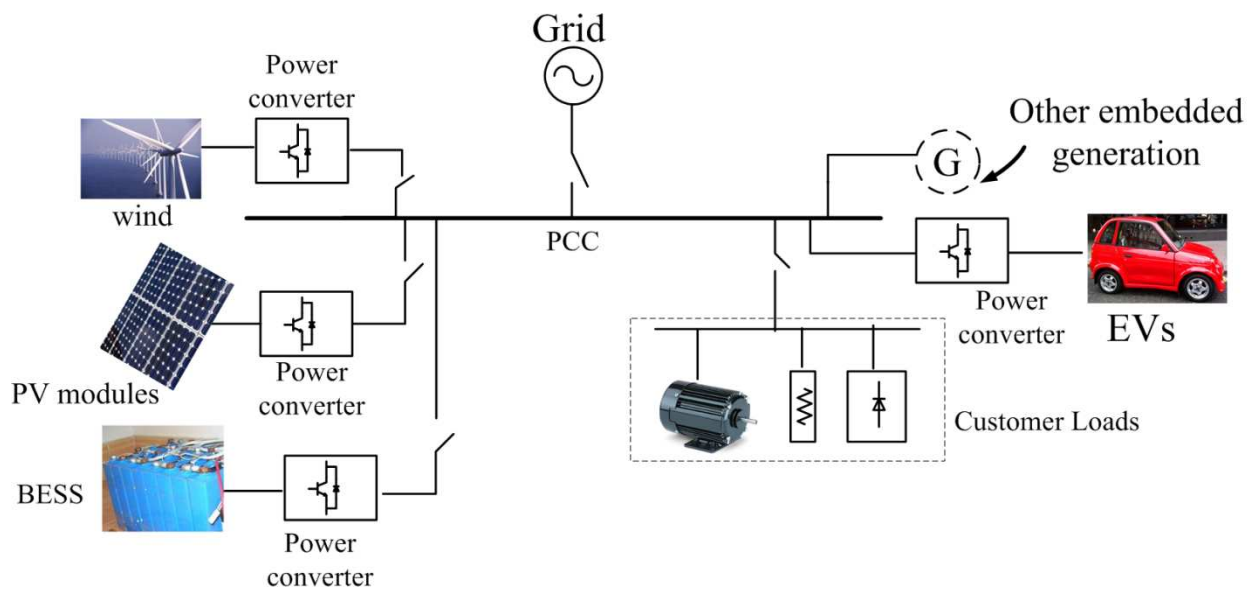


Fig. 1.1 A Smart grid concept with multiple embedded generations

However, the power generated from wind and solar is intermittent and uncertain in nature, which presents challenges to normal power systems operation. Fig. 1.2 shows some examples of the load mismatches that could occur due to the intermittent nature of wind power and PV systems as reported in [19], [20]. This can cause voltage rise/dip problems in low voltage networks [21] – [27] whereas in medium/high voltage networks it can cause frequency stability problem as reported in [28] – [30]. The most commonly used approach in mitigating the variability of renewable generation is using medium and fast-ramping generators, such as

diesel combined-cycle combustion turbines and gas turbines [31]. However, having a generator operating as spinning reserve offsets a proportion environmental benefit of renewable energy. Moreover, these existing generators are of low efficiency and may introduce time lag in their AVR/governor control system. An alternative to using spinning reserve generation is employing an energy storage system (ESS) in order to mitigate against this variability. Therefore it is an important addition to the smart grid as shown in Fig. 1.1.

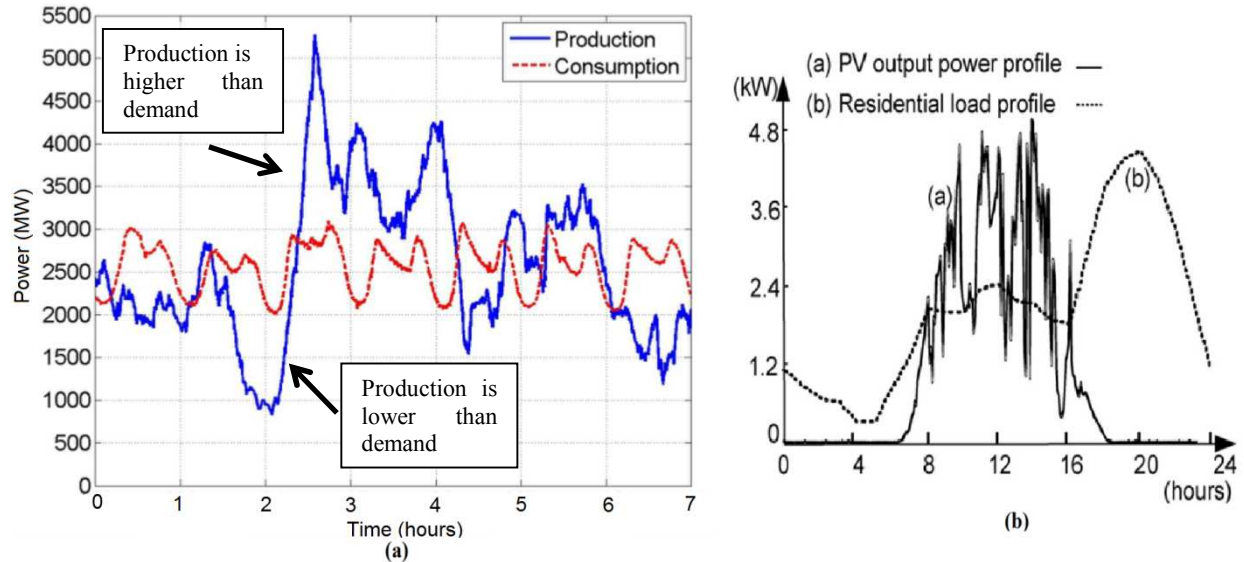


Fig. 1.2 Typical renewable energy and load demand: a) wind power case [32], b) PV power case [19]

1.2 Importance of energy storage system in the smart grid

Large-scale energy storage systems (ESS) are widely regarded as a potential technology in improving the flexibility and receptivity of the power grid and solving the coordination problem of intermittent energy. In particular the energy storage systems (ESS) can be used on two different time scales: a) long term support, b) short term support. Over a long time scale (e.g. in days/hours), bulk energy storage systems, can be “charged” by the excess renewable energy generation during off-peak hours and “discharged” during peak hours and over a short time scale (e.g. minutes/seconds), fast-response energy storage systems, such as batteries and flywheels, can help smooth the output of renewable energy generators. Moreover, the ESSs can also be used to address the power quality issues to the grid [33] – [36]. The main roles of an ESS in the smart grid have been summarised in Fig. 1.3. Brief descriptions of these services are described as follows.

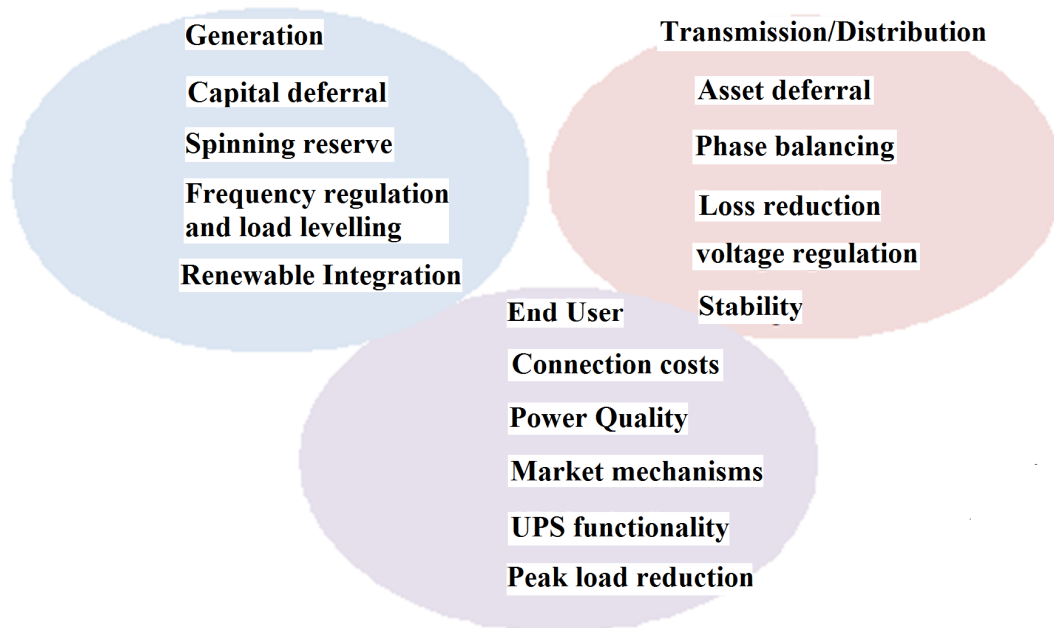


Fig. 1.3 Uses of energy storage system in smart grid

Frequency regulation/Spinning reserve/stability: Spinning Reserve is the on-line reserve capacity that is synchronized to the grid system and ready to meet the electric demand when necessary. Spinning Reserve is needed to maintain the system frequency stability during emergency operating conditions and unforeseen load swings. An inverter connected energy storage unit is well suited for this purpose because of the speed of the power electronic interface. Due to the large amount of research in this area, references [37] – [43] are quoted as giving examples related to the research and conclusions on this area.

Load Levelling/Peak shaving: Energy storage has been used to flatten an electrical load by charging the storage when the system load is low and discharging the storage when the system load is high as described in the references [44] – [49]. This technique is known as load levelling. The load levelling is also referred to as peak load shaving, includes using energy storage to eliminate the peaks and valleys in the load profile [49], [50] – [54]. Therefore, it is similar to load-levelling, except instead of constant power draw from the grid to supply the daily average load, less power is drawn from the grid during peak demand times. Consequently more power needs to be drawn at low demand time to replace the expended stored energy during peak times. This practice offers direct and indirect benefits to utilities in generation costs, line loss reduction, and voltage support as reported in [55] – [56]. The net effect is a significant reduction in peak power levels drawn from the grid which reduces the peak power cost charged by the utility.

Renewable Energy Integration: An ESS unit could be placed within a wind or solar generation installation, effectively converting it to a constant power source. There are significant recent researches on this area concentrating on both the control aspect as well as the economic aspect [57] – [61]. All these research agree on the placing energy storage systems along with renewable energies to compensate the fluctuation of power to improve the power quality and grid stability.

Asset/Capital deferral: An ESS can be used to defer investment into network or customer asset upgrades through the use of energy storage in a mechanism similar to load levelling as asset overload conditions are removed by local energy storage [62] – [64].

Power quality/phase balancing/voltage regulation: The influence of the wind or PV power sources in the grid system concerns the power quality such as the active power, reactive power, and variation of voltage, harmonics, and electrical behavior in switching operation. The power quality problems when wind turbine installed to grid side can be resolved using an ESS for example, a Static Compensator (STATCOM) is connected at a point of common coupling with a battery energy storage system (BESS) can rectify the power quality problems [65] – [67]. The combination of battery storage with wind energy generation system can synthesize the output voltage and current waveform by absorbing or injecting reactive power and enable the real power flow required by the load.

Loss reduction: A localised ESS can reduce power flow through the distribution network to reduce I^2R losses. The references [68] – [70] discuss these economic benefits and also the optimal location of an ESS on the distribution network.

Connection cost/Market mechanism: An energy storage system can be used by customers looking to minimise energy costs through tariff manipulation by adjusting load demand at the peak time as discussed in [71] – [73].

UPS functionality: All the above mentioned services are applicable when the grid is present. However, there is additional opportunity to be gained from also using ESS in grid independent mode when the main power source is not present e.g. feeding islanded industrial plants or localized loads as reported in [74] – [79]. In grid independent mode also, there could be multiple loads including motors in pumps, fans and compressors which may be operated frequently. Therefore, such industrial plant can undergo voltage and frequency fluctuations under both normal and fault operation. For large establishments, multiple power sources/generators can be used and it is practical to use an ESS to provide short term power and then, after run up time, to switch to other generators such as reported in [80].

1.3 Types of energy storage systems

To fulfill these above mentioned grid based functions, the energy storage system is required to be cost effective with a reasonable life cycle, reliable, safe and with sufficient ramp times. There are thousands of references for energy storage technology on the grid both formally published and available on manufacturers and interest group websites. Energy storage technology can be summarised into the following categories below [81] – [84]:

- Pumped Storage (>20GW worldwide)
- Compressed air (>400MW worldwide)
- Batteries
 - NaS (> 200MW worldwide)
 - Redox Flow (>11MW worldwide)
 - Lead Acid, Lead Carbon (> 125MW)

- Lithium ion (>100MW worldwide)
- NiMH (sub 25kW level only)
- NiCad (>27MW worldwide)
- Flywheels (>3MW Worldwide)
- Electromechanical capacitors (450kW, 30s demonstrator CA)
- Superconducting Magnetic Energy Storage (3MW demonstrator in Texas + smaller units)

References [83] and [85] – [87] are good examples of comprehensive reviews of these different energy storage systems and their possible applications. Table 1-1 shows a brief comparison of the different energy storage solutions in terms of their key parameters; efficiency, energy density, power density and response time based on these research. The most literatures such as [19], [85] – [87] agree that flywheels and super-capacitors have good energy efficiency. However, a flywheel responds in the order of seconds while the super-capacitor is capable of responding quickly in the order of 100's of μ s to few ms. The energy densities for these two solutions are low which means they cannot be employed to provide the long term power backup. On the other hand, compressed air energy storage system (CAESS) is a low efficiency, low energy density, poor dynamic response solution which makes it unsuitable for fast response, but good for bulk storage. Fuel cells have a low energy efficiency but good energy density and power density. The fuel cells may be a unidirectional ESS and has a slow response time. Super-conducting magnetic energy storage solution (SMES) has been used in the past because of its high efficiency and reasonably fast response time. However, a SMES coil is inductive in nature which can be bulky and expensive which limits its application. Batteries provide high energy density, high efficiency and power density as well as fast dynamic response. Therefore, in utility applications the battery energy storage system (BESS) offers a good compromise between all the desired features. Within BESS there are different battery chemistries or types which have differences in performances both in terms of power density and energy density because of differences in chemical compositions, internal impedances and capacities which influence their efficiency and power/energy density. Fig. 1.4 shows a comparison between different energy storage system in terms of energy density and power density [19] compared to fuel cells and capacitors. Fig. 1.4 is similar to many other general figures published in the literature around this topic.

Table 1-1 Comparison among different energy storage systems

Type	Energy Efficiency	Energy density (Wh/kg)	Power density (W/kg)	Speed of response
Flywheel	≈ 95%	30	1000	In seconds
Compressed Air	≈40 – 50%	20	-	In seconds
Fuel Cell	≈60-70%	60-70	200-300	In 100's ms
Batteries	≈70 – 90%	90-200	300-500	10 – 50ms
Super-capacitor	≈95%	20-30	4000	1 – 10ms
Super conducting magnetic elements	≈ 90%	-	-	20 – 50ms

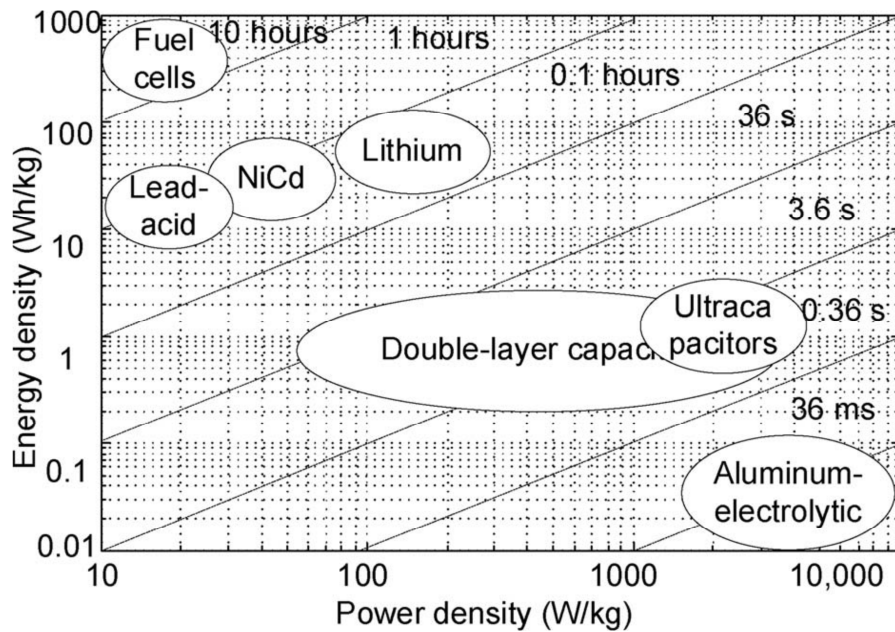


Fig. 1.4 Power versus energy density characteristics of different energy storage systems [19]

It was reported in [19] that fuel cells have very low power density but the highest energy density compared to batteries and super-capacitors. However, no information about the associated accessories such as, fuel cell tanks was included in that research. This could have an impact on the overall energy density of the fuel cell energy storage as reported in [88]. On the other hand, capacitors have the lowest energy density but have very high power density. From this comparison it can be seen that a battery offers a good compromise between energy density and fast speed of response which are important criterion in fast acting grid support applications. For these reasons, the focus of this thesis is around BESS.

1.4 Battery technology

Battery energy storage systems have been the focus of extensive attention in literature in grid based applications as a power system stabiliser, ancillary applications [89] – [90], renewable energy system [91] – [92], power quality conditioners [93] – [94], [36] and automotive or V2G applications [95] – [98]. Since 2008, heavy US and EU investment in battery technology R&D for transport applications has placed increasing focus on battery technology [100] – [102]. There are well over 60 different types of battery [103]. Around half of these are primary batteries (no recharge available) and the remainder are secondary (capable of recharge) [103].

An illustration of the cost against energy density (more important for transport than energy storage) for common types of battery is shown in Fig. 1.5 [99] – [108]. What is clear is that Lead Acid battery costs are the lowest and consequently, vehicle based lead acid batteries dominate the market. In recent years, lithium-ion (Li-ion) batteries have emerged as a key contender for both vehicle and electricity storage. Lithium-ion battery technology presents a number of advantages over traditional lead-acid, nickel-metal hydride and nickel-cadmium rechargeable batteries, including high energy density, low self-discharge rate, light weight and flexible battery shape, and absence of ‘memory effect’ (batteries not recharging to their

original maximum capacity when repeatedly re-charged after only partial discharge) [109] – [110]. The most common lithium ion battery type is lithium iron phosphate (LiFePO₄) battery [111].

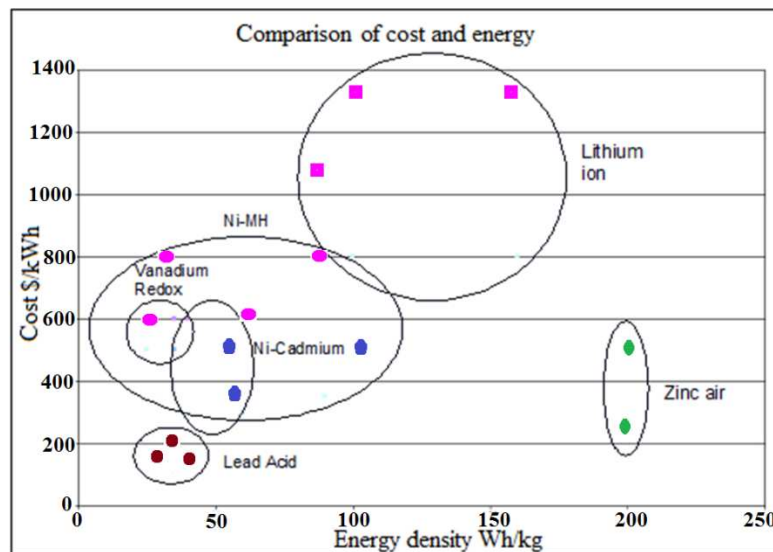


Fig. 1.5 Comparison on energy density and cost [128]

However, there are also some disadvantages of lithium ion batteries which include reduction of cell capacity over time and increasing internal resistance, along with vulnerability to overheating and over-discharge and the high cost of components such as cobalt (LiCoO₂). Recent technical innovations have addressed these issues, including more stable and conductive materials for the cathode, anode and electrolyte; the development of advanced battery management systems to regulate output voltages within strict limits [112] – [113].

Sodium–sulfur (NaS) batteries are primarily manufactured by one group, the NGK/TEPCO consortium in Japan, producing around 90 MW of storage capacity each year [114]. However, there is no other large scale manufactures. Megawatt scale NaS Battery Systems were first operated in the field more than 10 years ago. Although the basic design concept of NaS battery cells and modules has not changed, the technology has been improved through many field demonstrations and commercial installations. Initially, the target application for NaS batteries was load levelling, which remains its primary use. Recently, NaS Battery applications have focused on stabilising fluctuating power from renewable energy resources, such as wind turbines or photovoltaic generators. More than 300 MW of NaS Battery Systems have been installed globally. However, NaS batteries mostly operate at over 300°C and contain highly corrosive chemicals [115] – [116].

A 27 MW 15 minute (6.75 MWh) nickel-cadmium demonstration battery bank was installed at Fairbanks Alaska in 2003 to stabilize voltage at the end of a long transmission line [117]. However, there are no other large installations. When compared to other forms of rechargeable battery, the Ni–Cd battery has a number of distinct advantages: The batteries are more difficult to damage than other batteries, tolerating deep discharge for long periods. This is in contrast, for example, to lithium ion batteries, which are less stable and will be

permanently damaged if discharged below a minimum voltage. Ni–Cd batteries typically last longer, in terms of number of charge/discharge cycles, than other rechargeable batteries such as lead/acid batteries. However, a Ni–Cd battery has a higher self-discharge rate especially at a high temperature. Therefore, it is recommended to keep them in cooler environments [118] compared to other battery types. The primary trade-off with Ni–Cd batteries is their higher cost and the use of cadmium (an environmental hazard, highly toxic to all higher forms of life). They are also more costly than lead–acid batteries because nickel and cadmium cost more. One of the biggest disadvantages is that the battery exhibits a very marked negative temperature coefficient. This means that as the cell temperature rises, the internal resistance falls. This can pose considerable charging problems, particularly with the relatively simple charging systems employed for lead–acid type batteries [119]. Nickel–metal hydride (NiMH) batteries are the newest, and most similar, competitor to Ni–Cd batteries. Compared to Ni–Cd batteries, NiMH batteries have a higher capacity are less toxic, no memory effect and are generally more cost effective. But NiMH batteries have high self-discharge rate compared to Ni-Cd batteries [120].

Rechargeable flow batteries can be used as a rapid-response storage medium. Vanadium redox flow batteries are currently installed at Huxley Hill wind farm (Australia), Tomari Wind Hills at Hokkaidō (Japan), as well as in other non-wind farm applications [121] – [122]. These storage systems are designed to smooth out transient fluctuations in wind energy supply. The main advantages of the Vanadium redox battery are that it can offer almost unlimited capacity simply by using larger and larger storage tanks, it can be left completely discharged for long periods with no ill effects, it can be recharged simply by replacing the electrolyte if no power source is available to charge it, and if the electrolytes are accidentally mixed the battery suffers no permanent damage. The main disadvantages with Vanadium redox technology are a poor energy-to-volume ratio, and the system complexity in comparison with other types of batteries [123].

Hydrogen Bromide has been proposed for use in a utility-scale flow-type battery as an alternative to a Vanadium flow battery [124]. The hydrogen/bromine energy storage system has some advantages over other battery systems: The hydrogen and bromine electrodes are fully reversible, the cell is capable of operating at a high current and high power density and the components are low cost (plastics and composites). The major disadvantage of the hydrogen/bromine energy storage system is its use of bromine. Bromine is reactive and corrosive and has a substantial vapor pressure at room temperatures.

When a battery is first developed in a laboratory, it is treated with care, in an ambient temperature environment and loaded using load banks to help determine the energy density and performance. Batteries within the field do not have such an easy life and are frequently subject to real life events that occur due to system effects such as harmonics from the power electronics, short circuits, high di/dt , thermal cycling either with or without charge/discharge occurring and vibration. The battery itself may take a significant period of time to charge and durability and variability of cells may increase this time and reduce life further. Consequently not all batteries in the lab make it through to commercialisation. Batteries can be expensive,

or have high maintenance, or have limited lifespan [126]. Other issues with using battery energy storage include; regulation and market forces (for example difficulty in formulating a bidding strategy) and lack of experience with energy storage by the Utilities hampering growth opportunities.

With the great variety of battery chemistries and the push in the vehicle industry for high power and energy density, such as the research towards lithium-ion batteries [127], the only certainty is that battery chemistry is unlikely to be fixed within the next 10 years and research in this field needs to take into account of battery evolution so as not to render itself obsolete.

1.5 Battery Energy Storage Systems (BESS) components

A typical battery energy storage system consists of three stages as shown in Fig. 1.6: a) battery management system, b) power electronic converter and c) a centralised controller/control system. The description of each is provided in detail.

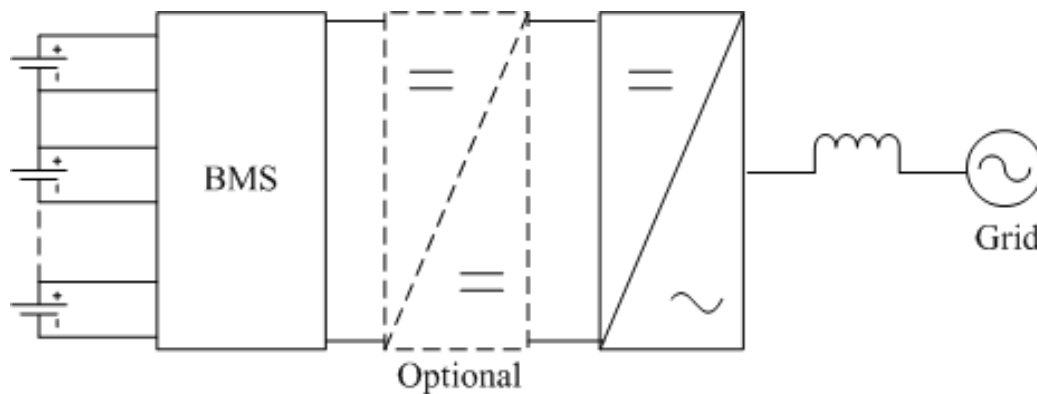


Fig. 1.6 Typical grid connected BESS

1.5.1 Battery management systems (BMS) and its operation

In any battery system, the BMS is a key element to ensure all cell/battery voltages are kept within the limits (maximum/minimum) for safe operation and to maximise the cycle life. These can be undertaken through two key functions of the BMS– monitoring and charge equalization. The operational of a BMS has been shown through a simplified diagram in Fig. 1.7 . First, the BMS monitors the status of all the series connected battery cells in a module. The parameters being monitored include cell voltage, cell temperature, charging or discharging current. The voltage, current and temperature information are then processed by the BMS controller to determine the state-of-charge (SOC) which a measure of the amount of electrochemical energy left in a cell or battery. It is expressed as a percentage of the total available battery charge. Secondly, the BMS applies active or passive balancing circuit/control to equalize the charge and/or voltages of the cells in the pack and to ensure all the cells operating within the designed SOC range (e.g. say 10 – 90%) as reported in [125] – [132].

It has been a long-standing challenge for the battery industry to precisely estimate the SOC of batteries. The electrochemical reaction inside batteries is very complicated and hard to model electrically. There are various ways SOC can be found as discussed in [133] – [136].

Table 1-2 shows a summary of different SOC calculation methods based on the comprehensive review presented in [134]. Among all the practical techniques, the SOC-OCV relationship based method is considered to be a low-cost and accurate method for online estimation of SOC where the battery capacity is not accurately known. However, it requires a pre-characterisation to be performed prior to operation.

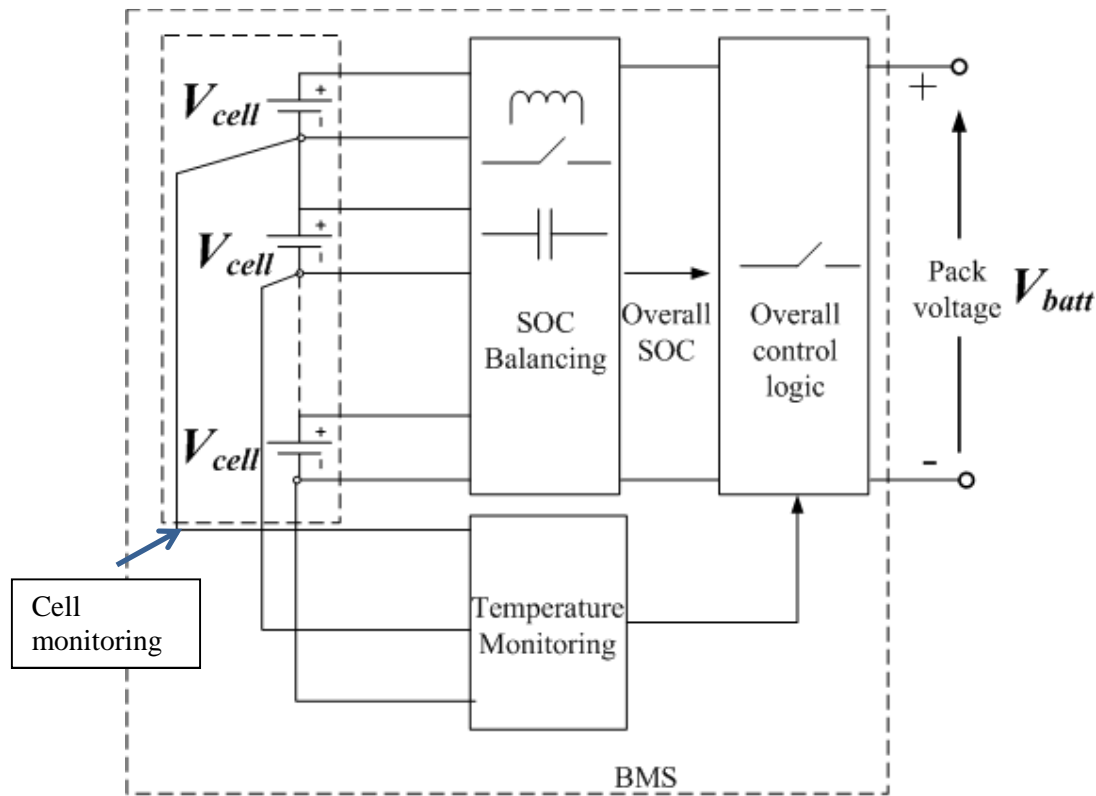


Fig. 1.7 A typical battery management system

Owing to the fact that voltage in a single battery cell is inherently low, the battery cells are connected in series for many practical applications. However, within a series connection of large number of cells, cell voltage imbalance can be attributed to the differences of cell internal resistance, imbalanced state-of-charge (SOC) between cells, degradation, and the gradients of ambient temperature of the battery pack during charging and discharging. Imbalanced cell voltage will cause overcharge or deep-discharge, and decrease the total storage capacity and consequently the total cycle life of a battery. Equalization or balancing among the cells in a series connected battery string is therefore necessary to minimize the mismatches across all the cells to help extend the battery lifecycle.

The balancing methods can be classified into two categories: active [139], [125] – [132] and passive circuits [140] – [142]. The passive balancing circuit consists of resistor, capacitor or diodes and is connected across each cell. The circuit is connected to the positive and negative terminals of each cell in a battery string. This essentially acts as a two terminal voltage controlled current shunt. It provides each cell with an alternate current path for string float current. The principle concept of this circuit is to divert the excess energy from the higher voltage battery to the lower voltage battery within a string. It can be explained this way also: a cell requiring less float current to maintain its required voltage level increases the current flow through the passive shunt, thereby decreasing the cell's float current during the

discharging to prevent deep discharge and vice versa to prevent overcharge. It is a straightforward approach to implement and also independent of battery types and widely used especially when a large string of batteries present such as in automotive applications. On the other hand, active cell balancing circuit helps balance the cells in a battery module to maintain the same voltage or SOC by monitoring and injecting appropriate balancing current into individual battery cell based on the balancing scheme. This active cell balancing circuit can be divided into two groups: unidirectional and bidirectional cell balancing as shown in Fig. 1.8. Among these schemes, multiple-winding transformer-based solutions are attractive for their effective low-cost equalization. However, it is difficult to implement multiple windings in a single transformer when a battery string consists of more than 100 cells such as in electric vehicle (EV) application. The switched capacitor-based solution is also not considered for the long equalization time. The isolated bidirectional dc-dc converter regulates from the battery stack voltage to each individual cell voltage. The average current mode control is employed such that the average inductor current is regulated to the command current, which is set by the active cell-balancing control algorithm.

Compared to the traditional passive cell balancing approach, the active cell balancing approach offers advantages of higher system efficiency and faster balancing time. However, active balancing is difficult and more expensive to implement if there is a large number of battery modules present. Moreover, the selection of active balancing methods is also dependent on the battery types or chemistry, e.g. a lithium-ion battery types requires more advanced balancing method and management system compared to other battery types because of safety.

Table 1-2 Comparison of different SOC estimation methods [134]

Technique	Summary of the method	Advantages	Drawbacks
Discharge	Discharge with DC current and measure time to reach a certain threshold point	Accurate	Cannot be performed online
Coulomb counting	Counting charges that have been injected/pumped out of a battery	Online method	Inaccuracy can occur due to measurement of initial SOC
Open circuit voltage	SOC-OCV look-up table or a derived relationship	inexpensive and Online method	Pre-characterisation is needed
ANN based method	Adaptive artificial neural network system	Online method	Pre-defined training data needed
Impedance spectroscopy	Frequency response plot is used to characterise the battery	Accurate	Expensive and temperature sensitive
Impedance based method	Uses an impedance based battery model	Gives indication of state-of-health (SOH) and SOC	Temperature sensitive, e.g. impedance varies with temperature
Kalman filter	Averaging information using a Kalman filter and observer – can handle inaccurate data better	Online method	Large computation and matrix calculation is needed

There have been extensive researches done on different active equalisation control along with developing different active equalisation circuit, as reported in [147] – [155]. This type of control has been predominantly based on employing a dc-dc converter/cell or using a modular dc-ac converter [155] – [156]. The control structure can be explained with the help of Fig. 1.9. These controls aim to equalize the mismatch of instantaneous SOC's, between the modules by controlling the individual module converter. The effect of this control can be explained with the help of Fig. 1.10. It can be seen how the balancing current references are generated from the differences between average SOC and module SOC. The main idea is to force the difference between average SOC and individual SOC (ΔSOC) to zero. It can be seen how the module SOC's are made equal by using individual module currents, e.g. the higher module SOC is discharged at a higher rate and the lower module SOC is discharged at a lower rate until all the SOC's become equal.

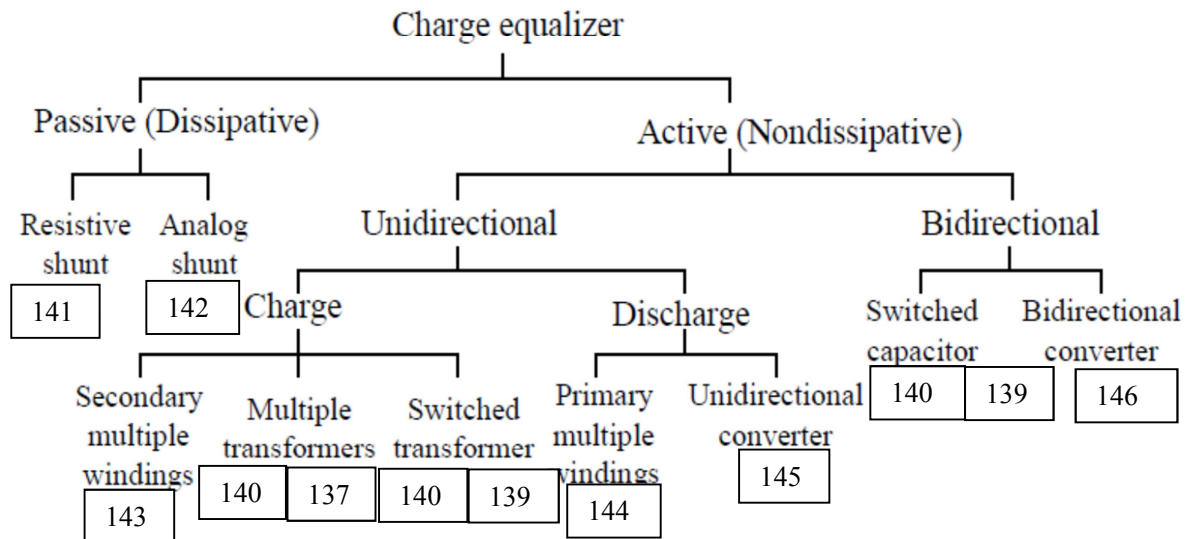


Fig. 1.8 Classification of different charge equalisation methods

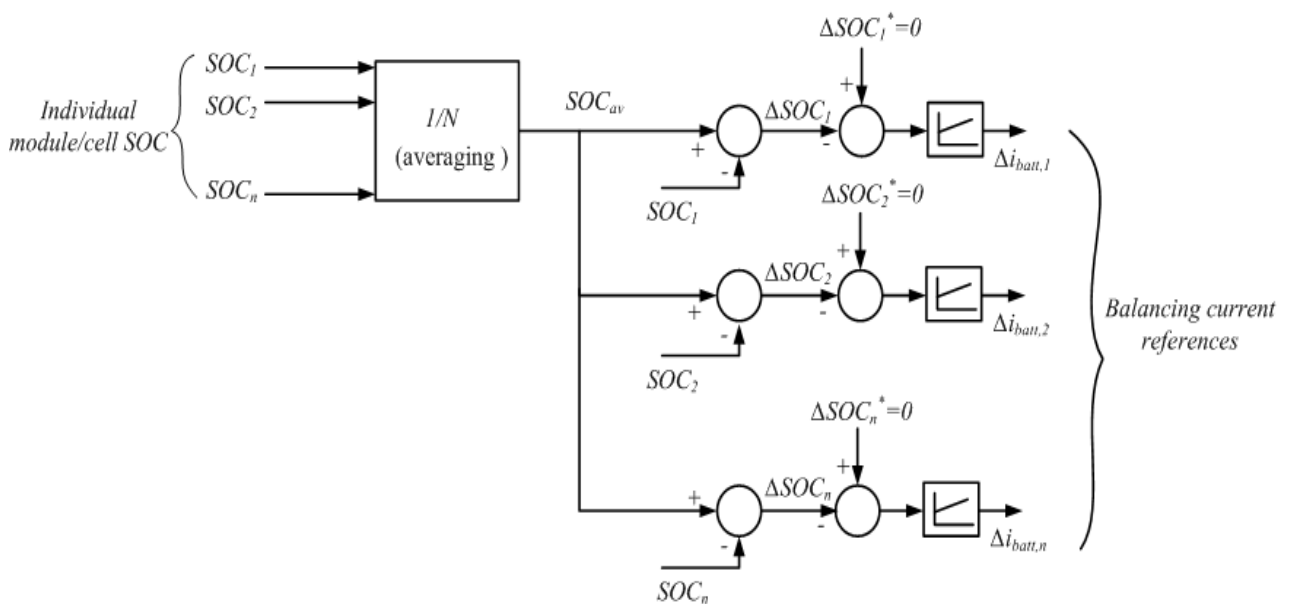


Fig. 1.9 An example of active SOC balancing control structure

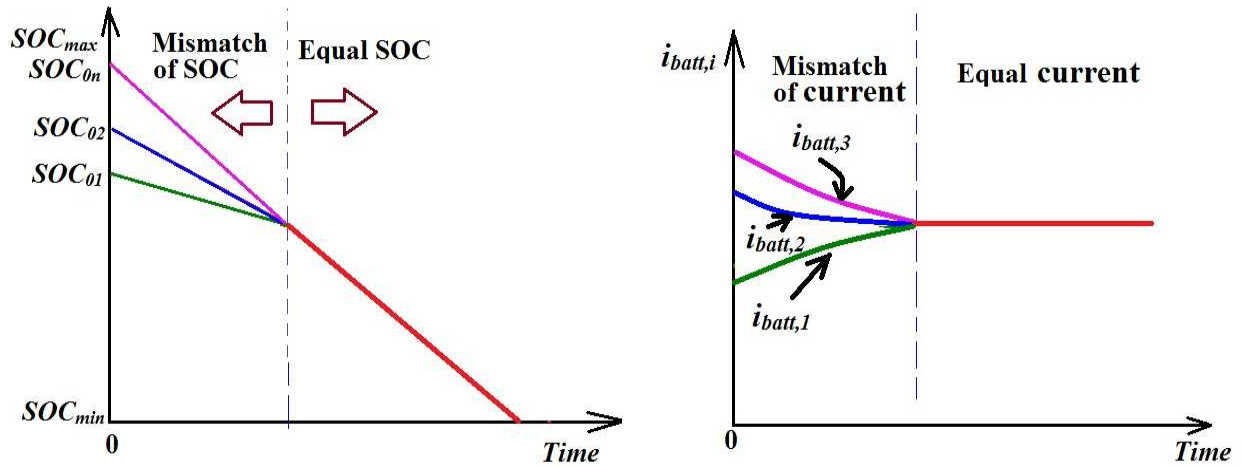


Fig. 1.10 Effect of equalisation or balancing control during discharging

It should be noted that this strategy is only applicable with the same type battery cells and assume equal capacity and charge/discharge limits but this will not be feasible if the battery capacity, charge/discharge limits are widely different. However, such a situation (dealing with widely different batteries) is not considered to be relevant in the existing literature. Within this thesis an active balancing through the BMS is used and passive resistive shunt type balancing method is used depending on battery types.

1.5.2 Power converter topologies

In a battery energy storage system, a bidirectional dc-dc and/or ac-dc converter topology with a proper charging-discharging control is required to transfer energy between the battery system and the ac grid. Different power converter topologies have been used in conjunction with BESS, hybrid energy storage systems in grid, power quality, automotive, UPS and DC-micro-grid applications have been summarised in [157] – [209]. Different applications use different converter topologies to interface with the utility grid system or with the load because the control flexibility, efficiency, power quality reliability etc. are dependent on choice of topology as discussed in the review [157]. The topologies may include a dc-dc converter on the battery side or could directly integrate the battery bank to an inverter. The topologies are split into two types: non-isolated and isolated converters. Isolated topologies are useful to obtain the galvanic isolation between ac grid and dc source which is mandatory in some of the applications, such as, aircraft, automotive for safety. However, this isolation increases the size and cost of the system as well as reducing efficiency of the overall energy storage system. In a grid system where fault current magnitude is important for protection co-ordination, it may be necessary to use a non-isolated system. Due to the nature of this thesis in providing grid support, a non-isolated configuration is taken as the main focus of this research and used in the following topology descriptions. However, the theory is equally valid for an isolated system. Moreover, the non-isolated converters offer advantages because these systems are lower in cost, size, more compact and more efficient than isolated topologies.

It is necessary to consider a wide range of topologies not just in BESS because topologies

applicable on hybrid energy storage system and PV applications are also quite relevant in BESS. In order to study all the converter topologies [157] – [209] used in BESS or in hybrid energy systems, they are divided into two broad areas: a) modular configurations, b) non-modular configurations. Non-modular configurations can be further divided into four groups: i) single-stage configuration using only a dc-ac converter between the battery bank and grid [160] – [167], ii) two-stage configuration which uses a front-end dc-dc converter before dc-ac converter to boost the battery voltage [169] – [178], iii) three-stage configuration where a high frequency transformer is used along with dual active bridges (DAB) in between the battery bank and dc-ac converter for the purpose of providing isolation as well as boosting the low battery bank voltage to the grid using the transformer turns ratio [192] – [196] and iv) topologies with cell bypassing [180] – [182]. The modular topologies can be divided into two groups: i) dc-side modular converters [183] – [190] and ii) ac-side modular configurations such as, cascaded H-bridge converters [192] – [206] and parallel converters [210] – [214] in high voltage applications such as, in medium voltage grid connection (3.3kV/4.16kV).

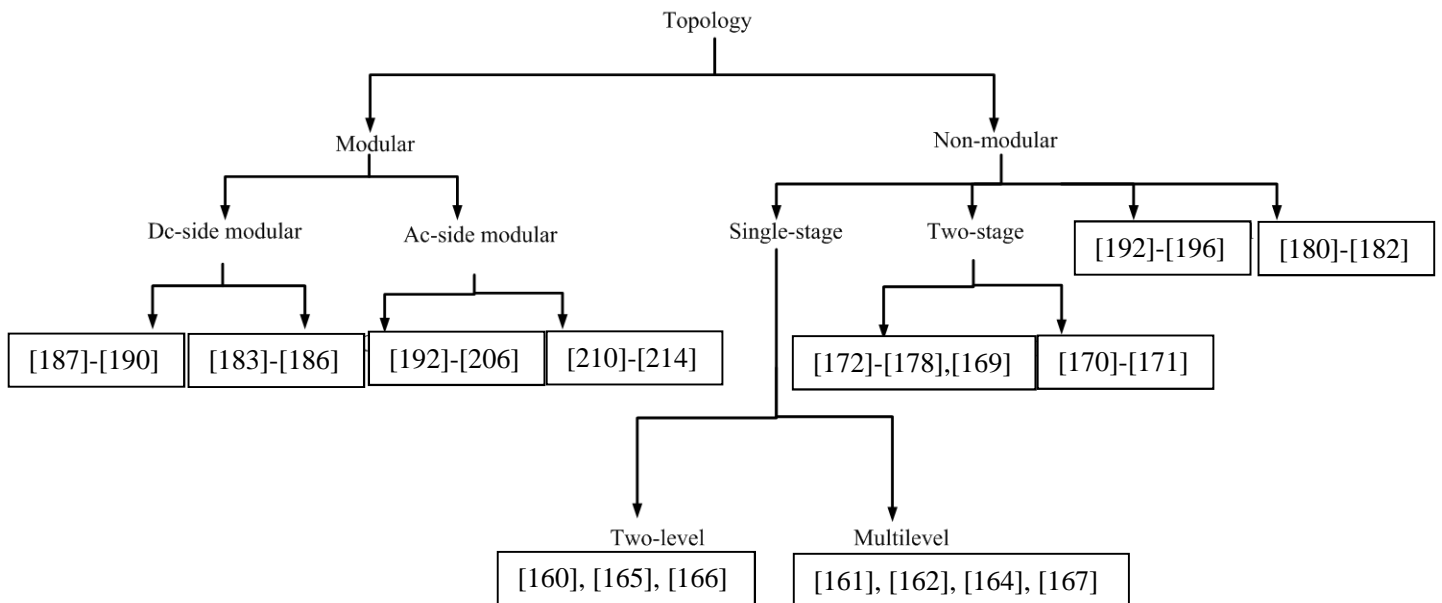


Fig. 1.11 Classification of different converter topologies bidirectional energy storage system

Some applications (e.g. wind energy or PV with battery storage) employ multilevel inverters (such as, NPC, flying capacitor multilevel etc.) on the grid side instead of H-bridge to integrate energy storage systems as described in [167] – [171]. Some published work on multi-stage or interleaved/coupled inductor based dc-dc converters on the battery side [173] – [176] to achieve high power quality, reduce switch stress and increase boost ratio. A comprehensive summary of the converter topologies has been presented in Fig. 1.11 with their different classifications. Each group is discussed separately in the following sections.

1.5.2.1 Single-stage

A single-stage configuration is commonly used in conventional BESS or energy storage systems especially where a large battery bank or a high input voltage (e.g. >400V) is

available [160] – [168]. The configuration is shown in Fig. 1.12 where a battery bank is directly connected across the dc-link of a bidirectional dc-ac converter before interfacing with the grid. Since it uses a single power conversion stage from the input to output, it is referred to as single-stage configuration. The principle advantages of this scheme are high efficiency due to single power conversion stage, straightforward control structure, a low number of switches/drivers, low complexities in power electronic stage. This topology requires a suitable number of series batteries to directly interface with the grid and cells of similar characteristics are needed. The main limitations of this topology are: a) the reliability of the converter is greatly influenced by the reliability of battery bank, b) a high dc-link filter capacitor is required to filter any AC-component of current from the battery bank (e.g. double frequency component in 1- ϕ systems), c) the modulation index of the line converter is entirely dependent on the battery bank voltage and can cause distortion in the line side current if the system is on over-modulation region in the case of a wide variation in the battery terminal voltage.

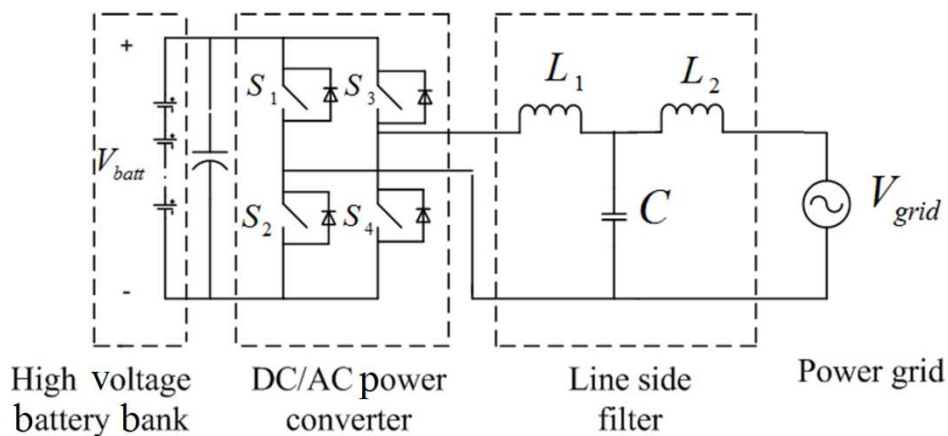


Fig. 1.12 Single stage BESS

1.5.2.2 Two-stage

Fig. 1.13 shows another widely used converter interfacing scheme for BESS suitable for a lower voltage battery bank, e.g. < 300 – 400V [169] – [178]. The main difference compared to the single-stage scheme is that a lower battery bank voltage can be used because a dc-dc boost converter decouples the main DC-link voltage of the inverter to the battery bank which ensures a stable dc-link voltage and allows the grid side power converter to operate over a wide and stable modulation index. Battery charging/discharging current can be controlled through the dc-dc converter which can also filter any AC-component drawn from the battery bank. However, due to the extra power conversion stage the efficiency of this interfacing scheme is lower than the single-stage configuration. This configuration also demands similar characteristics of cells.

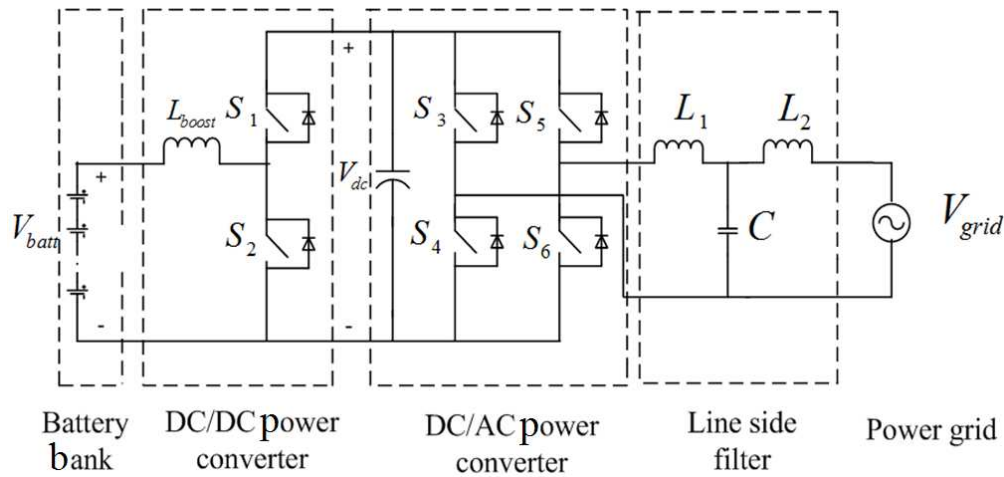


Fig. 1.13 Two-stage BESS

1.5.2.3 Three-stage

Another popular converter interface topology is the three-stage high frequency link converter based scheme as shown in Fig. 1.14 [177], [179], [192] – [196] primarily used when the isolation is important and when two or more sources share the same input voltage to avoid the circulating currents. This converter interfacing scheme uses dual active bridges where the dc voltage of battery is first converted to high frequency ac and then is again transformed back to dc before being inverted to the grid. This configuration provides isolation and necessary boosting from low voltage battery bank to the grid through the high frequency transformer. The main limitation of this topology is lower efficiency and potentially higher cost compared to single-stage or two-stage configurations due to the high frequency transformer, increased number of power electronic switches and drivers. This kind configuration is useful where isolation is mandatory for safety between the energy storage element and ac-source such as, in aircraft applications.

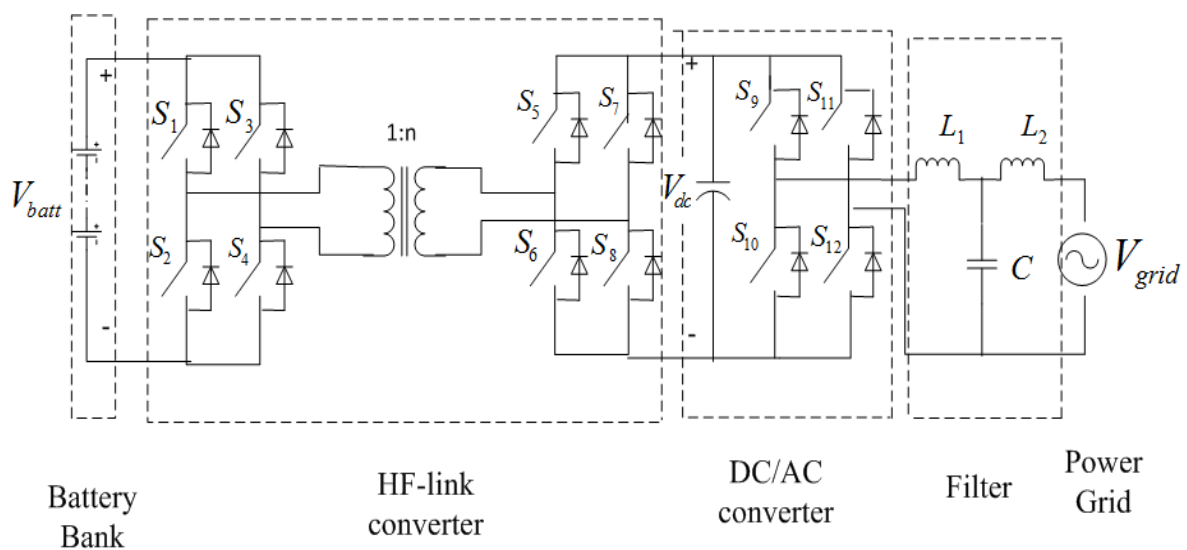


Fig. 1.14 Three-stage BESS based on high frequency-link transformer

1.5.2.4 Conventional topologies with cell bypassing

All the topologies mentioned above would require extra switches such as those in the two-stage converter in Fig. 1.13 to encompass a bypass capability in the event of cell failure. The two stage configuration can include cell bypassing capability through switches as shown in Fig. 1.15 [180] – [182]. This arrangement is sometimes referred to as a smart battery [180]. The main advantage of this configuration is faulty cells can be bypassed when required. This type of configuration is not usually used except in very low power levels (up to couple of Watts) for example in computers, smart phones where a few series connected cells are present because bypass switches over each cell increase the complexity and cost in a large series string of batteries.

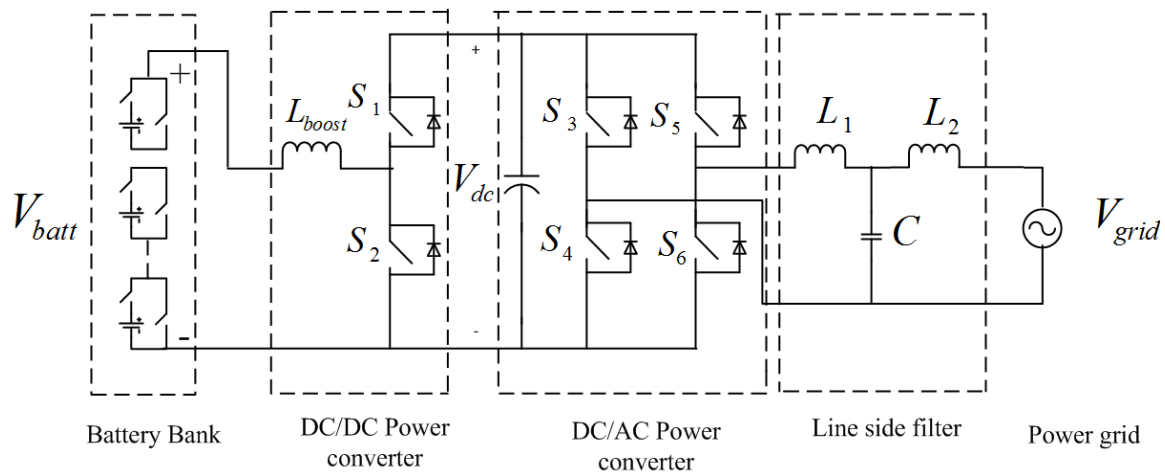


Fig. 1.15 Two-stage BESS with cell bypassing functionality

1.5.2.5 Modular Configurations

The modular configuration can be two types: a) dc-side modular with a line side inverter and b) ac-side modular converters. Therefore, these are discussed separately.

Dc-side modular converters: The dc-side modular converters achieve modularity through dc-dc converters. They are of two types: a) cascaded or series type and b) parallel type. This type of converters has been used both in energy storage and PV applications. Therefore, both are studied. The power circuit of parallel dc-dc converter based BESS are shown in Fig. 1.16(a) as reported in [183] – [186] while the cascaded or series type configuration is shown in Fig. 1.16(b) as reported in [187] – [188]. This type of converter is suitable to integrate heterogeneous dc-sources either of same type with different characteristics such as PV panels under partial shading conditions or different types to a grid-tie inverter or machine drive. It is a popular converter structure in PV applications such as reported in [189] – [190] because PV panels seldom have equal characteristics, as they are subjected to varied radiation conditions which causes differences in output power and modular dc-dc converters can be used to cater for such differences by controlling the individual module converters. However, in a conventional BESS, batteries do not have such significant differences in characteristics, and only a few researches [187] – [188] considered dc-side modular converters in BESS

applications. Predominantly a dc-dc boost converter is employed in dc-side modular configurations because for most of the cases as reported in [187] – [188], [189] – [190], the battery bank voltage or the input voltage (in case of PV panels) is considered lower than the central dc-link voltage of the inverter. The cascaded dc-dc converter provides advantages of lower cost (employing low rated semiconductors, magnetic components), higher efficiency and is lower in size compared to the parallel type converters for low input voltages [189]. However, the control and protection of parallel dc-dc converters are more straightforward than the cascaded dc-dc converters. Moreover, the parallel dc-dc converter structure is inherently fault-tolerant with respect to source failure compared to the cascaded or series type of dc-dc converters which needs additional bypass mechanisms to block the source failure.

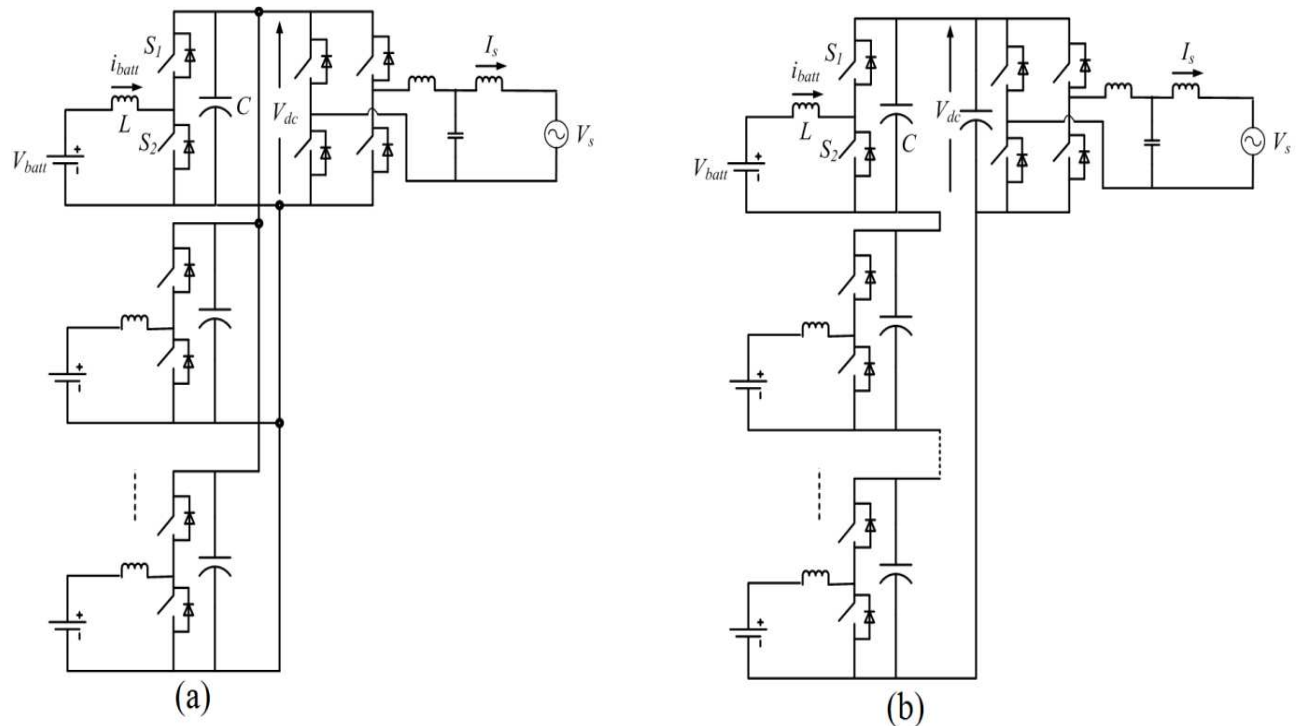


Fig. 1.16 Dc-side modular converters: a) parallel type, b) cascaded or series type

AC-side modular converters: Modular configurations like in Fig. 1.17 to Fig. 1.19 have received attention in high power (from 100's of kW to MW levels) or in medium-high voltage (3.3kV/11kV) grid connection [192] – [201]. Low dc-link voltage per module ($<1\text{kV}$), low switch stress and low number of series batteries/module are employed in this type of converters as shown in Fig. 1.17. The main advantages of this scheme are the inherent ability to bypass a module as shown in [202], high efficiency due to the low voltage semiconductors with lower on-state resistance (R_{dson}) can be used in each module. Apart from the reliability related advantages, the converter can have a smaller filter at the output before interfacing with the utility grid compared to single-stage or two-stage converters because of the multilevel voltages giving less harmonic content (i.e. better THD) at the output which reduces the overall size and cost of the converter.

Another type of modular converter configuration reported in the literature is cascaded H-bridge with integrated dc-dc converters [203] – [206] as shown in Fig. 1.18. The dc-dc converter can be a standard dc-dc boost converter or in some cases HF-link converter to achieve the necessary isolation. The principle advantage of this configuration is the less

number of modules are required to interface with the grid without a transformer because of the presence of the front-end dc-dc boost converter with each module. Moreover, a module battery current can be directly controlled using the dc-dc converter without depending on the line side converter and the overall dc-ac converter can operate in a wide modulation index. Traditionally each module of the cascaded converter is taken to be identical to each other in terms of battery voltage, battery type etc. However, both these kinds of modular topologies are capable of integrating heterogeneous energy storage systems together unlike single-stage, two-stage or three-stage configurations which gives them extra advantages like better reliability, more efficient over the traditional two-level design. Moreover, it is possible to independently control each module according to the characteristics of each module while providing necessary grid support which provides enhanced control flexibility. Therefore, these kinds of topologies are gaining popularity in hybrid energy storage system such as those reported in [207] – [209] where different types of sources like PV, batteries, super-capacitor or fuel cells are integrated together in a grid system.

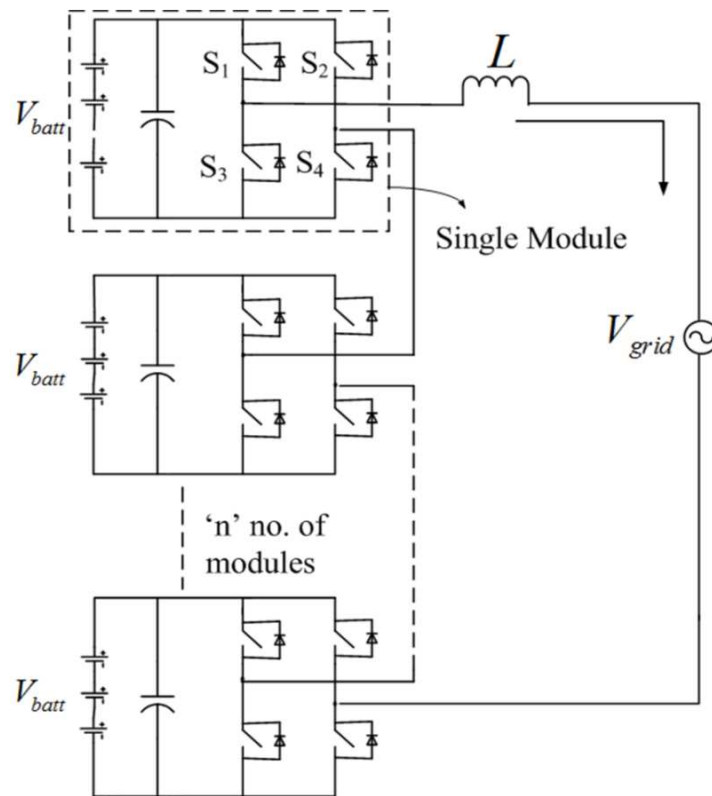


Fig. 1.17 AC-side modular: Cascaded H-bridge converter

Another widely used ac-side modular converter structure is parallel dc-ac converters which employ multiple parallel dc-ac modules instead of cascaded modules as shown in Fig. 1.19 [210] – [214]. This type of converter may or may not include a front-end dc-dc converter with each module before interfacing with the line side inverter depending on the available dc-voltage. This is a very popular converter structure in microgrid because of having multiple generating units. Main advantages of such structure are easier protection, high reliability, enhanced control flexibility and scalability as reported in these literatures. However, the main problem of parallel inverter based system is the load sharing, therefore, the main focus of

parallel inverter based has been confined to control among the multiple modules such as reported in [212] – [214].

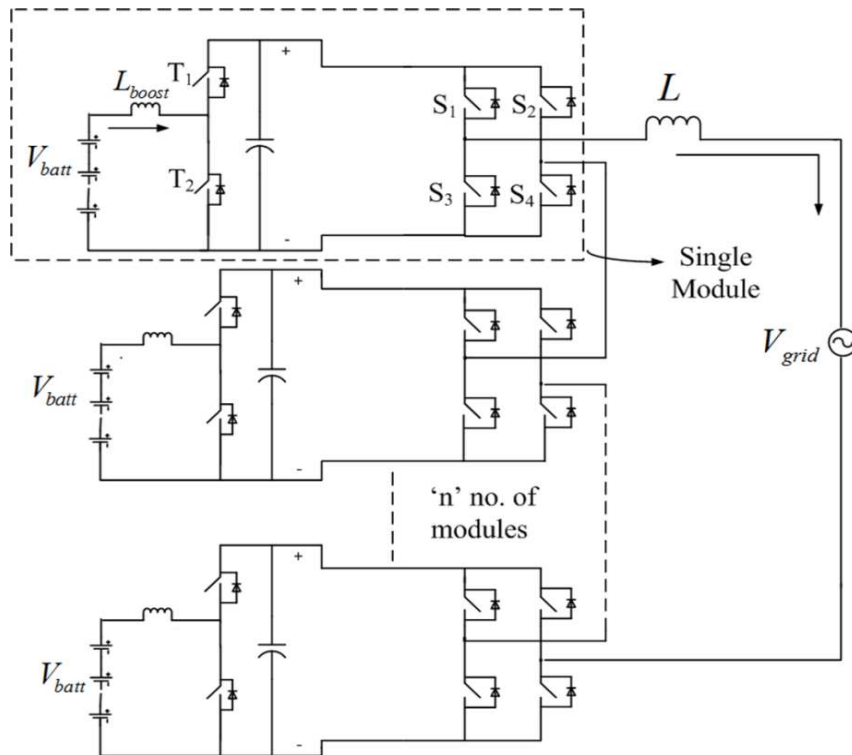


Fig. 1.18 AC-side modular: Cascaded H-bridge converter with integrated dc-dc converter

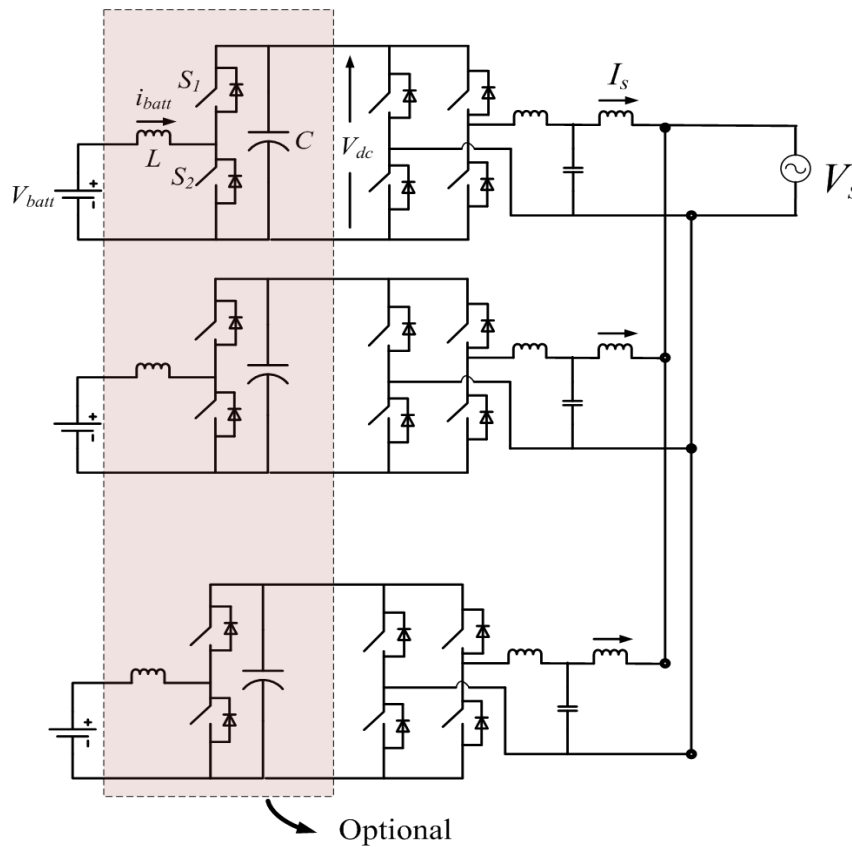


Fig. 1.19 AC-side modular configuration: parallel dc-ac topology

Table 1-3 Comparison of different configuration in BESS

converter type	Advantage	Disadvantage	Applications
Single stage [161] – [168]	Low number of switches and drivers, simple control, high efficiency	Low reliability of battery bank, high dc-link capacitor, less control flexibility	High battery voltage ($V_{batt} > 400V$) and high efficiency system (e.g. > 98%)
Two-stage [169] – [178]	Good control flexibility, low battery voltage	Reduced efficiency, higher cost than single-stage	Majority of BESS applications to date including renewable energy, dc-microgrid, PHEV, automotive
Three-stage [177], [179], [192] – [196]	Good control flexibility, low battery voltage and isolation from input to output	Reduced efficiency, reduced reliability, higher cost than single-stage and two-stage,	Aircraft, automotive etc.
Cell bypassing/smart batteries [180] – [182]	High reliability	more complex control, reduced efficiency	Low power applications such as, Laptops, smart phones, integrated circuits
Modular [183] – [209]	High reliability, high efficiency, flexible control capability	High number of switches, drivers, more complex control	High power applications and hybrid energy storage systems

A brief overall comparison between different types of configuration is given in Table 1-3. Within all these configurations it is possible to vary the topology of both the dc-dc converter and dc-ac converter within the topologies already discussed. Common variations on these converters are discussed for completeness in the next sections.

1.5.3 Dc-dc converters

Within the conventional converter classification there are many different topologies based on variations in design of each converter stage – a common example includes the variation in dc-dc converter topology from Fig. 1.13. This section provides some of the other variants of dc-dc converter family as discussed in [215]. A dc-dc converter can be of three basic types as shown in Fig. 1.20. A boost type converter (Fig. 1.20(a)) is used where the input voltage is lower than the output voltage. A buck type converter (Fig. 1.20(b)) is employed where the input voltage needs to be higher than the output voltage and buck-boost converter can be used where input voltage could be higher or lower than the output voltage. Among different types of dc-dc converters a buck-boost type of converter has a drawback of poor switch utilisation,

lower efficiency and higher cost compared to boost or buck type configurations [215]. A buck type module has not been found much application in grid-tie BESS because a high voltage battery bank needs only an inverter to interface with the grid without needing an additional dc-dc buck converter. On the other hand, a dc-dc boost converter has found an extensive application in BESS [216] – [234] and is the most commonly employed dc-dc converter in interfacing the energy storage system with the grid because energy storage systems or batteries predominantly have low module or cell voltage ($< 300\text{V}$) and it has a better switch utilisation and higher efficiency than a buck-boost converter. Moreover, it provides a continuous input current which eliminates the need of high input capacitor and makes it suitable in BESS or in energy storage systems. For these reasons a dc-dc boost converter has been discussed in detailed. There could be a wide range of dc-dc boost converter as reported in [216] – [234] which could be broadly categorised in five major groups as shown in Fig. 1.21. Each one has its own advantages, drawbacks and applications as discussed briefly in the following section.

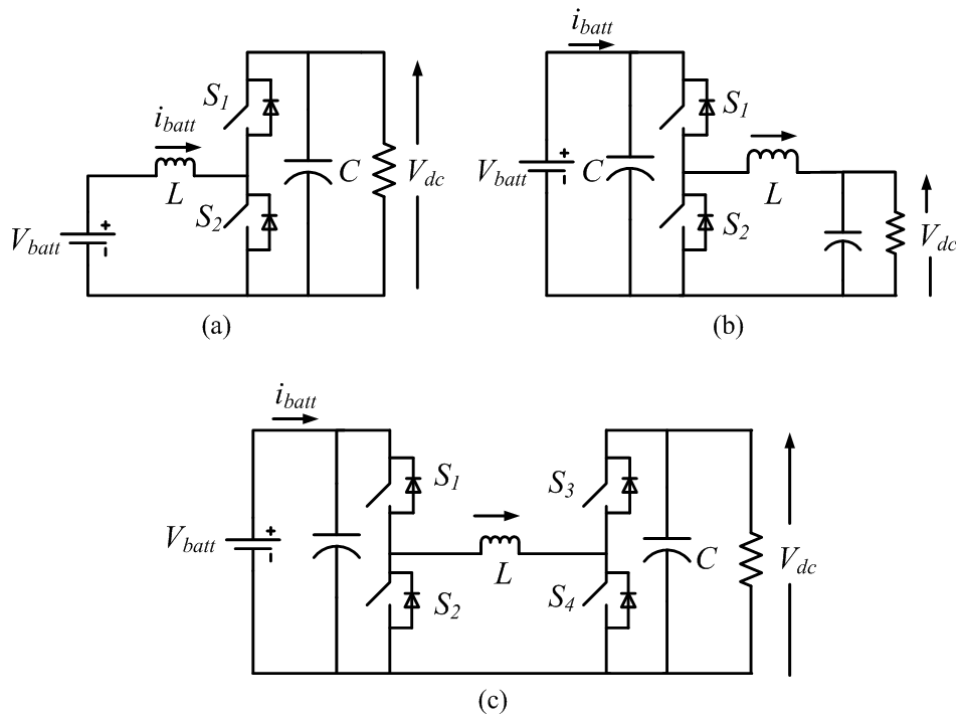


Fig. 1.20 Family of bidirectional dc-dc converters: a) boost, b) buck, c) buck- boost

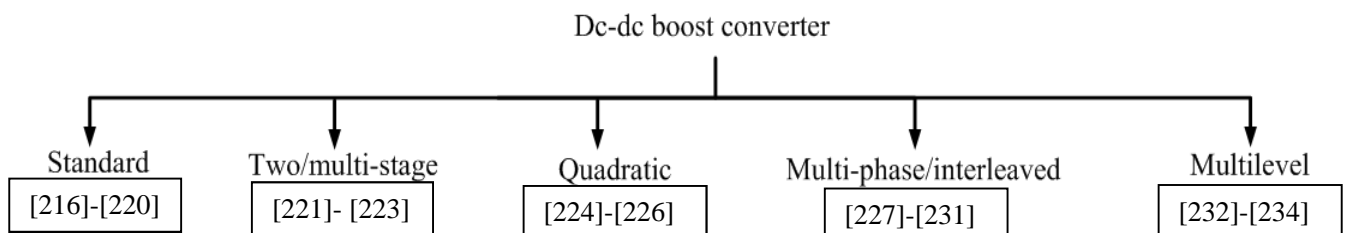


Fig. 1.21 Classification of different dc-dc boost converter topologies

1.5.3.1 Standard DC-DC boost converter

The switches S_1 and S_2 are switched in complimentary fashion in boost converter in Fig. 1.20(a). This converter performs well for low-medium boost ratios (3-6) depending on the

input voltage such as shown in [216] – [220]. However, the performance such as input current ripple increases and switch utilisation, efficiency starts to degrade in higher boost ratio (>10) applications. Moreover, a high input side current ripple current may impact the battery life in BESS, increases noise and a high boost ratio (> 10) demands a high boost inductor (e.g. 5 – 10mH) which can make the system bulky/costly and causes poor dynamic response from control point of view.

1.5.3.2 Multi-stage DC-DC boost converter

A multi-stage dc-dc converter can provide a higher boost ratio with lower inductor current ripple using two or multiple dc-dc converters in cascade (i.e. connecting the output of one stage as an input of another). Some of them are given in [221] – [223]. The converter structure is shown in Fig. 1.22. Each stage can have a lower boost ratio which leads to a lower inductor current ripple and better switch utilisation while achieving a high overall boost ratio from the input to output. However, a multiple number of power stages cause a lower overall system efficiency because the total system efficiency is a product of individual power stages.

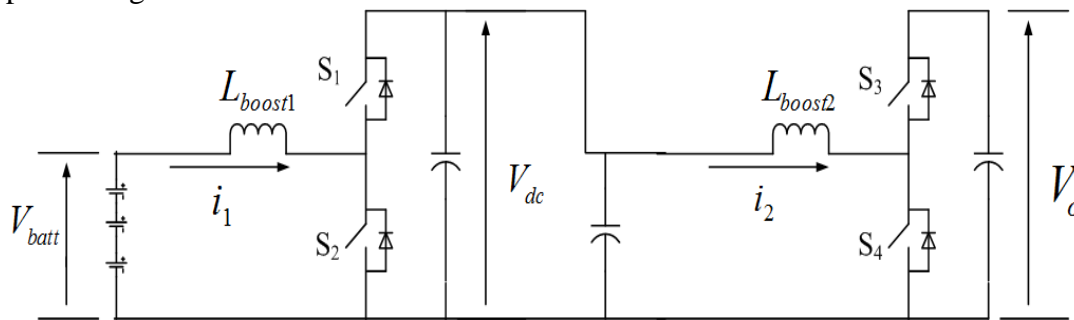


Fig. 1.22 Two-stage dc-dc converter

1.5.3.3 Quadratic DC-DC boost converter

A quadratic dc-dc converter is shown in Fig. 1.23 and is similar to a cascaded structure and also suitable for high boost ratio applications (> 10) such as in fuel cell where a low voltage input source is available, for example reported in [224] – [226]. S_3 and S_4 are the main power switches which are used in complementary fashion. The detailed operation of this converter is reported in [224] – [226]. Performance of this converter is similar to a two-stage dc-dc converter. Moreover, an additional advantage of the quadratic boost converter is, a coupled inductors (e.g. $L_{boost,1}$ and $L_{boost,2}$ in Fig. 1.23 could be coupled) can be used to achieve a high boost ratio (e.g. 20) such as shown in reference [225]. However, increased magnetic components can cause the overall converter to be bulky and poor efficiency.

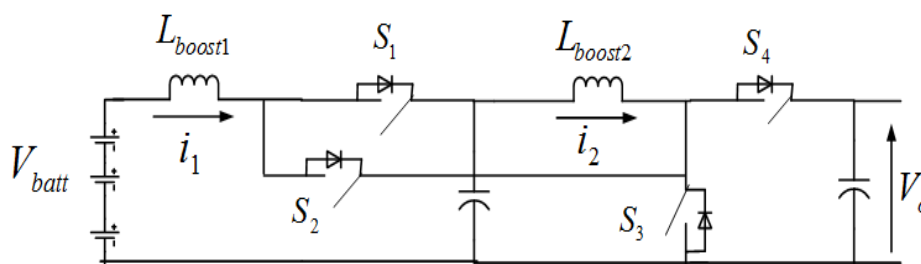


Fig. 1.23 Quadratic boost dc-dc converter

1.5.3.4 Multiphase DC-DC boost converter

Multiphase dc-dc converters are commonly employed in low voltage, high current, high boost ratio applications such as reported in [227] – [231] to reduce individual inductor current rating and current ripple using multiple inductors in each leg as shown in Fig. 1.24 which shows a two-phase system. This type of configuration has applications in automotive, aircraft and certain energy storage system such as, super-capacitors which are predominantly low voltage and high current applications. An interleaved or ripple cancellation technique using phase shifted carriers among the parallel half-bridge legs is often used to reduce the total input current ripple drawn from the energy storage element. This reduced current ripple in turn helps to reduce the size of magnetic components and to increase the effective switching frequency. However, the problem of current sharing among the inductors is one of the challenges of this topology which makes the control more complicated compared to other types of dc-dc converters.

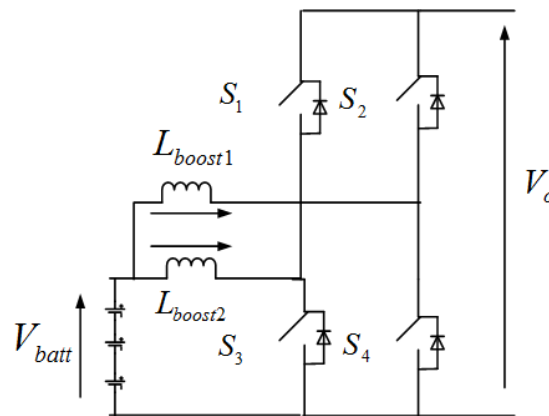


Fig. 1.24 Two-phase dc-dc converter

1.5.3.5 Multilevel DC-DC boost converter

Multilevel boost converters have received some attention in the literature in high voltage, high boost and/or high power applications compared to a traditional dc-dc boost converter because of the size, cost and efficiency related reasons. These types of converters have an advantage of achieving higher output voltage levels using less magnetic components e.g. a single inductor as shown in Fig. 1.25. The principle advantage of this structure is the ability to produce multilevel (here two levels) output $V_o = 2NV_{batt}$ where ‘N’ is the boost ratio, and $V_o = 2V_{batt}$ using different switching states [232] – [234]. However, it uses more switches than a conventional dc-dc converter but at a lower voltage. Moreover, the multilevel operation helps to reduce the size of the boost inductor compared to a traditional boost converter because the effective switching frequency can be increased. Due to having multiple voltage levels, it is suited with multilevel inverters such as, NPC or flying capacitor converters as reported in [235]. This dc-dc converter structure is best suited at power levels greater than 50kW and at voltage levels more than 1kV because low voltage, low cost switches, drivers, magnetics components can be used which helps to reduce the cost and enhances the converter efficiency.

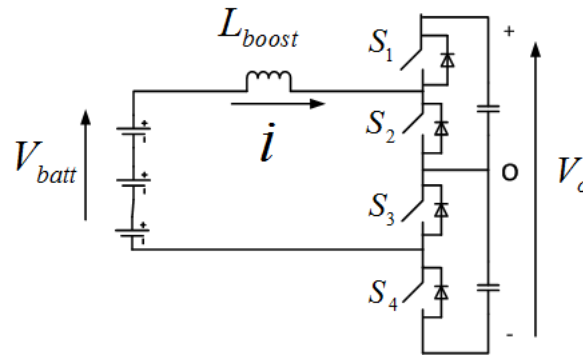


Fig. 1.25 An example of multilevel dc/dc converter

A summary of different dc-dc converter variation has been shown in Table 1-4 to help understanding their relative advantages and disadvantages.

Table 1-4 Comparison of different types of dc-dc boost converter

dc-dc converter type	Advantage	Disadvantage	Applications
Standard boost [216] – [220]	Low number of switches and drivers, simple control, low number of inductor/capacitor	Low efficiency, high current ripple and poor switch utilisation at high boost ratio	Low-medium boost ratio applications such as in BESS. Modular converters
Two-stage (cascaded) [221] – [223]	High boost ratio (> 10) at low current ripple, low inductor size	Poor efficiency if multiple stages are present	Low input voltage applications such as, fuel cell, PV
Quadratic boost [224] – [226]	High boost ratio (>10), low number of switches, good switch utilisation	Bulky due to increased magnetic component, low efficiency	Micro-source application such as fuel cell
Multi-phase boost [227] – [231]	Can handle high current, low current ripple, high efficiency ($> 95\%$)	High number of switches and drivers, high number of inductors, control complexity	Automotive, aircraft, super-capacitor based ESS
Multilevel boost [232] – [234]	Low current ripple, low inductor size, can handle high boost ratio	High number of switches and drivers, high number of capacitors	High power ($> 10\text{kW}$), medium-high voltage ($> 1\text{kV}$) applications in conjunction with multilevel inverters

It can be seen that the advanced dc-dc boost converter topologies are employed in high boost ratio, high power, and high current applications. However, it is not very common to employ these kinds of dc-dc converters in modular converters because modular converters generally

have multiple modules connected in cascade or parallel where each module should be low in size, compact and is not desired to handle a high boost ratio, high switch stress or high current. Therefore, predominantly the application of these types of dc-dc converters has been confined in non-modular configurations to date.

1.5.4 Dc-ac Converters

Two-level converters (Fig. 1.12.) have been used extensively in energy storage systems and DER applications, for example those reported in [172] – [178], [169], [236] – [240]. The two-level converters can be of single phase type and of three-phase type depending on applications. The application of single-phase two-level inverter is mainly confined to low power applications (<10kW) because of the current limitation of the devices in single-phase system. On the other hand, three-phase converters find application up to 100 kW power levels. However, it is impractical to use these type of converters in high power applications (> 100kW to MW) because of available semiconductor rating and switching frequency limitations at such power levels.

In order to address these issues with two-level converters, multilevel converters have found extensive application in high power motor drives application such as those reported in [241] – [243] and have also been receiving attention in renewable energy systems and energy storage systems too [244] – [246], [170] – [171], [161], [162], [164], [167]. Multilevel converters have multiple advantages over the conventional two-level design such as: potentially higher efficiency, higher reliability, better power quality, reduced EMI and reduced switch stress. However, it has disadvantages like: a larger number of power switches and drivers, increased control complexity and the need for multiple isolated dc sources.

Several topologies have been proposed for multilevel converters which could be broadly categorised into three distinct groups: a) diode-clamped converter (also known as neutral point clamped/NPC), b) capacitor-clamped converter (or Flying capacitor) and c) cascaded converter (also known as a chain-link converter). Each one has specific applications, advantages and drawbacks which are discussed in a survey reported in [241].

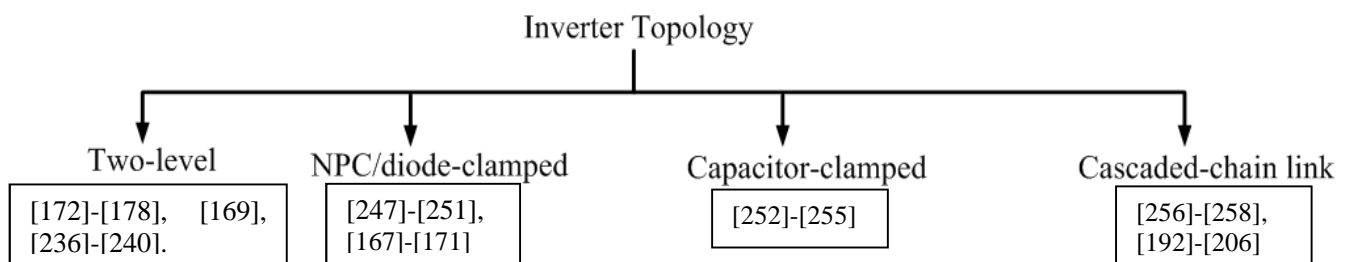


Fig. 1.26 Classification of different inverter topologies

1.5.4.1 Diode-clamped/NPC Multilevel Inverter

Fig. 1.27 shows a three-level diode-clamped topology also known as neutral-point-clamped (NPC) which was proposed first in [247]. It was the first widely used multilevel converter in industrial applications and had been continued to be extensively used in many applications such as industrial drives, FACTS devices [248]. Later, the NPC inverter was generalised for a

higher number of levels using the same concept resulting into the current designation of a diode-clamped converter. For ‘N’ level converter, it requires $2(N-1)$ switches, $(N-1)$ $(N-2)$ clamping diodes, $(N-1)$ capacitors. This type of converters have been receiving attention in recent years as a line side inverter in conjunction with BESS and other ESS applications as reported in [167] – [171] for its potential advantages over the conventional two-level inverters at high power or medium voltage grid applications.

The disadvantage of this topology is the necessity for capacitor voltage balancing (floating of neutral point ‘o’) when the capacitors are floating [249] – [250]. Apart from this, the clamping converter structure requires clamping diodes in order to clamp the voltage to particular levels which may increase losses especially in high-current applications. However, this drawback can be overcome using an Active Neutral Point Clamped (ANPC) converter which uses extra switches in the place of diodes which helps in reducing the overall loss and increases the efficiency of the converter [251].

1.5.4.2 Capacitor-clamped/Flying Capacitor based multilevel inverter

The structure and characteristics of this type converter are dual of diode-clamped (NPC) converters. This structure does not require additional diodes but requires additional capacitances in place of diodes to clamp the voltage as shown in Fig. 1.28. This topology has several attractive properties compared to the NPC converters, such as: a) more redundant switching states which provide the opportunity to distribute the switching stresses equally among the semiconductor devices, b) these redundant switching states can also be used to enhance the fault-tolerance/ reliability as reported in [252]. For ‘N’ level converter, it requires $2(N-1)$ switches, $N(N-1)/2$ clamping capacitors. However, the capacitor voltages are required to be maintained all the time. Therefore, this converter finds a wide application where the reactive power support is necessary such as in power quality applications as reported in [253] – [255]. It can also be used in active power support applications provided the capacitors are fed from isolated dc-sources. However, it needs separate dc-sources for each capacitor which may not be available all the time. For this reason it has not received much attention in energy storage systems compared to the NPC type converter where active power support is more important.

1.5.4.3 Cascaded Multilevel Inverters

Cascaded H-bridges are used within this topology. This topology has been shown in Fig. 1.17. The main advantages of this configuration are: least number of components/switches (including diodes) among the topologies, and fault-tolerant/modular structure. For ‘N’ level converter, it requires $2(N-1)$ switches and $(N-1)/2$ capacitors. This configuration has been extensively used in utility application, renewable energies like PV, Fuel Cell as well as in FACTS devices for its potential advantages over other type of converters when there is multiple dc-sources present as reported in [256] – [258], [192] – [206].

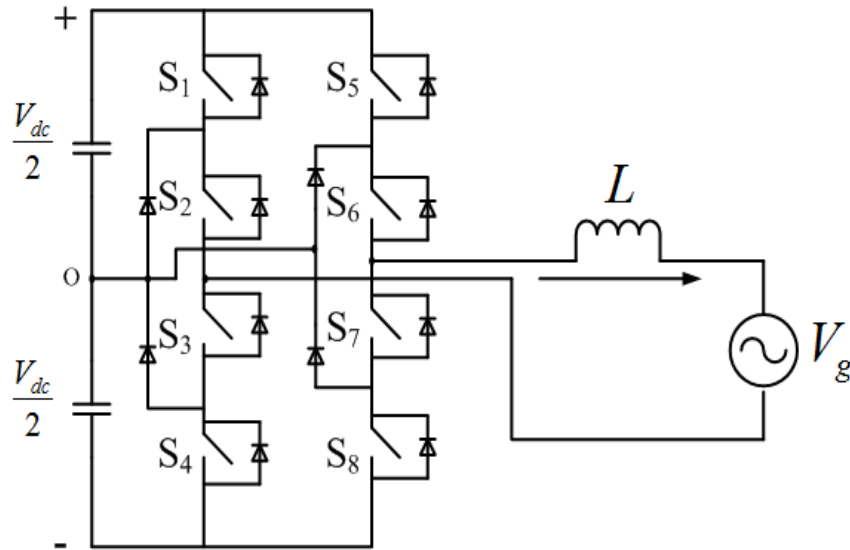


Fig. 1.27 Diode-clamped or NPC multilevel converter

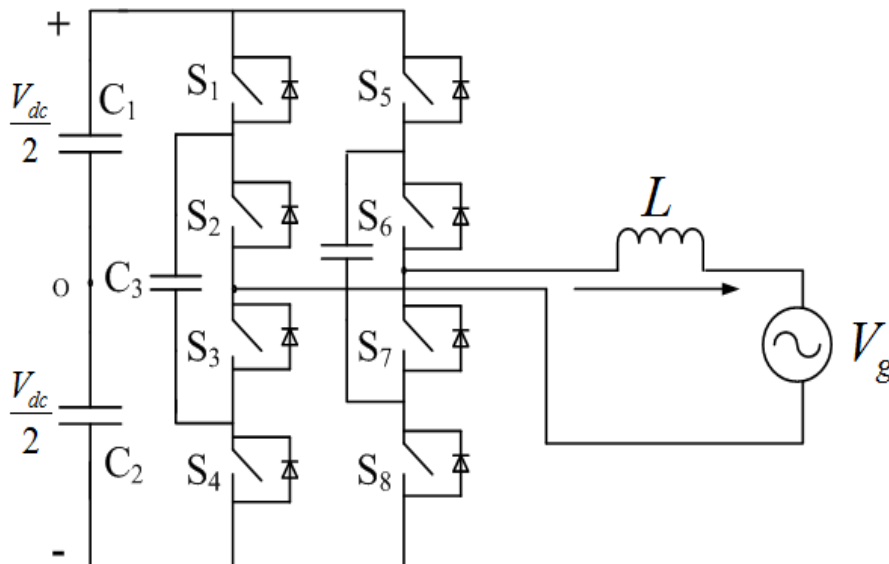


Fig. 1.28 Capacitor-clamped multilevel inverter

However, the multilevel inverters like NPC and flying capacitor are seldom considered in modular converters as a module because each module in modular converter is not desired to handle high voltage or high power such as reported in [256] – [258], [192] – [206]. Predominantly two-level configuration (e.g. a full bridge or a half bridge) is considered in one module. This thesis mainly looks at low voltage grid connection (either 230V for single phase or 415V for three-phase), therefore, NPC type or flying capacitor type configurations have not been considered.

Table 1-5 Comparison of different dc-ac converter topologies

Dc-ac converter type	Advantages	Disadvantages	Applications
Two level [172] – [178], [169], [236] – [240]	Simple control scheme, low number of switches/drivers – low complexity	Unavailability of semiconductor devices at higher power and higher voltage levels, high EMI, higher filter size	Pre-dominantly at 230V or 440V and level up to 100kW power levels.
Diode-clamped (NPC) [247] – [251]	Low switch stress, low EMI, single dc-source is required	Large no. of clamping diodes, uneven loss distribution between switches and diodes	High or medium voltage (3.3kV/11kV) grid connected renewable energy system such as wind power, medium voltage drives, high power HVDC
Flying Capacitor [252] – [255]	Low switch stress, low EMI, fault-tolerant due to having multiple redundant switching states	Large no. of clamping capacitances or isolated dc-sources are essential	Reactive power compensators such as active power filters, FACTS devices
Cascade/chain-link [256] – [258], [192] – [206]	Fault-tolerant, enhanced reliability due to modular in structure, enhanced control flexibility	Large no. of isolated inputs or dc-sources is required	Medium voltage drives such as open-end winding induction machine system, modular ESS, hybrid energy system, renewable energies such as PV system

1.5.5 Power converter control

The converter control is an important part in the BESS because it influences the direction of power flow, speed of response, type of grid support, stability, and also battery lifespan. The overall control of a battery energy storage system can be broadly divided into three stages: a) active balancing control (if applicable) as discussed in 1.5.1, b) dc-side or dc-dc converter control and c) dc-ac converter control or line side converter control.

1.5.5.1 Control of BESS

Dc-dc converter control: Previous work has concentrated on energy storage systems with batteries in conjunction with other power sources such as wind and PV where the energy storage medium is used as a mechanism for either smoothing the power from the system or to

compensate power mismatch between generation and the required dispatched amount through dc-dc converter control [217] – [218]. The dc-dc converter's power reference (in terms of voltage or current) is generated to compensate the mismatch between the load and the generation. A cascaded control loop consisting of an outer and inner loop has been employed to control the converter associated with the battery. In some cases, a battery/super-capacitors combination is used in a hybrid energy storage system to increase the battery useful life especially in automotive applications [219] – [220]. These researches have also considered a single type of battery with a single dc-dc converter and have mainly concentrated on optimizing the performance of each source.

Dc-ac converter control: Most of the past work in BESS has focused on ac-side control rather than on the dc-side control in keeping with the single-stage, two-stage or three-stage topologies of Fig. 1.12, Fig. 1.13 and Fig. 1.14. In those researches a single battery bank has been used in grid support applications and has predominantly concentrated on the line side or inverter control system to provide a frequency support [259] – [260], voltage support [261], to act as a power quality conditioner [262] in applications such as in DVR (Dynamic voltage restorer), renewable energy applications [217] – [218]. In all these researches the performance implications on the batteries have been ignored.

1.5.5.2 Different types of controller in power converter

The different control methods were discussed in the literature to control the power converter both in BESS and in other energy storage applications: a) linear control such as proportional-integral (PI) control, b) proportional-resonant (PR) control, c) non-linear control, such as sliding mode control, Lyapunov based control, sigma-delta modulation method and hysteresis control.

PI control is the most widely used control method for dc-ac converters as well as dc-dc converters [217] – [222], [259] – [262]. Although the PI control can provide good dynamic response with zero steady-state error, its direct applicability is limited to a dc-system as it can handle only dc errors. It can be used in ac-system also with a proper transformation such as Park Transformation. However, this indirect approach increases the control computation. Moreover, it has poor disturbance rejection capability which means if a system has some low frequency oscillations, the PI controller cannot fully mitigate against that as reported in [263].

The drawback of PI controllers in mitigating the low frequency oscillations and applicability in ac-system was overcome by introducing PR (proportional resonant) controller which produces high gains (ideally infinite gain) at the desired frequencies to produce better disturbance rejection capability and to eliminate the steady state error in case of any low frequency oscillation present as reported in [264] – [269]. However, this control scheme suffers from two drawbacks: a) the numerical accuracy in actual implementation because the accuracy of this control method depends on the magnitude of resonance peak which is difficult to implement some time because a high resonance peak or a very high is prone to enhance the system noise inside the digital controller and b) the application is only limited to a dc-ac converters because it can handle only ac errors.

In control theory, sliding mode control is a nonlinear control method that alters the dynamics of a nonlinear system by application of a discontinuous control signal that forces the system to "slide" along a cross-section of the system's normal behavior. Sliding mode is a variable structure control method as described in [270] – [275]. It provides fast dynamic response and robustness to parameter variations, but it is difficult to design and analyse the control performance and stability by applying conventional feedback method [275]. Therefore, its application is limited in power electronics. For similar reasons, this thesis does not look at using the sliding mode control.

The hysteresis band control is often used in power converters in various applications starting from machine drives, grid connected to standalone systems very often because it is straightforward to implement and generate switching signals with minimum computation [276] – [281]. It also provides a fast tracking performance (i.e. a fast dynamic response) because it controls the tracking error on an instantaneous basis. Also, besides fast dynamic response, the method does not need any knowledge of load parameters. For this reason it has received attention pre-dominantly in current control loop in power converters where it requires a fast response. However, the current control with a fixed hysteresis band has the disadvantage that the PWM frequency varies within a band because peak-to-peak current ripple is required to be controlled at all points of the input voltage. If input voltage varies in a wide range the switching frequency also varies in a wide range. It can be used in both dc-dc converter and also in dc-ac converters. However, it makes the switching frequency variable according to the input voltage. This variable switching frequency spectrum makes the output filter design challenging. There have been some research on adaptive hysteresis control which aim to keep the switching frequency constant by varying the hysteresis band according to the input voltage for example reported in [282] – [283] but it may sacrifice the overall control bandwidth compared to the fixed hysteresis band control (because the switching frequency is made fixed) and also may lead to additional complexities in calculating the accurate hysteresis band. Therefore, it is not used in this thesis.

Sigma-delta modulation is another type of control method used in power converters as reported in [284] – [285]. However, this type of control is pre-dominantly used in very high frequency applications such as audio frequency range (in MHz) and not a common method of controlling power converters. Such frequency range is not considered in this research and therefore, it is not considered in this thesis.

Lyapunov based control has been reported as an alternative to the PI based approach in certain applications [286] – [290] where conventional PI control approach has proven to be providing a slow dynamic response in order to maintain stability and good power quality. The main advantage of this control is the guaranteed stability along with a fast dynamic response. However, the application of this approach is limited in power electronic application because of the complexity of the design and difficulty in finding an appropriate Lyapunov function to meet the control requirements.

Table 1-6 Comparison of different controller

Controller type	Advantages	Disadvantages	Applications
PI/PID [217] – [222], [259] – [262]	Straightforward design and easy tuning	Poor disturbance rejection capability, cannot mitigate low frequency oscillation	Range of dc-dc, dc-ac converters
Proportional Resonant (PR) [264] – [269]	Good disturbance rejection capability, good for mitigating harmonics	Accuracy depends on resonance peak which can vary and difficulty in implementing accurately because of noise	Grid connected inverters, matrix converters
Sliding Mode [270] – [275]	Robust and fast dynamic response	Difficult to formulate, design and implement	Very limited
Hysteresis [276] – [281]	Fast dynamic response and simple to implement	Variable switching frequency spectrum, EMI problem	dc-dc buck converter, multilevel inverters, motor drives especially in DTC (direct torque control) based system
Adaptive Hysteresis [282] – [283]	Fixed switching frequency	Difficult to get an explicit expression of hysteresis band and design	Machine drive system and grid connected converter
Sigma-delta [284] – [285]	Very high switching frequency is achievable and also simple to implement	High switching loss in high power applications and also difficult to design driver at this frequency range.	Audio frequency and wireless power transfer applications
Lyapunov [286] – [290]	Stable, robust and fast dynamic response	Difficult to design and to find a Lyapunov function	Limited - PFC converter, active power filters

The comparison of different types of controller has been shown in Table 1-6 with their relative advantages and disadvantages. This thesis adopts a PI based approach on the dc-side for the initial part of the study for simplicity and accuracy but in later parts of the study shows the limitations of PI-controller based approach in certain circumstances because of stability reasons and therefore, employs a Lyapunov based nonlinear control design approach to mitigate that. A rotating frame based approach in 'dq'-domain using a PI controller is used

on the ac-side throughout the study for grid support applications which provides a fast dynamic response and accurate reference tracking.

1.6 Introduction to second life battery energy storage system (SLBESS)

Conventional BESS mostly use new batteries as an energy storage element. The main drawback to more widespread use of conventional BESS is the cost. If cost issues can be overcome, battery energy storage systems could have multiple benefits which include deferral of system upgrade, optimisation of renewable and improving power quality. Therefore, investigation has started in recent years into re-use of the EV/HEV batteries in grid support applications after their primary usage in the vehicle [291] – [295].

There are several figures from a number of sources including the DECC and Arup and Cenex reports indicate anything from 70,000 to 2.6 million electric and hybrid vehicles on the road by 2020 [296]. Once the vehicle battery has degraded to around 70-80% of its capacity it is considered to be at the end of its first life application. Assuming a battery capability of around 5-18kWhr (MHEV 5kWh - BEV 18kWh battery) and a 10 year life span, this equates to a projection of battery storage capability available for second life of >1GWhrs by 2025. There is a significant interest in industry (e.g. ABB with GM, Sumitomo Corporation with Nissan) also in using second life batteries in an energy storage system [297] – [299]. With so many more electric cars on the road, reusing the battery would increase the overall value and green credentials of the car. It might also give a boost to the renewable energy market and the current generation of secondary application batteries will fulfil the requirements for many applications such as grid frequency support, voltage support, off-grid applications such as feeding an islanded microgrid etc. However, although several potential applications exist for secondary use the financial cost needs to be balanced against the income generation.

In the coming years, particularly as the electric and hybrid vehicle market grows there could be a substantial market of second life batteries. The challenge is establishing the supply chains that can take redundant relatively good performance batteries (which have sufficient amount of capacity left) from the automotive and transportation markets and extract maximum value for secondary market applications, from collection, testing and qualification, to modification, refurbishment and reselling of batteries. In addition to large global industrial firms such as Siemens and ABB, other specialist companies are well placed to help establish a second life battery market. The likely recycling route for ex-transportation batteries is that the vehicles will be returned to the manufactures and they will supply the batteries directly or pass the batteries through contracts to a battery re-cycler as shown in Fig. 1.29. The battery will be stripped down into modules and tested before being leased or sold on for a second life application. It is probably impractical to strip the batteries down to cell level, however, within a vehicle there are likely to be modularized units which the battery can easily be reduced into. These modules will be likely tested and sorted at the recycler or manufacturer before being sent on for a second life application.

1.6.1 Key Advantages

Key advantages of 2nd life batteries include

- It lowers the effective cost of batteries by introducing a realizable residual value, maximizes the use. Moreover, it is possible to lower the cost of integrating renewable energy into the electric grid through low-cost energy storage, contributing to the reduction of greenhouse gas emissions (e.g. CO₂) by assisting with electrifying transportation in its first life and enabling renewable energy in its second life.
- Uninterruptible power supply (UPS), for example for hospitals, cell phone towers and data processing centers, as a potential applications where these batteries could be used to provide a cleaner solution compared with diesel generation with low maintenance costs.
- Multiple grid ancillary services as discussed in section 1.2 can also be met using these batteries into the grid system

There has been a recent study by multiple organisations on technical feasibility and financial viability in the UK as reported in [300]. According to that, different services are presented in Table 1-7 where second life batteries could be used. Among the different services, the firm frequency response (FFR) as indicated in Table 1-7 is the most profitable service.

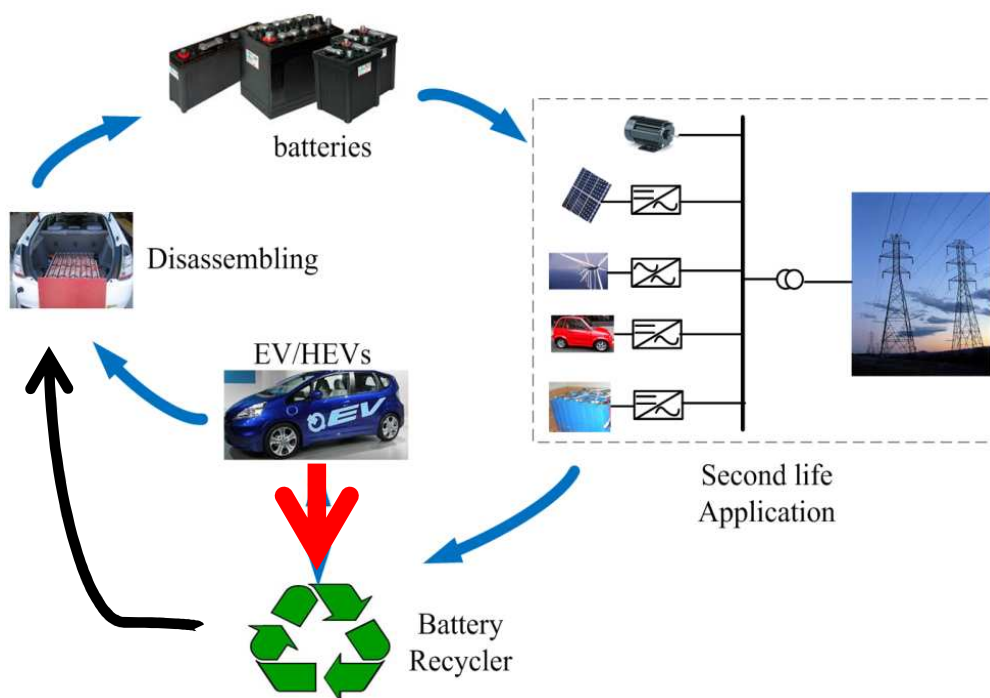


Fig. 1.29 Second life battery supply chain

1.6.2 Challenges of SLBESS

The reliability and performance of these batteries are not clear and are certainly lower than a new battery. Manufacturers indicate that a mixture of gradual degradation and sudden failure are both possible and failure mechanisms are likely to be related to how hard the batteries were driven. The condition of the batteries at the point of second life application, even if they are of the same type and from the same manufacturer, will be dependent on driver behavior and first life drive cycle.

Table 1-7 Revenue stream

	Day/night standard tariff	TRIAD tariff	Red DUOS rate	STOR	FCDM	FFR	Network charging /discharging
Description of service	Standard contract	Pass through contract	Pass through contract	Manually instructed switch on/off	Automatic - grid freq. measurement	Automatic grid freq. measurement	Charging off peak - discharging peak
Can it link with other services?	Yes	Yes					FFR, FCDM, etc.
Availability window				Specified grid by	Any	Any	5.30-10.30pm
Time required for (minutes)				12	30	30	300
Minimum size / capacity (kW)				3,000	3,000	10,000	375
Frequency of use	Daily	TRIAD warning periods	Daily	3 times/week	1,500 events/year	1,500 events/year	Daily – 4 months/year

Most profitable

1.6.2.1 Reliability issue

The remaining quality and life span of a battery after its first life can be dependent on a number of factors including, but not limited to; the battery chemistry, the number of cycles, the discharge current, the State of charge (SOC) or Depth of discharge (DOD) swing, and the cell temperature. There exists many publications looking at some or all of these variables for a range of chemistries under a variety of lab based conditions [301] – [307]. Typically the temperature is held to be constant either ambient 20°C or around 45°C – 50°C with either a constant charge-discharge regime to a set SOC or DOD or a constant drive cycle (to simulate vehicle behaviour). Battery chemistry and even the same chemistry from different manufacturers due to different manufacturing processes show differences in life cycle, failure modes and capacity fade. In addition to the other factors listed above, the failure rate of second life transportation batteries are also dependent on failure mechanisms related to how hard the batteries were driven inside the vehicle. At present most published data is based on VRLA or Li Ion chemistries. Previously published papers on battery lifecycle testing are largely split into the following categories;

- Small scale testing (small numbers of cells) under fixed conditions including typical drive cycles.
- Theoretical failure rates adjusted from experimental data, like that in 1, to take into account factors such as temperature and even proposed maintenance strategy which may be compared to either lab or field tests.

- Field testing experience.
- EV experience on a drive cycle.

A large proportion of the tests, especially on VRLA batteries, are also undertaken on behalf of the telecommunications industry and their use in backup supplies which traditionally float until needed and which is less relevant to the application presented in this thesis as most second life batteries are considered to be from vehicle applications. The previous work on life cycle testing was used to estimate the failure rate because it is difficult to get a fixed expression for battery failure rate, especially those that have completed a first life and are in a second life application. The remaining number of cycles was suggested to be one method to predict the battery life [308]. However, this is dependent on how batteries would be used in their second life application and the proposed DOD on each cycle.

A sample of previously published data is shown in Table 1-8 “?” marks where the data is not known and “(T)” and “(V)” indicate telecoms and vehicle applications respectively. The estimated lifespan for the purposes of this thesis is based on the “capacity at start - end of test column” in Table 1-8. The failure rate is based on the estimated life span extrapolated linearly to 0% capacity. It may not be always true but this linear extrapolation provides a good way of predicting the trend of unknown data. Therefore it is used in this thesis. Where lifespan is given in cycles as opposed to years, a nominal 200 cycles per year (from a typical EV application) is used to estimate failure rate. The range of failure rate values goes from 0.2 to 60×10^{-6} . Within this thesis, this range is used to investigate the effect of the variation of failure rate on second life battery energy storage system design.

Table 1-8 Range of inferred failure rates of batteries

Subset	Reference	Temperature	Battery	%DoD	Capacity at start -end of test	Estimated Lifespan	Estimated Failure rate/hr (inferred value)
1	[302]	20°C	VRLA	Varied (T)	Varied - 50%	2-9 years	1×10^{-5} to 6×10^{-5}
1	[301]	?	VRLA	?	New-50%	7 years to 50%	8×10^{-6}
1	[303]	20°C/40°C	VRLA	Varied	New-80%	30 to 100 years	2×10^{-7} to 7×10^{-7}
2	[304]	25°C to 40°C	VRLA	80% (V)	New-80%	200 cycles	2×10^{-5}
3	[305]	20°C	VRLA	Varied (T)	New -50%	(11 years)	1×10^{-5} to 50% fade

4	[306]	?	VRLA	? (T)	?	4-6 years	$2- 3 \times 10^{-5}$
4	[307]	?	VRLA	Varied (V)	New-80%	40,000 cycles	1×10^{-7}
4	[303]	20°C/40°C	VRLA	Varied	New-80%	4 to 36 years	1×10^{-6} to 1×10^{-5}
2	[308]	25°C - 40°C	LiIon	25% from 90% initial SOC	New to 90%	Aprox.100 000 cycles	2×10^{-7}
2	[309]	50°C and other	LiIon	(V)	New to 82%	5250 cycles	8×10^{-7}
2	[310]	43°C	LiIon	50%	New to EOL	1300 cycles	2×10^{-5}
2	[311]	25°C	LiIon	50% – 80%	New to EOL	3000 /500 cycles	4×10^{-5} to 7×10^{-6}
2	[312]	20°C	LiIon	30% - 80% (T)	New	3000-30,000 cycles	7×10^{-7} to 7×10^{-6}
2	[313]	25°C	LiIon	40% (V)	New to 80%	10,000 cycles	2×10^{-6}
2	[313]	45 – 55°C	LiIon	100%	New to 64%	800 cycles	2×10^{-5}
5	[308]	?	LiIon	20%-60%	New to 80%	1 year	2×10^{-5}

1.6.2.2 Difference in characteristics

Another important issues with SLBESS is the ability to deal with heterogeneous battery elements because there are three main considerations with second life batteries; 1. The electric vehicle battery chemistry is continually evolving and research is underway on many different types of battery chemistries. 2. The recycling chain has not been fully established for second life batteries and is unlikely to be mature until the uptake on new EV's and HEV's is in sufficient numbers to warrant the investment necessary [296]. 3. The condition of the batteries at the point of second life application, even if they are of the same type and from the same manufacturer, will be dependent on driver behavior and first life drive cycle. Moreover, different vehicles use different battery chemistries e.g. lead acid, nickel metal hydride (NiMH), lithium-ion etc. and these come in a range of sizes (both power and energy) depending on the application (e.g. EV, HEV, bus, motorbike). Therefore, batteries in second-use applications may have different chemistries, capacities, nominal voltages, internal impedances, state of health, charging/discharging limits and physical size.

To enable research and investment in this area and to maximize the remaining life of these batteries, it is necessary to combine the batteries into a single grid-tie converter where their different performance characteristics can be catered for while providing an uninterrupted grid

support and a hot swapping mechanism is available so that as a battery ends its second life, it can be replaced without affecting the overall system operation. This integration of either similar batteries with vastly different performance capability or a hybrid battery system with widely different characteristics and reliability is different to currently published work on battery energy storage systems which predominantly use homogeneous battery modules. The power electronics design both in terms of converter topology and control system of such an energy storage system is much more challenging compared to that of conventional BESS and as such many of the topologies in section 1.5.2 have been analysed for use in this application.

1.7 Research summary

This research aims to investigate, simulate, design and build a new generation of multi-functional second life battery energy storage systems (SLBESS) which could interface with a low (or medium) voltage distribution network to provide frequency and/or voltage support to the grid. There have been a couple of recent researches which report about the feasibility studies of second life batteries in grid support applications both in industry and in research papers [314] – [318], [294] which shows the advantages and some of the challenges of using these batteries on the grid system. However, the practicality of such a system as a grid-tie ESS has not yet been published or developed. This thesis studies the power electronic topology, control and their inherent design issues of SLBESS. And in particular focuses on the challenges of a hybrid energy storage system using different types of batteries integrating through a single grid-tie converter and their associated control considering the relative performances and parameter variation.

This thesis aims to address the shortfalls in current research which are delaying 2nd life battery energy storage system development contributing in the following areas to help integrating second life batteries to the grid.

- **Converter topology**

Power converter topology is an important aspect of designing this type of energy storage system because it can be used to overcome reliability and performance issues with such battery systems. Moreover, a converter topology greatly influences efficiency, reliability, dynamic response and fault-tolerance of such a hybrid energy storage system. This thesis presents a suitable multi-modular converter topology to integrate the second life hybrid batteries to the grid system through a cost-reliability analysis. Thereafter, this research looks at different multiple operational modes of the proposed converter and discusses which are suitable for integrating widely different batteries with a grid-tie inverter in a reliable manner.

- **Hybrid battery control strategy**

After getting these batteries from different vehicles, their past history will most likely be unknown. Information is available from initial strip down and preliminary testing or pre-characterization and includes; a) battery module type/chemistry, b) battery module remaining capacity, c) battery module nominal open circuit voltage d) battery module lumped internal

impedance e) possible state-of-health (SOH) and f) initial battery module SOC. Each module contains battery cells of similar chemistry and performance. However, there could be widely different such module present in SLBESS.

Thereafter, one of the design challenges is to develop a utilisation or a power sharing strategy of the hybrid batteries in grid connected system so that individual module are utilised in the best manner because these hybrid battery module will charge or discharge at different rates and have different levels of degradation. Therefore, the existing balancing and/or equalisation strategy published to-date for similar battery modules will not be applicable in this case where modules are significantly different. This thesis provides the theory for utilising the hybrid batteries within a grid-tie converter while providing uninterrupted grid support through a line side inverter.

- **Parameter estimation**

Parameter variation is quite common in second life applications. Capacity and internal impedance are the two most important parameters in a battery which can vary. This thesis also provides a method to estimate these parameters which helps to track the level of degradations or state-of-health (SOH) online during the converter operation.

- **Converter control structure**

The closed control of modular energy storage systems has been previously undertaken using a single type of battery or super-capacitors with equal nominal module voltages and capacities where set points are largely constant between modules or the differences are fairly minimal. This means each converter module operates at similar current and voltage levels. However, a mix of widely different modules could be present in the second life applications where such a strategy is not applicable. Therefore, this thesis introduces two new distributed control architectures to the proposed converter topology which enables control of individual modules according to their characteristics in a particular grid support application.

1.8 Thesis Structure

This thesis is structured as follows:

Chapter 2 discusses the converter topology selection. A range of multi-modular topologies are investigated which could be suitable in the present application and compared to find a suitable multi-modular converter topology. A reliability-cost optimisation approach has been followed with subsequent numerical analysis to identify the best converter topology for use in this application considering a wide range of second life battery failure rate. The proposed approach also provides a suggestion on redundancy, number of modules and number of series batteries per module.

Chapter 3 explores the different operational modes of the proposed converter topology. Three different operational modes have been described and are dependent on the set of available batteries in the second life application. Thereafter, the design of the individual modules and associated loss or efficiency calculation has been provided corresponding to

each operational mode. Simulation and experimental validations of two operation modes have been presented and the measured loss/efficiency has been compared with the calculation.

Chapter 4 proposes a distributed power sharing strategy based on a sample-by-sample weighting factor which adaptively distributes the total grid side power into the hybrid modules according to their characteristics to take into account differences in battery capacity, state-of-charge and chemistry. The detailed derivation of the weighting factor is provided. Thereafter, simulation and experimental studies have been presented to validate the proposed strategy.

Chapter 5 proposes two different distributed control structures which can independently utilise the modular dc-dc converter module according to the desired weighting and is also capable of bypassing the faulty battery module in a controlled manner. A distributed voltage based control structure is proposed which implements the distributed current sharing strategy for the hybrid batteries in boost mode of operation. The detailed controller design and dynamic response are presented to maintain the converter stability and to achieve a fast dynamic response. Secondly, a concept of distributed duty ratio is proposed in boost-buck mode which offers a wider operational envelope compared to the boost mode of operation. The suitability of the boost-buck mode is discussed over the boost mode of operation. A comparison between boost and boost-buck mode has been presented to suggest a suitable operational mode of the converter depending on the set of batteries. All the operational modes have been experimentally implemented to validate the proposed claims.

Chapter 6 investigates possible stability issues in the different modes of operation of the converter. It was found that the boost mode of operation suffers from a stability issue. This also limits the speed of response in the boost mode of operation. Therefore, two solutions have been proposed to mitigate this issue: a) adaptive PI controller based approach, b) a non-linear robust Lyapunov controller based approach. The comparison between the two approaches has been presented to suggest a suitable control mode of the converter in boost mode.

Chapter 7 provides the details of the hardware implementation. The detailed description of the laboratory built prototype and components are documented. The overall control architecture and implementation issues and interface with the digital controller have been described.

Chapter 8 describes the key conclusions of this thesis and also suggests possible future work in this area.

2 Power Converter Topology for SLBESS

2.1 Introduction

A converter topology can greatly influence the reliability, efficiency, size/weight and overall cost of an energy storage system. In a SLBESS application, batteries are expected to be lower in cost but have lower capacity, degraded performance, lower reliability and be heterogeneous in nature compared to conventional new batteries. Therefore, the selection of converter topology is an important step in designing such an energy storage system. This chapter addresses the challenges in selecting a topology for a second life battery energy storage system (SLBESS) through reliability analysis. Finally this chapter uses reliability analysis to determine a suitable converter topology to integrate second life batteries to the grid system while attempting to optimise the overall converter reliability/cost. Within industry FMEA (failure mode effect analysis) is sometimes used as an alternative to reliability calculations because it offers a more pragmatic approach. However, it does not allow for a numerical comparison and therefore makes it difficult to compare topologies.

2.2 Reliability issues of Second Life Batteries and the effect of converter topologies

Most battery storage schemes use new batteries where the reliability of individual batteries is considered to be high. The batteries can therefore be connected in series, even though this arrangement is not the most efficient in terms of system reliability. This research looks at using second-life batteries that have previously been utilised in electric or hybrid vehicles. The main problem with these batteries is poor reliability compared to new batteries as described in chapter 1. This reliability issue greatly influences the reliability of the overall converter. This section uses a reliability based analysis of the existing BESS topologies to help determine the best topology for a 2nd life application.

2.2.1 Reliability calculation background

Failure rate of electronic components is the key to reliability calculations of power electronic systems. It is essential to have the knowledge of failure rates of different components in order to predict the overall reliability. The MIL-HDBK217F handbook [319] lists the approximate basic failure rate λ_b of typical electronic components like capacitor, inductors, switches, diodes etc. and is freely available in an early version (1991). Although it has been upgraded the values in this version are considered accurate enough for this initial analysis. The failure rate of the second life battery cells is assumed to be in the range of $\lambda_{batt} = 0.2 - 60 \times 10^{-6}$ with 7.7×10^{-6} with considered a reasonable figure based on discussion presented in chapter – 1 and previous work [315]. The failure rate of the driver, controller and sensors have not been

included in the analysis as these are assumed to be the same in each case and are considered negligible compared to the reliability of the power circuitry.

The overall failure rate of a component λ_p can be found from the failure rate of that component using (2.1) where n is the number of π factors (numerical factors from the MIL-HDBK217F) for each device which are dependent on factors such type of device, operating environment (such as, temperature), power loss etc. The reliability of the component can be found using (2.2) over a specified time period and the mean time to failure (MTTF) is defined by (2.3). The reliability calculation has been performed using a method similar to that described in [319].

$$\lambda_p = \lambda_b (\prod_{i=1}^n \pi_i) \quad (2.1)$$

$$R(t) = e^{-\lambda_p t} \quad (2.2)$$

$$\text{MTTF} = \int_0^{\infty} R(t) = \lambda_p^{-1} \quad (2.3)$$

The reliability of any power electronic system comprising of a number of different power components can be expressed in (2.4) where n is the total number of components and the term R_j corresponds to the individual reliability of the components. In the case of a conventional BESS (single-stage/two-stage configuration), the reliability block diagram is shown in Fig. 2.1.

$$R_T = \prod_{j=1}^n R_j \quad (2.4)$$

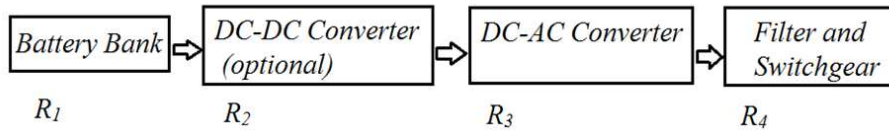


Fig. 2.1 Reliability diagram of a conventional BESS

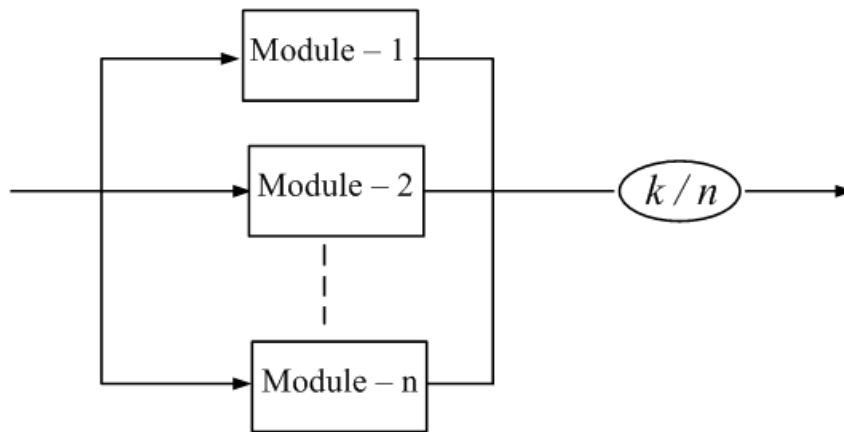


Fig. 2.2 Reliability diagram of modular BESS

The reliability diagram of a modular BESS is shown in Fig. 2.2. If there is ‘ n ’ number of modules in a system and out of that any ‘ k ’ modules have to in operation for successful operation of the system, then the system is said to have k -out-of- n redundancy. This method

greatly enhances the overall system reliability. The overall system reliability of such a structure can be calculated using equation (2.5) where R_m is the reliability of one module.

$$R(k, n) = \sum_{i=k}^n \binom{n}{i} R_m^i (1 - R_m)^{n-i} \quad \forall n \geq k \quad (2.5)$$

2.2.2 Component failure rates

The key components in a power electronic system is the power semiconductor switches (MOSFET, IGBT etc.), electrolytic capacitors, filters. The MIL-HDBK217F handbook [319] lists most of the components' failure rate expressions. Failure rate/reliability of the power semiconductor devices can be found from (2.6) where λ_b , π_T , π_A , π_Q and π_E are respectively the basic failure rates of a particular switch, temperature factor which depends on the junction temperature (T_j), application factor which depends on power rating of the device, quality factor and environmental factor. The basic failure rate λ_b also differs from one type of device to another, e.g. FET type to transistor type. It was reported in [320] that a transistor type device is more reliable than a FET type devices. Some of the new transistor types of devices such as, IGBT/IGCT etc which are widely used in the power electronic converter nowadays are not listed in MIL-HDBK217F. The failure rate of these devices was found to be much less than FET type devices by practical experience. For this reason, IGBT failure rate was assumed to be almost half that of a MOSFET ($\lambda_{IGBT} = 0.5\lambda_{MOSFET}$) as suggested by [320].

$$\lambda_{sw} = \lambda_b \pi_T \pi_A \pi_Q \pi_E \quad (2.6)$$

Among all the π factors in (2.6), the temperature factor π_T is a variable quantity for a particular type of switch and is dependent on the operating junction temperature. This junction temperature is also depends on the design of heatsink for a particular power device. The range of possible failure rate is given in Table 2-1 assuming a range of practical operating junction temperature (e.g. 80 – 120°C for MOSFETs and 80 – 100°C for IGBTs).

The electrolytic capacitors are often considered to be the weakest link in a power converter circuit because of their limited lifetime [321]. One way to predict the failure rate of the capacitor is to use manufacturer datasheets such as Cornell Dubilier [322] – [323]. The lifetime of electrolytic capacitors can be calculated from the manufacturer datasheet along with the Arrhenius equation as shown in (2.7) where L_b , M_v , T_m , T_a are the expected operating life for rated voltage and temperature (generally specified in datasheets, e.g 3000 – 5000hrs at 105°C), voltage multiplier for voltage derating, maximum operating temperature and actual temperature of operation respectively. The failure rate can be found from this lifespan as shown in (2.8).

$$L_{life} = L_b M_v 2^{\frac{T_m - T_a}{10}} \quad (2.7)$$

$$\lambda_{cap} = \frac{1}{L_{life}} \quad (2.8)$$

The numerical values of these failure rates depend mainly on operating condition and lifespan at maximum operating temperature. The dc-link capacitors are put very close to power switches and heat-sink in a practical converter. Therefore, the average temperature of operation remains higher than the ambient temperature. Assuming a range of operating temperature (40 – 50°C) for an ambient temperature of 20°C, the range of failure rates of electrolytic capacitor are calculated in Table 2-1.

Table 2-1 Range of failure rate and average failure rate of different components

Component	Range of Failure Rate (λ) $\times 10^{-6}$ hrs	Failure rate $\times 10^{-6}$ hrs (used in calculation)
Switch (λ_{sw}) – MOSFET	1.8 – 3.14	2.47
Switch (λ_{sw}) – IGBT	0.9 – 1.22	1.06
DC-link Electrolytic capacitor (λ_{cap})	2.8 – 5.5	4.15
Filter capacitance (AC capacitor) ($\lambda_{capacitance}$)	0.042	0.042
Filter Inductance ($\lambda_{inductance}$)	0.0004 – 0.0006	0.0005
dc-dc converter (λ_{DC-DC}) \rightarrow ($2\lambda_{sw} + \lambda_{cap} + \lambda_{inductance}$)	6.4 – 11.5 (MOSFET based) 4.6 – 7.94 (IGBT based)	9 (MOSFET) 6.27 (IGBT)
dc-ac converter (H-bridge) (λ_{DC-AC}) \rightarrow ($4\lambda_{sw} + \lambda_{cap} + \lambda_L$)	10 – 17.5 (MOSFET based) 6.4 – 10.38 (IGBT based)	14 (MOSFET based), 8.4 (IGBT)
Transformer (high frequency link) + two H-bridges $\rightarrow \lambda_{DAB}$	8.53	8.53
Second Life battery failure rate \rightarrow λ_{batt}	0.2 – 60	7.7

2.2.3 Reliability Estimation of Different Topologies

This sub-section performs an example reliability calculation of different BESS topologies for a transformerless 230V 1- ϕ grid connection over a period of 5 years and then a cost comparison at 10MW power level in order to meet 96% reliability. The battery cell voltage was taken as 3.3V and current rating is taken as 20A continuous. This power level and the desired reliability target have been taken as an example; the calculation is similar for any power levels and any reliability target.

2.2.3.1 Failure rate for Single-stage Configuration

The unit failure rate of the single-stage BESS (Fig. 1.12 in chapter – 1) is given by equation (2.9). In order to connect to 230V grid system without a line side transformer, there has to be

a minimum dc-bus voltage (around 350 – 400V). Therefore, around 120 series connected cells have been assumed to be in series to achieve this voltage level. It is clear from equation (2.9) that the series connection of the cells means that the overall system reliability (λ_T) is strongly influenced by the reliability of a single cell (λ_{batt}) and hence the total number of cells.

$$\lambda_T = (N\lambda_{batt}) + (\lambda_{DC/AC}) + (\lambda_{Filter}) \quad (2.9)$$

$$\lambda_{DC/AC} = 4\lambda_{switch} + \lambda_{cap} \quad (2.10)$$

$$\lambda_{Filter} = 2\lambda_{inductance} + \lambda_{capacitance} \quad (2.11)$$

2.2.3.2 Failure rate for Two-stage Configurations

This configuration (Fig. 1.13 in chapter – 1) has a similar format of total failure rate (λ_T) but includes the failure rate of a dc-dc converter as shown in (2.12). A lower number of series batteries is sufficient for transformerless grid connection in this case because the dc-dc converter can be used to boost the low battery bank voltage to the required dc-link voltage unlike single-stage configuration. However, it should be noted that the number of series connected batteries cannot be reduced indefinitely because of the need to boost the voltage to a sufficient value for inverting to the grid and very high boost ratio of the dc-dc converter could reduce the system efficiency to a very low value.

$$\lambda_T = (N\lambda_{batt}) + (\lambda_{DC/DC}) + (\lambda_{DC/AC}) + (\lambda_{Filter}) \quad (2.12)$$

The battery bank voltage is created by connecting 60 cells (3.3V each) in series to achieve a reasonable voltage (say around 200V) before using the dc-dc boost converter. The dc-dc converter boosts the 200V to 400V (boost ratio of 2) in order to form the main dc-link for the inverter. It is also possible to connect even a lower number of series batteries but that will need a higher boost ratio to achieve the desired voltage level. Therefore, the boost ratio of 2 has been considered as an example. The switching frequency of the dc-dc converter is assumed to be 10 kHz. Equation (2.13) and equation (2.14) gives the failure rate for the dc-dc and dc-ac converters. The same switches are used for the DC-AC and DC-DC converters as in the single stage topology.

$$\lambda_{DC/DC} = \lambda_{inductance} + 2\lambda_{switch} \quad (2.13)$$

$$\lambda_{DC/AC} = 4\lambda_{switch} + \lambda_{cap} \quad (2.14)$$

2.2.3.3 Failure rate for Three-stage Configuration

The failure rate of this topology (Fig. 1.14 in chapter – 1) is described by (2.15) where N is the number of cells connected in series; λ_{DAB} is the failure rate of the dual H-bridges and high frequency transformer.

$$\lambda_T = (N\lambda_{batt}) + (\lambda_{DAB}) + (\lambda_{DC/AC}) + (\lambda_{Filter}) \quad (2.15)$$

The battery side voltage is assumed to be the same as the two-stage configuration (60 cells in series) for a fair comparison with the two-stage configuration. As a result the high frequency link transformer will have a 1:2 turn ratio (similar to boost ratio of 2). Most of the components are the same as in two-stage BESS. Equation (2.16) gives failure rate for the dual active bridges (λ_{DAB}) and the expression of $\lambda_{DC/AC}$ is the same as (2.10) or (2.12).

$$\lambda_{DAB} = 4\lambda_{switch200V} + 4\lambda_{switch400V} + \lambda_{HFT} \quad (2.16)$$

2.2.3.4 Failure rate for a cascaded multilevel configuration

This topology (Fig. 1.17 in chapter – 1) can use a low number of series batteries and a high number of modules in cascade. This configuration can include redundancy (or extra modules) to increase reliability. Therefore, a large number of batteries may be needed. Equation (2.17) describes the unit failure rate of a single module. The number of cells (N) connected in series/module has been taken as 10 and 24 such modules has been considered (10x24 = 240 cells) for transformerless grid connection. Out of 24 modules 12 modules can be bypassed (=120 cells to meet the voltage), to create 12-out-of-24 redundancy. This number has been taken as an example to show the ability of this topology to go into bypass mode and will be considered in more detailed later in the chapter.

$$\lambda_{unit} = (N\lambda_{batt}) + (\lambda_{DC/AC}) \quad (2.17)$$

2.2.3.5 Failure rate for cascaded multilevel configuration with integrated dc-dc converters

This topology (Fig. 1.18 in chapter – 1) requires a lower number of modules compared to simple cascaded H-bridge converter to meet the ac grid voltage using individual module integrated dc-dc converters. Therefore, the total number of batteries per unit can be same as a two-stage or three-stage configurations. Equation (2.18) describes the module failure rate where ‘N’ is the number of cells connected in series/per module in Fig. 1.18. Total number of cells has been taken as N = 60 where 10 cells/module makes 6 overall modules. Out of that 3-out-of-6 module redundancy has been taken. Here also, this redundancy is just an example with more detailed described later in the chapter.

$$\lambda_{unit} = (N\lambda_{batt}) + (\lambda_{DC/DC}) + (\lambda_{DC/AC}) \quad (2.18)$$

2.2.3.6 Reliability comparison

Reliability calculation based on the example topologies has been presented in Table 2-2 using their corresponding failure rate (equations (2.9), (2.12), (2.15), (2.17) and (2.18)) expressions. It can be observed that a high number of series batteries is the limiting factor in achieving a good reliability especially when λ_{batt} is high (e.g. 7.7×10^{-6} or 60×10^{-6}). However, it is not a serious issue when λ_{batt} is low (0.2×10^{-6}). It can also be seen that the topologies with dc-dc

converters provide a better reliability figure when λ_{batt} is high because they can avoid a high number of series cells. The three-stage configuration always provides a lower reliability compared to the two-stage configuration due to the increased number of power electronic components. Moreover, the modular topologies enjoy much better reliability figure compared to the single-stage, two-stage or three-stage topologies for a given battery failure rate. The modular configuration can employ a higher level of redundancy (n/k) to achieve a good reliability even if the battery failure rate is high. It is interesting to note that the cascaded multilevel converter (CMC) topology is better than the CMC with integrated dc-dc converter based topology when the battery failure rate is low (0.2×10^{-6}). This is because the reliability of power electronic components (e.g. switches, capacitors) dominates over the battery failure rate (0.2×10^{-6}) at this range. On the other hand, the CMC with integrated dc-dc converter based topology provides a better reliability figure compared to the CMC topology when the battery failure rate is high. Therefore, in second life applications where the battery failure is expected to dominate over the power electronic components due to their limited lifespan, CMC with integrated dc-dc converter based topology provides the best reliability among common BESS topologies.

Table 2-2 Reliability comparison of different topologies for transformerless grid connection

Converter Topology	Total number of cells (N)	Redundancy	Reliability % after 5-years ($\lambda_{batt} = 0.2 \times 10^{-6}$)	Reliability % after 5-years ($\lambda_{batt} = 7.7 \times 10^{-6}$)
Single-stage	120	N/A	0.242 (Eq. 2.9 and 2.2)	1.83×10^{-16}
Two-stage	60	N/A	0.33 (Eq. 2.12 and 2.2)	9×10^{-8}
Three-stage	60	N/A	0.28 (Eq. 2.15 and 2.2)	7.76×10^{-8}
Conventional CMC	240	12-out-of-24	0.58 (Eq. 2.17 and 2.5)	2.55×10^{-13}
CMC with integrated DC-DC converter	60	3-out-of-6	0.45 (Eq. 2.18 and 2.5)	0.012

2.2.3.7 Overall reliability/cost comparison of existing BESS topologies

Due to the requirements to have different numbers of battery cells to support a particular voltage level and different levels of redundancy, the reliability of an individual unit (as calculated in Table 2-2) was calculated and then the total number of such units required (in parallel) to meet a particular power level (say 10MW) at a set reliability target (say 96% over 5 year time) was determined. From this figure the total number of batteries and switches to meet the overall target was compared. This allows the total cost of a full system to be estimated and compared fairly rather than basing conclusions on a single unit comparison. This is done in two steps;

Step – 1: Calculate how many units are required to produce unit power at 96% reliability.

Suppose, the reliability of a single unit is R_m (<0.96) and ‘y’ number of such units are required in parallel to get a reliability of 96%. Using equation (2.19) for 1-out-of-y structure, allows the required number of units required to give the reliability through equation (2.20).

$$R = 1 - (1 - R_m)^y \quad (2.19)$$

$$y = \frac{\ln(1-R)}{\ln(1-R_m)} \quad (2.20)$$

Step – 2: Determine the total number of units (m) necessary to meet the given power ‘P’ (e.g 10MW) is given in (2.21) where P_m is the unit power. The cost indicator of a particular converter topology is given by (2.22). It is to be noted that variation of ‘m’ is linear and variation of ‘y’ is nonlinear.

$$m = \frac{P}{P_m} \quad (2.21)$$

$$\text{Cost indicator} = m \times y \quad (2.22)$$

For an example, a high number of series batteries/module reduces module reliability (R_m) which in turn demands a high number of redundant modules (n) to meet a desired reliability target (according to (2.19)). On the other hand, a low number of series batteries/modules increases the module reliability but it reduces the module power (P_m) rating which then demands a high number of modules to meet overall power rating (according to (2.21)). Therefore, depending on the relative values of R_m and P_m , the total cost varies.

2.2.3.8 Sensitivity study

Fig. 2.3 shows a surface plot with a cost indicator represented as the log of the total number of switches needed in a system to produce 10MW/hr power for a given reliability and battery failure rate. Each of the surfaces refers to a different configuration. The battery failure rate and reliability target both have been varied between 2×10^{-6} /h to 7.7×10^{-6} /h (higher than switch failure rate) and 0.1 (low reliability target) to 0.9 (high reliability target) respectively. The single stage converter offers the least value for money because of the high number of series strings of batteries. The three stage converter is always slightly less reliable than the two stage converter because of the addition of the transformer and the extra switches for what is essentially the same battery configuration. Adding redundancy to the two stage converter helps with the reliability but is not as good as adding redundancy through the use of the dc-dc and CMC configuration. The CMC configuration is not as reliable at high battery failure rates due to the fact that it always requires a high number of modules (k) to meet the voltage levels. However, as the battery failure rate drops to become close to that of the switches the CMC converter becomes more attractive and the total reliability is more dependent on the power electronics configuration and therefore this gains against the CMC with dc-dc converter which has more switches/unit. As battery failure rate increases it is clear that the CMC with dc-dc converter is the most suitable topology among the existing BESS topologies

to use when the battery reliability is poor. The effect of increasing overall system reliability is to increase the number of units required.

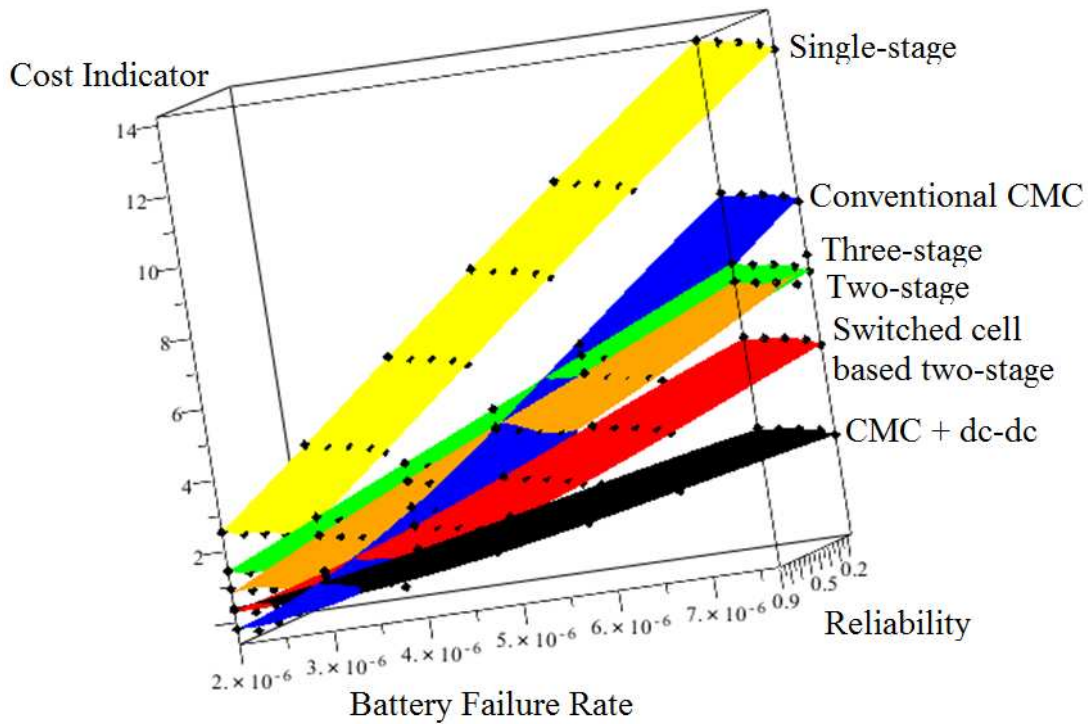


Fig. 2.3 Overall cost comparison of different topologies at 10MW power level meeting 96% reliability

2.3 Multi-modular Topologies

A multi-modular converter topology either with or without dc-dc converter offers the best value for money compared to a more conventional BESS especially when the battery failure rate is high. Moreover, it can also integrate heterogeneous sources in a single converter and also utilise each module independently. However, various types of modular configurations could be used. For these reason, this section investigates other types of modular topologies and performs a cost comparison based on their VA rating in order to meet a minimum reliability, voltage (for transformerless grid connection) and power, to find the optimum modular converter topology. This section also discusses the best values of x , k and n (where x = number of series cells/module, k = number of essential modules to meet voltage and power, n = total number of modules to meet the desired reliability target).

2.3.1 Different Multi-modular Topologies

Different multi-modular topologies are shown in Fig. 2.4. These topologies can be broadly divided into two categories: cascaded form and parallel form. Fig. 2.4(a) shows the conventional cascaded multilevel converter where each battery bank is directly connected to the main dc-link of a dc-ac module. Fig. 2.4 (b) shows a parallel structure where dc-ac modules are connected in parallel. Fig. 2.4 (c) shows the cascaded multilevel converter with integrated dc-dc converter while Fig. 2.4 (d) shows the parallel form of Fig. 2.4(c) where dc-ac modules are connected in parallel on the grid side. Fig. 2.4(e) and Fig. 2.4 (f) show dc-side

modular converters, cascaded and parallel form respectively where only a single dc-ac converter is used on the grid side.

All these topologies may have redundancy against battery failure. The battery failure could be a high impedance open circuit failure or a short circuit failure. In parallel topologies (Fig. 2.4b, Fig. 2.4d and Fig. 2.4f), the battery failure can be handled simply by shutting down the individual module converter but in cascaded topologies it cannot be performed in the same fashion due to the fact that a common current flows through all the modules which cannot be interrupted. Therefore, a bypass current path is necessary to handle the source failure for the cascaded topologies. For ac-side modular cascaded topologies such as, (Fig. 2.4a, Fig. 2.4c) this can be done by turning ON the two top switches or two bottom switches simultaneously in an H-bridge module (i.e. employing a zero switching state). However, it is not possible in the cascaded boost converter (Fig. 2.4e) because there is no such bypass path available in the entire converter module. This can be done by using two methods: a) bypassing only the faulty battery module by using bypass switches directly in parallel with battery module, b) bypassing the whole module integrated dc-dc converter. The later approach is followed in this work for multiple reasons: i) a converter bypassing technique can handle any malfunctioning of the associated converter's components which offers a more flexible protection, ii) it is a more efficient bypassing method because the current flows only through a bypass switch rather than through the whole converter as well as through the inductor as shown in shown in Fig. 2.5 and iii) switches of the same rating can be used in a module if the converter bypassing method is adopted (essentially an H-bridge structure, Fig. 2.5b) which simplifies the modular converter design rather than two different switch ratings are needed in the other method (Fig. 2.5a).

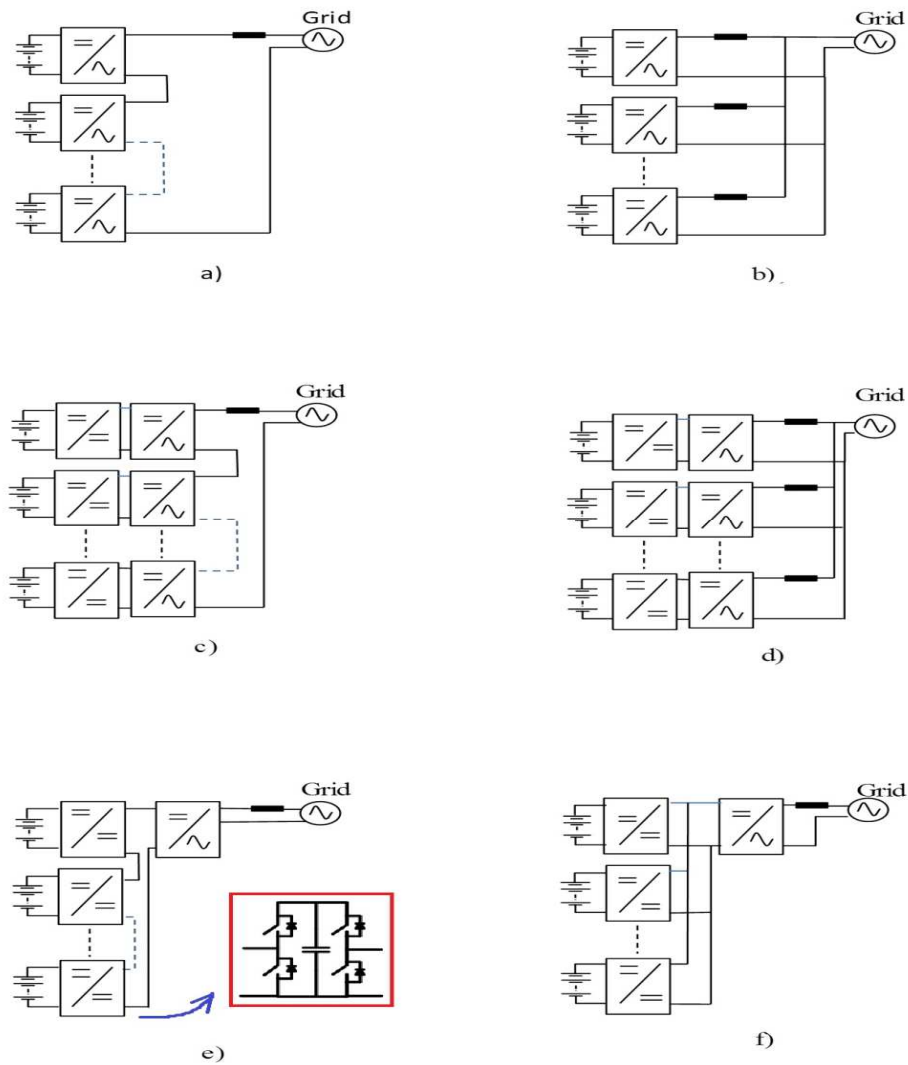
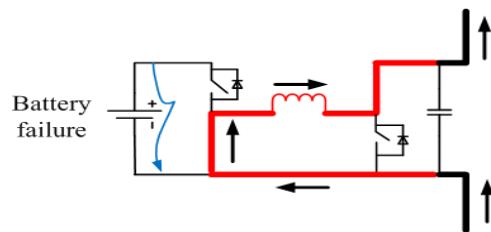
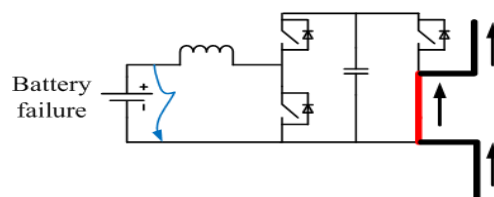


Fig. 2.4 Different possible multi-modular topologies for SLBESS : a) cascaded dc-ac, b) parallel dc-ac, c) cascaded dc-ac with integrated dc-dc, d) parallel dc-ac with integrated dc-dc, e) cascaded dc-dc with inverter, f) parallel dc-dc with inverter



a) battery bypassing



b) converter bypassing

Fig. 2.5 Ways to handle the battery failure: a) direct battery bypassing, b) bypassing through converter

2.3.2 Topology Optimisation

Previous work on reliability of power converters that includes the power source, is mostly based on wind power and PV applications, where the wind speed and inhomogeneous radiation (or partial shading) affect the failure rates of the power converter operation as described in references [320], [324]–[326]. Work that is more closely related to this application includes previous optimisation work on a parallel converter configuration [321] using converter failure, a fixed reliability target and optimising the overall system cost. However, this method is not directly applicable in this current context because of the interdependencies between a) the number of essential modules (k), b) number of series batteries/module (x), c) module power rating (P), c) voltage level and d) desired range of reliability (R^*). For example, the number of series batteries/module (x) directly affects module reliability (R_m). A high number of series batteries/module reduces module reliability which in turn demands very high number of redundant modules (n) to meet desired reliability target. On the other hand – a low number of series batteries/module increases the module reliability but it reduces module power rating which then demands very high number of modules to meet overall power rating. Apart from that, there is another challenge to meet the desired voltage for transformerless grid connection ($>$ line-line peak). Therefore, a careful selection of series batteries strings and converter redundancy is essential is necessary to meet a desired power, minimum voltage level and reliability all at a time.

As discussed earlier a general means of creating redundancy is to use a ‘k-out-of-n’ system, where any “ k ” modules must be operating to ensure the system power output is assured and ‘ n ’ number of modules is required to meet the desired reliability. In a ‘k-out-of-n’ reliability structure, there are four conditions which affect the overall reliability: a) topology b) total number of modules (n), c) number of essential modules (k), d) module reliability (R_m). The magnitude of R_m depends on the number of series batteries/module (x), the power electronic configuration and failure rate and the second life battery failure rate (λ_{batt}). The number of series connected batteries “ x ” is related to the “ k ” term to ensure a minimum power output and to “ n ” to ensure a minimum reliability. The failure rate of different battery cells could be different for different cells but for simplicity all the batteries are assumed to have the same failure rate.

The challenge is to select the best topology and its values of n , k and x to ensure an acceptable reliability target $R \geq R^*$ at a minimum power level (P) keeping cost to a minimum value. The power electronic system cost is considered to be proportional to the VA (volt-Amp) rating of the power electronic switches, energy stored in the components (such as, inductors/capacitors), associated gate drivers, sensors etc. The cost of the driver is usually neglected in high voltage/high power applications, because the cost of high voltage switches (such as, IGBT modules) is significantly higher than the drivers. However, this is not the case in low voltage applications where the commercial low voltage switches (such a LV MOSFETs) can be cheaper than some drivers (or driver IC) or at least comparable in value. Apart from driver IC’s, each gate driver requires isolation and protection especially in the modular converter (where a common ground reference cannot be used for all the modules)

which increases the cost. Therefore, the cost of a driver has also been included in this analysis. Additional system costs due to digital controllers etc. are considered to be common across the solutions for the purposes of this research.

The system cost f (cost) has been determined as a function of switch kVA rating ($f_1(kVA)$), inductor and capacitor energy rating ($f_3(Joule)$ and $f_4(Joule)$), driver cost as a function of switch voltage rating, ($f_2(VA)$) and sensor cost (f_5) (which can be constant) by plotting costs against size from the different component suppliers and deriving the line of best fit. The component suppliers RS (<http://uk.rs-online.com/web/>) and Farnell (<http://uk.farnell.com/>) have been chosen to identify different components. Fig. 2.6, for example, shows the costs of different components as a function of their rating and associated curve of best fits.

Therefore, the problem is to minimise the system cost and find values k , n , and x such that:

- Min $f(Cost)$, Subject to
- Minimum Reliability $R = \sum_{i=k}^n \binom{n}{i} R_m^i (1 - R_m)^{n-i} \geq R^*$ For $\forall k \leq n$
- Minimum voltage $V_T(k, x) \geq 340 (= 230 \times \sqrt{2} + \Delta\omega LI_s)$ \leftarrow Nominal 1- ϕ grid voltage (230V)
- Minimum power $P(k, x) \geq P^*$ (2.23)

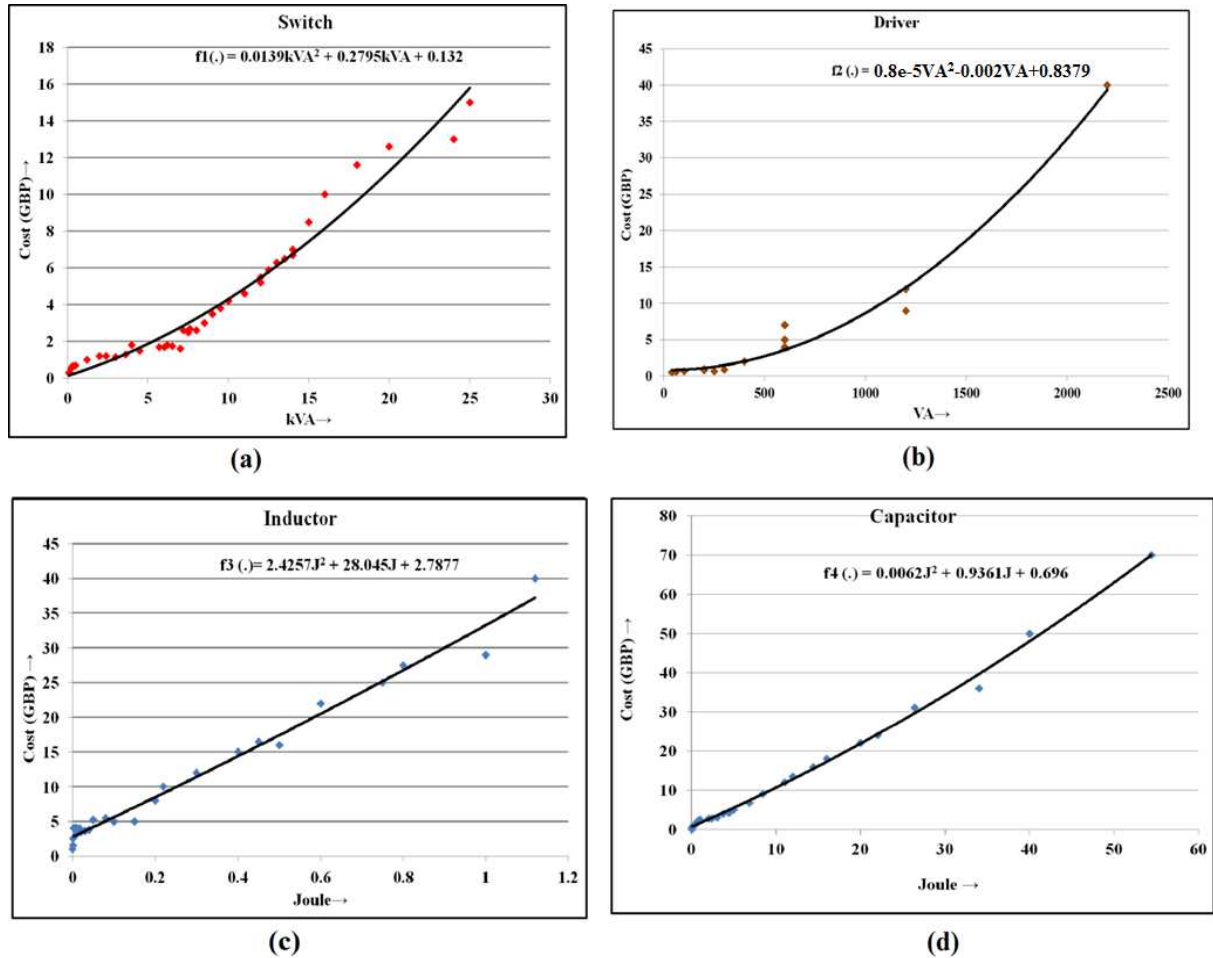


Fig. 2.6 Cost of components: a) power electronic switches, b) drivers, c) inductors, d) capacitors

Table 2-3 Reliability and voltage functions for different multi-modular topologies

Topology	Min Power Output (P)	Reliability (R)	Module reliability (R_m)	Min dc voltage condition (V_T)
Fig. 2.4a	$k_a x_a V_{cell} I_{batt}$	$\sum_{i=a}^{n_a} \binom{n_a}{i} R_{m,a}^i (1 - R_{m,a})^{n_a-i}$	$e^{-(x_a \lambda_{batt} + \lambda_{DC-AC})t}$	$x_{min,a} > \frac{340}{k_a V_{cell}}$
Fig. 2.4b	$k_b x_b V_{cell} I_{batt}$	$\sum_{i=k_b}^{n_b} \binom{n_b}{i} R_{m,b}^i (1 - R_{m,b})^{n_b-i}$	$e^{-(x_b \lambda_{batt} + \lambda_{DC-AC})t}$	$x_{min,b} > \frac{340}{V_{cell}}$
Fig. 2.4c	$k_c x_c V_{cell} I_{batt}$	$\sum_{i=k_c}^{n_c} \binom{n_c}{i} R_{m,c}^i (1 - R_{m,c})^{n_c-i}$	$e^{-(x_c \lambda_{batt} + \lambda_{DC-DC} + \lambda_{DC-AC})t}$	$x_{min,c} > \frac{340}{b_c k_c V_{cell}}$
Fig. 2.4d	$k_d x_d V_{cell} I_{batt}$	$\sum_{i=k_d}^{n_d} \binom{n_d}{i} R_{m,d}^i (1 - R_{m,d})^{n_d-i}$	$e^{-(x_d \lambda_{batt} + \lambda_{DC-DC} + \lambda_{DC-AC})t}$	$x_{min,d} > \frac{340}{b_d V_{cell}}$
Fig. 2.4e	$k_e x_e V_{cell} I_{batt}$	$\sum_{i=k_e}^{n_e} \binom{n_e}{i} R_{m,e}^i (1 - R_{m,e})^{n_e-i} + e^{-\lambda_{DC-AC}t}$	$e^{-(x_e \lambda_{batt} + \lambda_{DC-DC})t}$	$x_{min,e} > \frac{340}{b_e k_e V_{cell}}$
Fig. 2.4f	$k_f x_f V_{cell} I_{batt}$	$\sum_{i=k_f}^{n_f} \binom{n_f}{i} R_{m,f}^i (1 - R_{m,f})^{n_f-i} + e^{-\lambda_{DC-AC}t}$	$e^{-(x_f \lambda_{batt} + \lambda_{DC-DC})t}$	$x_{min,f} > \frac{340}{b_f V_{cell}}$

Table 2-4 Expression of cost indicators for different multi-modular topologies

	Approximate cost indicator (switch+ inductor/capacitor + drivers + sensors)
Fig. 2.4a	$4n_a f_1(x_a I_{batt} V_{cell}) + 4n_a f_2(x_a I_{batt} V_{cell}) + \frac{n_a}{2} f_3(C(x_a V_{cell})^2) + 2n_a f_5$
Fig. 2.4b	$4n_b f_1(x_b I_{batt} V_{cell}) + 4n_b f_2(x_b I_{batt} V_{cell}) + \frac{n_b}{2} f_3(C(x_b V_{cell})^2) + 3n_b f_5$
Fig. 2.4c	$2n_c f_1(x_c I_{batt} b_c V_{cell}) + 6n_c f_2(x_c I_{batt} V_{cell}) + 4n_c f_1\left(x_c \frac{I_{batt}}{b_c} b_c V_{cell}\right) + \frac{n_c}{2} f_4(L_{boost} I_{batt}^2) + \frac{n_c}{2} f_3(C(b_c x_c V_{cell})^2) + 3n_c f_5$
Fig. 2.4d	$2n_d f_1(x_d I_{batt} b_d V_{cell}) + 4n_d f_1\left(x_d \frac{I_{batt}}{b_d} b_d V_{cell}\right) + 6n_d f_2(x_d I_{batt} b_d V_{cell}) + \frac{n_d}{2} f_4(L_{boost} I_{batt}^2) + \frac{n_d}{2} f_3(C(b_d x_d V_{cell})^2) + 4n_d f_5$
Fig. 2.4e	$2n_e f_1(x_e I_{batt} b_e V_{cell}) + 2n_e f_1\left(x_e \frac{I_{batt}}{b_e} b_e V_{cell}\right) + f_1\left(4k_e x_e \frac{I_{batt}}{b_e} b_e V_{cell}\right) + (4n_e + 4)f_2(x_e I_{batt} V_{cell}) + \frac{n_e}{2} f_4(L_{boost} I_{batt}^2) + \frac{n_e}{2} f_3(C(x_e b_e V_{cell})^2) + 3n_e f_5$
Fig. 2.4f	$2n_f f_1(x_f I_{batt} b_f V_{cell}) + 2n_f f_1\left(x_f \frac{I_{batt}}{b_f} b_f V_{cell}\right) + f_1\left(4k_f x_f \frac{I_{batt}}{b_f} b_f V_{cell}\right) + (4n_f + 4)f_2(x_f I_{batt} V_{cell}) + \frac{n_f}{2} f_4(L_{boost} I_{batt}^2) + \frac{n_f}{2} f_3(C(x_f b_f V_{cell})^2) + 3n_f f_5$

The values of R_m , V_T and P are different for different topologies. The voltage and reliability function have been derived in the Table 2-3 and the cost function is presented in Table 2-4. Since there is no explicit mathematical solution for equation (2.23), a numerical solution has been found. The results are generated assuming a fixed battery type, a fixed cell voltage, and a constant boost ratio. However, with respect to second life battery context – all of this may not be necessarily the case, but it acts as a valid topology indicator for comparison purpose. Since the battery failure rate is uncertain, a range of failure rate has been used to show the effect of topology choice. The losses or efficiency of each converter type are not explicitly included in this optimisation routine and are considered separately in later chapter (chapter – 3). The following conditions are used in this example;

Minimum time period = 5 years

Cell description = 3.3V, 20Ah (minimum module size)

Minimum system reliability = 70%

Minimum power = 1kW

Boost ratio of all dc/dc converters (b) = 5

2.3.3 Numerical Analysis

The results are generated at different battery failure rates to see the effect of battery failure on the cost, total number of modules (n), level of redundancy (n/k) and number of series batteries/module (x). Two set of results have been generated: a) including power converter reliability, b) excluding power converter reliability to see how the power converter reliability and the battery reliability separately affects the overall cost, level of redundancy and topology choice.

The results using a very low battery failure rate (0.2×10^{-6}) have been presented in Table 2-5. The optimum point of the cascaded topologies (Fig. 2.4a, Fig. 2.4c, Fig. 2.4e) is at $x=1$ (or at minimum module size) for both the cases, including and excluding power converter reliability. This means the converter per minimum module size provides the lowest cost solution for this kind of topologies. One reason for this is a large number of cascaded/series connected modules with smaller boost ratio (here it is 5) or even with no boost ratio (Fig. 2.4a) can provide the minimum voltage for transformerless grid connection. On the other hand, the optimum point for parallel topologies (Fig. 2.4b, Fig. 2.4d, Fig. 2.4f) reaches at $x=21$ or $x=104$ because parallel topologies cannot meet the desired dc-bus voltage at a low number of series batteries/module. However, these values represent the lowest number of series connected cells to meet the voltage limit. This high number of series batteries/module reduces the module reliability (R_m). Due to this reason, the parallel topologies require high level of redundancy (high n/k) to meet the desired reliability. Among the parallel topologies, the dc-side modular converter (Fig. 2.4f) provides the lowest cost solution. It is also important to notice that all parallel topologies incur much higher cost compared to cascaded topologies even with a lower number of modules (n) because the cost largely depends on the product of n and x (as shown in Table 2-4) where the x is much higher for the parallel

topologies compared to the cascaded topologies. The cost is higher (both for cascaded and parallel topologies) when the power converter reliability is included in the analysis as expected. However, the trend in results is the same and the cascaded dc-side modular converter (Fig. 2.4e) provides the lowest cost solution among all the topologies.

Table 2-5 Optimisation result for different topologies – 1

Topology	Lowest cost solution for $\lambda_{batt} = 0.2 \times 10^{-6}$									
	Excluding power electronic components in reliability calculation					Including power electronic components in reliability calculation				
	x	k	n	n/k	Cost indicator	x	k	n	n/k	Cost indicator
Fig. 2.4a	1	104	110	1.05	1004	1	104	208	2	1825
Fig. 2.4b	104	1	3	3	1876	104	1	4	4	2571
Fig. 2.4c	1	21	22	1.04	433	1	21	63	3	1240
Fig. 2.4d	21	1	42	2	915	21	1	42	4	1373
Fig. 2.4e	1	21	22	1.04	390	1	21	42	2	1045
Fig. 2.4f	21	1	63	3	412	21	1	147	7	1431

The result using a higher battery failure rate (7.7×10^{-6}) has been presented in Table 2-6. It can be noticed from the table that the parallel topologies (Fig. 2.4b, Fig. 2.4d and Fig. 2.4f) cannot provide a feasible/practical solution at this battery failure rate because a high number of series batteries demands impractically high levels of redundancy (n/k) to meet a minimum reliability target which makes the cost function very high. The optimum point for cascaded topologies is still at $x=1$ (or at minimum module size) and here also, the cascaded dc-side modular converter provides the lowest cost solution. However, the cost and the level of redundancy (n/k) are higher than compared to when the battery failure rate is low.

A third result has been generated for when the battery failure rate is very high (60×10^{-6}). It was found that the optimum solution reached still at $x=1$ (or at minimum module size) for the cascaded topologies when the power converter reliability was not included but the overall cost and the level of redundancy (n/k) was found to be very impractically high. Moreover, no practical solution was found when the power converter reliability was included for any topologies because the module reliability became very low when using such high failure rate which needed impractically high level of redundancy ($n/k > 10$) compared to earlier cases. Therefore this would not be considered to be feasible in practical applications.

Table 2-6 Optimisation result for different topologies – 2

Topology	Lowest cost solution for $\lambda_{batt} = 7.7 \times 10^{-6}$									
	Excluding power electronic components in reliability calculation					Including power electronic components in reliability calculation				
	x	k	n	n/k	Cost indicator	x	k	n	n/k	Cost indicator
Fig. 2.4a	1	104	149	1.43	1360	1	104	312	3	2546
Fig. 2.4b	No practical solution (very high n , n/k and cost value)					No practical solution (very high n , n/k and cost value)				
Fig. 2.4c	1	21	31	1.47	611	1	21	84	4	1733
Fig. 2.4d	No practical solution (very high n , n/k and cost value)					No practical solution (very high n , n/k and cost value)				
Fig. 2.4e	1	21	31	1.47	554	1	21	63	3	1537
Fig. 2.4f	No practical solution (very high n , n/k and cost value)					No practical solution (very high n , n/k and cost value)				

The following conclusions can be drawn from the above analysis:

- If the battery reliability is low (e.g. $\lambda_{batt} = 60 \times 10^{-6}$) then it is impractical to use second life batteries within any application because of the cost of the power electronics needed to overcome the low system reliability.
- A series cascaded converter is a better option than a parallel connected converter because of the high series number of batteries needed to attain the voltage level in the parallel configuration and the impact of this on reliability.
- Configurations with a boost converter present offer a better option than without for the same reason (i.e. reducing the number of series batteries to attain the voltage levels).
- Topology Fig. 2.4e) offers the best cost value as it combines the cascaded configuration with a boost converter. This is even with the extra bypass switches present.
- If the power electronics is removed from the reliability calculation then the n/k ratio result for Fig. 2.4 (e) is equal to Fig. 2.4 (c) but the cost is lower because the VA rating of the large dc/ac converter is equal to k multiplied by the module VA rating as compared to n multiplied by the module VA for topology Fig. 2.4 (c) in Table 2-5.
- The choice of topology is independent of the battery failure rate and also the power electronics reliability within the fixed bounds of this example.
- Not visible by the results table – but also understandable is that having set x to the lowest possible value; k is also a minimum value in order to meet the voltage at minimum cost.

Due to similarities between the cascaded topologies, the results of the cascaded dc-side modular converter (Fig. 2.4e) have been plotted in 3D plane to better visualize the results obtained from the numerical analysis. For the same reason the results of the parallel dc-side converter (Fig. 2.4f) have also been presented. The result of the numerical analysis has been

plotted showing the variation cost against n/k against x using the equations given in Table 2-4. The ratio n/k is chosen because the cost is dependent on both n and k for the topology and it is not practical to plot in 4-D. Fig. 2.7 shows a set of numerical solutions of cost against ratio n/k against x for all those solutions for the cascaded dc-side modular topology (at $\lambda_{batt} = 0.2 \times 10^{-6}$) which meet a minimum reliability, power and overall dc bus voltage with and without power converter reliability. It can be seen from Fig. 2.7(a) that the solutions appear primarily as a series of lines of constant x starting at $x = 1$. The set of solution gradually moves upwards as x increases. This is because the cost increases as x increases. The result of Fig. 2.7b shows the set of solutions reduces (solutions become less dense on 3D plane) and the cost goes high when the power converter reliability is included as expected.

Another set of solutions is presented in Fig. 2.8 for the same topology at $\lambda_{batt} = 7.7 \times 10^{-6}$. It can be seen that the set of solutions reduces compared to at $\lambda_{batt} = 0.2 \times 10^{-6}$. Fig. 2.8b clearly depicts that the solution exists mainly at $x=1$. There is a reduction in the number of solutions when the power converter reliability is included. This is because the single dc-ac converter in this topology limits the overall reliability.

A similar trend can be observed from Fig. 2.9 where the solutions have been plotted for high battery failure rate $\lambda_{batt} = 60 \times 10^{-6}$. There are very few solutions found between $x = 1$ to $x = 4$ because a single module becomes very unreliable at this failure rate which demands impractical level of redundancy (very high n/k) to meet the desired reliability.

A different representation can be used in 2D plane to show separately the variation of cost against n/k with constant x , and cost against x with constant n/k when the power converter reliability is included at 0.2×10^{-6} . It can be seen from Fig. 2.10a and Fig. 2.10b that the cost is monotonically increases with n/k and with x when n/k increases as shown in the cost function in Table 2-4. Due to the need for integer numbers of x , n and k the solutions appear primarily as a series lines of constant x starting at $x = 1$ (Fig. 2.10b). These plots also show how the cost increases with n instead of having the constant lines n/k (Fig. 2.10a).

The results for the parallel topology (Fig. 2.4f) are shown in Fig. 2.11. The solutions at $\lambda_{batt} = 0.2 \times 10^{-6}$ is shown both with and without power converter reliability. The solutions for parallel topologies start to appear at a higher value of x ($=21$). The result is shown up to $x = 30$ because the costs function become excessively high when x increases because the reliability of the battery bank decreases. More dense solutions are found when power converter reliability is excluded but the difference is not as significant as compared cascaded topologies because the battery bank reliability dominates (due to higher number of series batteries/module) in parallel topologies.

Similar representation in the 2D plane for this kind of topologies is shown in Fig. 2.12a and Fig. 2.12b. A similar trend of variation of cost against n/k and cost against x is found compared to cascaded topologies. However, in the case of a parallel topology, the rate of variation of cost with n/k is higher compared to cascaded topology for a given x and vice-versa. This means, the cost is more influenced by n/k and x (refer to Table 2-3) This is understandable because the parallel topology uses higher rated power electronic components

(high voltage switches) in contrast to cascaded topology which uses low rated power electronic components.

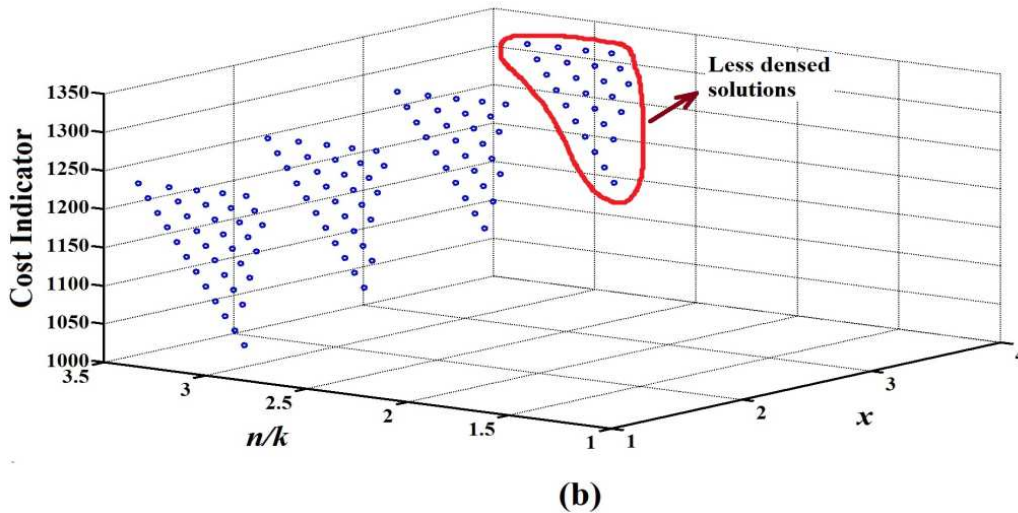
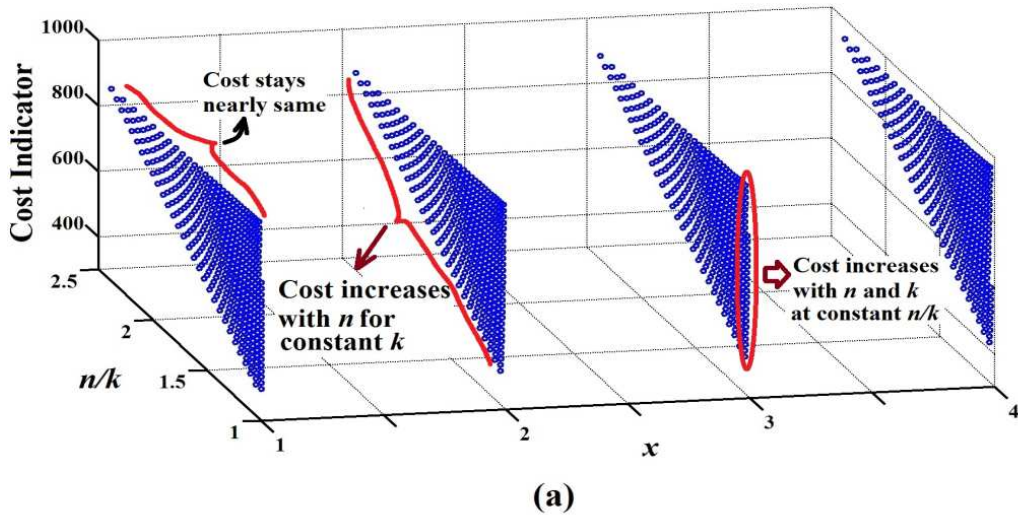


Fig. 2.7 Solutions for cascaded dc-side modular topology at $\lambda_{batt} = 0.2 \times 10^{-6}$: a) excluding power converter reliability, b) including power converter reliability

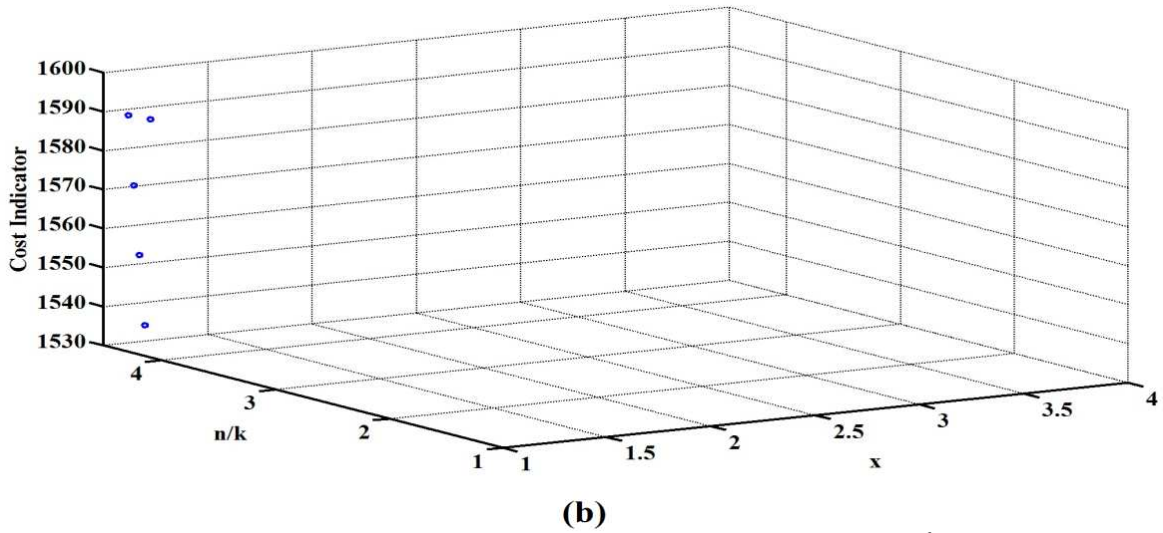
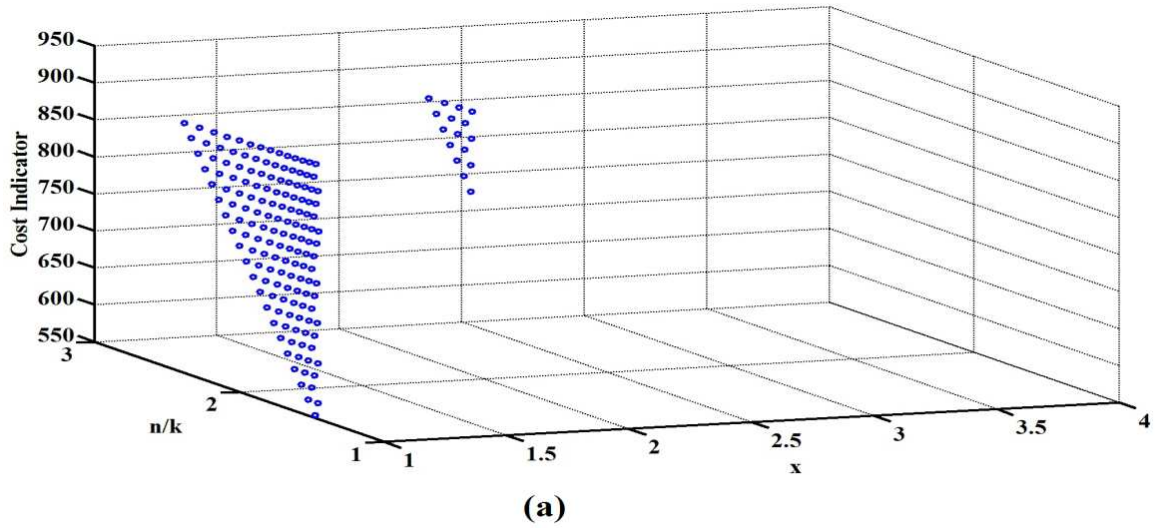


Fig. 2.8 Range of solutions for cascaded dc-side modular topology at $\lambda_{batt} = 7.7 \times 10^{-6}$: a) excluding power converter reliability, b) including power converter reliability

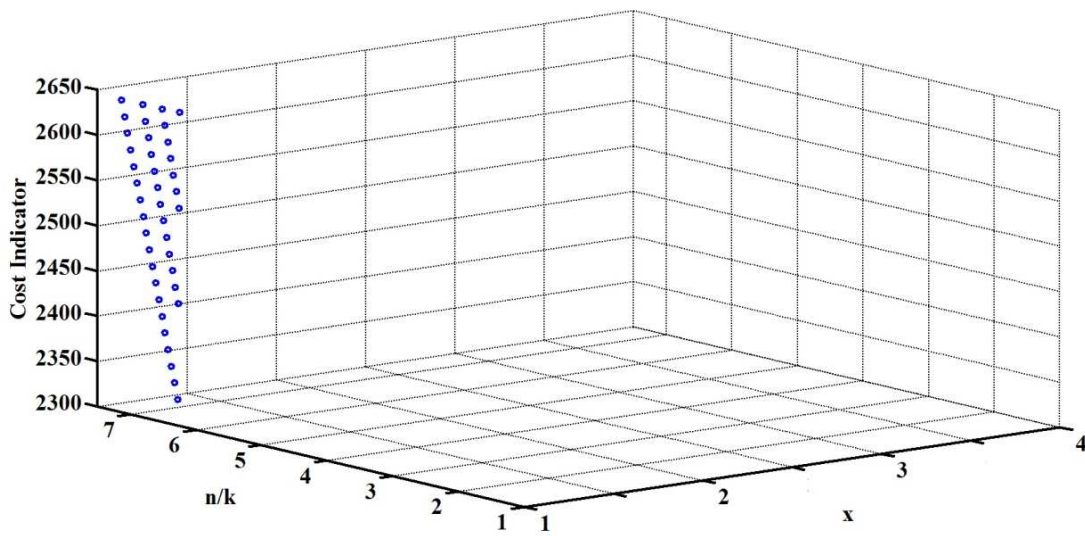


Fig. 2.9 Range of solutions for cascaded dc-side modular topology at $\lambda_{batt} = 60 \times 10^{-6}$: excluding power converter reliability

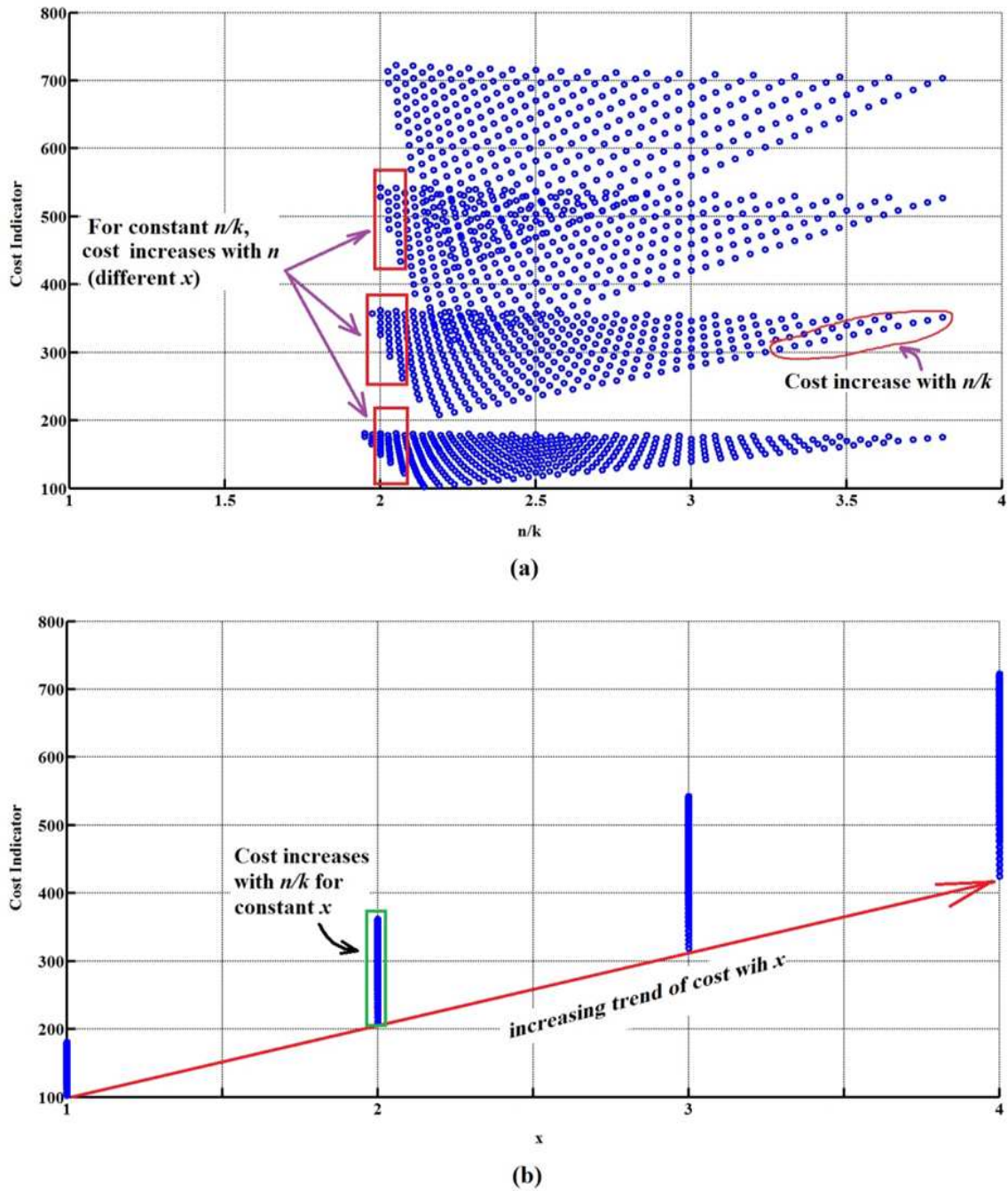


Fig. 2.10 2D-plot showing the variation of cost with n/k and x at $\lambda_{batt} = 0.2 \times 10^{-6}$ a) variation with n/k , b) variation with x

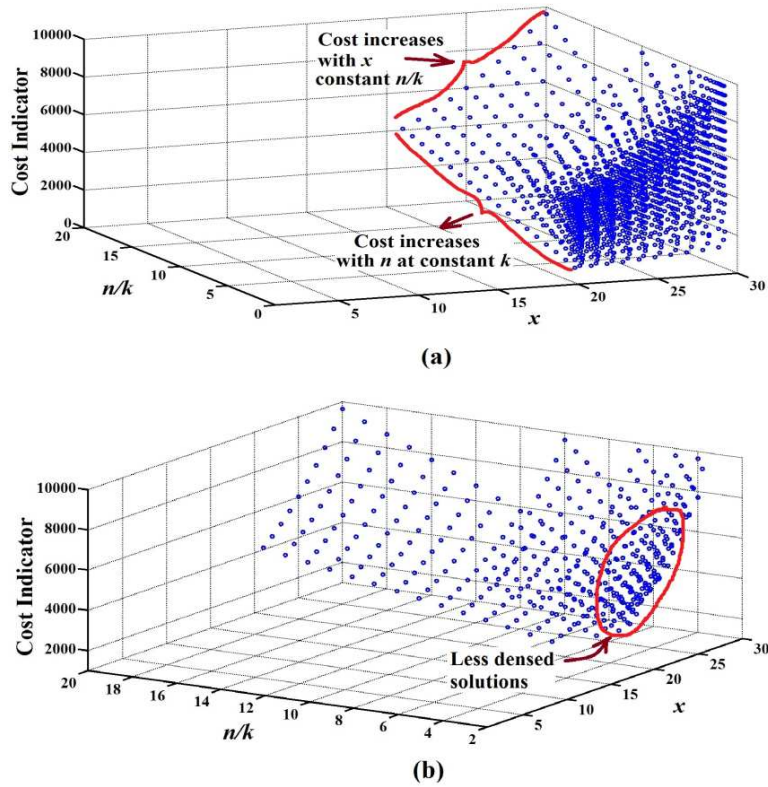


Fig. 2.11 Range of solutions for parallel dc-side modular topology at $\lambda_{batt} = 0.2 \times 10^{-6}$: a) excluding power converter reliability, b) including power converter reliability

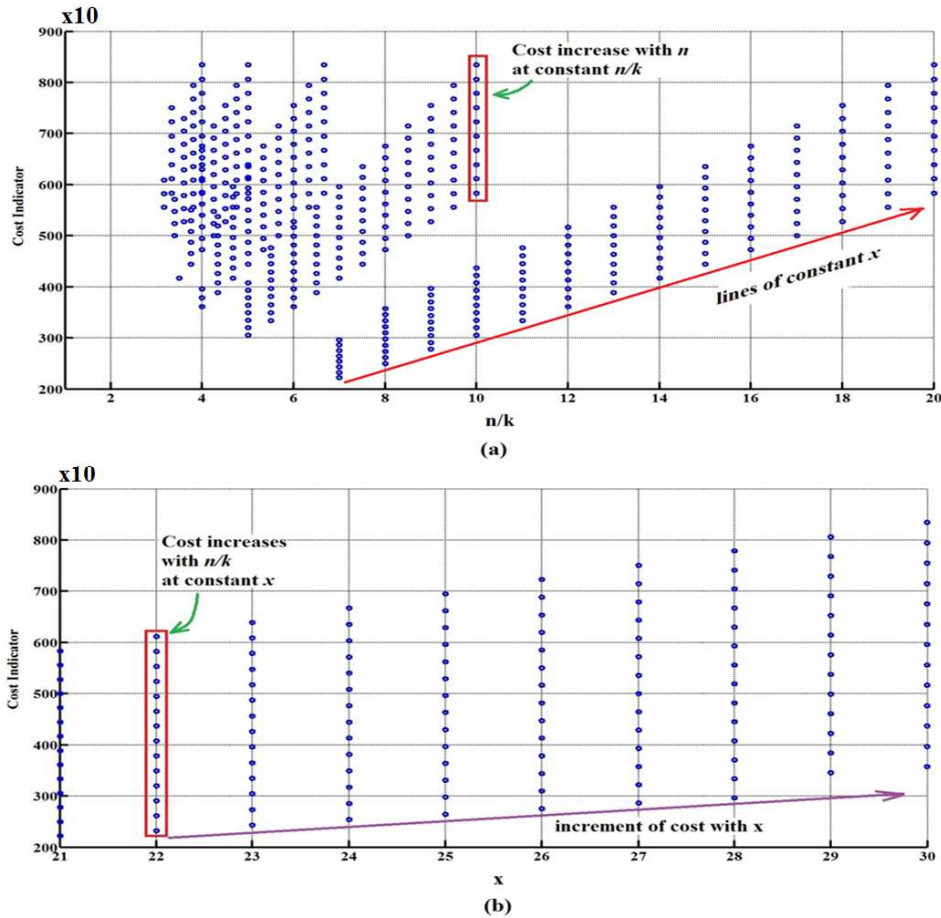


Fig. 2.12 2D-plot showing the variation of cost with n/k and x for parallel topology at $\lambda_{batt} = 0.2 \times 10^{-6}$ a) variation with n/k , b) variation with x

To validate the topology selection an FMEA (Failure Mode Effect Analysis) has been undertaken (in chapter 7) to prove that this design is also valid under alternative selection criterion and to assist with hardware protection.

2.3.4 Conclusion

This chapter provides an overview of different converter topologies for BESS analysing each topology for use in a second life application. From this analysis, a multi-modular converter is determined to be the best solution for this kind of application. An approach to find out the best choice of multi-modular topology and associated values for x , k and n at a lowest cost factor for transformerless grid connection at a minimum power and reliability was used. It concludes that minimizing x and k as far as possible is the best method to reduce overall cost and that a series configuration or cascaded converter is better than a parallel configuration. Among the cascaded converters, the fault-tolerant dc-side modular converter with a single inverter connected to the ac-side comes out as the optimum topology regardless of the battery reliability (within a feasible range) and power electronics reliability (since uncertainty in calculation is removed by considering the both with and without power electronic reliability). The optimum solution in terms of number of series batteries/module reaches at $x = 1$ or at minimum module size. However, it may not always possible to strip down a battery module to cell level or access of each cell and also, the converter efficiency could be low when a converter per cell approach is followed. Therefore, a practical design method may not always support converter per every cell approach but the system should be designed based on the lowest available battery module size as far as possible for second life applications.

3 Proposed Topology: Operational Modes

3.1 Introduction

In the second life context, a battery could come from any supplier and/or manufacturer. The module voltage range of these batteries could be in any range starting from as low as 1.8V, 3.3V, 12V, 24V to as high as 220V or 600V upwards. It is impractical to strip down a battery to cell level or there may not be access to the cell level. Therefore, it would be beneficial to integrate these hybrid/heterogeneous automotive batteries (which would be coming through the supply chain) with different reliability and performances through a single power electronic unit/converter irrespective of their voltage, characteristics or type to build a flexible hybrid SLBESS. This type of hybrid battery integration within a BESS has not been specifically considered, not even with new batteries because the majority of research reports using homogeneous batteries with equal module size, type and characteristics both in grid connected and grid independent mode [83] – [84], [327] – [329]. Therefore converter topology design for this type of hybrid battery integration has not received attention in previously published literatures.

According to the analysis presented in the last chapter, a cascaded dc-side modular converter is the optimum topology from a cost and reliability perspective. Therefore, all further analysis in this research uses this topology. To overcome the reliability problem, a bypass switch network is used with the existing cascaded dc-side modular converter to deal with the second life battery reliability aspect previously described and in the FMEA. However, apart from reliability related reasons, there are multiple challenges that the converter has to deal with especially in second life applications namely: a) to integrate unequal battery module voltages with different number of modules together to a common dc-bus with an inverter. This needs to handle two situations: i) when the sum of the battery side voltage is less than the desired dc-link voltage of the inverter ($\sum V_{batt,i} \leq V_{dc}^*$) and ii) when the sum of the battery side voltage is greater than the desired dc-link voltage of the inverter ($\sum V_{batt,i} > V_{dc}^*$) depending on the second life supply chain, b) to control hybrid modules independent according to their characteristics so that they are utilised optimally while providing the necessary grid support, c) to achieve good converter efficiency.

Depending on a set of batteries present the overall dc-side modular converter demands boost as well as buck capability to integrate to a single grid-tie converter. For this reason, it is necessary to investigate multiple operational modes which can cope with a hybrid battery configuration. This chapter explores the topology in more depth, namely: a) different modes operation especially in the context of second life application, b) the design of each module and c) power loss/efficiency.

3.2 Different modes of operation of the Converter

Cascaded dc-side modular converter considered in this work uses four active switches per

module to handle the reliability and protection issue as described in chapter 2. As a result, the topology looks like an H-bridge structure per module.

The first leg (S_i, S_{ii}) of each module acts a boost converter to form the dc-link voltages ($V_{dc,1}, V_{dc,2} \dots V_{dc,n}$), then the modules are cascaded through the fault-tolerant legs (T_i, T_{ii}) and thereafter, all the module are connected to the central dc-link of an inverter through an additional inductor as shown in Fig. 3.1. Primarily the control signals of T_i, T_{ii} are either 0 or 1. However, this fault-tolerant leg (T_i, T_{ii}) at the output of each module can be exploited to achieve additional operational flexibilities along with providing necessary bypassing of faulty battery modules. This H bridge combination along with the magnetics can be used to get a wide operational range. The details of the different operational modes are described below.

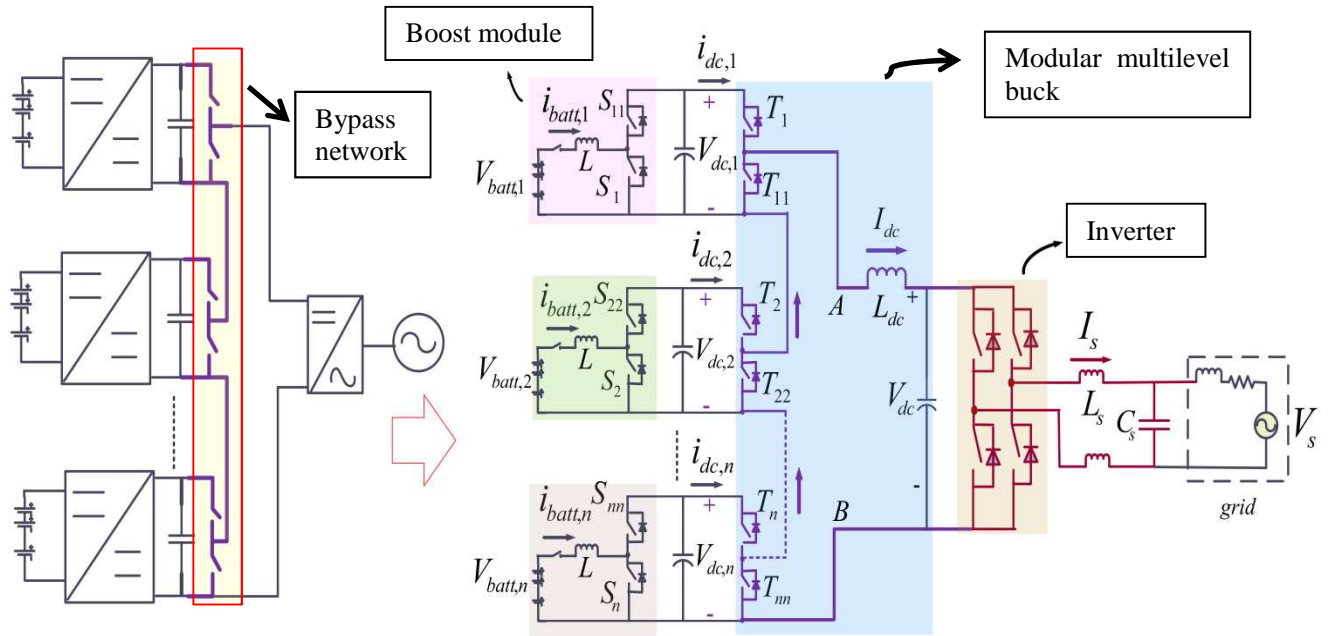


Fig. 3.1 Power circuit of the proposed topology

Mode – 1 (boost): The converter can be operated in boost mode when all the batteries meet the condition $\sum V_{batt,i} \leq V_{dc}^*$ by operating S_i and S_{ii} in PWM mode and keeping T_i, T_{ii} in idle mode (T_i is ON and T_{ii} is OFF). This mode of operation is shown in Fig. 3.2a. In this case, T_i, T_{ii} provides the bypassing to the battery modules. Under an abnormal condition, such as battery failure, the controller turns T_{ii} ON and T_i OFF, which in turn bypasses the i^{th} module. In this mode, a common dc-link current I_{dc} flows through all the modules. However, apart from the voltage constraint, a major limitation of this mode is, the $i_{batt,i}$ cannot be made lower than the dc-link current ($i_{batt,i} \geq I_{dc}$) which means an individual module cannot deliver the desired power when a mix of different modules are present such that the modules requires a current in one module lower than the dc-link current (I_{dc}). The operational range of this mode is shown in Fig. 3.3a.

Mode – 2 (buck): The converter can also be operated only in buck mode when all the batteries present operate under the condition $\sum V_{batt,i} \geq V_{dc}^*$. In this mode, S_i and S_{ii} are operated in idle mode (S_i is OFF and S_{ii} is ON) and switching T_i, T_{ii} in PWM mode along with the dc-link inductor L_{dc} as shown in Fig. 3.2b. In this case, a common dc-link current I_{dc}

can be decoupled from the module battery current using appropriate PWM patterns of T_i , T_{ii} . However, the limitations of this mode also such as, a) $i_{batt,i}$ is always less than the link current ($i_{batt,i} \leq I_{dc}$), b) the total battery side voltage has to be higher than the central dc-link voltage of the inverter. The operational range of this mode is shown in Fig. 3.3b.

Mode – 3 (boost-buck): There could be another mode of the converter which is boost-buck mode when both of the legs of a module, S_i and S_{ii} as well as T_i , T_{ii} are operated in PWM mode. This mode is more generalised because it is applicable for both of the conditions $\sum V_{batt,i} \geq V_{dc}^*$ or $\sum V_{batt,i} \leq V_{dc}^*$ due to boost and buck capability. The principle idea behind this mode of operation is to make the sum of the module dc-link voltages greater than the central dc-link voltage ($\sum V_{dc,i} \geq V_{dc}^*$) using the module integrated boost converters and then use the leg (T_i , T_{ii}) to buck it down to V_{dc}^* . Therefore, under $\sum V_{batt,i} \leq V_{dc}^*$ condition, all the module converters operate in a higher boost ratio and under $\sum V_{batt,i} \geq V_{dc}^*$ condition all the module converters operate in a lower boost ratio. The switching operation of S_i , S_{ii} and T_i , T_{ii} can be totally independent and because of this, each module current $i_{batt,i}$ can be either greater or lower than the link current ($i_{batt,i} \geq I_{dc}$ or $i_{batt,i} \leq I_{dc}$) as desired. This provides wide control flexibility especially when heterogeneous/hybrid battery modules are present which demand widely different module currents but it gives rise to the lowest efficiency of all the operational modes due to additional switching losses. The operational range of this mode is shown in Fig. 3.3c.

Mode – 4 (hybrid): In this mode of operation, some of the module integrated boost converters works in idle mode (S_j OFF and S_{jj} ON) and some of them (S_i , S_{ii}) work in PWM mode while all the T_i , T_{ii} work in PWM mode as shown in Fig. 3.2c. This mode is referred to as hybrid mode of operation where any wide range of battery module voltage can be integrated more effectively (such as 12V/24V module with 200V/400V module) However, in this mode of operation the sum of the module dc-link voltages must be higher than the desired dc-link voltage ($\sum V_{dc,i} \geq V_{dc}^*$).

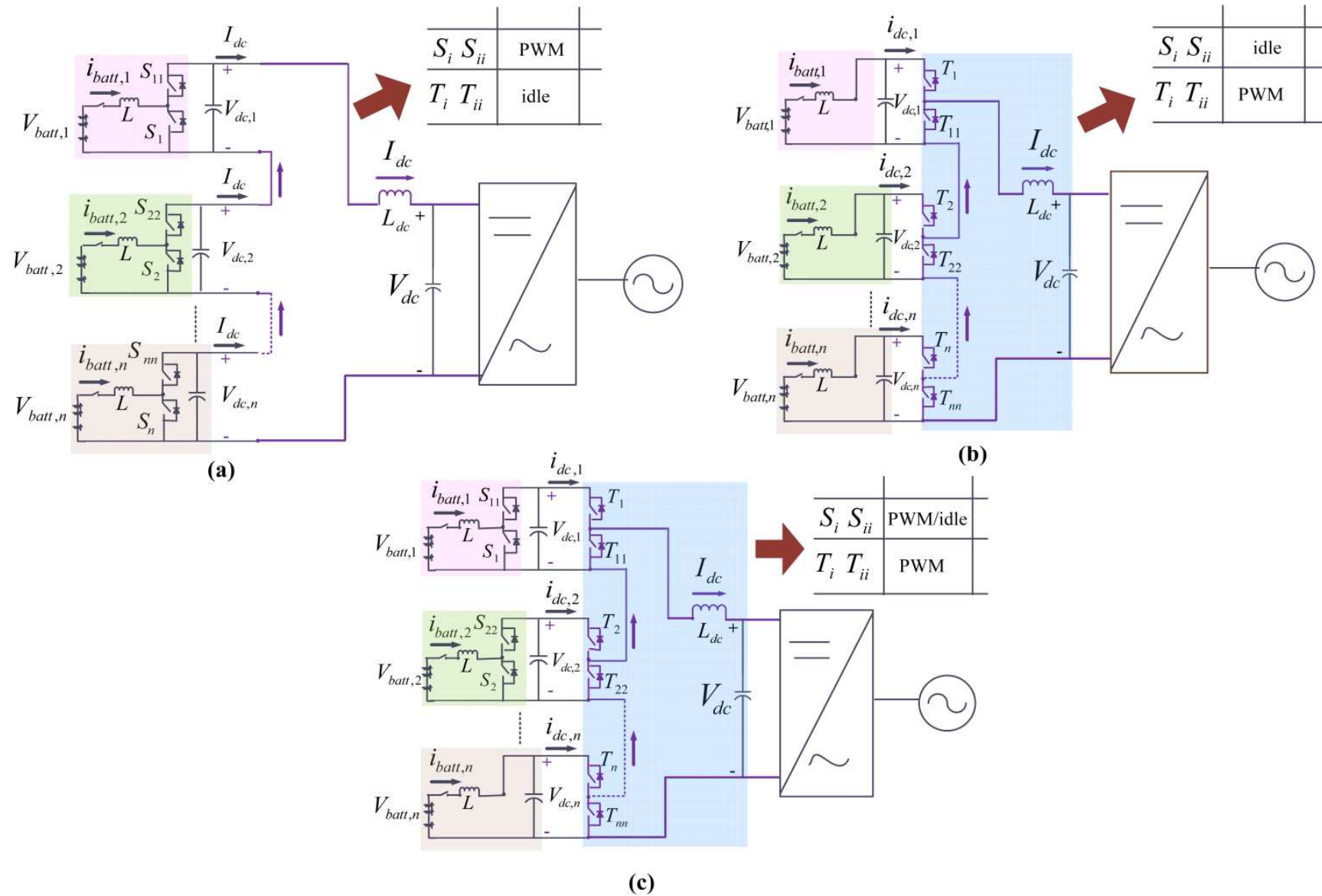


Fig. 3.2 Multiple modes of the proposed converter from the input to output: a) Cascaded boost mode, b) multilevel buck mode, c) Boost-multilevel buck mode

The functional block diagram of the overall converter can be re-presented in Fig. 3.4 which essentially shows multiple dc-dc converters connected through a combined multi-input dc-dc converter before integrating to the dc-link of an inverter.

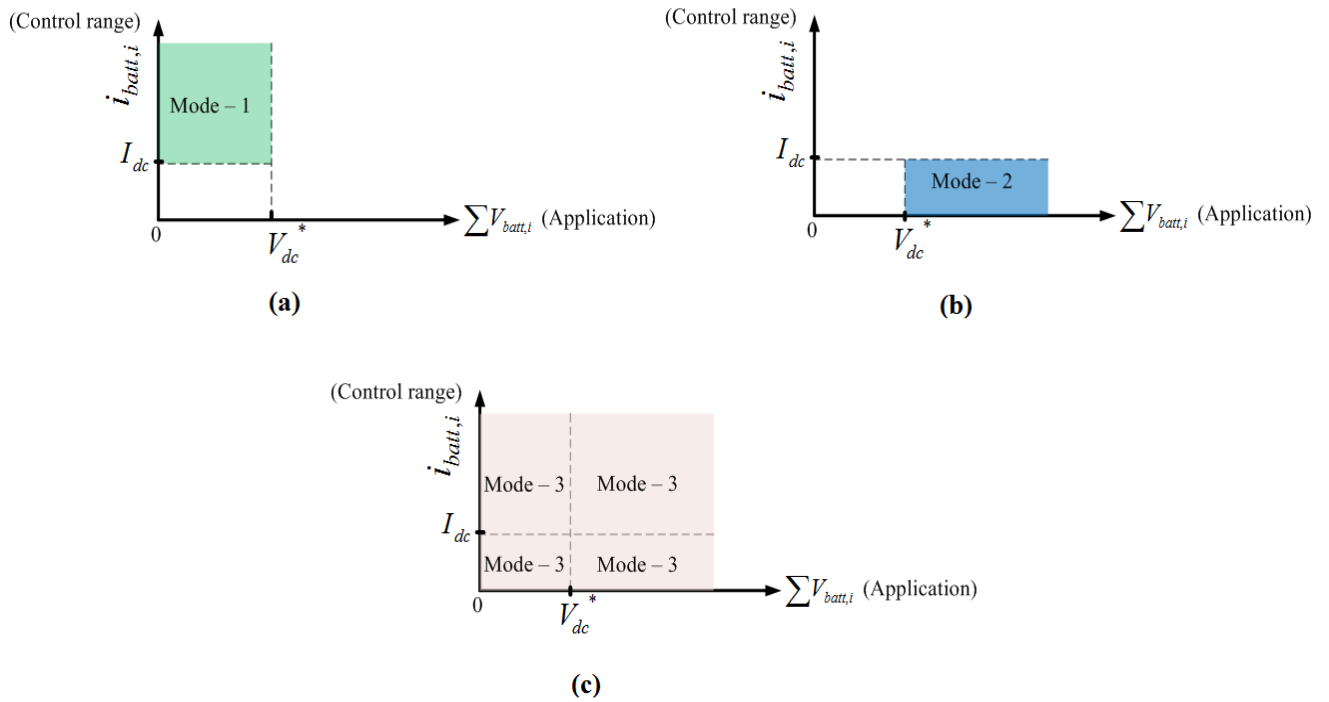


Fig. 3.3 Operational diagram for each mode: a) control range of boost mode, b) control range of buck mode, c) control range of boost-buck mode

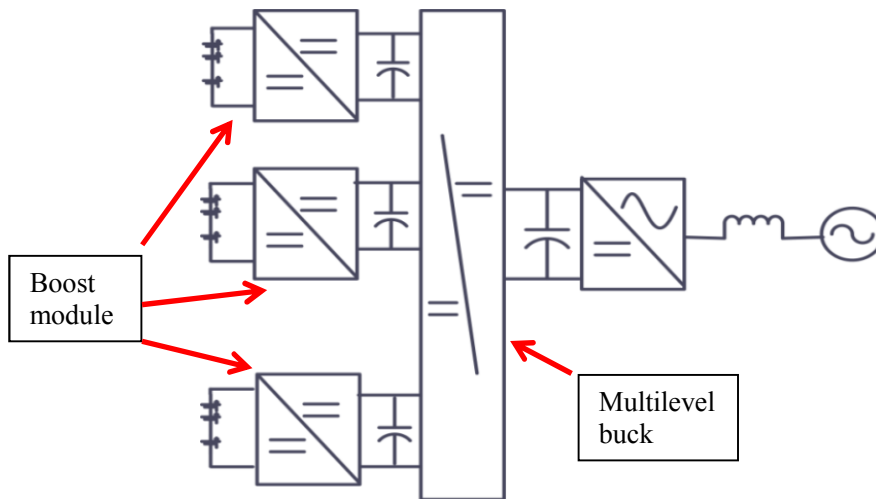


Fig. 3.4 Block diagram of the Proposed Configuration

3.3 Design of module inductor and capacitors

The design of each module inductor and capacitor within a set voltage and current operating envelope is important for several reasons: a) an improper design of module inductor and capacitor value may increase the size and cost of the converter, b) an improper design may also cause increased voltage and current ripple on the battery side which may degrade the battery lifespan and can cause EMI issues, c) the dynamic response and/or overall stability of the modular converter can be adversely affected by the improper selection of module inductor

value or capacitor value.

3.3.1 Design of module inductor

The design of module inductor (L) is challenging because of the potential for unequal module voltages and due to the fact that each module could be utilised independently accordingly to their module battery characteristics. As a result of this, current handled by different module could be different. There are two approaches: a) designing different module inductor according to individual module current and voltages, b) designing the same inductor for all the modules. The later approach has been followed in this work because: a) different inductors in different modules complicates the design of the modular converter because under the distributed utilisation, different modules may undergo same or different boost ratio at the same time depending on the control system operation, b) using the same inductor for all the modules increases the flexibility of the system which should allow batteries to be replaced in any module when bypassed which means by choosing a common inductor any batteries can be swapped in any module when a module fails which could be an advantage in this applications where any batteries could be available depending on the supply chain, c) using the different inductors the dynamic response/response time of the individual modules could be different which may cause significant voltage and current overshoot in some of the modules while responding to a sudden change in load (i.e. poor disturbance rejection capability). On the other hand, the dynamics response/response time and stability margin could be kept the same for all the modules when using the same magnetics in all the modules which ensures better converter stability and better dynamic response.

The design of the boost inductor for each module assumes CCM (continuous conduction modes) of the converter. The design is undertaken by choosing a maximum module voltage and current. The current ripple can be used to design the inductor. Therefore, the boost inductor in (3.1) corresponding to a maximum duty ratio condition is given 5% ripple (for example).

$$L = D_{max} \frac{\max(V_{batt,i})}{\Delta i_{batt,i}} T_s \quad \text{Where}$$

$$\Delta i_{batt,i} = 0.05 \times \max(i_{batt,i}) \quad (3.1)$$

The maximum allowable duty in a boost converter can be near unity but this is not practical to use such an extreme duty ratio in a dc-dc converter because the output voltage will be impractically high and can cause poor switch utilisations. The maximum allowable output voltage is limited by the maximum switch rating of a module. Therefore, the expression of L_{boost} can be modified to (3.2).

$$L = \left(1 - \frac{\max(V_{batt,i})}{V_{sw}}\right) \times \frac{\max(V_{batt,i})}{0.05 \times \max(i_{batt,i})} T_s \quad (3.2)$$

Now let us assume the case with unequal modules, 3.3V, 7.2V, 12V, 24V and 20A, 6.5A, 16A etc. module currents where maximum switch rating is say, 100V. The value of L_{boost} can be found as follows

$$L = 0.76 \frac{24V}{0.05 \times 20} 100\mu = 1.82 \text{ mH}$$

3.3.2 Design of module capacitor in boost mode

The design of the module capacitor is also undertaken assuming maximum module dc-link capacitors for all the modules. Since the module dc-link voltages could be different due to the fact that each module is to be utilised independently accordingly to their module battery characteristics. In boost mode (Fig. 3.2a), each module capacitor sees a constant load current I_{dc} across it as shown in Fig. 3.5(a). For single phase operation, there may be 100Hz ripple current on it but for the purpose of capacitor design this is neglected. The expression of the capacitor current is $i_{c,i} = i_{dc,i} - I_{dc}$. The maximum value of the capacitor current would be dependent on this constant load current and the peak of the module inductor current $I_{batt,i}$ which means $i_{c,i}|_{max} = \left(I_{batt,i} + \frac{\Delta i_{batt,i}}{2}\right) - I_{dc}$ as shown in Fig. 3.5(b). Therefore, the capacitor design consideration has to take care of this magnitude. This type of current generates voltage ripple across the capacitor. Therefore, the design of the capacitor should correspond to the maximum allowable ripple on the module (set to 1% of dc-bus voltage). This magnitude of ripple is taken just an example to ensure a stable dc-link voltage. The design of module capacitor is as follows:

$$C = D_{max} \frac{I_{dc}}{\Delta V} T_s \quad \text{Where } \Delta V = 0.01 \times \max(V_{dc,i}) \quad (3.3)$$

Let's assume unequal module input voltages 3.3V, 7.2V, 12V, 24V with dc-link voltages 20V,40V, 60V, 80V with a maximum switch voltage 100V and $I_{dc} = 10A$. The value of C can be found as follows:

$$C = 0.76 \frac{10}{0.8} 100\mu = 950\mu F$$

3.3.3 Design of module capacitor in buck/boost-buck mode

In boost-buck mode (Fig. 3.2c) or in buck mode (Fig. 3.2b), the capacitor design could be different because the magnitude of the capacitor ripple current is different. In that case, the switches T_i, T_{ii} in Fig. 3.1 work in PWM mode. As a result of this, an approximate nature of the load current across each module capacitor will be a pulse type constant load current as shown in Fig. 3.5(c). It is difficult to predict an exact behaviour of capacitor current in this case because it is very much dependent on the duty ratio of T_i, T_{ii} . Therefore, the module load current is approximated to its average value $D_{ii} I_{dc}$ for predicting the behaviour of capacitor current as shown in Fig. 3.5(d). This is a reasonable assumption because the switching ripple on I_{dc} will be small due to multilevel operation. The approximate expression of the capacitor current would be $i_{c,i} = i_{dc,i} - D_{ii} I_{dc}$ as shown in Fig. 3.5(b). The maximum value of $i_{c,i}$ would be $i_{c,i}|_{max} = i_{dc,i}|_{max}$, or $\left(I_{batt,i} + \frac{\Delta i_{batt,i}}{2}\right)$ because the minimum D_{ii} can be zero. This means that the peak of the capacitor current increases in buck or boost-buck mode compared to the boost mode of operation for the same module current $I_{batt,i}$. This peak of the capacitor current influences the lifespan of a capacitor because a high ripple current causes

high I^2R losses which increases internal heating and thereby reducing the lifespan of the capacitor.

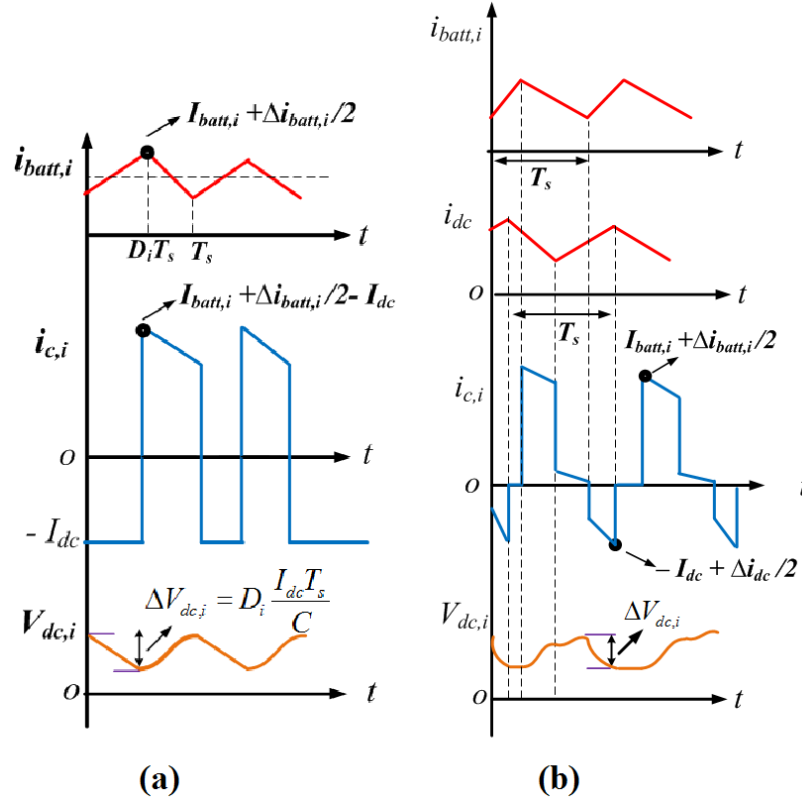


Fig. 3.5 Nature of load current in module capacitor design: a) boost-mode, b) boost-buck mode

The design of module capacitor is as follows:

$$C = D_{max} \frac{D_{ii} I_{dc}}{\Delta V} T_s \quad \text{Where } \Delta V = 0.01 \times \max(V_{dc,i}) \quad (3.3)$$

Let's assume unequal module input voltages 3.3V, 7.2V, 12V, 24V with dc-link voltages 20V, 40V, 60V, 80V with a maximum switch voltage 100V, $I_{dc} = 10A$ and $D_{ii} = 0.5$ (for an example). The value of C can be found as follows:

$$C = 0.76 \frac{5}{0.8} 100\mu = 475\mu F$$

The magnitude of the capacitor could be less in buck/boost-buck mode if D_{ii} is less than unity. Therefore, it can be concluded from this design and analysis that the boost mode of the converter (Fig. 3.2a) requires high capacitor value but peak current in the capacitor is low and on the other hand, buck/boost-buck mode (Fig. 3.2b/ Fig. 3.2c), requires less capacitor value but the peak current in the capacitor is high which may reduce the reliability of the capacitor.

3.3.4 Capacitor ripple current and life expectancy

The most commonly used capacitor in the power converter is electrolytic type because of its higher energy density and lower cost compared to other type of capacitors such as, Film capacitors. However, the reliability of this type of capacitor becomes an important issue. The

life of an electrolytic capacitor was expressed using (2.7) in chapter – 2. However, that expression did not take the ripple current of the capacitor into account. The temperature rise in the surface of a capacitor can be expressed in (3.4) due to ripple current [330].

$$\Delta T_c = \frac{I^2 R}{\beta \times S} \quad (3.4)$$

Where T_c = Heat rise in the case ($^{\circ}\text{C}$), β = Heat radiation factor ($\text{W}/^{\circ}\text{C}.\text{cm}^2$) and S = Surface area of the capacitor (cm^2), I = Ripple current applied (A) and R = ESR of the capacitor (Ω). Therefore, it can be seen that temperature rise is proportional to the $I^2 R$ loss of the capacitor. The explicit expression of the lifespan considering the ripple current can be expressed as (3.5) [330]. The factor $\left(2^{\frac{\Delta T_s - \Delta T_c}{10}}\right)$ in (3.5) is due to the ripple current of the capacitor.

$$L_{life} = L_b M_v 2^{\frac{T_m - T_a}{10}} \times \left(2^{\frac{\Delta T_s - \Delta T_c}{10}}\right) \quad (3.5)$$

Where L_b , M_v , T_m , T_a , ΔT_s and ΔT_c are the expected operating life for rated voltage and temperature (generally specified in datasheets, e.g 3000 – 5000hrs at 105°C), voltage multiplier for voltage derating, maximum operating temperature, actual temperature of operation, heat rise at rated temperature and actual heat rise respectively. Therefore, it is clear from (3.5) that the ripple current magnitude greatly influences the lifespan of a capacitor. In the present context, the boost and boost-buck/buck mode have different ripple currents which clearly implies different $I^2 R$ losses in the capacitor and consequently different capacitor lifespan as shown in (3.6) and (3.7) for the same operating conditions.

$$\frac{L_{life|boost}}{L_{life|boost-buck}} = \frac{2^{\frac{\Delta T_c|boost-buck}{10}}}{2^{\frac{\Delta T_c|boost}{10}}} \quad (3.6)$$

$$\frac{L_{life|boost}}{L_{life|boost-buck}} = \frac{2^{\frac{I^2 R|boost-buck}{10}}}{2^{\frac{I^2 R|boost}{10}}} \quad (3.7)$$

3.4 Power loss/efficiency

Power loss or efficiency is an important criterion in the design and operation of a practical converter. The proposed converter has multiple operational modes where different control modes use different switching combinations of S_i , S_{ii} , T_i and T_{ii} which give rise to different losses in the modular dc-dc converter. Therefore, an analysis of power loss/efficiency is useful because the overall power loss of the configuration is the sum of dc-dc converter and dc-ac converter. However, the inverter power loss or efficiency remains the same for all the three control modes because the inverter operates with the same dc-bus voltage for all the operational modes. Therefore, only the dc-side efficiency or power losses have been compared.

In addition on the number of series batteries/module or module input voltage also affects the efficiency. For an example, very low battery module voltage demands very high number of modules to meet a desired voltage and power levels or in other words, very low input

voltage requires a higher converter boost ratio to meet a desired dc-bus voltage which reduces the efficiency. Therefore, in this section the power loss or efficiency of the main three operational modes of the converter have been calculated for different numbers of series batteries/module or different module voltages. Equal module size in terms of voltage and current has to be assumed for the purpose of calculating the power loss/efficiency when using different number of series batteries/module. Finally, the power loss and efficiency has been calculated by considering a hybrid mix of modules (a more practical scenario in hybrid SLBESS).

3.4.1 Theoretical calculation of Mode – 1 (boost Mode)

An expression of the power losses in mode – 1 is shown in (3.7). The power losses in this mode comprises of: a) losses in module boost inductor, b) conduction and switching losses of S_i and S_{ii} , c) conduction losses in T_i or T_{ii} , d) losses in the dc-link inductance (L_{dc}). It is assumed all the switches in the H-bridge are identical and have the same turn on and turn off times.

$$P_{L1} = \left(\sum_{i=1}^N i_{batt,i}^2\right)R_L + \left(\sum_{i=1}^N i_{batt,i}^2\right)R_{ds(on)} + \left(\sum_{i=1}^N V_{dc,i}i_{batt,i}\right)\left(\frac{T_{on}+T_{off}}{T_s}\right) + NI_{dc}^2R_{ds(on)} + I_{dc}^2R_{dc} \quad (3.7)$$

The proposed converter can make use of low voltage semiconductors which have low on-state resistance and low switching time. The on-state resistance of commercial MOSFETs gradually reduces with the blocking voltage as shown in Fig. 3.6. Apart from using low voltage semi-conductor devices (LV MOSFETs) such a configuration can use a low boost inductance due to the low input voltage. An example calculation of boost inductor has been presented in Table 3-1. The calculation of power loss for a range of fixed battery voltages/module is shown in Table 3-2 using Table 3-1 assuming that each cell voltage is 3V.

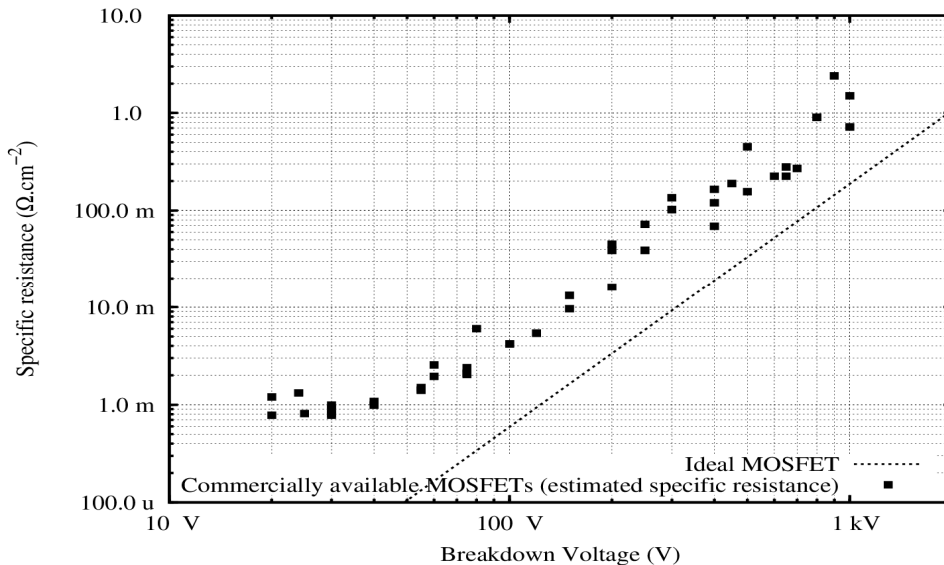


Fig. 3.6 Approximate variation of on-state resistance of commercially available MOSEFTs with their voltage rating [331]

Table 3-1 Boost inductor values with a considered range of input voltages

Module input voltage (assuming equal modules)	Module Current	Number of modules to meet 1kW power level	Inductor values (calculated from (3.2))
3V (1-cell)	19.6A	17	$\approx 0.3\text{mH}$ ($R_L = 4\text{m}\Omega$)
6V (2-cells)	18.5A	9	$\approx 0.6\text{mH}$ ($R_L = 8\text{m}\Omega$)
12V (4-cells)	16.66A	5	$\approx 1.2\text{mH}$ ($R_L = 16\text{m}\Omega$)
24V (8-cells)	13.88A	3	$\approx 2.8\text{mH}$ ($R_L = 20\text{m}\Omega$)

Table 3-2 Efficiency/power loss calculation in boost mode (equal module) at 1kW power level

module input voltage (assuming equal modules)	Module Current	Module dc-link voltage ($V_{dc,i}$)	Number of modules to meet 1kW power level	Boost inductor	Active Switch (Approximately lowest available on-resistance MOSFET)	dc-link current (I_{dc})	Efficiency
3V (1-cell)	19.6A	23.5V (= 400/17)	17	0.3mH ($R_L = 4\text{m}\Omega$)	SIS410DN ($R_{ds} = 4\text{m}\Omega$), $T_{on} + T_{off} = 85\text{ns}$	2.5A	$\approx 94.0\%$
6V (2-cells)	18.5A	44.44V (= 400/9)	9	0.6mH ($R_L = 8\text{m}\Omega$)	CSD18531Q5A ($R_{ds} = 5\text{m}\Omega$), $T_{on} + T_{off} = 35\text{ns}$	2.5A	$\approx 96\%$
12V (4-cells)	16.66A	80V (= 400/5)	5	1.2mH ($R_L = 16\text{m}\Omega$)	AON7280 ($R_{ds} = 6.5\text{m}\Omega$), $T_{on} + T_{off} = 80\text{ns}$	2.5A	$\approx 96\%$
24V (8-cells)	13.88A	133.33V (= 400/3)	3	2.8mH ($R_L = 20\text{m}\Omega$)	FDMS86250 ($R_{ds} = 20\text{m}\Omega$), $T_{on} + T_{off} = 80\text{ns}$	2.5A	$\approx 97.0\%$

Different voltage batteries need different devices. This device selection has been done based on to commercially available MOSFET's with the lowest on-resistance (R_{dson}) to get the highest possible efficiency. It can be seen that (in Fig. 3.6) on-state resistance reduces as the voltage reduces (100V). However, the rate of reduction of on-state resistance decreases at the very low end. For this reason, the efficiency of the converter reduces when using a low number of series batteries per module as shown in Table 3-2. The highest efficiency reaches at 24V input voltage (i.e. 8-cells in series) in this case. Efficiency again starts to reduce when the module input voltage increases gradually because the MOSFET on-state resistance starts to increase at higher voltages. Table 3-3 shows the power loss calculation using unequal modules. A particular set of batteries was taken to replicate the hardware setup and afford comparison in this case.

It can be concluded that calculated efficiency of the converter has a reasonable value across a range of voltages within the accuracy of the calculation.

Table 3-3 An example calculation in boost mode (unequal module) at 1kW power level

Modes	module input voltages	Current in the modules	Boost inductor	Active Switch (MOSFET)	dc-link current (I_{dc})	Theoretical Efficiency
Boost	12V, 24V, 7.5V	8.0A, 17A, 4.5A	1.5mH ($R_L=20m\Omega$)	FDPF085N10A ($R_{ds} = 8.5m\Omega$, $T_{on} + T_{off} = 77ns$)	2.5A	98.0%

3.4.2 Theoretical calculation of Mode – 2 (buck mode)

The expression of the power losses in mode – 2 is shown in (3.8). The power losses in this mode comprises of: a) losses in module inductor, b) conduction losses in S_{ii} , c) conduction and switching losses in T_i and T_{ii} , d) losses in the dc-link inductance (L_{dc}). It is assumed all the switches in an H-bridge are identical and have same turn on and turn off times. Therefore, an expression of power loss can be written as follows where N represents the total number of modules:

$$P_{L2} = (\sum_{i=1}^N i_{batt,i}^2)R_L + (\sum_{i=1}^N i_{batt,i}^2)R_{ds(on)} + (\sum_{i=1}^N V_{dc,i}i_{batt,i})\left(\frac{T_{on}+T_{off}}{T_s}\right) + NI_{dc}^2 R_{ds(on)} + I_{dc}^2 R_{dc} \quad (3.8)$$

In this mode the overall voltage of the battery side has to be greater than the central dc-link voltage ($\sum_{i=1}^N V_{batt,i} > V_{dc}^*$). Therefore, either extremely large numbers of relative low voltage (3V/12V etc.) modules or low number of high voltage (200V/400V etc.) modules is required as a result of this voltage constraint. Therefore, each module will have to deliver much less current to achieve the same power level (1kW) as shown in Table 3-4. However, it should be noted that the dc-link current (I_{dc}) will remain to the same value as before. The input boost inductance becomes almost inoperative in this mode because (S_i, S_{ii}) do not operate in PWM fashion. Assuming a minimum 400V dc-link voltage has to be met, two cases have been studied: a) 3V cell (standard cell voltage) with 150 modules at 2.20A current ($\sum_{i=1}^{150} V_{batt,i} = 450V$), b) 150V (a standard voltage of EV battery/battery charger), 3 modules at 2.20A current ($\sum_{i=1}^3 V_{batt,i} = 450V$). The loss/efficiency result has been presented in Table 3-4 at the same power level as earlier. It can be seen that the calculated efficiency is very high (99%) because the increase in number of modules is largely compensated for by the lower $R_{ds(on)}$ component and low module current. However, it may not be feasible to build a power converter with such a high number of modules under utilising the semi-conductors particularly at lower power levels (< 10kW). Therefore, this operational mode is mainly suitable for higher power levels.

Table 3-4 Efficiency/power loss calculation in buck mode at 1kW power level

module voltage (assuming equal modules)	input equal	Module Current	Active (MOSFET) Switch	dc-link current (I_{dc})	Efficiency
3V		2.20A	SIR494DP ($R_{ds} = 1.5\text{m}\Omega$), $T_{on} + T_{off} = 88\text{ns}$	2.5A	> 99.0%
150V		2.20A	RJK2057DPA ($R_{ds} = 85\text{m}\Omega$), $T_{on} + T_{off} = 128\text{ns}$	2.5A	> 99.0%

3.4.3 Theoretical calculation of Mode – 3 (boost-buck mode)

The power losses in this mode comprises of: a) losses in module boost inductor, b) conduction and switching losses in S_i and S_{ii} , c) conduction losses and switching losses in T_i and T_{ii} , d) losses in dc-link inductance (L_{dc}). The expression of the power loss in mode – 3 is shown in (3.9). It can be noticed that, the power loss includes the switching losses of all the four switches in a module. Therefore, the power loss in this mode is higher than mode – 1 and mode – 2 for the same power level.

$$P_{L3} = \left(\sum_{i=1}^N i_{batt,i}^2\right)R_L + \left(\sum_{i=1}^N i_{batt,i}^2\right)R_{ds(on)} + \left(\sum_{i=1}^N V_{dc,i} i_{batt,i}\right) \left(\frac{T_{on}+T_{off}}{T_s}\right) + \left(\sum_{i=1}^N V_{dc,i}\right)I_{dc} \left(\frac{T_{on}+T_{off}}{T_s}\right) + NI_{dc}^2 R_{ds(on)} + I_{dc}^2 R_L \quad (3.9)$$

In this mode, the voltage of the battery side can be greater or less than the central dc-link voltage ($\sum_{i=1}^N V_{batt,i} > V_{dc}^*$ or $\sum_{i=1}^N V_{batt,i} \leq V_{dc}^*$). As a result, this operational mode is suitable at low as well as at high number of modules. Each module is operated at higher boost ratio (say > 5) when working with a lower number of modules, compared to mode – 1 and modules are operated with a lower boost ratio (2-3) while working with a higher number of modules. In order to compare with the mode – 1, the same case has been studied as before: e.g. a) 3V cell with 17 modules 19.6A current. At first, equal modules have been assumed and efficiency has been calculated. Thereafter, a case with unequal modules has been taken to calculate the loss. Since there could be a large set of unequal modules, therefore, the same set as mode – 1 has been considered.

It can be seen from Table 3-5 that the efficiency of this mode is approximately less than 1 – 2% compared to mode – 1. Moreover, the efficiency with low module input voltage is very low (similar to mode – 1 with the same set of batteries). The loss or efficiency calculation for unequal modules has been presented in Table 3-6.

Table 3-5 Efficiency/power loss calculation in boost-buck mode (equal modules)

module input voltage (assuming equal modules)	Current	No. of modules meet minimum 1kW	Boost inductor	boost inductor	Active Switch (MOSFET)	dc-link current (I_{dc})	Efficiency
3V	19.6A	17	0.3mH ($R_L = 4m\Omega$)	0.15mH ($R_L=0.75m\Omega$)	AO4726 ($R_{ds} = 4.5m\Omega$, $T_{on} + T_{off} = 108ns$)	2.5A	$\approx 93.0\%$
6V	18.5A	9	0.6mH ($R_L = 8m\Omega$)	0.3mH ($R_L = 1.5m\Omega$)	CSD18531Q5A ($R_{ds} = 5m\Omega$, $T_{on} + T_{off} = 35ns$)	2.5A	$\approx 95.0\%$
12V	16.66A	5	1.2mH ($R_L = 16m\Omega$)	0.6mH ($R_L = 3m\Omega$)	AON6452 ($R_{ds} = 18m\Omega$, $T_{on} + T_{off} = 38ns$)	2.5A	$\approx 95.0\%$
24V	13.88A	3	2.8mH ($R_L = 20m\Omega$)	1.2mH ($R_L = 6m\Omega$)	FDMS86250 ($R_{ds} = 25m\Omega$, $T_{on} + T_{off} = 44.5ns$)	2.5A	$\approx 97\%$

Table 3-6 Efficiency/power loss calculation in boost-buck mode (unequal modules)

Mode	module input voltages	Current in the modules	Boost inductor	Active Switch (MOSFET)	dc-link current (I_{dc})	Theoretical Efficiency
Boost-buck	12V, 24V, 7.5V	8.0A, 17A, 4.5A	1.5mH ($R_L=20m\Omega$)	FDPF085N10A ($R_{ds} = 8.5m\Omega$, $T_{on} + T_{off} = 77.0ns$)	2.5A	$\approx 97\%$

3.5 Validation of different modes of operation

The converter operation has been validated under fixed conditions in keeping with equipment availability. the power loss/efficiency reading has been measured at a particular operating point. A hardware set-up using the prototype described in chapter –7 has been built using three battery modules as detailed in Table 3-7. The two operational dc modes have been validated: a) cascaded boost, b) boost-buck mode. Buck mode has not been separately tested due to the fact that building a high number of modules (e.g. > 10) or using a high voltage battery system (e.g. > 200V) is difficult in the available laboratory test environments. Experimental analysis was carried out to validate different modes of operation and the power loss and efficiency. Both simulation and experimental has been provided for comparison and completeness of the study.

3.5.1 Boost Mode

In order to demonstrate the operational of this mode, all the dc-link voltages ($V_{dc,i}$) and total dc-link voltages were measured. Simulation and experiments have been performed using specifications presented on Table 3-7 . The validation is performed in two stages: a) module

dc-link voltages ($V_{dc,i}$) and the central dc-link voltage (V_{dc}) have been measured; b) the dc-link current (I_{dc}) and voltage across A and B (V_{AB}) in Fig. 3.1 are measured.

It can be seen from Fig. 3.7 and Fig. 3.8 that the sum of all the dc-link voltages is the total dc-link voltage. This cross-checks that all the modules are in series/cascaded and T_i, T_{ii} are operating in idle mode. Moreover, the voltage V_{AB} in Fig. 3.1 and dc-link current I_{dc} has been shown V_{AB} is a continuous dc voltage ($=V_{dc}^*$) (due to T_i ON and T_{ii} OFF) and I_{dc} is a dc current with 100Hz ripple on it due to the 1- ϕ operation. Fig. 3.9 shows the simulation result of cascaded boost mode. Similar experimental result is shown in Fig. 3.10. Simulation and experimental results show a reasonable match.

Table 3-7 Components specifications used in experimental validations

Type/Name	Rating/specification
Boost inductors of dc-dc modules	1.5mH, 15A, $R_L = 20\text{m}\Omega$
Switching frequency of the dc-dc modules	10kHz
Operating central dc-bus voltage	150V
Grid Voltage	120 (peak), 50 Hz
Test Power Level	$\approx 500\text{W}$
Battery module -1	12V, 10Ah lead acid – $V_{max} = 13.8\text{V}$ $V_{min} = 9.6\text{V}$, $Z_{nom} = 0.015\Omega$
Battery module -2	24V, 16Ah lead acid – $V_{max} = 29\text{V}$ $V_{min} = 19\text{V}$, $Z_{nom} = 0.02\Omega$
Battery module -3	7.2V, 6.5Ah NiMH – $V_{max} = 8.5\text{V}$ $V_{min} = 5\text{V}$, $Z_{nom} = 0.011\Omega$

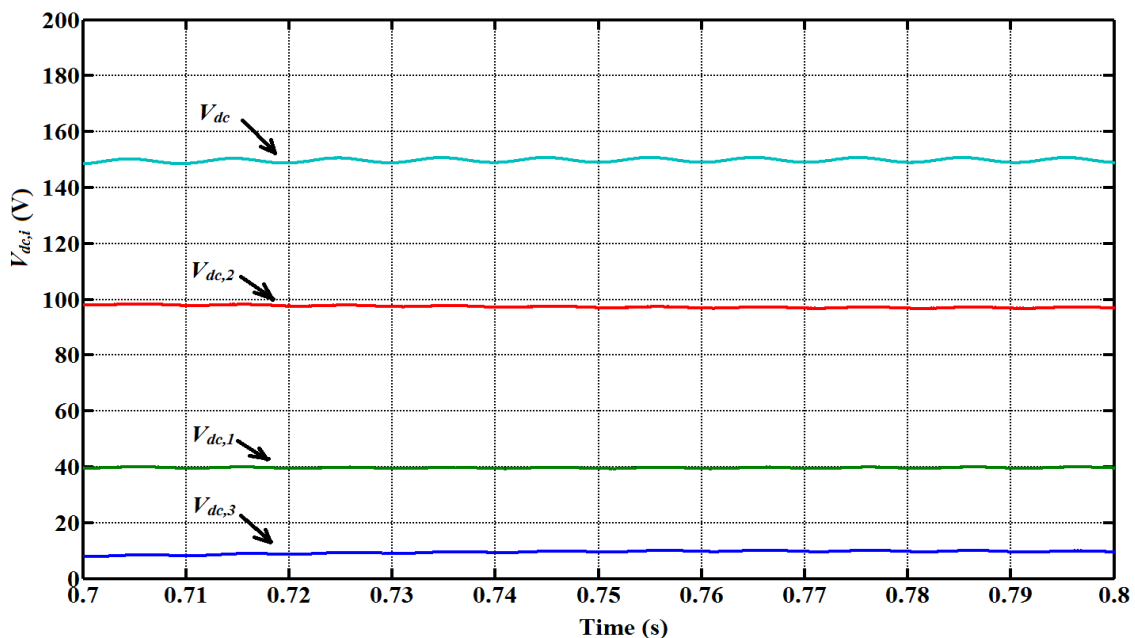


Fig. 3.7 Cascaded boost mode of operation: Simulation result – 1



Fig. 3.8 Cascaded boost mode of operation: Experimental result – 1 (time scale 20ms/div, voltage scale 20V/div)

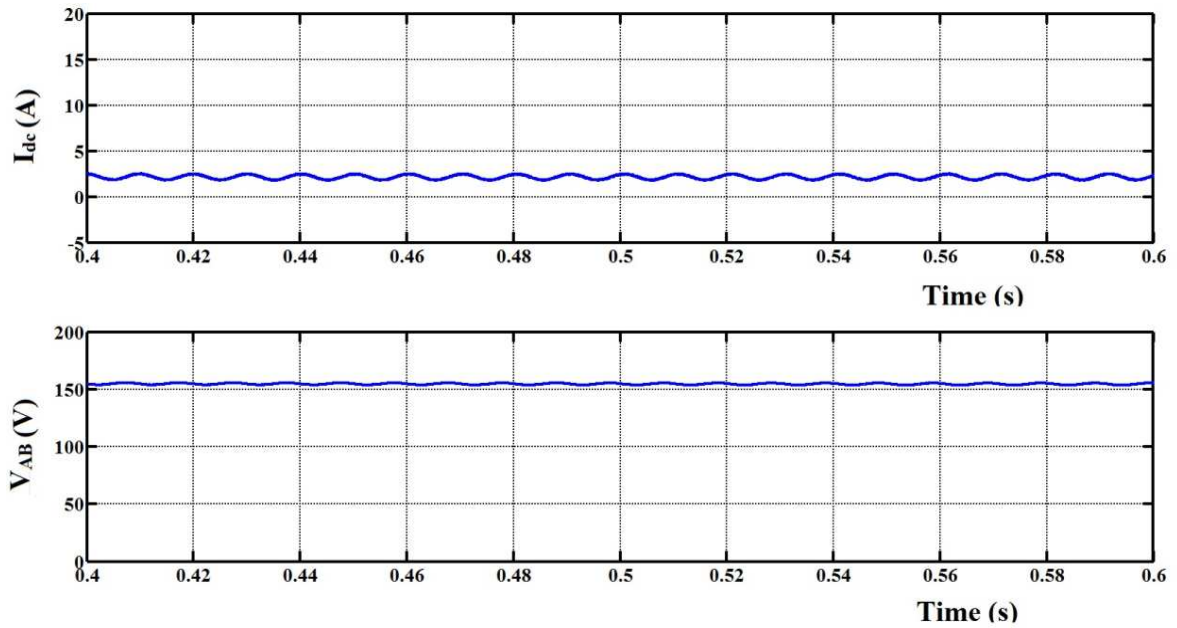


Fig. 3.9 Cascaded boost mode of operation: Simulation result – 2



Fig. 3.10 Cascaded boost mode of operation: Experimental result – 2 (time scale 20ms/div, voltage scale 50V/div, current scale 5A/div)

3.5.2 Boost-buck Mode

In boost-buck mode also the voltage V_{AB} and the dc-link current I_{dc} act as a representative of this mode of operation. In this mode, the voltage V_{AB} is a multilevel waveform due to PWM switching of T_i, T_{ii} in contrast to earlier and I_{dc} is a continuous dc current without having 100Hz ripple due to the control of dc-dc converter. Fig. 3.11 shows a simulation result of boost-buck mode of operation. It can be seen that V_{AB} shows a multilevel dc-dc operation per switching cycle (four levels of operation can be seen with three modules) and I_{dc} is a continuous current with switching ripple on it. The multilevel operation is possible due to the fact that individual modules have been switched with different duty ratios (due to distributed control of the hybrid batteries). On the other hand, Fig. 3.12 shows the corresponding experimental result. This multilevel dc-dc operation proves the functionality of switching operations all the four switches S_i, S_{ii}, T_i and T_{ii} . However, there is a clear difference between the simulation and the experimental steps in multilevel dc-dc waveform. This is because of relative distribution of duty ratios for T_i, T_{ii} in simulation and in experiments. This difference appears because of the closed loop control of the overall multilevel converter and the battery operating conditions in practice which are subjected to change as a battery module charge/discharge. The experimental result was captured at a particular operating point which was very difficult to match with the operating point in simulation. However, these results show the functionalities of multilevel dc-dc converter. The details of this control system are presented in chapter 5.

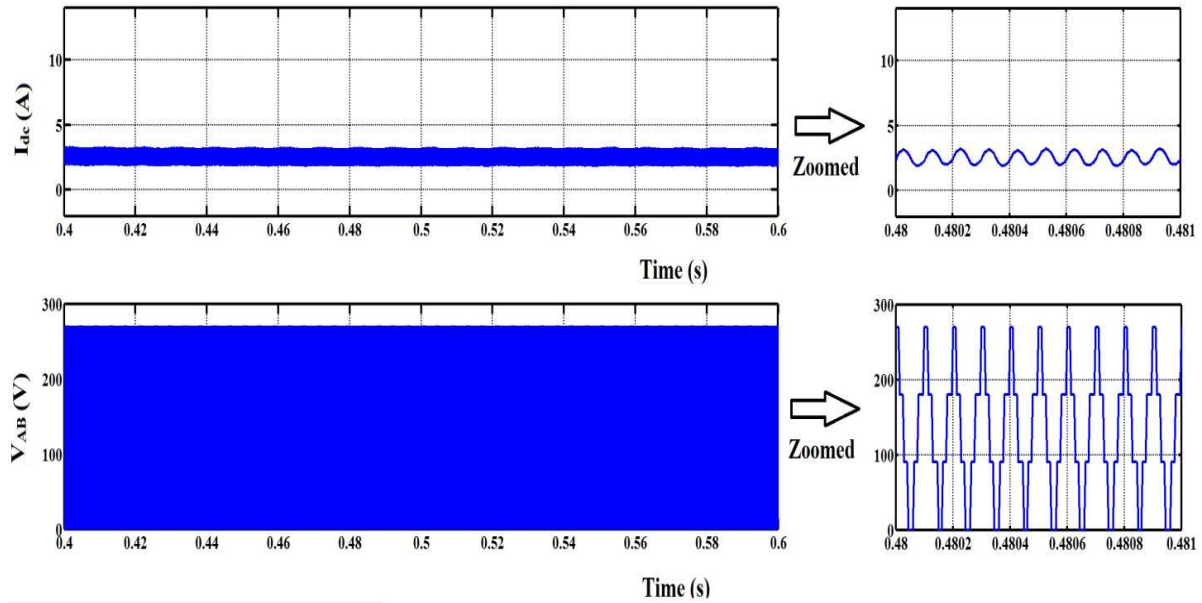


Fig. 3.11 Boost-buck mode of operation: Simulation result

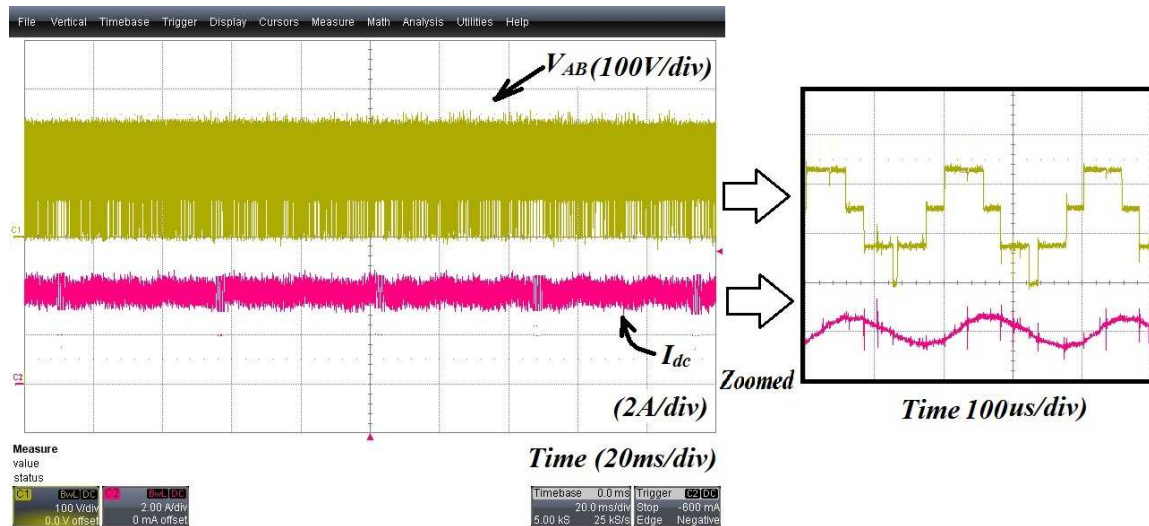


Fig. 3.12 Boost-buck mode of operation: Experimental result (time scale 20ms/div, voltage scale 100V/div, current scale 2A/div)

3.6 Validation of Power loss/efficiency

The converter power loss/efficiency can be estimated using the ratio of output power to input power of the converter. This does not provide a very accurate result but it acts as a good indication of efficiency. More accurate methods have been investigated in the literature which uses calorimetric power loss measurement (CPLM) methods as described [332] – [334]. These methods are used in specific applications where a precise measurement of efficiency is needed such as high efficiency power converters. However, this equipment was not available for use.

In this work, the former estimation approach has been followed to get an indication of converter efficiency in different operational modes. The converter losses and efficiency was measured using a high precision LeCroy oscilloscope and multi-meters. Cascaded boost mode and boost-modular multilevel buck mode were tested.

3.6.1 Switching Loss Measurement

Switching loss has been estimated using voltage and current measurement on an oscilloscope. The product of voltage, current and switching time, the energy loss has been used to estimate. Therefore, the method is similar to [335]. The transient between turn ON and turn OFF as shown in Fig. 3.13. There is a current overshoot (about two times of the nominal current) observed during turn ON of the device. This is due the reverse recovery of the body diode. This reverse recovery slightly increases the switching loss. There is a little voltage overshoot is observed during turn OFF due to the parasitic inductance of the PCB. The transition is shown for only for one module, similar result can be obtained for remaining modules because all the modules use identical switches in the designed prototype.

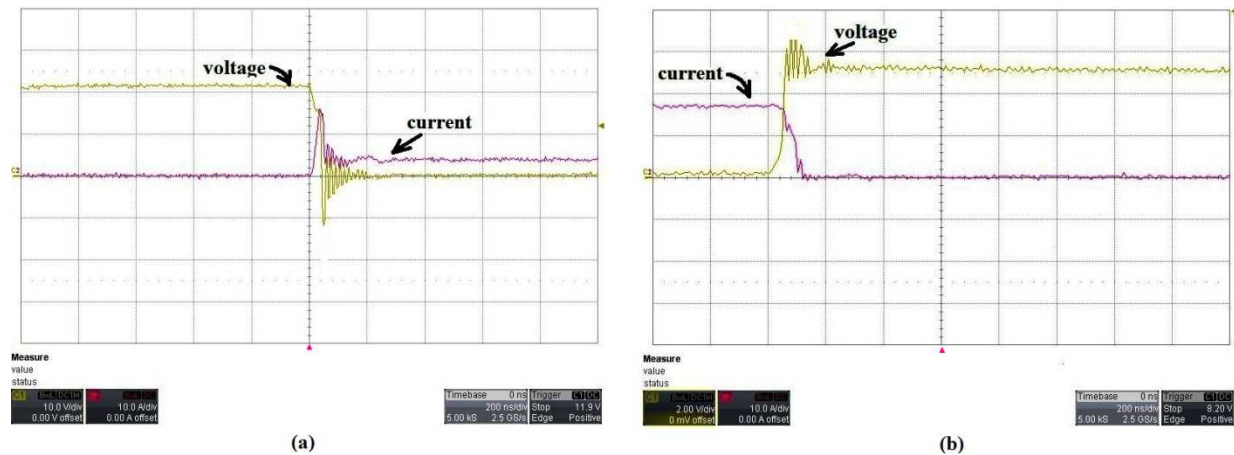


Fig. 3.13 Switching transients of FDPF085N10A: a) Turn ON transient b) Turn OFF transient (scale time 200ns/div, voltage 40V/div, current 10A/div)

3.6.2 Conduction loss measurement

In order to estimate the conduction losses of a switch, three steps have been followed: a) first estimate the total loss of a switch, b) estimate the switching loss, and c) estimate the conduction loss = total loss – switching loss. The procedure has been detailed as follows:

- i) At first, the case temperature (T_c) of a switch is measured using a thermocouple and thermo camera.
- ii) Approximate junction temperature (T_j) is predicted using the thermal coefficient found from the device data sheet.
- iii) Then the total power loss in the switch is calculated using $P_{sw} = \frac{T_j - T_A}{\theta_{jA}}$ where T_A is the ambient temperature (taken as 20°C).
- iv) The conduction loss is taken as the difference between the total estimated power loss and switching loss measured by above mentioned method.

3.6.3 Inductor Loss Measurement

Inductor loss can be of two types: a) high frequency AC loss – eddy current or hysteresis loss and, b) conduction loss – due to leakage resistance of an inductor. The former loss generally

becomes significant when the switching frequency is very high (> 50 kHz) [336]. Therefore, in this research, only conduction losses have been considered as a potential inductor loss. This loss has been measured as a product of measured inductor voltage and current through it.

3.6.4 Overall loss

Power loss in the modular dc-dc converter was measured at the same power levels (≈ 500 W) for boost and boost-buck mode at the same battery operating point. Fig. 3.14 shows the comparison between the two modes. It is found that boost-buck mode has higher losses and lower efficiency (about 1 – 2%) compared to boost mode as expected. However, the difference comes down in higher power levels. Theoretical and experimental estimation comparison is provided in Table 3-8. The detailed loss distribution along with calculated values is presented in Table 3-9 where the loss in each part of the converter has been shown separately along with corresponding calculated values. The measured case temperature of the switches is presented in Table 3-10 to provide an indication of losses in each module. It can be seen that the second module which takes a higher share of current has the higher case temperature as expected.

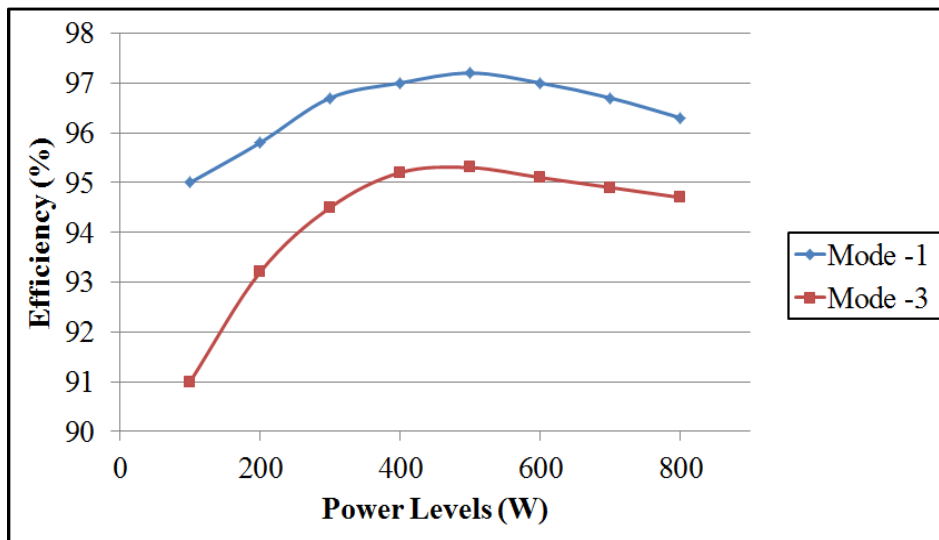


Fig. 3.14 Experimental efficiency comparison of different modes of operation

Table 3-8 Theoretical and experimental efficiency using different modes at a particular operating point

Modes	module nominal input voltages	Current in the modules	module capacitor voltages	Boost inductor	Active Switch (MOSFET)	dc-link current (I_{dc})	Theoretical Efficiency	Measured Efficiency (from input to output)
Boost	12V, 24V, 7.2V	8.0A, 17A, 4.5A	60V, 70V, 20V	1.5mH ($R_L=20m\Omega$)	FDPF085N10A ($R_{ds} = 8.5m\Omega$)	2.5A	$\approx 98\%$	$\approx 97.0\%$
Boost-buck	12V, 24V, 7.2V	8.0A, 17A, 4.5A	90V, 90V, 90V	1.5mH ($R_L=20m\Omega$)	FDPF085N10A ($R_{ds} = 8.5m\Omega$)	2.5A	$\approx 96\%$	$\approx 95.0\%$

Table 3-9 Detailed Loss distribution in the converter

Modes	Conduction loss		Switching loss		Inductor loss		Total loss	
	Calculated	Measured	Calculated	Measured	Calculated	Measured	Calculated	Measured
Boost	3.5W	≈ 4W	1.3W	≈ 2W	7.5W	≈ 9W	12.3W	≈ 15W
Boost-buck	3.5W	≈ 5W	3W	≈ 4.0W	7.5W	≈ 9W	14W	≈ 18W

Table 3-10 Measured case temperature of the module switches under real operating condition

Modes	module nominal input voltages	Current in the modules	module capacitor voltages	Measured case temperatures of module switches
Boost	12V, 24V, 7.2V	8.0A, 17A, 4.5A	60V, 70V, 20V	$S_1/S_{11} \rightarrow (40/30^\circ\text{C})$ $T_1/T_{11} \rightarrow (26/20^\circ\text{C})$ $S_2/S_{22} \rightarrow (70/40^\circ\text{C})$ $T_2/T_{22} \rightarrow (26/20^\circ\text{C})$ $S_3/S_{33} \rightarrow (28/24^\circ\text{C})$ $T_3/T_{33} \rightarrow (26/20^\circ\text{C})$
Boost-buck	12V, 24V, 7.2V	8.0A, 17A, 4.5A	90V, 90V, 90V	$S_1/S_{11} \rightarrow (40/30^\circ\text{C})$ $T_1/T_{11} \rightarrow (38/30^\circ\text{C})$ $S_2/S_{22} \rightarrow (70/40^\circ\text{C})$ $T_2/T_{22} \rightarrow (36/30^\circ\text{C})$ $S_3/S_{33} \rightarrow (28/24^\circ\text{C})$ $T_3/T_{33} \rightarrow (32/24^\circ\text{C})$

3.7 Conclusion

This chapter has presented the practical operational modes of the proposed converter for second life battery energy storage systems. The proposed converter has cascaded H-bridge dc-dc modules where both of the legs can be switched independently to get every possible operational mode (e.g. boost, buck, and boost-buck). The detail of each operational mode has been described. The proposed converter is capable of integrating widely different batteries (with equal or unequal modules) to a common dc-bus with an inverter where differences in the sum of the total battery voltages (> or < dc-link voltage) can be accounted for. The converter design has been undertaken in a manner such that any batteries within a pre-defined operating envelope can be swapped if any of the modules fail during the operation.

Power loss and efficiency have also been analysed and experimentally validated in different modes as far as the equipment available. A careful selection of module size is important to maximise converter efficiency. Moreover, different operational modes can give rise to different efficiency figures for a set power level. The boost mode of operation is more efficient compared to boost-buck mode of operation at all power levels. However, the latter mode of operation provides a wide range of control flexibility which will be helpful to control widely different batteries.

4 Distributed Power Sharing Strategy for Second Life Hybrid Batteries

4.1 Introduction

To enable research and investment on hybrid new/second life batteries systems, prior to a significant second life market, requires that these different batteries with different characteristics and reliability be combined within a single energy storage system that allows the differences in performance to be taken into account. This is unlike a new battery system which has homogenous units formed together into modules, with batteries likely to react the same way. A hybrid second life system has different modules of different ages and sizes which are more prone to vary (e.g. capacity fade, impedance increase) during the second life operation. This makes the control strategy significantly different compared to existing BESS. This chapter concentrates on a power sharing strategy development for the hybrid batteries or in other words, the way of distributing the total converter power among the heterogeneous battery modules so that each individual module is utilised optimally.

Previous research related to dealing with differences in the performance of a hybrid system has been focused around three different areas; a) dealing with batteries with slightly different performance, b) dealing with batteries in conjunction with other power sources such as, PV/wind or super-capacitors etc. and c) dealing with PV panels under conditions of partial shading.

Batteries with slightly different performance (for example voltage or state of charge imbalance) are typically dealt with through either active or passive balancing/equalization circuits without considering the overall energy storage system [125] – [131], [155] as described in chapter – 1. However, these systems deal with one type of battery and the differences between cells is fairly minimal. This approach can be used within the same battery cell type but isn't feasible across different batteries where the performance differences are greater than just voltage and SOC balancing.

Energy storage systems with batteries in conjunction with other power sources such as, wind/PV typically use the energy storage medium as a mechanism for either smoothing the power from the system or to compensate power mismatch between generation and the required dispatched amount [259], [218]. In some cases, the battery/super-capacitors combination is used in hybrid energy storage systems (to increase the battery useful life) [219] – [220]. Most of these researches use a common dc bus and the power sources are connected in parallel. Reference [261] presents a supervisory control technique to optimize the power output of a wind-PV hybrid generation system. It uses a single type of lumped battery system connected in parallel with a central dc-bus and mainly concentrates on optimizing the performance of each source while ignoring the performance implications of

the battery. Another set of research [337] – [338] discuss similar hybrid energy storage system with PV panels using parallel dc-dc converter which allows maximising the energy extracted from the PV panels in grid connected and islanded modes.

Previous researches into PV panels mainly concentrate on peak power tracking in the event of some of the PV panels operating under partially shaded conditions. Early research set the output voltage of each panel based on a weighting factor designed vary directly with the irradiance [338]. More complicated control algorithms under varying irradiance look to limit voltages under an adaptive supervisory control system were reported in [339]. However, the control strategy for a PV system is unidirectional and dependent only on radiation condition which is not applicable in BESS.

There are no published research till now reports explicitly on a grid-tie hybrid energy storage system using different types of batteries together (new/second life) together, with a suitable power sharing and its control strategy considering widely different performance characteristics. This shortfall is addressed in this chapter where a distributed power sharing strategy based on weighting function is proposed which represents instantaneous characteristics of a battery module. This weighting factor based strategy enables the utilisation of any set of hybrid batteries according to their characteristics while providing the uninterrupted grid support.

4.2 Preliminary characterisation

After getting these batteries from different vehicles, their past history will most likely be unknown. Information is available from initial strip down and preliminary testing/characterization and should include; a) battery module type/chemistry, b) battery module capacity, c) battery module nominal open circuit voltage, d) maximum and minimum safe voltages, d) battery module lumped internal impedance and e) initial battery module SOC. Each module of the converter should contain similar batteries (in terms of capacity, nominal voltage etc.) with proper balancing among of the series connected cells.

4.2.1 Capacity

The initial capacity of a battery can be determined from a number of different methods such as; discharge characteristics [341], open circuit voltage (OCV) [342], internal impedance [345]. The discharge method calculates the total time to fully discharge a battery from the fully charged condition at a constant current and then takes the product of time and current to estimate the capacity. The takes a long time to perform but was found to be reasonably accurate. The second method uses an OCV-SOC look-up table or a derived relation to find the SOC and then a coulomb counting equation to find the capacity. The method is accurate but suffers from a drawback in measuring the initial SOC accurately. However, the drawback of initial SOC measurement can be overcome using sample-by-sample approach as reported in [343]. The third method is based on the internal impedance of a battery. At first the internal impedance is estimated and then a pre-defined capacity-impedance ($Q_{max} - Z$) relation is used to calculate the capacity. This relationship can be a linear relationship as reported in [344] or can be a nonlinear relationship [341]. This thesis adopts the method of discharge characteristics to determine the initial capacity because it is simple to perform on

an unknown battery and is the only method which does not require any characterisation to be performed prior to the test. The accuracy of this method depends on the temperature, e.g. high temperature of operation increases the battery capacity and vice-versa. Therefore, the experiment was performed at around 20°C.

4.2.2 SOC-OCV relationship

SOC determination is necessary for use in the power sharing strategy. The methods for calculating SOC were described in chapter – 1. Within this thesis it is deemed sufficiently accurate to use the SOC-OCV relationship because it is easy to use a derived relationship online and also widely used method to estimate the SOC [346] – [350]. To generate an OCV-SOC look-up table, the following steps are used.

- a) SOC was determined through the coulomb counting equation for a known capacity
- b) Discharge the battery with a small current (about 1A) on small regular intervals and keep at rest for about 10 – 15 min to attain *OCV*. Some cases it takes a long time (e.g. hours) to attain *OCV* depending on the battery types especially after a deep discharge as reported in [351]. However, such deep discharge situation is avoided here while performing the experiments and therefore, such situation has not been considered in this work.
- c) Terminal voltages were measured on regular intervals.
- d) Plot the voltages and the SOC.

Fig. 4.1 shows a sample result for a 12V, 10Ah lead acid and 7.2V, 6.5Ah NiMH batteries that were used in the experimental prototype. It can be seen that the curve appears to be linear within the 10 – 90% SOC range. Therefore, a curve of best fit has been taken to simply the relationship. This relationship is later used to estimate the SOC from the OCV.

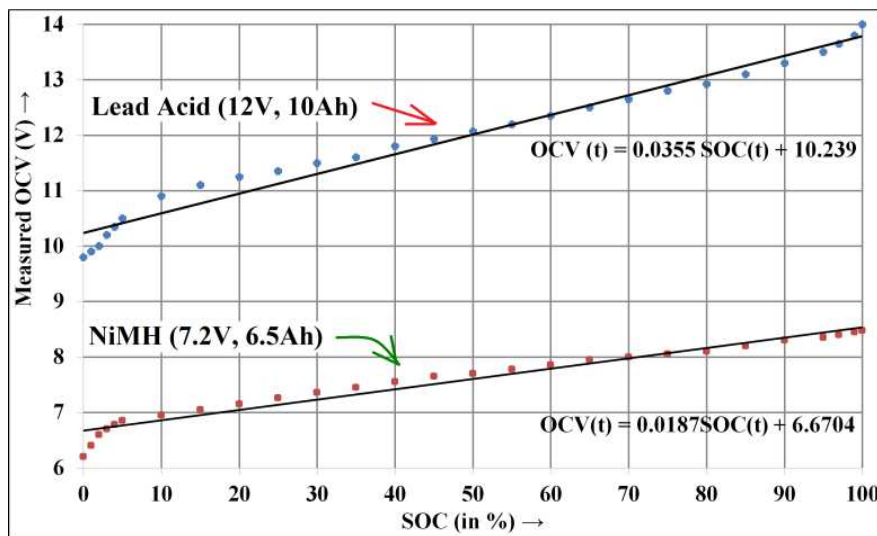


Fig. 4.1 SOC-OCV relationship for Lead acid and NiMH batteries

4.2.3 Initial impedance

Internal impedance of a battery can be used as an indication of state-of-health (SOH) determination, both with and without capacity data [345]. Moreover, this internal impedance value can be used to help detect the battery failure [352]. Battery impedance tends to vary with the age, usage and ambient conditions such as, temperature. In the laboratory, the experiments are performed at 20°C ambient conditions. Therefore this temperature coefficient has not been taken into consideration at this stage.

There are many methods to estimate the impedance of battery: a) a pulse current based method [353], b) an online impedance method similar to [354] and [359], c) EIS based techniques [355]. Among the different methods, a pulse current based method is simple, inexpensive and is suitable when a battery is stationary i.e. when a battery is not connected to a load. EIS based technique [355] is also suitable for when a battery is stationary but it requires an expensive equipment.

Within this work, a pulse load test as described in [353] has been used to find the initial impedance of a battery because of simplicity and unavailability of EIS equipment. A dc-dc converter can be controlled according to a pulse current reference as shown in Fig. 4.2. The terminal voltage is measured at every instance and the impedance is found from the ratio of sudden voltage drop to current ($Z = \frac{\Delta V}{I}$). This is reasonable approach because SOC does not change instantaneously, therefore the battery OCV can be considered to be constant during this small time interval and the instantaneous drop in terminal voltage is due to the internal IR drop only during discharging. However, this method is only used for pre-characterisation to ensure the starting condition is correct and an alternative method is used for online-calculation (described later) which tracks impedance online.

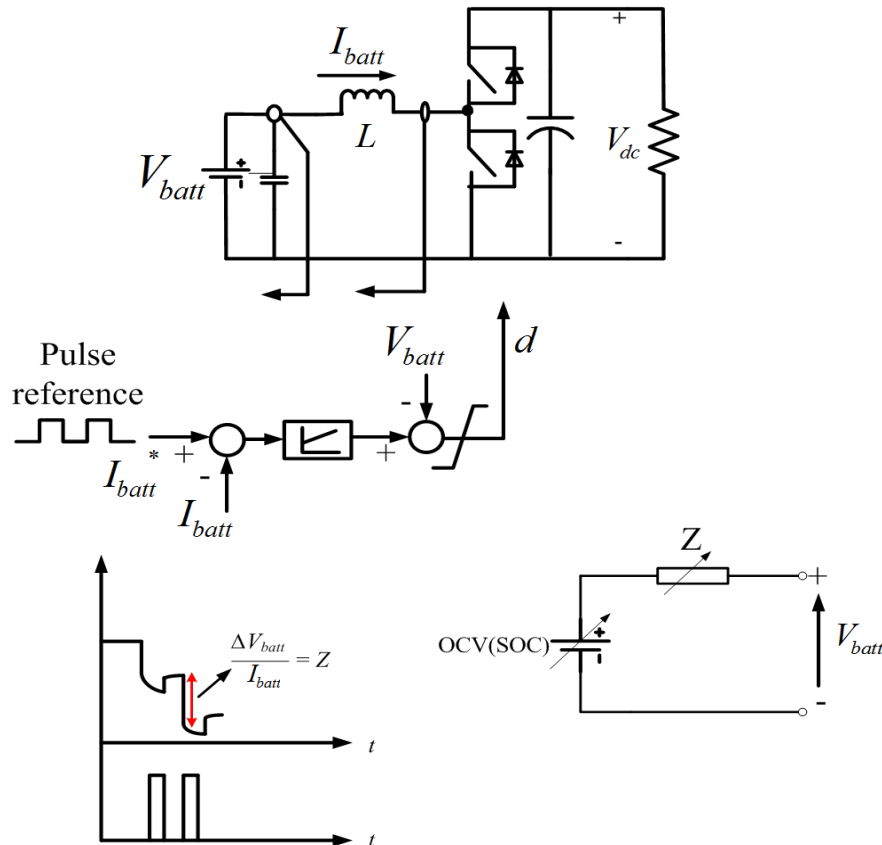


Fig. 4.2 Pulse load test to find initial internal impedance using a dc-dc converter control

4.3 Proposed distributed sharing strategy

Battery charging or discharging thoroughly depends on the current and all the battery parameters under investigation SOC, impedance, voltage, capacity can be related to the battery current through equations or lookup tables and therefore it is appropriate to distribute the total power using the individual module current. Therefore, a current sharing strategy is adopted in this thesis.

There is a hybrid mix of modules within the BESS. Therefore each of these module types will charge/discharge at different rates and have different maximum/minimum safe amounts of charge and voltages. Ideally none of the modules should be bypassed unless an abnormal condition or a fault is detected, so each battery module should take a proportionate share of the total power contribution relative to each other.

Therefore, the charging/discharging strategy proposed in this thesis is to ensure that the charging/discharging trajectory of the hybrid modules during a charging or discharging cycle will all arrive at their respective maximum and minimum values (in terms of voltage or SOC) at the same time. This means all the modules would reach their SOC_{max} or V_{max} and SOC_{min} or V_{min} at the same time.

Before developing a sharing strategy, the following terminology and assumptions are listed;

- A *battery* is a collection of identical cells types
- A *battery module* is a collection of identical battery types
- A battery capacity has been taken as the maximum charge left (Q_{max} in C or Ah) that a battery can deliver to a load
- A module battery is modelled as an open circuit voltage (OCV) with series impedance (Z) as shown in Fig. 4.3 or in other words $V_{batt,i} = OCV_i \pm i_{batt,i} Z_i$. There are other battery models as reported in [356] – [358] which are specific to battery types. However, this impedance based battery model is commonly used in the control system study with reasonable accuracy such as in [184] because it is straightforward, widely used and easy to estimate the OCV from the terminal voltage and the current measurement within a controller.
- Each battery module have different initial SOC (or $OCV_{o,i}$) at start, different maximum/minimum voltage limits and also different capacity ($Q_{max,i}$).
- The instantaneous charge (Q) available in a module is represented by the maximum charge available (Q_{max}) times the SOC (as a per unit representation).

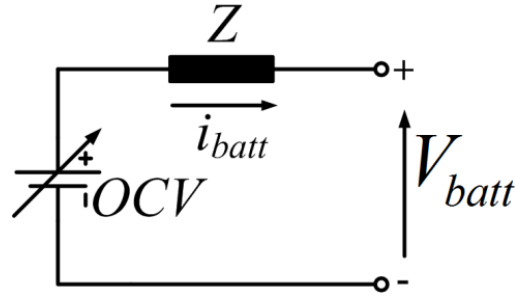


Fig. 4.3 Impedance based battery model

Each battery and module contains a balancing network and it is assumed that within each module the following parameters are equal and where necessary known from pre-characterization:

- Maximum and minimum voltage limits ($OCV_{max,i}$, $OCV_{min,i}$)
- Maximum and minimum charge limits or Capacity ($Q_{max,i}$)
- Relationship between SOC and open-circuit voltage (OCV)
- Initial internal impedance

The concept of the proposed power sharing strategy can be explained with the aid of Fig. 4.4, which shows batteries with different capacity and starting charge, finishing their discharge cycle at the same time.

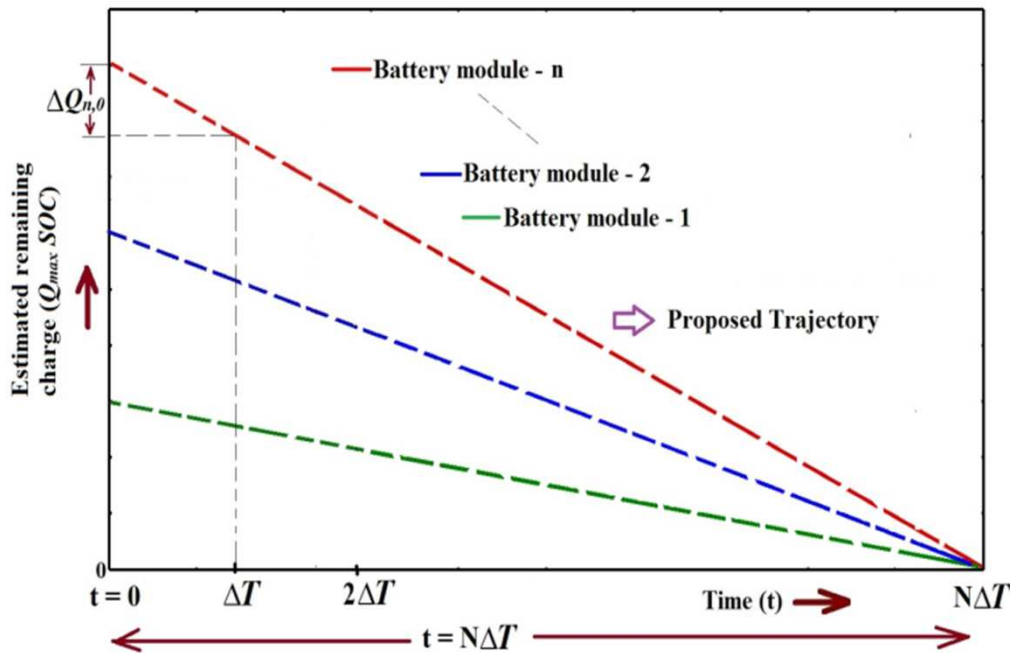


Fig. 4.4 Proposed strategy to deal with the hybrid batteries trajectory

Let's assume that the total remaining time to charge or discharge (say t) can be considered to be divided into a number of small equal time periods (ΔT), dependent on the sample time, i.e. $t = N\Delta T$ as shown in Fig. 4.4. During discharging, in the first time step the required change in charge of n^{th} module is $\Delta Q_{n(0)}$, where

$$\Delta Q_{n,(0)} = \frac{Q_{max,n,(0)}SOC_{n,(0)}}{N} \quad (4.1)$$

So that an equal change in charge per time step is assumed and $Q_{max,n}SOC_{n,0}$ represents the total remaining charge in module n at time $t = 0$ and N is the total number of sample periods before the battery is fully discharged.

A similar expression can be obtained for charging at $t = 0$ as shown in (4.2):

$$\Delta Q_{n(0)} = \frac{Q_{max,n,(0)}(1-SOC_{n(0)})}{N} \quad (4.2)$$

Charging/discharging depends on the module current. Previous research shows battery SOC and capacity are related through a linear coulomb counting equation [353]. The fundamental charge equation, the relation between charge and SOC for a module is given by (4.3) where the Q_o is the initial charged stored.

$$Q(t) = Q_0 + \int_0^T i_{batt} dt \quad (4.3)$$

Over a small sample period, ΔT , (4.3) can be re-written as

$$\int_0^{\Delta T} i_{batt,n} dt = \Delta Q_n \quad (4.4)$$

Within the small time period ΔT , it is reasonable to assume the current is constant. Substituting from (4.1) into (4.4) for the n^{th} module, with a small discharging current gives:

$$I_{batt,n,(0)} = \frac{\Delta Q_{n,(0)}}{\Delta T} = \frac{Q_{max,n,(0)}SOC_{n,(0)}}{N\Delta T} \quad (4.5)$$

A similar expression could be obtained for the charging current,

$$I_{batt,n,0} = \frac{Q_{max,n,(0)}(1-SOC_{n,(0)})}{N\Delta T} \quad (4.6)$$

Due to the fact that we require the charge or discharge time to be the same between the modules, the remaining time $t (=N\Delta T)$ will be same across all the modules. It can be seen that the current needs to be split in proportion to the remaining capacity (Q_{max}) and SOC available at a certain instant.

To calculate the expression for the desired current for a given total power, the converter power balance equation over each sample period, can be used as shown below.

$$P = \sum_{m=1}^n V_{batt,m(0)} I_{batt,m(0)} \quad (4.7)$$

Where n is the number of active modules and each module say m has a different voltage, $V_{batt,m}$ and current $I_{batt,m}$.

Now, substituting (4.6) into (4.7) for each module m discharging, gives:

$$P = \sum_{m=1}^n V_{batt,m(0)} \frac{Q_{max,m(0)} SOC_{m(0)}}{N\Delta T} \quad (4.8)$$

To find, say, $I_{batt,1,0}$ and eliminate $N\Delta T$ from (4.8) which is equal for all modules, substitute for $N\Delta T$ from (4.5):

$$P = \sum_{m=1}^n V_{batt,m(0)} \frac{Q_{max,m(0)} SOC_{m(0)}}{\left(\frac{Q_{max,m(0)} SOC_{m(0)}}{I_{batt,1(0)}} \right)} \quad (4.9)$$

Re-arranging gives:

$$I_{batt,1,0} = P \left(\frac{Q_{max,1(0)} SOC_{1(0)}}{\sum_{m=1}^n V_{batt,m(0)} Q_{max,m(0)} SOC_{m(0)}} \right) \quad (4.10)$$

The desired current for the i^{th} module will therefore be:

$$I_{batt,i,0} = P \left(\frac{Q_{max,i(0)} SOC_{i(0)}}{\sum_{m=1}^n V_{batt,m(0)} Q_{max,m(0)} SOC_{m(0)}} \right) = P \omega_{i(0)} \quad (4.11)$$

A similar expression for charging can be derived:

$$I_{batt,i,0} = P \left(\frac{Q_{max,i(0)}(1 - SOC_{i(0)})}{\sum_{m=1}^n V_{batt,m(0)} Q_{max,m(0)} SOC_{m(0)}} \right) = P \omega_{i(0)} \quad (4.12)$$

Therefore, the desired current sharing of the modular converter can be written for discharging and charging respectively as follows:

$$I_{batt,1(0)}: I_{batt,2(0)}: \dots: I_{batt,n(0)} = Q_{max,1(0)} SOC_{1(0)}: Q_{max,2(0)} SOC_{2(0)}: \dots: Q_{max,n(0)} SOC_{n(0)}$$

$$I_{batt,1(0)}: I_{batt,2(0)}: \dots: I_{batt,n(0)} = Q_{max,1(0)}(1 - SOC_{1(0)}): Q_{max,2(0)}(1 - SOC_{2(0)}): \dots: Q_{max,n(0)}(1 - SOC_{n(0)})$$

After the first time instant the current has discharged the battery and Fig. 4.4 turns to Fig. 4.5. The charge used in the first time step is calculated from the product of SOC and Q_{max} as detailed later. Two different equations have been used to calculate these parameters so avoid cross-coupling.

During the time step from ΔT to $2\Delta T$ the equations can be re-written as follows:

Equation (4.1) becomes

$$\Delta Q_{n,\Delta T} = \frac{Q_{max,n(\Delta T)} SOC_{n(\Delta T)}}{N-1} \quad (4.13)$$

Again over a small sample period, $i_{batt,n,\Delta T}$ can be considered constant and (4.5) becomes (4.14).

$$I_{batt,n(0)} = \frac{Q_{max,n(\Delta T)} SOC_{n(\Delta T)}}{(N-1)\Delta T} \quad (4.14)$$

From the equations (4.7), (4.8) and (4.9) can re-written (eliminating $(N-1)\Delta T$) to give

$$I_{batt,1(\Delta T)} = P \left(\frac{Q_{max,1(\Delta T)} SOC_{1(\Delta T)}}{\sum_{m=1}^n V_{batt,m(\Delta T)} Q_{max,m(\Delta T)} SOC_{m(\Delta T)}} \right) \quad (4.15)$$

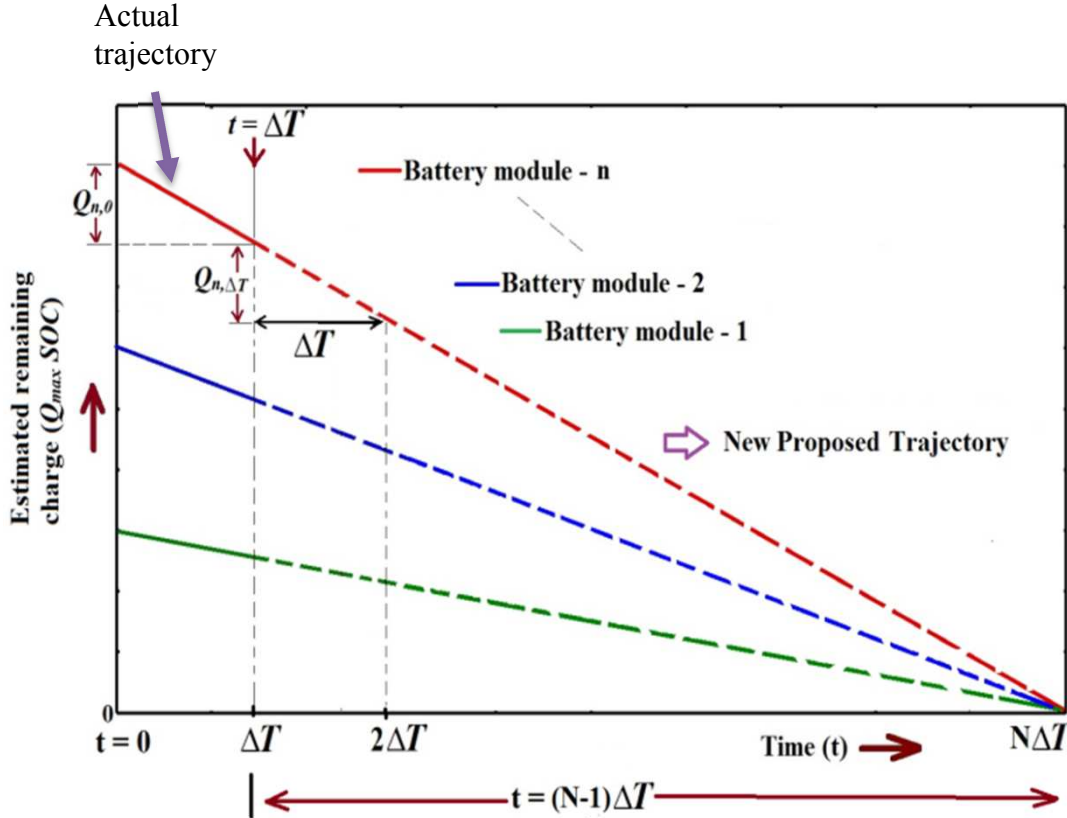


Fig. 4.5 Proposed trajectory during discharging at $t = \Delta T$

It is important to note that the current is in the same format as the first time, but uses the calculated values of Q_{max} and SOC from the start of time. This equation (4.15) can therefore be generalised for each time step to be

$$I_{batt,1(k\Delta T)} = P \left(\frac{Q_{max,1,(k\Delta T)} SOC_{1,(k\Delta T)}}{\sum_{m=1}^n V_{batt,m,(k\Delta T)} Q_{max,m,(k\Delta T)} SOC_{m,(k\Delta T)}} \right) \quad (4.16)$$

Similar expression can be obtained for charging,

$$I_{batt,1(k\Delta T)} = P \left(\frac{Q_{max,1,(k)\Delta T} (1 - SOC_{1,(k)\Delta T})}{\sum_{m=1}^n V_{batt,m,(k\Delta T)} Q_{max,m,(k\Delta T)} (1 - SOC_{m,(k\Delta T)})} \right) \quad (4.17)$$

In the expressions (4.16) and (4.17), k is an integer number which represents the time step. Moreover, the relative magnitude of the module currents is independent of power and individual battery terminal voltages. This means if a module fails, the currents re-distribute between the modules and end up getting fully charged and discharged at the same time. The method works to compensate for battery degradation, because as the battery degrades the estimated $Q_{max,n}$ drops through the calculation and this in turn allows the current at the next time step to reduce or a lower current share is taken.

Now, the module battery $SOC_{n(k\Delta T)}$ is some function $f()$ of its open-circuit voltage $OCV_{n(k\Delta T)}$ within the sample time and $\omega_{i(k\Delta T)}$ is the weighting function over a sample period ΔT and

depends on instantaneous SOC and Q_{max} . It is important that the battery capacity (or Q_{max}) and internal impedance (Z) are tracked during the battery operation because long term battery degradation and/or temperature variation will affect capacity [341]. As a result, the module current will vary throughout the period and the controller has to generate references based on the instantaneous weighting factors which are different in charging and discharging mode.

To determine the SOC and capacity the following method is used step-by-step:

- Estimate the internal impedance using the method described in the 4.4.1 section.
- Estimate the corresponding OCV using the impedance based battery model and using the measured value of V_{batt} , i.e. $OCV = V_{batt} + i_{batt}Z$ (discharging) and $OCV = V_{batt} - i_{batt}Z$ (charging)
- Determine the SOC using an OCV - SOC look-up table or derived function.
- Estimate the capacity using the method described in 4.4.2.

This SOC can be obtained using a look up table or derived function $f(OCV)$. An example curve between SOC and OCV has been shown in where the experimental results for two different battery types are presented. The line of best fit can be taken to simplify the function $f(.)$ [148]. However, more accurate curve fitting (or a look-up table) can also be used to calculate SOC from the OCV.

4.4 Online Battery Parameter Tracking

In second life battery applications, the battery parameters are prone to vary. Among the different parameters, there are two parameters such as, a) internal impedance (Z) and b) battery capacity or maximum charge left (Q_{max}), indicate the battery state-of-health (SOH).

4.4.1 Internal impedance estimation

In second life applications, this parameter tends to go high with time compared to the nominal value. Impedance estimation has been undertaken using EIS techniques, pulse load test methods etc. previously [353] – [355], [311] when a battery is stationary (disconnected from a power circuit). These tests use external excitation signals (such as pulse current or high frequency AC signal) to measure the impedance without involving a power converter. Therefore, these are difficult to apply during the grid-tie energy storage system operation. To overcome this shortfall, this work uses a high frequency converter ripple based online impedance estimation method similar to [359]. The principle concept is to use the high frequency inductor ripple current of the associated dc-dc converter and corresponding to high frequency ripple of the battery terminal voltage to calculate the internal impedance. The switching frequency is in kHz, so it can be assumed that the SOC does not change significantly during this small switching interval. This means OCV can also be considered constant within that interval. Therefore, two different equations can be written, a) at $t = 0$ and b) at $t = dT_s$ as shown in (4.22) and (4.23). The internal impedance can be calculated using

(4.24). The ripple components of battery current and voltage can be extracted from the measured current and the voltage using a LPF (low pass filter) with a cut-off frequency $1/10^{\text{th}}$ of the switching frequency as shown in Fig. 4.6. After extracting the ripple part of voltage and current, the magnitude impedance can be calculated.

$$V_{batt_{max/min}} = OCV \pm i_{batt_{min/max}}Z \text{ at } t = 0 \quad (4.22)$$

$$V_{batt_{min/max}} = OCV \pm i_{batt_{max/min}}Z \text{ at } t = dT_s \quad (4.23)$$

$$Z = \frac{|(V_{batt_{max}} - V_{batt_{min}})|}{|(i_{batt_{max}} - i_{batt_{min}})|} = \frac{|\Delta V_{batt}|}{|\Delta i_{batt}|} \quad (4.24)$$

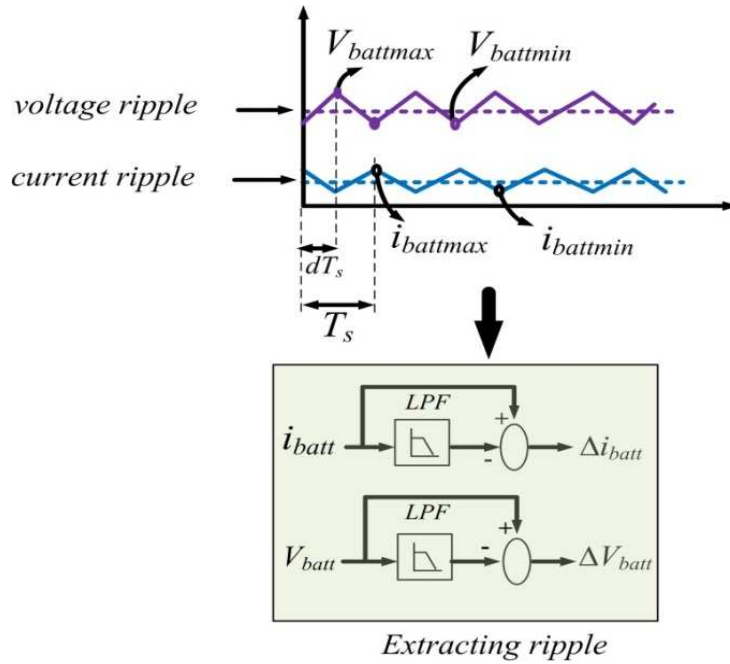


Fig. 4.6 Ripple based impedance estimation

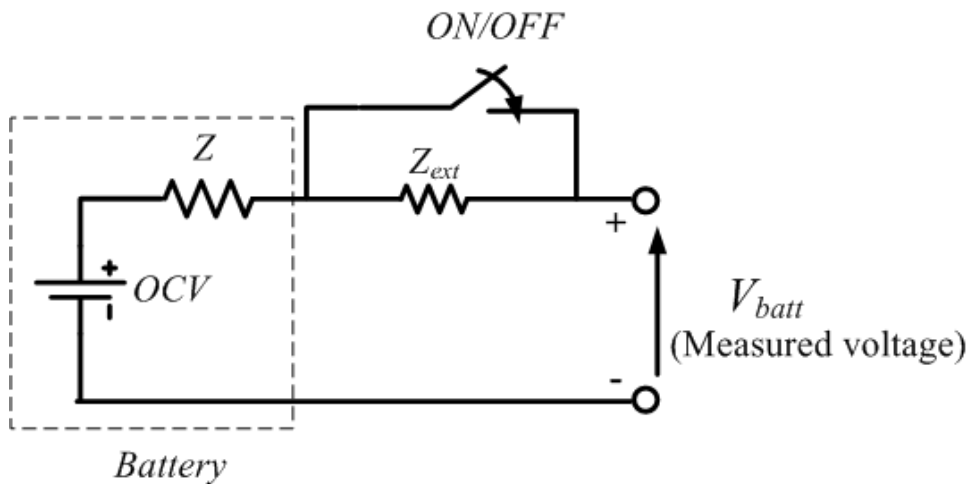


Fig. 4.7 Validation of ripple based impedance estimation method using external impedance

It is important to note that this voltage and current ripple are always present when the converter runs and therefore, this method can detect any change in internal impedance online. The battery terminal voltage ripple always shows a change with impedance variation

(because of the battery IR drop). Even though the method is designed assuming only the ohmic part or dc-impedance of the total battery impedance, but it is capable of detecting the total impedance of the battery.

In order to experimentally validate the proposed method an external resistance Z_{ext} has been put through an ON/OFF dc-breaker as shown in Fig. 4.7. Therefore, the battery terminal voltage sees $(Z + Z_{ext})$ when the breaker is OFF and only Z when the breaker is ON. The Fig. 4.8 shows the experimental results of using a 24V battery with $Z_{ext} = 0.033\Omega$ in series with the battery. It can be seen that the voltage ripple shows a sudden change when the impedance varies and this change is used to estimate the impedance. The speed of tracking or estimation depends on the bandwidth of the LPF. In this case, a bandwidth of 100Hz is used. The sensing should be accurate when using this method. Note the accuracy of this method reduces with the increase of switching frequency because of the measurement accuracy because it is difficult to sense very high frequency signals through the voltage and current sensors unless specifically designed to. It is assumed that the measurements (V_{batt} and i_{batt}) at the switching frequency (here it is 5 – 10 kHz) are accurate through the sensors due to high bandwidth (= 50 KHz) sensors. Therefore, the switching frequency has to be limited when using such method. However, this limitation is not a serious drawback in high power applications (e.g. > 10kW) because: a) the switching frequency is usually limited because of high switching losses, and b) the magnitude of voltage and current ripple is high which can be sensed with a reasonable accuracy.

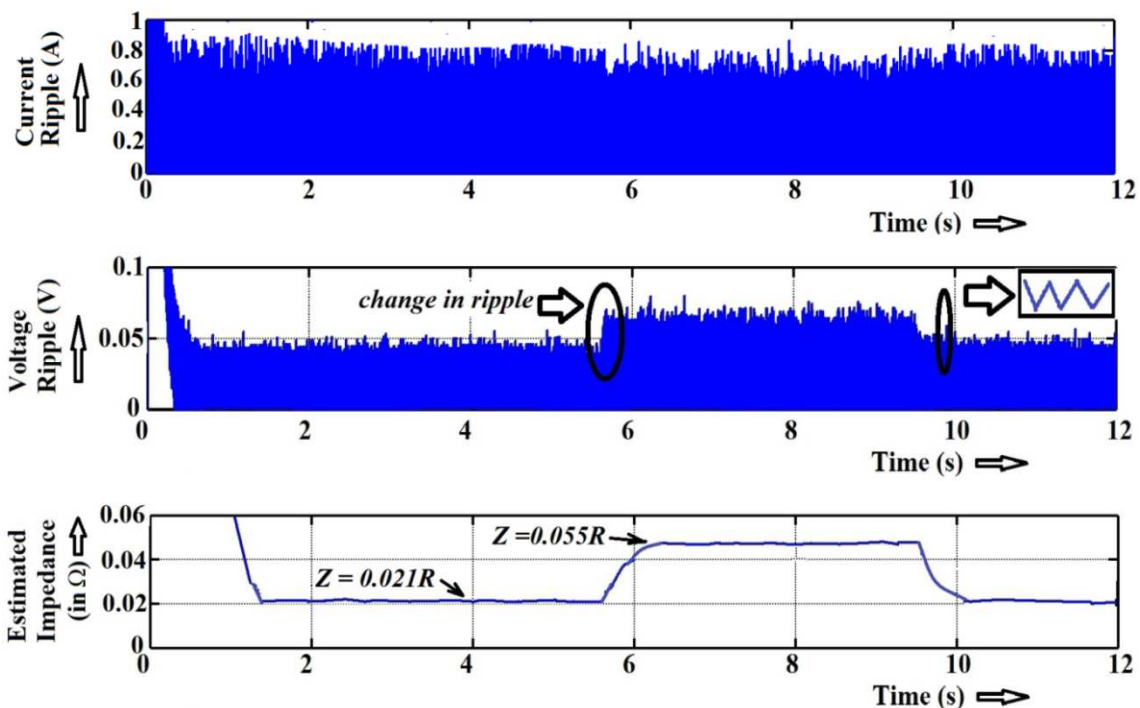


Fig. 4.8 Experimental validation of impedance estimation method for 24V battery ($Z_{nom} = 0.02\Omega$) at 10 kHz switching frequency: a) measured current ripple, b) measured voltage ripple, c) estimated impedance

4.4.2 Capacity or charge estimation

In the second life battery application, the capacity or the maximum charge left in a battery

can also vary during operation. The initial capacity has to be known but it is necessary to track the Q_{max} for the power sharing strategy. The method adopted in this paper is similar to that in [343] where the SOC-capacity coulomb counting equation is used to estimate the capacity when the SOC is obtained from a SOC-OCV look-up table. The method is explained in steps:

- Find corresponding SOC Vs OCV look-up table or a derived function as explained in section 4.3
- After obtaining SOC from the above, the capacity (or maximum charge left) can be found using (4.25) which is essentially a coulomb counting equation.

$$Q_{max} = \left| \frac{\int_0^t i_{batt} dt}{SOC(0) - SOC(t)} \right| \quad (4.25)$$

In order to validate this method, two identical batteries with equal voltage (12V) and equal capacity (10Ah) have been put in parallel through a dc-breaker as shown in Fig. 4.9. As a result the combination behaves as 12V, 20Ah battery. Mid-way through the discharging experiment one battery has been disconnected to emulate the change in capacity. Fig. 4.10 shows the validation of the capacity estimation process when two 10Ah batteries are put in parallel at a constant current (here it is 5A). It can be seen that the process can able to detect the battery capacity. In order to show the adaptability of this method, suddenly one of the battery modules was taken out to reduce the overall capacity. i_{batt} is the overall current which is monitored as shown in Fig. 4.9. It can be seen that the process is capable of tracking such variation approximately. The error in the estimation process is mainly due to SOC estimation process and current measurement process. This can be improved if more accurate estimation and measurement process are employed.

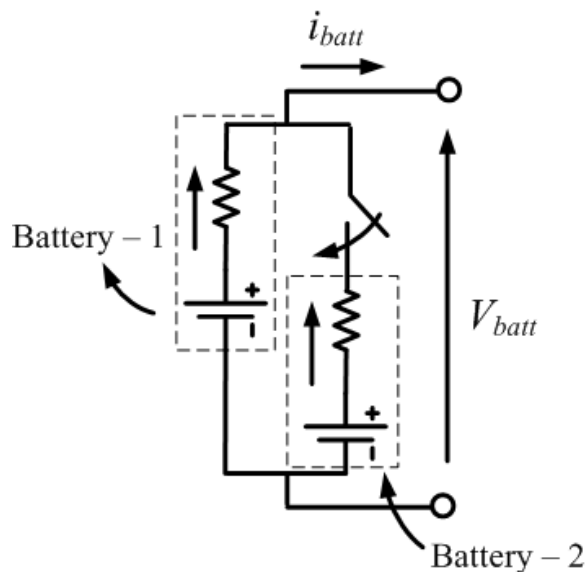


Fig. 4.9 Validation of capacity estimation method using two identical batteries in parallel

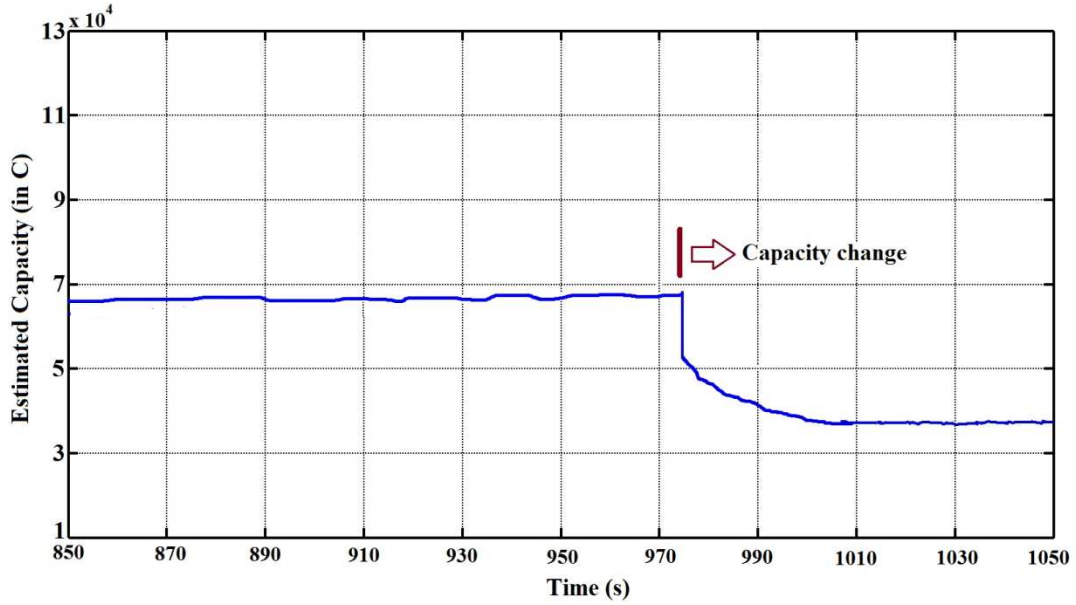


Fig. 4.10 Experimental validation of capacity estimation process using two 12V, 10Ah batteries and dynamic change in capacity

4.5 Modelling and validation

In order to validate the proposed power sharing strategy with the hybrid batteries, a simulation study and then subsequent experimental studies have been presented. The modelling is composed of two stages: a) modelling of batteries, b) modelling of the modular dc-dc converter and c) modelling of the line side inverter.

4.5.1 Battery modelling

Due to the linear OCV-SOC assumption, a battery module can be modelled as a high capacitance with small series resistance where the voltage across capacitance will increase or decrease depending on the current flowing through it. Therefore, the model can be expressed by following equations (4.26) – (4.28). The $OCV_{0,i}$ is the initial capacitor voltage which represents battery open circuit voltage and C_{batt} is the equivalent battery capacitance. Fig. 4.11 shows the Matlab/Simulink battery model using (4.26) – (4.28) which uses a dependent voltage source with a series resistance to model a battery.

$$OCV_i = OCV_{0,i} \pm \frac{1}{C_{batt}} \int i_{batt,i} dt \quad (4.26)$$

$$C_{batt} = \frac{Q_{max,i}}{OCV_{max,i} - OCV_{min,i}} \quad (4.27)$$

$$OCV_i = V_{batt,i} \pm i_{batt,i} Z_i \quad (4.28)$$

4.5.2 Modelling of estimation

Fig. 4.12 shows the Matlab/Simulink model of the battery capacity estimation process. The SOC and integration of current have been used to estimate the capacity during the online operation as described in section 4.4.2. On the other hand, the internal impedance estimation process is shown in Fig. 4.13. The ripple extraction and impedance estimation have been

shown separately for a three-module system.

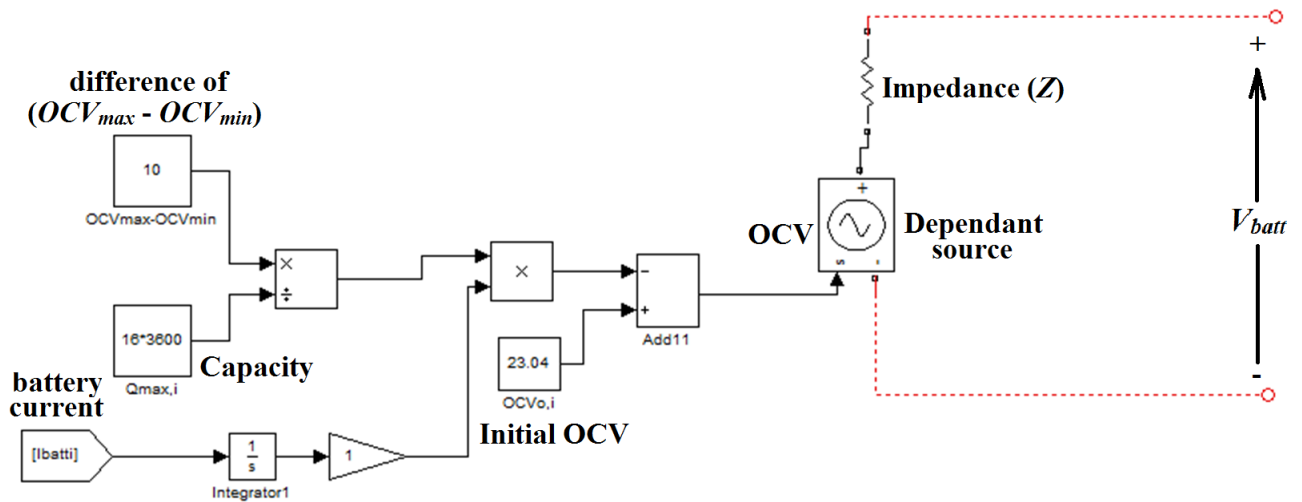


Fig. 4.11 Battery Model in Matlab/Simulink during discharging

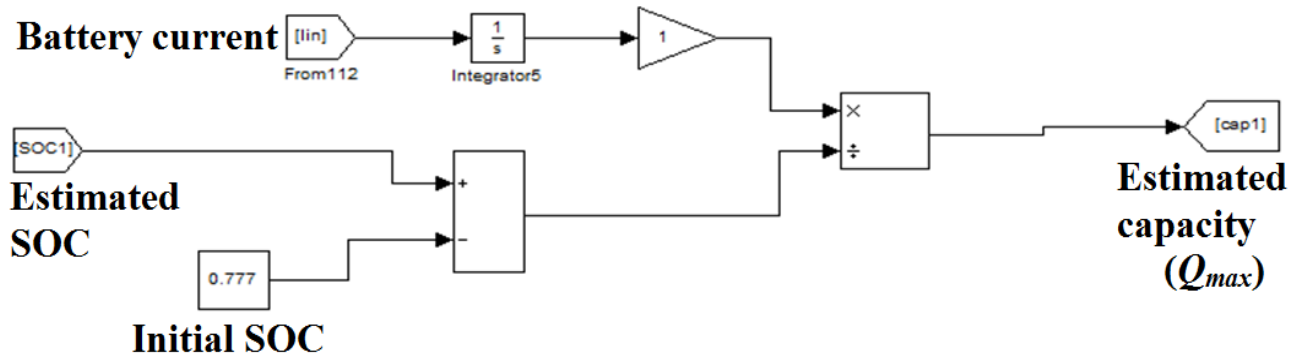


Fig. 4.12 Matlab/Simulink model for the online capacity estimation

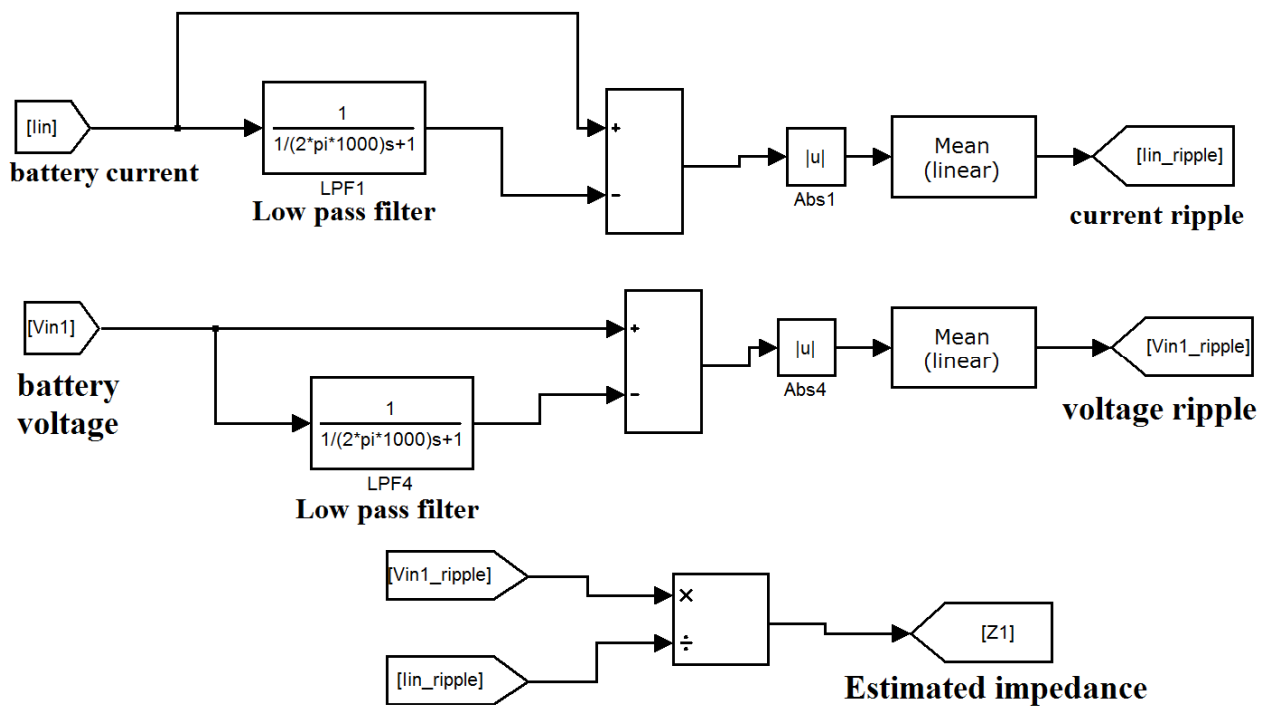


Fig. 4.13 Matlab/Simulink model for the online impedance estimation

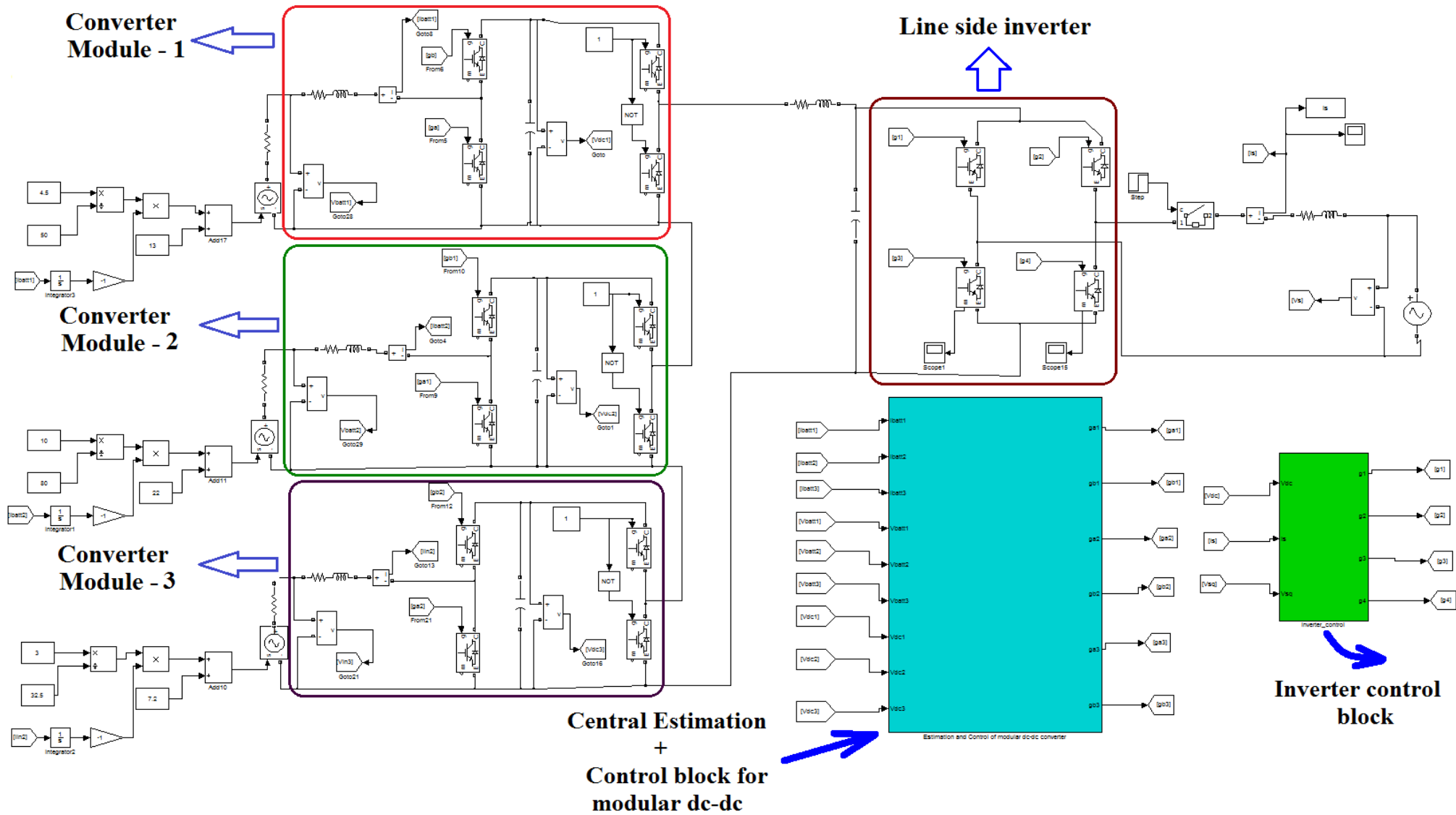


Fig. 4.14 Overall Matlab/Simulink model of the bi-directional hybrid battery energy storage system

4.5.3 Modelling of modular dc-dc converter and inverter

One of the stages of the proposed energy storage system is the converter modelling. The overall converter structure consists of: a) modular dc-dc converter and b) line side inverter. The modular dc-dc converter consists of three converter modules. Each module is essentially an H-bridge as described in earlier chapters. The Matlab/Simulink model is shown in Fig. 4.14. The battery model in each converter module is same as in Fig. 4.11. It can be seen that the three modules are in cascaded in form the central dc-link of the inverter. The proposed power sharing is implemented in the central control and estimation block shown in the figure. There is a separate control block for the line side inverter. The inverter is controlled to meet a certain grid side power demand. The modular dc-dc converter is controlled in such a way that the current is drawn from the individual module in appropriate proportion. The detailed description of the control system and associated control architecture will be presented in later chapters.

Table 4-1 Component specifications used in simulation and/or experimental validation

Type/Name	Rating/specification	Sim/Exp
LV Trench MOSFET for H-bridge dc-dc modules	100V 40A – $R_{ds(on)}=6\text{m}\Omega$, $t_{on} + t_{off}=75\text{ns}$ (FDPF085N10A)	Exp
Field Stop IGBT for inverter	$V_{CE(sat)} = 2.2\text{V}$, $E_{on} + E_{off} = 0.53\text{mJ}$	Exp
Boost inductors of dc-dc modules	1.5mH, 15A, $R_L = 20\text{m}\Omega$	Sim+Exp
dc-link capacitor in each module	2700 μF , 100V	Sim+Exp
dc-link capacitor for inverter	1200 μF , 400V	Sim+Exp
Total line side inductance	3mH, 15A	Sim+Exp
Line side capacitor	10 μF	Sim+Exp
Switching frequency of the dc-dc modules	10kHz	Sim+Exp
Switching frequency of inverter	10kHz	Sim+Exp
Operating central dc-bus voltage	150V	Sim+Exp
Nominal grid voltage	120V (peak)	Sim+Exp
Grid current	7.5A (peak)	Sim+Exp
Battery module -1	12V, 10Ah lead acid – $V_{max} = 14\text{V}$ $V_{min} = 9.6\text{V}$, $Z_{nom} = 0.015\Omega$	Sim+Exp
Battery module -2	24V, 16Ah lead acid – $V_{max} = 29\text{V}$ $V_{min} = 19\text{V}$, $Z_{nom} = 0.02\Omega$	Sim+Exp
Battery module -3	7.2V, 6.5Ah NiMH – $V_{max} = 8.5\text{V}$ $V_{min} = 5.5\text{V}$, $Z_{nom} = 0.011\Omega$	Sim+Exp

4.5.4 Validation in grid connected mode under normal operation

In order to validate the proposed strategy, a hybrid battery configuration was chosen based on the available set of batteries. The parameters used in simulation and experimental study are shown in Table 4-1. The distributed sharing strategy and its effect on charging/discharging trajectory is validated for a fixed power reference (450W) on the grid side. The overall validation is undertaken in two steps; part A validates the control system implementation of the strategy under transient conditions. Part B validates the long term distributed strategy and its effect on actual charge/discharge trajectory. This chapter presents only the key results of the transient power sharing and a detailed charging and discharging trajectory to validate the theory developed in 4.3. The later chapters provide more additional validation of transient distributed sharing strategy along with the full control system description.

The experiment and simulation was run over two complete cycles to validate the charging/discharging trajectory. All the modules were started at widely different initial SOC and voltage levels at the start of the tests. Fig. 4.15 and Fig. 4.16 show the current distribution at the moment of connecting to the grid. The estimated instantaneous state-of-charge (SOC) is plotted with time to validate the full charging and discharging trajectory. The simulation and experimental results of charging and discharging trajectories are shown on the same scale for easy comparison. Fig. 4.17 and Fig. 4.18 show the simulation (solid line) and experimental (dotted points) results for discharging and charging respectively. It can be seen that a module with a lower initial SOC has a larger slope compared to higher initial SOC during charging and vice-versa during discharging. In this way, all the modules stay together while providing the necessary grid support and reach their fully charged or discharged state at approximately the same time in the both simulation and experiments. Experimental results show a sudden voltage change at the start of operation and some mismatch at the end of the cycle compared to simulation. This is due to the assumption in the modelling and weighting function calculation that the SOC is linearly related to open circuit voltage. Other differences between the simulation and experiment could be due to the error in estimation of the exact battery capacity and the difficulty of measuring the battery parameters.

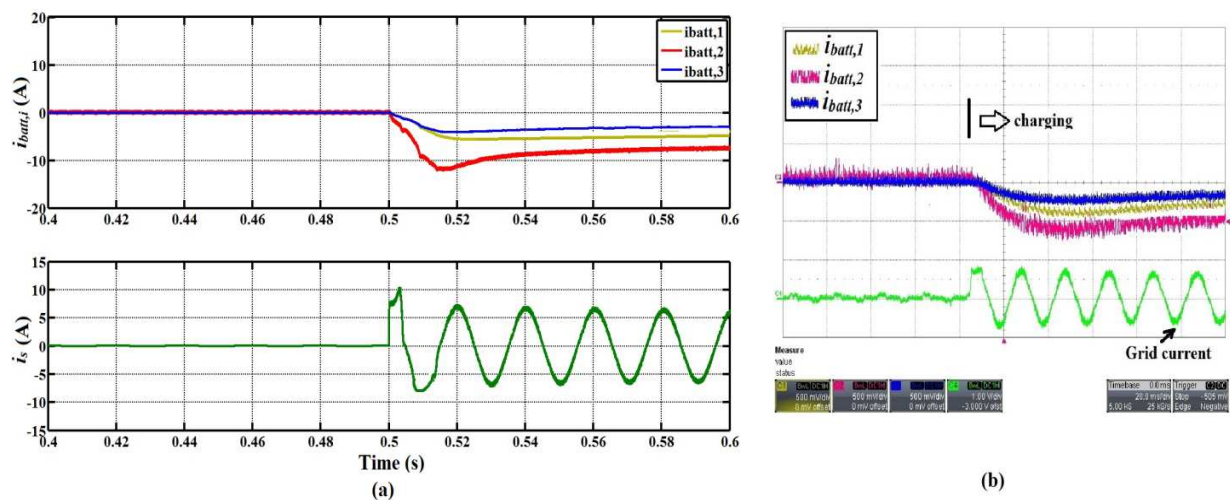


Fig. 4.15 Current sharing while connecting to grid during charging: a) simulation, b) experimental results

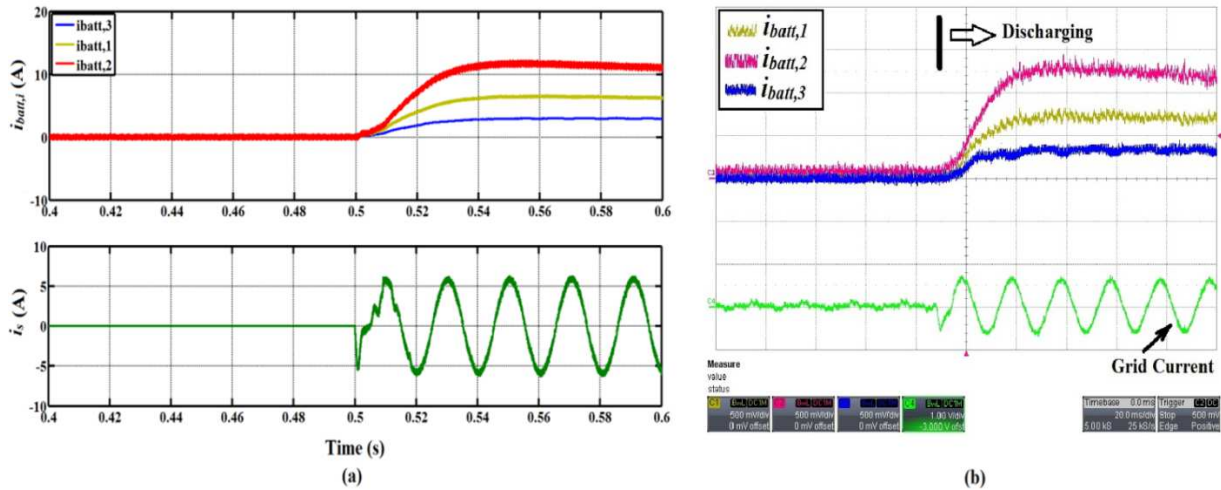


Fig. 4.16 Current sharing while connecting to grid during discharging: a) simulation, b) experimental results

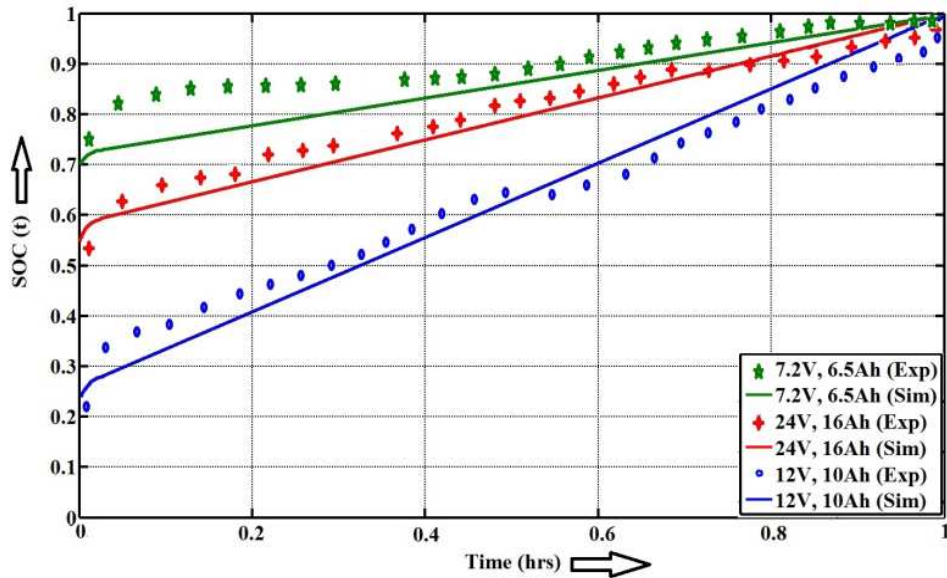


Fig. 4.17 Simulated and experimental charging trajectory using the distributed power sharing strategy

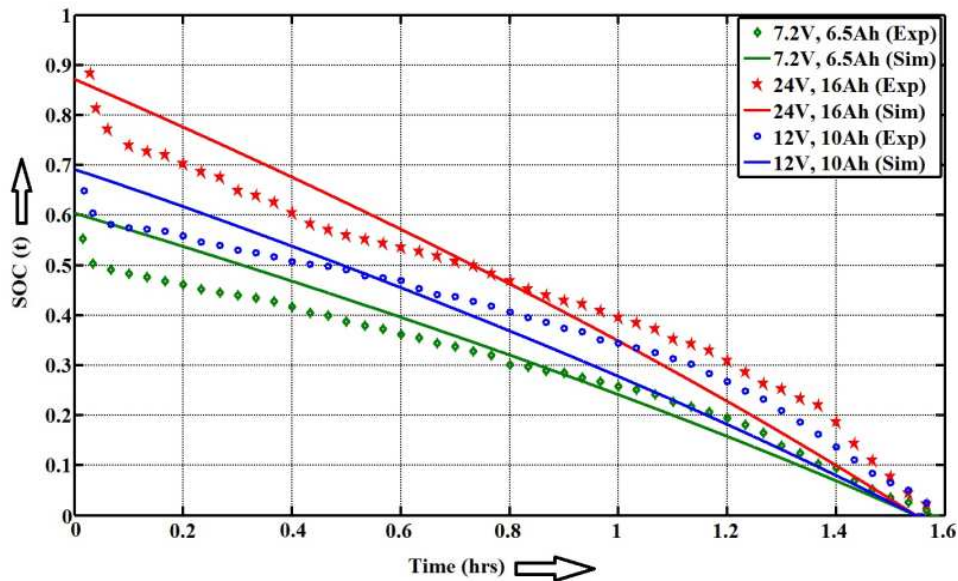


Fig. 4.18 Simulated and experimental discharging trajectory using the distributed power sharing strategy

4.5.5 Validation in grid connected mode under abnormal conditions

In second life applications, a battery module can fail at any time. Therefore, it is necessary to investigate the effect of the proposed sharing strategy on the remaining modules when a module fails and is bypassed. The module bypassing is done by turning on T_{ii} and turning off T_i in the converter as explained in the chapter 3. In order to demonstrate the effect of module bypassing, module – 3 (7.2V module) has been bypassed both in the simulation and in experiments. The transient result is shown in Fig. 4.19 and Fig. 4.20. Note: the remaining modules take a higher share of the current to maintain the same power output. Module – 3 current slightly goes to negative value during the discharging mode and slightly above zero during the charging mode before it settles down to zero because of changing the corresponding module voltage references during module bypassing. The description of this control will be presented in chapter – 5. The effect of the module bypass on the discharging and charging trajectory is shown in Fig. 4.21 and Fig. 4.22. The simulation and experimental results have been plotted in same scale. The key point to note is that the current in the remaining modules adjusts in proportion to the power required as explained in section 4.3 and the batteries end up fully charged/discharged at around the same time. This shows the proposed strategy is fault-tolerant in nature and remains valid even when one module fails.

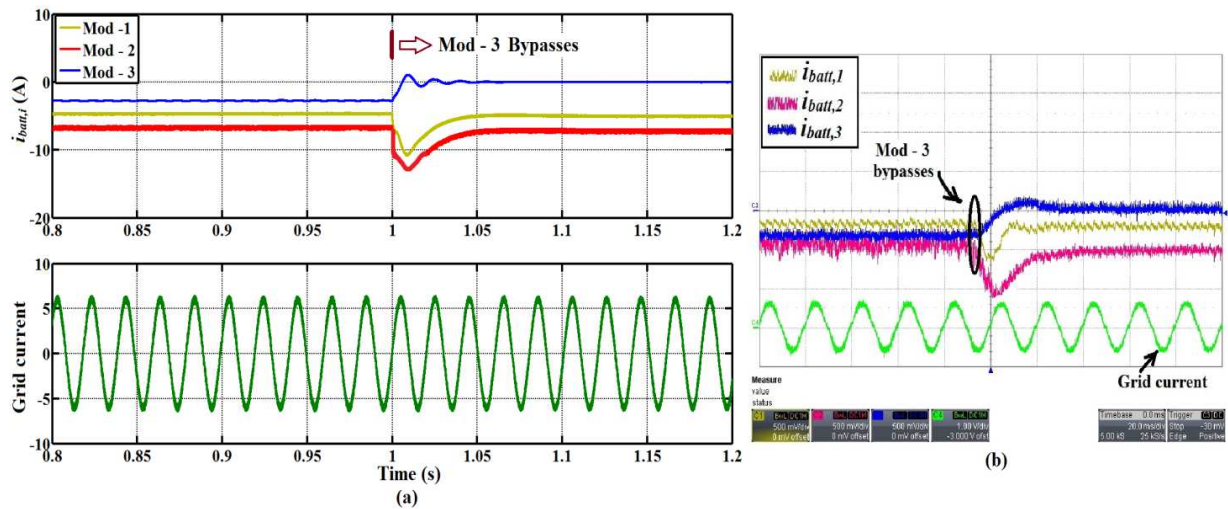


Fig. 4.19 Distributed sharing under module bypassing in charging mode: a) simulation, b) experimental

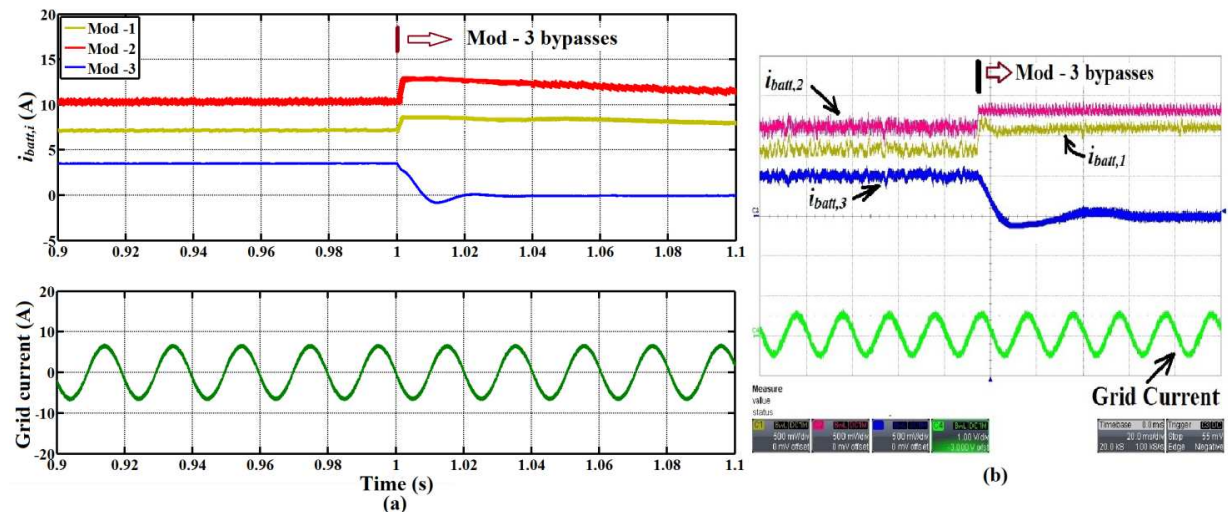


Fig. 4.20 Distributed sharing under module bypassing in discharging: a) simulation, b) experimental

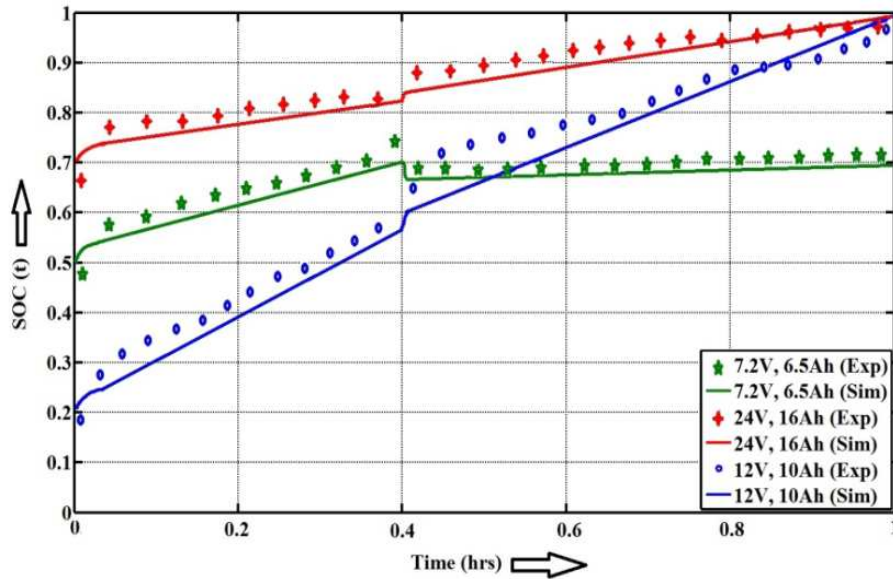


Fig. 4.21 Simulated and experimental charging trajectory of the hybrid batteries: module bypassing

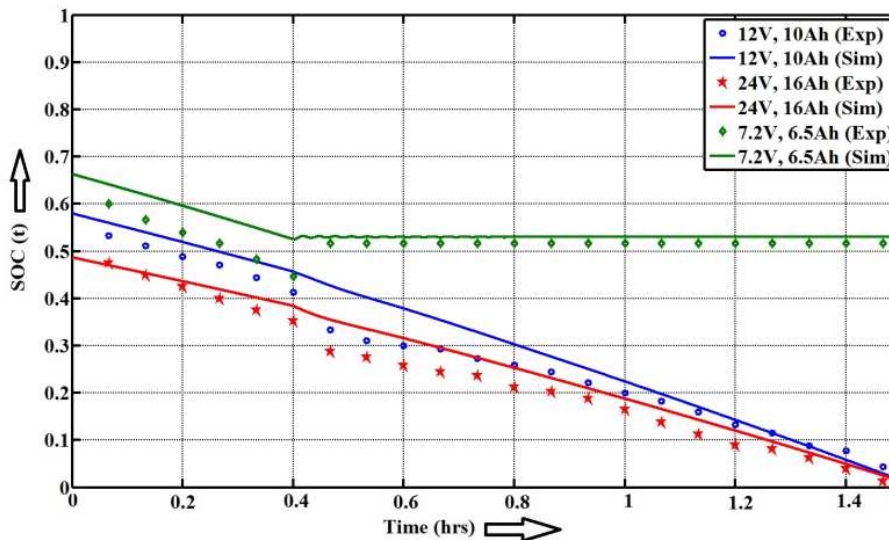


Fig. 4.22 Simulated and experimental discharging trajectory of the hybrid batteries: module bypassing

4.5.6 Validation under parameter variation

Parameter variation is an important phenomenon in second life battery application. Among the different parameters there are two parameters: a) maximum charge or capacity (Q_{max}) and b) internal impedance (Z) that are likely to vary with time due to degradation. In the case of batteries, Q_{max} is related to Z [341] in this way an increment of Z reduces Q_{max} . The exact relationship is very much dependent on the battery chemistry and it is difficult to find an explicit mathematical expression between these two. Moreover, previous research show that Q_{max} represents an indicative to state-of-health (SOH) of a battery as it tends to change with the usage e.g. reported in [360]. Therefore, it is assumed that if the variation of capacity and impedance is tracked online and considered in the sharing strategy, the variation of state-of-health is automatically incorporated in the analysis.

Online capacity and impedance variation: In order to demonstrate the variation of capacity

and impedance on the charging and discharging trajectory, two 12V 10Ah batteries were put in parallel to achieve approximately 20Ah effective capacity and suddenly one of the battery module was switched out during operation to reduce the overall capacity to nearly 10Ah. This variation affects Q_{max} and Z and changes the weighting factor according to (4.16) and (4.17). This change in the weighting factor adjusts the current share of the individual modules. The transient variation of current sharing is shown in Fig. 4.23 for the discharging and Fig. 4.24 for the charging respectively. The full charging and discharging trajectories are shown in Fig. 4.25 and Fig. 4.26. It can be seen that the charging and discharging slopes change slightly at the point of parameter variation because of the changes in current distributions. Note: the batteries end up with maximum and minimum points around at the same time both in simulation and experiments. A good correlation has been found between the simulation and the experiments and any difference between simulation and experimental result is likely to be related to the accuracy of the measurement and estimation process.

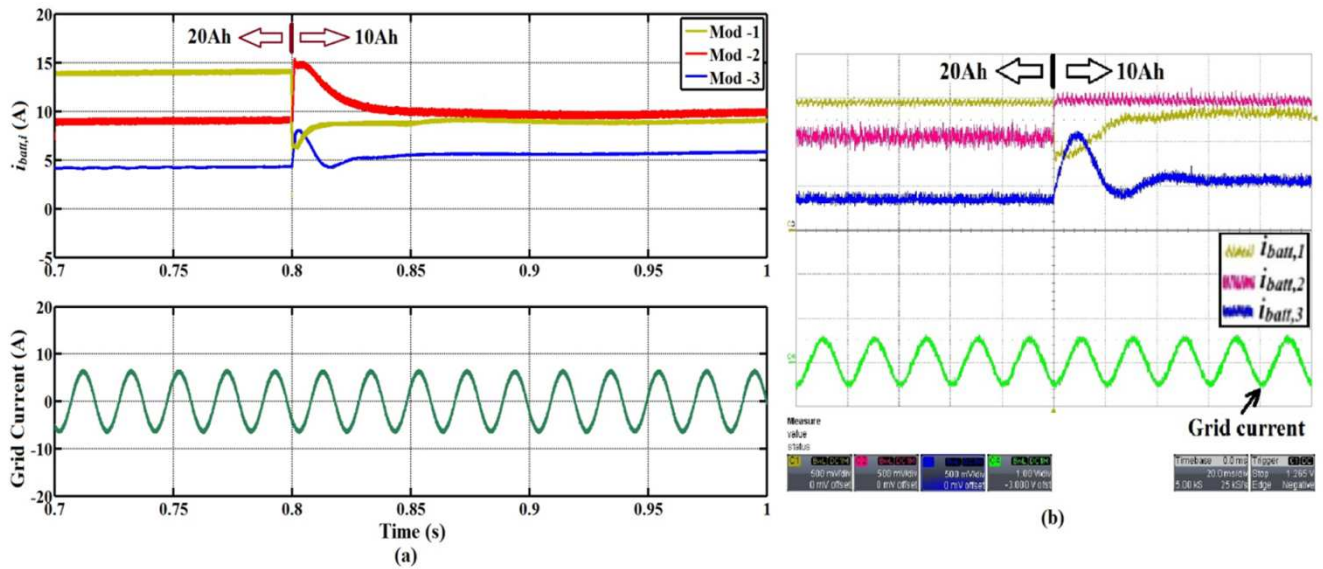


Fig. 4.23 Power sharing under capacity fade during discharging: a) simulated, b) experimental result

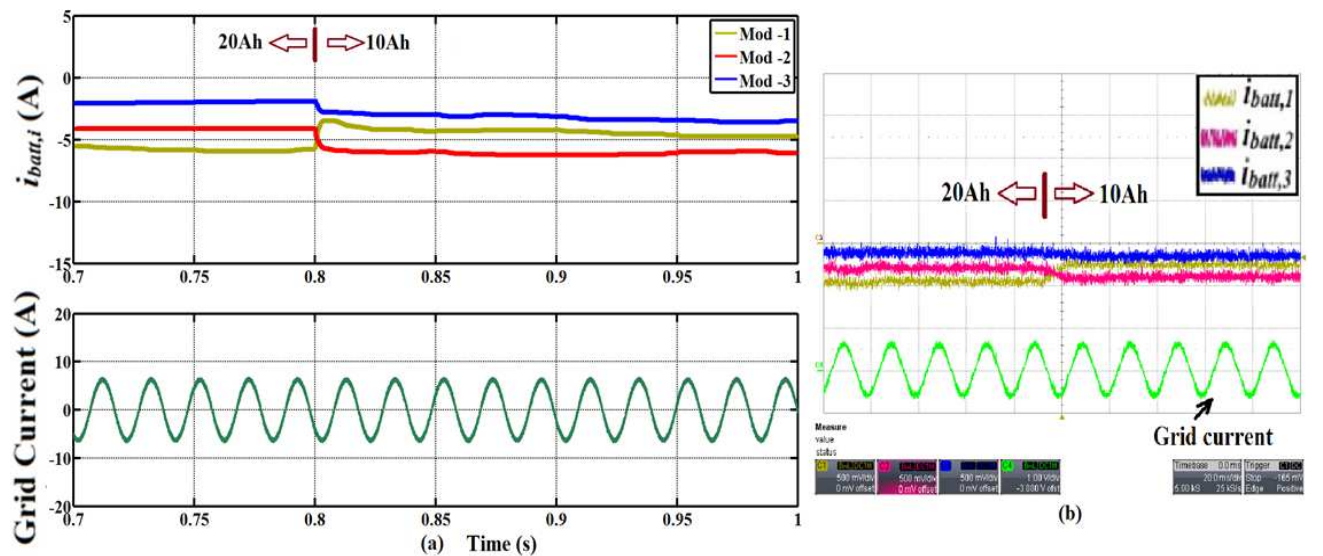


Fig. 4.24 Power sharing under capacity fade during charging: a) simulated, b) experimental result

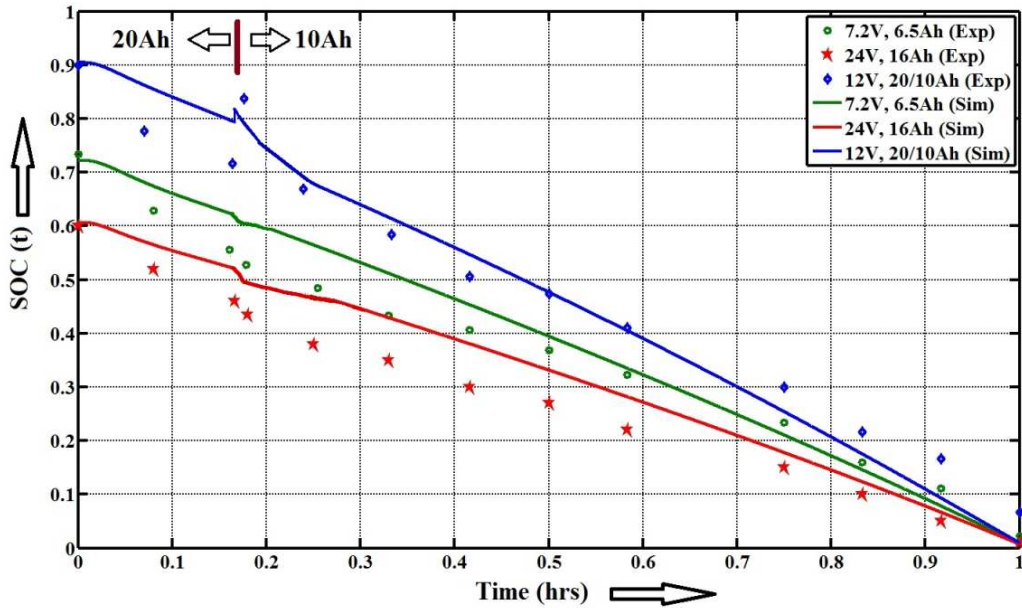


Fig. 4.25 Discharging trajectory under capacity fade: a) simulation, b) experimental result

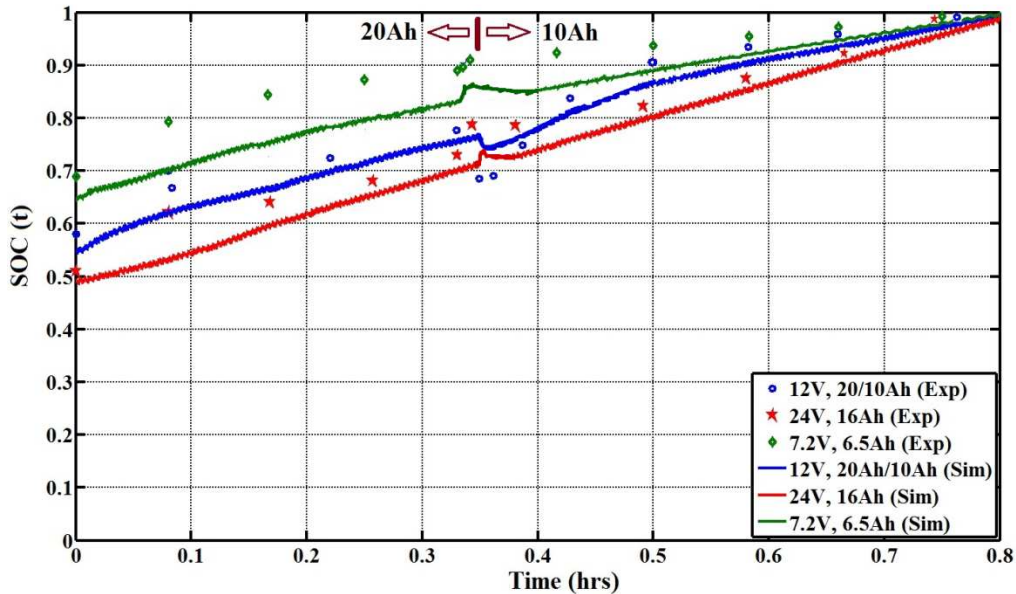


Fig. 4.26 Charging trajectory under capacity fade: a) simulation, b) experimental result

4.5.7 Validation with sudden power change

The grid side power seldom remains constant in real grid system because many times the energy storage is employed to smooth out the power oscillation or demand. Therefore, an ESS may require providing power in small intervals. Therefore, it is necessary to cross-check the applicability of the proposed concept under a sudden change in power. Simulation studies have been undertaken to see the effect of a sudden step change in power on the charging and discharging trajectory. Fig. 4.27 and Fig. 4.28 show the validation of distributed strategy with a sudden change in total power demand during discharging and charging respectively. A step change from 250W to 500W step has been applied through the side inverter to perform that. It can be seen from Fig. 4.27 and Fig. 4.28 that charging and discharging trajectory show a sudden change in slope and all the modules reach their respective maximum or minimum points at the same time. This validates the concept in variable power conditions also.

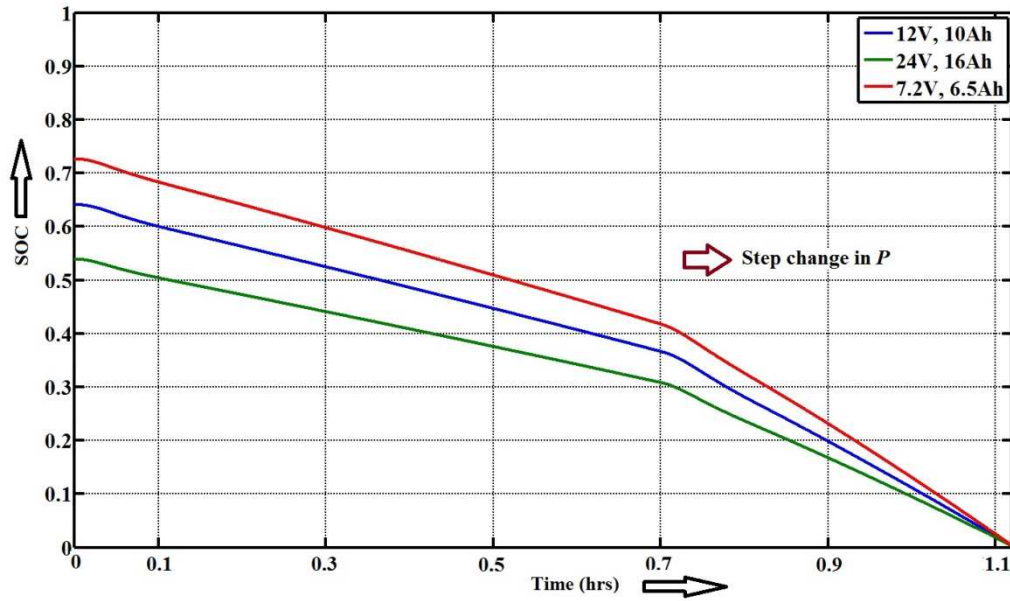


Fig. 4.27 Simulated discharging trajectory with a step change in power

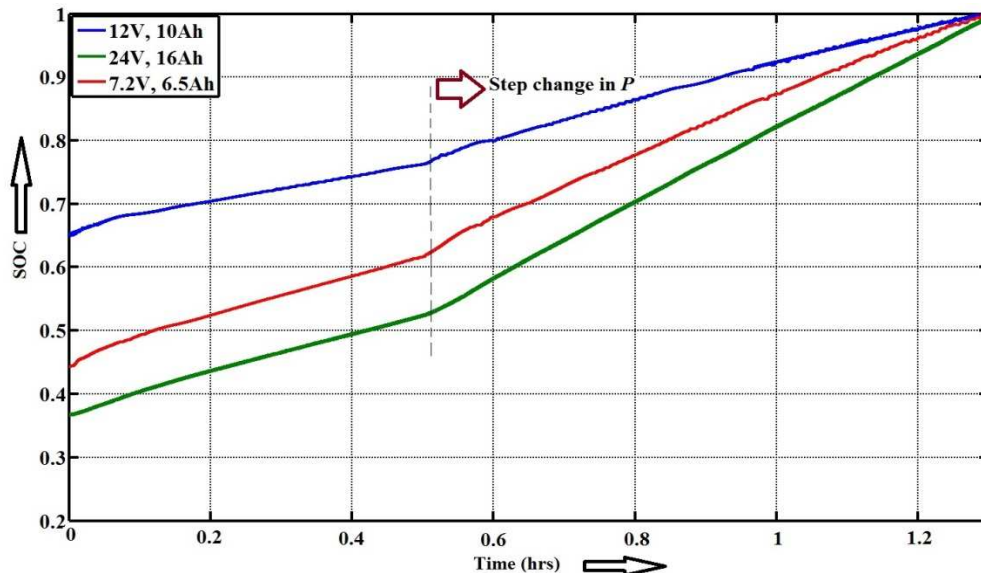


Fig. 4.28 Simulated charging trajectory with a step change in power

4.6 Conclusion

A generalised distributed power sharing strategy has been proposed to integrate hybrid second life batteries to the grid system. The proposed power sharing is based on a weighting factor which is found to be suitable for any set of batteries with widely different characteristics. The distribution strategy aims to make the charging/discharging trajectory of the hybrid battery modules reach their respective maximum/minimum points at the same time. In this way, all the modules stay in operation unless under a fault is detected, so that each battery module is undertaking a proportionate share of the contribution relative characteristics and SOH.

The proposed strategy is adaptive in nature and is capable of detecting parameter variation online such as, capacity fade, impedance increase and acts to change the current share of the respective module. Moreover, the strategy is capable of bypassing a faulty battery module

when necessary without interrupting the overall energy storage operations. The results show the effectiveness of the proposed scheme. A detailed simulation/modeling and experimental study have been presented to validate the proposed claim both in normal and abnormal conditions such as, module bypassing, capacity fade. It found through the simulation and experimental studies that the strategy is fully adaptive in nature and remains valid under all practical conditions considered.

5 Distributed Control Architecture

5.1 Introduction

In the second life hybrid battery energy storage application, it is necessary to deal with each battery module in an independent fashion according to their state-of-health (SOH) and state-of-charge (SOC) while providing the necessary grid support. To perform this, the previous chapter has suggested a weighting factor based strategy to utilise any set of hybrid batteries according to their module characteristics. This weighting factor indicates the *goodness* or *badness* of a battery module on an instantaneous basis. This chapter presents suitable distributed control structure of the modular converter which enables to control of each converter module to be undertaken independently according to the desired weighting factors while providing uninterrupted grid support.

The closed loop control of a modular energy storage systems has been previously undertaken using a single type of battery or super-capacitors with equal modules in terms of voltage, capacity etc. Equalization and balancing control among the modules has been considered to be relevant, for example, to balance the SOC/voltage among the modules using a modular dc-ac converter [155] or modular dc-dc converters [361]. The main concept of these researches was to control/distribute the total voltage (modular dc-dc converter) or total modulation index (modular dc-ac) equally among the converter modules. Therefore, those were termed as balancing/equilisation control. This type of module balancing control is justifiable when similar energy sources are integrated. However, a mix of widely different modules could be present in the second life applications where such strategy is not directly applicable. Therefore, independent module control according to individual battery parameters within the modular converter is an important function in this application. This is termed as a distributed control of the modular converter.

Closely related work was previously undertaken, relates to distributed MPPT control of cascaded dc-dc converter based PV systems where each dc-dc module performs MPPT depending solely on radiation conditions and the line side inverter maintains the central dc-link voltage [339], [362]. The power injected into the grid is solely decided by the PV-modules. The drawbacks of this strategy are: a) bidirectional power cannot be handled when the module converters on the dc-side are in cascaded/series because of module capacitor voltage imbalance problem, b) line side inverter cannot respond to meet the line side load demand or cannot actively participate in energy management which can cause overall slow dynamic response on the grid side. Due to these reasons such a strategy is not useful for SLBESS applications in the smart grid where a bidirectional control structure and line side inverter control according to the grid side power demand are necessary. Therefore, a new control structure is desired.

This chapter proposes different bidirectional distributed control strategies using the cascaded dc-side modular converter and the line side inverter considering charging and

discharging separately.

5.2 Modelling of different control modes

The proposed converter in Fig. 5.1 is capable of operating in every control modes such as boost, buck or boost-buck to meet all current and voltage requirements as described in chapter – 3. Each control mode uses different switching strategies. Therefore, separate control structures are investigated and compared.

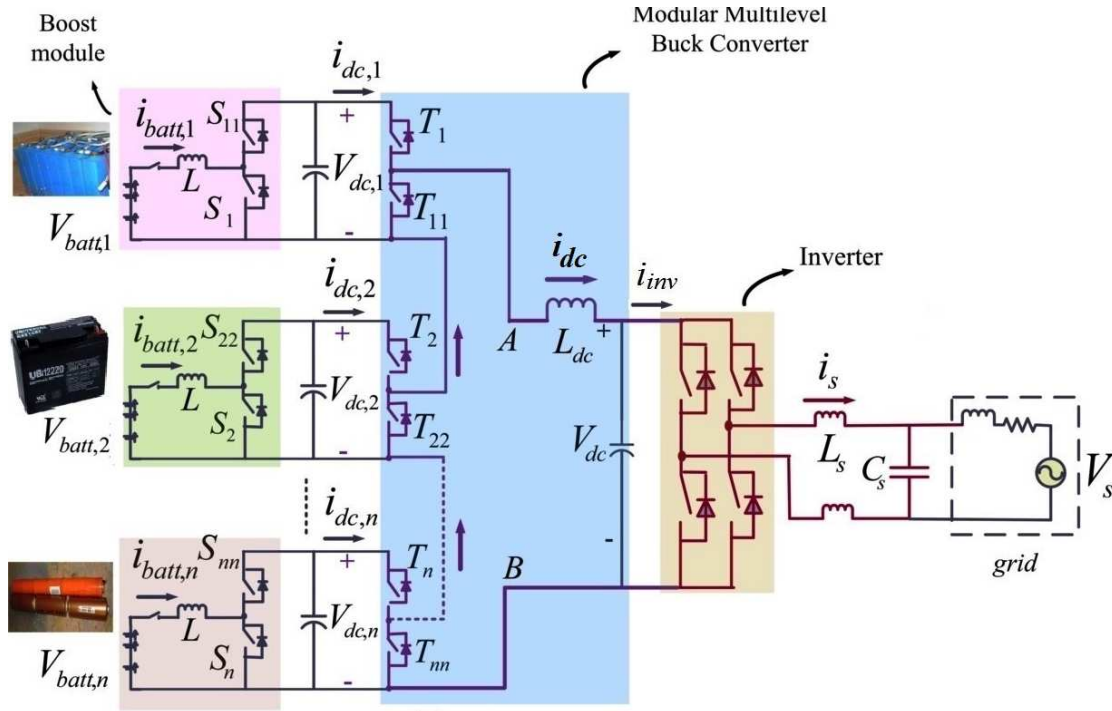


Fig. 5.1 Considered converter topology for hybrid second life batteries

5.3 Modelling in boost mode

The dynamic equations of the converter can be written on a module-by-module basis using of Fig. 5.1 in (5.1) – (5.3) (T_i ON and T_{ii} is OFF).

Module current dynamics:

$$L \frac{di_{batt,i}}{dt} + Ri_{batt,i} + (1 - d_i)V_{dc,i} = V_{batt,i} \quad \forall i = 1 \dots n \quad (5.1)$$

Module voltage dynamics:

$$C \frac{dV_{dc,i}}{dt} - (1 - d_i)i_{batt,i} = -I_{dc} \quad \forall i = 1 \dots n \quad (5.2)$$

Total dc-link voltage:

$$V_{dc} = V_{dc,1} + V_{dc,2} + \dots + V_{dc,n} \quad (5.3)$$

The power balance equations of the modules are given in (5.4) where η_1, η_2 etc. are the efficiencies of the dc-dc modules. In this case, these efficiencies are very high (≈ 1) because of the efficient LV MOSFET can be used in the cascaded converter. It is also to be noted that for a constant V_{dc} and grid power, I_{dc} also remains constant. Therefore, the module capacitor voltages, $V_{dc,i}$ is proportional to the module power ($V_{batt,i} i_{batt,i}$).

$$V_{dc,i} I_{dc} = \eta_i V_{batt,i} i_{batt,i} \quad \forall i = 1 \dots n \quad (5.4)$$

The overall power balance equation is given by (5.5) which relates the grid voltage and central dc-bus voltage where η_{inv} stands for the inverter efficiency.

$$V_{dc} I_{dc} = \eta_{inv} V_s I_s \cong V_s I_s = P \quad (5.5)$$

In this case, the common dc-link current I_{dc} acts as a combined load to all modules which is dictated by the grid side power. Equations (5.6) and (5.7) provide small signal equations for i^{th} module where $V_{dc,i}$, $I_{batt,i}$ and D_i is the steady-state values of module dc-link voltage, current and duty ratio.

$$L \frac{d\widehat{i_{batt,i}}}{dt} + \widehat{i_{batt,i}} R + (1 - D_i) \widehat{V_{dc,i}} - \widehat{d}_i V_{dc,i} = \widehat{V_{batt,i}} \quad (5.6)$$

$$C \frac{d\widehat{V_{dc,i}}}{dt} - (1 - D_i) \widehat{i_{batt,i}} + \widehat{d}_i i_{batt,i} = -\widehat{i_{dc}} \quad (5.7)$$

There are two state variables chosen as, $i_{batt,i}$ and $V_{dc,i}$ per module, one control input d_i , one power input $V_{batt,i}$ and one disturbance input i_{dc} . The state-space equation of i^{th} module is therefore:

$$\dot{X} = \begin{pmatrix} -\frac{R}{L} & -\frac{(1-D_i)}{L} \\ \frac{(1-D_i)}{C} & 0 \end{pmatrix} X + \begin{pmatrix} \frac{1}{L} & \frac{V_{dc,i}}{L} & 0 \\ 0 & -\frac{i_{batt,i}}{C} & -\frac{1}{C} \end{pmatrix} U$$

where, $X = \begin{pmatrix} i_{batt,i} \\ V_{dc,i} \end{pmatrix}$, $U = \begin{pmatrix} V_{batt,i} \\ \widehat{d}_i \\ \widehat{I_{dc}} \end{pmatrix}$ (5.8)

Since the control input is \widehat{d}_i , the transfer functions of interests are: a) $\frac{\widehat{i_{batt,i}}(s)}{\widehat{d}_i(s)}$ and b) $\frac{\widehat{V_{dc,i}}(s)}{\widehat{d}_i(s)}$ which can be directly derived from this state-space equation as shown in (5.9) and (5.10). These expressions can help to design the current and/or voltage controller for a particular module.

$$\frac{\widehat{i_{batt,i}}(s)}{\widehat{d}_i(s)} = \frac{I_{batt,i}}{(1-D_i)} \frac{1 + \frac{sV_{dc,i}C}{(1-D_i)I_{batt,i}}}{1 + s\left(\frac{R}{L}\right) + s^2 \frac{LC}{(1-D_i)^2}} \quad \forall i = 1 \dots n \quad (5.9)$$

$$\frac{\widehat{V_{dc,i}}(s)}{\widehat{d}_i(s)} = \frac{V_{dc,i}}{(1-D_i)} \frac{1 - \frac{sI_{batt,i}L}{(1-D_i)V_{dc,i}}}{1 + s\left(\frac{R}{L}\right) + s^2 \frac{LC}{(1-D_i)^2}} \quad \forall i = 1 \dots n \quad (5.10)$$

5.4 Control in boost mode

Traditionally dc-dc converters in an ESS are controlled using an output capacitor voltage control loop and/or an inner inductor current loop employing a fixed reference. However, such strategy is not applicable in this case because there are multiple constraints including: a) controlling the total dc-link voltage (V_{dc}) to a constant value for uninterrupted line side inverter operation, b) controlling of individual modules according to the desired current references ($i_{batt,1}^*$, $i_{batt,2}^*$... $i_{batt,n}^*$) or weighing factors as described in chapter – 4, and c) controlling of the module capacitor voltages ($V_{dc,1}$, $V_{dc,2}$... $V_{dc,n}$) such that they meet the constraint of a boost converter ($V_{dc,i} \geq V_{batt,i}$ and $i_{batt,i} > I_{dc} \forall i = 1..n$) to deliver the desired power from a module.

5.4.1 Proposed DC-side control structure

The proposed control structure controls each module capacitor to different voltage levels to distribute the total power among the modules because the same dc-link current (I_{dc}) flows through all the cascaded modules. Therefore, the control structure behaves like a voltage sharing scheme which calculates the different module voltage references ($V_{dc,1}^*$, $V_{dc,2}^*$... $V_{dc,n}^*$) where the sum of all the references is a fixed central dc-bus reference (V_{dc}^*) for the inverter. The required module voltage references are generated to allow the control system to share the current according to the desired ratio. These are derived using the power balance equations (5.4) and weighting factors as shown in (5.11) for charging and discharging respectively. Fig. 5.2(a) describes the proposed module dc-link voltage references ($V_{dc,1}^*$, $V_{dc,2}^*$... $V_{dc,n}^*$) generation from the weighting factors and Fig. 5.2(b) shows how the individual module is controlled. Moreover, the reference generation makes use of the binary control signal of the switches T_i , T_{ii} to adjust/re-calculate the weighting factors when any of the modules bypasses because the control signals of the fault tolerant leg T_i , T_{ii} are either 0 or 1. Each module is controlled by an outer voltage control loop and an inner current control loop as shown in Fig. 5.3. The output of each inner loop provides the desired duty ratio command. The bandwidth of each inner current loop is set to several times higher than the outer voltage loop to help to maintain module control stability.

$$i_{batt,i}^* \propto \omega_i, V_{dc,i}^* \propto V_{batt,i} \omega_i = V_{dc}^* \frac{\omega_i V_{batt,i} T_i}{\sum_{k=1}^n \omega_k V_{batt,k} T_k} \quad \forall i = 1 \dots n \quad (5.11)$$

Since the module dc-link voltages are different, some of the module voltage ($V_{dc,i}$) may exceed the maximum switch rating during the operation and can cause failure of the module. To avoid this, the control system needs to know the maximum duty ratio of a module so that such a situation can be avoided. Expression (5.12) provides the limit of each module duty ratio (d_i) which is dependent on maximum switch stress (V_{sw}). The V_{sw} is set up from the choice of hardware and levels of redundancy. This limit also indicates the control range of the converter. The Matlab/Simulink model of the proposed control structure in boost mode is shown Fig. 5.4 where three control loops are shown separately. The simulation results are generated using this model to compare with the hardware results.

$$d_i \leq d_{max,i} \leq \left(1 - \frac{V_{batt,i}}{V_{sw}}\right) \forall i = 1..n \quad (5.12)$$

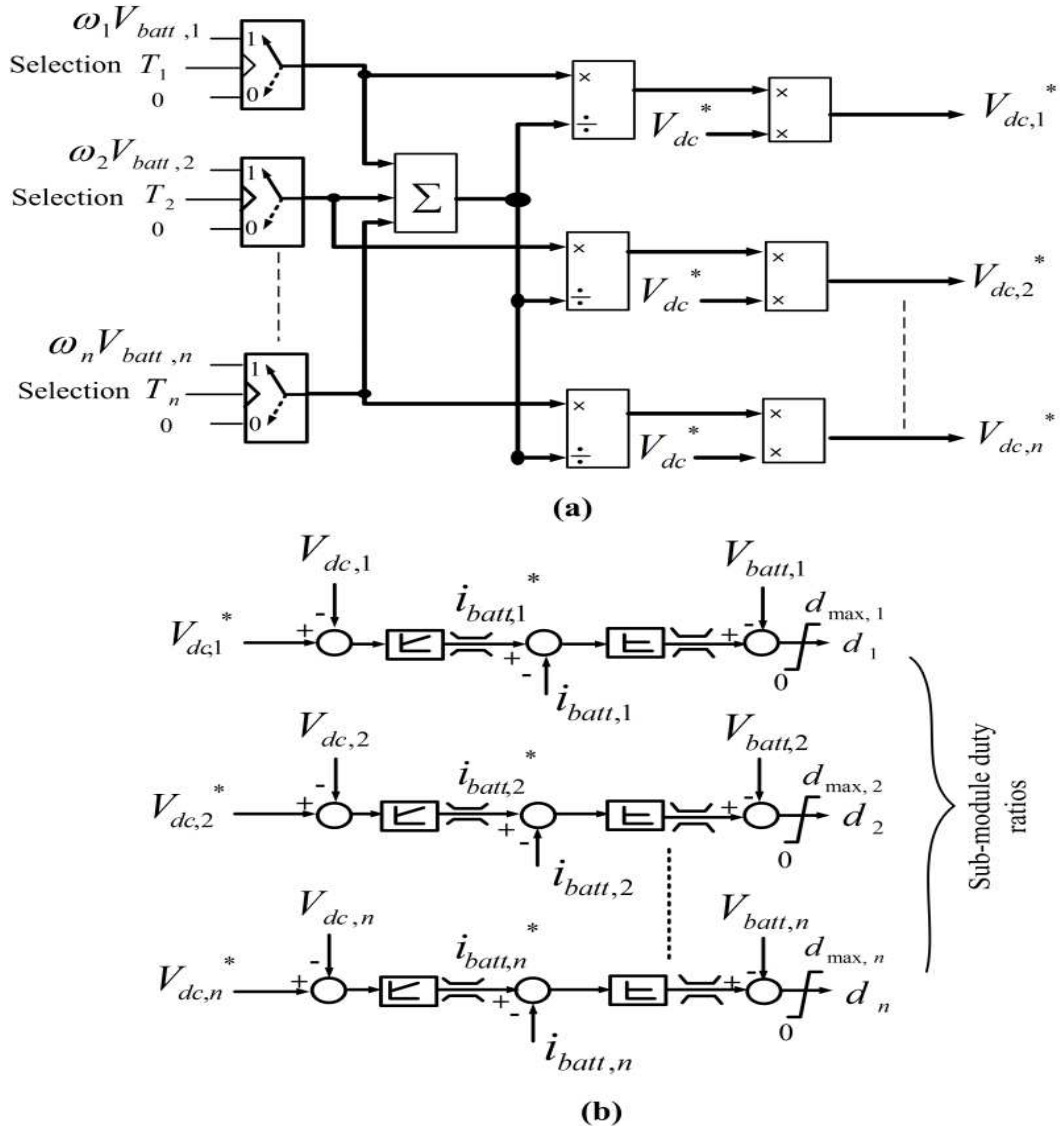


Fig. 5.2 Proposed distributed control architecture in boost mode: a) module dc-link voltage reference generation, b) module based voltage control structure

5.4.2 Controller design

The controller design is performed in two-stages: a) module outer voltage loop design, b) module inner current loop design.

5.4.2.1 Voltage controller design:

Fig. 5.3(a) shows the voltage control loop assuming inner current loop delay (T_d) of around four times sample time (T_s). The open loop transfer function $GH_v(s)$ is shown in (5.13) to help design suitable control parameters. It can be noticed that $GH_v(s)$ is dependent on all the battery parameters such as voltage, capacity. The control parameter can be designed using symmetric optimum method as described in [363] keeping the same phase margin (PM) for all the modules ('a' depends on the desired PM) to ensure the overall stability of the modular

converter. The frequency response plot of the voltage control loop is shown in Fig. 5.5. The PM of a stable control system is generally taken to be anything higher than 45° . In this case, it is assumed to be around 70° which gives rise to $a = 6$ to guarantee the module stability. As a result of this the gain crossover frequency becomes around 35Hz which represents the closed loop bandwidth. The Maltlab/Simulink model of this controller design method is shown in Fig. 5.6.

$$GH_v(s) = K_{v,i} \left(\frac{1 + sT_v}{sT_v} \right) \left(\frac{1}{1 + sT_d} \right) \left(\frac{V_{batt,i}}{V_{dc,i}} \right) \left(\frac{1}{sC} \right) \text{ where}$$

$$K_{v,i} = \frac{1}{a} \left(\frac{V_{dc,i}}{V_{batt,i}} \right) \frac{1}{T_d} C \text{ and } T_v = a^2 T_d \quad \forall i = 1 \dots n \quad (5.13)$$

5.4.2.2 Current controller design

The current loop can be formed as shown in Fig. 5.3(b). Proportional control has been chosen in the current loop to improve the speed of response and stability. K_c can be set from the desired closed loop bandwidth (BW). In this case, it is taken to be 2 kHz for all the modules. The current loop transfer function $\frac{\widehat{i_{batt,i}}(s)}{\widehat{d_i}(s)}$ (derived from Fig. 5.3(b)) has been approximated at high frequency to design K_c as shown in (5.14). Here ‘G’ represents the PWM carrier peak inside the controller which is taken as $V_{dc,i}$. It can be seen from Fig. 5.7 that modules have the same current loop bandwidth (same high frequency response). It is important to note that the module current controller parameters are independent of ω_i . As a result, the current controller parameters do not need to be adaptive in nature unlike the voltage controller parameters.

$$GH_I(s) = K_c \frac{1}{G} \frac{i_{batt,i}(s)}{d_i(s)} \approx K_c \frac{1}{G} \frac{V_{dc,i}}{sL} \quad \leftarrow \text{At high frequency}$$

$$K_c = \frac{(BW)L}{V_{dc,i}} G = (BW)L \quad (5.14)$$

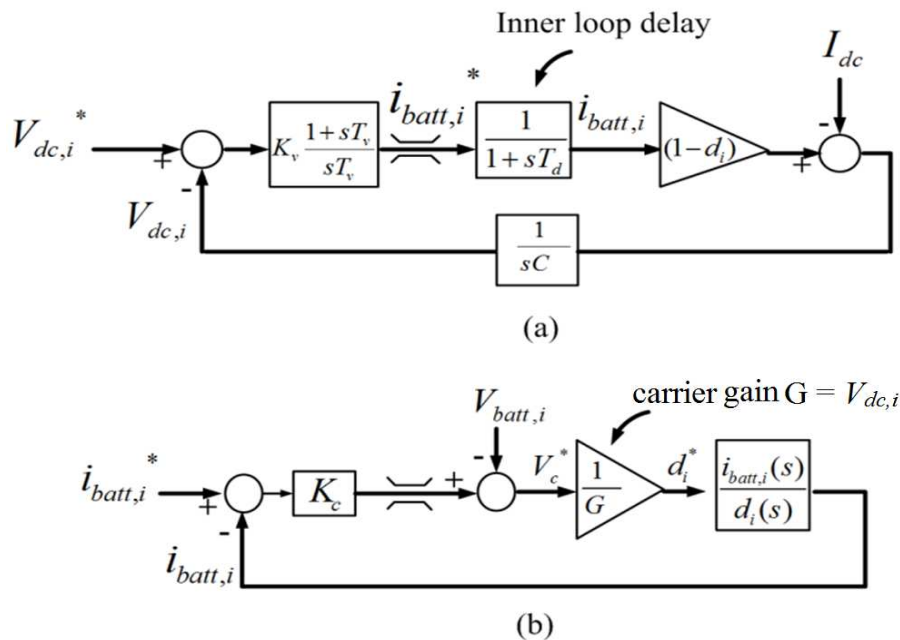


Fig. 5.3 Control loops per module: a) module voltage loop, b) current control loop

5.4.3 Dynamic response

The response time as shown by the rise time is directed by the closed loop bandwidth of a system. The closed loop bandwidth can be taken approximately equal to the gain crossover frequency if the system magnitude plot crosses the 0dB axis at -20dB/decade (as shown in Fig. 5.5). This closed loop bandwidth then can be used to estimate the response time.

In an SLBESS, the response time can be calculated by combining the response time of the inverter and associated dc-dc converters. In the converter, all the modules are controlled such that their closed loop bandwidths are the same (Fig. 5.5). The inverter is controlled in constant power mode responds and the dc-dc converters are controlled in voltage mode. Therefore, the response time of the line side inverter decided by the current loop bandwidth and the response time of the dc-dc converter is determined by the module voltage loop bandwidth. The line side inverter when working in current loop responds very fast to meet the load demand with the dc-dc converters responding slower than the inverter. Therefore, the total response time ($T_{r,i}$) \approx the response time of dc-dc converters ($T_{r,d}$). Traditionally the bandwidth of the voltage control loop in a conventional BESS is kept to a low value ($\leq 10\text{Hz}$) to ensure control stability [217] – [218]. This is because a high value of boost inductance is used (8 – 10mH) in conventional dc-dc converters which limit the bandwidth of the inner current control loop which in turn limits the outer voltage loop bandwidth. This slow control bandwidth makes the response time of a conventional BESS in the range of 50 – 100ms or higher.

In this work, the response time of each module voltage control loop can be made faster compared to a conventional BESS by exploiting the advantage of the lower input boost inductor/module (due to cascaded multi-modular converter structure) which makes the inner current tracking control of the modular dc-dc converters almost instantaneous. This provides an opportunity to increase the outer module voltage control bandwidth to achieve faster dynamic response. However, there is a limit up to which the bandwidth can be increased or the boost inductance can be reduced. A low value of inductance would increase di/dt and high frequency noise such as current ripple in the module current which makes the protection design more challenging and could be a drawback from the practical implementation point of views.

For stable second order systems, it is well known that the product of rise time and bandwidth ($T_r \omega_{gc}$) is approximately constant and is given by (5.15) [364]. The gain crossover frequency ($\omega_{gc,i}$) can be found by solving (5.16) for this case. Due to the presence of a higher order equation, the gain crossover frequency is found using a numerical program (written in MATLAB) and by directly entering the measured battery values and dc-link voltages found in the experimental setup.

$$T_{r,i} = \frac{0.35}{f_{BW}} = \frac{2.2}{\omega_{gc,i}} \quad (5.15)$$

$$|GH(j\omega_{gc,i})| = 1 \Rightarrow \frac{K_y V_{batt,i}}{T_v V_{dc,i} C} \left(\frac{\sqrt{1+(\omega_{gc,i} T_v)^2}}{(\omega_{gc,i})^2 \sqrt{1+(\omega_{gc,i} T_d)^2}} \right) = 1 \quad (5.16)$$

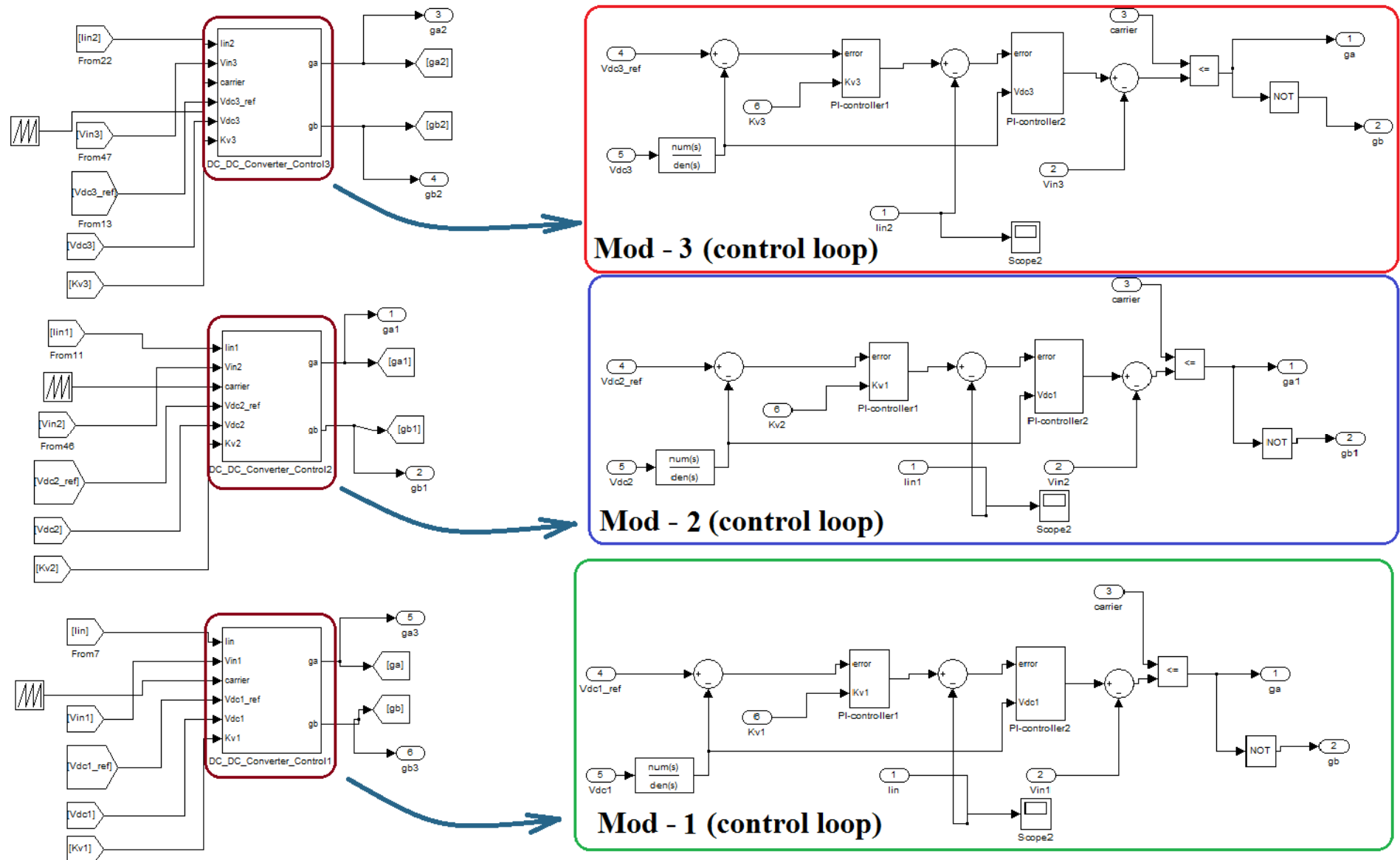


Fig. 5.4 Matlab/Simulink model of the control loops in boost mode

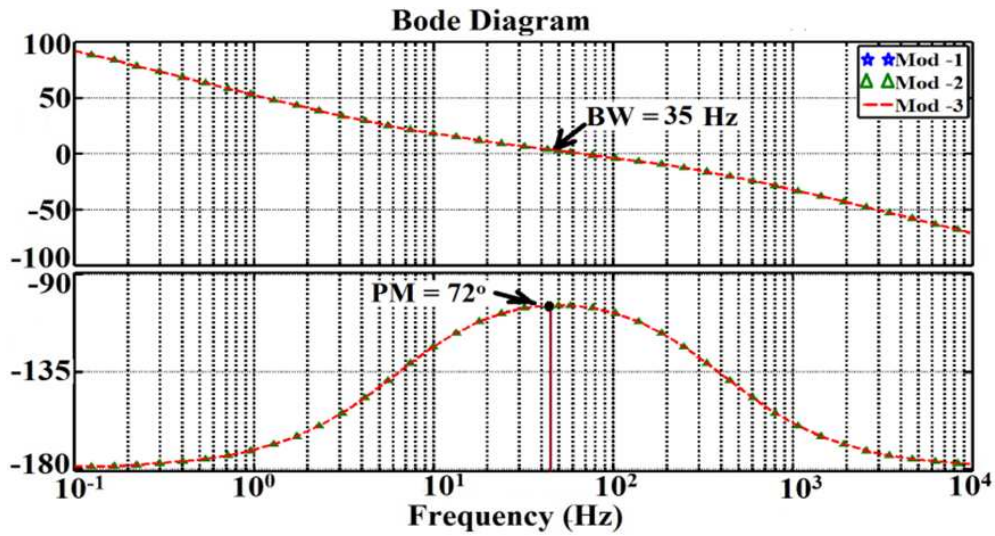


Fig. 5.5 Frequency response plot of the module voltage control loop

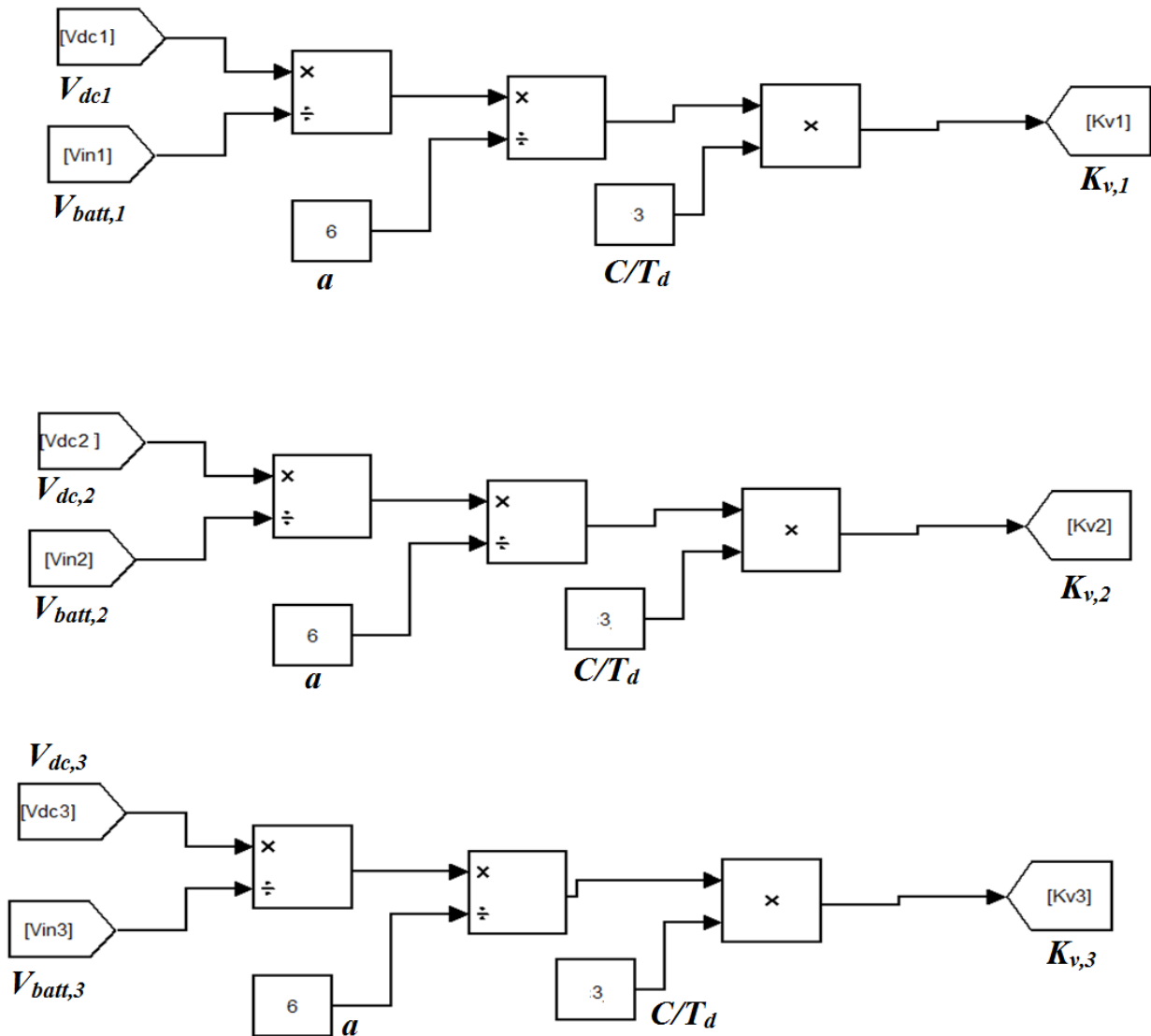


Fig. 5.6 Adaptive PI-tuning and controller parameter determination for three modules

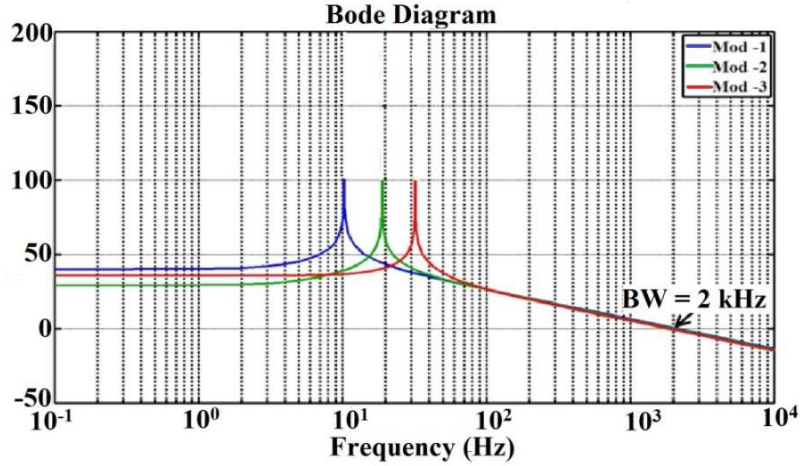


Fig. 5.7 Frequency response plot of the module inner current control loop

5.4.4 Proposed overall control structure including the line side inverter

The overall control structure while operating in boost mode (T_i , T_{ii} in idle mode) is shown in two stages: dc-side distributed control in Fig. 5.8. It can be seen that there is an interaction between the line side inverter control and the dc-side control. The grid side control depends on the type of application of the energy storage system, e.g., voltage control or the frequency control and the rotating virtual rotating ‘dq’ frame based approach has been followed for the inverter as shown in Fig. 5.9.

The dynamics of the equation can be described using (26) where \vec{i}_s , \vec{V}_s are the line side space vectors and \vec{U}_{inv} is converter output space vector. The θ denotes the angle of rotation which comes from output of PLL. The grid voltage space vector (\vec{V}_s) is made to be aligned with the ‘q’-axis (Fig. 5.9) which means $V_{sq} = |V_s|$. This way the actual unit vector θ is made equal to the estimated unit vector ($\hat{\theta}$) as shown in Fig. 5.10 and Fig. 5.11. So, the ‘q’ axis acts as an active power axis and ‘d’ axis acts as the reactive power axis in this case. The line side control structure is shown in Fig. 5.12. A low pass filter (LPF) has been employed to generate the ‘ $\alpha\beta$ ’ (orthogonal components) in single phase application. After generating the ‘ $\alpha\beta$ ’ components, the unit vector $e^{j\theta}$ has been employed to transform them in ‘dq’ frame. The dynamic equation can be transformed in ‘dq’ domain putting $(i_{sd} + ji_{sq})e^{j\theta}$, $(V_{sd} + jV_{sq})e^{j\theta}$ and $(U_{invd} + jU_{invq})e^{j\theta}$ which gives (5.17) to (5.20). It is to be noted that there exists a clear coupling between ‘d’-axis and ‘q’-axis which requires appropriate feed-forward terms to decouple those as indicated in Fig. 5.12.

$$L_s \frac{d\vec{i}_s}{dt} + R_s \vec{i}_s + \vec{V}_s = \vec{U}_{inv} \quad (5.17)$$

$$L_s \frac{di_{sd}}{dt} + R_s i_{sd} - \omega L_s i_{sq} = U_{invd} \quad (5.18)$$

$$L_s \frac{di_{sq}}{dt} + R_s i_{sq} + \omega L_s i_{sd} = U_{invq} \quad (5.19)$$

$$\frac{d\theta}{dt} = \omega \quad (5.20)$$

The expression of active and reactive power can be found using (5.21) and (5.22). Therefore,

controlling the active power requires controlling of ‘ q ’-axis current while the reactive power requires controlling ‘ d ’-axis current.

$$P_{inv} = \frac{1}{2} V_{sq} i_{sq} \quad (5.21)$$

$$Q_{inv} = -\frac{1}{2} V_{sq} i_{sd} \quad (5.22)$$

The output of the voltage or frequency controller provides the reference for the inner q -axis current loop. The d -axis current reference is set from the reactive power requirements of the converter (if any). The weighting factor (ω_i) of the proposed dc-side distributed control is different in charging and discharging. The mode selection is performed in this thesis using the sign of active line current reference i_{sq}^* through an edge detector because i_{sq}^* is positive for discharging and negative for charging. This selection method dynamically changes the module dc-link voltage references ($V_{dc,i}^*$) to alter the current sharing ($i_{batt,i}$) while switching from the charging to discharging and vice-versa. The Matlab/Simulink model of the inverter control structure is shown in Fig. 5.13.

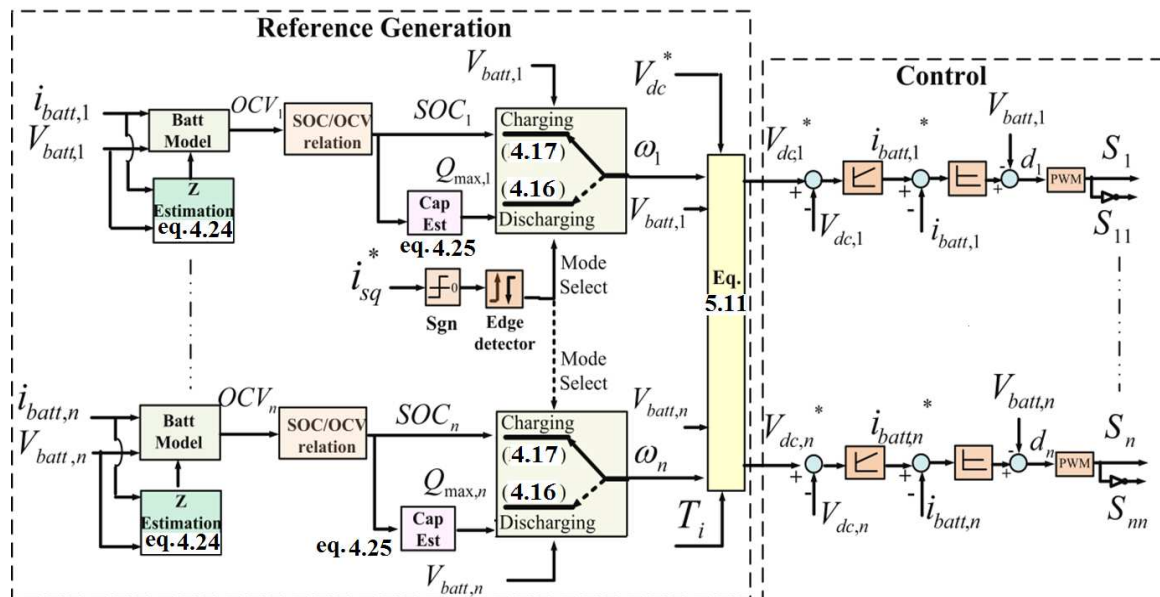


Fig. 5.8 Proposed overall control architecture in boost mode: dc-side distributed control

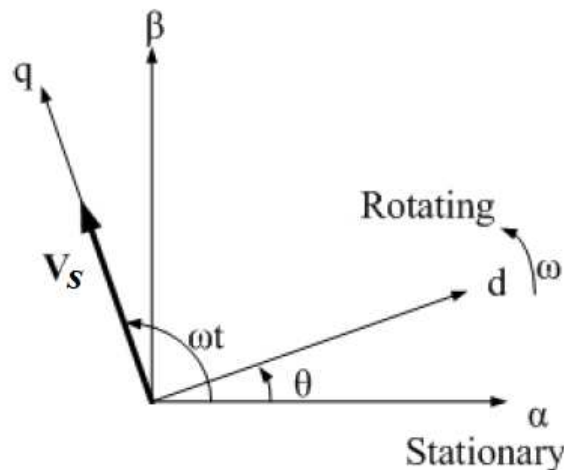


Fig. 5.9 Rotating frame for the line side inverter control

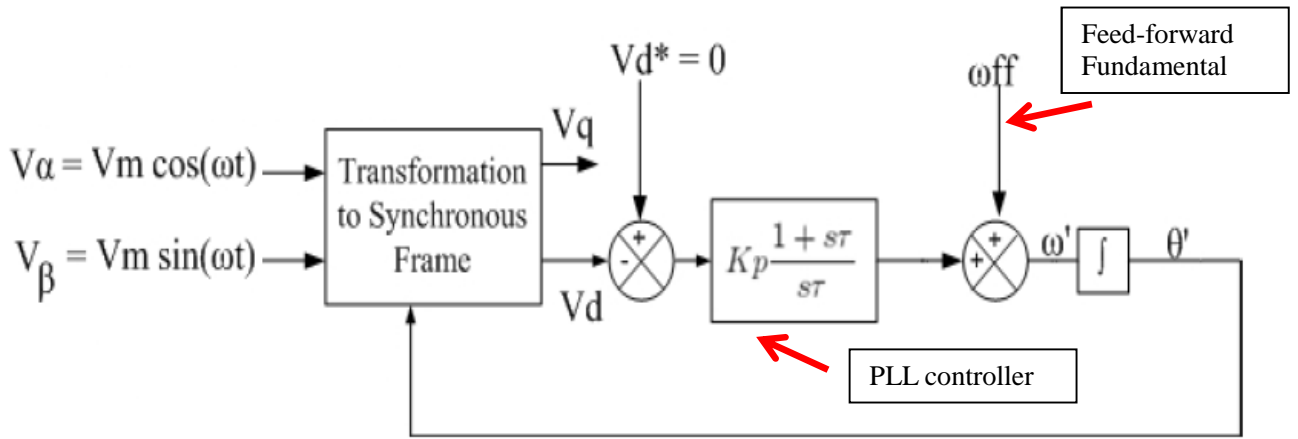


Fig. 5.10 Single phase PLL structure

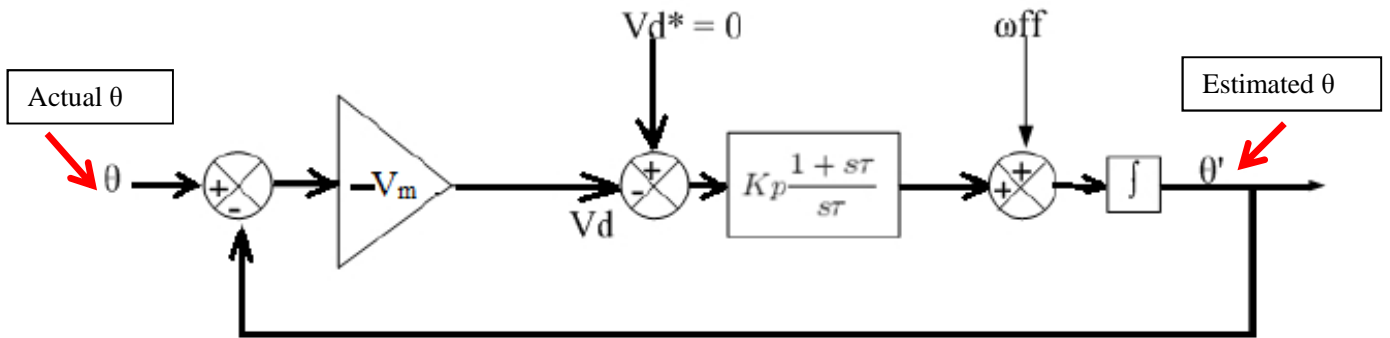


Fig. 5.11 Simplified block diagram of the PLL control

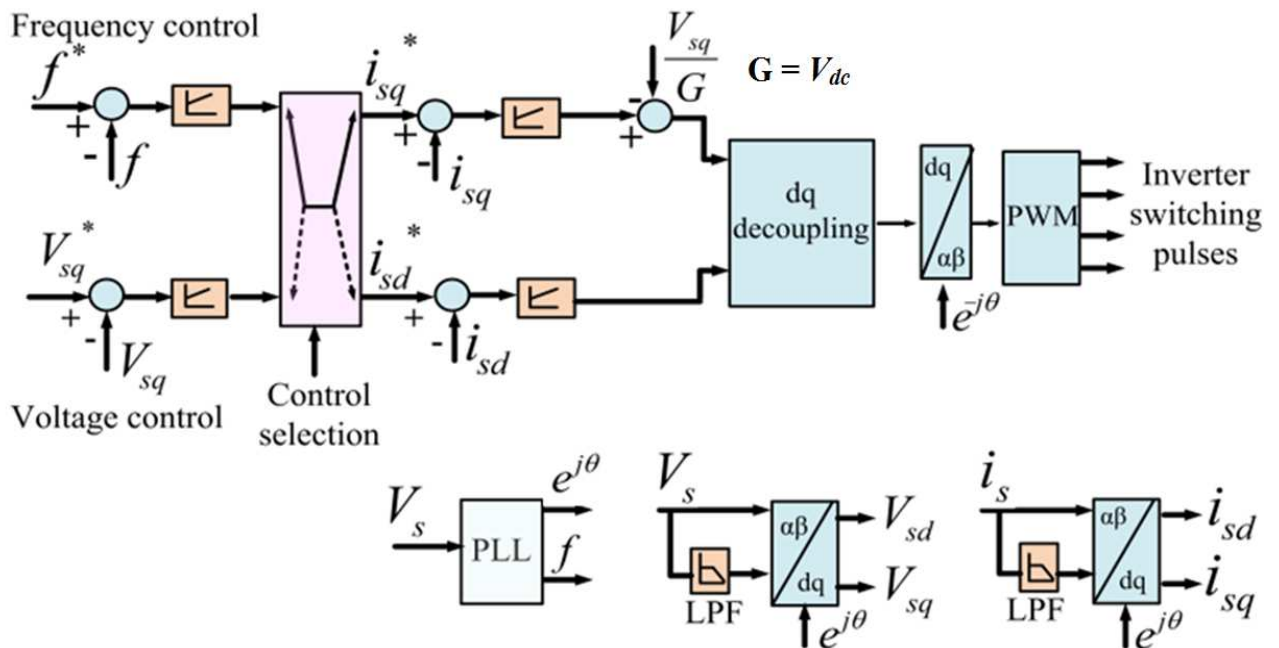


Fig. 5.12 Rotating frame based integrated control strategy for the line side inverter

5.5 Modelling in buck mode

This mode of operation corresponds to $\sum V_{batt,i} > V_{dc}^*$ and the modeling has been performed assuming $S_i, S_{ii} \forall i = 1 \dots n$ in idle mode as described in chapter – 3. The module current and voltage dynamics of the converter are written in (5.23) – (5.24). It is to be noted that the average value of $V_{batt,i}$ and $V_{dc,i}$ are the same here because S_{ii} is ON and S_i is OFF. Therefore, in this mode, the dynamics of $i_{batt,i}$ mainly depends on the dynamics of $i_{dc,i}$. There are two types of duty ratio possible in this mode: a) average duty ratio (d_{av}) which maintains the central dc-bus V_{dc} and, b) individual module duty ratio of T_i, T_{ii} (d_{ii}) which controls the individual module current ($i_{batt,i}$) using $i_{dc,i}$. The relation between these two is provided in (5.25). The dc-link dynamics are given in (5.26) – (5.27) which describe how I_{dc} and V_{dc} are related.

$$L \frac{di_{batt,i}}{dt} + Ri_{batt,i} + V_{dc,i} = V_{batt,i} \forall i = 1 \dots n \quad (5.23)$$

$$C \frac{dV_{dc,i}}{dt} = i_{batt,i} - i_{dc,i} \forall i = 1 \dots n \quad (5.24)$$

$$d_{av} = \frac{\sum V_{dc,i} d_{ii}}{\sum V_{dc,i}} \quad (5.25)$$

$$L_{dc} \frac{di_{dc}}{dt} + R_{dc} i_{dc} + V_{dc} = d_{av} \sum V_{dc,i} \forall i = 1 \dots n \quad (5.26)$$

$$C_{dc} \frac{dV_{dc}}{dt} = i_{dc} - i_{inv} \quad (5.27)$$

The power balance equations of the modules are given in (5.28). It should be noted that the average value of $V_{dc,i}$ and $V_{batt,i}$ are the same which makes the average value of $i_{dc,i}$ and $i_{batt,i}$ are the same in this mode. Moreover, the efficiency η_i is approximated to 1 based on the results from chapter – 3 due to the efficient low voltage semiconductors in the cascaded converter.

$$V_{dc,i} i_{dc,i} = \eta_i V_{batt,i} i_{batt,i} \forall i = 1 \dots n \quad (5.28)$$

The small signal modelling is performed in two-stages; module level (5.29) to (5.30) and dc-link level (5.27) – (5.28).

$$L \frac{d\widehat{i}_{batt,i}}{dt} + R\widehat{i}_{batt,i} + \widehat{V}_{dc,i} = \widehat{V}_{batt,i} \forall i = 1 \dots n \quad (5.29)$$

$$C \frac{d\widehat{V}_{dc,i}}{dt} = \widehat{i}_{batt,i} - \widehat{i}_{dc,i} = \widehat{i}_{batt,i} - \widehat{d}_{ii} I_{dc} - D_{ii} \widehat{v}_{dc} \forall i = 1 \dots n \quad (5.30)$$

The state-space equation of i^{th} module is:

$$(\dot{X}) = \begin{pmatrix} -\frac{R}{L} & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{pmatrix} (X) + \begin{pmatrix} \frac{1}{L} & 0 \\ 0 & -\frac{I_{dc}}{C} \end{pmatrix} (U)$$

$$\text{where, } \dot{X} = \begin{pmatrix} \frac{di_{batt,i}}{dt} \\ \frac{dV_{dc,i}}{dt} \end{pmatrix}, U = \begin{pmatrix} V_{batt,i} \\ \widehat{d}_{ii} \end{pmatrix} \quad (5.31)$$

The transfer function of interests is $\frac{i_{batt,i}(s)}{\widehat{d}_{ii}(s)}$ because d_{ii} is the main control variable. It can be derived from the state-space equation as shown in (5.32).

$$\frac{i_{batt,i}(s)}{\widehat{d}_{ii}(s)} = \frac{I_{dc}}{LC} \frac{1}{s^2 + s\left(\frac{R}{L}\right) + \frac{1}{LC}} \quad \forall i = 1 \dots n \quad (5.32)$$

At dc-link level, the small signal equations are;

$$L_{dc} \frac{d\widehat{i}_{dc}}{dt} + R_{dc} \widehat{i}_{dc} + \widehat{V}_{dc} = (D_{av}) \sum \widehat{V}_{dc,i} + \widehat{d}_{av} \sum V_{dc,i} \quad (5.33)$$

$$C_{dc} \frac{d\widehat{V}_{dc}}{dt} = \widehat{i}_{dc} - i_{inv} \quad (5.34)$$

The state-space equation of buck converter can be written as following:

$$(\dot{X}) = \begin{pmatrix} -\frac{R_{dc}}{L_{dc}} & -\frac{1}{L_{dc}} \\ \frac{1}{C_{dc}} & 0 \end{pmatrix} (X) + \begin{pmatrix} \frac{D_{av}}{L} & \frac{\sum V_{dc,i}}{L} & 0 \\ 0 & 0 & -\frac{1}{C_{dc}} \end{pmatrix} (U) \quad \forall i = 1 \dots n$$

$$\text{where, } X = \begin{pmatrix} \widehat{i}_{dc} \\ \widehat{V}_{dc} \end{pmatrix}, U = \begin{pmatrix} \sum \widehat{V}_{dc,i} \\ \widehat{d}_{av} \\ i_{inv} \end{pmatrix} \quad (5.35)$$

The transfer functions of interests are: a) $\frac{\widehat{i}_{dc}(s)}{\widehat{d}_{av}(s)}$ and b) $\frac{\sum V_{dc,i}(s)}{\widehat{d}_{av}(s)}$ because d_{av} is the main control variable and is responsible for controlling the dc-link voltage V_{dc} .

$$\frac{\widehat{i}_{dc}(s)}{\widehat{d}_{av}(s)} = \frac{I_{inv}}{L_{dc} C_{dc}} \frac{1}{s^2 + s\left(\frac{R_{dc}}{L_{dc}}\right) + \frac{1}{L_{dc} C_{dc}}} \quad \forall i = 1 \dots n \quad (5.36)$$

$$\frac{\sum V_{dc,i}(s)}{\widehat{d}_{av}(s)} = \frac{I_{inv}}{C_{dc}} \frac{s + \frac{R_{dc}}{L_{dc}}}{s^2 + s\left(\frac{R_{dc}}{L_{dc}}\right) + \frac{1}{L_{dc} C_{dc}}} \quad \forall i = 1 \dots n \quad (5.37)$$

5.6 Control in buck mode

This control in buck mode is the dual of the boost control mode which is described in section 5.4 (applicable only when $\sum V_{batt,i} > V_{dc}^*$). In this case, the module dc-link voltages ($V_{dc,i}$) are automatically maintained by battery terminal voltages $V_{batt,1}, V_{batt,2} \dots V_{batt,n}$. Therefore,

the aim of this control mode are: a) to maintain the central dc-link voltage to V_{dc}^* irrespective of the set of battery modules present, b) to distribute the total power to the hybrid battery modules according to desired weighting factor (ω_i).

The module independent control is achieved by distributed duty ratios $d_{11}, d_{22} \dots d_{nn}$ of T_i, T_{ii} which controls the module dc-link current $i_{dc,i}$ to control $i_{batt,i}$. As a result these duty ratios become a function of ω_i . The overall dc-link voltage V_{dc} is maintained by the overall duty ratio (d_{av}) as described in the dynamic equations (5.25) – (5.27). The desired distribution of duty ratios can be found from power balance equation (5.28) as shown in (5.38) and (5.39). The exact expression of module duty ratio can be found using overall duty ratio as shown in (5.39).

$$V_{batt,i} i_{dc,i} = V_{batt,i} i_{batt,i} \rightarrow i_{dc,i} = i_{batt,i} \text{ or}$$

$$i_{batt,i}^* \propto \omega_i \rightarrow d_{ii} \propto \omega_i \quad \forall i = 1 \dots n \quad (5.38)$$

$$d_{av} = \frac{\sum V_{dc,i} d_{ii}}{\sum V_{dc,i}} = \frac{\sum V_{batt,i} d_{ii}}{\sum V_{batt,i}} \text{ Solving for } d_{ii}$$

$$d_{ii} = \omega_i d_{av} \frac{(\sum_{i=1}^n V_{batt,i})}{\sum_{i=1}^n \omega_i V_{batt,i}} \quad \forall i = 1 \dots n \quad (5.39)$$

Therefore, the module duty ratios continue to vary online with the battery weighting factor to change the power sharing. As a result of this distributed operation, the converter behaves as a multilevel dc-dc converter per switching cycle because a single carrier and multiple reference signals are used to generate the control signals of the switches (T_i, T_{ii}) as shown in Fig. 5.14. For an n-module dc-dc converter connected in the similar fashion, maximum $n+ 1$ level is achievable. The number of levels depends on the number of modules as well as on the distribution of duty ratios. In the case where the same duty ratio is calculated for multiple modules, the number of levels will be less than $(n+1)$.

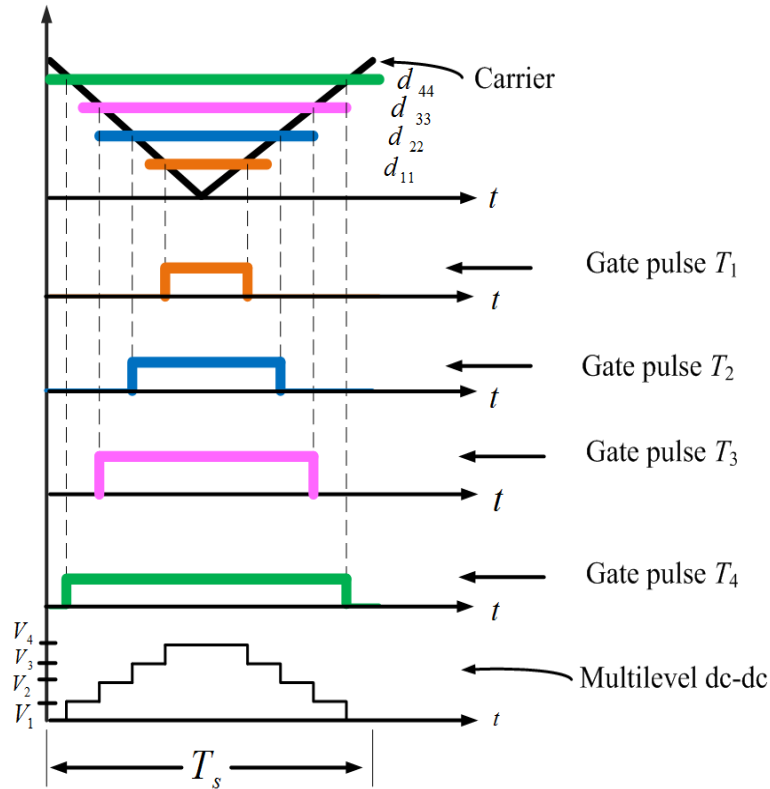


Fig. 5.14 Multilevel operation per switching cycle using distributed duty ratio

5.6.1 Proposed DC-side control structure

The detailed control structure of the multilevel converter is shown in Fig. 5.15. The control structure is composed of: a) control of central inverter dc-link voltage and b) control of individual module according to the weighting factors. The control structure employs a central dc-bus voltage loop and the output of that controller provides the overall duty ratio (d_{av}) command through an inner dc-link current loop which controls V_{dc} and then this overall duty ratio is split into module duty ratios (d_{ii}) using (5.39). It should be noted that input side boost converters become inoperative in this case which implies $d_1 = d_2 = \dots = d_n = 0$. The weighting factor for charging and discharging is different and the change-over of weighting factor between charging and discharging is performed using the sign of i_{sq}^* because the sign of it acts as an indicative of the phase angle between the line side voltage and the current.

5.6.2 Controller design

In this mode of operation, the controller design is performed in two-stages: a) central dc-link voltage loop, b) inner dc-link current loop. Fig. 5.16(a) shows the voltage control loop assuming inner current loop delay (T_d) is around four times of sample time (T_s). The open loop transfer function $GH_v(s)$ is written in (5.40) to help design suitable control parameters. It can be noticed that $GH_v(s)$ is not dependent on any of the battery parameters or weighting factor. The control parameters can be designed as before using symmetric optimum method [363] selecting a particular PM ('a' depends on the desired PM). However, in this case, PM is taken as 45° to get a fast dynamic response because no stability problem can arise due to

weighting factor variation over the time unlike in boost mode of operation. This PM gives $a = 4$. The current loop can be formed as shown in Fig. 5.16(b). A proportional control has been chosen in the current loop to improve the speed of response and stability. K_{cd} can be set from the desired closed loop bandwidth (BW) of the inner current loop.

$$GH_v(s) = K_{dc} \left(\frac{1 + sT_{dc}}{sT_{dc}} \right) \left(\frac{1}{1 + sT_d} \right) \left(\frac{1}{sC_{dc}} \right) \text{ where}$$

$$K_{dc} = \frac{1}{aT_d} C_{dc} \text{ and } T_{dc} = a^2 T_d \quad (5.40)$$

$$GH_I(s) = K_{cd} \frac{1}{G} \frac{i_{dc}(s)}{d_{av}(s)} \approx K_c \frac{1}{G} \frac{V_{dc}}{sL_{dc}}, \leftarrow \text{At high frequency}$$

$$K_{cd} = \frac{(BW)L_{dc}}{V_{dc}} G = (BW) \cdot L_{dc} \quad (5.41)$$

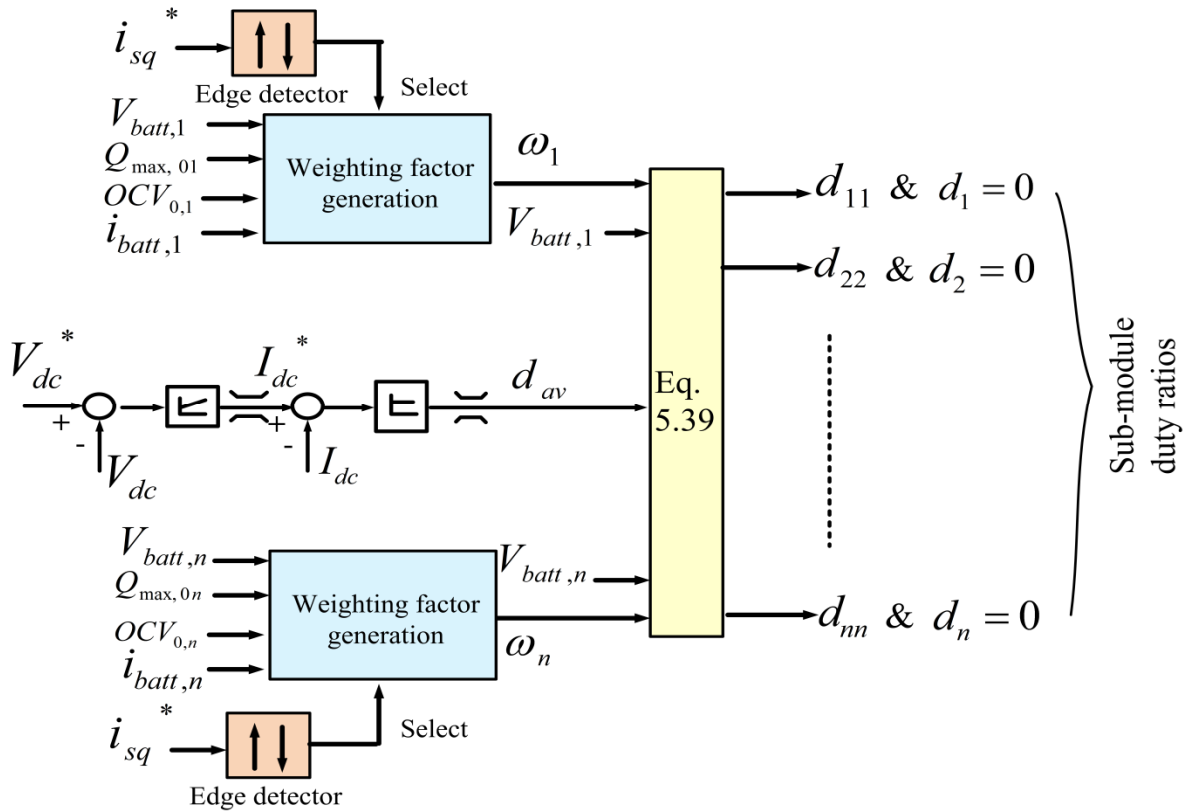


Fig. 5.15 Proposed DC-side control architecture in buck mode

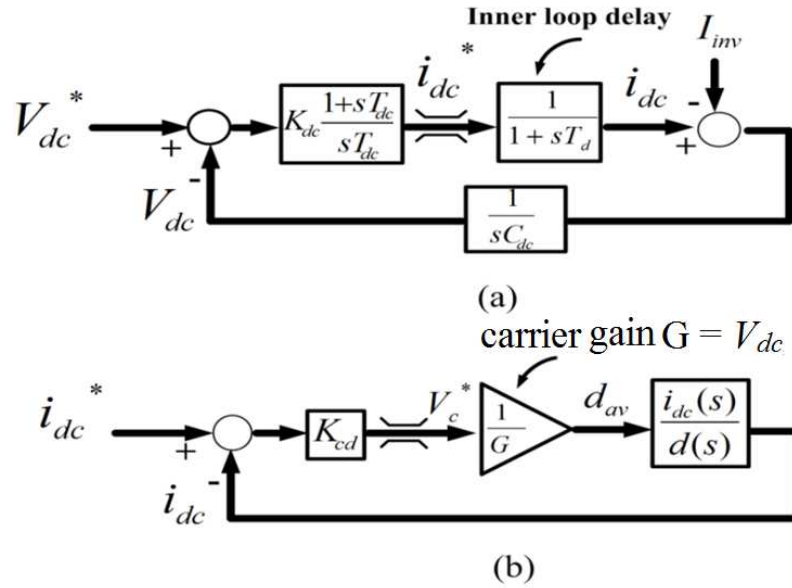


Fig. 5.16 DC-link control loops: a) dc-link voltage control loop, b) dc-link current control loop

5.7 Modelling in boost-buck mode

This mode of operation is more generalised as it covers both boost and multilevel buck mode together. As a result of this, it is applicable to $\sum V_{batt,i} < V_{dc}^*$ or $\sum V_{batt,i} > V_{dc}^*$. H Bridge switches (S_i , S_{ii} and T_i , T_{ii}) in the module are all controlled in PWM mode. The dynamic modeling of this system is composed of a combination of boost mode and buck mode. Therefore, the equations (5.1) and (5.2) provide the dynamics of boost module and while (5.23) – (5.27) describes the dynamics of the output side of the multilevel buck converter. The expressions (5.13) and (5.14) are used to design the module voltage and current controller. The expressions (5.40) and (5.41) are used to design the dc-link voltage and dc-link current controller respectively.

5.8 Control in boost-buck mode

The proposed control structure uses the module integrated boost converters to boost the overall battery side voltage higher than the desired dc-link voltage ($\sum V_{dc,i} > V_{dc}^*$) and then uses the concept of distributed duty ratio ($d_{ii} \forall i = 1 \dots n$) of the buck converter switches (T_i , T_{ii}) as a function of battery weighting factors (ω_i) to maintain the inverter dc-link voltage constant. There are two separate cases which need to be considered in this mode: a) the module input voltages are in similar range such as, 7.2V, 12V or 24V and all the input modules can be operated in boost-buck mode (S_i , S_{ii} in PWM and T_i , T_{ii} in PWM $\forall i = 1 \dots n$), b) the module voltages are widely different such as, 24V, 220V or 600V and not all the modules can operate in boost/buck mode for example, when the switch rating is not sufficient to allow the boost operation of a higher voltage connected battery (or to avoid extra losses) – the control strategy to deal with this is: *i*) to operate the higher input voltage module only in buck mode with the corresponding boost converters (k) in idle mode (i.e. S_k , S_{kk} in idle and T_k , T_{kk} in PWM), *ii*) to operate the remaining modules ($n-k$) in boost/buck mode as previously described (S_i , S_{ii} in PWM and T_i , T_{ii} in PWM $\forall i \neq k$).

5.8.1 Case – 1: All the modules in boost-buck mode

The module battery voltages are boosted to $V_{dc,1}, V_{dc,2} \dots V_{dc,n}$ using the input side boost converters ($S_i, S_{ii} \forall i = 1 \dots n$) and then the overall voltage ($\sum V_{dc,i}$) is bucked using the multilevel buck converter (T_i, T_{ii}) to maintain the central inverter dc-link voltage. Apart from maintaining the inverter dc-bus, it can achieve the desired module independent control using the distributed duty ratio $d_{ii} \forall i = 1 \dots n$.

All the module boost converters are controlled to a same voltage reference $V_{dc,m}^*$ independent of the weighting factors where the upper limit of this reference is limited by the maximum switch rating V_{sw} of a module. The selection of this voltage reference is according to (5.42). Due to this uniform voltage control, lower module input voltages within a set of hybrid batteries operate at a higher boost ratio compared to higher module voltages. The distribution of duty ratio is derived from (5.28) as shown in (5.43) – (5.45).

$$nV_{dc,m}^* > V_{dc}^* \text{ or } V_{dc,m}^* > \frac{V_{dc}^*}{n} \rightarrow \frac{V_{dc}^*}{n} < V_{dc,m}^* \leq V_{sw} \quad (5.42)$$

$$V_{dc,m}(d_{ii})I_{dc} = V_{batt,i}i_{batt,i} \text{ or } d_{ii} \propto V_{batt,i}i_{batt,i} \quad (5.43)$$

$$\text{If } i_{batt,i}^* \propto \omega_i \rightarrow d_{ii} \propto \omega_i V_{batt,i} \forall i = 1 \dots n \quad (5.44)$$

$$\text{From (5.19), } d_{av} = \frac{\sum V_{dc,i}d_{ii}}{\sum V_{dc,i}} = \frac{V_{dc,m}(\sum d_{ii})}{nV_{dc,m}} \rightarrow \sum d_{ii} = nd_{av}$$

$$\text{Therefore, } d_{ii} = nd_{av} \frac{\omega_i V_{batt,i}}{\sum_{i=1}^n \omega_i V_{batt,i}} \forall i = 1 \dots n \quad (5.45)$$

5.8.2 Case – 2: Boost- k -out-of- n modules only in buck mode

In this case, the module operates in a mix of PWM and idle mode using appropriate switching combinations. The module voltage reference ($V_{dc,m}^*$) will be according to (5.56) in this case. The desired duty ratio distribution can be derived as follows:

$$\frac{(V_{dc}^* - \sum_{k \neq i} V_{batt,k})}{(n-k)} < V_{dc,m}^* < V_{sw} \forall i \neq k \quad (5.46)$$

$$\text{From (5.22), } V_{dc,i} = V_{dc,m}, d_{ii} \propto \omega_i V_{batt,i} \forall i \neq k = 1 \dots n$$

For the (k) modules in buck mode, from (5.28);

$$V_{dc,k} = V_{batt,k}, V_{batt,k}i_{dc,k} = V_{batt,k}i_{batt,k} \rightarrow d_{kk} \propto \omega_k \forall k \neq i \quad (5.47)$$

Now with the help of (5.25), following expressions are derived:

$$V_{dc,m} \sum_{i \neq k} d_{ii} + \sum_k V_{batt,k} d_{kk} = d_{av} \left((n-k)V_{dc,m} + \sum_k V_{batt,k} \right) \quad (5.48)$$

$$\text{Equating, } V_{dc,m} \sum_{i \neq k} d_{ii} = d_{av}(n-k)V_{dc,m} \text{ and } \sum_k V_{batt,k} d_{kk} = d_{av} \sum_k V_{batt,k} \quad (5.49)$$

$$\sum_{i \neq k} d_{ii} = (n - k)d_{av} \text{ and } d_{av} = \frac{\sum_k V_{batt,k} d_{kk}}{\sum_k V_{batt,k}}$$

$$\text{From (5.45), (5.47) and (5.49) } d_{ii(i \neq k)} = (n - k)d_{av} \frac{\omega_i V_{batt,i}}{\sum_{i \neq k} \omega_i V_{batt,i}} \text{ \& } d_{kk} = d_{av} \frac{\omega_k \sum_k V_{batt,k}}{\sum_k \omega_k V_{batt,k}}$$

$$\text{Where } d_{kk} = d_{av} \text{ when } k=1 \quad (5.50)$$

5.8.3 Control structure

The detailed control structure is shown in Fig. 5.17 where the battery side and the grid side control are separately described. The grid control depends on the type of grid support needed as described in boost mode, e.g. voltage support or frequency support. The dc-side control is composed of: a) control of the boost converter and b) control of the multilevel buck converter. The module boost converters are controlled using a voltage reference ($V_{dc,m}^*$) which is selected by (5.36). The control of multilevel buck converter employs a central dc-bus voltage loop. The output of that controller provides the overall duty ratio (d_{av}) command through an inner dc-link current controller which controls V_{dc} and then this overall duty is split into module duty ratios (d_{ii}) using (5.45) or (5.50). The weighting factor for charging and discharging is different. This change-over of weighting factor between charging and discharging is performed using the sign of i_{sq}^* as shown in Fig. 5.17. The control structure of boost-buck mode is described in Fig. 5.18. The inverter and module control structure are not shown separately because they are similar to Fig. 5.13 and Fig. 5.4.

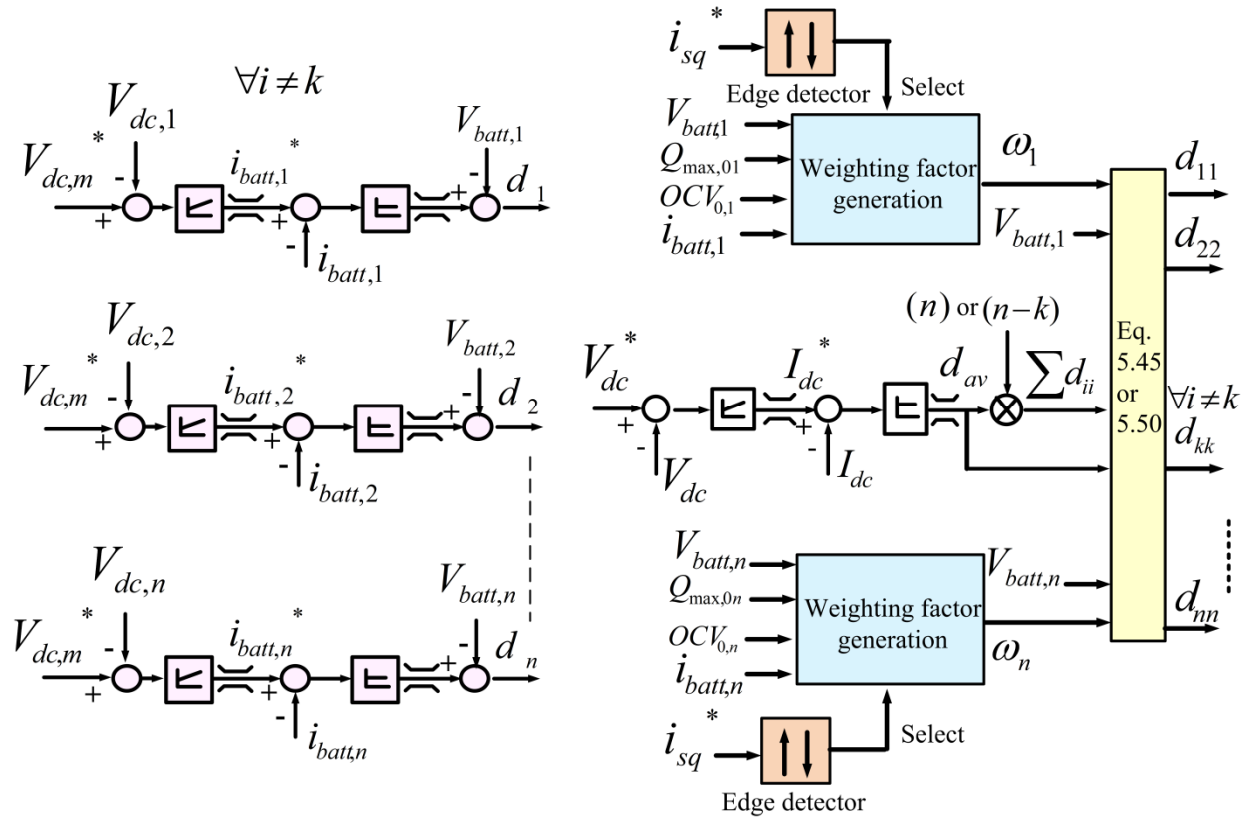


Fig. 5.17 Proposed dc-side control architecture in boost-buck control mode

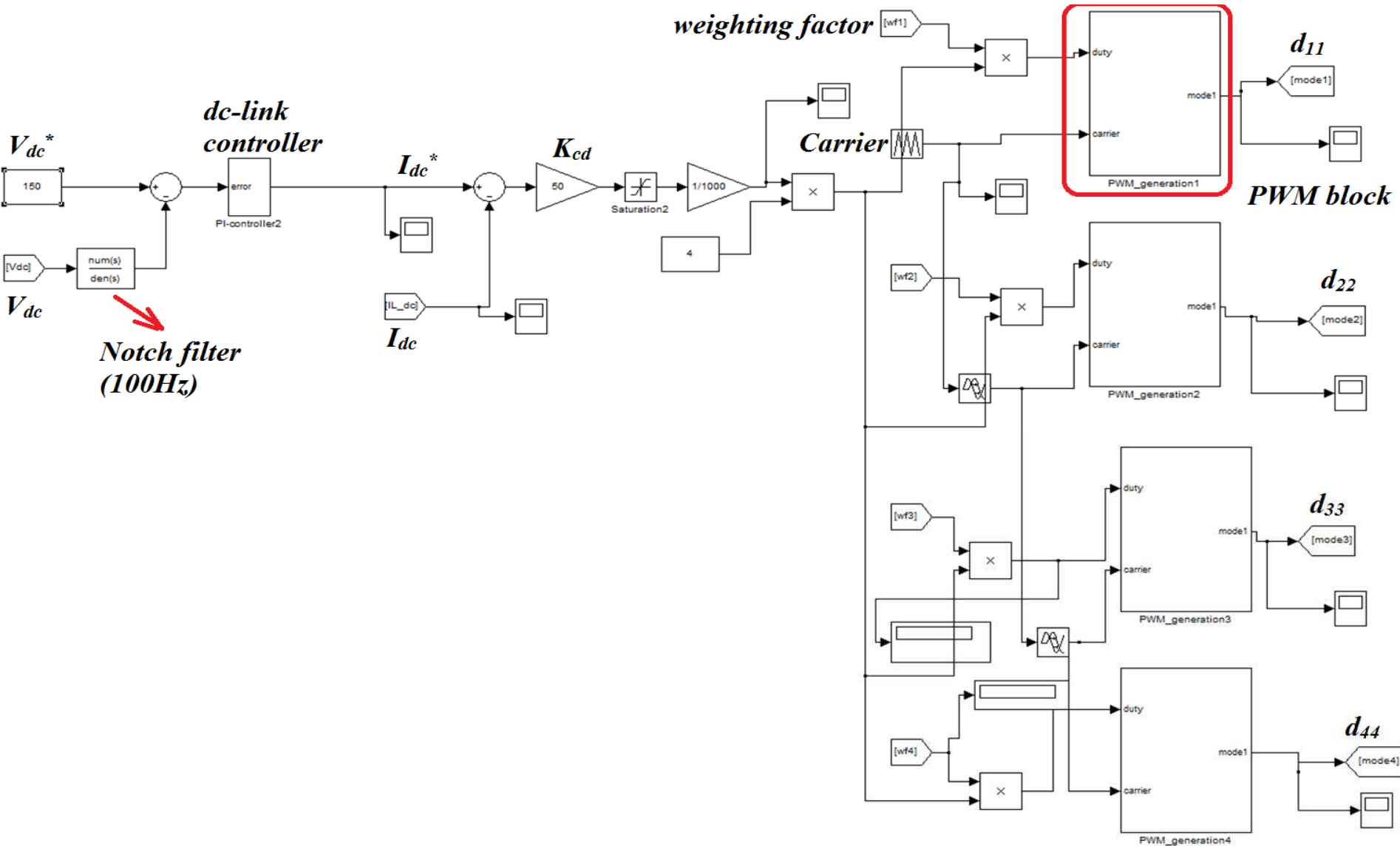


Fig. 5.18 Matlab/Simulink model of the boost-buck control mode

5.9 Experimental validation

It was discussed earlier that the boost mode is only applicable when $\sum V_{batt,i} < V_{dc}^*$, i.e. when all the dc-sources are low voltages while buck mode is mainly for $\sum V_{batt,i} > V_{dc}^*$ and boost-buck mode is applicable for both the conditions: $\sum V_{batt,i} \leq V_{dc}^*$ or $\sum V_{batt,i} > V_{dc}^*$. Due to the battery voltages available, the validation of boost and boost-buck modes are considered to be adequate to validate buck mode because of the control system commonality.

5.9.1 Boost mode

A three-module set-up has been built in order to validate the boost mode as shown in Table 5-1. Constant power command has been used on the grid where appropriate.

Case – 1 zero to discharging transition mode (current dynamics): Fig. 5.19(a) shows the simulation result for distributed control scheme at the moment of connecting to the grid ($t = 0.50s$). It is noted that the module currents are significantly different. The second module shares the highest current while third module shares the lowest current among the three. The current distribution is 1: 1.5: 2.5. The sharing is according to instantaneous state-weightages which are calculated online depending on initial SOC, voltage, and capacity of the module. Fig. 5.19(b) shows the corresponding experimental result at the time of connecting to the grid. The module currents, grid current and steady state values are within 5-10% in simulation and between the experimental result. The details are given in Table 5-2.

Case – 2 zero to charging transition mode (current dynamics): Fig. 5.20(a) shows the simulation result when the converter switches to charging mode at the moment of connecting to the grid ($t = 0.5s$). The second module is charged at a higher current than the remaining modules because it has highest state weightage during the charging mode. Fig. 5.20(b) shows the experimental result in the same operating conditions. It can be seen that the module currents in the charging are less than that of discharging for a fixed grid side current because the magnitudes of the battery voltages are higher when charging. The details are given in Table 5-2.

Case – 3 charging to discharging transition mode (current dynamics): Fig. 5.21(a) shows the simulation result when the converter switches from charging mode to discharging mode at $t=0.5s$. It is important to note that the sharing between the modules is different in charging and in discharging. The first module takes significantly higher current compared to rest of the modules because of higher state-weightage. The steady state values are provided in Table 5-2 with their corresponding state weightages. Fig. 5.21(b) shows the experimental result of mode-switching from charging to discharging mode. It can be observed from that both the results have similar dynamics and steady state values are within 5%.

Case – 4 discharging to charging transition mode (current dynamics): Fig. 5.22(a) shows the simulation result when the converter switches from discharging mode to charging mode. It is to be noted that the three currents are different in discharging mode but when the converter switches to charging mode, module – 1 and module – 2 share similar currents while module – 3 takes the lowest current as expected. The details are given in Table 5-2. Fig. 5.22(b) shows

the corresponding experimental result. Importantly, it can be noticed that the simulation and experimental results have similar dynamics and steady state values.

Case – 5: Module bypassing (current dynamics): Module bypassing could be an important functionality in second life battery applications because of the poor battery reliability. Fig. 5.23 and Fig. 5.24 show the experimental results of module bypassing during charging and discharging mode respectively. In this experiment, module – 3 has been bypassed. Note that the remaining modules immediately take a higher share of the currents to keep the same power.

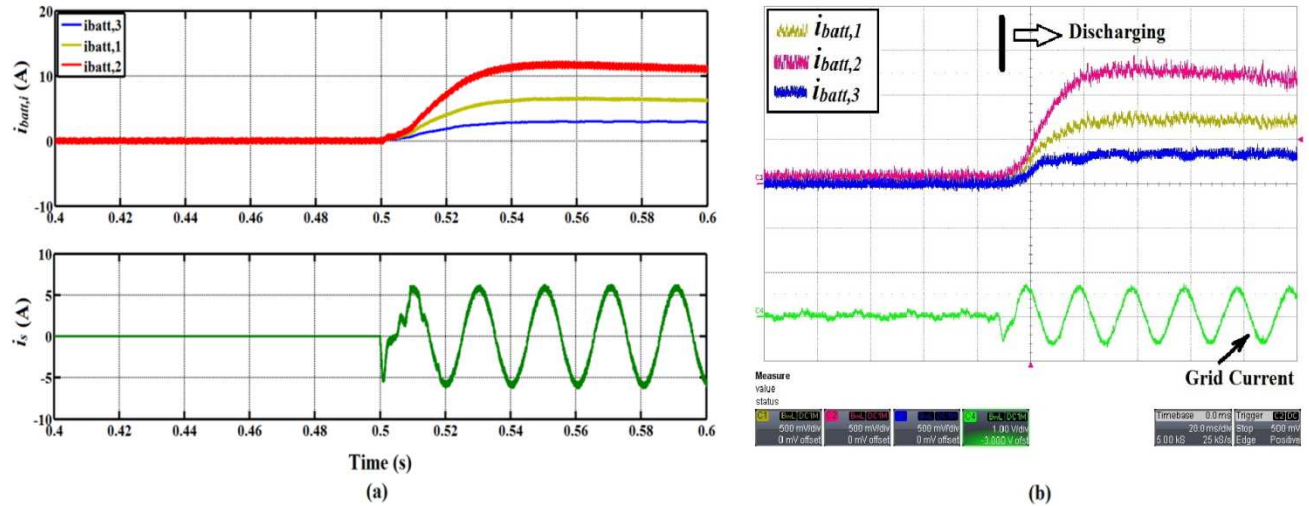


Fig. 5.19 Distributed sharing (current dynamics): a) zero to discharging in simulation, b) zero to discharging in experiment (scale: current 5A/div, time 20ms/div)

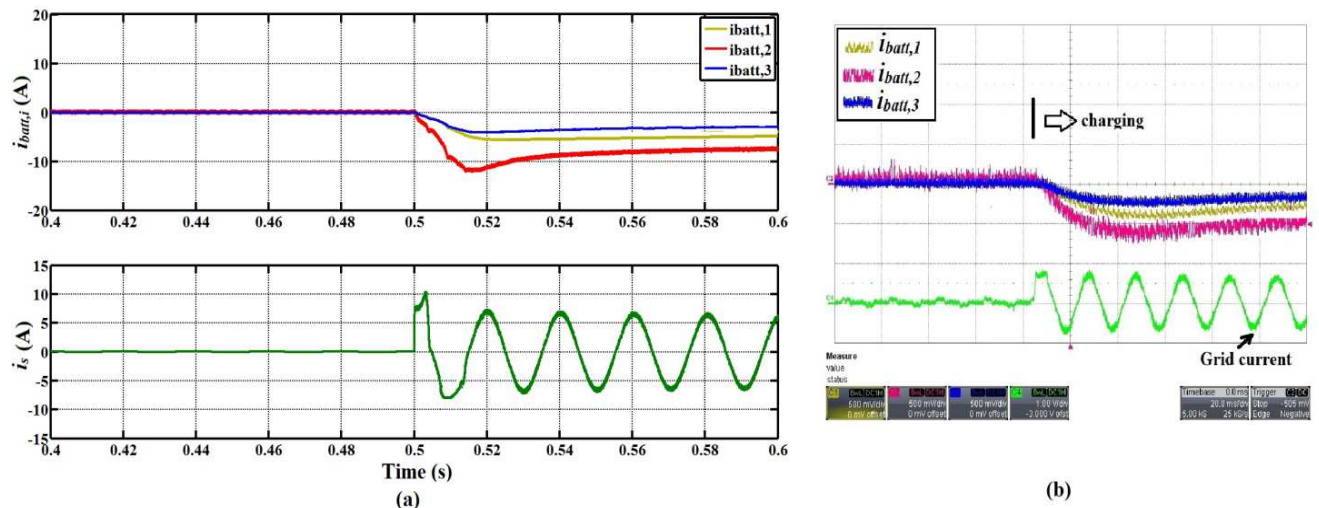


Fig. 5.20 Distributed sharing (current dynamics): a) zero to charging in simulation, b) zero to charging in experiment (scale: current 5A/div, time 20ms/div)

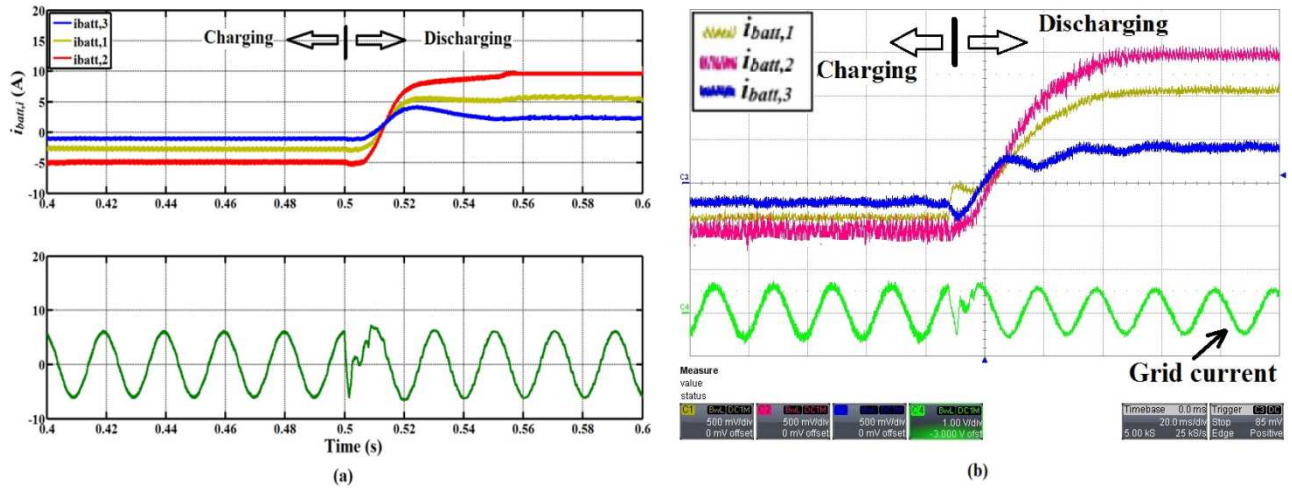


Fig. 5.21 Distributed sharing (current dynamics): a) charging to discharging in simulation, b) charging to discharging in experiment (scale: current 5A/div, time 20ms/div)

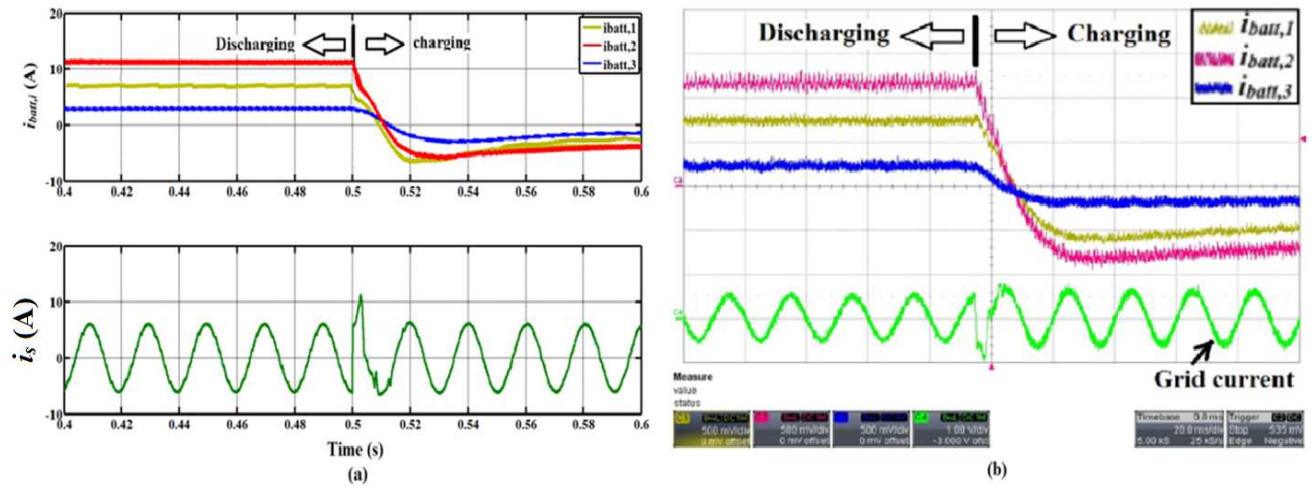


Fig. 5.22 Distributed sharing (current dynamics): a) discharging to charging in simulation, b) discharging to charging in experiment (scale: current 5A/div, time 20ms/div)

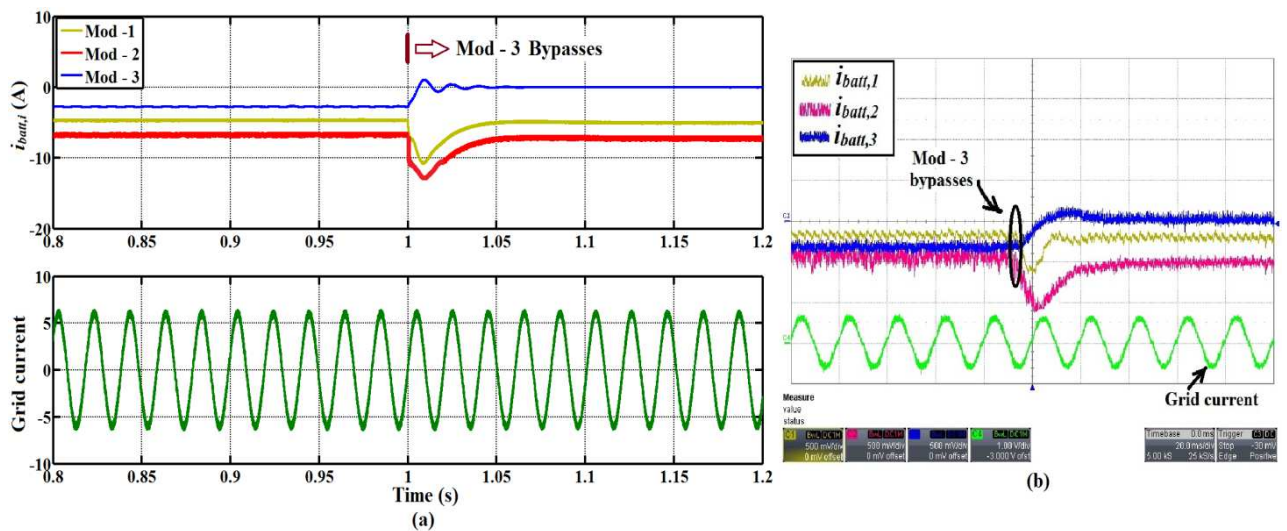


Fig. 5.23 Distributed power sharing under module bypassing in charging mode: a) simulation, b) experimental result

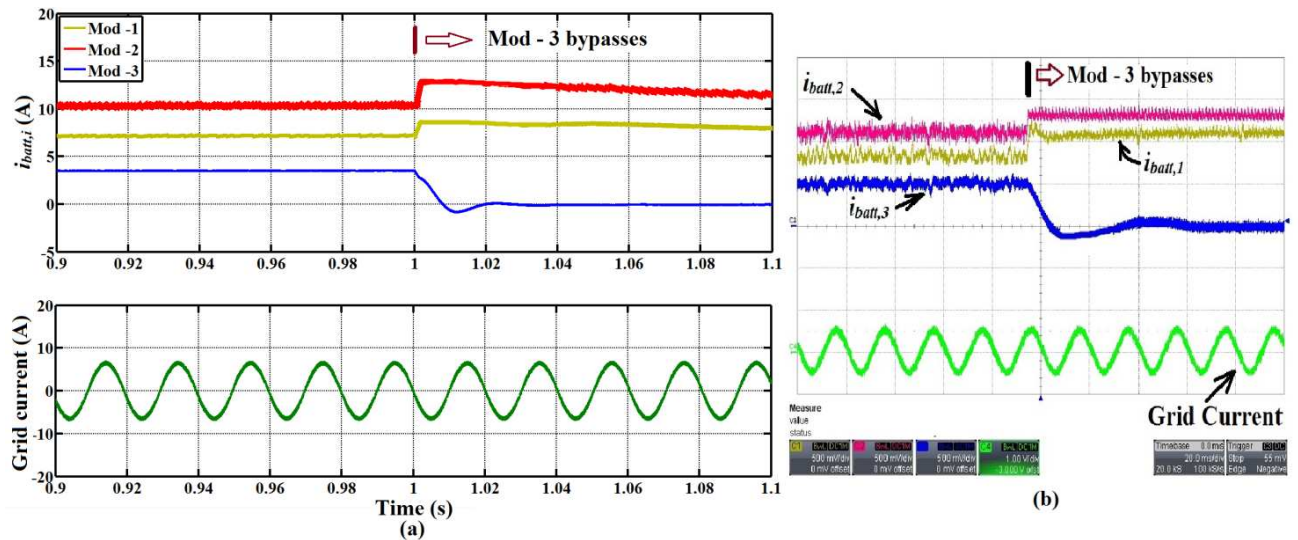


Fig. 5.24 Distributed power sharing under module bypassing in discharging mode: a) simulation, b) experimental result

Fig. 5.25 shows the simulation and experimental results of module dc-link voltage ($V_{dc,i}$) dynamics in the transition from charging to discharging. This result is presented to show how the module dc-link voltages are changed to alter the current sharing as described in the section 5.4.1. It is important to note that the module capacitor voltages ($V_{dc,i}$) are changed dynamically while switching the operational mode. It is also noticeable that module – 2 has the highest module voltage. This is because the nominal voltage of module – 2 (24V) is much higher than the remaining modules.

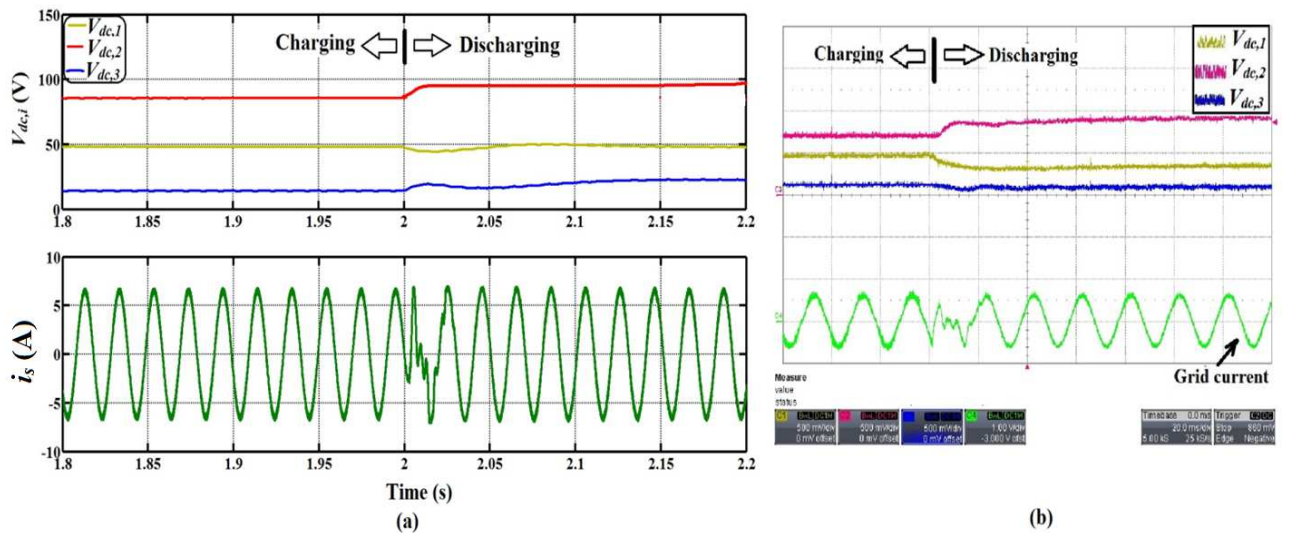


Fig. 5.25 Distributed sharing (voltage dynamics): a) charging to discharging in simulation, b) charging to discharging in experiment (scale: voltage 50V/div, time 20ms/div)

Table 5-1 Operating condition in boost mode

Operating central dc-bus voltage	150V
Experimental Grid voltage	120V (peak)
Grid current	7A (peak)
Battery module – 1	12V, 10Ah lead acid – $V_{max} = 13.8V$ $V_{min} = 9.6V$, $Z_{nom} = 0.015\Omega$
Battery module – 2	24V, 16Ah lead acid – $V_{max} = 29V$ $V_{min} = 19V$, $Z_{nom} = 0.02\Omega$
Battery module – 3	7.2V, 6.5Ah NiMH – $V_{max} = 8.5V$ $V_{min} = 5V$, $Z_{nom} = 0.011\Omega$

Table 5-2 Theoretical and experimental comparison of module currents at an instant in boost mode

Mode of operation	Calculated steady-state module current references	Experimentally measured steady-state module currents	Calculated overall response time (from module voltage controller BW)	Experimental overall response time (from module voltage controller BW)
case - 1:	$i_{batt,1}^* = 6.5A$ $i_{batt,2}^* = 11.5A$ $i_{batt,3}^* = 2.2A$	$i_{batt,1} = 7.0A$ $i_{batt,2} = 12.0A$ $i_{batt,3} = 2.4A$	Module – 1: 16.0ms Module – 2: 16.0ms Module – 3: 16.0ms	Module – 1: 17ms Module – 2: 15ms Module – 3: 15ms
case - 2:	$i_{batt,1}^* = -4.2A$ $i_{batt,2}^* = -7.5A$ $i_{batt,3}^* = -2.5A$	$i_{batt,1} = -4.8A$ $i_{batt,2} = -7.3A$ $i_{batt,3} = -2.4A$	Module – 1: 16.0ms Module – 2: 16.0ms Module – 3: 16.0ms	Module – 1: 18ms Module – 2: 17ms Module – 3: 16ms
case - 3:	$i_{batt,1}^* = 10.0A$ $i_{batt,2}^* = 15A$ $i_{batt,3}^* = 2.5A$	$i_{batt,1} = 11A$ $i_{batt,2} = 14.5A$ $i_{batt,3} = 3A$	Module – 1: 16.0ms Module – 2: 16.0ms Module – 3: 16.0ms	Module – 1: 18ms Module – 2: 17ms Module – 3: 16ms
case - 4:	$i_{batt,1}^* = -5A$ $i_{batt,2}^* = -4.8A$ $i_{batt,3}^* = -2.9A$	$i_{batt,1} = -5A$ $i_{batt,2} = -5A$ $i_{batt,3} = -3.0A$	Module – 1: 16.0ms Module – 2: 16.0ms Module – 3: 16.0ms	Module – 1: 18ms Module – 2: 17ms Module – 3: 17ms

5.9.2 Boost-buck mode

A Four-module or five-level hybrid battery energy storage system has been built as shown in Fig. 5.26 and tested in a grid connected condition to validate the proposed control. The line inverter was controlled to a fixed power demand. Different modules contain different types of battery in terms of voltage, capacity as shown in Table 5-3. One of the batteries (module – 2) is significantly larger (in terms of capacity) than the others to show the benefit of being able to operate in boost-buck mode in terms of battery current control range.

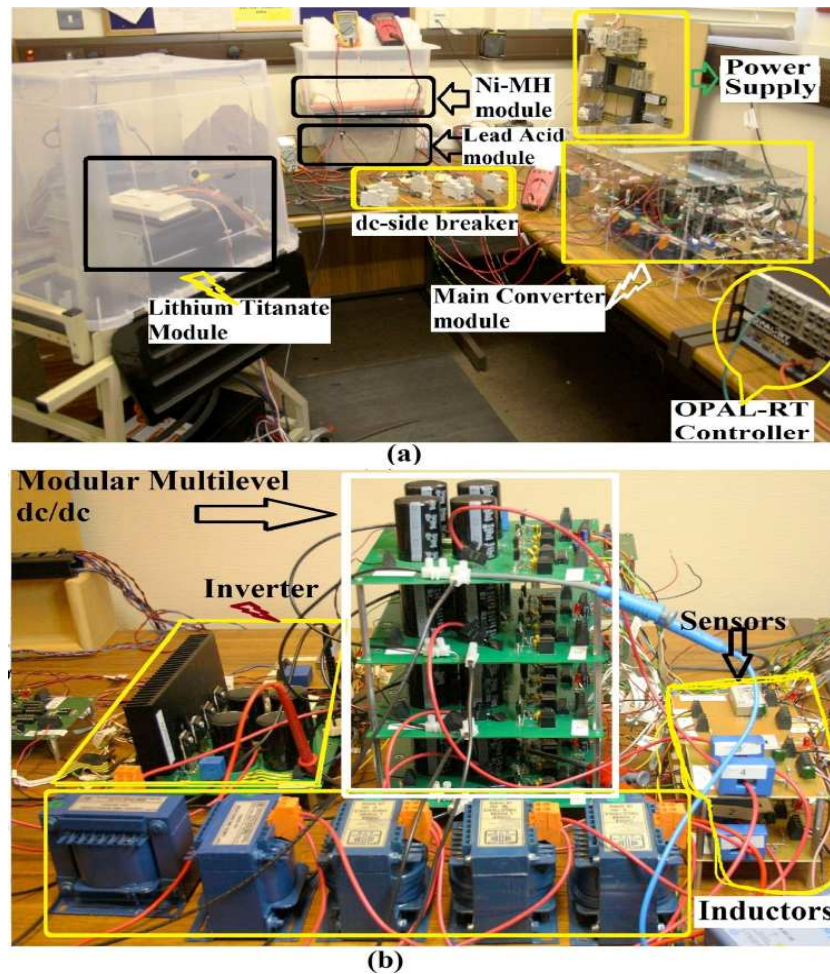


Fig. 5.26 Laboratory built multi-modular converter based hybrid battery energy storage system

Case – 1 zero to discharging mode (current dynamics): Fig. 5.27 shows the simulation and experimental results for the distributed control scheme at the moment of connecting to the grid. Table 5-4 shows the comparison of desired and measured module currents along with their initial conditions. It can be seen that module currents are almost in 1:10 ratio and the converter is able to maintain such widely different current levels.

Case – 2 zero to charging mode (current dynamics): Fig. 5.28 shows the simulation and experimental result when the converter switches to charging mode. The second module is charged at a significantly higher current than the remaining modules. Module currents are wide different (1:20 ratio exists between the highest and lowest module currents). The steady state values of module currents are presented in Table 5-4.

Case – 3 charging to discharging mode (current dynamics): Fig. 5.29 shows the simulation and experimental result when the converter switches from charging mode to discharging mode. It is important to note that the sharing between the modules is different in charging and in discharging. The details are given in Table 5-4.

Case – 4 discharging to charging mode (current dynamics): Fig. 5.30 shows the simulation and experimental result when the converter switches from discharging mode to charging mode. It is to be noted that the all the module currents in charging and discharging mode are

different due to the differences in weighting functions between the two modes. Importantly, the current sharing changes after switching from discharging to charging mode.

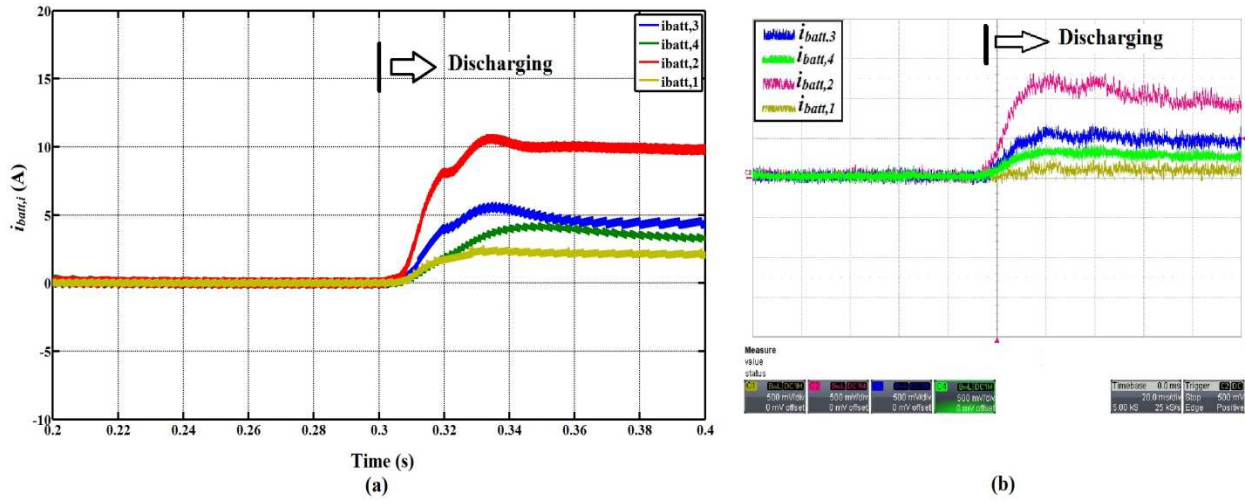


Fig. 5.27 Distributed current sharing: a) zero to discharging in simulation, b) zero to discharging in experiment (scale: current 5A/div, time 20ms/div)

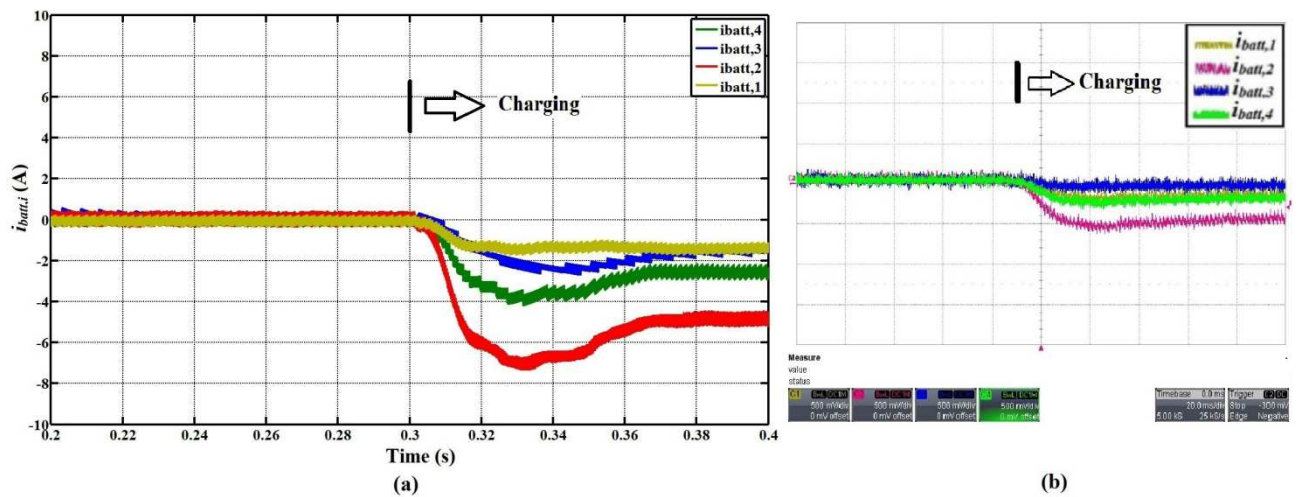


Fig. 5.28 Distributed current sharing: a) zero to charging in simulation, b) zero to charging in experiment (scale: current 5A/div, time 20ms/div)

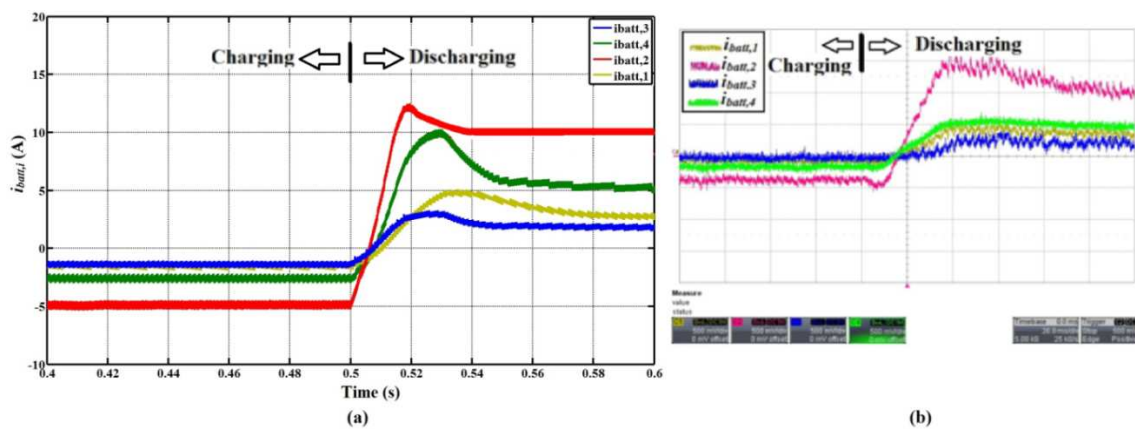


Fig. 5.29 Distributed current sharing: a) charging to discharging in simulation, b) charging to discharging in experiment (scale: current 5A/div, time 20ms/div)

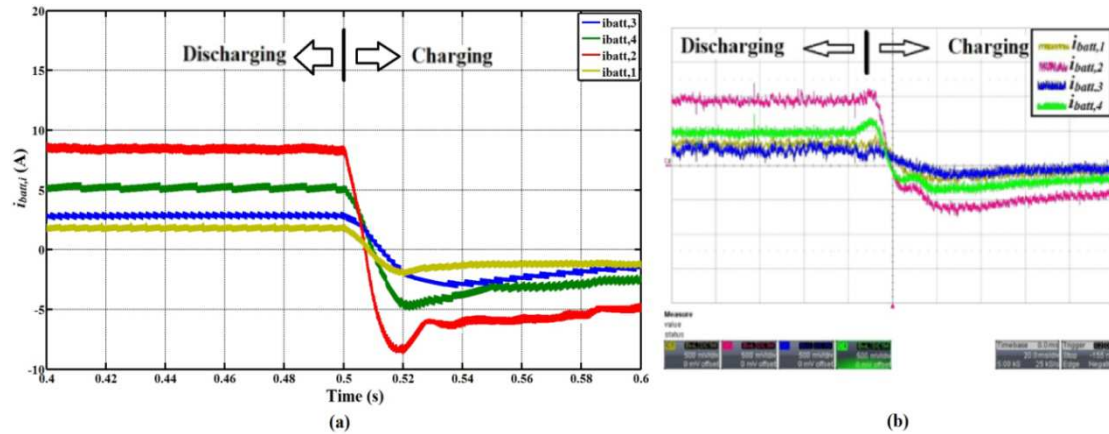


Fig. 5.30 Distributed current sharing: a) discharging to charging in simulation, b) discharging to charging in experiment (scale: current 5A/div, time 20ms/div)

Fig. 5.31 shows the simulation and experimental results of module bypassing during discharging. In this experiment, module – 4 has been bypassed. The remaining modules clearly take a higher share of the currents to keep the power. Momentarily drop in the currents occur due to sudden dips in V_{dc} which causes d_{av} to drop and subsequently $\sum d_{ii}$ to change suddenly. However, it recovers quickly due to having a central dc-link voltage loop as shown in Fig. 5.17. This shows the converter is capable of bypassing a faulty module without interrupting the overall system operation.

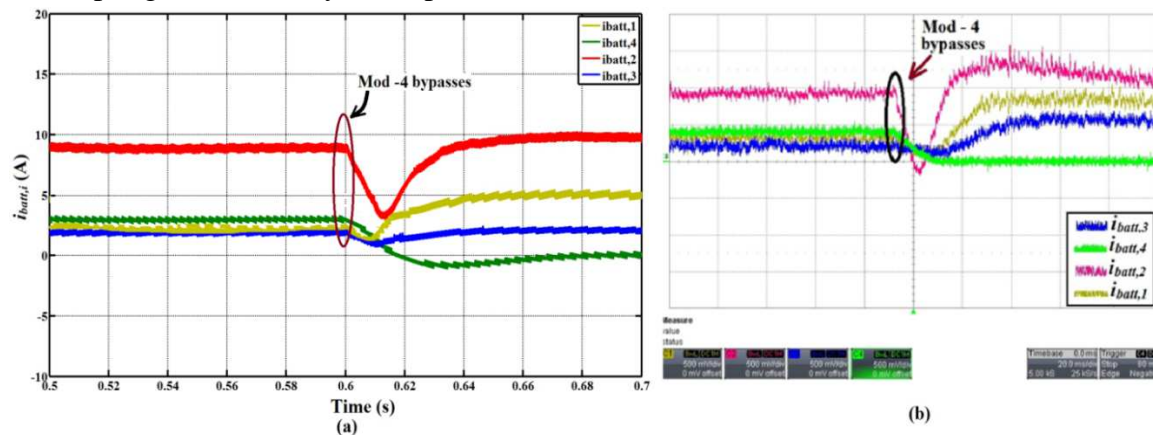


Fig. 5.31 Module bypassing during simulation: a) in simulation, b) in experiment (scale: current 5A/div, time 20ms/div)

Table 5-3 Operating condition in boost-buck mode

module dc-link voltage ($V_{dc,m}$)	80V
Operating central dc-bus voltage (V_{dc})	150V
Nominal Grid voltage (V_s)	120V (peak)
Test power command (P)	450W
Battery module – 1	12V, 10Ah lead acid – $V_{max} = 14V$ $V_{min} = 9.5V$, $Z_{nom} = 0.015\Omega$
Battery module – 2 (From Altairnano)	24V, 60Ah lithium titanate – $V_{max} = 27V$ $V_{min} = 18V$, $Z_{nom} = 0.02\Omega$
Battery module – 3 (From Honda-Insight)	7.2V, 6.5Ah NiMH, $V_{max} = 8.5V$, $V_{min} = 5V$, $Z_{nom} = 0.011\Omega$
Battery module – 4	24V (2x12V), 16Ah lead acid – $V_{max} = 18V$ $V_{min} = 28V$, $Z_{nom} = 0.024\Omega$

Table 5-4 Theoretical and experimental comparison of module currents in boost mode

Cases	Initial SOC before changing a mode	Calculated current references	Experimentally measured steady-state module currents
Case – 1	SOC _{O1} =38% SOC _{O2} =46% SOC _{O3} =88% SOC _{O4} =55%	$i_{batt,1}^* = 1.5A$ $i_{batt,2}^* = 11.5A$ $i_{batt,3}^* = 3A$ $i_{batt,4}^* = 3.9A$	$i_{batt,1} = 1.3A$ $i_{batt,2} = 10A$ $i_{batt,3} = 2.5A$ $i_{batt,4} = 3.5A$
Case – 2	SOC _{O1} =73.4% SOC _{O2} =70.9% SOC _{O3} =68.7% SOC _{O4} =62.0%	$i_{batt,1}^* = - 0.6A$ $i_{batt,2}^* = - 6.1A$ $i_{batt,3}^* = - 0.48A$ $i_{batt,4}^* = - 2.0A$	$i_{batt,1} = - 0.5A$ $i_{batt,2} = - 5A$ $i_{batt,3} = - 0.55A$ $i_{batt,4} = - 1.8A$
Case – 3	SOC _{O1} =83.8% SOC _{O2} =78% SOC _{O3} =76% SOC _{O4} =72.4%	$i_{batt,1}^* = 2.3A$ $i_{batt,2}^* = 9.5A$ $i_{batt,3}^* = 1A$ $i_{batt,4}^* = 3.2A$	$i_{batt,1} = 2.6A$ $i_{batt,2} = 9.6A$ $i_{batt,3} = 1.5A$ $i_{batt,4} = 3A$
Case – 4	SOC _{O1} =63% SOC _{O2} =66.0% SOC _{O3} =73% SOC _{O4} =52.6%	$i_{batt,1}^* = - 0.9A$ $i_{batt,2}^* = - 4.8A$ $i_{batt,3}^* = - 0.5A$ $i_{batt,4}^* = - 2.1A$	$i_{batt,1} = - 0.7A$ $i_{batt,2} = - 4.8A$ $i_{batt,3} = - 0.4A$ $i_{batt,4} = - 1.9A$

5.9.3 Charging and discharging trajectory

The charging/discharging trajectory results in chapter – 4 were shown for the boost mode of operation. These are replicated for the boost-buck mode for completeness due to the differences in the control system. All the modules were started at different initial *SOC* and/or voltage levels at the start. The converter was run for a long time using the distributed strategy. The estimated state-of-charge (*SOC*) is plotted during discharging and charging respectively. Fig. 5.32 and Fig. 5.33 show the experimental results for charging and discharging respectively under normal condition. It can be seen that the module with a lower initial *SOC* has a larger slope compared to the module with a higher initial *SOC* during charging and vice-versa during discharging. It can also be seen that all modules *SOC*'s reach their limits at around the same time using the boost-buck mode. There is some nonlinearity has been found in the estimated *SOC* at the beginning of charging and discharging process. This happens because the power sharing and weighting factor calculation described in chapter – 4 are based on the assumption that *SOC* – *OCV* curve is a straight-line. However, it may not be always the case in full *SOC* range or for some battery types (e.g. Li- ion). However, it can be made linear if a non-linear *SOC* – *OCV* relationship has been considered in the weighting factor calculation. Future research work would consider this issue in more detailed.

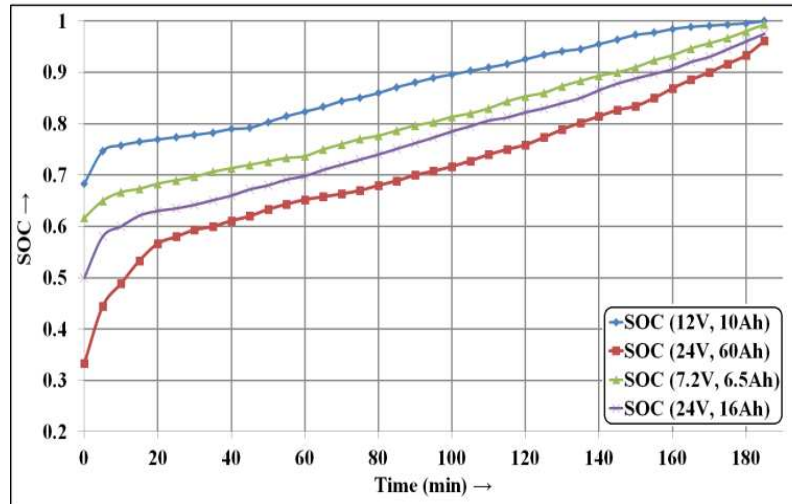


Fig. 5.32 Experimental results of charging trajectory

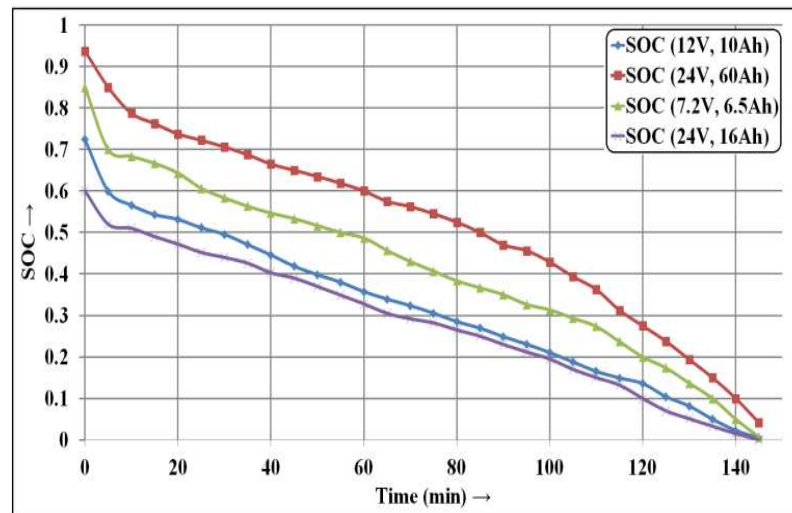


Fig. 5.33 Experimental results of discharging trajectory

It can be seen from the experimental results that the theoretically calculated values are within $\pm 10\%$ both in terms of steady-state and transient values. The hybrid battery modules are utilised according to their instantaneous characteristics and the module currents dynamically change depending on the corresponding battery parameters during charging/discharging in order to optimally utilise the modules. Moreover the proposed strategy is capable of detecting the battery failure and is able to bypass the corresponding module without interrupting the overall energy storage operation.

5.10 Comparison between different control modes

It was found from the previous sections that each operational mode of the modular converter (boost, buck or boost-buck) has a different operational envelop and different switching strategy which gives rise to different applications, different control flexibility, different converter utilisation as well as different power losses.

Among the different modes the comparison between the buck mode and the boost-buck mode is possible because they can be applied for the same application ($\sum V_{batt,i} > V_{dc}^*$). On

the other hand, a direct comparison between boost and boost-buck mode is possible because of the similar reason. A comparison between the boost and boost-buck mode is performed here.

Under distributed utilisation of hybrid battery modules, different battery modules need to be charged or discharged according to their state-weightage or weighting factors. In case where the weighting factors are widely different (different batteries with widely different capacity or SOC), the module currents could be substantially different. Therefore, the distributed control should have the capability to force the currents according to desired magnitude as well as should able to maintain a fixed dc-bus for the line side inverter. This allows an investigation into the control range of each mode to be undertaken.

To order to perform a comparison, the range of $i_{batt,i}$ is investigated. In a cascaded boost mode, the lower limit of $i_{batt,i}$ is limited by the common dc-link current I_{dc} (due to boost operation) and the upper limit of $i_{batt,i}$ is limited by the maximum allowable switch stress/boost ratio of a module. Therefore, the range of operation of module current in boost mode can be written as shown in (5.44).

$$V_{dc,i}I_{dc} = V_{batt,i}i_{batt,i} \rightarrow I_{dc} \leq i_{batt,i} \leq \frac{V_{sw}}{V_{batt,i}}I_{dc} \quad (5.44)$$

On the other hand, in boost-buck mode the module currents can be controlled in wider range compared to boost mode. In this case, the upper limit of $i_{batt,i}$ is limited by the maximum switch stress/boost ratio of a module while there is no lower limit as shown in (5.45). This means a module current can be controlled as low as it is desired to be. Therefore, it can be concluded that the range of battery currents allowable within a boost-buck system is higher.

$$V_{dc,i}(d_{ii})I_{dc} = V_{batt,i}i_{batt,i} \rightarrow 0 \leq i_{batt,i} \leq \frac{V_{sw}}{V_{batt,i}}I_{dc} \quad (5.45)$$

The limitation of the boost mode can be shown in Fig. 5.34 and Fig. 5.35 for a zero to discharge step change, with widely varying weighting functions cause the minimum current rating from (5.44) to be breached. A comparison with boost-buck mode is shown alongside when i_{batt} range is significantly different. It can be seen from Fig. 5.34(a) and Fig. 5.35(a) that the boost mode cannot utilise the modules appropriately because the module currents are limited by I_{dc} which contains a 100Hz component. This is because the single-phase power always contains a double frequency ac-component (2x line frequency, e.g. for 50Hz grid system, 100Hz component) super-imposed with the average component. This double frequency component appears in the dc-current and in the dc-link voltage. Even though the state-weightages of all the modules are different (as shown in Table 5-5), the same currents flow through module – 1, module – 3 and module – 4. However, it can be seen that from Fig. 5.34(b) and Fig. 5.35(b) boost-buck utilises the modules properly and forces different currents to different modules (as shown in Table 5-6).

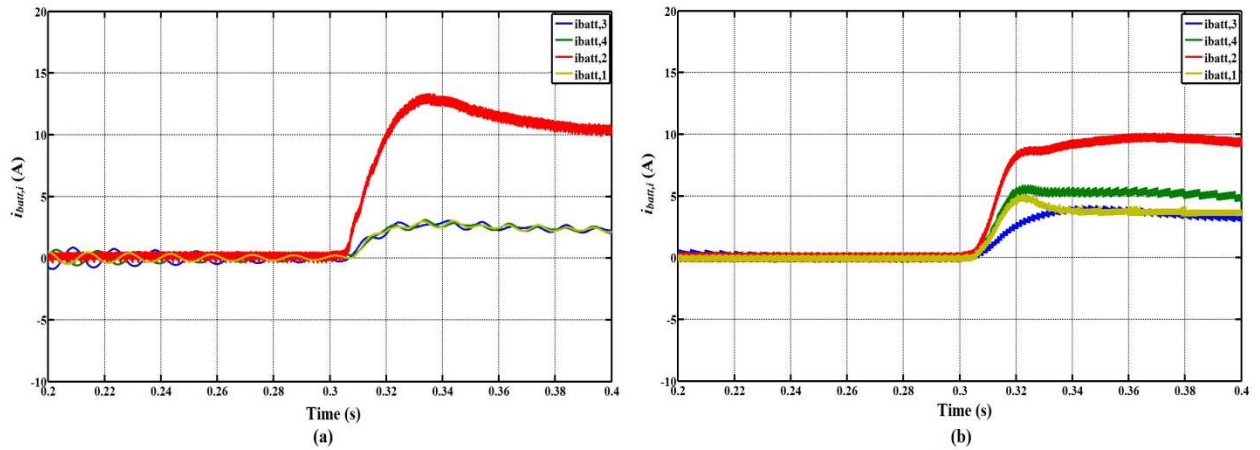


Fig. 5.34 Simulation comparison in discharging mode: a) boost mode, b) boost-buck mode

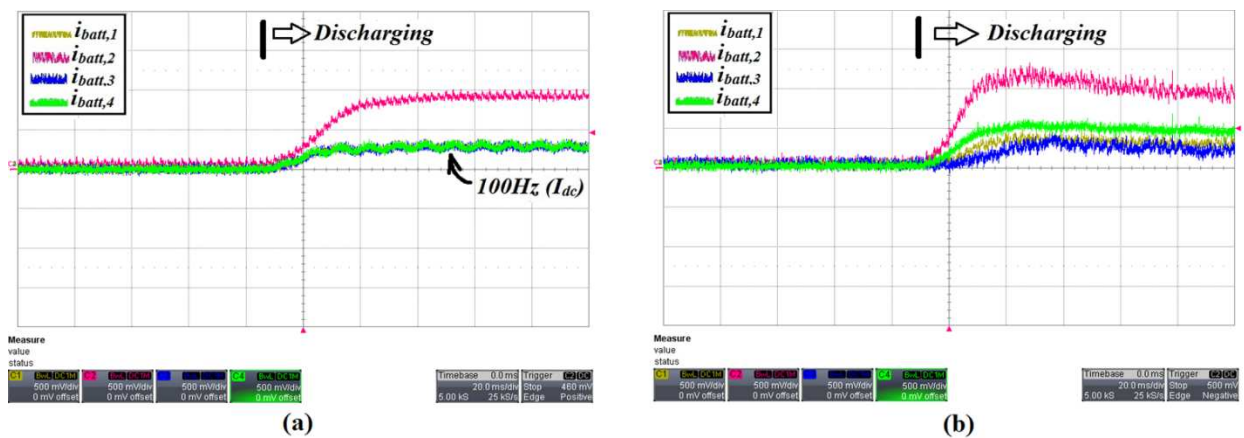


Fig. 5.35 Experimental comparison in discharging mode: a) boost mode, b) boost-buck mode (scale: current 5A/div, time 20ms/div)

A similar set of results can be obtained for zero charging, discharging to charging and charging to discharging conditions also. Fig. 5.36 and Fig. 5.37 show the simulation and experimental results for distributed control scheme at the moment of connecting to the grid in charging mode using boost and boost-buck control modes. It can be seen from Fig. 5.36(a) and Fig. 5.37(a) that the boost mode fails to utilise the modules appropriately because the module currents are limited by I_{dc} which contains 100Hz component. Even though the state-weights of all the modules are different (as shown in Table 5-5), the same currents flow through module – 1, module – 3 and module – 4. However, it can be seen that from Fig. 5.36(b) and Fig. 5.37(b) boost-buck utilises the modules properly and forces different currents to different modules (as shown in Table 5-6). Fig. 5.38 and Fig. 5.39 show the simulation and experimental result when the converter switches from charging mode to discharging mode. Fig. 5.40 and Fig. 5.41 show the simulation and experimental result when the converter switches from discharging mode to charging mode.

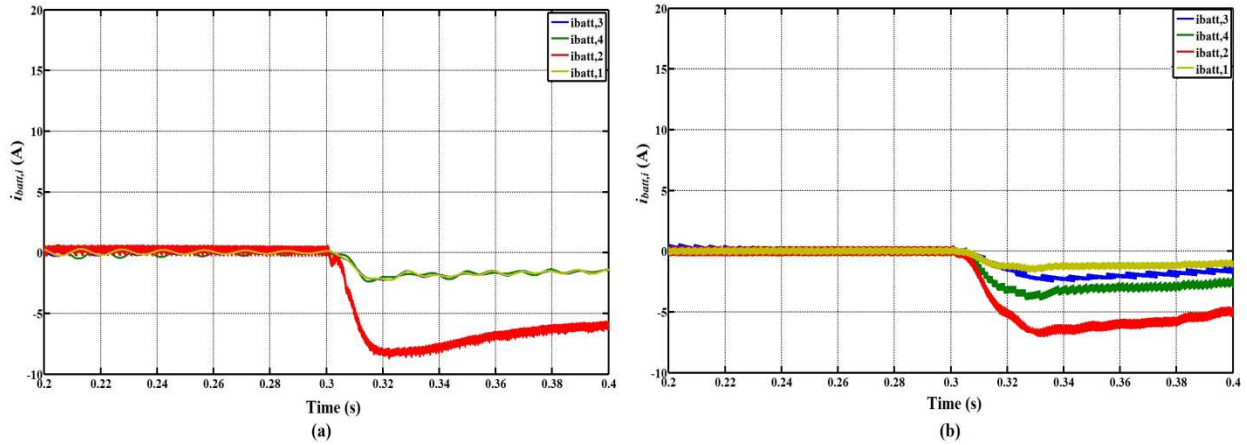


Fig. 5.36 Simulation comparison in charging mode: a) boost mode, b) boost-buck mode

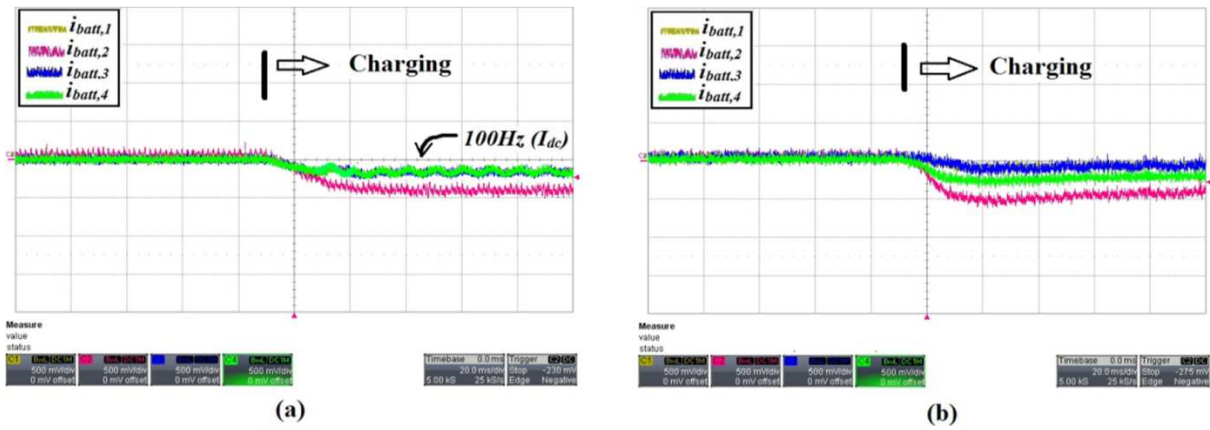


Fig. 5.37 Experimental comparison in charging mode: a) boost mode, b) boost-buck mode (scale: current 5A/div, time 20ms/div)

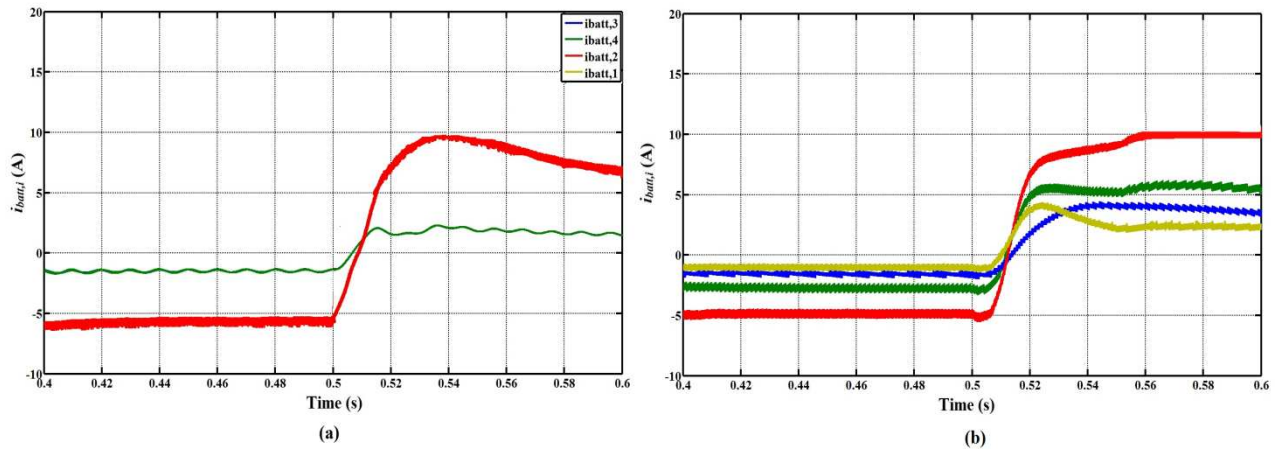


Fig. 5.38 Simulation comparison in charging to discharging mode: a) boost mode, b) boost-buck mode

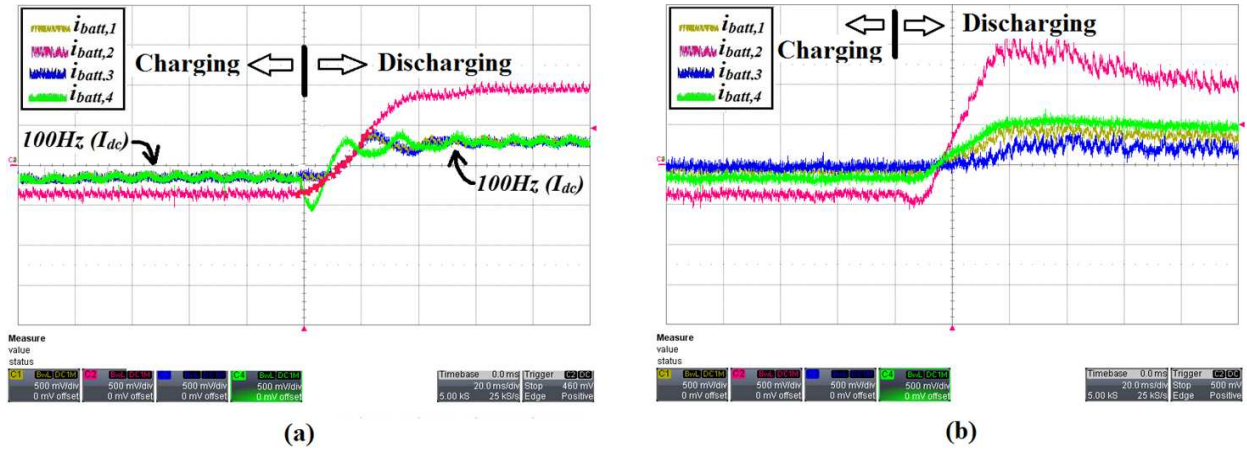


Fig. 5.39 Experimental comparison in charging to discharging mode: a) boost mode, b) boost-buck mode (scale: current 5A/div, time 20ms/div)

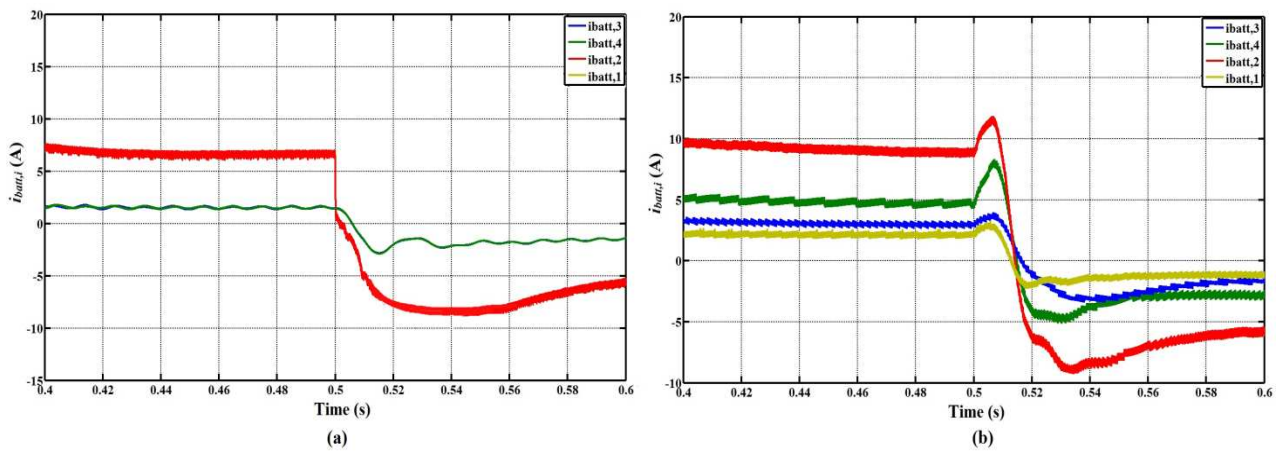


Fig. 5.40 Simulation comparison in discharging to charging mode: a) boost mode, b) boost-buck mode

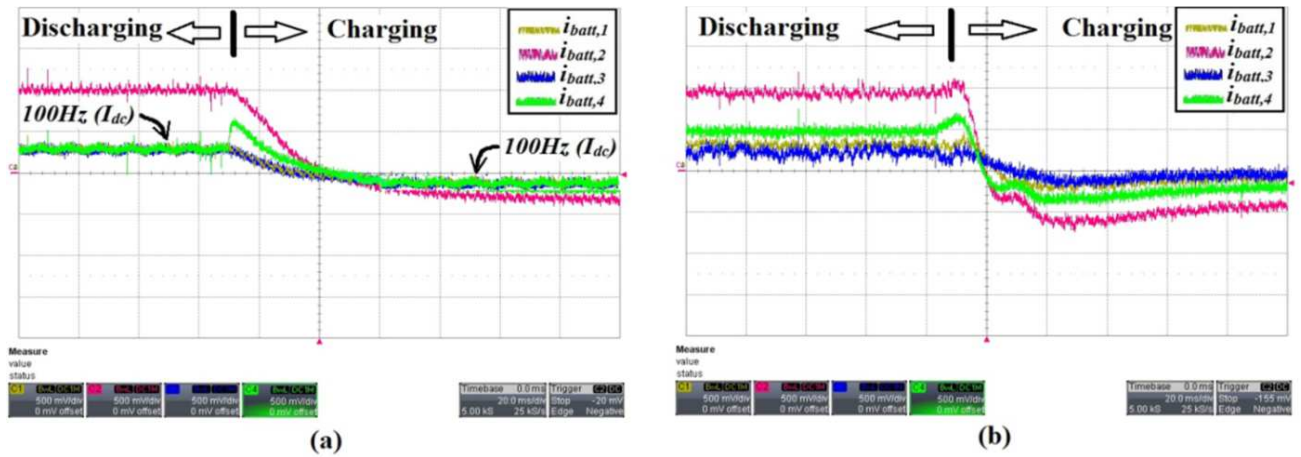


Fig. 5.41 Experimental comparison in discharging to charging mode: a) boost mode, b) boost-buck mode (scale: current 5A/div, time 20ms/div)

Table 5-5 Comparison of theoretical and experimental values of module currents in boost mode

Cases	Desired current ratio $\omega_1 : \omega_2 : \omega_3 : \omega_4$	Calculated current references	Actual current ratio $\omega_1 : \omega_2 : \omega_3 : \omega_4$	Experimentally measured steady-state module currents
Case – 1	1.38: 6.94: 1: 3.05	$i_{batt,1}^* = -1A$ $i_{batt,2}^* = -5A$ $i_{batt,3}^* = -0.72A$ $i_{batt,4}^* = -2.2A$	1: 3.2 : 1 : 1	$i_{batt,1} = -1.5A$ $i_{batt,2} = -4.8A$ $i_{batt,3} = -1.5A$ $i_{batt,4} = -1.5A$
Case – 2	1.75: 12: 1: 2.75	$i_{batt,1}^* = 1.5A$ $i_{batt,2}^* = 9.6A$ $i_{batt,3}^* = 0.8A$ $i_{batt,4}^* = 2.2A$	1: 3.82 : 1 : 1	$i_{batt,1} = 2.5A$ $i_{batt,2} = 9.55A$ $i_{batt,3} = 2.5A$ $i_{batt,4} = 2.5A$
Case – 3	1.42: 9.69: 1: 2.24	$i_{batt,1}^* = 1.4A$ $i_{batt,2}^* = 9.5A$ $i_{batt,3}^* = 0.98A$ $i_{batt,4}^* = 2.2A$	1: 3.84 : 1 : 1	$i_{batt,1} = 2.5A$ $i_{batt,2} = 9.6A$ $i_{batt,3} = 2.5A$ $i_{batt,4} = 2.5A$
Case – 4	1.42: 9.69: 1: 2.24	$i_{batt,1}^* = -1.1A$ $i_{batt,2}^* = -5A$ $i_{batt,3}^* = -0.8A$ $i_{batt,4}^* = -2.1A$	1: 3.2 : 1 : 1	$i_{batt,1} = -1.5A$ $i_{batt,2} = -4.8A$ $i_{batt,3} = -1.5A$ $i_{batt,4} = -1.5A$

Table 5-6 Comparison of theoretical and experimental values of module currents in boost-buck mode

Cases	Desired current ratio $\omega_1 : \omega_2 : \omega_3 : \omega_4$	Calculated current references	Actual current ratio $\omega_1 : \omega_2 : \omega_3 : \omega_4$	Experimentally measured steady-state module currents
Case – 1	1.25: 12.7: 1: 4.16	$i_{batt,1}^* = -0.6A$ $i_{batt,2}^* = -6.1A$ $i_{batt,3}^* = -0.48A$ $i_{batt,4}^* = -2.0A$	0.9: 9.1 : 1 : 3.27	$i_{batt,1} = -0.5A$ $i_{batt,2} = -5A$ $i_{batt,3} = -0.55A$ $i_{batt,4} = -1.8A$
Case – 2	1.5: 9.6: 1: 2.1	$i_{batt,1}^* = 1.5A$ $i_{batt,2}^* = 9.6A$ $i_{batt,3}^* = 1A$ $i_{batt,4}^* = 2.1A$	1.42: 7 : 1 : 1.8	$i_{batt,1} = 2.0A$ $i_{batt,2} = 9.7A$ $i_{batt,3} = 1.4A$ $i_{batt,4} = 2.6A$
Case – 3	2.3: 9.5: 1: 3.2	$i_{batt,1}^* = 2.3A$ $i_{batt,2}^* = 9.5A$ $i_{batt,3}^* = 1A$ $i_{batt,4}^* = 3.2A$	1.73: 6.4 : 1 : 1	$i_{batt,1} = 2.6A$ $i_{batt,2} = 9.6A$ $i_{batt,3} = 1.5A$ $i_{batt,4} = 3A$
Case – 4	1.8: 9.6: 1: 4.2	$i_{batt,1}^* = -0.9A$ $i_{batt,2}^* = -4.8A$ $i_{batt,3}^* = -0.5A$ $i_{batt,4}^* = -2.1A$	1.75: 12 : 1 : 4.75	$i_{batt,1} = -0.7A$ $i_{batt,2} = -4.8A$ $i_{batt,3} = -0.4A$ $i_{batt,4} = -1.9A$

5.10.1 Overall comparison and Selection of control mode

Table 5-7 shows a summary of the comparison between the boost and boost-buck mode. It can be seen from the table that the boost-buck mode is more versatile in terms of application and control range. However, it gives rise to lower efficiency compared to the other modes (at least 2 – 3% lower). In many applications where widely heterogeneous batteries could be present (widely different weighting factors), the boost-buck control mode is the most practical mode of operation. However, in the specific application where all LV batteries or all HV modules with similar characteristics (or similar weighting factors) are present, boost or buck mode should be chosen over boost-buck mode respectively in order to achieve higher converter efficiency. Therefore, the choice of control mode is dependent on the weighting factors as well as on the application. Table 5-7 shows the overall comparison of different control modes of the converter. Such comparison helps a designer to find suitable control architecture depending on available set of batteries.

Table 5-7 Overall comparison

Control mode	Applicability	Control range (the range of $i_{batt,i}$)	DC-side Peak Efficiency (from chapter – 3)
Boost	$(\sum V_{batt,i} \leq V_{dc}^*)$	$(I_{dc} \leq i_{batt,i} \leq \frac{V_{sw}}{V_{batt,i}} I_{dc})$	around 97 – 98%
Buck	$(\sum V_{batt,i} \geq V_{dc}^*)$	$(0 \leq i_{batt,i} \leq I_{dc})$	around 97 – 98%
Boost-buck	$(\sum V_{batt,i} \geq V_{dc}^*)$ or $(\sum V_{batt,i} \leq V_{dc}^*)$	$(0 \leq i_{batt,i} \leq \frac{V_{sw}}{V_{batt,i}} I_{dc})$	around 94 – 95%

5.11 Conclusion

This chapter presents the different distributed control architectures needed to operate the proposed converter. To independently utilise each converter module according to their desired weighting function so as to directly integrate any set of hybrid second life batteries in a grid-tie energy storage system. Three control modes have been discussed: a) boost, b) buck and c) boost-buck and their associated control structures have been introduced. A detailed discussion of their applicability, range of control and suitability has been considered. A comparison between the different control modes was performed. Simulation and experimental studies are used to validate each control mode. This application is mainly focused on low voltage grid systems. However, a similar control strategy is valid for medium/high voltage grid applications.

6 Stability Investigation of Distributed Control

6.1 Introduction

The closed loop control structure suggested in the chapter 5, employs cascaded control loops per module: a) an outer voltage control loop and b) an inner current control loop. This chapter investigates more comprehensively any stability issues associated with the control structure both in boost and boost-buck mode and suggests possible mitigation techniques. There are three previous types of studies which are considered similar to the present application: a) modular converter with the same type of sources such as batteries/super-capacitors, b) modular converters with different types of sources such as, PV with battery or wind/PV hybrid system, c) modular converters with the same type of sources under different operating conditions such as, PV panels in partial shading conditions.

In the first case, where the modular converter consists of the same type of sources (batteries/super-capacitors), a converter module balancing strategy was reported to enhance the overall performance of the system [155] – [156]. The differences between the modules were minimal. So, all the module controllers are operated in the similar fashion. Since batteries with similar nature with known parameters were considered, the parameter variation had not been looked at. As a result, no module based and module-to-module control stability issues was found in the literature due to parameter variation

In the second type of study, an energy management strategy between the multiple sources is of some relevance to this work. Mainly the grid side converter control has been emphasized [365] – [369] and the power mismatch between the multiple sources produces line side voltage and frequency stability problem depending on the R/X ratio of the network. This issue was addressed and was handled by employing energy storage systems in parallel to the central inverter dc-link to smooth out the power oscillations if any. The grid impedance variation was found to be one of the significant reasons for the inverter instability. This grid stability was handled by an adaptive control strategy as reported in [372] – [373] which adaptively tunes the controller parameters in accordance with the variation of grid impedance. However, in those studies, no stability problems were found between multiple types of sources due to their individual parameter variation.

In the third type of studies, distributed MPPT control of cascaded dc-dc converter based PV systems has been investigated as most closely related to the work in this thesis. A weighting factor based strategy similar to the present work was reported [339]. However, the weighting factor was solely based on different radiation conditions where the only variable parameter was the solar irradiation factor. It was reported that the inhomogeneous radiation could only cause improper power sharing among the modules. As the converter modules were controlled according to the MPPT algorithm depending on the irradiation factor and the total dc-bus voltage was controlled by the inverter. No module based or module-module control stability problems were reported for the cascaded dc-dc converter based structure due to the variation

of weighting factor.

There are several researches which discuss the stability aspect of a modular dc-dc converter based system, including interconnection problems such as, the voltage sharing or current sharing issues of input parallel output series (IPOS) or input parallel output parallel (IPOP) based systems [374] – [377]. These researches do not focus on control stability problem but more on the operating stability such as, mitigation of circulating current among the multiple modules, power balancing, and voltage balancing problem or current sharing issues. These researches are not closely linked to the present application because these issues are irrelevant when isolated sources are present and module integrated converters are employed.

The control stability aspect of a modular energy storage system or modular renewable energy system due to uneven power sharing or parameter variation has not been reported in literature as can be discovered. It is an important issue in the modular converter because the uneven power sharing (e.g. voltage/current stress per module) among the modules can affect the overall stability of the converter if there is any stability issue in one module. This makes the guaranteed stability of the distributed control system is a challenging issue.

This chapter investigates the stability issues of the converter under the distributed power sharing based on weighting factor in detailed and discusses why there is a stability issue under certain conditions and how severe this problem can be for the converter. Thereafter, two new control solutions: a) an adaptive PI controller based method and b) a Lyapunov function based method has been proposed to mitigate these stability problem issues while ensuring fast dynamic response. The Lyapunov based distributed control structure for the cascaded boost converters is found to be promising in the present application as it guarantees stability as well as providing a fast dynamic response irrespective of battery operating conditions. On the other hand, the boost-buck mode is found to be more stable than the boost mode of operation. Therefore, the conventional PI-approach is found to be suitable for this mode of operation. A detailed analysis of the stability problem and the proposed control structure has been presented. Supporting simulation and experimental studies have been provided to validate the claims.

6.2 Stability of boost mode

6.2.1 Analysis

The distributed control structure of this converter, as reported in chapter 5, is based on distributed voltage control. The required module voltage references ($V_{dc,1}^*$, $V_{dc,2}^*$... $V_{dc,n}^*$) are generated to allow the control system to share the current according to the desired references ($i_{batt,1}^*$, $i_{batt,2}^*$... $i_{batt,n}^*$). This reference generation is based on a weighting factor (ω_i). The module voltage reference generation is shown in (6.1) – (6.2). Moreover, these module voltage references continue to vary to change the current sharing among the modules because the state-weightage varies when the battery parameter changes according to (6.3).

$$\text{If } i_{batt,i}^* \propto \omega_i, V_{dc,i} I_{dc} = V_{batt,i} i_{batt,i}^* \forall i = 1 \dots n \quad (6.1)$$

$$V_{dc,i}^* \propto V_{batt,i} \omega_i \forall i = 1 \dots n \text{ for a constant } I_{dc} \quad (6.2)$$

$$\sum V_{dc,i}^* = V_{dc}^*, V_{dc,i}^* = V_{dc}^* \frac{\omega_i V_{batt,i} T_i}{\sum_{k=1}^n \omega_k V_{batt,k} T_k} \quad \forall i = 1, n \quad (6.3)$$

Each module consists of two cascaded control loops: a) a slow outer voltage module voltage loop and b) a fast inner current loop. Fig. 5.2(a) shows the cascaded control loop structure. The associated inner current loop delay (e^{-sT_d}) has been taken as four times of the sample time (T_s). The open loop transfer function for the voltage control loop can be derived as shown in (6.4). It can be seen that the open loop transfer function for the module voltage loop $GH_v(s)$ depends $V_{dc,i}$ and $V_{batt,i}$ according to (6.5).

$$GH_v(s) = K_v \left(\frac{1+sT_v}{sT_v} \right) \left(\frac{1}{1+sT_d} \right) \left(\frac{V_{batt,i}}{V_{dc,i}} \right) \left(\frac{1}{sC} \right) \quad (6.4)$$

$$\begin{aligned} \omega_i &= \frac{SOC_i Q_{max,i}}{\sum_{k=1}^n V_{batt,k} SOC_k Q_{max,k}} \text{ for discharging} \\ &= \frac{(1-SOC_i)Q_{max,i}}{\sum_{k=1}^n V_{batt,k}(1-SOC_k)Q_{max,k}} \text{ for charging} \end{aligned} \quad (6.5)$$

Now, with the help of Fig. 5.3(a) the following relation between $V_{dc,i}^*$ and $V_{dc,i}$ can be found.

$$\frac{V_{dc,i}}{V_{dc,i}^*} = \frac{GH_v(s)}{1+GH_v(s)} \quad (6.6)$$

Substituting (6.6) in (6.4) gives,

$$GH_v(s) = K_v \left(\frac{1+sT_v}{sT_v} \right) \left(\frac{1}{1+sT_d} \right) \left(\frac{V_{batt,i}}{\frac{GH_v(s)}{1+GH_v(s)} V_{dc,i}^*} \right) \left(\frac{1}{sC} \right) \text{ Re-arranging gives,}$$

$$\frac{GH_v^2(s)}{1+GH_v(s)} = K_v \left(\frac{1+sT_v}{sT_v} \right) \left(\frac{1}{1+sT_d} \right) \left(\frac{V_{batt,i}}{V_{dc,i}^*} \right) \left(\frac{1}{sC} \right) \quad (6.7)$$

Now solving (6.7) for $GH_v(s)$,

$$GH_v(s) = \frac{F(s) \pm \sqrt{F^2(s) + 4F(s)}}{2} \text{ Where } F(s) = K_v \left(\frac{1+sT_v}{sT_v} \right) \left(\frac{1}{1+sT_d} \right) \left(\frac{V_{batt,i}}{V_{dc,i}^*} \right) \left(\frac{1}{sC} \right) \quad (6.8)$$

It can be seen from (6.8) that variation of ω_i causes $V_{dc,i}^*$ to change and which in turn changes $V_{dc,i}$. This change in $V_{dc,i}$ causes the open loop gain of $GH_v(s)$ to vary which in turn varies the set gain crossover frequency or closed loop bandwidth automatically. This change in gain crossover frequency may result in a control stability problem. However, it is to be noted that the expression (6.8) is not directly solvable for $GH_v(s)$ in terms of 's'. There is no closed form solution of $GH_v(s)$ as a function of weighting factor or in terms of $V_{dc,i}^*$. Therefore, a range of $V_{dc,i}^*$ and $V_{dc,i}$ has been considered to analyse the stability problem.

On the other hand, the inner current loop is shown in Fig. 5.3(b). A proportional controller is considered in the inner current loop for a fast response and stability. The open loop transfer is shown in (6.9) using the expression (5.9) in chapter – 5 where G is the converter gain ($\propto V_{dc,i}$).

$$GH_I(s) = K_{c,i} \frac{1}{G} \frac{i_{batt,i}}{(1-D_i)} \frac{1+s \frac{V_{dc,i}C}{(1-D_i)i_{batt,i}}}{1+s^2 \frac{LC}{(1-D_i)^2}} \quad (6.9)$$

In second life applications, an important issue is parameter variation. In the current context two types of variations have been investigated: a) SOC_i or OCV_i and b) capacity $Q_{max,i}$ because the weighting factor (ω_i) is predominantly a function of these two variables. The variation of any of these two can give rise to sudden/or slow changes in the control bandwidth or system stability margin. This can be explained using the gain crossover frequency or phase margin (PM). Expression (6.10) shows the equation for gain crossover frequency ($\omega_{gc,i}$) and (6.11) shows the expression of PM per converter module. It is important to note that the PM depends on $\omega_{gc,i}$, T_v and T_d . However, for a fixed set of T_v and T_d , the PM is mainly governed by $\omega_{gc,i}$ and it varies with $V_{dc,i}$ or weighting factor (ω_i). Therefore, it can be seen that the designed PM of the converter does not remain to a fixed value throughout a charging or discharging cycle. Due to the presence of the higher order equation, an explicit expression of $\omega_{gc,i}$ is difficult to find and therefore, a frequency response plot or a bode plot has been taken to analyse the effect of variation of stability margin.

$$|GH(j\omega_{gc,i})| = 1 \rightarrow \frac{K_v V_{batt,i}}{T_v V_{dc,i}C} \left(\frac{\sqrt{1+(\omega_{gc,i}T_v)^2}}{(\omega_{gc,i})^2 \sqrt{1+(\omega_{gc,i}T_d)^2}} \right) = 1 \quad (6.10)$$

$$PM = \angle GH_v(j\omega_{gc,i}) + 180^\circ = \tan^{-1} \frac{\omega_{gc,i}(T_v - T_d)}{1 + \omega_{gc,i}^2 T_v T_d} \cong f(\omega_{gc,i}) \quad (6.11)$$

6.2.1.1 Case – 1: Variation of SOC

The state-of-charge (SOC) in the weighting factor is updated in every sample period and can be anything between 0 to 100%. Therefore, a very low SOC at the start, during the operation or during the transition from charging to discharging can cause a reduction of ω_i which in turn increases the open loop gain or gain crossover frequency according to (6.10) because the term $V_{dc,i}$ sits in the denominator of (6.4) and gets influenced by the change in ω_i . This makes the open loop gain $K_v \frac{1}{C} \left(\frac{V_{batt,i}}{V_{dc,i}} \right)$ in (6.4) variable. Fig. 6.1 shows the range of variation of $V_{dc,i}$ and $V_{dc,i}^*$ with the weighting factor. Since $V_{dc,i}^*$ varies with the weighting factor, the voltage $V_{dc,i}$ also varies with the weighting factor. It can be seen that variation of $V_{dc,i}$ is quite higher compared to $V_{batt,i}$ because $V_{sw} \gg V_{batt,i}$ which makes the ratio $V_{batt,i} / V_{dc,i}$ in (4) to vary in a wide range. This wide variation causes the outer voltage loop bandwidth to vary and therefore it can cause the degradation of converter stability margin or phase margin. Fig. 6.2 shows an example of such bandwidth variation of the module control voltage loop with module SOC using the gain crossover frequency. It can be seen that the bandwidth varies in nonlinear fashion and reaches to a high value at higher SOC during charging and vice-versa during discharging. Fig. 6.3 shows the frequency response plot to study the effect on the PM by theoretically varying the SOC of the third module. It can be seen that the stability margin (PM) of the third module goes down and gain cross over frequency goes up with the lower SOC. A similar change will happen if any other module SOC is made to vary.

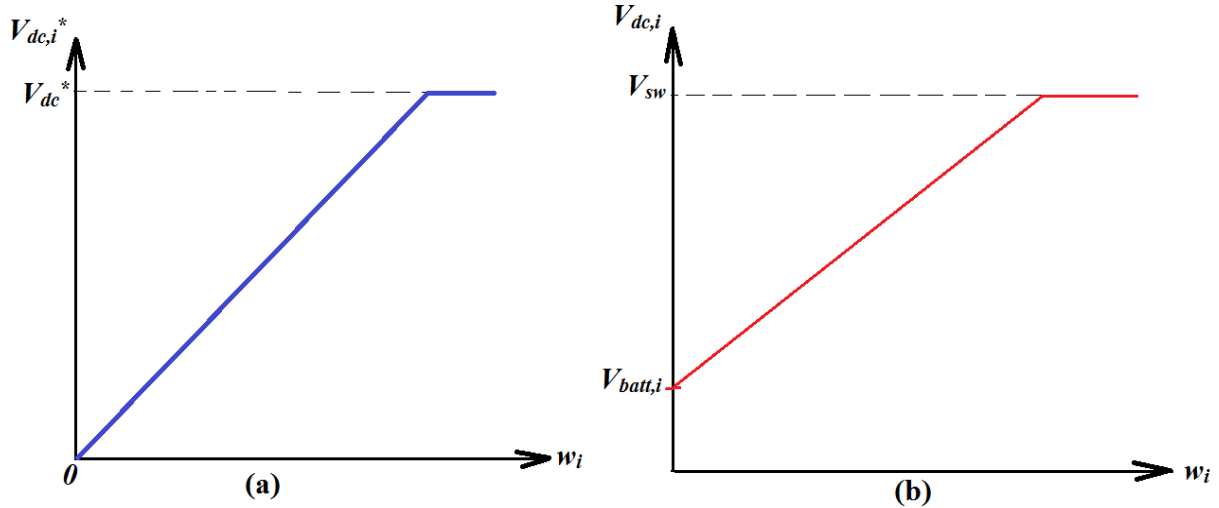


Fig. 6.1 Range of variation of module dc-link voltage reference and actual voltage with weighting factor: a) range of $V_{dc,i}^*$, b) range of $V_{dc,i}$

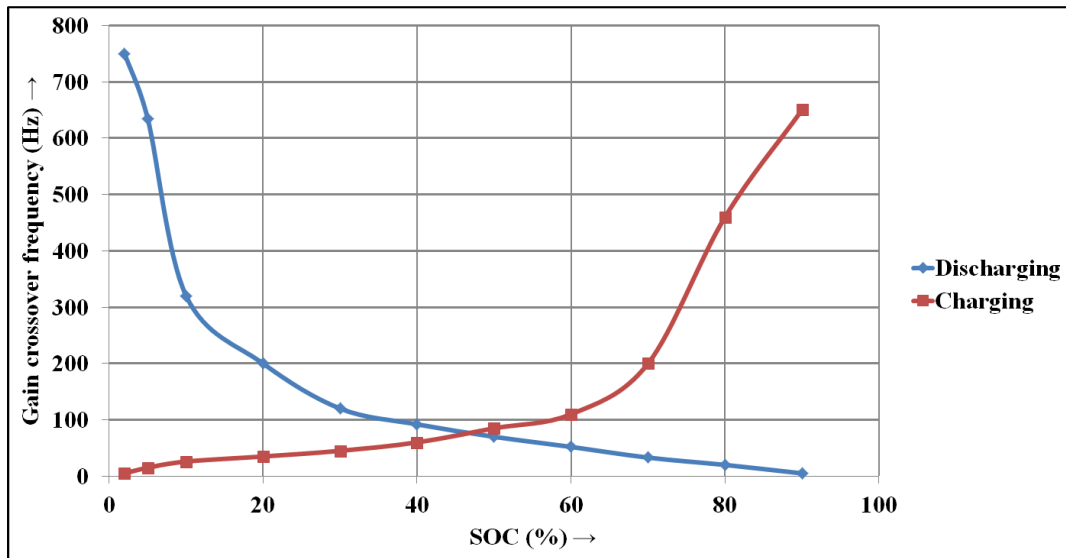


Fig. 6.2 Variation of gain crossover frequency or closed loop BW with SOC for 7.2V battery module

Generally, the inner current loop bandwidth is set to several times higher (typically 20-50 times more than the outer loop bandwidth) than the outer voltage loop for the control loop stability. Therefore, the high frequency behaviour of the inner loop is important. The inner current loop bandwidth can be derived by approximating the transfer function at a high frequency as shown in (6.12). The term ‘ G ’ depends on the carrier peak. Most of the cases, it is considered to be fixed (a fixed carrier) and set to the maximum $V_{dc,i}$. However, it is possible to vary the carrier gain dynamically (i.e. modulated carrier gain). The inner loop performance would be different in two cases. Therefore, both the cases are studied: a) $V_{dc,i}/G$ is nearly constant or a variable/modulated carrier, b) $V_{dc,i}/G$ is variable or a fixed carrier.

In the former case (modulated carrier gain), the inner loop bandwidth ($= \frac{K_{c,i}}{L G} V_{dc,i}$) can be considered to be constant ignoring the variation of L and in the latter case, the inner loop bandwidth cannot be treated as constant. Fig. 6.4 illustrates the current loop performances for a similar variation of state-of-charge (SOC) as the voltage loop. Note that, the high frequency

bandwidth of the current loop remains unaffected by variation of any battery parameters because all modules have the same inner loop bandwidth.

$$GH_I(s) \Big|_{\omega \rightarrow \infty} \approx \frac{K_{c,i}}{sL} \frac{1}{G} V_{dc,i} = \frac{K_{c,i}}{sL} \text{ or } BW = \frac{K_{c,i}}{L} \leftarrow \text{Variable/modulated carrier}$$

$$GH_I(s) \Big|_{\omega \rightarrow \infty} \approx \frac{K_{c,i}}{sL} \frac{1}{G} V_{dc,i} \text{ or } BW = \frac{K_{c,i}}{L} \frac{1}{G} V_{dc,i} \leftarrow \text{Fixed carrier} \quad (6.12)$$

Fig. 6.5 illustrates the effect on the high frequency bandwidth (BW) of the inner current loop when using a fixed carrier gain (G). It can be noted from Fig. 6.5(b) that the variation of SOC causes the weighting factor (ω_i) to vary which in turn changes the $V_{dc,i}$ with the SOC . This variation causes the inner loop bandwidth to vary. Note from Fig. 6.5(b) that such a wide variation of one SOC just causes a slight change in the corresponding inner loop BW. In the present case, inner loop bandwidth of module – 1 goes down from 2 kHz to 1.6 kHz. This variation may not cause a significant change in the overall system performance.

Therefore, it is found that due to the variation of battery parameters, the outer voltage loop bandwidth tends to get faster while inner current loop bandwidth remains almost unaffected. It can be seen from Fig. 6.3 and the corresponding Fig. 6.4 that the ratio of the inner loop to outer loop bandwidth was 125 in the first case which means the two bandwidths were well separated. As a result, the outer loop sees the inner loop as instantaneous and stability is maintained. However, the ratio changes to 11.4 in the second case and 3.15 in the third case. As a result, it is difficult for the converter to guarantee stability if the ratio falls to a low value if using the cascaded control loop.

Moreover, the current loop bandwidth is limited by the sampling frequency (related to the switching frequency of the converter) and inductor value in each module. As a result, this type of variation of outer voltage loop bandwidth can cause stability problem which are difficult to handle using a set of fixed controller parameters. Fig. 6.6 shows the variation of outer voltage control loop bandwidth with the SOC for a 7.2V battery module. It can be seen that as the SOC goes towards 100% during charging, the phase margin tends to zero and vice-versa during the charging mode. Therefore, the stability problem is inevitable when using the cascaded control structure after a particular operating point.

6.2.1.2 Case – 2: Variation of capacity ($Q_{max,i}$)

The variation of available battery capacity is another important phenomenon in second life applications. This variation of $Q_{max,i}$ can also cause the weighting factor ω_i to vary. This also causes variation of the gain crossover frequency or phase margin. Fig. 6.7 shows the variation of stability margin with capacity degradation. It is clear that the phase margin also goes down with the variation of battery capacity.

However, the variation is not as extreme as the SOC variation because it is unlikely that the capacity is a fast variable and does not go down to a low value so quickly. Therefore, this effect can be considered to be less significant compared to the SOC variation. However, there could be a cumulative effect from both low SOC and the capacity-fade. Therefore, it is difficult to ensure the converter stability using fixed controller parameters.

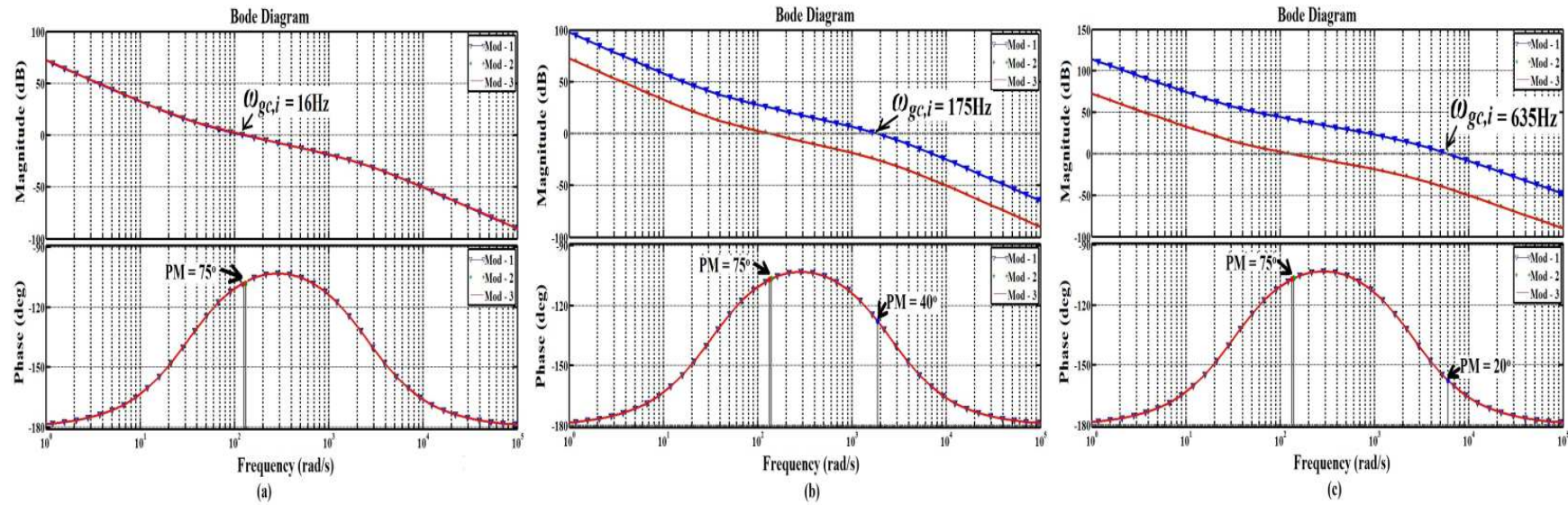


Fig. 6.3 Effect of initial SOC variation on outer voltage loop stability margin for a 7.2V, 6.5Ah module during discharging mode: a) $SOC = 70\%$, b) $SOC = 33.3\%$, c) $SOC = 10\%$

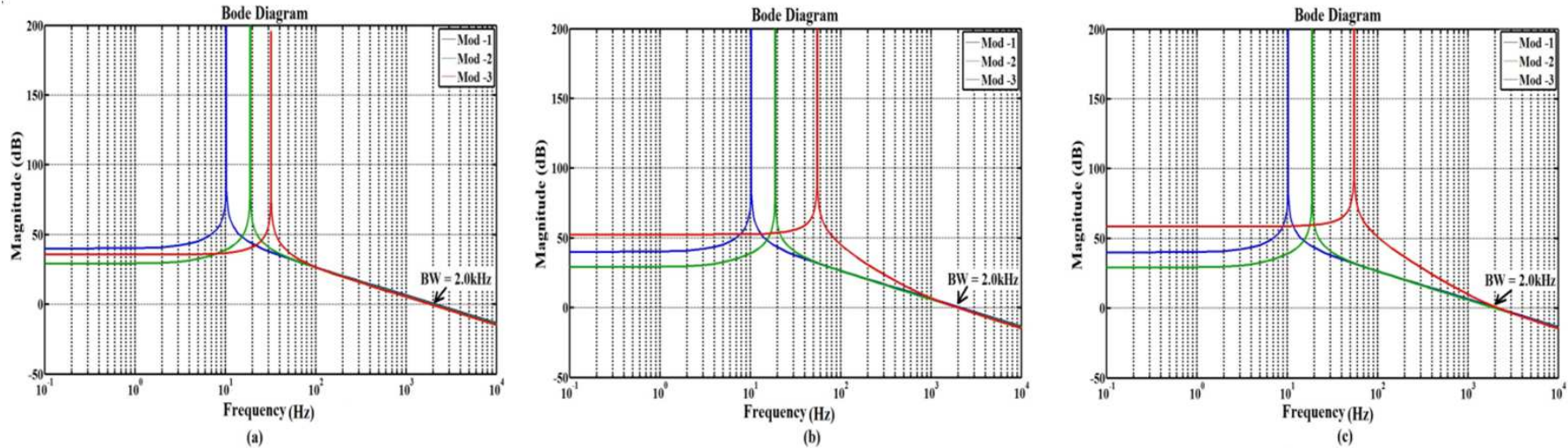


Fig. 6.4 Effect of SOC variation on inner loop using a modulated carrier gain (variable G) for a 7.2V, 6.5Ah module during discharging mode: a) $SOC = 70\%$, b) $SOC = 33.3\%$, c) $SOC = 10\%$

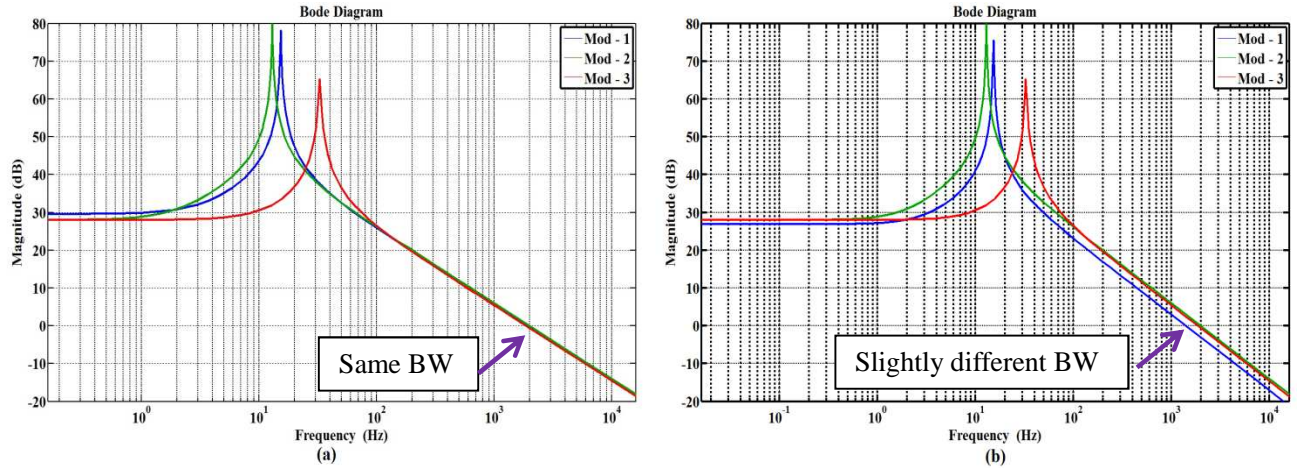


Fig. 6.5 Effect of SOC variation on inner current loop using a fixed carrier gain (fixed G) for a 12V, 10Ah module during discharging mode: a) SOC = 80%, b) SOC = 20%

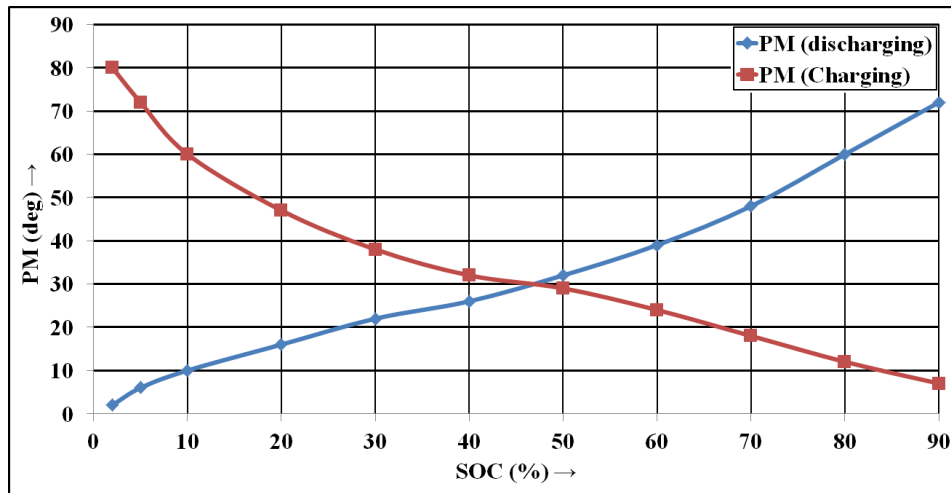


Fig. 6.6 Variation of control stability margin with initial SOC for a 7.2V battery module

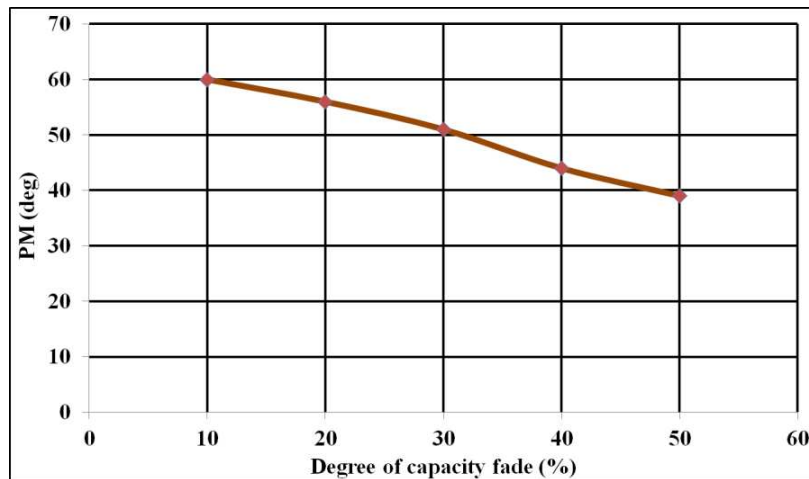


Fig. 6.7 Variation of control stability margin for capacity fade: a 7.2V battery module

6.2.2 Other effects

It is not only important to ensure the stability of one module but also to analysis the effect on other modules. If one module becomes oscillatory the stability of the remaining modules also gets adversely affected in this converter. This is because the overall control of the modular

dc-dc converter guarantees the total dc-link voltage ($\sum V_{dc,i} = V_{dc}$) is fixed. Therefore, if one of the voltages ($V_{dc,i}$) gets oscillatory that oscillation propagates in all the modules because the instantaneous sum of these voltages is fixed. This oscillation in $V_{dc,i}$ forces the remaining module currents to be oscillatory because the current reference is always the output of the voltage controller according to the module control structure (as shown in Fig. 5.2). Therefore, it is essential to maintain a uniform stability margin for all the modules when using such cascaded converter structure.

Apart from the stability issue, this dynamic outer loop bandwidth variation also causes the system to have poor dynamic response because the response time is inversely proportional to the outer voltage controller bandwidth as explain in chapter 5. Any attempt to increase the dynamic response could cause a similar stability problem.

6.2.3 Validation of fixed controller stability issues

In order to show the limitation of fixed controller based approach, simulation and experimental studies have been undertaken. Two of the modules were started from a low initial SOC during discharging mode and high initial SOC during charging condition module – 1 $OCV_{o,1} = 9.75V$ (SOC = 3.4%), module – 2 $OCV_{o,2} = 19V$ (10%), $OCV_{o,3} = 5.75V$ (7%) during discharging mode. The simulation and experimental results are presented in Fig. 6.8(a) and Fig. 6.8(b) respectively. It can be seen that the system is unstable while delivering to the load in grid-tie mode. It can be seen that the responses are quite oscillatory both in simulation and experiments. The current oscillates close to the positive and negative controller limits. Note that the current with the lowest initial SOC (here module – 1) oscillates the most.

There is another test has been performed in charging mode where the system were found to be oscillatory even before connecting to the grid. The result has been presented in Fig. 6.9(a) and Fig. 6.9(b). The initial condition were $OCV_{o,1} = 13.6V$ (SOC = 89%), $OCV_{o,2} = 27V$ (SOC = 90%), $OCV_{o,3} = 8.3V$ (SOC = 96.6%). The current were found to be oscillating instead of being zero before connecting to the grid. Simulation and experimental results show a reasonable match. These results demonstrate that the stability of the overall system stays at stake when using a fixed controller based approach. This validates the theory behind the stability problem.

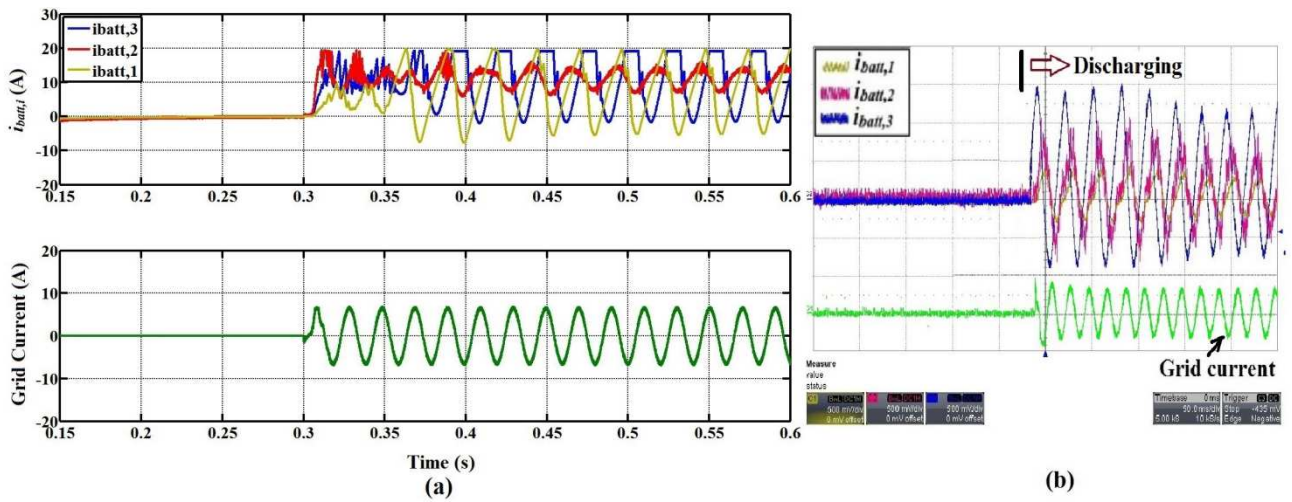


Fig. 6.8 Fixed PI-controller in discharging condition in grid-tie mode: a) simulation study, b) experimental study: $OCV_{o,1} = 9.75V$, $OCV_{o,2} = 19V$, $OCV_{o,3} = 6.8V$: scale 50ms/div, grid current 10A/div, module currents 5A/div

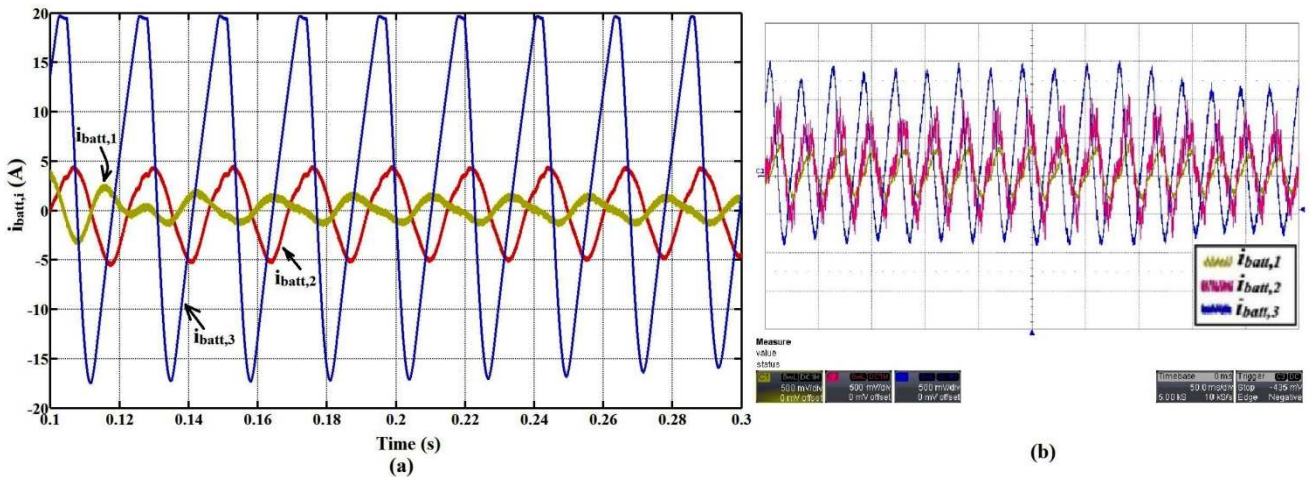


Fig. 6.9 Fixed PI-controller in charging condition before connecting to the grid: a) simulation study, b) experimental study: $OCV_{o,1} = 13.6V$, $OCV_{o,2} = 27V$, $OCV_{o,3} = 8.3V$: scale 50ms/div, module current 5A/div

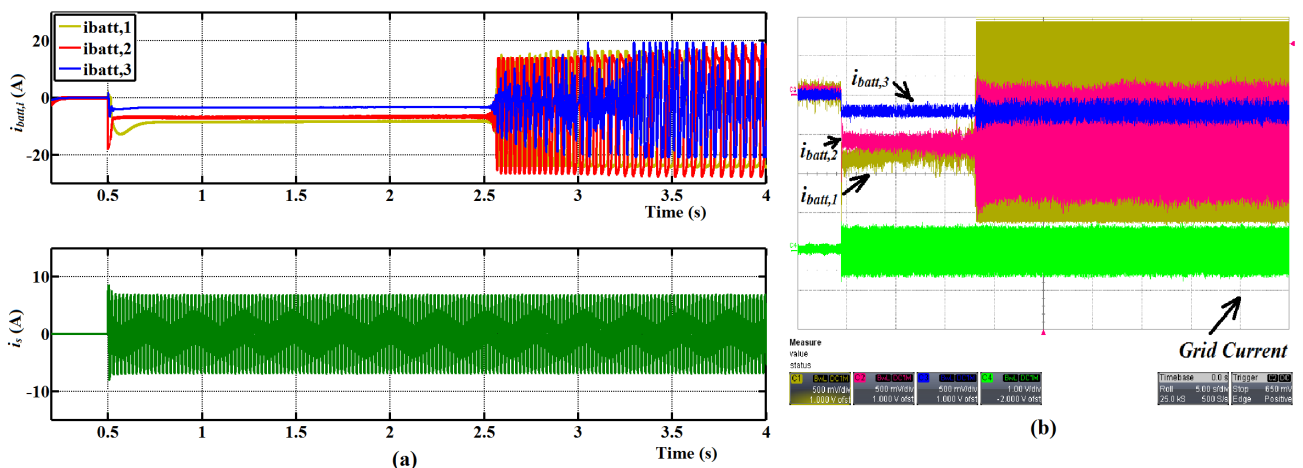


Fig. 6.10 Fixed PI-controller in charging condition after connecting to the grid: a) simulation study, b) experimental study: scale 5s/div, module current 5A/div, grid current 10A/div

The stability problem may arise gradually when using a fixed controller parameter because the state-of-charge (SOC) is subjected to change in every sample time and capacity also gets affected in the long run. In order to validate this converter was run for a long time using a

fixed set of control parameters as shown in Fig. 6.10. It can be seen that the converter was stable and was sharing current among the module but starts to get oscillatory after a point of time when the modules get close to fully charged.

It was found from the analysis, simulation and experimental study that any degradation in stability margin in the worst case can result in an overall stability problem in the modular dc-dc converter. Under this condition, the module current can be highly oscillatory in nature which may result in inadvertent tripping of the converter leading to complete shutdown of the system at any time. Moreover, such an oscillation may also be harmful for the battery life because a battery is not intended to deliver such oscillatory current. Therefore, mitigation is required.

6.3 Mitigation of stability problem – an adaptive PI approach

A fixed controller parameter based approach cannot guarantee the stability in all possible operating conditions. Therefore, this section discusses an adaptive PI control based approach where the controller parameters are tuned adaptively with the battery operating conditions or with the weighting factor.

6.3.1 Adaptive tuning

Using the symmetric optimum method [363], the phase margin of each converter module can be expressed as shown in (6.13) from (6.11) assuming $T_v = aT_d$. To select a desired PM, the parameter a can be calculated and used within (6.14) to set the controller parameters.

$$PM = \tan^{-1} \frac{\omega_{gc,i}(T_v - T_d)}{1 + \omega_{gc,i}^2 T_v T_d} = \tan^{-1} \left\{ \frac{1}{2} \left(a - \frac{1}{a} \right) \right\} \quad (6.13)$$

The proportional gain $K_{v,i}$ can be a function of battery parameters or weighting factor through $V_{dc,i}$ which is measured. Therefore, it is possible to keep a uniform phase margin for all the modules by tuning the controller parameter according to the weighting factor. The comparison between the fixed and adaptive control approach has been presented in frequency domain as shown in Fig. 6.11. It can be seen that a non-adaptive controller based approach can give rise to widely different phase margins within the converter this can either cause stability problem or widely different response time which in turn may incur overshoot/undershoot when responding to a load. On the other hand, adaptive controller based approach maintains a uniform stability margin.

$$K_{v,i} = \frac{1}{a} \left(\frac{V_{dc,i}}{V_{batt,i}} \right) \frac{1}{T_d} C \text{ and } T_v = a^2 T_d \quad (6.14)$$

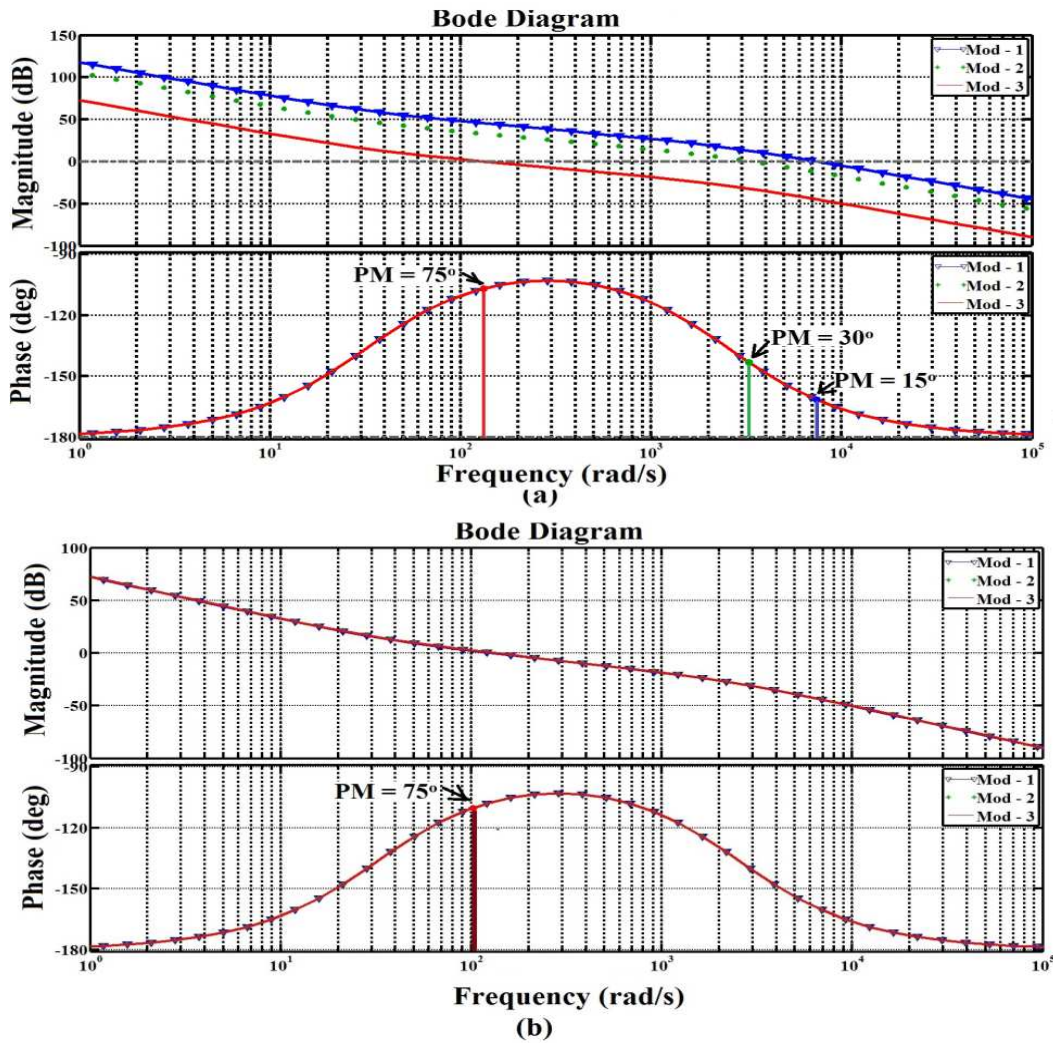


Fig. 6.11 Comparison of non-adaptive and adaptive controller performance during discharging mode: a) non-adaptive controller, b) adaptive controller: Operating condition $OCV_1 = 9.8V(SOC_1 = 4.5\%)$, $OCV_2 = 19V(SOC_3 = 10\%)$, c) $OCV_3 = 7.8V(SOC_3 = 76\%)$

6.3.2 Validation of adaptive PI-controller based approach

PI-controller parameters have been tuned to mitigate the stability problem as shown in simulation and experimental graphs in Fig. 6.12(a) and Fig. 6.12(b) for discharging and Fig. 6.13(a) and Fig. 6.13(b) for charging respectively. The initial voltage of the modules are: $OCV_{o,1} = 10V$, $OCV_{o,2} = 22.2V$ and $OCV_{o,3} = 6V$ during discharging and $OCV_{o,1} = 13.4V$, $OCV_{o,2} = 26.2V$ and $OCV_{o,3} = 8V$ during charging. It can be seen that no stability problem arises when using such an approach and the system responds as expected. The simulation and experimental studies were found to be similar in both the operational modes.

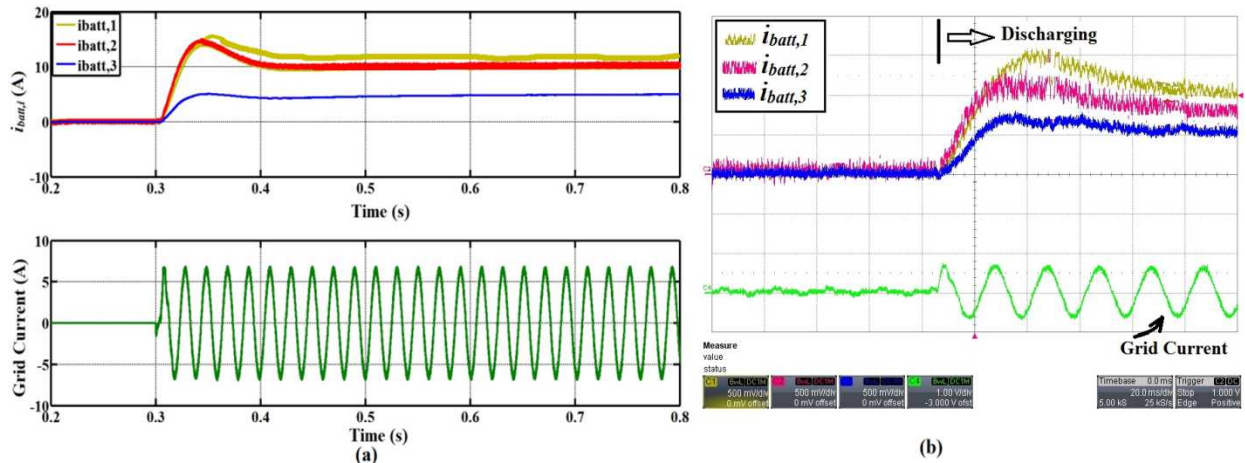


Fig. 6.12 Adaptive PI-controller in discharging: a) simulation study, b) experimental study $OCV_{o,1} = 10V$, $OCV_{o,2} = 22.2V$, $OCV_{o,3} = 6V$: scale 100ms/div, grid current 10A/div, module currents 5A/div

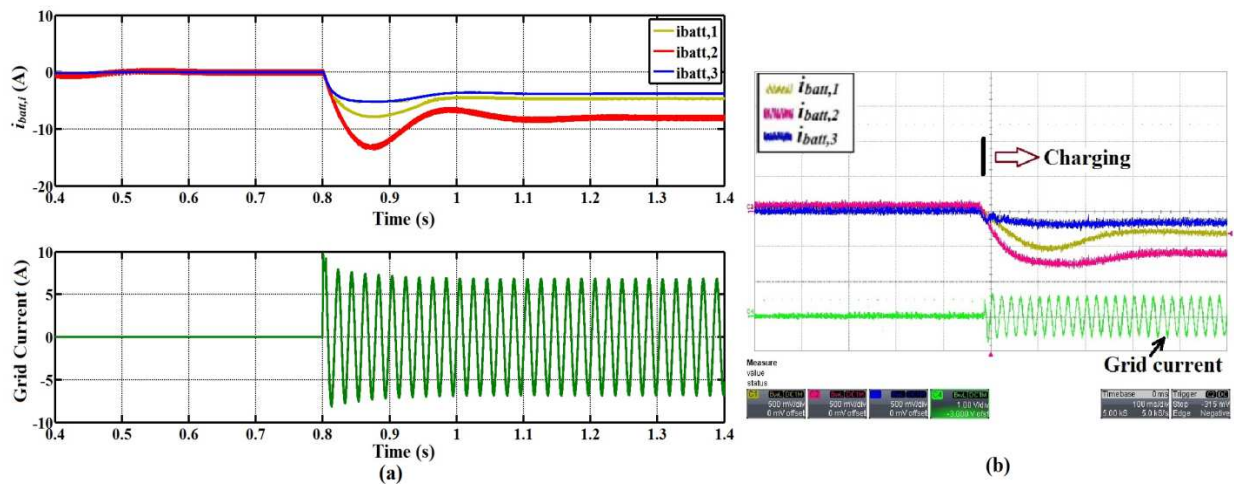


Fig. 6.13 Adaptive PI-controller in charging: a) simulation study, b) experimental study $OCV_{o,1} = 13.4V$, $OCV_{o,2} = 26.2V$, $OCV_{o,3} = 8V$: scale 100ms/div, grid current 10A/div, module currents 5A/div

In spite of being a straightforward change design approach, this adaptive tuning approach suffers from a shortcoming in the present applications – the controller parameter is very much dependent on system parameters which can give steady state error and poor dynamic response time if there are inaccuracies in the measurement, noise and/or estimation process. The accuracy of this approach can be improved if a more accurate measurement and estimation process is adopted.

6.4 Mitigation of stability problem – Lyapunov Approach

In order to overcome the drawbacks of cascaded control loops in the current distributed control context, an alternative approach based on the Control Lyapunov Function (CLF) has been investigated as a means to guarantee stability in all possible operating conditions. The Lyapunov control structure has been employed successfully in the power electronic converters to improve the slow response time of certain power converters such PFC (power factor correction) converters. However, it is mainly focused on non-modular converters where a single dc-dc or dc-ac converter is controlled [290], [379] – [380] and its application in the context of distributed control has not been reported. The main aim of using the

Lyapunov based control is to avoid the cascaded control loops so that the relative dependencies of control bandwidths can be avoided and guarantee stability in the present context.

6.4.1 Background

Lyapunov stability criterion is a useful approach in analysing the stability of nonlinear systems and designing nonlinear controller. This is appropriate to use in the current context because a boost converter is a non-minimum phase system and its large signal model is nonlinear [215]. Therefore, any linear control system cannot fully guarantee stability in all possible conditions.

Lyapunov stability utilises two different approaches: Lyapunov indirect method and Lyapunov direct method. For Lyapunov indirect method the idea of system linearization around a given point is normally used and one can achieve local stability with small regions. On the other hand the Lyapunov direct method is a useful tool for design and analysis of nonlinear systems. This method can be applied directly to a nonlinear system and even to a linear system. Lyapunov direct method deals directly with nonlinear systems and can be used to guarantee global stability with reduced computations.

Therefore, the direct approach is therefore widely used in power electronics [378] – [380]. The fundamental concept of the Lyapunov direct method is that if the total energy of a system is continuously dissipating, then the system will eventually reach an equilibrium point and remain at that point. The direct approach consists of two steps: a) firstly to construct a suitable scalar function which is referred to as a Lyapunov function [381], b) then to evaluate its first order time derivative along the trajectory of the system to check the trend of variation of the function of the system state variable. If the derivative of the Lyapunov function is decreasing along the system trajectory as time increases, this indicates that the system energy is dissipating and the system will finally settle down which indicates the stability.

Consider a dynamic system $f(x, t)$ which satisfies the properties (6.15) and (6.16) where f is a given continuous function in t .

$$\dot{x} = f(x, t), t \geq 0 \quad (6.15)$$

$$x(t_0) = x_0, t_0 \geq 0 \quad (6.16)$$

A state x^* is an equilibrium point of the system if $f(x^*) = 0$. Intuitively, let us assume an equilibrium point is locally stable if all solutions which start near x^* (meaning that the initial conditions are in a neighbourhood of x^* remain near x^* for all time. The equilibrium point x^* is said to be locally asymptotically stable if x^* is locally stable and, furthermore, all solutions starting near x^* tend towards x^* as $t \rightarrow \infty$.

Now, define on an energy-like function $L(x)$, often termed as the Lyapunov function in terms of the system states. Any linear or nonlinear system is globally asymptotically stable if $L(x)$ satisfies the following properties [381].

- 1) $L(0) = 0$;
- 2) $L(x) > 0$ for all $x \neq 0$;
- 3) $\frac{dL(x)}{dt} < 0$ for all $x \neq 0$;
- 4) $L(x) \rightarrow \infty$ as $\|x\| \rightarrow \infty$.

6.4.2 Lyapunov based control for cascaded dc-dc converters

There are two states per converter module: a) $i_{batt,i}$ and b) $V_{dc,i}$. Now, assume the reference values of these states are $i_{batt,i}^*$ and $V_{dc,i}^*$. The dynamic equations at the reference point are:

$$L \frac{di_{batt,i}^*}{dt} + Ri_{batt,i}^* + (1 - D_i)V_{dc,i}^* = V_{batt,i} \quad \forall i = 1 \dots n \quad (6.17)$$

$$C \frac{dV_{dc,i}^*}{dt} - (1 - D_i)i_{batt,i}^* = -I_{dc} \quad \forall i = 1 \dots n \quad (6.18)$$

Let us define the following error functions for the states:

$$x_{1i} = i_{batt,i} - i_{batt,i}^* \quad \text{and} \quad x_{2i} = V_{dc,i} - V_{dc,i}^* \quad \forall i = 1 \dots n.$$

Substituting, $i_{batt,i} = x_{1i} + i_{batt,i}^*$, $V_{dc,i} = x_{2i} + V_{dc,i}^*$ in (5.1) and (5.2) of chapter 5 respectively,

$$L \frac{d(x_{1i} + i_{batt,i}^*)}{dt} + R(x_{1i} + i_{batt,i}^*) + (1 - d_i)(x_{2i} + V_{dc,i}^*) = V_{batt,i} \quad (6.19)$$

$$C \frac{d(x_{2i} + V_{dc,i}^*)}{dt} - (1 - d_i)(x_{1i} + i_{batt,i}^*) = -I_{dc} \quad (6.20)$$

d_i is the control input of the converter, therefore, it can be written as a combination of reference and perturbed points $d_i = D_i + \hat{d}_i$. Substituting d_i in (6.19) and (6.20) gives

$$L \frac{d(x_{1i} + i_{batt,i}^*)}{dt} + R(x_{1i} + i_{batt,i}^*) + (1 - D_i - \hat{d}_i)(x_{2i} + V_{dc,i}^*) = V_{batt,i} \quad (6.21)$$

$$C \frac{d(x_{2i} + V_{dc,i}^*)}{dt} - (1 - D_i - \hat{d}_i)(x_{1i} + i_{batt,i}^*) = -I_{dc} \quad (6.22)$$

Subtracting (6.17) and (6.18), from equations (6.21) and (6.22) gives (6.23) and (6.24) respectively gives

$$L \frac{d(x_{1i})}{dt} + Rx_{1i} + (1 - D_i)(x_{2i}) - \hat{d}_i(x_{2i} + V_{dc,i}^*) = 0 \quad (6.23)$$

$$C \frac{d(x_{2i})}{dt} - (1 - D_i)(x_{1i}) + \hat{d}_i(x_{1i} + i_{batt,i}^*) = 0 \quad (6.24)$$

A suitable candidate as a Lyapunov function in this applications is similar to [378] which also looked at Lyapunov function of dc-dc converter:

$$L(x) = \frac{1}{2}Lx_{1i}^2 + \frac{1}{2}Cx_{2i}^2 \quad (6.25)$$

Taking the derivative,

$$\frac{dL(x)}{dt} = x_{1i}L \frac{dx_{1i}}{dt} + x_{2i}C \frac{dx_{2i}}{dt} \quad (6.26)$$

Now substituting, (6.23) and (6.24) in (6.26) and rearranging gives:

$$\frac{dL(x)}{dt} = -(x_{2i}i_{batt,i}^* - x_{1i}V_{dc,i}^*)\widehat{d}_l - R(x_{1i})^2 \quad (6.27)$$

According to the criterion listed above, it requires $\frac{dL(x)}{dt} < 0$ for the stability. Therefore, select $\widehat{d}_l = K(x_{2i}i_{batt,i}^* - x_{1i}V_{dc,i}^*)$ and substituting back into (6.27) gives

$$\frac{dL(x)}{dt} = -Rx_{1i}^2 - K(x_{2i}i_{batt,i}^* - x_{1i}V_{dc,i}^*)^2 \quad (6.28)$$

The expression (6.28) is clearly negative definite at all the time provided $K > 0$. Therefore, the necessary and sufficient condition for module stability becomes $K > 0$.

6.4.2.1 Significance of ‘K’ in the Design

In order to study the importance of K , let us substitute $\widehat{d}_l = K(x_{2i}i_{batt,i}^* - x_{1i}V_{dc,i}^*)$ from (6.28) in (6.23) and (6.24),

$$L \frac{d(x_{1i})}{dt} = -(1 - D_i - Ki_{batt,i}^*V_{dc,i}^*)(x_{2i}) + K(x_{2i})^2i_{batt,i}^* - Kx_{1i}x_{2i}V_{dc,i}^* - x_{1i}(R + KV_{dc,i}^{*2}) \quad (6.29)$$

$$C \frac{d(x_{2i})}{dt} = (1 - D_i + Ki_{batt,i}^*V_{dc,i}^*)(x_{1i}) + K(x_{1i})^2V_{dc,i}^* - Kx_{1i}x_{2i}i_{batt,i}^* - Kx_{2i}(i_{batt,i}^*)^2 \quad (6.30)$$

Now linearizing the following expressions by writing $x_{1i} = X_{1i} + \widehat{x}_{1i}$ and $x_{2i} = X_{2i} + \widehat{x}_{2i}$

$$L \frac{d(\widehat{x}_{1i})}{dt} = -(1 - D_i - Ki_{batt,i}^*V_{dc,i}^*)\widehat{x}_{2i} - \widehat{x}_{1i}(R + KV_{dc,i}^{*2}) \quad (6.31)$$

$$C \frac{d(\widehat{x}_{2i})}{dt} = (1 - D_i + Ki_{batt,i}^*V_{dc,i}^*)\widehat{x}_{1i} - K\widehat{x}_{2i}(i_{batt,i}^*)^2 \quad (6.32)$$

Rearranging in the matrix form,

$$\begin{pmatrix} \frac{d(\widehat{x}_{1i})}{dt} \\ \frac{d(\widehat{x}_{2i})}{dt} \end{pmatrix} = \begin{pmatrix} -\frac{(R + KV_{dc,i}^{*2})}{L} & -\frac{(1 - D_i - Ki_{batt,i}^*V_{dc,i}^*)}{L} \\ \frac{(1 - D_i + Ki_{batt,i}^*V_{dc,i}^*)}{C} & -\frac{K(i_{batt,i}^*)^2}{C} \end{pmatrix} \begin{pmatrix} \widehat{x}_{1i} \\ \widehat{x}_{2i} \end{pmatrix} \text{ or}$$

$$\begin{aligned}
 & \begin{pmatrix} \frac{d(\widehat{x}_{1i})}{dt} \\ \frac{d(\widehat{x}_{2i})}{dt} \end{pmatrix} \\
 &= \begin{pmatrix} -\frac{(R + KV_{dc,i}^{*2})}{L} & -\frac{(1 - D_i - Ki_{batt,i}^* V_{dc,i}^*)\omega}{Z_o} \\ (1 - D_i + Ki_{batt,i}^* V_{dc,i}^*)\omega Z_o & -\frac{K(i_{batt,i}^*)^2}{C} \end{pmatrix} \begin{pmatrix} \widehat{x}_{1i} \\ \widehat{x}_{2i} \end{pmatrix} \text{ where} \\
 & Z_o = \sqrt{\frac{L}{C}} \text{ and } \omega = \frac{1}{\sqrt{LC}} \tag{6.33}
 \end{aligned}$$

Now, averaging (6.33) the matrix around the frequency ω , the expression can be further simplified.

$$\begin{pmatrix} \frac{d(\widehat{x}_{1iav})}{dt} \\ \frac{d(\widehat{x}_{2iav})}{dt} \end{pmatrix} = \begin{pmatrix} -\frac{(R+KV_{dc,i}^{*2})}{L} & 0 \\ 0 & -\frac{K(i_{batt,i}^*)^2}{C} \end{pmatrix} \begin{pmatrix} \widehat{x}_{1iav} \\ \widehat{x}_{2iav} \end{pmatrix} \tag{6.34}$$

Solving the average value of x_{1i} and x_{2i} from (6.34),

$$\frac{d(\widehat{x}_{1iav})}{dt} = -\frac{(R+KV_{dc,i}^{*2})}{L} \widehat{x}_{1iav} \rightarrow \widehat{x}_{1iav}(t) = e^{-\frac{(R+KV_{dc,i}^{*2})}{L}t} \tag{6.35}$$

$$\frac{d(\widehat{x}_{2iav})}{dt} = -\frac{K(i_{batt,i}^*)^2}{C} \widehat{x}_{2iav} \rightarrow \widehat{x}_{2iav}(t) = e^{-\frac{K(i_{batt,i}^*)^2}{C}t} \tag{6.36}$$

These equations are important because they contain the explicit expressions of the error dynamics. These error dynamics are important to predict the steady-state errors and dynamics responses of their individual states. It can be seen from (6.35) and (6.36) that the average values of steady state errors asymptotically to zero for any positive values of K . The higher is the value of K the faster the rate of convergence. Therefore, the individual control bandwidth of module voltage ($BW_{v,i}$) and current ($BW_{c,i}$) can be taken proportional to these values as shown in (6.37). Here K is the control variable and any change in K influences the current and voltage controller bandwidths proportionately. So, if one control bandwidth changes (increases or decreases) due to change in the battery operating conditions, there will be a subsequent change in the other control bandwidth which means the state variables are controlled at the same time. As a result, this control system always guarantees stability and eliminates instability due to mismatches of their control bandwidths.

$$BW_{c,i} \propto \frac{(R+KV_{dc,i}^{*2})}{L} \text{ and } BW_{v,i} \propto \frac{K(i_{batt,i}^*)^2}{C} \tag{6.37}$$

Moreover, if a uniform voltage controller bandwidth is chosen for all the modules, then the ratio of K among the three modules will be according to (6.38). This means that the module with a higher share of current has a lower K compared to the module with a lower share of current.

$$K_{v1}: K_{v2}: K_{v3} = \frac{1}{i_{batt,1}^{*2}}: \frac{1}{i_{batt,2}^{*2}}: \frac{1}{i_{batt,3}^{*2}} \quad (6.38)$$

6.4.2.2 An effect of parameter variation /inaccurate reference values on stability

It is necessary to investigate the effect of system parameter changes in control stability because any error in the measurement and/or estimation process can result in inaccurate references. These inaccurate references may make the derivative of the lyapunov function non-negative according to (6.27) which in turn raises a stability concern.

Assume the inaccurate references due to measurement and/estimation process, are $i_{batt,ic}^*$ instead of $i_{batt,i}^*$ and $V_{dc,ic}^*$ instead of $V_{dc,i}^*$. Therefore, under this situation the derivative $\frac{dL(x)}{dt}$ becomes:

$$\frac{dL(x)}{dt} = -K(x_{2i}i_{batt,i}^* - x_{1i}V_{dc,i}^*)(x_{2i}i_{batt,ic}^* - x_{1i}V_{dc,ic}^*) - Rx_{1i}^2 \quad (6.39)$$

This expression can be written in the form $X^T Q X$ for convenience of analysis where $X = [x_{1i} \ x_{2i}]$ and Q is the following matrix:

$$Q = \begin{pmatrix} -(KV_{dc,i}^*V_{dc,ic}^* + R) & \frac{K}{2}(i_{batt,i}^*V_{dc,ic}^* + i_{batt,ic}^*V_{dc,i}^*) \\ \frac{K}{2}(i_{batt,i}^*V_{dc,ic}^* + i_{batt,ic}^*V_{dc,i}^*) & -K(i_{batt,i}^*i_{batt,ic}^*) \end{pmatrix} \quad (6.40)$$

In order to fulfil the criterion $\frac{dL(x)}{dt} < 0$, the matrix Q has to be negative definite which means $(KV_{dc,i}^*V_{dc,ic}^* + R) > 0$ and $\det(Q) < 0$. The expression $(KV_{dc,i}^*V_{dc,ic}^* + R) > 0$ if $K > 0$ as $V_{dc,i}^*$, R and $V_{dc,ic}^*$ all are positive. $Det(Q)$ is derived below.

$$\det(Q) = -\frac{K^2}{4} \left(a^2V_{dc,i}^{*2} + b^2i_{batt,i}^{*2} - 2abi_{batt,i}^*V_{dc,i}^* - 4\frac{R}{K}ai_{batt,i}^* \right) \text{ where} \\ a = i_{batt,ic}^* \text{ and } b = V_{dc,ic}^* \quad (6.41)$$

Rearranging (6.41) provides,

$$\det(Q) = -\frac{K^2}{4} \left[(aV_{dc,i}^* - bi_{batt,i}^*)^2 - 4\frac{R}{K}ai_{batt,i}^* \right] \quad (6.42)$$

Therefore, necessary condition for which $Det(Q) < 0$ will be:

$$\left(aV_{dc,i}^* - bi_{batt,i}^* \right)^2 > 4\frac{R}{K}ai_{batt,i}^* \text{ or} \\ K > \frac{4R}{(aV_{dc,i}^* - bi_{batt,i}^*)^2} ai_{batt,i}^* \quad (6.43)$$

It can be seen that if there is an error in $V_{dc,i}^*$ and $i_{batt,i}^*$, $\frac{dL(x)}{dt}$ is not always negative. Therefore, the stability is not guaranteed. The expression (6.43) provides the minimum value of K . Now, if there is a $\varepsilon_1\%$ and $\varepsilon_2\%$ error are assumed in $i_{batt,i}^*$ and $V_{dc,i}^*$ then the minimum K needed from (6.43) can be further modified as below.

$$K_{min,i} = \left| \frac{4R(1 \pm \varepsilon_1)}{V_{dc,i} *^2 (\varepsilon_1 \sim \varepsilon_2)^2} \right| \quad (44)$$

Therefore, the following conclusions can be drawn about the proposed control:

- A high value of K provides better stability, faster convergence and better control bandwidth from (6.34) and (6.41).
- An appropriate design value of K ($K > K_{min}$) is needed by considering the maximum possible error in the measurement/estimation process to eliminate any dependency system parameter(s) in this control structure.
- However, an excessive high value of K can increase noise and ripple in the module voltage and current because it enhances the perturbation part of d_i ($= \hat{d}_i$). Moreover, a high value of K can distort the reference duty ratio point D_i in $d_i = D_i + \hat{d}_i$ which can cause improper voltage and current sharing among the modules.
- Therefore, the upper limit of K is limited by the ripple/noise while the lower limit is determined from the stability criterion according to (6.44).

6.4.3 Control architecture development

After designing each converter module according to the control Lyapunov function (CLF), it is necessary to build a control structure which can suitably control each converter module and also maintain the central dc-link voltage. The block diagram of the proposed control approach with measured signals is shown in Fig. 6.14. Each converter module is controlled using the Lyapunov function so that stability and dynamic response are guaranteed at a module level. Moreover, it is necessary to maintain the central dc-link voltage to a constant value along with the module independent control.

The individual references for the system states are generated independently unlike in the cascaded control approach (based on the PI-controller) where each outer voltage loop generates the reference for the inner current and the output of the inner current controller generates the duty ratio references. Therefore, a central reference generation block as shown in Fig. 6.14 is necessary in this control structure.

The proposed control structure consists of four stages: a) reference generation for module voltages, b) reference generation for module currents, c) reference generation for module duty ratio, and d) actual control logic.

In the first stage, the module dc-bus voltage references can be generated using the central dc-link voltage reference and weighting factors as shown in Fig. 6.15a.

In the second stage, the module current references are generated from the output of an overall dc-link controller which helps to maintain the central dc-link voltage as shown in Fig. 6.15b. The output of that controller generates the reference for the common dc-link current (I_{dc}) which in turn generates the power reference for each module. These power references are then converted to individual current references using their module input voltages.

Fig. 6.15c shows the reference generation for the module duty ratio through the equation (6.17). A small LPF (low pass filter) $\frac{1}{1+sT_f}$ with a cut-off frequency $(1/T_f)$ $1/10^{\text{th}}$ of sampling frequency has been employed to eliminate the high frequency noise generated from the differentiation. At last, the overall control of each module is described in Fig. 6.15(d).

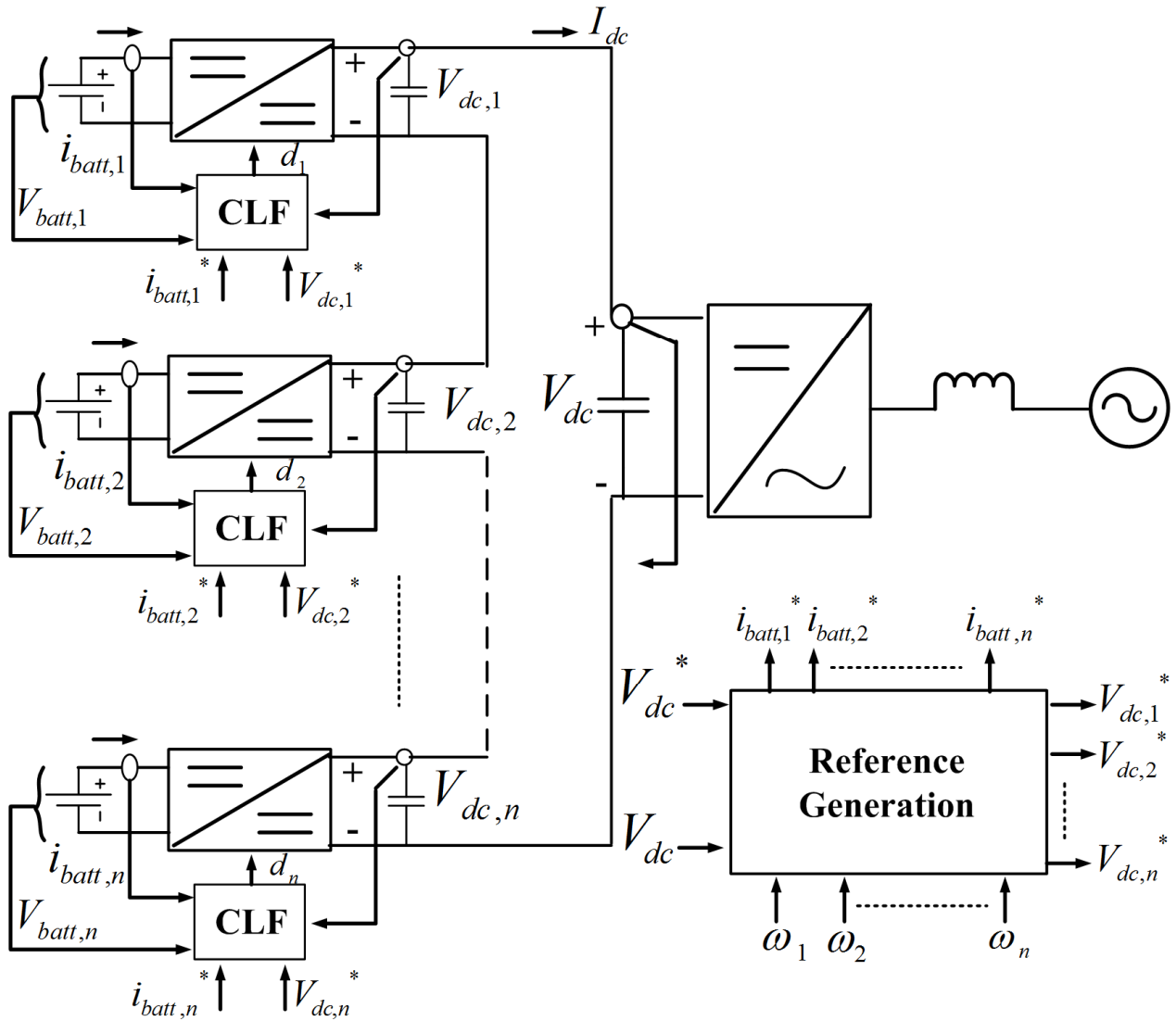


Fig. 6.14 Proposed distributed control approach for the cascaded dc-dc converter

The Matlab/Simulink model of the module control structure is shown in Fig. 6.16. Each block has been clearly marked showing the reference duty ratio generation and module control structure. The dc-link control loop and module current reference generation is shown in Fig. 6.17.

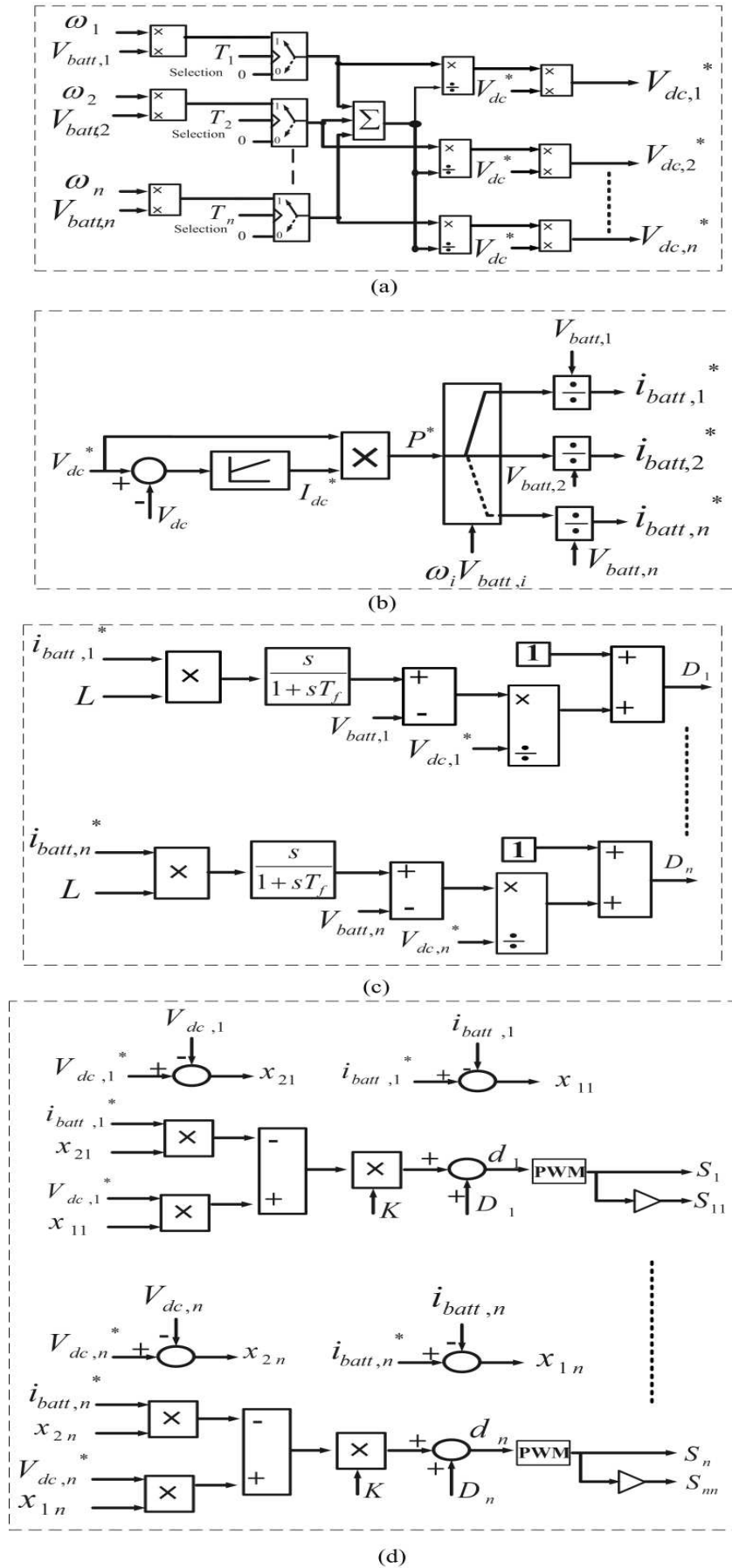


Fig. 6.15 Proposed distributed control structure for the cascaded dc-dc converter: a) voltage reference generation, b) current reference generation, c) duty ratio reference generation, d) actual control logic

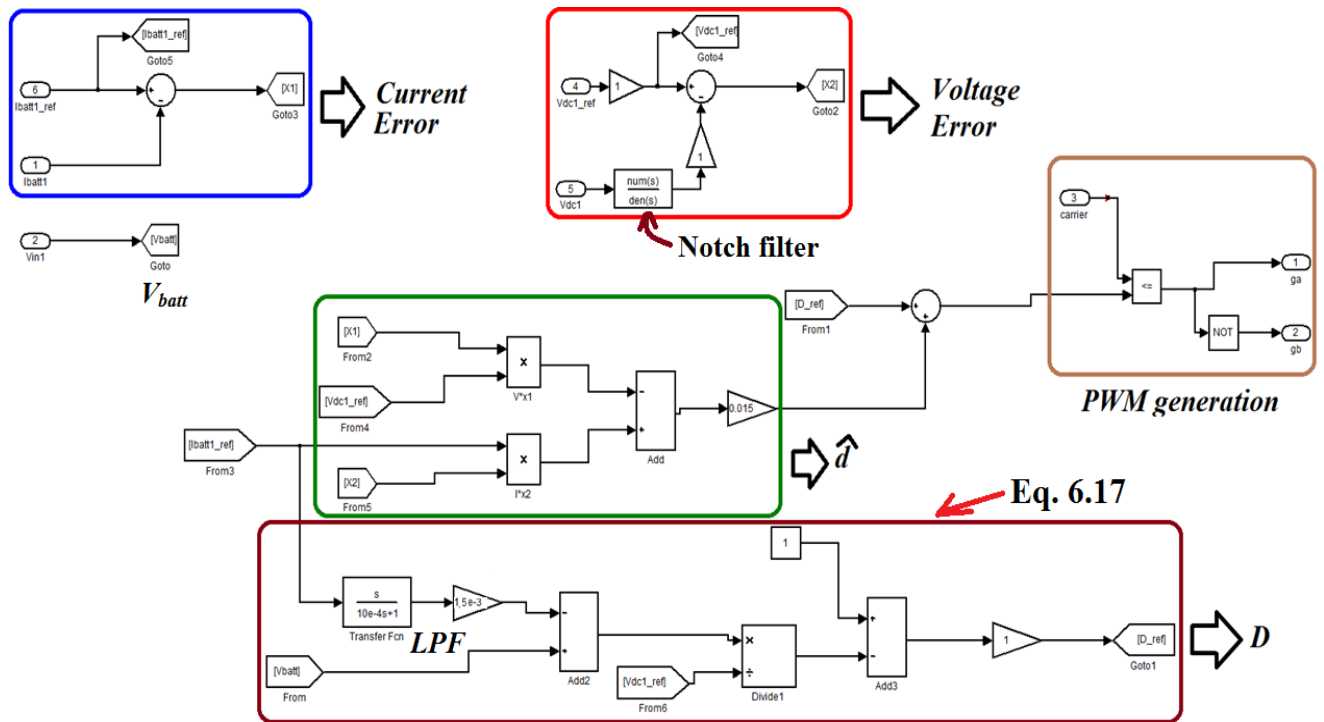


Fig. 6.16 Matlab/Simulink Model of module Lyapunov based control

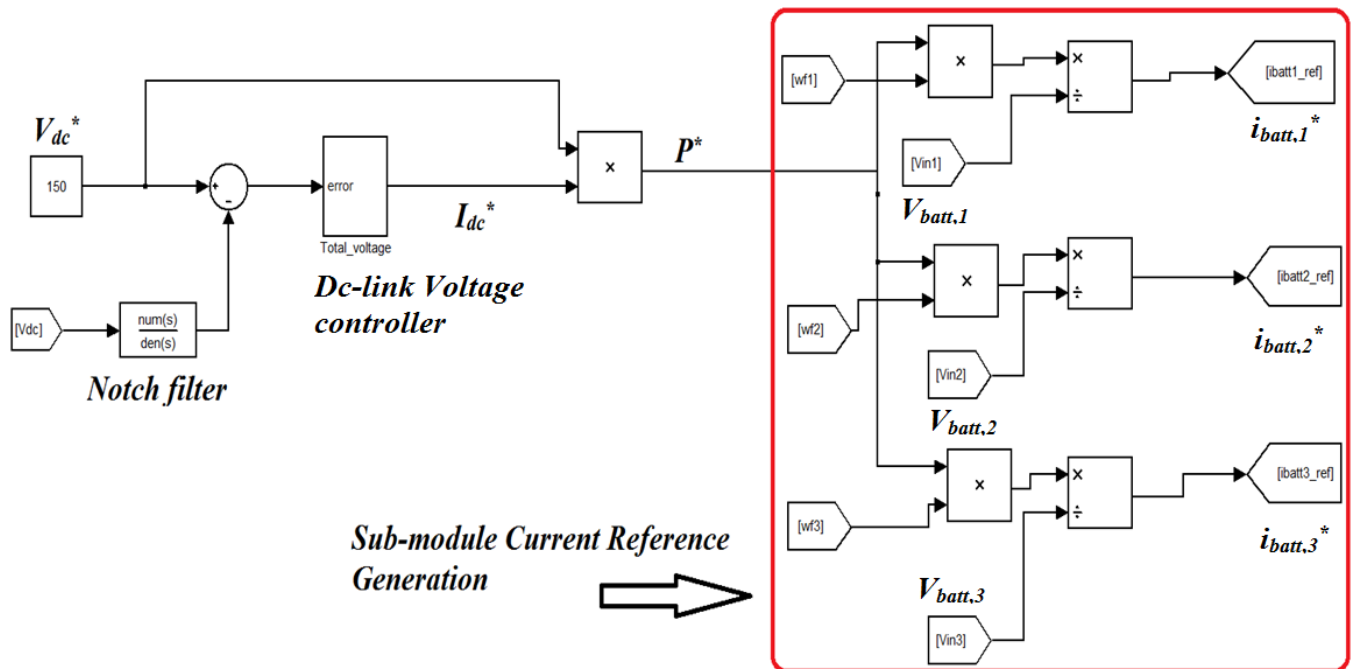


Fig. 6.17 Matlab/Simulink model of central dc-link control loop and reference generation

6.5 Simulation and experimental validation

The simulation and experimental validations were performed on the setup using the same set of batteries as in earlier chapters.

6.5.1 Lyapunov based control approach

The lyapunov function based approach has been validated using the theory from in 6.4.2

under extreme conditions to prove stability. The starting SOC were kept to approximately to similar values as before. $OCV_{o,1} = 9.9V$, $OCV_{o,2} = 22.0V$ and $OCV_{o,3} = 5.9V$ during discharging and $OCV_{o,1} = 13.3V$, $OCV_{o,2} = 26.0V$ and $OCV_{o,3} = 8.25V$ during charging. The responses using the proposed control approach have been shown in Fig. 6.18 and Fig. 6.19 for discharging and charging mode respectively. There is a noticeable improvement in terms of dynamic response compared to Fig. 6.12 and Fig. 6.13. The time scale both in simulation and experiments are same as with Fig. 6.12 and Fig. 6.13 to help comparison with the adaptive PI-controller based approach.

Moreover, the charging to discharging transition and discharging to charging conditions were also captured as shown in Fig. 6.20 and Fig. 6.21. It can be seen that smooth and fast transition as well as fast dynamic response even at the extreme conditions are possible. The overall response time of the energy storage system from the charging to discharging transition and vice-versa was found to be around 18 – 20ms and a settling time around 30ms which is faster compared to a conventional approach under these conditions. Importantly this response time is found to be more uniform throughout the operating points irrespective of parameter variations. The value of K in this Lyapunov control has been chosen differently for different modules to keep a uniform response time for all the modules according to (6.43) assuming the maximum current measurement error and the voltage measurement error ϵ_1 , ϵ_2 to be around 20% and 10% respectively.

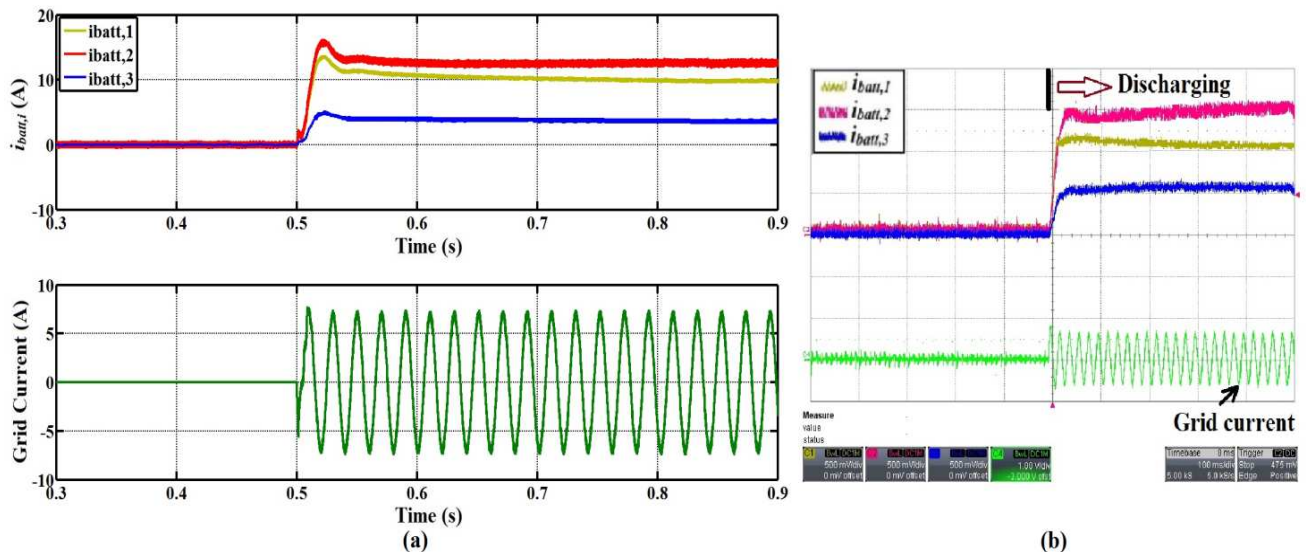


Fig. 6.18 Lyapunov controller in discharging: a) simulation study, b) experimental study $OCV_{o,1} = 9.9V$, $OCV_{o,2} = 20.2V$, $OCV_{o,3} = 5.9V$: scale 100ms/div, grid current 10A/div, module currents 5A/div

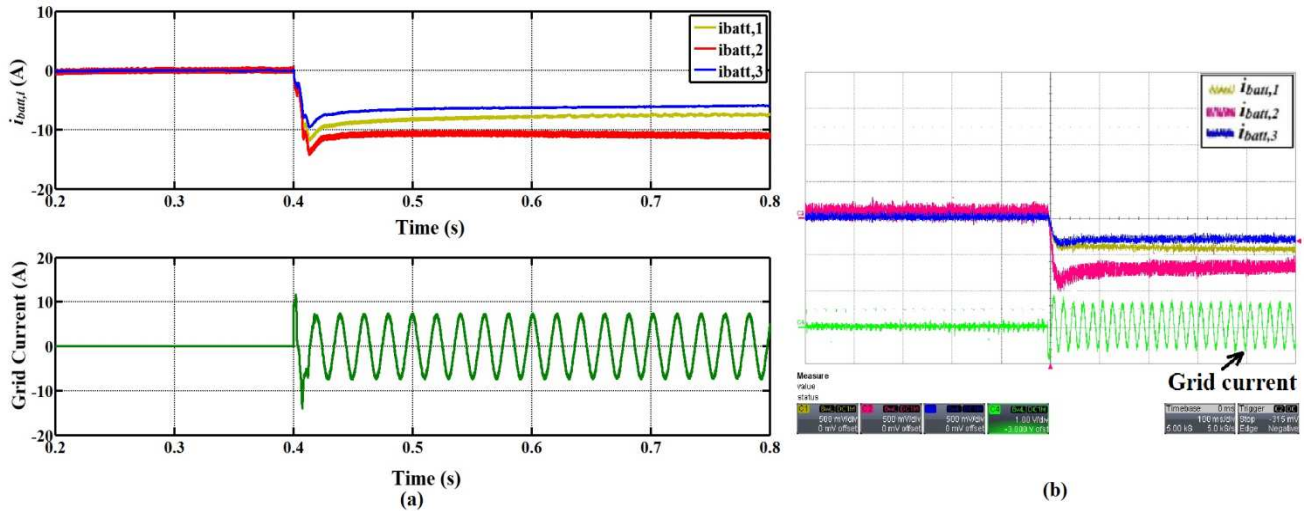


Fig. 6.19 Lyapunov controller in charging: a) simulation study, b) experimental study $OCV_{o,1} = 13.4V$, $OCV_{o,2} = 26.2V$, $OCV_{o,3} = 8V$: scale 100ms/div, grid current 10A/div, module currents 5A/div

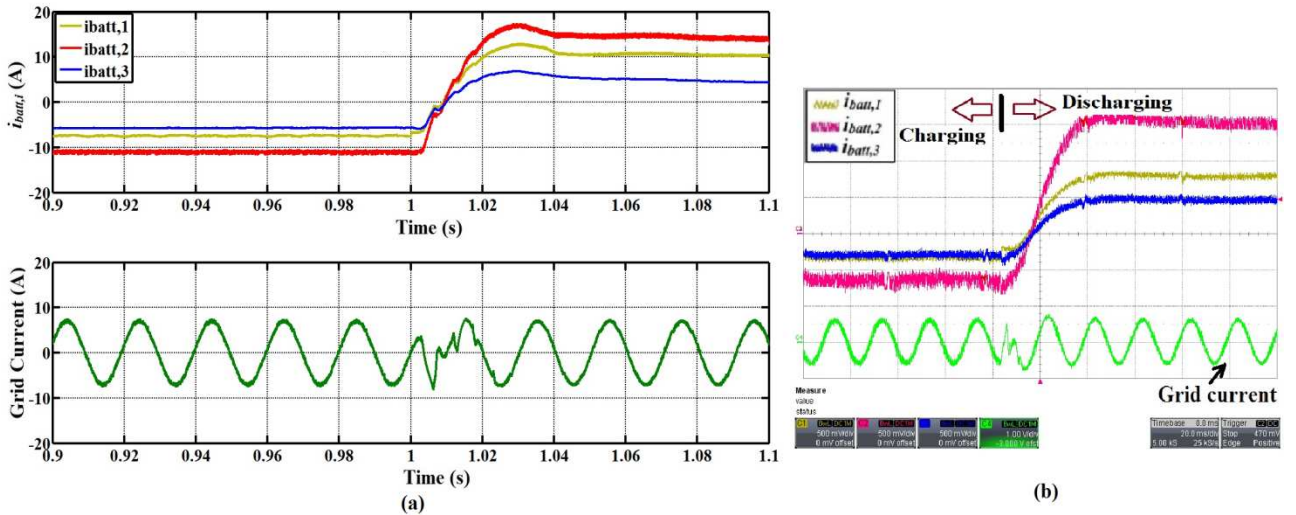


Fig. 6.20 Lyapunov controller during charging to discharging: a) simulation study, b) experimental study $OCV_{o,1} = 9.8V$, $OCV_{o,2} = 22.0V$, $OCV_{o,3} = 6.1V$: scale 20ms/div, grid current 10A/div, module currents 5A/div

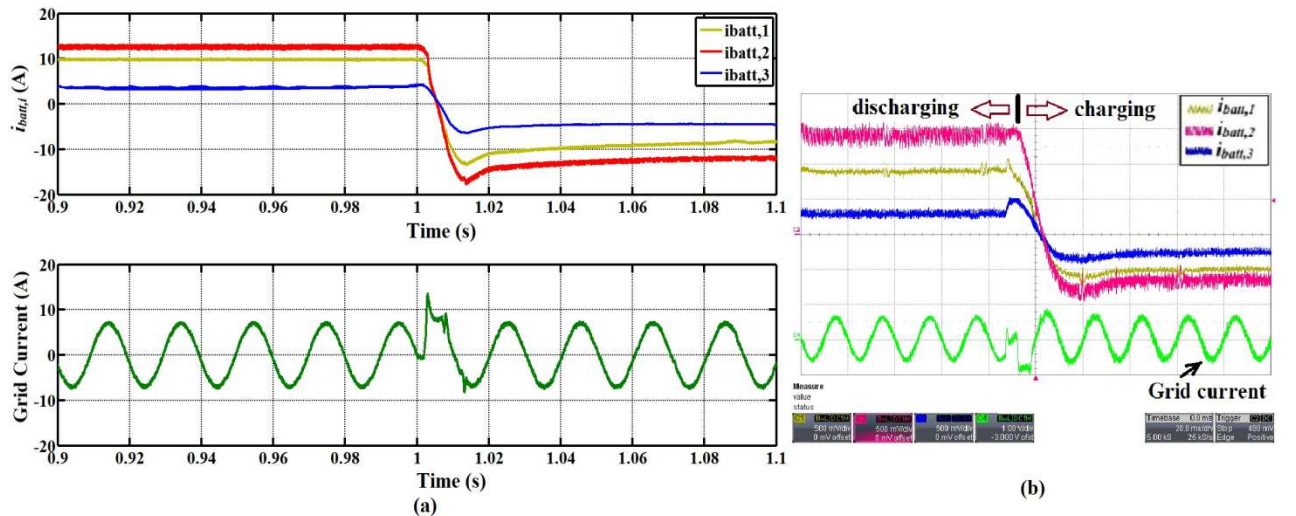


Fig. 6.21 Lyapunov controller during discharging to charging: a) simulation study, b) experimental study $OCV_{o,1} = 13.8V$, $OCV_{o,2} = 27.2V$, $OCV_{o,3} = 8.3V$: scale 20ms/div, grid current 10A/div, module currents 5A/div

The effect of the variation of the control parameter in the Lyapunov control has been experimentally investigated to validate the theory presented 6.4.2.1 and 6.4.2.2. The result is presented in two stages: a) increasing K , b) decreasing K . Fig. 6.22 shows the effect of increase of K . The value of K of module – 2 has been varied from a designed value ($K = 0.015$) to a higher value ($K=0.04$). It can be seen that the ripple content increases due to the variation and steady-state value also gets affected. However, there is no effect on stability or ripple on other modules as expected. A similar result can be obtained in charging mode also. The effect of decreasing K has been shown in Fig. 6.23. The value of K of module – 3 has been reduced from 0.045 to 0.005. It was found that a very low value of K creates stability problem. Therefore, it can be concluded that there is a minimum K is needed to ensure the system stability. Moreover, it is interesting to note that if one module goes unstable, it also impacts the stability of the other modules because the module capacitor voltages are in series as discussed earlier in the chapter. Therefore, it is essential to keep the stability of all the modules. It can be seen that the Lyapunov approach not only overcomes the stability problem but it also maintains a more uniform dynamic response throughout the battery operating conditions assuming suitable values of K . It is important to note that by choosing an appropriate value of K can eliminate any need for online tuning in the proposed approach which simplifies the control complexity and parameter dependency.

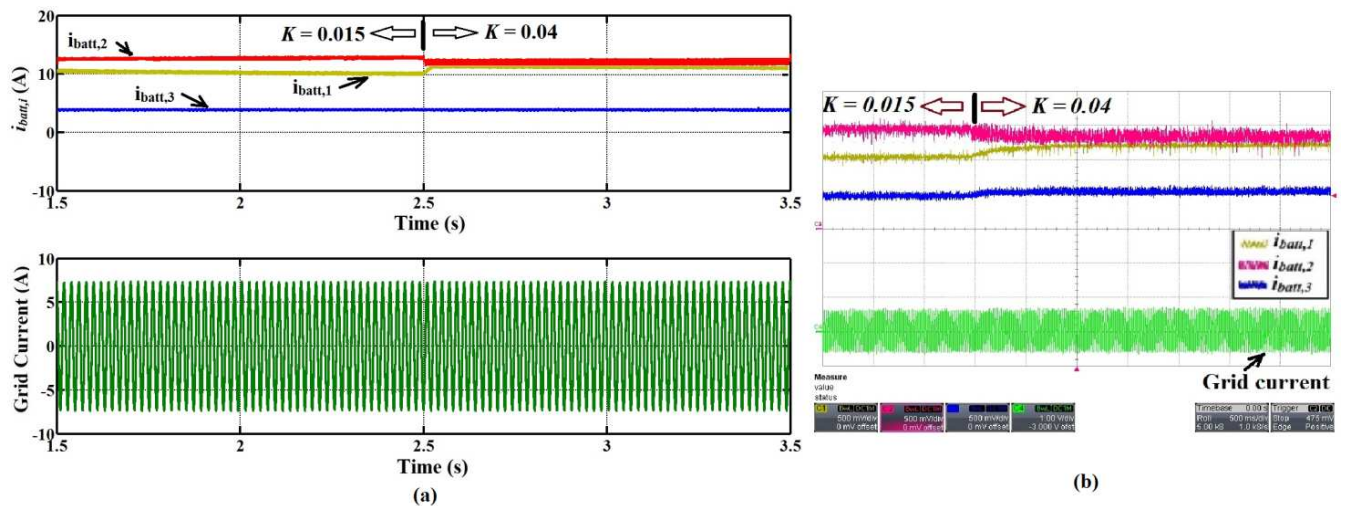


Fig. 6.22 Effect of very high value of K : a) simulation study, b) experimental study of variation of K for module – 3: scale 500ms/div, grid current 10A/div, module currents 5A/div

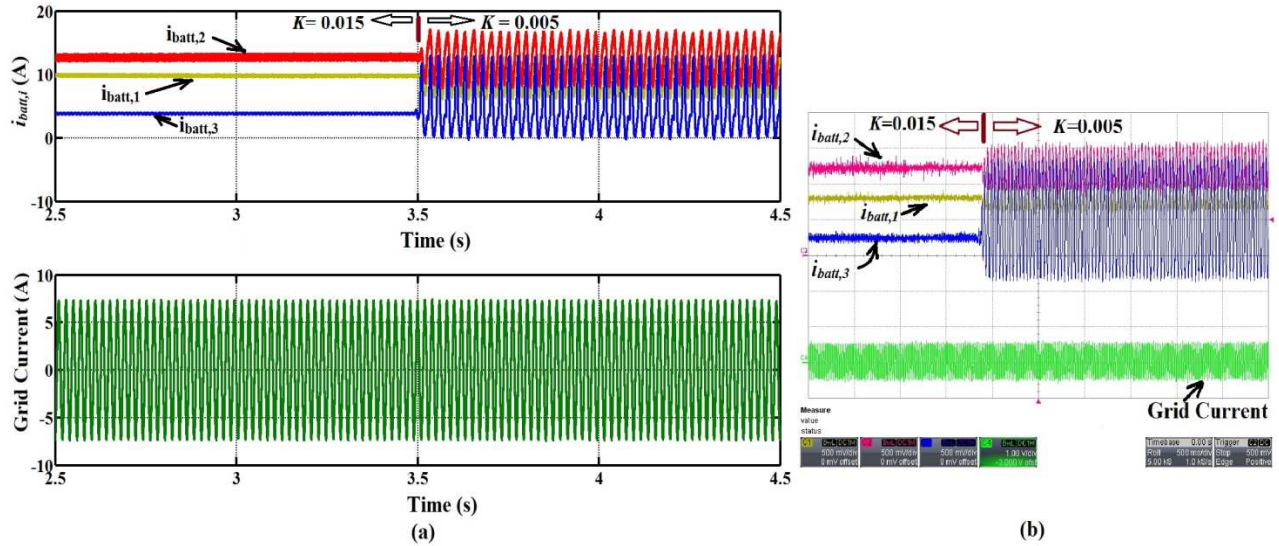


Fig. 6.23 Effect of very low value of K : a) simulation study, b) experimental study of variation of K for module – 3: scale 500ms/div, grid current 10A/div, module currents 5A/div

Converter dynamic response or response time using the proposed control approach has been investigated experimentally and can be compared to that in section 6.4.2.1. Fig. 6.24 shows a transition from the charging to discharging both in simulation and experiments. It can be seen that the response time of the overall energy storage system is 22ms in simulation and 24ms in experiments under normal operation. However, the response time can increase if a low value of K is used. The value of K in module – 3 was changed from the designed value 0.045 to 0.02 with a corresponding increase in response time increases from 22ms to 32ms in simulation and 24ms to 40ms in experimental conditions.

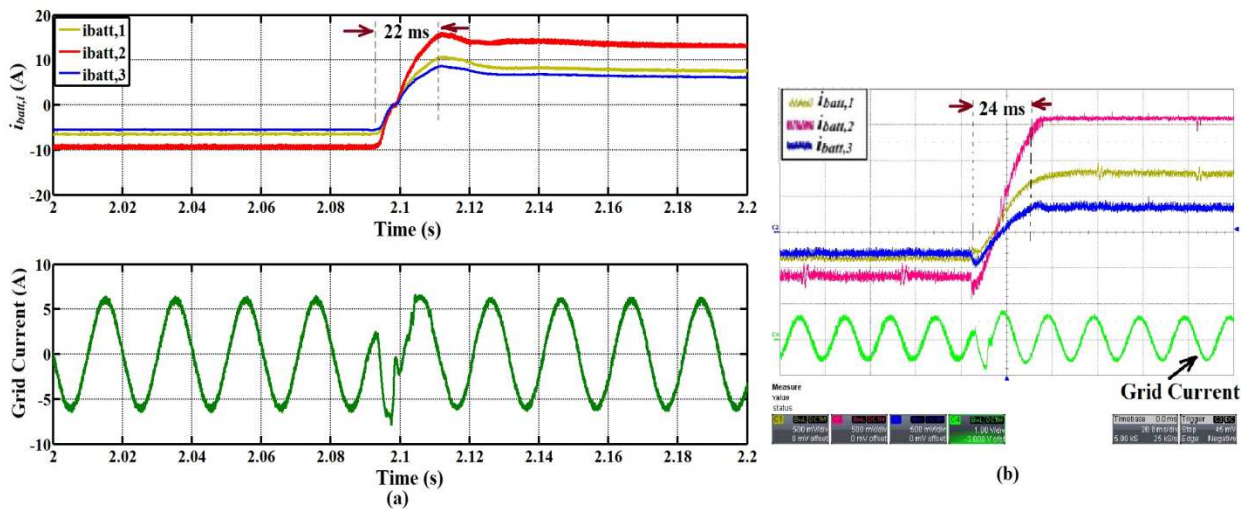


Fig. 6.24 Test of dynamic response – 1: a) simulation study, b) experimental study scale 20ms/div, grid current 10A/div, module currents 5A/div

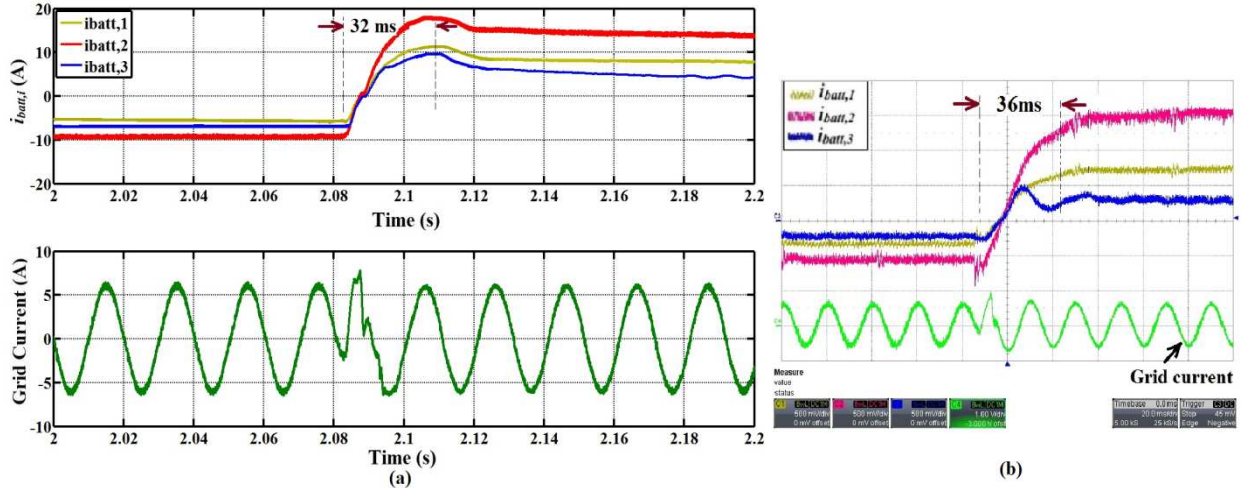


Fig. 6.25 Test of dynamic response – 2: a) simulation study, b) experimental study scale 20ms/div, grid current 10A/div, module currents 5A/div

6.6 Stability of boost-buck mode

6.6.1 Boost converter analysis

The distributed control structure of the boost-buck mode was described in chapter 5, is based on distributed duty ratio operation of the multilevel buck converter switches. The module voltage control loop is shown in Fig. 6.26.

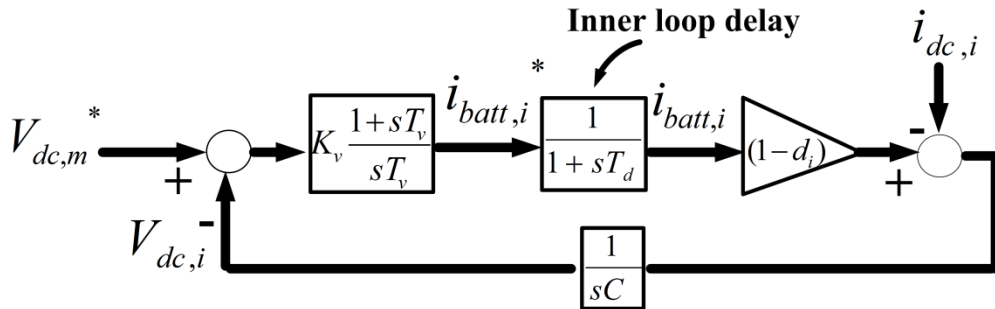


Fig. 6.26 Module voltage control loop in boost-buck mode

Each module consists of two similar cascaded control loops: a) a slow outer voltage module voltage loop and b) a fast inner current loop. The associated inner current loop delay (e^{-sT_d}) has been taken as four times of the sample time (T_s) in this case also. The open loop transfer function for the voltage control loop can be derived as shown in (6.45) from Fig. 6.26. It can be seen that the open loop transfer function $GH_v(s)$ depends $V_{dc,i}$ and $V_{batt,i}$ as in the boost of operation.

$$GH_v(s) = K_v \left(\frac{1+sT_v}{sT_v} \right) \left(\frac{1}{1+sT_d} \right) \left(\frac{V_{batt,i}}{V_{dc,i}} \right) \left(\frac{1}{sC} \right) \quad (6.45)$$

Similarly, the current loop is shown in Fig. 6.27. A proportional controller is considered in the inner current loop for a fast response and stability. The open loop transfer is shown in (6.46) where G is the converter gain ($\propto V_{dc,i}$).

$$GH_I(s) = K_c \frac{1}{G} \frac{i_{batt,i}}{(1-D_i)} \frac{1+s \frac{V_{dc,i}C}{(1-D_i)i_{batt,i}}}{1+s^2 \frac{LC}{(1-D_i)^2}} \quad (6.46)$$

It should be noted that in this mode of operation, the module voltage reference $V_{dc,m}^*$ and in turn, $V_{dc,i}$ are independent of battery weighting factor ω_i . Therefore, the variation of ω_i does not influence the control loop performance because the open loop gain $K_v \frac{1}{C} \left(\frac{V_{batt,i}}{V_{dc,i}} \right)$ remains unaffected by the variation of ω_i . As a result, the outer voltage loop bandwidth or the gain crossover frequency remains fixed at the designed value all the time. Similarly the current loop bandwidth according to (6.12) is always fixed by the inductor value and K_c . Therefore, the relative bandwidth between the voltage and current loop remains fixed all the time which guarantees stable operation of the module boost converter.

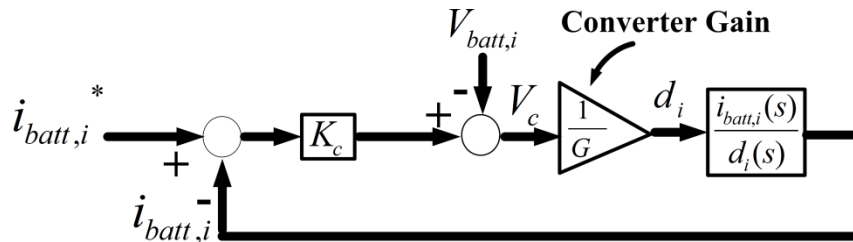


Fig. 6.27 Module current control loop in boost-buck mode

6.6.2 Multilevel buck converter analysis

The control of the multilevel buck converter is shown in Fig. 6.28. It employs a slow outer central dc-link voltage loop and a fast inner dc-link current loop. The open loop transfer function is derived in (6.47) from Fig. 6.26. It is important to note that the open loop gain of the voltage control $K_{dc} \frac{1}{C_{dc}}$ is completely independent of the battery weighting factor and remains always fixed for a fixed K_{dc} . On the other hand, the inner current loop transfer function is shown in (48). The transfer function can be approximated at high frequency to get the current loop bandwidth as shown in (6.49). It can be seen that buck converter's inner loop bandwidth is also independent of battery weighting factor.

Therefore, the stability of the multilevel buck converter also remains affected by the battery weighting factor and this guarantees stability of the boost-buck mode under all operating conditions. Moreover, due to not having the stability problem, the dynamic response of the boost-buck mode will be better than the boost when using PI-controllers. However, the dynamic response of the boost mode can be made faster using a Lyapunov approach if required. The stability based comparison between the two control modes has been presented in Table 6-1.

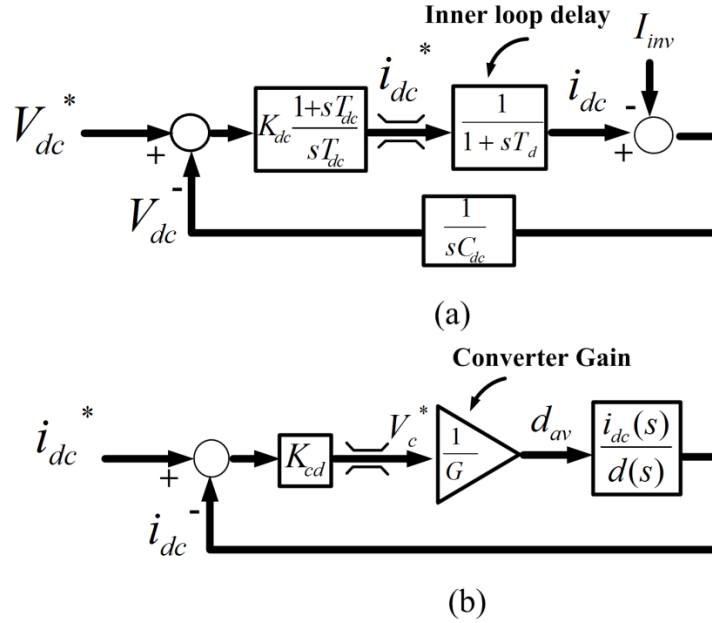


Fig. 6.28 Control loop for the multilevel buck converter: a) outer dc-link voltage loop, b) inner current loop

$$GH_{dc-v}(s) = K_{dc} \left(\frac{1+sT_{dc}}{sT_{dc}} \right) \left(\frac{1}{1+sT_d} \right) \left(\frac{1}{sC_{dc}} \right) \quad (6.47)$$

$$GH_{dc-I}(s) = K_{cd} \left(\frac{1}{G} \right) \frac{\sum V_{dc,i}}{I_{inv}} \left(\frac{1+sC_{dc} \frac{V_{dc}}{I_{inv}}}{1+s \frac{L_{dc}}{V_{dc}} + s^2 LC} \right) \quad (6.48)$$

$$GH_{dc-I}(s)|_{\omega \rightarrow \infty} \approx K_{cd} \frac{1}{sL_{dc}} \quad (6.49)$$

Table 6-1 Stability comparison between the boost and boost-buck mode of operation

Mode of operation	Stability issue	Mitigation	Dynamic response
Cascaded Boost	Due to outer voltage loop bandwidth variation	Adaptive PI control Lyapunov based control	Limited due to the stability issue in PI controller based approach but lyapunov based design provides a better response
Boost-multilevel buck	N/A	N/A	Good dynamic response

6.7 Conclusion

This chapter reports on a stability problem with the distributed control structure of hybrid second life battery energy storage system in boost mode. It was found that the variation of SOC or open circuit voltage and capacity degradation could give rise to a control stability problem at a module level and/or system level when using the conventional cascaded control loop approach in boost mode. Two solutions have been discussed: a) an adaptive PI controller

based approach where the stability is improved by varying controller parameters according to the system parameters and b) control Lyapunov function based approach where stability is always guaranteed irrespective of the system parameters. It was found that the accuracy of the adaptive PI based approach is dependent on the system parameters which can cause either poor dynamic response or steady-state errors.

It was found that a Lyapunov based control approach is better than the adaptive PI-approach in performance in this application where widely different batteries are integrated because this approach is capable of providing a fast dynamic response without compromising the stability irrespective of operating points. A detailed design and analysis of the proposed approach has been presented. A detailed simulation and experimental studies have been performed to validate the proposed claims.

On the other hand, the stability of a boost-buck mode has also been analysed. It is found that the control stability of the boost-buck mode remains unaffected by battery parameter change or weighting factor variation. Therefore, the boost-buck control mode is a more stable mode of operation compared to the boost mode of operation with the conventional PI controller in the current context.

7 Hardware Implementation

7.1 Introduction

This chapter presents the hardware design and details used in the experimental implementation of the hybrid battery energy storage system. The power converter described in chapter 3 is modular in nature on the dc-side with a single inverter on the grid side. Therefore, the overall converter hardware design consists of: a) hybrid battery modules which were described in chapter 4, b) modular dc-dc converters, and c) the inverter. The associated hardware based and software based protection for the battery, inverter and modular dc-dc converter have to be included. The system architecture and controller interface with the modular converter have also been discussed in detailed.

The system architecture consists of two-stages: a) boost mode and b) boost-buck mode as shown in Fig. 7.1 which shows all the input, outputs, sensed signals and their interface with the controller in the practical implementation. It can be seen that there are three signals sensed from each module and three signals from the line side inverter. Based on these sensed signals, the centralised controller generates the control signals/duty ratio command to control each module and the line side inverter as described in chapter – 5 and chapter – 6. It can be seen from that there are additional control signals/duty ratios d_{11} , d_{22} ... d_{mn} generated in boost-buck mode.

Table 7-1 shows the maximum rating of the dc-side and ac-side voltages and currents of the designed laboratory prototype. . Fig. 7.2 shows the operational envelope. The minimum and maximum battery modules are set to 7.2V, 6.5Ah and 24V, 60Ah respectively to encompass the battery types that are readily available. Since the 24V, 60Ah module take a higher share of input current and output voltages during the distributed utilisation/control (described in chapter 5). Each converter module is designed according to this envelope. The hardware set-up is mainly designed to support 1kW power. The 24V battery which can reach up to 28V when fully charged. Therefore, the dc-side current is set to 35A when delivering the full power. The grid voltage is taken as 100V (rms) or 141V peak in the scaled-down laboratory based design.

Table 7-1 Rating specification for maximum 1kW laboratory prototype

	Absolute maximum rating
Power	1kW
Battery voltage (V_{batt})	28V
Output voltage of a dc-module ($V_{dc,i}$)	100V
Battery current (I_{batt})	35A
Inverter Dc-link voltage (V_{dc})	200V
Ac-side voltage (V_s)	100V (rms)/ 141V peak
Ac-side current (I_s)	10A (rms)/ 14A peak

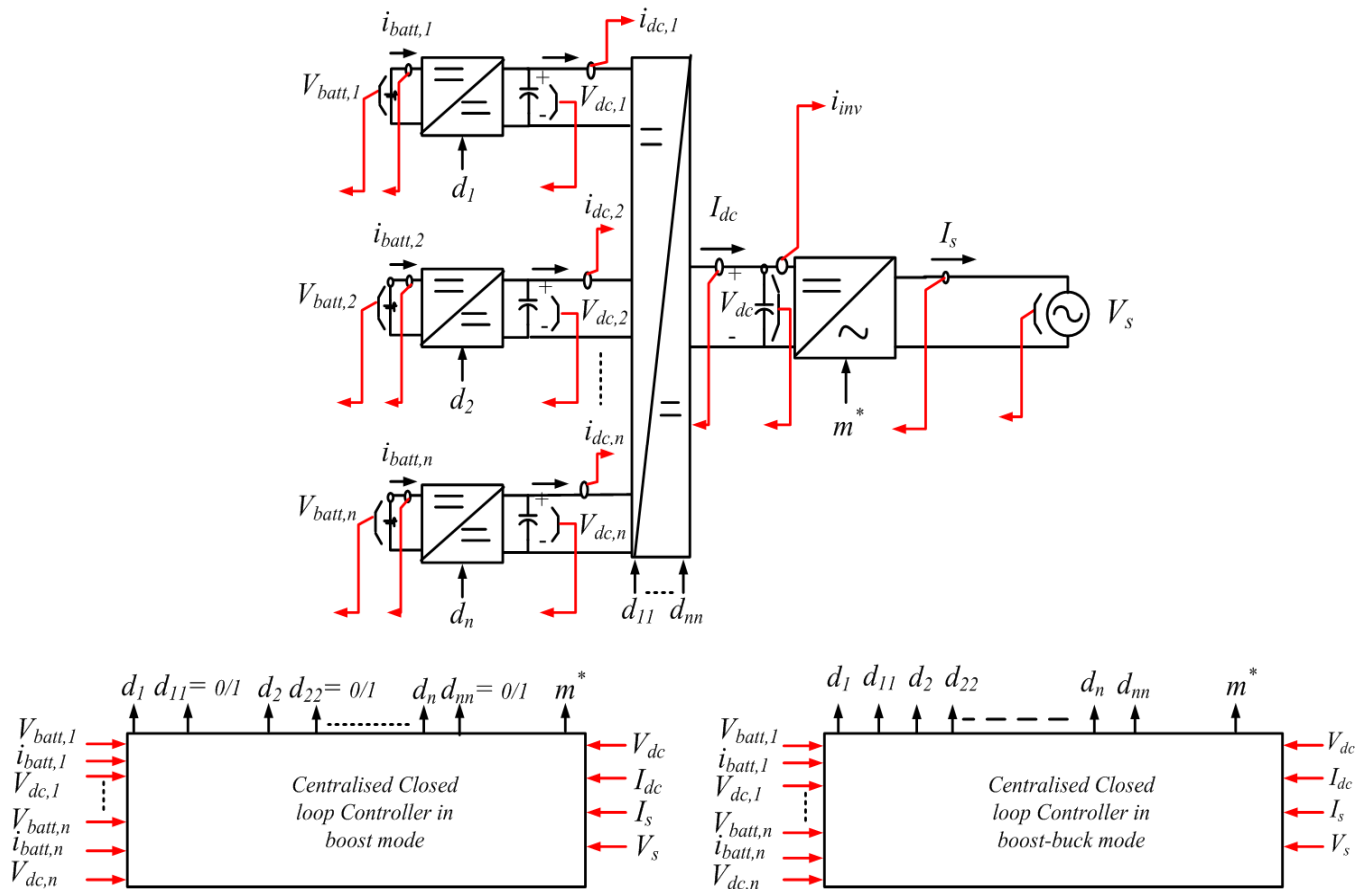


Fig. 7.1 System architecture implemented

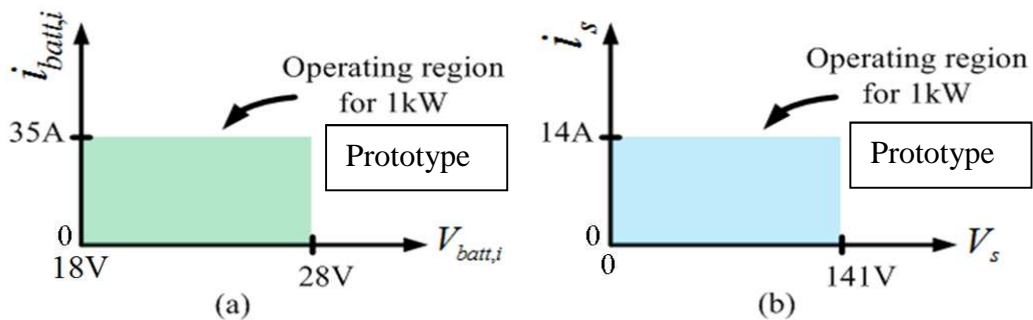


Fig. 7.2 Operational envelope for 1kW prototype: a) input side region, b) output side region

7.2 Converter design

7.2.1 Dc-dc Converter module design

Each dc-dc converter module schematic is shown in Fig. 7.3 which consists of an H-bridge where devices of identical rating are used. The current handled by S_i , S_{ii} is different from T_i , T_{ii} because the module current ($i_{batt,i}$) is generally higher than the dc-link current (I_{dc}) due to boost operation. Therefore, the rating was set on maximum module dc-link voltage $V_{dc,i}$ and maximum module input current $i_{batt,i}$.

The laboratory built H-bridge module with integrated driver and sensor is shown in Fig. 7.4. The components used in the H-bridge dc-dc are shown in Table 7-2. A 100V, 40A OptiMOS is used because it is one of the most efficient devices available within the voltage and current specification. 35A is the maximum current that a module can draw under worst situation. A 2700 μ F, 100V capacitor is used as it is one of the standard capacitor value available at this range and above the designed value calculated in chapter 3. Each module has four integrated drivers. Each driver consists of a driver ic and isolated dc-dc converter (5 to +/-15V). A low-cost isolated Opto-coupler HCPL 3150 has used (isolation up to 1kV) to drive the MOSFETs. This driver has a low peak current delivering capacity (e.g. 0.5A) which suits driving a low voltage MOSFETs which has very low gate charge. There is a current sensor in the PCB to measure the dc-link current ($i_{dc,i}$) of the H-bridge for protection purpose. An HX-25P PCB based sensor was chosen because it has a small in size, good isolation voltage (3kV), good accuracy (+/-1%) and good bandwidth (50 kHz).

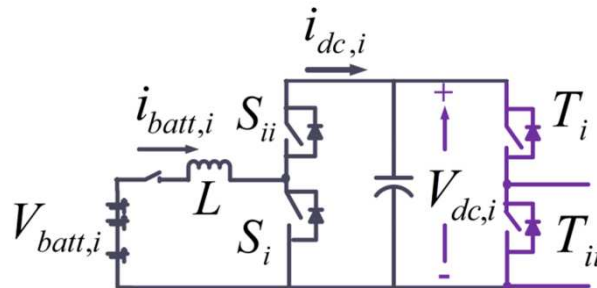


Fig. 7.3 One converter module

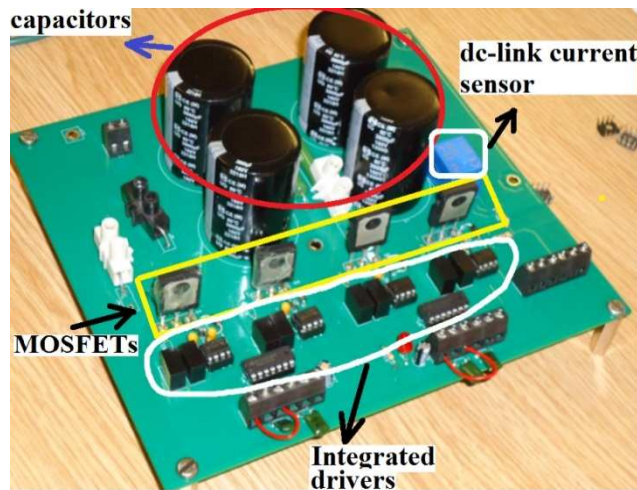


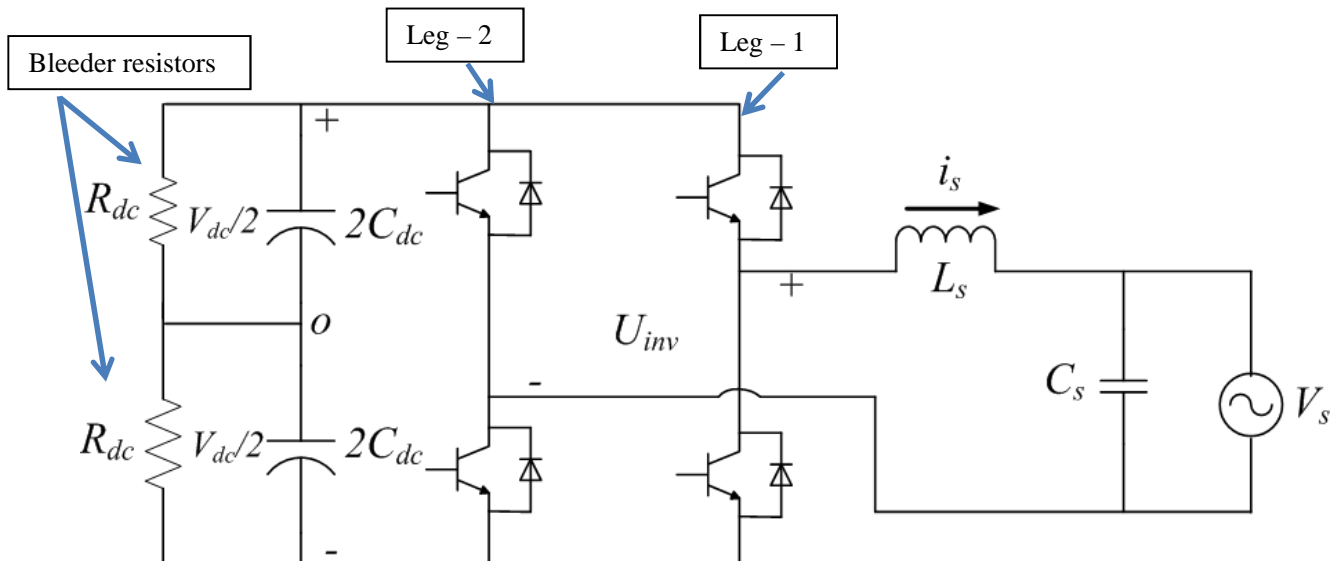
Fig. 7.4 Laboratory built converter module with integrated driver

Table 7-2 Components used per H-bridge dc-dc module

Components/Type	Specification
Switches (MOSFET), package TO 220	100V 40A (FDPF085N10A)
Drivers	HCPL 3150 (0.5A peak current driver)
Capacitors	2700 μ F, 200V Electrolytic
Isolated dc-dc converter for driver	IES0515S (15V)
PCB sensor	HX-25-P, up to 50A (Isolation voltage 3kV, Bandwidth 50kHz, accuracy $\pm 1\%$)

7.2.2 Grid-tie Inverter design

The single phase grid connected inverter used in the present work is shown in Fig. 7.5. The inverter is made of three-stages: a) PWM/modulation method, b) line side EMI filters, c) dc-link capacitor with bleeder resistors. Packaging and earth leakage have been not considered because the design and experiments done in laboratory based environment. However, it should be carefully considered in real operating conditions. The description of each one is provided in detailed.

**Fig. 7.5 Grid-tie single phase inverter**

7.2.2.1 Modulation method for grid-tie inverter

A single phase grid-tie inverter (Fig. 7.5) can have two types of modulation methods: a) unipolar PWM and b) bipolar PWM. Both are generated using a carrier based method as described in [382]. In unipolar PWM method have three states at the output U_{inv} such as, zero, $+V_{dc}$ and $-V_{dc}$ whereas the bipolar PWM method can have only two states at the output e.g. $+V_{dc}$ and $-V_{dc}$. This means in unipolar PWM method, all the switches except the top and bottom switches of a leg can be turned ON/OFF at the same time whereas, in bipolar PWM

method, only the top switch of a leg and the bottom switch of another leg are turned ON/OFF at the same time. The expression of duty ratios of an inverter leg can be written in (7.1) – (7.2) for bipolar and unipolar PWM methods respectively. Note: bipolar PWM has only one expression of duty ratio while the unipolar one has two different duty expressions.

$$d = 0.5 + 0.5M \cos(\omega t) \quad (7.1)$$

$$d|_{leg1} = 0.5 + 0.5M \cos(\omega t), d|_{leg2} = 0.5 - 0.5M \cos(\omega t) \quad (7.2)$$

Where, M is the modulation index of the inverter ($= \frac{|V_s|}{V_{dc}}$). Both of the method is applicable in the grid-tie inverter. However, unipolar PWM suffer the drawback of increased common mode noise which can be a critical issue for the transformerless grid connected converter. Therefore, more advanced circuit may be required to reduce the common mode noise should this method be employed in transformerless grid connections as reported in [383]. On the other hand, the bipolar PWM method does not produce any common mode noise, therefore is a more preferred method in transformerless grid-tie converter. However, the later method has increased current ripple and slightly more switching losses compared to the former method. In this present work which aims for transformerless grid connection, bipolar PWM method has been chosen over the unipolar method.

7.2.2.2 EMI filter and its design

Grid connected two-level inverters produce a high amount switching noise due to their PWM operation therefore, an appropriate filter design is mandatory to meet the power quality standards such as, IEEE 519 or G5/4 etc. In the present work, an LC filter has been chosen over the traditional L filter in grid-tie operation because of better switching frequency attenuation.

The design of L_s has been performed to keep the current ripple on the grid side to be 5% of the fundamental (i_s). The nature of the current ripple is shown in Fig. 7.6. The expression (7.3) can be used to find the inductor L_s where D is the duty of one leg of the inverter.

$$L_s = \frac{V_{dc} D (1-D)}{f_s \Delta i_s} \quad (7.3)$$

The variation of current ripple with the duty ratio is shown in Fig. 7.7. It can be seen that the maximum ripple is at $D = 0.5$, therefore, substituting $D = 0.5$,

$$L_s|_{max} = \frac{V_{dc}}{4f_s \Delta i_s} \quad (7.4)$$

Now, in the present case, the operating dc-bus is taken as 150V, the maximum grid current 14A (Fig. 7.2). So, the required inductor will be according to (7.5).

$$L_s|_{max} = \frac{150}{4 \times 10 \times (0.05 \times 14)} = 5.3mH \quad (7.5)$$

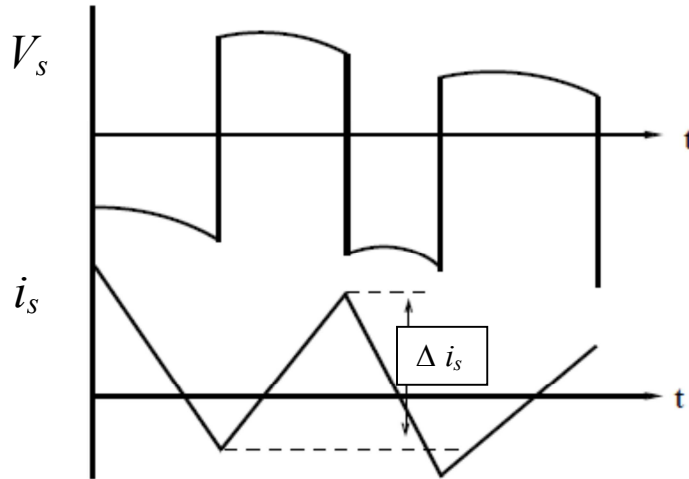


Fig. 7.6 Line side current ripple

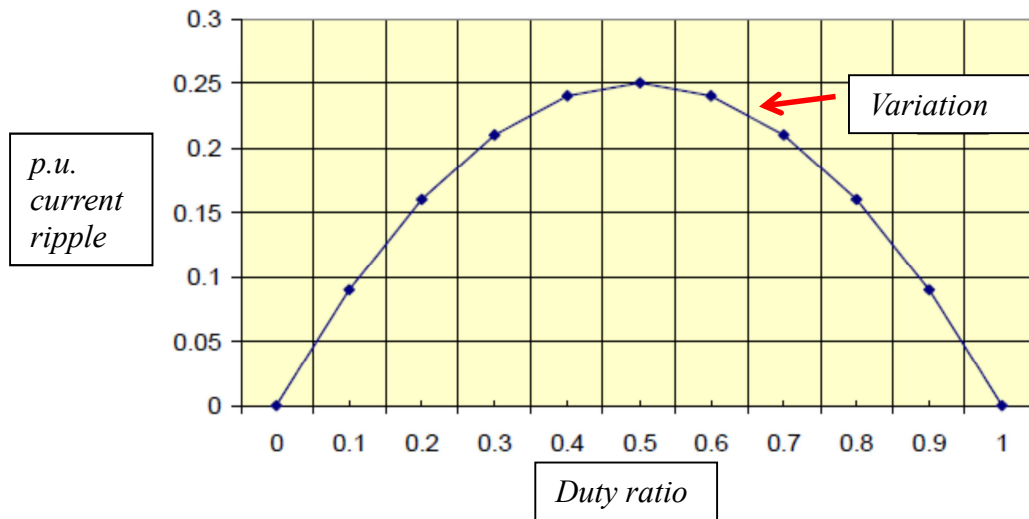


Fig. 7.7 Variation of output current ripple with the duty ratio of inverter leg

The line side capacitor (C_s) is designed from the cut-off frequency of the LC filter which is taken as the geometric mean of the fundamental and the switching frequency as shown in (7.6).

$$f_0 = \sqrt{f_{sw}f_s}, f_0 = \frac{1}{2\pi(\sqrt{L_s C_s})} \quad (7.6)$$

In this case, $f_s = 50 \text{ Hz}$ and $f_{sw} = 10 \text{ kHz}$, which sets $f_0 = 707 \text{ Hz}$. Therefore, the desired value of C_s will be,

$$C_s = \frac{1}{L_s(2\pi f_0)^2} = 10\mu\text{F} \quad (7.7)$$

Due to unavailability of single 5.3mH inductance, two 3mH inductors and one 10 μ F capacitor have been chosen for the grid connected inverter as shown in Table 7-3.

7.2.2.3 Dc-link capacitor and bleeder resistor design

Capacitor design: The ripple current in the bus link capacitor is essentially the same as the ripple current in the phase leg e.g. Δi_s because the same current flows through the dc-link capacitors. When the top left and bottom right switches in Fig. 7.5 are turned ON, the current flows from the bus link capacitor through the load/grid via top left and bottom right switches and returns to the bus link capacitor. Similarly, the current flows from the bus link capacitor through the load when the bottom left and top right switches are turned on. However, for single phase inverters there is an additional 100Hz ripple present in the dc-link capacitor because of double frequency ($2f_s$) component present in the power as illustrated in (7.8) – (7.9).

$$P = V_{sm} i_{sm} \cos^2(\omega t) = \frac{1}{2} V_{sm} i_{sm} (1 - \cos 2\omega t) \quad (7.8)$$

$$i_{dc} = \frac{1}{2} \frac{V_{sm} i_{sm}}{V_{dc}} (1 - \cos 2\omega t) = I_{dc} + \hat{i}_{dc}|_{100Hz} \quad (7.9)$$

Therefore, the total ripple current that the dc-link capacitor C_{dc} has to carry will be

$$\Delta i_{dc} = \sqrt{(\Delta i_s)^2 + (\hat{i}_{dc}|_{100Hz})^2} \quad (7.10)$$

Now that the ripple current in the dc-link capacitor is known, it is now simple to calculate the resulting dc-link capacitor ripple voltage ΔV_{dc} .

$$C_{dc} \frac{dV_{dc}}{dt} = \Delta i_{dc}, C_{dc} = \frac{\Delta i_{dc}}{\Delta V_{dc}} DT_s \quad (7.11)$$

Where, D is the duty ratio of one inverter leg. In the present case, maximum possible Δi_{dc} has been calculated below using the maximum grid voltage and grid current from Fig. 7.2,

$$\hat{i}_{dc}|_{max,100Hz} = \frac{1}{2} \frac{V_{sm} i_{sm}}{V_{dc}} = \frac{1}{2} \frac{141 \times 14}{150} = 6.58A$$

Therefore, C_{dc} can be designed using (7.9) assuming the $D_{max} \approx 1$,

$$C_{dc} = \frac{6.58 \times 100\mu}{1} = 658\mu F$$

This capacitor value is not standard size therefore 1200 μ F capacitance has been used in the hardware set-up.

Bleeder resistor design: The bleeder resistor (R_{dc}) across the dc-link capacitor performs two functions: a) discharge the dc-link voltage when the inverter is OFF, b) balance the capacitor voltages. Discharge time constant can be taken to design R_{dc} as follows:

Assume the discharged time constant is about 30sec. The designed value is provided in Table 7-3.

$$\Gamma = R_{dc}C_{dc} \approx 30\text{sec}, R_{dc} \approx \frac{15}{1.2\text{m}} = 25\text{ k}\Omega$$

7.2.2.4 Heat-sink design

Heat-sinks are mandatory for the line side inverter when using IGBTs because they are not efficient compared to the low voltage MOSFETs. The heat-sink design has been performed using the thermal model of Fig. 7.8 where all the IGBTs/devices in the inverter share the same heat-sink. The thermal coefficients have been used from the datasheets to design the heat-sink following the similar method to [382].

$$(\sum P)(\theta_{jc} + \theta_{cs} + \theta_{sa}) = T_j - T_A \quad (7.12)$$

Assuming the $T_j = 80^\circ\text{C}$ and $T_A = 20^\circ\text{C}$, the desired value of θ_{jA} can be found as shown below calculating the expected power loss in each device of the inverter. The power loss in each device has been estimated from the datasheet under operating condition to be around 10 – 15W.

$$\theta_{jA} = \frac{80-20}{50} = 1.2^\circ\text{C/W}$$

The value of the designed heat-sink is shown in Table 7-3.

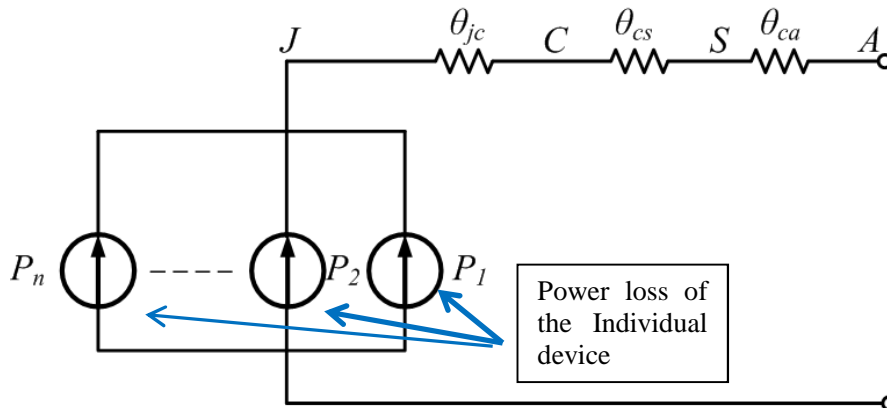


Fig. 7.8 Electrical equivalent circuit to design a common heat-sink for the inverter

The laboratory built inverter is shown in Fig. 7.9. The component ratings of the inverter are shown in Table 7-3. The inverter dc-link voltage is much higher than the dc-dc modules so IGBTs are used on the grid side instead of high voltage MOSFETs (>200V) which are expensive and inefficient because of their high reverse recovery losses. A 600V, 20A IGBT has been used because the inverter side maximum current is 14A (maximum 1kW operation at 100V grid) and 600V is a standard IGBT voltage level. A heat-sink has been used because IGBTs are not as efficient as low voltage MOSFETs. Moreover, a common heat-sink causes better heat dissipation than the individual heat-sinks. Apart from that, a different driver ic (HCPL 3120, 2A peak current) has been chosen to drive the IGBTs because they have a higher gate charge compared to the low voltage MOSFETs. The schematic of the inverter power circuitry has been provided in Appendix – 1 with integrated drivers.

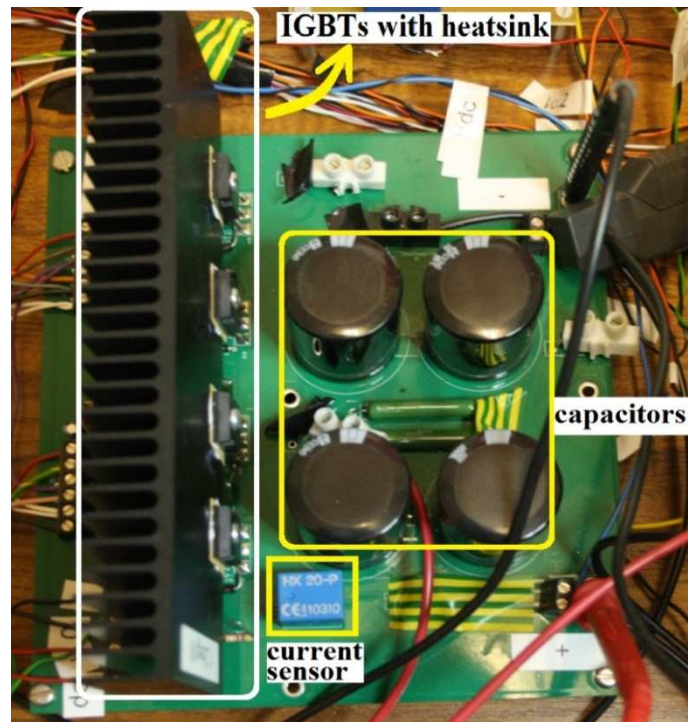


Fig. 7.9 Laboratory built line side inverter

Table 7-3 Components used in the inverter

Components/Type	Specification
Switches (IGBT), package TO – 247	600V 20A (FGH20N60UFD)
Drivers	HCPL 3120 (2.5A peak current)
Heat-sink	1.2deg/ ^o C
Line side filters	3mH, 3mH ($L_s/2$), 10 μ F (C_s)
dc-link capacitors (C_{dc})	1200 μ F, 200V Electrolytic
Bleeder resistor	25k Ω
Isolated dc-dc converter for driver	IES0515S (15V)
PCB current sensor	HX-20-P up to 50A (Bandwidth 50kHz, accuracy \pm 1%)

7.3 Protection

The protection strategy deals with each converter protection stage separately. The protection consists of three stages: a) protection in each battery module, b) protection on the modular dc-dc converter, c) protection on the line side (or at the inverter side). A comprehensive summary of the overall system protection is described in Table 7-4 and was generated by FMEA. All protection is undertaken in hardware with backup protection through the control system. There could be an additional battery side protection necessary in this kind application to avoid the reverse connection of a battery. However, such connection has not been

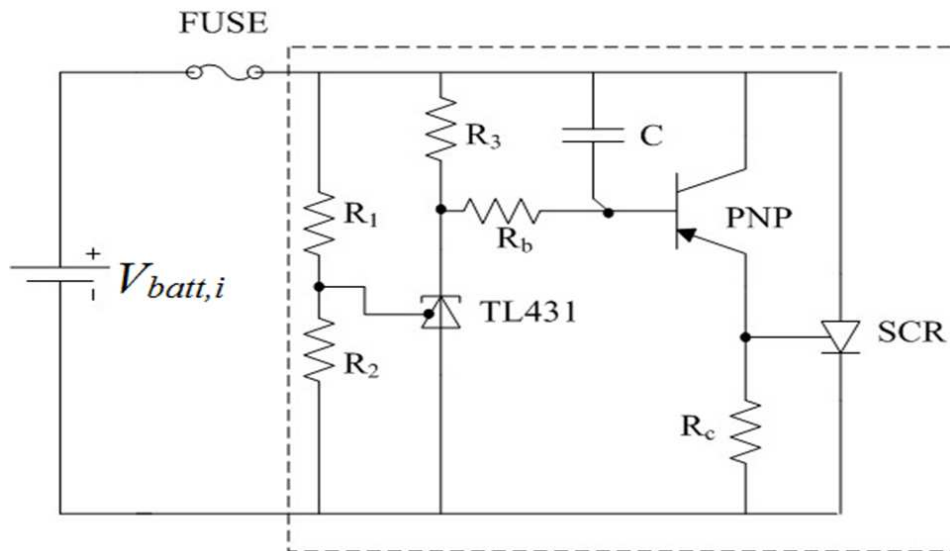
considered in this work and care has been taken to remove the faulty battery module in the laboratory environment. Future work may include this protection in detail.

Table 7-4 Different types of fault and proposed actions

Fault Types	Detection	Action taken
module input overvoltage	Picked up by $V_{batt,i}$	Trigger the Crowbar and disconnect the i^{th} module
module dc-link over voltage	Picked up by $V_{dc,i}$	Trip S_i, S_{ii} and bypass i^{th} module
module dc-link under voltage	Picked up by $V_{dc,i}$	Trip S_i, S_{ii} and bypass i^{th} module
module shoot-through	Picked up by $V_{dc,i}$ and/or $i_{dc,i}$	Trip S_i, S_{ii} and bypass i^{th} module
module battery side overcurrent	Picked up by $i_{dc,i}$	Trip S_i, S_{ii} and bypass i^{th} module
module battery side open circuit/short circuit	Picked up by $V_{batt,i}$	Trip S_i, S_{ii} and bypass i^{th} module
Overall dc-link overcurrent	Picked up by I_{dc}	Trip S_i, S_{ii} and Trip T_i, T_{ii} $\forall i = 1 \dots n$
Overall dc-link overvoltage	Picked up by V_{dc}	Trip the inverter
Grid side over current	Picked up by i_s	Trip the inverter
Inverter shoot-through	Picked up by i_{inv}	Trip the inverter
Battery open circuit failure	Picked up by $V_{dc,i}$	Bypass the module
Battery short circuit failure	Picked up $i_{batt,i}$	Trigger the crowbar + fuse+ bypass the module

7.3.1 Battery side protection

Depending on the battery operating condition, a battery module can have broadly two types of failure: a) open circuit failure, b) short-circuit failure as described in the Table 7-4. These two types of failure does not occur at the same time in the same battery, therefore, the battery module protection has to cope-up with both the failure modes. Three types of protections have been implemented for the second life battery modules: a) crow-bar protection for the over-voltage to avoid any sudden overvoltage which may occurs across the battery terminals, b) overcurrent or short circuit protection and c) open circuit failure protection based on online impedance estimation and/or comparing the battery terminal voltage ($V_{batt,i}$) with module dc-link voltage ($V_{dc,i}$). The protection schematics are shown in Fig. 7.10 and Fig. 7.11.



design: Self Powered Crowbar

R_1 & R_2 → To be decided upon based on over voltage limit OVL

$R_3 = 300\Omega$ & $R_b = 1k$, $C = 50nF$

$R_c = 1k$

PNP → BC560C

SCR → CS45 (800V, 75A)

Fig. 7.10 Crowbar protection

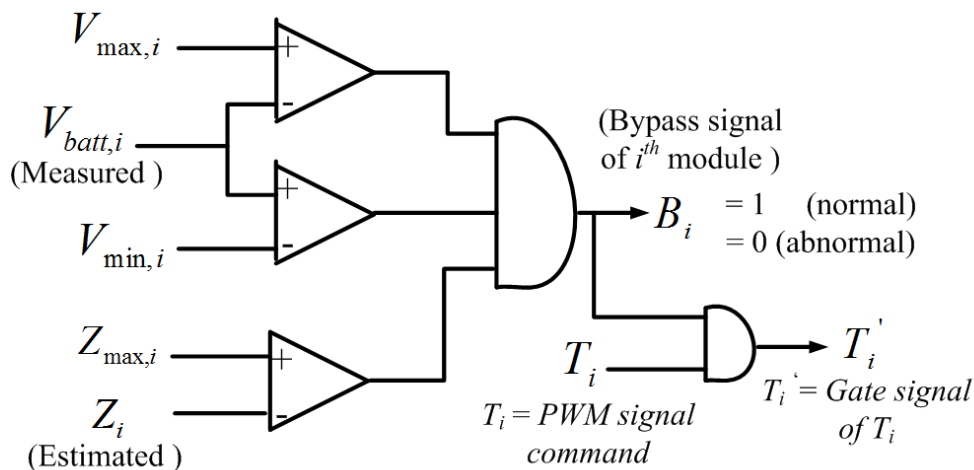


Fig. 7.11 logic circuit protection

7.3.2 Protection of modular dc-dc converter

The protection of the modular converter has been done on a per module basis. There is protection against two faults: a) overcurrent or shoot-through protections, b) overvoltage and under voltage protection. The protection logic schematic for each module is shown in Fig. 7.12 to incorporate all the converter protections. The laboratory built protection card is shown in Fig. 7.13. The protection settings are decided using a resistive divider circuit. The output from a voltage or current sensor circuit provides the input signals. The schematics of the

circuit diagram have been shown in Appendix – 1.

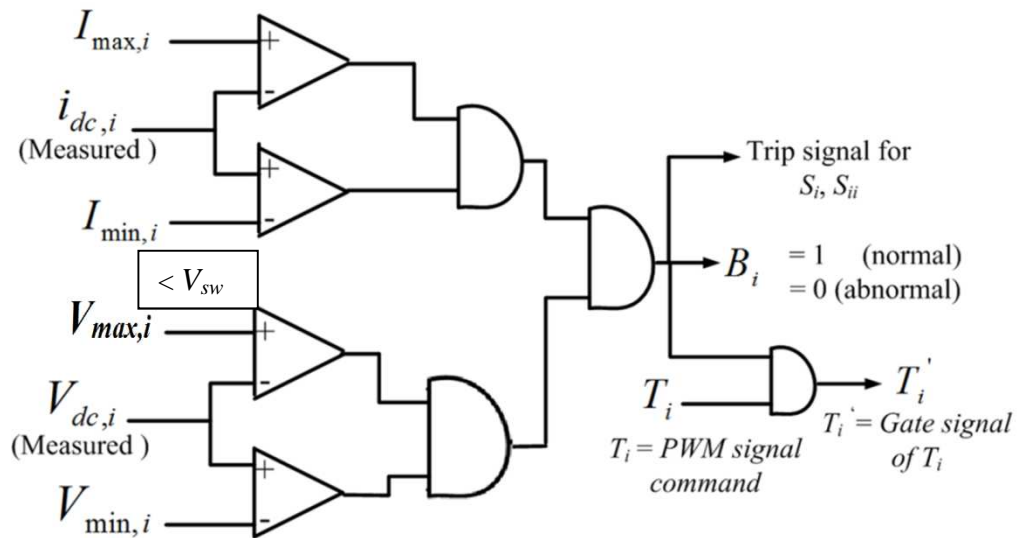


Fig. 7.12 Protection logic for each converter module

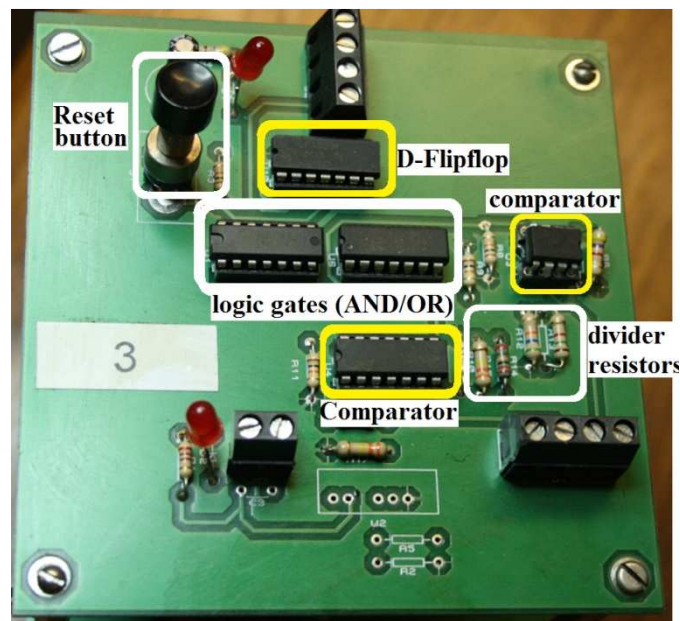


Fig. 7.13 Laboratory built protection card for one converter module

7.3.3 Protection of line side inverter

The protection of the line side inverter is designed for two faults: a) overcurrent or shoot-through fault, b) overvoltage/under voltage fault similar to the dc-dc converters. A separate protection card was built for the inverter to incorporate the necessary protection using the logic circuit shown in Fig. 7.14.

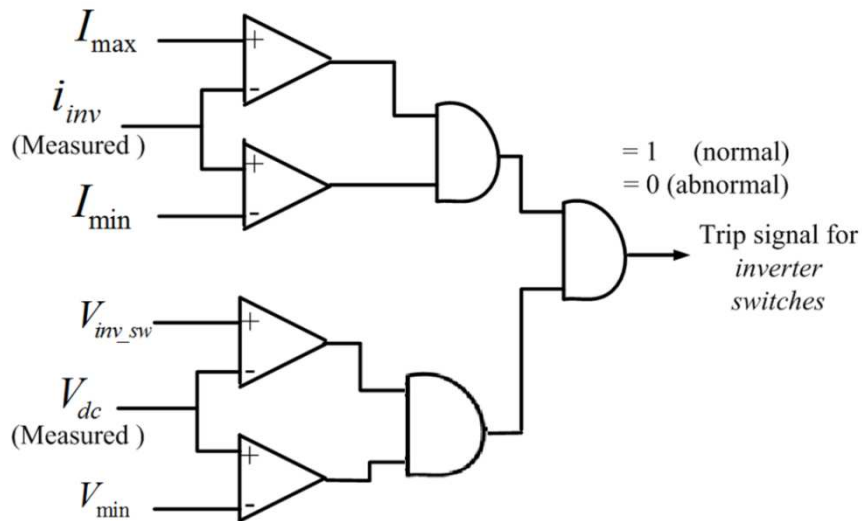


Fig. 7.14 Protection logic for the line side inverter

7.3.4 Shielding and fusing protections

Apart from the logic based protection for the converter and batteries, there is additional protection in the circuit: a) Fusing and b) shielding. This protection is needed to avoid any unforeseen failure of the converter and the batteries in case the logic based protection fails. Table 7-5 shows the details of such protections.

Table 7-5 Fusing and shielding protection

Type	Where	Why
Fuse	Converter module	To avoid direct short circuit of top and bottom devices + dc-bus capacitor short circuit
Fuse	Central power supply	Avoid any short circuit in the PCB board
Fuse	Between the inverter and the grid	To avoid grid short circuit + overcurrent
Fuse	Between the battery module and the converter module	To avoid short circuit of the bottom switch + battery short circuit failure + reverse connection of a battery
Shielding (Perspex cover)	Battery module	Avoid any chemical leakage + fire + explosion
Shielding (Perspex cover)	Overall converter	Avoid any damage due to external disturbances + fire

7.3.5 Sensors

Two types of sensors have been used in the experimental set-up: a) current sensors, b) voltage sensors. There are two types of current sensors are used: i) PCB type and ii) non-pcb type. The pcb type sensor (such as HX-25P) is used to detect the shoot-through between the top and the bottom switches whereas the non-pcb type sensors (LA-55P) are employed mainly for the control signals because it is a standard accurate, high bandwidth current sensor at these current levels. The voltage transducer (LV-25P) has been used for all the voltage

sensing because it has a good level of isolation (>3kV) and a high degree of accuracy ($\pm 1\%$).

7.4 Interfacing digital controller

An OPAL-RT based digital controller has been used to run the converter and to implement the closed loop control system. This controller has multiple in-built FPGA board to give a large number of I/O ports which is suitable for fast prototyping. The specifications of the controller are given in Table 7-6. It is programmed in Matlab and then that code is converted to VHDL to run the in-built FPGAs. The controller is interfaced with the pc through an Ethernet cable.

Table 7-6 Specification of OPAL-RT based digital controller

Type/Name of the board	Description	Specifications
OP5641 (x1)	OP5600 HIL Box real-time computer XEON Quad core 2.4 GHz , 4 cores	-
OP5340 (x3)	16-channels, 16-bit A/D	2.5 μ s sample time, ± 5 to ± 100 V input signal
OP5330 (x1)	16-channels, 16-bit D/A	1 μ s sample time, ± 1 to ± 16 V output
OP5353 (x2)	32-channels, digital input Opto-coupler	4.5V to 30V range
OP5354 (x4)	64-channels, digital output or PWM output	0 – 5V or 0 – 12V range

Table 7-7 Controller interface with the converter

Signal name	Type	Description	Input and output range from the sensors	Interface with OPAL-RT controller
$i_{batt,1}$	Analog	Battery current of module – 1	i/p: -40 / 40A (actual) o/p: -15/+ 15V (sensed)	Input to OPAL-RT
$i_{batt,2}$	Analog	Battery current of module – 2	i/p: -40 / 40A (actual) o/p: -15/+ 15V (sensed)	Input to OPAL-RT
$i_{batt,3}$	Analog	Battery current of module – 3	i/p: -40 / 40A (actual) o/p: -15/+ 15V (sensed)	Input to OPAL-RT
$i_{batt,4}$	Analog	Battery current of module – 4	i/p: -40 / 40A (actual) o/p: -15/+ 15V (sensed)	Input to OPAL-RT
$V_{batt,1}$	Analog	Battery voltage of module – 1	i/p: 0 – 30V (actual) o/p: 0 – 15V (sensed)	Input to OPAL-RT
$V_{batt,2}$	Analog	Battery voltage of module – 2	i/p: 0 – 30V (actual) o/p: 0 – 15V (sensed)	Input to OPAL-RT
$V_{batt,3}$	Analog	Battery voltage of module – 3	i/p: 0 – 30V (actual) o/p: 0 – 15V (sensed)	Input to OPAL-RT
$V_{batt,4}$	Analog	Battery voltage of module – 4	i/p: 0 – 30V (actual) o/p: 0 – 15V (sensed)	Input to OPAL-RT
$V_{dc,1}$	Analog	Capacitor voltage of module – 1	i/p: 0 – 100V (actual) o/p: 0 – 15V (sensed)	Input to OPAL-RT
$V_{dc,2}$	Analog	Capacitor voltage of module – 2	i/p: 0 – 100V (actual) o/p: 0 – 15V (sensed)	Input to OPAL-RT
$V_{dc,3}$	Analog	Capacitor voltage of module – 3	i/p: 0 – 100V (actual) o/p: 0 – 15V (sensed)	Input to OPAL-RT
$V_{dc,4}$	Analog	Capacitor voltage of module – 4	i/p: 0 – 100V (actual) o/p: 0 – 15V (sensed)	Input to OPAL-RT

V_{dc}	Analog	Inverter dc-link voltage	i/p: 0 – 200V (actual) o/p: 0 – 15V (sensed)	Input to OPAL-RT
V_s	Analog	Line side voltage	i/p: 0 – 200V (actual) o/p: 0 – 15V (sensed)	Input to OPAL-RT
i_s	Analog	Line side current	i/p: -20/20A (actual) o/p: -15/15V (sensed)	Input to OPAL-RT
S_1	Digital	Gate pulse for S_1	o/p: 0 – 5V	Output from OPAL-RT
S_{11}	Digital	Gate pulse for S_{11}	o/p: 0 – 5V	Output from OPAL-RT
S_2	Digital	Gate pulse for S_2	o/p: 0 – 5V	Output from OPAL-RT
S_{22}	Digital	Gate pulse for S_{22}	o/p: 0 – 5V	Output from OPAL-RT
S_3	Digital	Gate pulse for S_3	o/p: 0 – 5V	Output from OPAL-RT
S_{33}	Digital	Gate pulse for S_{33}	o/p: 0 – 5V	Output from OPAL-RT
S_4	Digital	Gate pulse for S_4	o/p: 0 – 5V	Output from OPAL-RT
S_{44}	Digital	Gate pulse for S_{44}	o/p: 0 – 5V	Output from OPAL-RT
T_1	Digital	Gate pulse for T_1	o/p: 0 – 5V	Output from OPAL-RT
T_{11}	Digital	Gate pulse for T_{11}	o/p: 0 – 5V	Output from OPAL-RT
T_2	Digital	Gate pulse for T_2	o/p: 0 – 5V	Output from OPAL-RT
T_{22}	Digital	Gate pulse for T_{22}	o/p: 0 – 5V	Output from OPAL-RT
T_3	Digital	Gate pulse for T_3	o/p: 0 – 5V	Output from OPAL-RT
T_{33}	Digital	Gate pulse for T_{33}	o/p: 0 – 5V	Output from OPAL-RT
T_4	Digital	Gate pulse for T_4	o/p: 0 – 5V	Output from OPAL-RT
T_{44}	Digital	Gate pulse for T_{44}	o/p: 0 – 5V	Output from OPAL-RT

7.5 Implementation issues

There are a couple of implementation issues with the proposed converter at the start-up which should be highlighted. a) Start-up inrush current from the battery modules, b) start-up in-rush current from the power electronic switches.

This happens under three situations due to step changes in the voltage across capacitors when either batteries or switches are turn ON at: i) switching in the batteries causes the module capacitors voltage to go from zero to the battery terminal voltage, ii) if the power converter starts with a fixed reference which is mismatched across the capacitor and iii) dc-link capacitor is charged. This issue of in-rush current could be significant at higher power levels. Therefore, a suitable pre-charging arrangement and soft-starting mechanisms should be incorporated.

7.6 Overall prototype

The overall prototype is shown in Fig. 7.15. It consists of a) modular dc-dc converter, b) inverter, c) hybrid battery modules, d) protection, e) controller and f) central power supply. Fig. 7.16 and Fig. 7.17 show the hybrid batteries used in the experimental implementation and the detailed modular converter built in the laboratory.

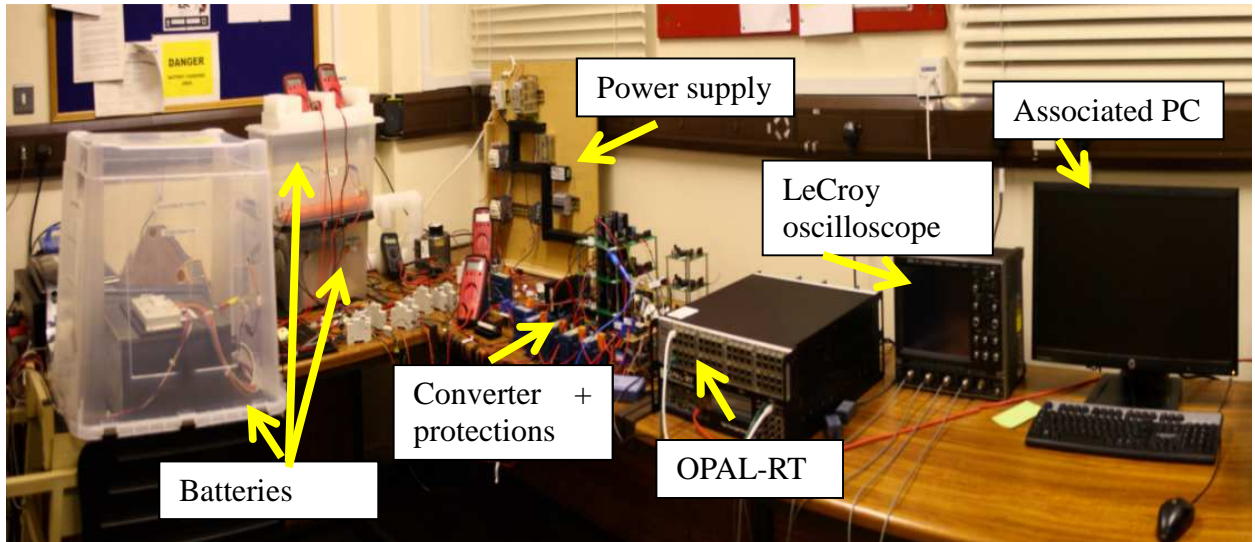


Fig. 7.15 Overall laboratory experimental set-up

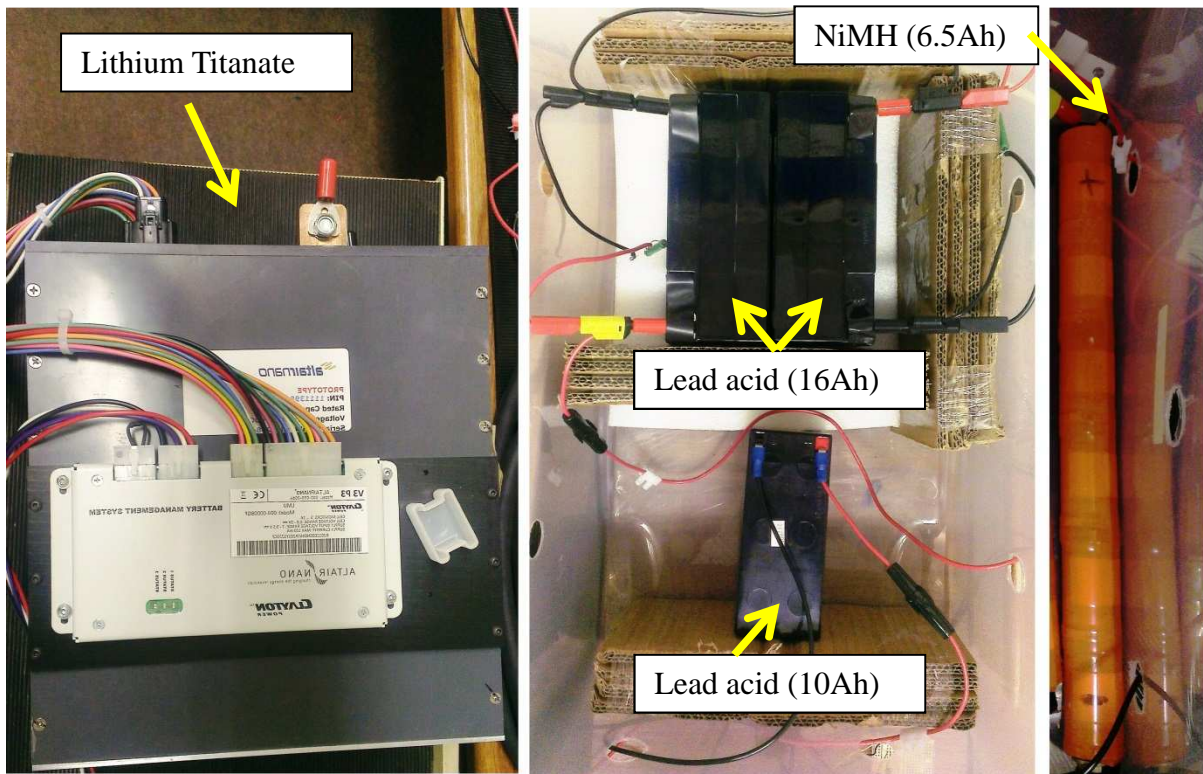


Fig. 7.16 hybrid batteries used in the experimental implementation

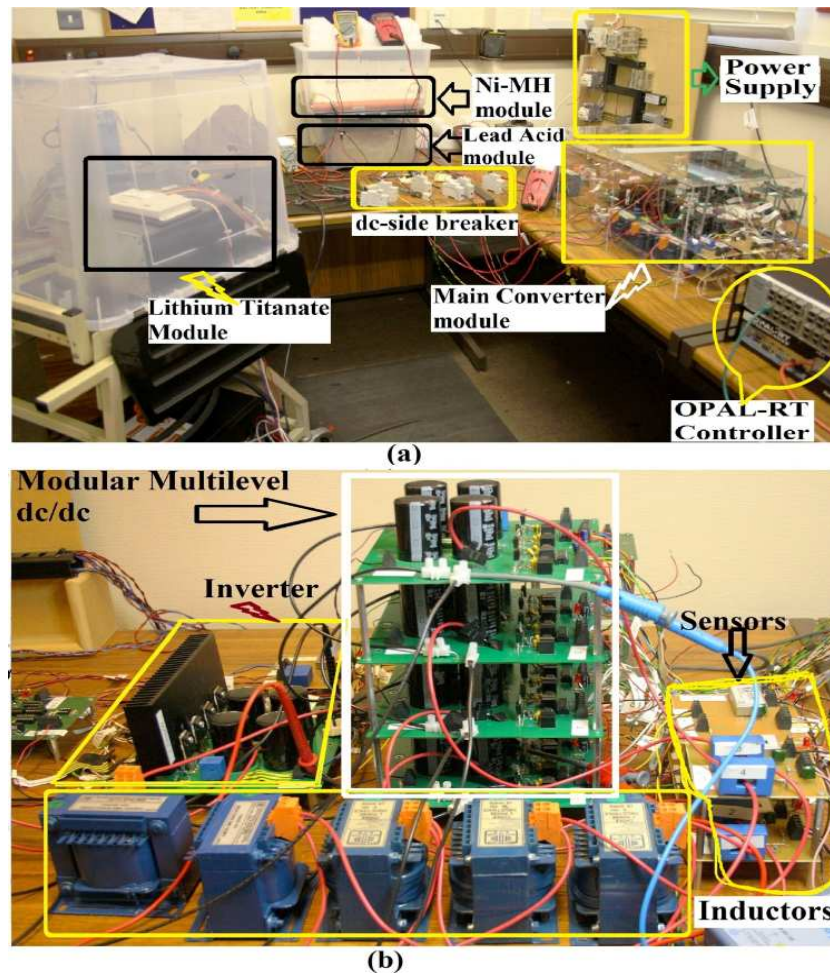


Fig. 7.17 Detailed overall set-up: a) overall set-up, b) power converter part

7.7 Conclusion

This chapter has described the hardware setup used in the experimental implementation for the scale down 1kW multi-modular laboratory prototype. The converter, associated components and their protection have all been detailed. The converter's interface with the digital controller has also been described in detailed. Since each dc-dc converter module is based on an H-bridge, each H-bridge has been designed on a PCB with integrated drivers and sensors for reducing the space and increasing compactness. The converter is mainly based on low voltage MOSFETs (such as OptiMOS) with IGBTs for the inverter which are available in TO-220 or TO-247 package which is helpful to reduce the converter size and enhance the efficiency. Due to the high efficiency of these devices, it avoided the need to use heat-sinks on the modular dc-dc converter. However, a common heat-sink was used for the inverter which uses IGBTs. A separate protection card was built for to each converter board. The inductors were separated out of each PCB because the inductor is bulky. The entire closed loop control system was run using an Opal-RT controller both under normal, transient and fault conditions. However, it should be noted that this hardware design is at low power levels and does not need to deal with the packaging issues and EMI issues which may arise when implementing at a higher power levels. A similar converter structure and design can be used in other energy storage systems like fuel cells and PV applications where a similar dc-side modular converter may be preferred.

8 Conclusions and Future Work

8.1 Introduction

The high cost of conventional new batteries for grid support has led to investigations of using second life transportation batteries (used EV/HEV batteries) to provide an energy storage capability. There is a significant interest in industry (e.g. ABB and GM) and research in using second life batteries in an energy storage system. This thesis proposed an integration strategy for the second life hybrid batteries in grid support applications such as, providing line side primary/secondary frequency response, voltage control or constant active/reactive power support. The thesis focuses on the power electronics design challenges in integrating such an energy storage system to the grid system both in terms of converter topology and control strategy. The proposed energy storage system consists of three hardware stages: a) the hybrid batteries, b) the dc-side modular converter, c) the line side inverter in conjunction with the control platform needed for the battery and grid side management systems. This chapter summarizes the key conclusions of the research and the future research needed in this area.

8.2 SLBESS system summary

The research into second life battery systems highlighted that batteries in second-use applications may have different chemistries, capacities, voltages, state of health, charging/discharging limits and physical size. Therefore, integration of different batteries from different sources in order to obtain a single hybrid second life solution is a key research challenge. This thesis addresses this challenges can be summarised as:

- Reliability of these second-use batteries are expected be lower than new batteries, therefore the power converter topology and associated control strategy needs to be designed so that a faulty battery module can be replaced with a healthy one without interrupting the overall operation of the energy storage system.
- A distributed control strategy needs to be implemented for this type of energy storage system because published existing control strategies deal with homogeneous batteries and this is not applicable in the present context.
- Parameters of the second life batteries such as, capacity and impedance could vary in a wide range during the operation. Therefore, the control strategy and control structure needs to adapt to deal with this.

8.3 Summary on converter topology

The research on converter topology has shown that a converter topology design is an

important because of the unknown reliability and heterogeneous nature of the second-use batteries. The major challenges in designing a converter topology are: a) ability to deal with the poor battery reliability, (e.g. able to hot-swap a battery module once it fails during the operation), b) ability to distribute the power from the hybrid batteries according to their characteristics, c) good efficiency and d) low cost. This thesis studied different multi-modular converter topologies and performs a reliability-cost optimisation with a numerical approach to find out a suitable topology for use in this application. The key conclusions of the research are:

- The cascaded H-bridge dc-side modular topology with an inverter is an appropriate converter topology to integrate these batteries from reliability, cost and efficiency perspective.
- The cascaded H-bridge dc-dc allows the topology to be fault-tolerant in nature with respect to a battery module offering potential to hot-swap a faulty battery module. The proposed converter structure provides a great flexibility and a wide operating region because of its ability to work in boost mode, buck mode as well as in boost-buck mode.
- Minimising the no. of cells in a module is a good way of getting better reliability.

8.4 Summary on control strategy

This thesis proposed a novel concept based on distributed power sharing strategy and distributed control architecture. The research into the control strategy of hybrid batteries can be described in three stages: a) battery power sharing scheme which can optimally distribute the required grid side power among the different battery modules, b) control of each converter module independently while providing the uninterrupted grid support through an inverter and c) stability issues.

8.4.1 Power sharing strategy

The key conclusions about the power strategy are summarised below:

- A weighting factor based strategy of power distribution was derived from first principle to deal with hybrid batteries. This result is important because it is capable of distributing the power between the batteries depending on their instantaneous characteristics to optimally use a set of hybrid batteries.
- The proposed weighting factor is based on the instantaneous impedance and estimated state-of-charge, and estimated battery capacity. It has been designed such that their charging/discharging trajectory of each battery module meets at the same point.
- The weighting factor based strategy reacts to changes in capacity, voltage, SOC and impedance to red-distribute the power share online by adjusting the weighting factor.

- The proposed strategy has been simulated and experimentally validated including the validation of battery parameter variation.

8.4.2 Control structure

The control system relating to the different operational modes has been developed. The boost and boost-buck mode control were validated in simulation and in hardware. The key conclusions about the control architecture are:

- A distributed voltage based control structure has been derived in the boost mode which maintains the central dc-link voltage of the inverter constant and is able to charge or discharge the hybrid modules according to their weighting factor when the line side inverter responds to the grid side power demand. The module capacitor dc-link voltages were controlled in such a way that it able to deliver the current according to the weighting function. However, the research showed that this control architecture is valid only in boost mode of operation where the total battery side voltage is less than the desired central dc-link voltage of the inverter.
- In boost-buck mode the control is based on distributed duty ratio of the multilevel buck converter. The research uniformly controlled the input side boost converters to make the module dc-link voltages the same and thereafter, altered the duty ratios of the buck converter switches as a function of battery weighting factor to utilise the hybrid battery modules. This novel mode of operation has been called a boost-multilevel buck. The main advantage of this mode is it provides a wide operating envelope to deal with any range of batteries. However, it has a higher power losses and lower efficiency compared to the boost mode of operation.

8.4.3 Summary Control stability

A key aspect of every control system is the ability to maintain stability especially in a high reliability application such as, grid side control. Maintaining the overall converter stability using such a distributed control structure has meant new control techniques have had to be developed with this topology and power sharing strategy. Two control techniques have been investigated: a) an adaptive PI-controller based approach and b) Lyapunov based nonlinear approach. The key points are summarised below:

- Depending on the weighting factor which varies according to the battery operating conditions, this can cause control loop instability in a module in boost mode operation. It is because the bandwidth of the outer voltage control loop varies over a wide range while the inner control loop remains unaffected.
- An adaptive PI-control approach has been investigated as a means of tuning the outer voltage loop dynamically to keep the control system stable. However, this approach has

some limitations such as, dependency on the battery parameters which can give errors and stability problems if there are inaccuracies in the measurement or estimation process along with reduced the dynamic response.

- Therefore, in order to overcome this issue, an alternate approach based on a Lyapunov function has been developed which not only overcomes this issue but also provides a fast dynamic response irrespective of battery operating conditions. Moreover, an important point is this approach can eliminate adaptive tuning which simplifies the design.
- Both the proposed approaches have been validated both in simulation and in experiments. It was found that Lyapunov approach more suitable than other approaches in this application.
- There is no such stability problem in boost-buck mode of operation. It is because a fixed voltage reference based control is used in the boost converter, therefore, no control loop performance is affected by the battery weighing factor or operating conditions. Therefore, it has better dynamic performance than an equivalent boost mode of operation.

8.5 Scope for additional and future Work

This thesis has stated the research into hybrid second life battery energy storage systems. However, because of the newness of the topic area there remains a significant number of unanswered research question which would benefit from further work and there is significant scope to take this work and apply it into other fields of study.

The ability to operate hybrid systems together could be of value to

- Any hybrid energy storage system based around isolated dc-sources.
- Fuel cell systems for example SOFC where the power distribution from each module could be tailored to the temperature of each module to maximise efficiency.
- PV systems and in particular organic solar modules which are significantly cheaper in price than silicon PV panels but less efficient and therefore require a greater surface area of active material to match the power. In order to compensate for this greater surface the panels could be set on different surfaces e.g. roofs, windows, wall and be of different size with different solar irradiation. This would benefit from the distributed power sharing approach and the weighting function can be used to trade-off life against power output to help their lifespan.
- Hybrid system with dc generation and energy storage.
- Other dc-generation including for example dc-generators driven by prime movers where fault tolerance and magnetic balancing could be important such as in aero-engines

In addition to advances in application additional research into the SLBESS would benefit from

- A better understanding of 2nd life battery reliability and failure including understanding of 1st life driver cycle and owner behaviour influence on 2nd life.
- A greater understanding is needed of how the batteries could be stripped down into sun-module and the variability of module cells in terms of characteristics.
- Research into pre-characterisations carried out prior to put the batteries into the converter because the second life batteries have unknown reliability and parameters. This work performs an initial characterisation to find out the initial parameters such as, initial internal impedance, capacity and relationship between the SOC and OCV.
- An analysis of how different 2nd life battery failure rate rates could affect system reliability and what impact this could have on converter design.
- An understanding of how the behaviour of the battery in its second life could impact its failure rate
- The distributed power sharing strategy is one based on charging/discharging trajectory the cells to end their trajectory at the different times. However, there are improvement that can be made to the accuracy of this method including
 - The proposed power sharing strategy assumes that a derived straight line relationship between the SOC and OCV from a look-up table in order to simply the control design. This is found to be a reasonable assumption. However, a more accurate non-linear relationship can be used based on pre-characterisation if OCV-SOC relationship could increase the accuracy of the power distribution.
 - Research into on-line capacity estimation, impedance estimation and SOC estimation.
 - Including the temperature explicitly into the power distribution equation rather than implicitly (assuming impedance and capacity change with temperature).
 - Investigating whether humidity has an effect on characteristics through better testing.
 - This thesis uses a passive balancing technique for the simplicity. An optimum balancing circuit using a combination of active/passive balancing depending on the individual battery types should be investigated.
- Alternative methods to distribute the power should also be investigated. These could include
 - Charging/discharging each battery in turn at a higher rate
 - Charging in blocks of batteries with rest periods to allow the battery to stabilise

-
- Charging/discharging the batteries based on optimised strategies e.g. reducing recycling cost based on battery chemistry.
 - Charging/discharging based on the location of the battery to assist with hot-swapping (e.g. having a sacrificing battery similar to switchgear component that is easy to replace)
 - Research into alternative power electronic topologies using multilevel boost converters from chapter – 1 to try for better reliability with additional complexity.
 - Power electronic scale-up packaging and thermal management research to understand scale-up issues and investigate other reliability/cost/size combinations
 - Economic research into full cycle costing of a full scale system and how the second life battery market could impact back on EV/HEV sales.
 - Fast acting frequency response research to understand how fast acting energy storage can displace slower conventional generation and the impact grid economics.
 - Alternative control strategies using alternative Lyapunov functions if possible
 - This research would also benefit from scaling up to understand if there are any issues relating to
 - Common mode noise
 - Earth leakage
 - EMI or EMC issues
 - Thermal management
 - Plant efficiency taking into account auxiliary supplies
 - Self-discharge is an important phenomenon in second life batteries especially some battery types e.g. NiMH when the battery in idle condition. This research does not take into account the self-discharge phenomenon. Future research work should take this into account.
 - This research assumes there is no BMS associated with the battery modules. Therefore, central control system estimates the essential battery parameters such as, SOC, capacity, impedance and distributes the power between hybrid battery modules. However, some of the commercial battery pack could come with their own BMS. In that case, the communication between the BMS and the centralised control system needs to be developed to monitor and use the data acquired from the external BMS.
 - The reliability and efficiency of the proposed topology is limited by the inverter which is assumed to be an H-bridge design in the present work. This two-level inverter is found to be suitable for the low voltage grid connection (e.g. 230V or 415V). However, it may not be a suitable inverter topology for the medium voltage (3.3kV/1kV) grid connection.

Therefore, a more efficient inverter e.g. interleaved inverter or multilevel inverter can be used to improve reliability and efficiency in grid support applications.

- There could be control stability and fault ride-through issues because of the interaction between multiple DERs in the grid system. This research does not take into account those issues. Therefore, the inverter control system needs to be modified accordingly if those issues need to be catered for.

9 Appendix – 1: Circuit Schematics

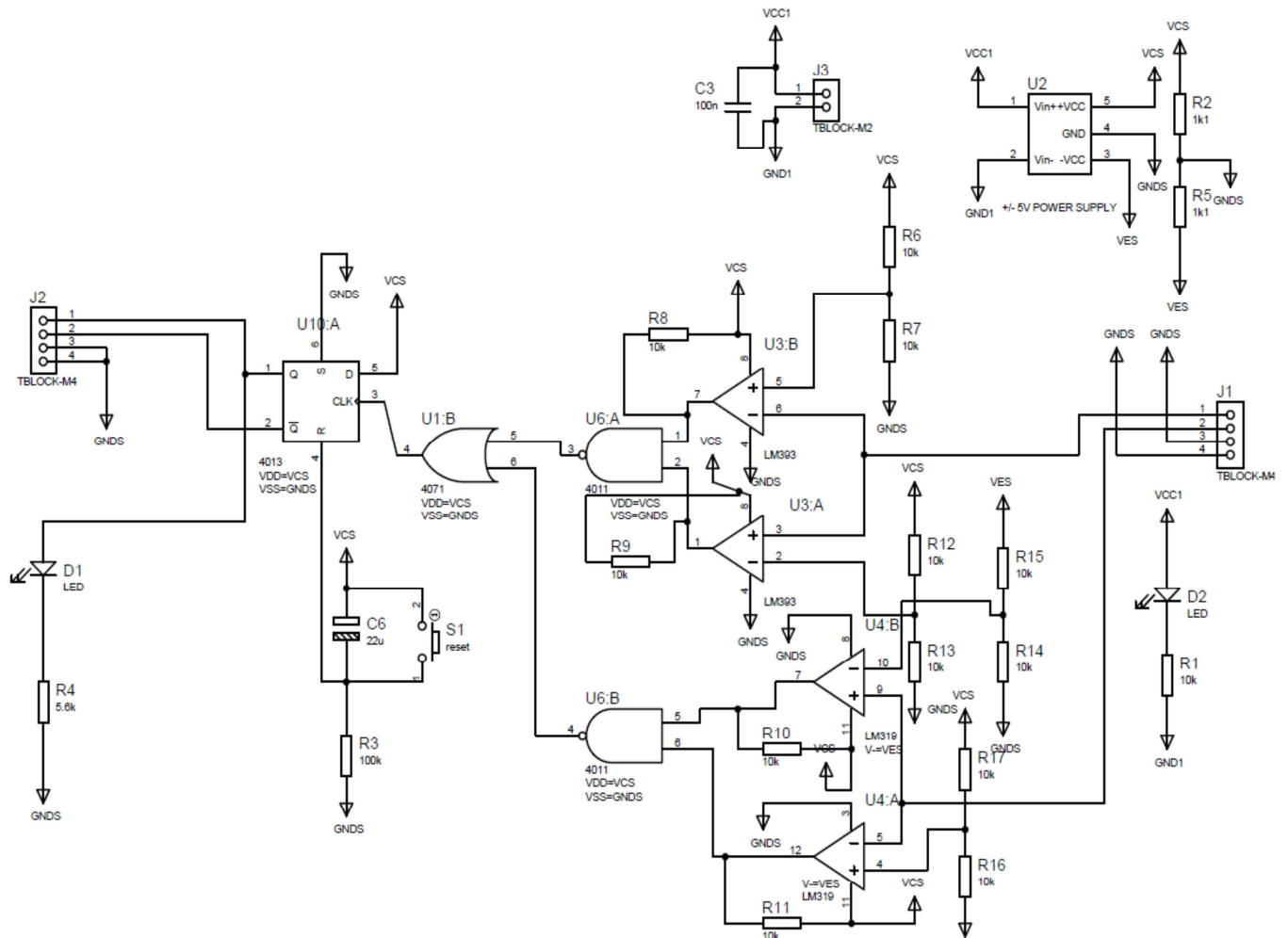


Fig. 9.1 Protection card schematics of an H-bridge module

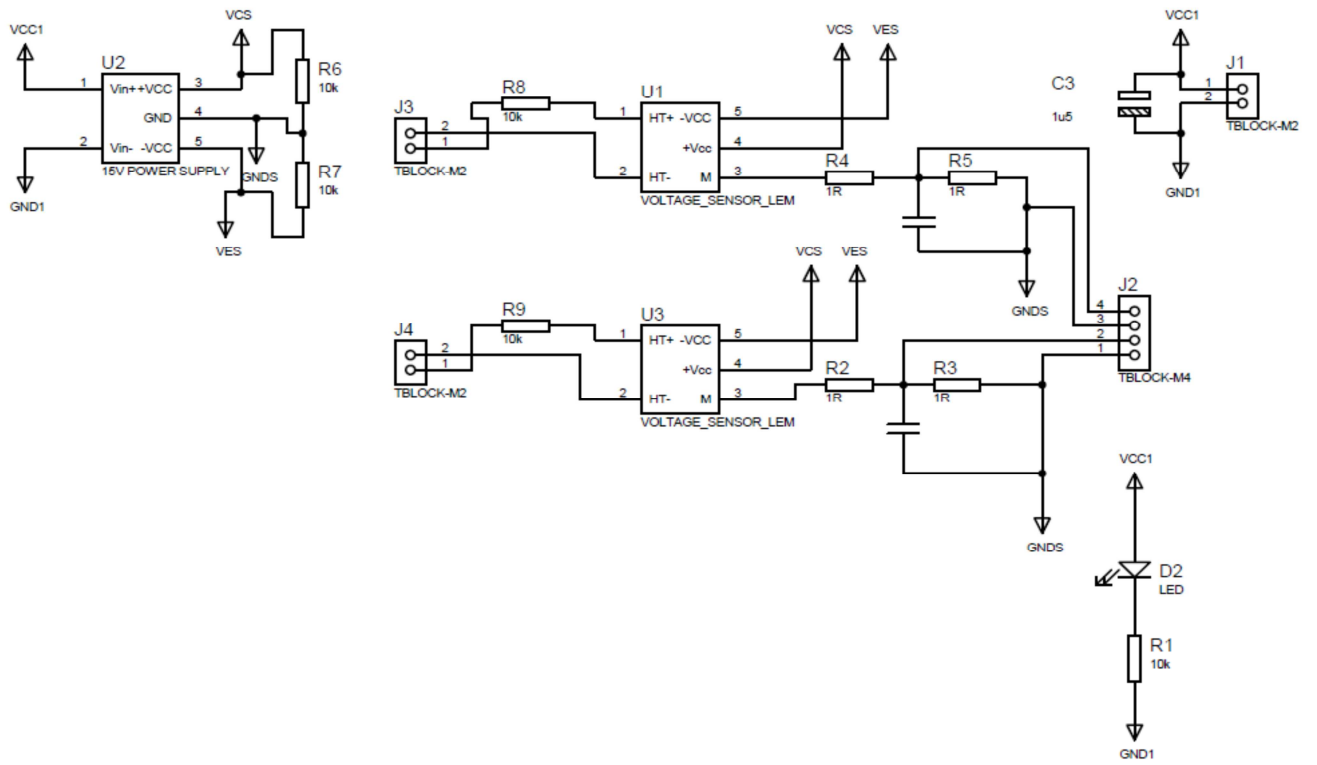


Fig. 9.3 Voltage sensor schematics

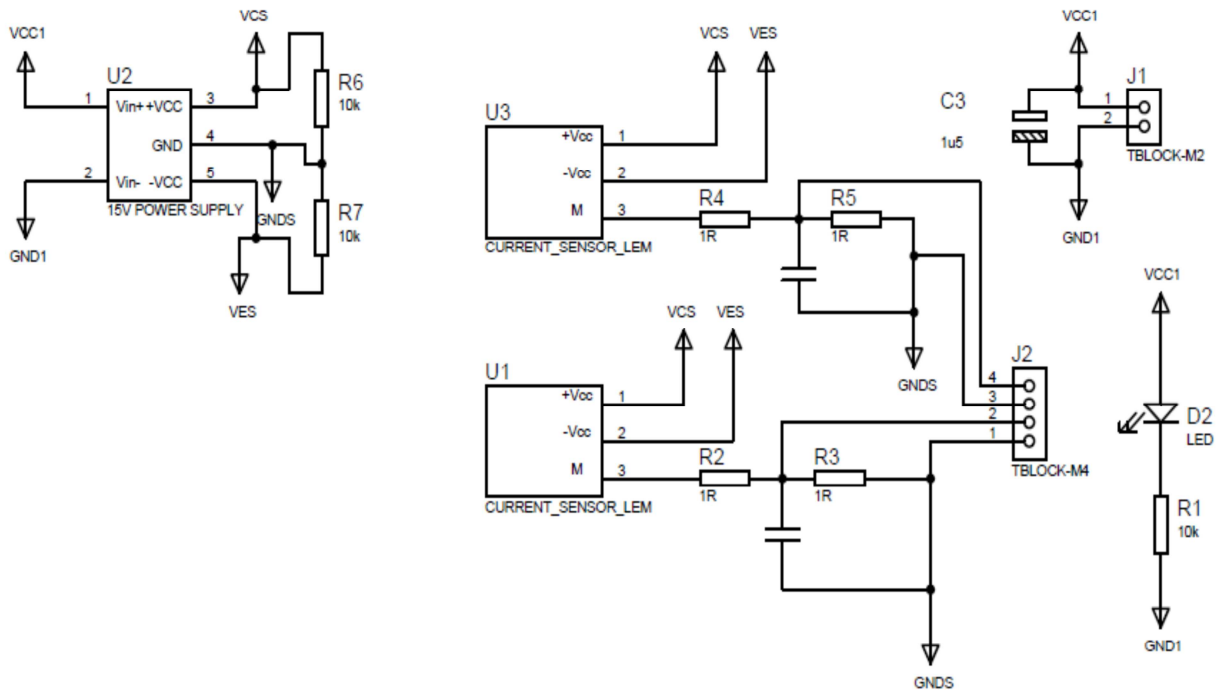


Fig. 9.4 Current sensor schematics

10 Appendix – 2: Sample Programs and Codes

10.1 Sample numerical program for the topology optimisation

```

clc;
clear all;
close all;
fbatt = 0.2e-6;
fdcdcl= 4.94e-6;
fdcdc= 9.1e-6;
fdcac = 8.1e-6;
Pcell = 3.3*20;
Vcell =3.3;
Ibatt = 20;
b=5;
C = 100e-6;
L = 0.16e-3;
Rdcac = exp (-fdcac*365*24*5);
% cost = zeros(60,30);
counter1=1;

for x=1:4
    Rm = exp (-1*(fbatt*x+fdcdc+fdcdcl)*(365*24*5));
    for n=22:70

        for k=21:n
            y(k)=0;

            V = b*k*x*Vcell;
            P = k*x*Pcell;
            if ((P > 1000) && (V >340))

                for ii=k:n
                    ytemp= nchoosek(n,ii)*(Rm^ii)*((1-Rm)^(n-ii));
                    y(k)=y(k)+ytemp;
                    RT = y(k);
                end
                if ((RT*Rdcac)>0.7)
                    cost(:,counter1)= [x n/k
(2*n*b*((x*Pcell/1000)^2*0.0126+(x*Pcell/1000)*0.2987+0.0915)+2*n*((x*Pcell
/1000)^2*0.0126+(x*Pcell/1000)*0.2987+0.0915)+
4*k*((x*Pcell/1000)^2*0.0126+(x*Pcell/1000)*0.2987+0.0915)+(4*n+4)*((b*x*Pc
ell/1000)*0.0029)+3*n*4+n*((-
0.5*C*(b*x*Vcell)^2)^2*0.0062+(0.5*C*(b*x*Vcell)^2)*0.9366+0.62)+n*(2.412*(
0.5*L*Ibatt^2)^2+28.0*(0.5*L*Ibatt^2)+2.7)];
                    counter1=counter1+1;
                end
            end
        end
    end
end
end
end

```

```

xlswrite
('C:\Users\mukhern2\Desktop\Matlab_reliability_cost_program\Data_reliabilit
y_2.xlsx',cost')

scatter3(cost(1,:),cost(2,:),cost(3,:))
xlabel('x')
ylabel('n/k')
zlabel('Cost Indicator')
grid on;
    
```

10.2 Sample OPAL-RT code

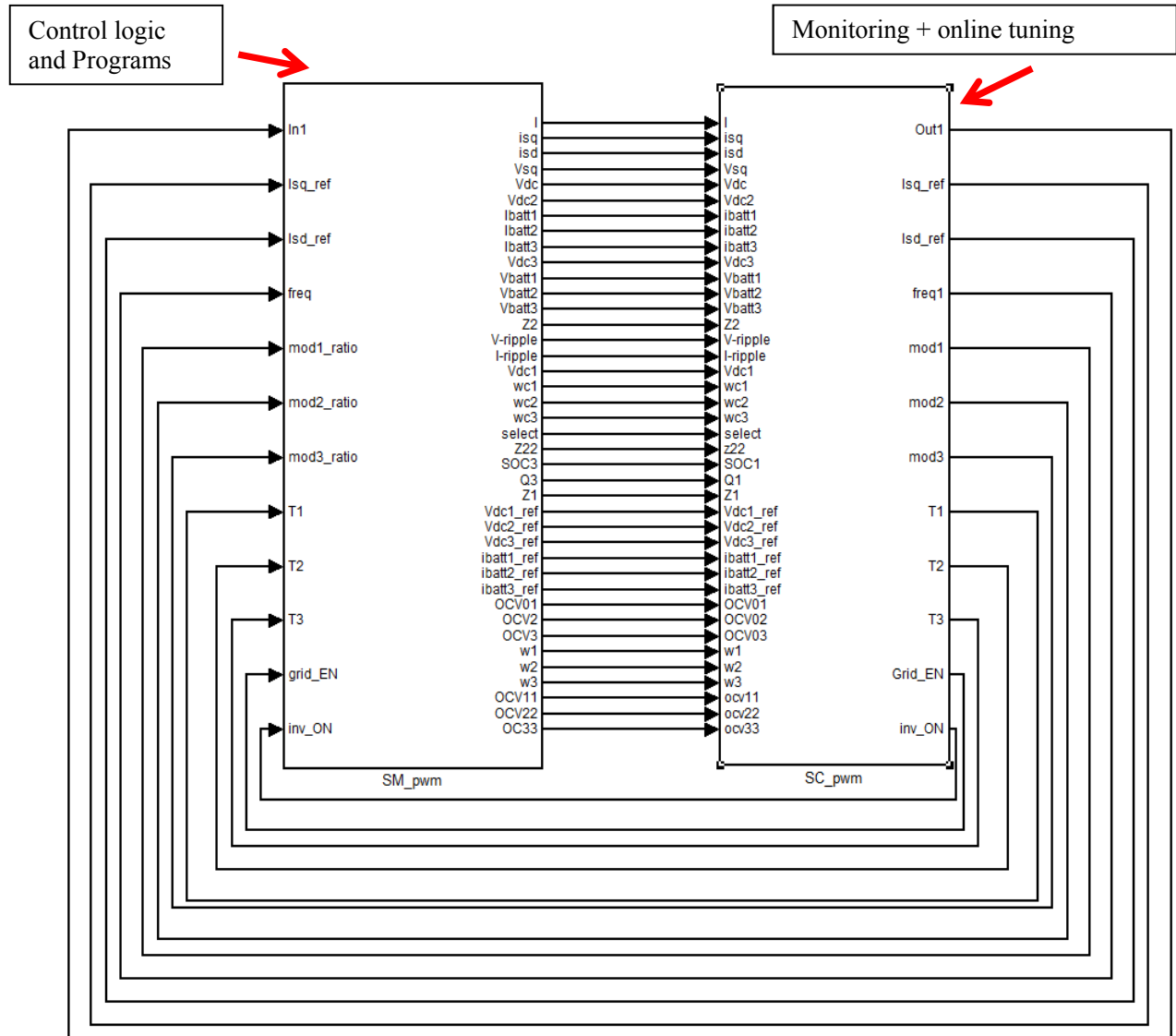


Fig. 10.1 Sample OPAL-RT program overview

11 Appendix – 3: List of Publications

1. Mukherjee, N.; Strickland, D., "Control of Second Life Hybrid Battery Energy Storage systems Based on Modular Boost-Multilevel Buck Converter," *IEEE Transactions on Industrial Electronics*, 2014 (in Press)
2. Mukherjee, N.; Strickland, D., "Adaptive Control of Hybrid Battery Energy Storage systems under Capacity Fade," *Power Electronics and Applications (EPE), 2014 16th European Conference on*, Aug. 2014
3. Mukherjee, N.; Strickland, D.; "Second life Battery Energy Storage System: Converter Topology and Redundancy Selection," *Power Electronics, Machines and Drives (PEMD 2014), 7th IET International Conference on* , vol., no., April 2014.
4. Mukherjee, N.; Strickland, D., "Modular ESS with second life batteries operating in grid independent mode," *Power Electronics for Distributed Generation Systems (PEDG), 2012 3rd IEEE International Symposium on*, vol., no., pp.653,660, 25-28 June 2012 .
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