

All-optical binary counter

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Abstract: We experimentally demonstrate an all-optical binary counter composed of four semiconductor optical amplifier based all-optical switching gates. The time-of-flight optical circuit operates with bit-differential delays between the exclusive-OR gate used for modulo-2 binary addition and the AND gate used for binary carry detection. A movie of the counter operating in real time is presented.

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OCIS codes: (200.4660) Optical logic; (200.4560) Optical data processing

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1. Introduction

The deployment of all-optical digital processing in future high-speed optical network architectures is dependent upon being able to add functionality directly at the optical layer [1]. In photonic networks based on binary modulated packets of optical pulses, all-optical processing directly at the bit-level can be used to regenerate the packets [2] and perform functions such as parity checking [3]. In this paper we describe a novel all-optical binary counter that demonstrates the ability of all-optical digital processing to perform even more complex operations. Within optical packet networks, a binary counter can be used at the packet level to verify network performance within a node. Ultimately, an optical pulse counter operating at the bit-level could enable functions such as header extraction and payload processing to be realised. In this proof-of-principle experiment we use two coupled optical regenerative memories [4] to form the optical counter. This architecture is the same as used for the full binary adder that we have demonstrated previously [5]. One memory contains an all-optical exclusive-OR (XOR) gate and is used to perform the modulo-2 addition (COUNT) of the incoming bit to the existing count. The other memory contains an AND gate and is used to generate the CARRY bits that arise when two ONES are added together in the COUNT. With this regenerative optical memory architecture we use two different wavelengths to distinguish clock and data pulses and so each memory uses two semiconductor optical amplifier (SOA) based all-optical switching gates, one for AND/XOR and one for wavelength conversion. We employ the TeraHertz Optical Asymmetric Demultiplexer (TOAD [6]) switching gate which is a type of all-optical nonlinear loop mirror comprising a 50:50 fused fibre coupler, a second fibre coupler to introduce the switching data pulses, polarisation controllers to bias the loop and a SOA as the nonlinear element. The SOA is placed asymmetrically in the loop to create a temporal switching window that allows an input switching pulse to change the gain of the SOA and hence impart a differential phase shift between the clock pulse components in the fibre loop. A relative phase shift of π radians is required for the clock components to interfere such that the clock pulse is transmitted out of the loop rather than being reflected. In principle, a single SOA based gate can be used for each memory if propagation direction [7] or polarisation [8] is used to distinguish clock and data pulses. In common with the all-optical parity checker and the full adder [3,5], we arrange the capacities of the two optical memories to differ by one bit so that there is a bit-differential delay for the CARRY bits being fed back to the COUNT memory. This arrangement correctly moves the CARRY bits to the next significant place in the count (and in time) and allows a carry ripple operation to progressively evolve with each circulation around the memories. A serial logic diagram of the counter circuit is shown in figure 1.

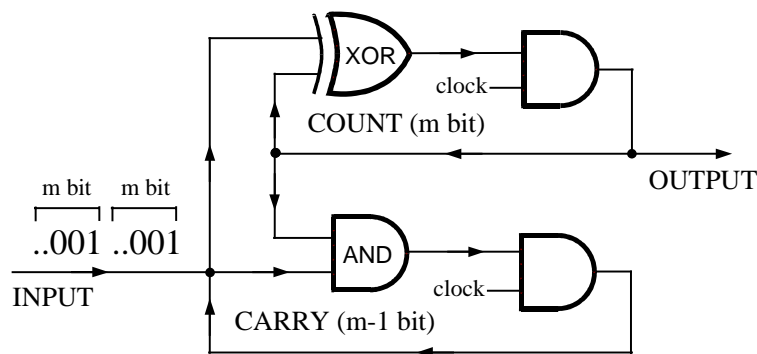


Fig. 1. Logic diagram of the binary counter with bit-differential delay. The COUNT memory has a capacity of m bits and the CARRY memory has a capacity of $m-1$ bits. The delay for the link between the COUNT memory and the AND gate input is m bits. The delay for the link between the CARRY memory and the XOR gate input is $m-1$ bits. The optical pulses to be counted are input singly with a period of m bits.

The binary bits to be counted arrive serially at the input to the circuit and the time between bits is configured to be the same as the round trip time of the COUNT optical memory. On each circulation of the memories there is a simultaneous XOR and AND performed between the accumulated count and the incoming bit. This is achieved by configuring the link between the COUNT memory loop and the AND gate input to also have a delay corresponding to the round trip time of the COUNT optical memory. The AND result (the CARRY bits) is fed back to both the AND gate and the XOR gate with a single bit-differential delay and the process repeats as described above. The clocked AND gate in each memory is equivalent to an all-optical regenerative wavelength conversion element.

2. Experiment

A schematic diagram of the experimental system used for the optical counter is shown in figure 2. The optical pulse sources were jitter-suppressed gain switched distributed feedback (DFB) semiconductor lasers. These gave ~ 10 ps pulses at a repetition rate of 1GHz at wavelengths of $\lambda_1 = 1552$ nm (DFB#1) and $\lambda_2 = 1534$ nm (DFB#2). TOAD1 was configured with a relatively wide switching window (~ 150 ps), which is longer than the gain recovery time of the SOA ($1/e \sim 80$ ps), so that a single TOAD could operate as a good all-optical XOR gate [3,5,9]. When the SOA recovery time is shorter than the switching window, this allows two temporal switching conditions: one where the signal pulses in the loop experience a differential phase shift due to the recovering gain of the SOA and one where the signal pulses arrive in time before and after the switching pulse. This allows the XOR gate to give an output of ONE when a switching pulse arrives in either of these switching conditions. However if two switching pulses arrive, one in each switching condition, then a very small differential phase shift occurs between the signal pulses in the loop and hence there is no switching of the signal pulses. This gives the required result for XOR that two input ONES gives a ZERO at the output of the gate.

The other TOADs had switching windows of ~ 50 ps and were used as AND gates. At a switching rate of 1GHz, the time between each bit was 1ns. The capacity of the COUNT memory was 297 bits and so the length of optical fibre in the CARRY memory was adjusted to have a capacity of 296 bits i.e. a single bit less than the COUNT memory for bit-differential operation. The length of optical fibre between TOAD1 and TOAD3 was also adjusted to give a delay of 297 bits (~ 60 m) so that for each incoming bit to be counted there was a simultaneous XOR operation in TOAD1 and an AND operation in TOAD3 to generate the CARRY bits. Erbium doped fibre amplifiers (EDFAs) were used to amplify the optical pulses to the TOAD switching energy (~ 100 fJ per pulse) and adjustable optical delay lines

interleaved within the 297 bit capacity of the present experimental system since only 34 bits are required to count to a time of >1 hour ($2^{34} \times 297\text{ns} \sim 85$ minutes).

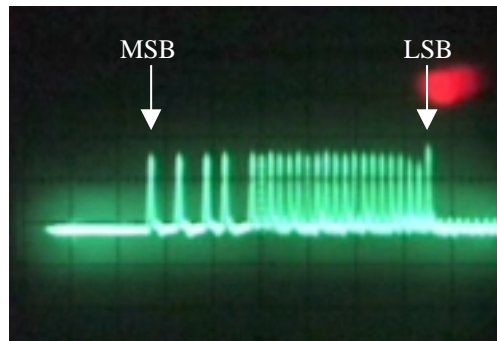


Fig. 3. Full optical count field with the LSB on the RHS and the MSB on the LHS. The time separation between pulses is 1ns corresponding to the switching rate of 1GHz and the count rate is $\sim 3.4\text{MHz}$. The movie (902kb version, 8.57Mb version) shows the real time evolution of the binary count.

In order to show in detail that the counter is counting correctly in binary, figure 4 shows a selective view of the count from 2^{21} to 2^{25} . In this real time movie clip it is possible to see the apparent evolution of the count from zero to 2^5 and the resetting to zero again as the MSB moves out of view of the oscilloscope screen.

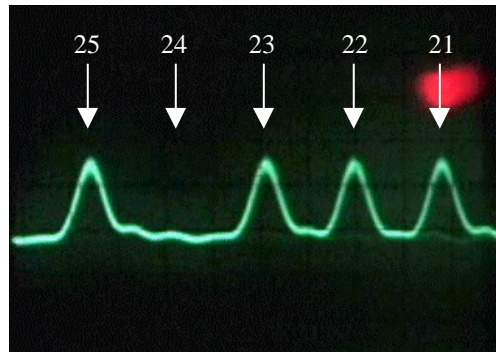


Fig. 4. Optical count field from 2^{21} (RHS) to 2^{25} (LHS). The movie (938kb version, 3.67Mb version) shows the real time evolution of the binary count.

Finally, in figure 5 we show the counting transition from 2^{28} to 2^{29} that shows the optical counter acting as a timer. We can use the knowledge of the count rate ($1/297\text{ns}$) to predict that

this binary evolution to the next significant place should occur in $2^{29} \times 297\text{ns} \sim 160\text{s}$ and this is indeed verified by the elapsed time in the real time movie shown in figure 5.

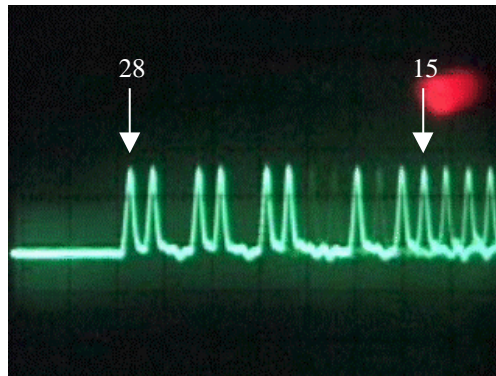


Fig. 5. Optical count field from 2^{12} (RHS) to 2^{28} (LHS). The movie (15Mb) shows the real time evolution of the count from $<2^{28}$ to $>2^{29}$ that takes $\sim 160\text{s}$.

4. Discussion

One of the advantages of time-of-flight designed systems is that they are simply scalable in operation speed to the fastest switching speed of the logic gates [10]. With SOA based gates, $\sim 100\text{Gbit/s}$ AND gate operation has been reported [11,12] with similar switching energies to those required here. However, at these switching rates it is likely that the XOR operation will require more than a single TOAD, but we have previously demonstrated how this is possible using two AND gates and an OR gate [13]. Reducing the capacities of the memories and hence increasing the count rate will require the time-of-flight latency to be reduced. This should be achievable using integrated SOA based all-optical switches [14-17] and using planar silica interconnects between the switching gates [18]. If the latency can be sufficiently reduced then it may be possible to create truly bit-serial optical delays so that the bit-differential technique described here would not be required. Optoelectronic counters based on true bit-serial design have been demonstrated previously [19].

5. Conclusions

In conclusion, we have successfully demonstrated an all-optical binary counter with bit-differential delay. In common with other time-of-flight designed, SOA based optical processing systems, this all-optical architecture should be scaleable in operating speed to the fastest switching speed of the all-optical gates.

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