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Scaling/LER Study of Si GAA Nanowire FET using 3D Finite Element Monte Carlo Simulations

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***Abstract*—3D Finite Element (FE) Monte Carlo (MC) simulation toolbox incorporating 2D Schrödinger equation quantum corrections is employed to simulate I_D-V_G characteristics of a 22 nm gate length gate-all-around (GAA) Si nanowire (NW) FET demonstrating an excellent agreement against experimental data at both low and high drain biases. We then scale the Si GAA NW according to the ITRS specifications to a gate length of 10 nm predicting that the NW FET will deliver the required on-current of above 1mA/μm and a superior electrostatic integrity with a nearly ideal sub-threshold slope of 68 mV/dec and a DIBL of 39 mV/V. In addition, we use a calibrated 3D FE quantum corrected drift-diffusion (DD) toolbox to investigate the effects of NW line-edge roughness (LER) induced variability on the sub-threshold characteristics (threshold voltage (V_T), OFF-current (I_{OFF}), sub-threshold slope (SS) and drain-induced-barrier-lowering (DIBL)) for the 22 nm and 10 nm gate length GAA NW FETs at low and high drain biases. We simulate variability with two LER correlation lengths (CL=20 nm and 10 nm) and three root mean square values (RMS=0.6, 0.7 and 0.85 nm).**

Keywords*—Schrödinger quantum corrections, Monte Carlo simulations, GAA nanowire FET, LER, variability.

I. Introduction

Gate-All-Around (GAA) nanowire (NW) FETs are considered to be excellent candidates for future CMOS integration for sub-10 nm digital technology to continue transistor down-scaling [1]. The GAA NW FETs have superior electrostatics and immunity to short channel effects while still delivering a large on-current [2]–[4]. However, to have a full realistic assessment of these potential candidates, we must take into account the exact device geometry and also determine how different sources of device variability can affect device characteristics and reliability. Variability of transistor characteristics is induced by material properties and by fabrication processes and can affect their performance in circuits. One of such sources is line-edge roughness (LER) which has a major impact on variability in NW/FinFETs [3], [5]–[7].

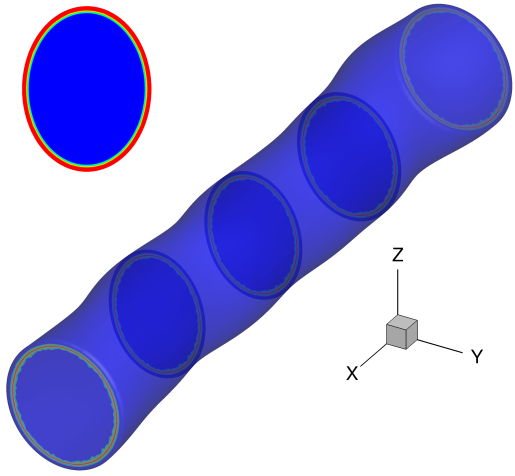

Fig. 1. Schematic of the 22 nm gate length n-channel Si GAA nanowire, showing LER and examples of 2D slices used for Schrödinger solver.

In this work, we report on performance, scaling and variability of nanoscale GAA Si NW FETs. We use an in-house 3D Finite Element (FE) Monte Carlo (MC) simulation toolbox which includes newly integrated calibration-free 2D FE anisotropic Schrödinger equation based quantum corrections (SEQC) [8] along the device channel. More details on the 3D FE MC toolbox are in Refs. [8]–[11]. Here, we start by comparing

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results from our 3D FE SEQC MC toolbox against experimental data of a 22 nm gate length GAA Si NW FET [2] with a ⟨110⟩ channel orientation. We then simulate the ⟨100⟩ channel orientation for the same NW for comparison. Next, we scale the NW to a gate length of 10 nm according to the International Technology Roadmap for Semiconductors (ITRS) specifications [12] and simulate the ⟨100⟩ and ⟨110⟩ channel orientations with the 3D FE SEQC MC. Finally, we use our 3D quantum corrected FE drift-diffusion (DD) simulation toolbox to study the LER-induced variability on the sub-threshold characteristics (threshold voltage (V_T), OFF-current (I_{OFF}), sub-threshold slope (SS) and drain-induced-barrier-lowering (DIBL)) at both low and high drain biases for the 22 nm and the 10 nm gate length GAA NW FETs. We simulate the variability with LER correlation lengths (CL) of 20 nm and 10 nm and three root mean square values (RMS) of 0.6, 0.7 and 0.85 nm chosen to represent the RMS observed in experiments [2], [3].

II. 3D Monte Carlo Simulations

The 3D FE method incorporated into 3D SEQC MC toolbox is capable of accurately describig the complex 3D geometry of the nanoscale devices. The accurate description of the simulation domain in nanoscale semiconductor devices is essential in determining quantum transport at highly non-equilibrium conditions. In our case, we chose a semi-classical transport technique, a 3D ensemble MC [8]–[11], with calibration-free quantum confinement corrections, the SEQC. Our in-house 3D FE MC simulation toolbox employs fully anisotropic 2D FE Schrödinger equation based quantum corrections (QC) [8] which depends on valley orientation and considers longitudinal and transverse electron effective masses. The MC transport engine considers an analytical anisotropic non-parabolic band-structure model with the same longitudinal and transverse masses and the following scattering processes: the acoustic phonon scattering, non-polar optical phonon scattering (g, f-processes) [13], ionized impurity scattering using the third-body exclusion model by Ridley [14] with a static screening model self-consistently calculating Fermi energy and electron temperature [15], and the interface roughness scattering using Ando's model [16]. This combination has been shown to be a very good compromise between the precision and the speed for accurate physical simulations of carrier transport in nanodevices which are strongly quantum confined systems at highly non-equilibrium transport conditions [9]–[11].

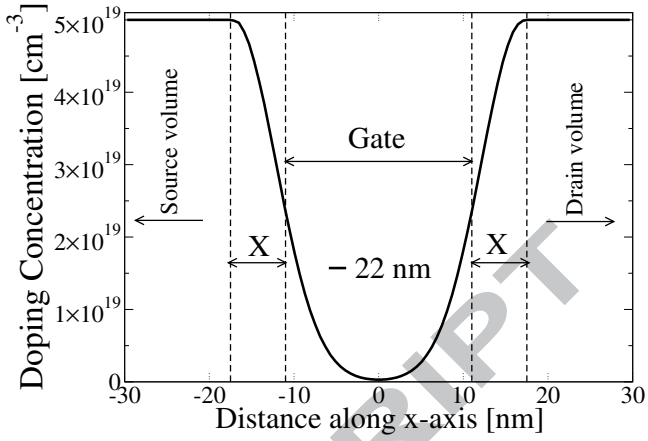

Fig. 2. Cross-section of Gaussian-like doping profile along the transport x-direction in the 22 nm gate length GAA NW FET.

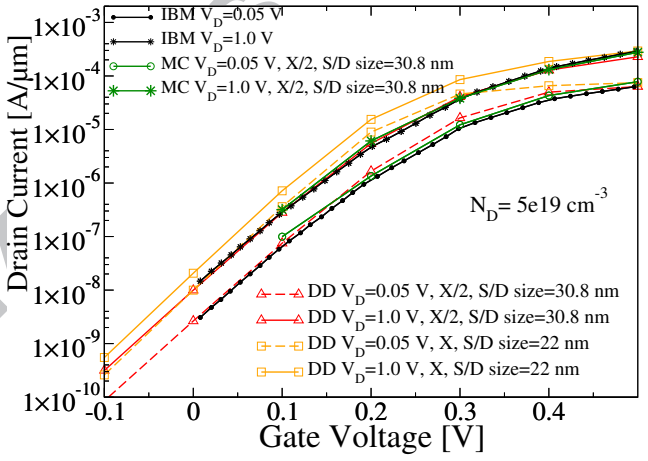

Fig. 3. Devising doping profile for the 22 nm GAA NW FET at V_D=0.05 V and V_D=1.0 V via DD simulations by changing the size of the S/D region and the doping spread X (open red triangles and orange squares). Final MC simulations (green open circles and stars) are compared to experimental data (black full circles and stars).

We start by comparing results from our 3D SEQC MC toolbox against experimental data of a 22 nm gate length GAA Si NW [2] with a ⟨110⟩ channel orientation. The NW has elliptical cross-section (Fig. 1) with a shorter diameter of 11.3 nm and

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a longer diameter of 14.22 nm; with an effective diameter (elliptical circumference/π) D_{NW}=12.8 nm and EOT= 1.5 nm which can be accurately described by the FE method.

The 3D FE quantum corrected (QC) drift-diffusion (DD) simulations using density gradient (DG) [17] were used to reverse engineer a doping profile in the sub-threshold region at V_D =0.05 V and V_D=1.0 V by changing the Gaussian-like doping profile (a doping maximum and a spread X which determine the abruptness of the doping profile) as shown in Fig. 2. The effective masses in the DG approach were used as calibration parameters. Fig. 3 shows examples of this reverse engineering process for the sub-threshold region which achieved excellent agreement with a maximum doping of $5 \times 10^{19}\mathrm{cm}^{-3}$, a work function of 4.512 eV, and a S/D size of 30.8 nm. We then use the 3D FE SEQC MC toolbox to simulate the I_D-V_G characteristics of the 22 nm gate GAA Si NW at low and high drain biases achieving an excellent agreement with the experimental data [2] as can be seen in Fig. 4. The current is normalized by nanowire perimeter (elliptical circumference=40.21 nm). Note here that the resulted drain current from 3D SEQC MC simulations gives the agreement with experiment without any need for additional lumping of external resistance from the experiment. This is because the S/D resistance is accurately reproduced in physically based 3D ensemble MC technique thanks to the size of the S/D access regions included into simulation domain.

Fig. 5 compares the average electron velocity at $V_G = 0.8$ V and $V_D = 1.0$ V for the 22 nm gate length GAA NW along the $\langle 100 \rangle$ and the $\langle 110 \rangle$ channel orientations, along with the average velocity in the three silicon valleys $\Delta 1$, $\Delta 2$ and $\Delta 3$. We see that the electron velocity exhibits a typical behaviour along the channel. The total average velocity in the $\langle 100 \rangle$ orientation is higher than the one in the $\langle 110 \rangle$ orientation due to a higher electron mobility in the $\langle 100 \rangle$ crystallographic orientation in Si. The source injects electrons at relatively large injection velocity of about 3.0×10^4 m/s where they are quickly accelerated along the gate reaching their maximum velocity of

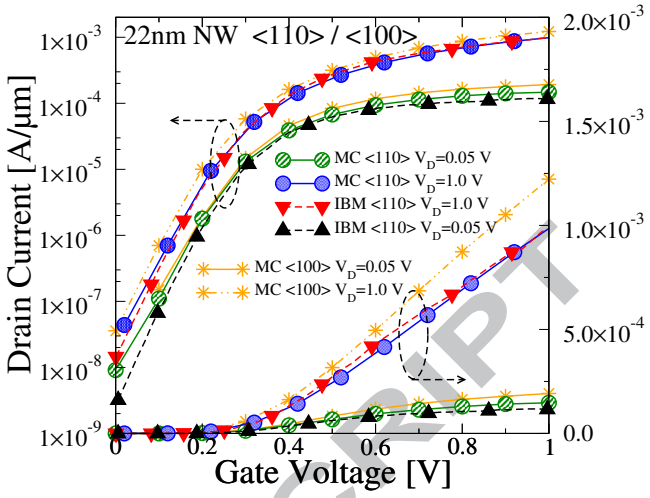

Fig. 4. I_D-V_G characteristics for the 22 nm GAA nanowire from the 3D FE MC with anisotropic Schrödinger quantum corrections, in the $\langle 110 \rangle$ (circles) and $\langle 100 \rangle$ (stars) channel orientations, compared against experimental data in the $\langle 110 \rangle$ (triangles) orientation [2].

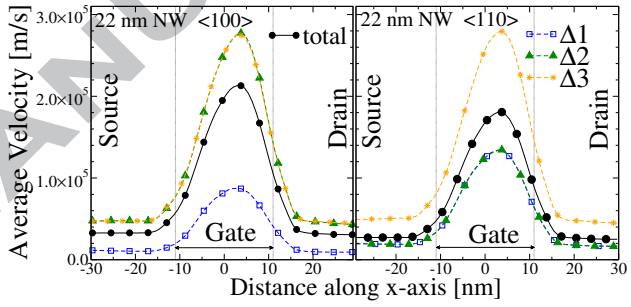

Fig. 5. Average electron velocity at V_D=1.0 V and V_G=0.8 V along the 22 nm gate length GAA NW (3D MC) along the $\langle 100 \rangle$ and $\langle 110 \rangle$ channel orientations. The zero is set in the middle of the channel.

$2.0/1.75 \times 10^5$ m/s, respectively, on the drain side of the gate. Then electrons decelerate into a heavily doped drain due to enhanced optical phonon emission assisted by ionised impurity scattering [18].

In the $\langle 100 \rangle$ orientation channel, the $\Delta 1$ velocity is the smallest because it has the heaviest mass in the transport direction. The $\Delta 2$ and $\Delta 3$ velocities are equal in the $\langle 100 \rangle$ channel device because they have the same effective transport masses. On the other hand, in the $\langle 110 \rangle$ channel, the $\Delta 3$ velocity is the largest because it has the lightest effective transport mass. The $\Delta 1$ and $\Delta 2$ velocities are equal because they have equal effective transport masses.

We then scale the Si GAA NW according to the ITRS specification [12] to a gate length of 10 nm and an EOT of 0.8 nm.

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Fig. 6 compares the eigenmodes ($|\psi(y,z)|^2$) corresponding to the lowest energy eigenvalue, in the $\langle 110 \rangle$ channel orientation, of the three Δ valleys in the middle of the channel for the 22/10 nm gate length GAA NW, respectively, at V_D =1.0/0.7 V and V_G=0.8 V (note that $\Delta 1$ and $\Delta 2$ have the same effective mass tensor in the $\langle 110 \rangle$ channel orientation, so they will have the same wavefunction). The asymmetry seen in the eigenmode of the $\Delta 3$ valley in the 22 nm gate NW FET (top–left) is the result of drain induced change into potential in the channel at a large applied drain bias of 1.0 V. This effect will not occur in the 10 nm gate device because this transistor, with a much stronger quantum confinement, has a much better control of the transport so that the drain induced change into potential is negligible.

Fig. 7 shows I_D-V_G characteristics (the current is normalized by nanowire perimeter (elliptical circumference=20.29 nm)) for the scaled 10 nm gate length NW FET at V_D =0.05 V and V_D =0.7 V along the $\langle 100 \rangle$ and the $\langle 110 \rangle$ channel orientations obtained from the 3D FE SEQC MC. Table I compares device operating characteristics with gate lengths of 22 nm and 10 nm predicting that the scaling to the 10 nm gate will ensure superior electrostatic integrity of a nearly ideal sub-threshold slope of 68 mV/dec and a DIBL of 39 mV/V and satisfactory on-current (the on-current increase is $\sim 8/10\%$ for the $\langle 100 \rangle$/$\langle 110 \rangle$ channel orientation with respect to the 22 nm NW).

The threshold voltage (V_T) is 0.3/0.35 V for the 22/10 nm gate length NW FET. The scaled GAA NW has a better sub-threshold slope (SS) at both low and high drain biases and a better drain-induced-barrier-lowering (DIBL) along the $\langle 100 \rangle$ and the $\langle 110 \rangle$ channel orientations. Due to the fact that electrons have a higher mobility in the $\langle 100 \rangle$ crystallographic orientation, both devices deliver a higher current for the $\langle 100 \rangle$ channel orientation than for the $\langle 110 \rangle$ channel at both low and high drain biases. For the 22 nm and the 10 nm GAA NW FETs, the drain current in the $\langle 100 \rangle$ channel device is larger than in that with the $\langle 110 \rangle$ channel by $\sim 30/20\%$ at a low/high drain bias.

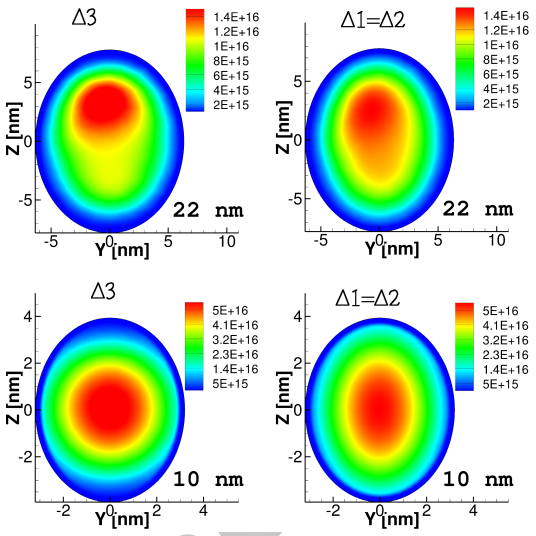

Fig. 6. Eigenmodes ($|\psi(y,z)|^2$) corresponding to the lowest energy eigenvalue of the three Δ valleys, in the middle of the $\langle 110 \rangle$ channel for the 22 nm (top, at V_D=1.0 V) and 10 nm (bottom, at V_D=0.7 V) Si GAA NW at V_G=0.8 V.

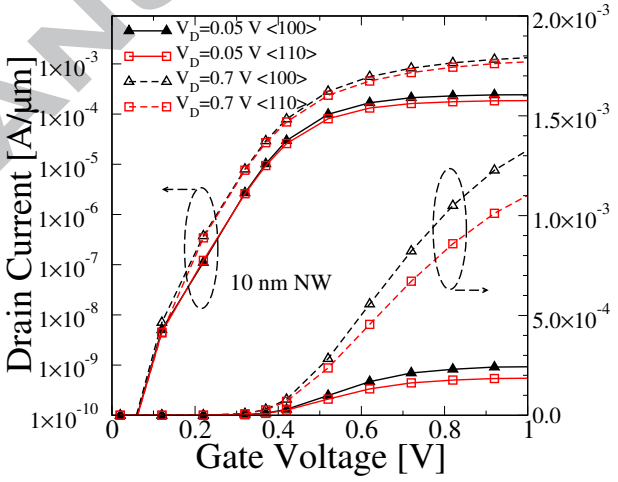

Fig. 7. I_D-V_G characteristics for the scaled 10 nm gate length GAA NW FET predicted by the 3D FE SEQC MC along the $\langle 100 \rangle$ and $\langle 110 \rangle$ channel orientations.

III. Line-Edge Roughness (LER)

Down scaling transistors to the nano regime increases the undesirable performance mismatch in identically designed transistors [19]. The line-edge roughness (LER) is considered as one of the major sources of device variability [20] which may lead to serious device parameter fluctuations and limit the performance in the VLSI circuit applications. Therefore, studying the LER variability, especially in GAA NWs which have all the channel interfaces affected by the LER, is essential

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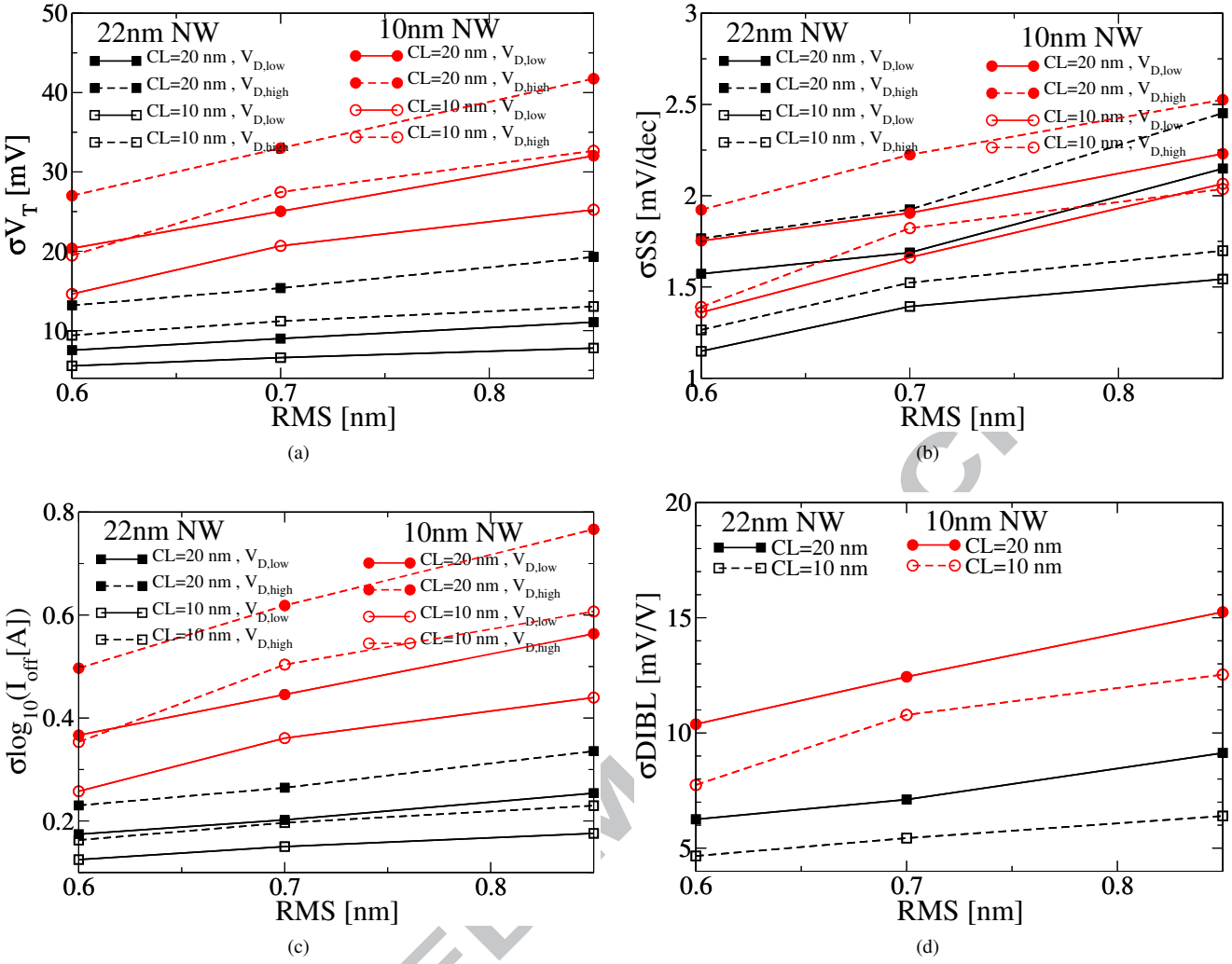

Fig. 8. Comparison of the V_T, SS, $\log_{10}$(IOFF) and DIBL variability versus the RMS height due to LER for the studied 22 nm and 10 nm gate length GAA NW FETs as a function of the drain bias, and the correlation length (CL). $V_{D,low}$=0.05 V and $V_{D,high}$=1.0 V for the 22 nm gate length NW, and $V_{D,low}$=0.05 V and $V_{D,high}$=0.7 V for the 10 nm gate length NW.

TABLE I. V_T AND SUB-THRESHOLD SLOPE (SS) AT $V_D = 0.05$ V (LOW) AND 1.0/0.7 V (HIGH) FROM THE DD, DIBL FROM THE DD AND FROM THE MC, AND DRIVE CURRENTS (I_{MC}) AT V_G = 1.0 V COMPARING 22 AND 10 NM GAA FETS.

Method	Gate length [nm]	22	10
MC	V_T [V]	0.3	0.35
DD	SS_{LOW} [mV/dec]	74	67
DD	SS_{HIGH} [mV/dec]	76	68
MC	$DIBL_{\langle 100\rangle}$ [mV/V]	81	66
MC	$DIBL_{\langle 110\rangle}$ [mV/V]	64	39
MC	$I_{\langle 100\rangle}$ [μA/μm]	1222	1320
MC	$I_{\langle 110\rangle}$ [μA/μm]	1000	1100

for predicting device behaviour in digital circuits. Here, we study the effect of uncorrelated LER (where we apply different LER profile at each side of the device, thus changing the width of the device across its length) using Fourier synthesis with Gaussian autocorrelation [21] implemented as described in Refs. [20], [22]. The LER is characterised by a correlation length (CL=Λ), and a root mean square value (RMS=Δ). The simulation method is based on the inverse discrete transformation and the application of a Gaussian filter over a list of random phases. The correlation length will be accounted for by the width of the Gaussian filter, and the amplitude will set the root mean square (RMS) value. To model the Fourier spectra, we use the following autocorrelation function:

$$S_G(\mathbf{k}) = \sqrt{\pi}\Delta^2\Lambda e^{(-k^2\Lambda^2/4)},$$

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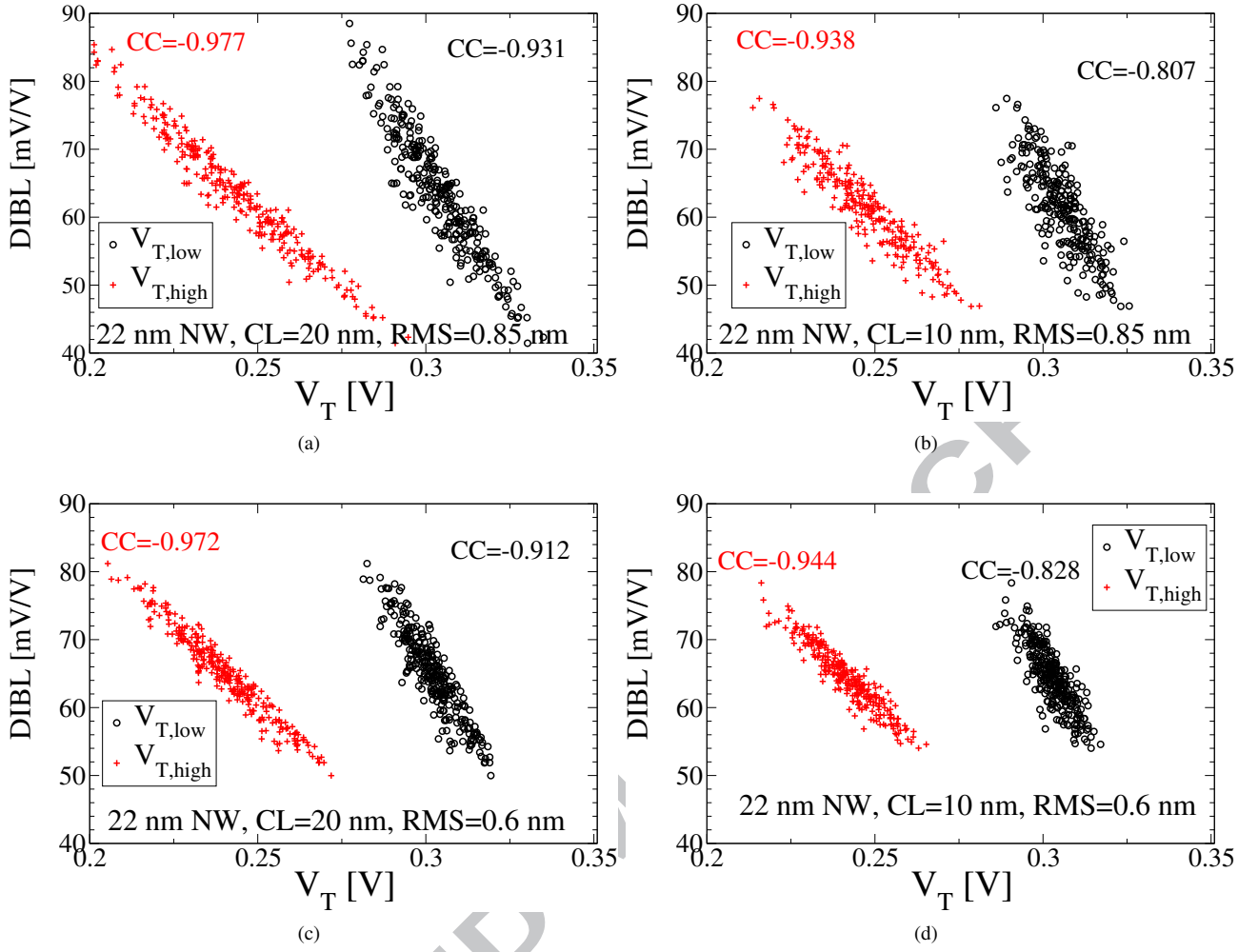

Fig. 9. Scatter plots showing the DIBL variation as a function of the V_T, at both low and high drain biases, due LER variations (CL=20/10 nm and RMS=0.6/0.85 nm) for the 22 nm gate GAA NW FET. $V_{D,low}$=0.05 V and $V_{D,high}$=1.0 V. Correlation coefficients (CC) are also calculated.

The simulations of variability for the 22 nm and the 10 nm gate length NW FETs are carried out using the 3D density gradient (DG) quantum corrected FE DD with a LER correlation length (CL) of 20 nm and 10 nm and three root mean square values (RMS=0.6, 0.7 and 0.85 nm) chosen to represent the RMS values observed in experiments [2], [3].

After we have calibrated DD-DG simulations to the results from 3D FE SEQC MC simulations, we analyse the LER-induced variability affecting the sub-threshold region of the device comparing four figures of merit: threshold voltage (V_T), OFF-current (I_{OFF}), sub-threshold slope (SS), drain-induced-barrier-lowering (DIBL). Ensembles of 300 devices have been used to investigate the LER-induced variability in the sub-threshold regions. We extract the threshold voltage using the fixed current approach and the OFF-current is extracted at $V_G = 0$ V. Fig. 8 shows a comparison of the V_T, SS, $\log_{10}$(IOFF) and DIBL variability due to the LER for the studied 22 nm and 10 nm gate length GAA NWs as a function of the drain bias, the correlation length, and the RMS height. In the presence of LER, the observed variations for the four figures of merit are smaller in the 22 nm gate length GAA NW at low and high drain biases than the ones observed in the 10 nm gate length GAA NW. As expected, the standard deviations for the four figures of merit are increasing with the increase of the RMS value. Note here that the standard deviations for the four figures of merit are strongly affected by the drain bias and the correlation length values in both NWs. The standard deviations for the four figures of merit are

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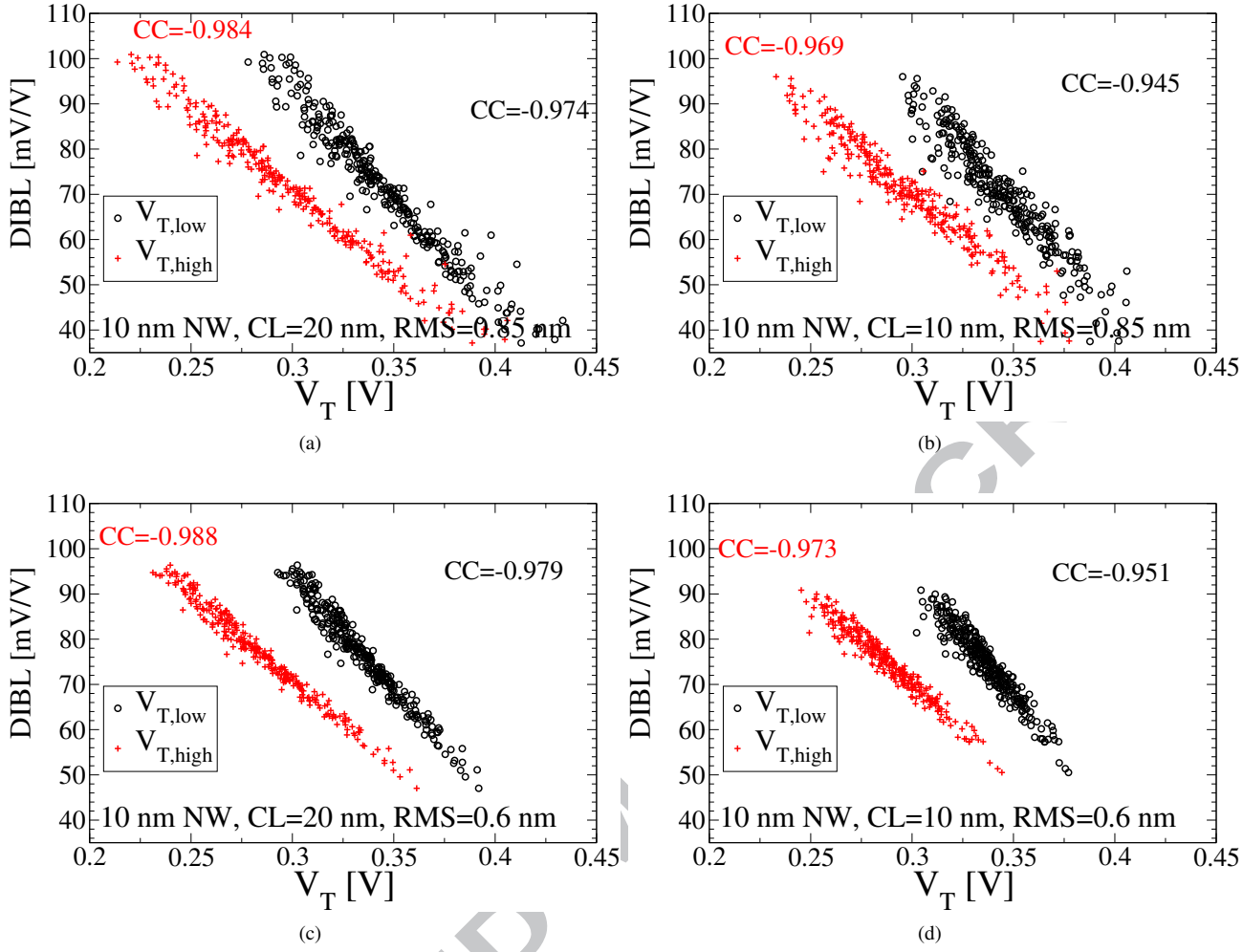

Fig. 10. Scatter plots showing the DIBL variation as a function of the V_T, at both low and high drain biases, due LER variations (CL=20/10 nm and RMS=0.6/0.85 nm) for the 10 nm GAA NW. $V_{D,low}$=0.05 V and $V_{D,high}$=0.7 V. Correlation coefficients (CC) are indicated as well.

increasing with the increase of the correlation length value, and also with the increase on the drain bias.

Fig. 9 shows the DIBL variability as a function of V_T at low and high drain biases due to LER with CL=(20 and 10 nm) and RMS=(0.6 and 0.85 nm) for the 22 nm gate length NW. In all cases, the DIBL shows strong negative correlations with $V_{T,low}$ (correlation coefficient (CC) ranges from -0.807 to -0.931) and shows even stronger correlations with $V_{T,high}$ (CC ranges from -0.938 to -0.977). The larger the CC value, the less sensitive the variability is to a change in the drain bias. The Q-Q plot (not shown here) indicates near-to-Gaussian behaviour especially at a high drain bias.

Fig. 10 shows the DIBL variability as a function of V_T at low and high drain biases due to LER with CL=(20 and 10 nm) and RMS=(0.6 and 0.85 nm) for the 10 nm gate length NW FETs. In all cases, the DIBL shows larger strong negative correlations with $V_{T,high}$ (CC ranges from -0.969 to -0.988) than with $V_{T,low}$ (CC ranges from -0.945 to -0.979). We can see that, for the 10 nm gate length NW, the CC values are larger than those for the 22 nm gate length NW. The Q-Q plot indicate more Gaussian behaviour as expected in a larger device but the DIBL for some specific 10 nm gate length devices can overtake the DIBL in the 22 nm one.

Fig. 11 shows the scatter plots of the threshold voltages at a high drain bias ($V_{T,high}$) against the threshold voltages at a low drain bias ($V_{T,low}$) for the 22 nm gate length Si GAA NW with CL=(20 and 10 nm) and RMS=(0.6 and

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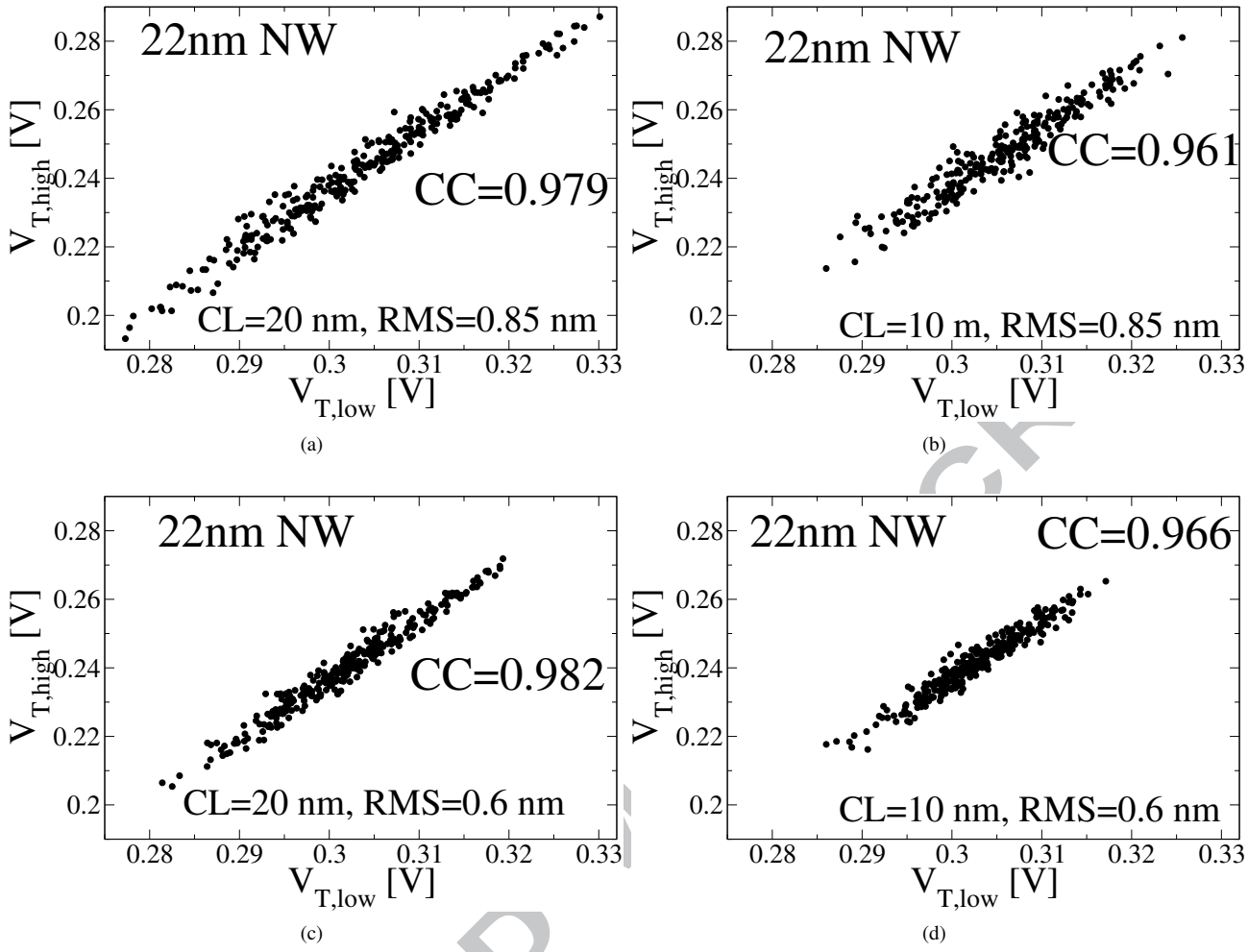

Fig. 11. Scatter plot showing the distribution of the threshold voltages at high drain bias ($V_{T,high}$) against the threshold voltages at low drain bias ($V_{T,low}$) for the 22 nm GAA NW with LER (CL=20, 10 nm and RMS=0.6, 0.85 nm) with respective correlation coefficients (CC).

0.85 nm). The threshold voltage at low and high drain biases are strongly correlated so we have used the same ranges for both the horizontal and vertical axis to show clearly the different behaviours. We can see that the threshold voltages with CL=20 nm have a larger CC value that those for the CL=10 nm which means the device variability is less sensitive to the change at the drain bias. In addition, the threshold voltages at a low drain bias ($V_{T,low}$=0.05 V) is more spread in the case of CL=20 nm. Fig. 12 shows the OFF-current ($I_{OFF,high}$) versus the threshold voltages ($V_{T,high}$) at V_D=1.0 V for the 22 nm GAA NW with CL=(20 and 10 nm) and RMS=(0.6 and 0.85 nm). The log of the OFF-current exhibits the typical linear dependence on the decreasing $V_{T,high}$ suggesting near-to-Gaussian behaviour as expected. Again, we can see that the variability with CL=20 nm have a larger CC value than those for the CL=10 nm, a characteristic of a lower variability in the SS.

IV. Conclusion

We have employed our 3D SEQC FE MC simulation toolbox to obtain the I_D-V_G characteristics of a 22 nm gate length GAA Si NW FET. The simulation toolbox accurately describes the nanoscale geometry of multi-scale transistors using the FE method, and employs a completely parameter-free model of carrier transport which uses fully anisotropic transport model together with fully anisotropic quantum corrections which dependent on the valley orientation (longitudinal and transverse electron effective masses orientation along the de-

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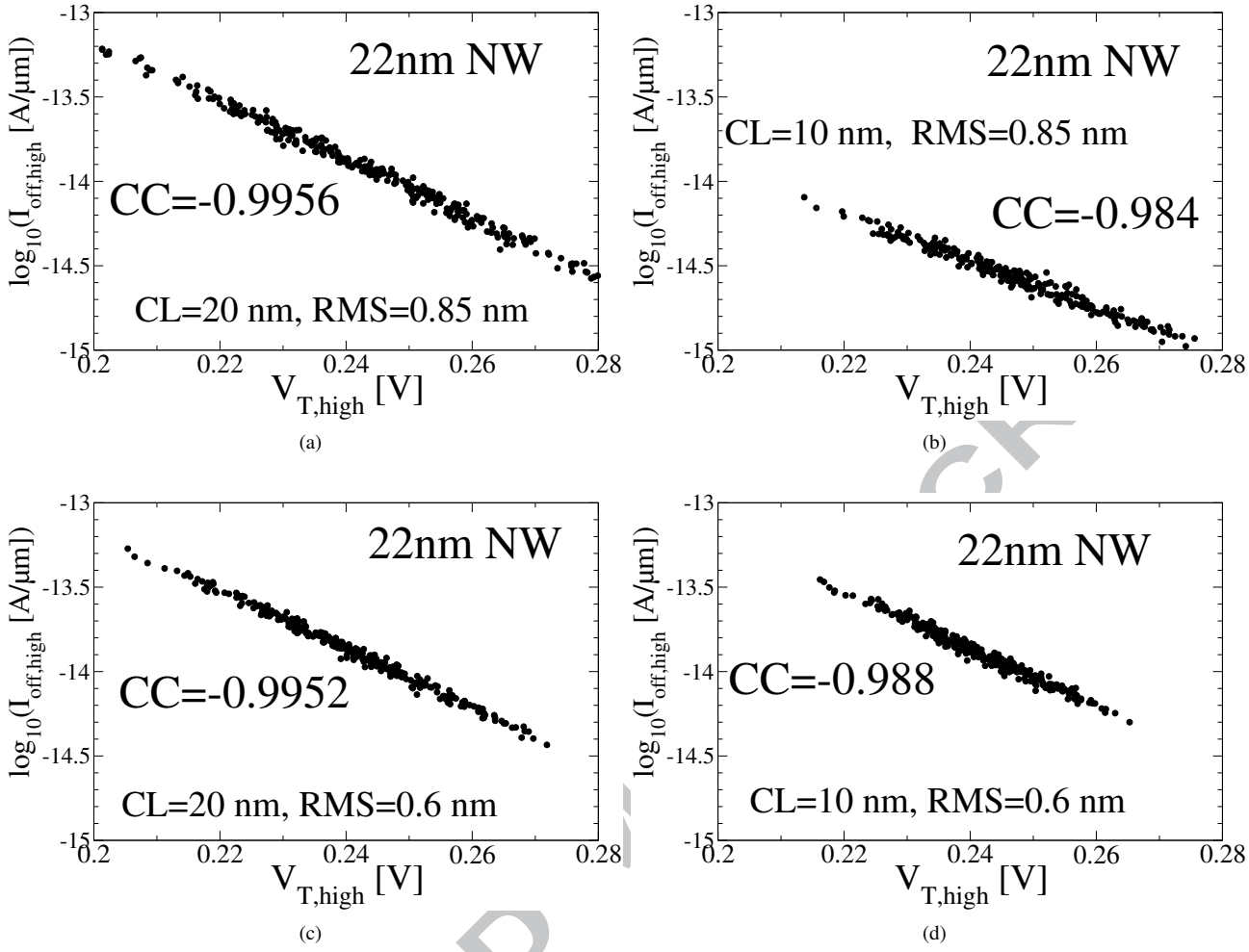

Fig. 12. $\log_{10}(I_{OFF,high})$ vs. $V_{T,high}$ at V_D=1.0 V for the 22 nm GAA NW FET with the LER (CL=20, 10 nm and RMS=0.6, 0.85 nm).

vice channel). The I_D-V_G characteristics at low and high drain biases obtained from the 3D MC toolbox demonstrated exceptional agreement with the experimental data [2] without any additional post-processing of lumping access resistance. We have then scaled the GAA Si NW FET to the 10 nm gate length and predicted that the scaled device will deliver an on-current of 1320/1100 μA/μm for the $\langle 100\rangle/\langle 110\rangle$ channel with superior electrostatic integrity of a nearly ideal sub-threshold slope of 68 mV/dec and a DIBL of 39 mV/V. Finally, we have studied the effects of LER-induced variability on the sub-threshold characteristics (V_T, I_{OFF}, SS and DIBL) for both the 22 nm and the 10 nm gate length GAA NWs. Our simulations indicate that the 22 nm gate length NW is less sensitive to variability than the 10 nm one. We have found that the LER induced variability of the threshold voltage in the 22 nm gate length GAA NW FETs exhibits σV_T of about $9.5-19.2$ mV and $\sigma \log_{10}(I_{OFF})$ of about $0.16-0.33$ A at high drain bias. The LER induced variability for the 10 nm GAA NW FETs is much larger. The variability of the threshold voltage, σV_T, is about $19.5-42$ mV and, the variability of the OFF-current, $\sigma \log_{10}(I_{OFF})$, is about $0.35-0.76$ A at a high drain bias. The 22 nm gate length GAA NW shows smaller variations for the four figures of merit at low and high drain biases than the ones observed in the 10 nm gate length GAA NW (see Fig. 8) as expected but the increase in the device variability is relatively small when comparing correlation coefficients (CC) [6], [7]. This demonstrates that the GAA NW FETs are strong candidates for future generation of digital transistors delivering large on-current required in a circuit design accompanied by a well controlled device variability.

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