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Simulation Study of Scaled $In_{0.53}Ga_{0.47}As$ and Si FinFETs for Sub-16 nm Technology Nodes

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Abstract. *We investigate the performance and scalability of III-V-OI $In_{0.53}Ga_{0.47}As$ and SOI Si FinFETs using state-of-the-art in-house-build 3D simulation tools. Three different technology nodes specified in the ITRS have been analysed with gate lengths (L_G) of* 14.0 *nm,* 12.8 *and* 10.4 *nm for the InGaAs FinFETs and of* 12.8 *nm,* 10.7 *and* 8.1 *nm for the Si devices. At a high drain bias, the* 12.8 *and* 10.4 *nm InGaAs FinFETs deliver* 15% *and* 13% *larger on-currents but* 14% *larger off-currents than the equivalent* 12.8 *and* 10.7 *nm Si FinFETs, respectively. For equivalent gate lengths, both the InGaAs and the Si FinFETs have the same* I_{ON}/I_{OFF} *ratio (5.9×10^4 when L_G =* 12.8 *nm and 5.7×10^4 when L_G = 10.4(10.7) nm). A more pronounced S/D tunnelling affecting the InGaAs FinFETs leads to a larger deterioration in their SS (less than 10%) and DIBL (around 20%) when compared to the Si counterparts.*

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Keywords: Monte Carlo, quantum-corrections, drift-diffusion, III-V materials, Si, scaling.

1. Introduction

The ITRS considers 3D multi-gate devices, such as FinFETs, to be the next solution for CMOS scaling into sub-16 nm digital technology nodes [1] because they provide improved electrostatic control, help to eliminate short channel effects, achieve close to ideal sub-threshold slopes and reduce the drain-induced barrier lowering (DIBL).

Nowadays, there is a great interest in the use of III-V materials in the channel of transistors for their possible use in future high-speed and low-power applications [2] because of their high electron mobility and saturation velocity [3]. However, thanks to the constant innovations in the field, Si-based devices are still the most popular in industry and this material is widely selected as channel for the CMOS tecnhology [4]. Therefore, a fair and complete scaling comparison between nanoscale Si and III-V FinFETs is of utmost importance. There have been previous efforts in literature to compare Si and III-V multi-gate technologies [5] [6]. In [5], Non-Equilibrium Green's Functions (NEGF) simulations have been used to analyse $In_{0.75}Ga_{0.25}As$ and strained-Si channel multi-gate transistors in a ballistic regime but only for a particular gate length (L_G=12 nm). In [6], the comparison was focused mainly on the on-current and the effective velocity.

In this paper, we investigate the performance and scalability of III-V-OI and SOI FinFETs in both the sub-threshold and on-region via 3D finite-element quantum-corrected drift-diffusion and ensemble Monte Carlo simulations. We also compare the average electron velocity, kinetic energy, and sheet density along the channel of the FinFET devices in the on-current transistor conditions as a function of the gate length. The Si and the $In_{0.53}Ga_{0.47}As$ FinFETs have been designed to meet the 2013 ITRS targets for high-performance logic multi-gate devices [1] so we compare equivalent technologies.

Simulation results will demonstrate that the InGaAs FinFETs show an similar overall performance than the Si devices but their sub-threshold region characteristics are more strongly affected in the scaling process. This larger sensitivity to the scaling may be an obstacle for the future integration of this technology.

2. Simulation methodology

2.1. Device structure

For both the $In_{0.53}Ga_{0.47}As$ (InGaAs) and Si devices, we have followed the ITRS 2013 prescriptions for high-performance logic multi-gate devices [1] dictating the gate length, EOT, body thickness and channel doping. The body height of the devices was chosen to be 2.5 times of the body thickness value. The S/D doping was obtained from the appropriate scaling of a 25 nm gate length device that had been calibrated against experimental data [7]. Therefore, we have not fixed any parameter to perform the comparison between InGaAs and Si devices, not even the off-current. The geometry of the simulated devices including rounded corners is shown in Fig. 1. Their dimensions,

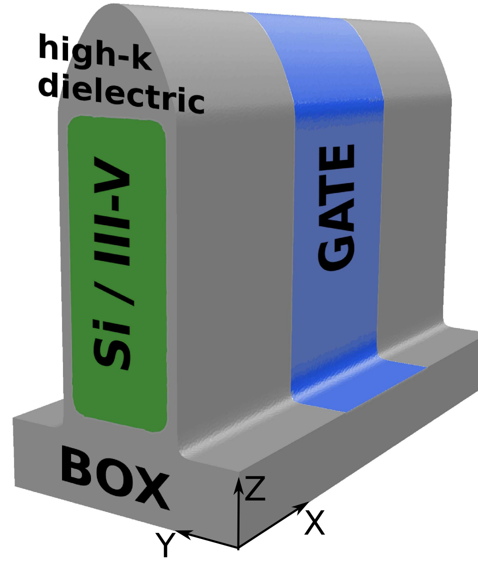

Figure 1. Schematic structure of the simulated InGaAs and Si FinFETs.

Table 1. Dimensions, doping concentrations, supply voltage (V_{DD}), threshold voltage (V_T) and (I_{ON}/I_{OFF}) ratio for the simulated $In_{0.53}Ga_{0.47}As$ and Si FinFETs.

Symbol	$In_{0.53}Ga_{0.47}As$			Si		
L_G(nm)	14.0	12.8	10.4	12.8	10.7	8.1
EOT(nm)	0.68	0.65	0.59	0.67	0.62	0.55
W_{fin}(nm)	8.5	7.7	6.1	7.0	5.8	4.5
H_{fin}(nm)	21.25	19.25	15.25	18.0	12.0	11.0
L_{SD}(nm)	14.0	12.8	10.4	12.8	10.7	8.1
N_{ch}(cm^{-3})	10^{17}	10^{17}	10^{17}	10^{15}	10^{15}	10^{15}
N_{SD}(cm^{-3})	5×10^{19}	5×10^{19}	5×10^{19}	10^{20}	10^{20}	10^{20}
V_{DD}(V)	0.60	0.60	0.60	0.70	0.70	0.60
V_T(V)	0.24	0.24	0.24	0.22	0.22	0.22
$\frac{I_{ON}}{I_{OFF}}$($\times 10^4$)	6.7	5.9	5.7	5.9	5.7	5.5

doping concentrations, supply and threshold voltages, and I_{ON}/I_{OFF} ratios are listed in Table 1. The *n*-type doping in the S/D regions is considered to be a Gaussian-like (with a peak value of N_{SD}) and the *p*-type doping (N_{ch}) in the channel is uniform.

In the comparison of the scaling of Si and InGaAs FinFETs, two mutually exclusive criteria can be followed: i) devices with corresponding gate lengths or ii) devices that belong to the same technological node. In this paper, we have compared two set of devices with either the same or very similar gate lengths (12.8/10.4 nm InGaAs FinFETs and 12.8/10.7 nm Si FinFETs). We have also compared the 14.0 nm InGaAs and the 12.8 nm Si FinFETs which are forecast for the same technology node (7 nm) expected to be in production around 2018. Finally, the 8.1 nm Si FinFET was selected following

the premises of having three technology nodes for each material, in order to have more data available to extract trends and analyse behaviours.

2.2. Three-dimensional simulators

Initially, we have used a parallel 3D finite-element (FE) drift-diffusion (DD) simulator [8] that includes quantum corrections via the density gradient (DG) approach [9] to obtain the sub-threshold region characteristics. These simulation results are also used as an initial condition for MC transport model. Bearing in mind the physical and numerical noise in Monte Carlo simulations that affects the calculations of currents at a low gate bias, the combination of quantum-corrected DD simulations employed in the sub-threshold region and a state-of-the-art 3D FE quantum corrected MC simulations used then in the on-region is perfectly reasonable [7].

The DD-DG simulations have been calibrated at both low (0.05V) and high drain biases ($\mathrm{V_{DD}}$) against 3D NEGF simulations [10, 11] with an excellent agreement (see examples in Fig. 2 and in [8]). The electron effective masses in the semiconductor region and in the oxide used in the DG approach act as calibration parameters [12] representing the strength of the confinement. The mass in the x-direction will partially account for the source-to-drain tunnelling in the sub-threshold region. Using DD-DG simulations, we have extracted all the figures of merit affecting the sub-threshold: off-current (I_{OFF}), sub-threshold slope (SS), threshold voltage ($\mathrm{V_T}$), and drain-induced-barrier-lowering (DIBL).

In the on-regime, we have used quantum-corrected 3D FE ensemble Monte Carlo (MC) simulations which are well-know for their predictive power from V_{T} on-wards [7], as seen in the comparison of NEGF and MC simulations in the inset of Fig. 2. The presented NEGF simulations include the phonon scattering but omit ionised impurity scattering and interface roughness [13], overestimating slightly current at a large overdrive [14]. In the MC simulator, the quantum corrections are included via the solution of the DG equation for the InGaAs device [7], and the 2D Schrödinger equation for the Si device [15]. This MC tool uses an analytic non-parabolic anisotropic model for energy dispersion in valleys [16], scatterings with acoustic phonon, non-polar optical intra-valley and inter-valley phonons, interface roughness via Ando's model [17], and ionized impurities using the third-body exclusion model by Ridley [18]. In the InGaAs device simulations, polar optical phonon, piezoelectric, and alloy scatterings are also included [19]. Finally, Fermi-Dirac statistics were considered in the modelling of III-V devices due to a relatively high level of doping in their S/D regions [20]. Note that all the in-house simulators used in this work have been previously compared to experimental data for both Si [7] and III-V [21] multi-gate devices. Finally, for the calculation of the ($\frac{\mathrm{I_{ON}}}{\mathrm{I_{OFF}}}$) ratio we have used the off-current coming from DD-DG simulations and the on-current coming from MC simulations.

Figure 3 shows the drain current as a function of the gate voltage in a generic FinFET device on a logarithmic scale at both low (blue curve) and high drain biases

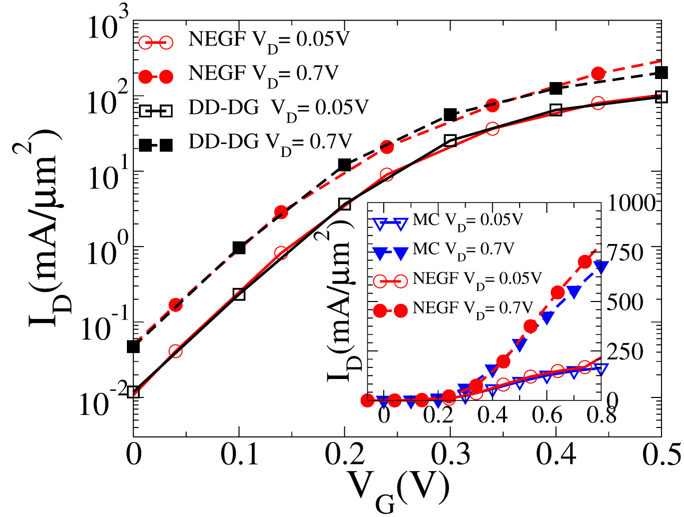

Figure 2. I_D-V_G characteristics at V_D=0.05 V and V_{DD}=0.7 V of the 10.7 nm gate length Si FinFET comparing 3D DD-DG to NEGF simulations in the sub-threshold region. The inset shows a comparison of NEGF and Monte Carlo simulations.

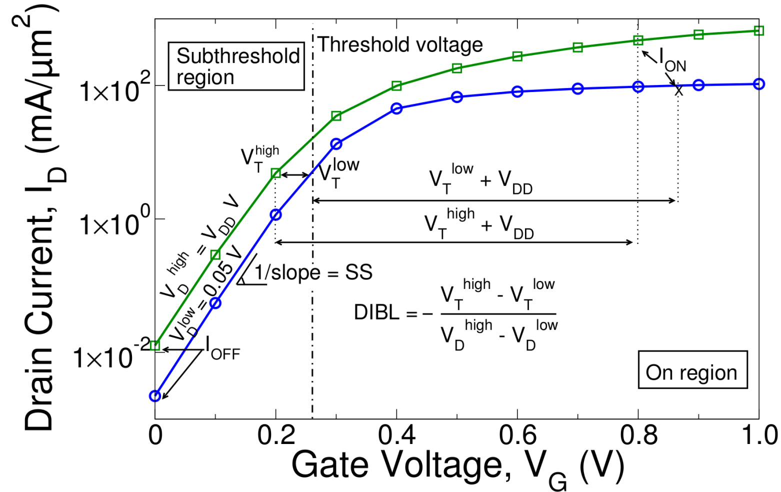

Figure 3. I_D-V_G characteristics in a generic FinFET device at both low (blue curve) and high drain biases (green curve). The figure provides information regarding the methodology followed to extract the different figures of merit under comparison.

(green curve). In both curves, we have marked how we have extracted the different figures of merit analysed in this paper; the off-current is the current at V_G=0.0 V and the on-current is calculated as the drain current when V_G=V_{DD}+V_T. In the sub-threshold region, the drain current increases exponentially with the gate bias, with a slope that on a logarithmic scale is the sub-threshold slope (SS). The formula used to calculate the DIBL, which provides a measurement of the reduction of the threshold voltage when the drain bias is increased, is also shown in the figure.

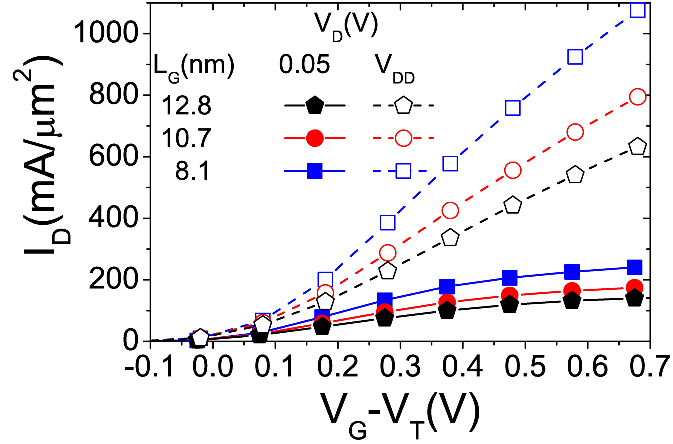

Figure 4. I_D-V_G characteristics normalised by the cross-section area at V_D=0.05 V and V_{DD} for the scaled Si FinFETs. V_{DD}=0.7 V when L_G=12.8, 10.7 nm and V_{DD}=0.6 V for L_G=8.1 nm.

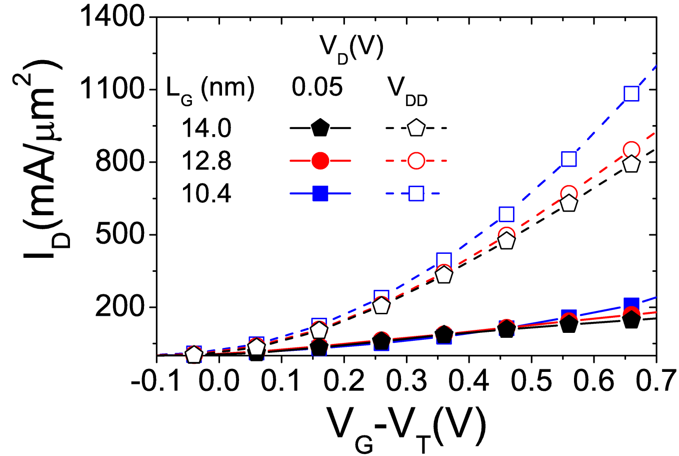

Figure 5. I_D-V_G characteristics at V_D=0.05 V and V_{DD}=0.6 V normalised by the cross-section area for the scaled InGaAs FinFETs.

3. Performance of Scaled FinFETs

3.1. I-V characterisation

Figs. 4 and 5 show the Si and InGaAs FinFETs I_D-V_G characteristics obtained from MC simulations for the three gate lengths at low and high drain biases. The channel orientation is always ⟨100⟩ for a fair comparison.

In our simulations we have not considered any external contact resistances since we are looking at the intrinsic device performance of the devices. However, knowing that at a high gate bias most of the resistance comes from the the S/D region, the access resistance has been calculated for the three different gate lengths. For the InGaAs FinFET, the S/D access resistance decreases from 72 $\Omega \cdot \mu$m when L_G=14 nm to 48 $\Omega \cdot \mu$m when L_G=12.8 nm and to 31 $\Omega \cdot \mu$m when L_G=10.4 nm. The S/D region in

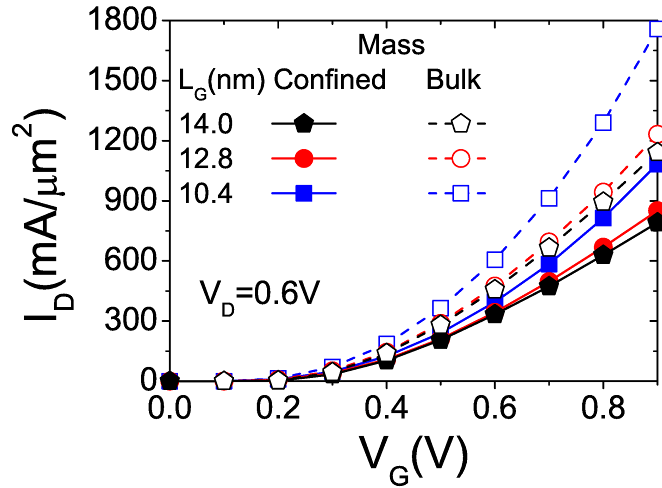

Figure 6. I_D-V_G characteristics at a high drain bias for the scaled InGaAs FinFETs comparing the effect of using the Γ-valley bulk electron effective masses or the confinement electron effective masses deduced from tight-binding calculations [22].

the 14 nm gate length InGaAs FinFET has a relatively low effective density of states with the most of carriers in the Γ valley, which explains a relative large value of the access resistance. When the device is scaled down, the L and X valleys will become more occupied. Thus the effective density of states will increase leading to the observed reduction in the access resistance [19]. The S/D region in the Si FinFETs with the three studied gate lengths has the most of carriers still in the X valley. Therefore, a change in both the density of states and, consequently, the access resistance (around 32 $\Omega \cdot \mu$m) is negligible.

The Γ valley confinement effective masses, deduced from tight-binding calculations for III-V ultra-thin body SOI MOSFETs [22], have been used in the InGaAs FinFETs, while the effective masses in the L and X valleys are assumed to be bulk. The following confinement effective masses have been used: 0.0693m_0 when L_G=14 nm, 0.0723m_0 when L_G=12.8 nm and 0.0835m_0 when L_G=10.4 nm. Fig. 6 shows the I_D-V_G characteristics comparing the effect of using the Γ valley bulk effective masses or the confinement effective masses. When the confined masses are used, there are substantial 29% (when L_G=14.0 and 12.8 nm) and 37% (when L_G=10.4 nm) decreases in the I_D-V_G characteristics when compared to the results from bulk effective mass calculations.

3.2. Comparison of off- and on-region figures of merit

Fig. 7 compares the scaling for on- and off-currents. At a high drain bias, the Si FinFET scaling from the 12.8 nm to 10.7 and 8.1 nm gate lengths increases the on-current 25% and 64%, respectively. For the InGaAs FinFET, the increases are 7% and 33% when scaled down from 14.0 nm to 12.8 and 10.4 nm gate lengths. At a drain bias of V_{DD}, the off-current increases by 29% and 59% in the Si FinFET scaled from 12.8 nm to 10.7 and 8.1 nm gate lengths. In the InGaAs FinFET, the increases in the off-current are

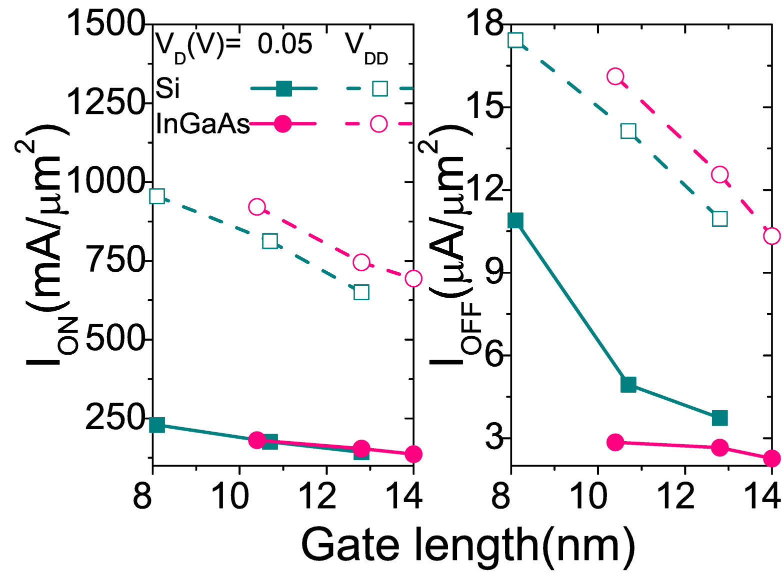

Figure 7. Comparison of the on-currents and off-currents as a function of the gate length and the drain bias for the InGaAs and Si FinFETs.

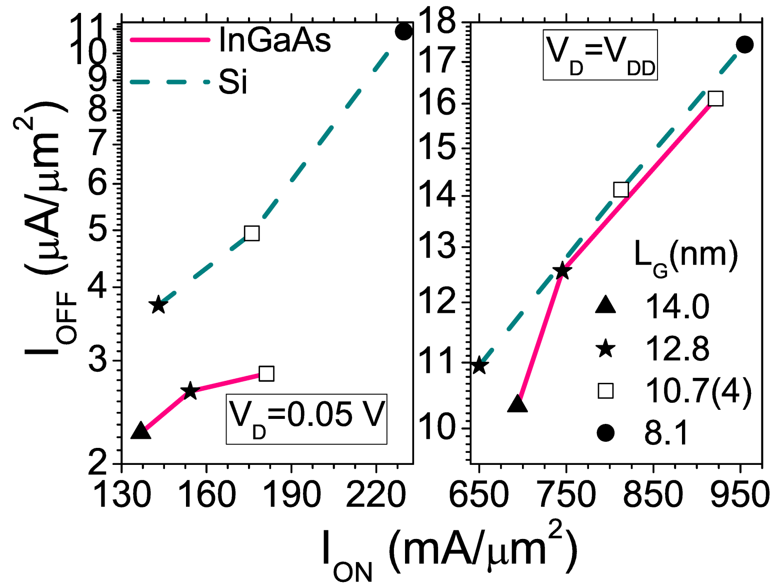

Figure 8. Off-current versus on-current for the three scaled InGaAs and Si FinFETs as a function of the drain bias.

21% and 56% for gate lengths scaled from 14.0 nm to 12.8 and 10.4 nm, respectively. Note that, at a low drain bias, the off-current is smaller for the InGaAs FinFET than that for the Si device. This is due to the confinement of the density in the channel, which is stronger in the InGaAs device than in the Si one [23], especially at a low gate bias, resulting in a better electrostatic integrity.

Comparing Si and InGaAs technologies for the devices with a similar gate length, the 12.8 and 10.4 nm InGaAs FinFETs deliver 15% and 13% larger on-currents and 14%

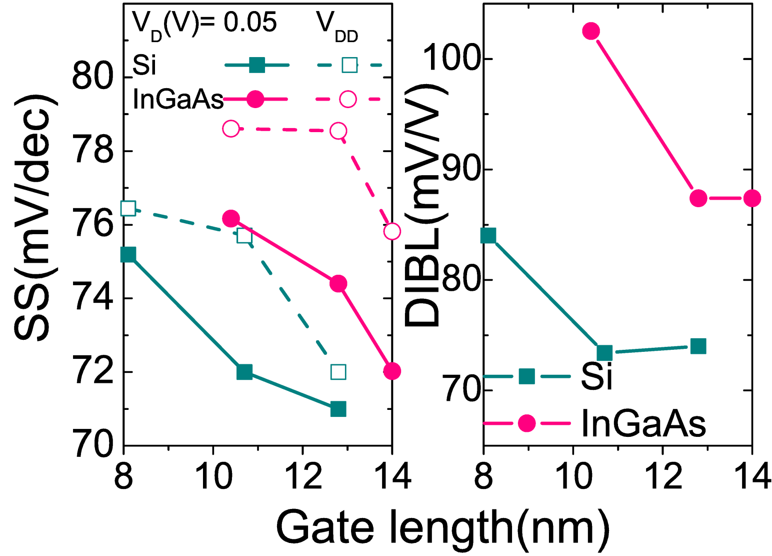

Figure 9. Comparison of the SS and DIBL as a function of the gate length and the drain bias for the InGaAs and Si FinFETs.

larger off-currents than the 12.8 and 10.7 nm Si FinFETs. Fig. 8 shows the off-current versus on-current as a function of the gate length and the drain bias. When focusing on the devices with a similar gate length, the InGaAs transistors have a larger I_{ON} at high drain bias and, at the same time, a larger I_{OFF}, thus lying on the same universal curve as Si transistors, indicating that they both have a comparable performance. As a consequence, both Si and InGaAs technologies have the same I_{ON}/I_{OFF} ratio for equivalent channel lengths (see Table 1). Note that, the higher the I_{ON}/I_{OFF} ratio, the better the trade-off between high-frequency performance and power consumption. Another figure of merit that can be assessed is the stand-by power consumption, which is critical for system-on-a-chip mobile applications. The static power is comparable for both technologies, with values around 8 μW/μm^2 and 10 μW/μm^2 for the 12.8 and 10.7(4) devices, respectively.

In this paper, the comparative study of InGaAs and Si transistors is centred in devices with the same channel length. However, both the 14.0 nm InGaAs and the 12.8 nm Si FinFETs are aimed for the same technology node (7 nm) that is expected to be in production in 2018 [1] and a comparison between them may also be relevant. The 14.0 nm InGaAs device exhibits 12% larger I_{ON}/I_{OFF} ratio and 20% lower static power than those of the 12.8 nm Si device.

Fig. 9 shows the scaling of the sub-threshold slope (SS) and drain-induced-barrier-lowering (DIBL) for the InGaAs and Si FinFETs (bottom figures). At a high drain bias, the SS in the Si FinFETs is ranging from 72 to 76 mV/dec when L_G is scaled down from 12.8 to 8.1 nm. For the InGaAs FinFETs, the SS is increasing from 76 to 79 mV/dec when the gate length is scaled from 14.0 to 10.4 nm. The more pronounced source-to-drain tunnelling affecting the InGaAs FinFETs leads to a slight degradation

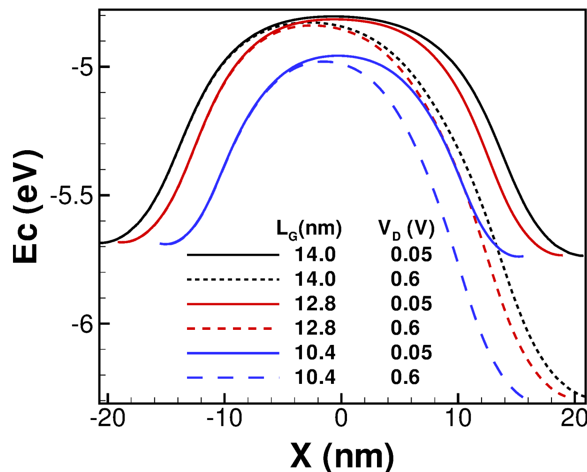

Figure 10. Conduction band profile along the channel of the InGaAs FinFET for the three analysed gate lengths at indicated low and high drain biases (V_D) when V_G=V_T.

in their SS (less than 10%) when compared to the Si counterparts, at both low and high drain biases. The smaller off-current and sub-threshold slope, which is related to the device switching speed, provided by the Si FinFETs may indicate that these devices are better suited to be used on digital applications.

The DIBL remains practically unchanged (around 74 mV/V) during the scaling from the 12.8 nm Si FinFET to the 10.7 nm gate and from the 14.0 nm InGaAs FinFET to the 12.8 nm gate (DIBL=87 mV/V). However, a noticeable increase in the DIBL is observed in the 8.1 nm Si (DIBL=84 mV/V) and 10.4 nm InGaAs FinFETs (DIBL=102 mV/V) because short channel effects start to occur. The worsening in the DIBL characteristics observed with the reduction in the gate length will have, from the fabrication point of view, an important impact on the scalability of both Si and III-V devices. In order to illustrate this effect, Fig. 10 shows the conduction band along the channel for the three scaled InGaAs FinFETs at the threshold. The electrostatic integrity of the 14.0 and 12.8 nm gate length InGaAs FinFETs (also seen for the 12.8 and 10.7 nm gate length Si devices) is similar, with barrier height values of 0.88 and 0.87 eV, respectively. However, when the gate length is reduced to 10.4 nm, there is a substantial decrease in the barrier height to 0.73 eV. Finally, note that, when comparing Si and InGaAs technologies for the devices with a similar gate length, the DIBL for the InGaAs devices is between 17%–27% larger to that of Si. This may have an impact on the suitability of III-V devices for future low-power high-performance digital applications.

3.3. Average velocity, carrier density and energy

Fig. 11 reports the average velocity profiles along the $\langle 100 \rangle$ channel in the scaled Si (left) and InGaAs (right) FinFETs. The velocity at a certain position in the transport direction X is calculated via an average of the velocity of all the particles located in the 2D perpendicular cross-sectional slice (Y and Z directions). The average velocity inside

the channel of the Si FinFET increases with a reduction in the gate length, reaching a peak value of 1.89×10^7 cm/s when the gate length is 12.8 nm and of 2.06×10^7 cm/s for the 8.1 nm gate length. The lower effective mass and reduced scattering present in the InGaAs FinFETs leads to a peak velocity three times larger than in the equivalent Si devices, which will favour a faster switching time and less power dissipation of the transistors. In the InGaAs FinFETs, when the gate length is shrunk from 14.0 12.8 nm, the average velocity also increases, with peak values ranging from 6.06×10^7 cm/s to 6.63×10^7 cm/s. However, when the gate length is 10.4 nm the average velocity is reduced (note that its peak value is 5.95×10^7 cm/s) due to the increase in the Γ valley confinement effective masses.

Fig. 12 shows the electron kinetic energy profiles along the $\langle 100 \rangle$ channel of the scaled Si (left) and InGaAs (right) FinFETs. The kinetic energy at a certain position X is calculated via an average of the energies of all the particles located in the 2D perpendicular cross-sectional plane. For the Si FinFETs, the kinetic energy increases at the end of the source region and along the channel until reaching a maximum inside the drain side of the device. Note that, when L_G=8.1 nm, the maximum kinetic energy is lower than the one observed in the 12.8 and 10.7 nm gate length devices due to the long-range Coulomb interaction between the S/D regions [19] (effect also seen in the 10.4 nm InGaAs device). On the other hand, the InGaAs FinFETs have a quite large kinetic energy (around 0.3 eV) in the highly doped region in the source due to a high level of degeneracy. At the end of the source region, the doping decreases and so does the degeneracy, leading to a sharp reduction in the energy of the electrons until they penetrate into the channel where their kinetic energy increases again until a maximum inside the channel, close to the drain. Then the kinetic energy will drop to finally increase once more in the heavily doped drain region.

Fig. 13 shows a comparison of the electron sheet density along the $\langle 100 \rangle$ channel for the scaled Si (left) and InGaAs (right) FinFETs. The sheet density at a certain position X is calculated via an average of all the particles located in the 2D perpendicular plane. Results show that, for the equivalent gate length devices, the electron sheet density is larger for Si than for InGaAs. At the start of the channel, the 12.8 and 10.7 nm gate length Si FinFETs have electron sheet densities of 2.0×10^9 and 1.7×10^9 cm^{-1}, whereas the sheet densities for the 12.8 and 10.4 nm gate length InGaAs FinFETs will only be 1.1×10^9 and 0.9×10^9 cm^{-1}.

4. Conclusion

In this paper, we have investigated the performance and scalability of three gate length $In_{0.53}Ga_{0.47}As$ (14.0, 12.8 and 10.4 nm) and Si FinFETs (12.8, 10.7 and 8.1 nm) using 3D quantum-corrected simulation tools. The selected FinFETs have been modelled following the ITRS targets for high-performance logic multi-gate devices.

When both technologies for the devices with equivalent gate lengths are compared, the 12.8 and 10.4 nm InGaAs FinFETs deliver larger on-currents (between 13% and

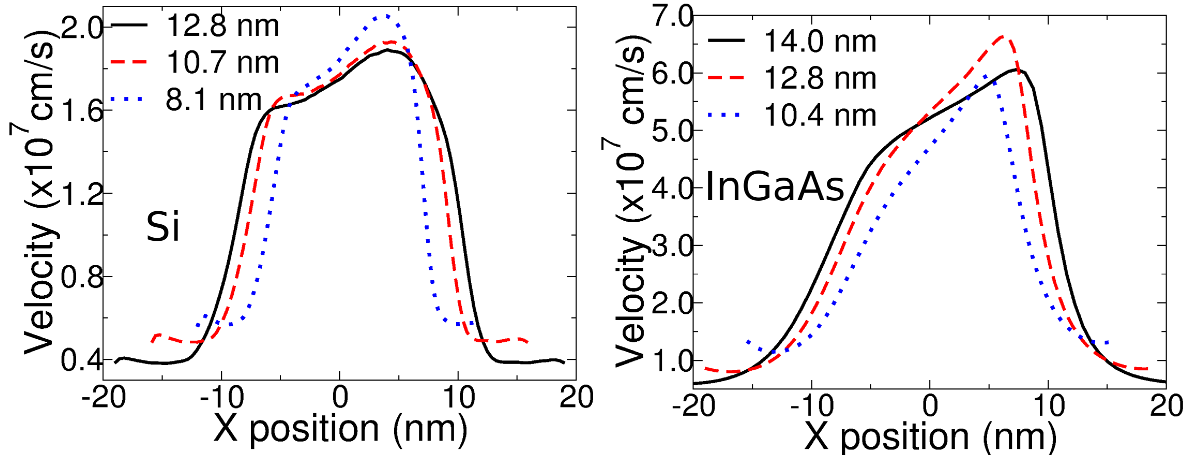

Figure 11. Average electron velocity along the ⟨100⟩ channel for the Si (left) and InGaAs (right) FinFETs with indicated gate lengths at V_G-V_T=V_{DD} and V_D= V_{DD}. The zero is set in the middle of the gate.

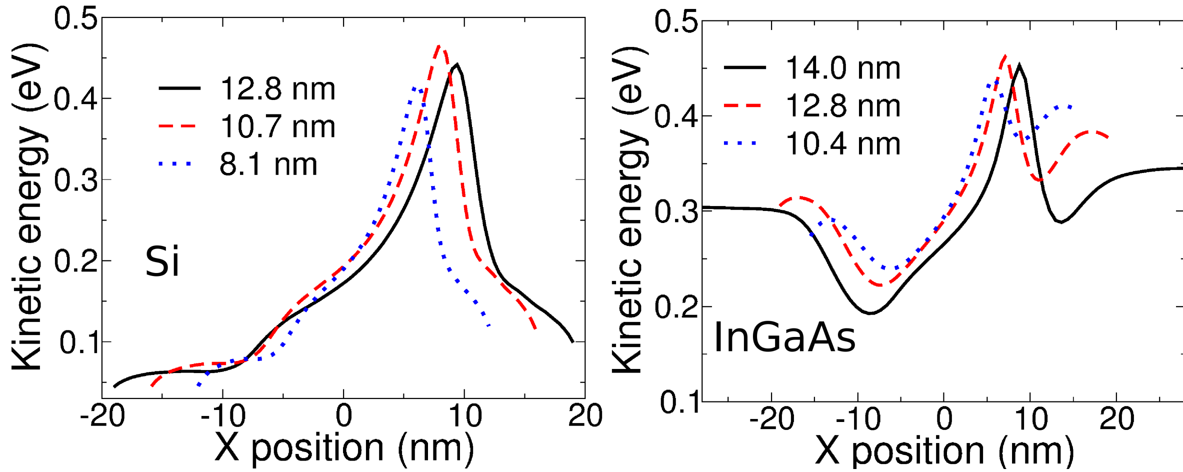

Figure 12. Kinetic energy along the ⟨100⟩ channel as a function of the gate length for the Si (left) and InGaAs (right) FinFETs with indicated gate lengths at V_G-V_T=V_{DD} and V_D= V_{DD}. The zero is set in the middle of the gate.

15%) and larger off-currents (around 14%) than the respective 12.8 and 10.7 nm Si FinFETs. Consequently, both technologies have a comparable performance, as indicated by their same I_{ON}/I_{OFF} ratio (5.9×10^{14} the 12.8 nm devices and 5.7×10^{14} for the 10.7(4) nm ones). The stand-by power consumption is also similar for both technologies, with values around 8 μW/μm^2 and 10 μW/μm^2 for the 12.8 and 10.7(4) devices, respectively.

When both technologies for the devices that belong to the same technology node of 7 nm are compared, the 14.0 nm InGaAs and the 12.8 nm Si FinFETs, results show that the 14.0 nm InGaAs device exhibits 12% larger I_{ON}/I_{OFF} ratio and 20% lower static power than those of the 12.8 nm Si device.

There is a sharp increase in the DIBL when these devices are scaled down to 8.1 nm

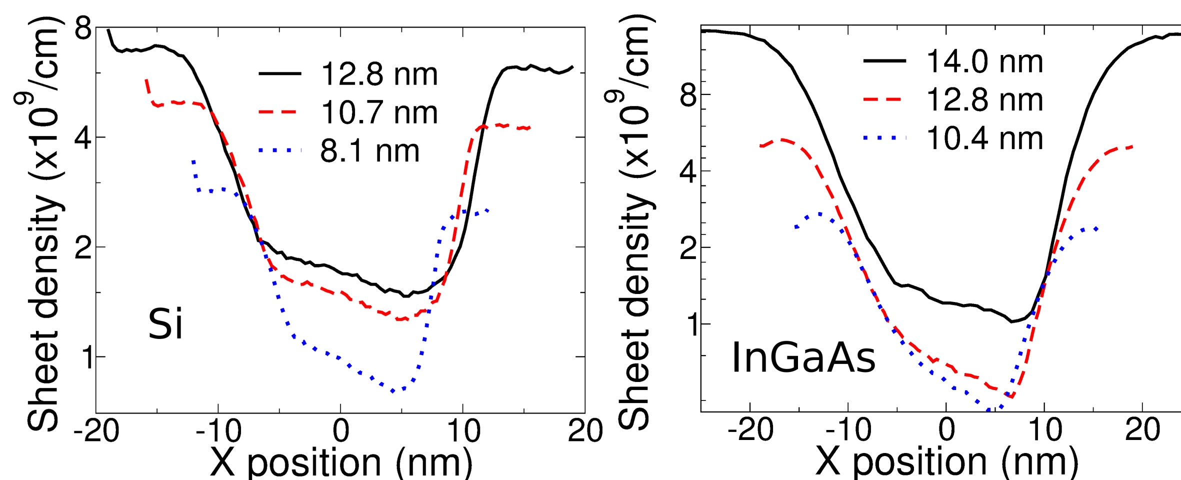

Figure 13. Electron sheet density along the ⟨100⟩ channel for the Si (left) and InGaAs (right) FinFETs with indicated gate lengths at V_G-V_T=V_{DD} and V_D= V_{DD}. The zero is set in the middle of the gate.

for the Si FinFETs and to 10.4 nm for the InGaAs FinFETs due to increase in short channel effects. However, the InGaAs FinFETs show up to 10% larger SS and around 17%-27% larger DIBL values compared to Si counterparts with the equivalent gate length. This deterioration in sub-threshold characteristics of the InGaAs multi-gate transistors has to be considered for a future integration of the technology. However, there is room for improvement of the sub-threshold characteristics in InGaAs FinFETs by adjusting the width of the quantum well (thickness of the InGaAs layer), the indium content, or the p-type doping in the substrate.

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References

[1] The International Technology Roadmap for Semiconductors (ITRS), 2013 URL `http://www.itrs.net/`
[2] Chau R, Datta S and Majumdar A 2005 *CSIC Digest* 17–20
[3] Kalna K, Seoane N, Garcia-Loureiro A, Thayne I and Asenov A 2008 *IEEE Trans. Electron Devices* **55** 2297–2306
[4] Antoniadis D, Khakifirooz A, Aberg I, Chlirigh C, Nayfeh O and Hoyt J 2006 *Electrochem. Soc. Trans.* **3** 3–15
[5] Park S, Liu Y, Kharche N, Jelodar M, Klimeck G, Lundstrom M and Luisier M 2012 *IEEE Trans. Electron Devices* **59** 2107–2114
[6] Fischetti M 2012 Post-Si-CMOS Devices - Scaling FETs to (Beyond?) 10 nm: From Semiclassical to Quantum Models *2012 International Silicon-Germanium Technology and Device Meeting (ISTDM)* pp 1–2

[7] Aldegunde M, García-Loureiro A and Kalna K 2013 *IEEE Trans. Electron Devices* **60** 1561–1567
[8] Seoane N, Indalecio G, Comesana E, Aldegunde M, Garcia-Loureiro A and Kalna K 2014 *IEEE Trans. Electron Devices* **61** 406–472
[9] Ancona M G and Iafrate G J 1989 *Phys. Rev. B* **39**(13) 9536–9540 URL `http://link.aps.org/doi/10.1103/PhysRevB.39.9536`
[10] Silvaco Inc. 2012 *ATLAS Users Manual*
[11] Martinez A, Aldegunde M, Seoane N, , Brown A, Barker J and Asenov A 2011 *IEEE Trans. Electron Devices* **58** 2209–2217
[12] Asenov A, JR W, DK F and Brown A 2002 *J. Comput. Electron.* **1** 503–513
[13] Aldegunde M, Martinez A and Asenov A 2011 *J. Appl. Phys.* **110** 094518
[14] Nagy D, Elmessary M, Aldegunde M, Valin R, Martinez A, Lindberg J, Dettmer W, Garcia-Loureiro A and Kalna K 2015 *IEEE Trans. Nanotechnol.* **14** 93–100
[15] Lindberg J, Aldegunde M, Nagy D, Dettmer W, Kalna K, Garcia-Loureiro A and Peric D 2014 *IEEE Trans. Electron Devices* **61** 423–429
[16] Jacoboni C and Lugli P 1989 *The Monte Carlo Method for Semiconductor Device Simulation* (New York: Springer-Verlag)
[17] Ferry D K 2000 *Semiconductor Transport* (New York: Taylor & Francis)
[18] Ridley B 1977 *J. Phys. C, Solid State Phys.* **10** 1589–1593
[19] Islam A, Benbakhti B and Kalna K 2011 *IEEE Trans. Nanotechnol.* **10** 1424–1432
[20] Islam A and Kalna K 2011 *Semicond. Sci. Technol.* **26** 055007
[21] Seoane N, Indalecio G, Comesana E, Garcia-Loureiro A, Aldegunde M and Kalna K 2013 *IEEE Electron Device Lett.* **34** 205–207
[22] Liu Y, Neophytou N, Klimeck G and Lundstrom 2008 *IEEE Trans. Electron Devices* **55** 1116–1122
[23] Gu J, Wu H, Liu Y, Neal T, Gordon R and Ye P 2012 *IEEE Electron Device Letters* **33** 967–969