Modeling of CMOS Devices and Circuits on Flexible Ultrathin Chips

Anastasios Vilouras, *Student Member, IEEE*, Hadi Heidari, *Member, IEEE*,
Shoubhik Gupta, *Student Member, IEEE*, and Ravinder Dahiya, *Senior Member, IEEE*

Abstract—The field of flexible electronics is rapidly evolving. The ultrathin chips are being used to address the high-performance requirements of many applications. However, simulation and prediction of changes in response of device/circuit due to bending induced stress remains a challenge as of lack of suitable compact models. This makes circuit designing for bendable electronics a difficult task. This paper presents advances in this direction, through compressive and tensile stress studies on transistors and simple circuits such as inverters with different channel lengths and orientations of transistors on ultrathin chips. Different designs of devices and circuits in a standard CMOS 0.18-μm technology were fabricated in two separated chips. The two fabricated chips were thinned down to 20 μm using standard dicing-before-grinding technique steps followed by post-CMOS processing to obtain sufficient bendability (20-mm bending radius, or 0.05% nominal strain). Electrical characterization was performed by packaging the thinned chip on a flexible substrate. Experimental results show change of carrier mobilities in respective transistors, and switching threshold voltage of the inverters during different bending conditions (maximum percentage change of 2% for compressive and 4% for tensile stress). To simulate these changes, a compact model, which is a combination of mathematical equations and extracted parameters from BSIM4, has been developed in Verilog-A and compiled into Cadence Virtuoso environment. The proposed model predicts the mobility variations and threshold voltage in compressive and tensile bending stress conditions and orientations, and shows an agreement with the experimental measurements (1% for compressive and 0.6% for tensile stress mismatch).

Index Terms—CAD, CMOS, device modeling, flexible electronics, thinning-down techniques, ultrathin silicon.

I. Introduction

MICROELECTRONICS has revolutionized our lives through fast communication and computing. Currently, the field is dominated by the silicon-based CMOS

electronics technology. The advances in CMOS electronics have been achieved mainly through high-performance and ultralarge-scale integration enabled by miniaturization [1]. The bendability or conformability is nowadays adding a new dimension to the electronics research. A range of alternative materials such as paper, plastic, or organic semiconductor are being explored for this purpose [2]–[6] as the brittle nature of Si precludes its use in flexible electronics. These new directions are reshaping electronics industry by enabling new solutions for emerging applications such as wearable systems, electronic skin, flexible displays, and Internet of things (IoT), and so on [7]–[10].

Bendability itself is not enough as many of these emerging applications require high performances to meet the fast communication and computation requirements. For example, the communication stack in IoT will be required to handle data in frequency bands up to ultrahigh frequencies (0.3–3 GHz) [11]. Similarly, the drive electronics in fully flexible or rollable displays require high current [12]. Achieving such performances, at par with conventional CMOS ICs, appears difficult with devices from materials such as organic semiconductors. As an example, recently reported organic semiconductor-based bendable microprocessor having 4000-transistor and 8-bit logic circuit operates at a clock frequency below 10 Hz [13]. This is four orders of magnitude (100 kHz) lower than Intel 4004 introduced in 1971. This modest performance is owing to the low inherent charge carrier mobility ($\sim$1 cm^2/V·s (maximum reported $\sim$43 cm^2/V·s [14]) cf. $\sim$1000 cm^2/V·s for single crystal Si) and the poor resolution of printing technologies typically used to fabricate the devices from organic semiconductors [15]. For these reasons, silicon and other high-mobility materials have caught the attention again and alternative ways of using them for flexible electronics, for example in new forms ranging from nanowires (NW) to ultrathin chips (UTCs) and so on are being explored [16]–[20].

One of the challenges for silicon-based flexible electronics (in fact for flexible electronics in general) is that the device response changes constructively of destructively as a result of bending induced stresses [21]–[23]. Mechanical stresses, either internally generated or externally applied, affect the carrier mobility, threshold voltage and so on and change the flatband voltage (V_{FB}) and the surface potential (Φ_S) [24]. For electronics design and to predict the response of circuits under different bending states it is important to understand these variations and present improved device models for future computer aided design (CAD) tools. The development of predictive,

TABLE I
COMPARISON OF SOME OF THE STATE-OF-THE-ART ULTRATHIN SILICON CIRCUITS UNDER STRESS

Circuit	Thickness [μm]	Radius of Curvature [mm]	Bending Test Structure	Orientation of channel	Carriers' Mobility μ_n | μ_p [cm²/V•s]	Size of Transistor nMOS | pMOS (W/L) [μm]	Thinning Process	Reference
Ring Oscillator	N/A	N/A	Externally applied package strain	Parallel and vertical n- and p-channels	N/A	4/0.24 | 10/0.24	N/A	[23]
Ring Oscillator	15	6.3, 15.8	Cylinder	N/A	N/A	0.1/0.02 | 0.1/0.02	UTB-SOI	[31]
Inverter	40	15	Cylinder	N/A	132 | 80	0.35/0.25 | 0.45/0.25	Sequential RIE	[21]
Inverter	30	N/A	Si microbumps and organic adhesive	N/A	1450 | 300	0.22/0.22 | 0.22/0.22	N/A	[22]
Inverter	1.7	0.085	Cylinder/Microscope cover slip	N/A	342 | 158 (x-strain) 396 | 134 (y-strain)	300/13 | 100/13	SOI wafer	[32]
Inverter	0.3	N/A	N/A	N/A	400 | 70	40/500 | 40/500	SOI wafer	[33]
Inverter	20	20, 40	Cylinder	0° and 90° layout in [100] wafer	1229 | 438	4/0.18 − 0.35 | 8/0.18 − 0.35	DBG	This work

Fig. 1. Illustration of ultrathin chips on flexible substrate under uniaxial tensile and compressive bending stress.

and accurate, models for flexible devices, and their compatibility with CAD tools will be a step change in bendable ICs. A few studies reported over last few years have theoretically analyzed some of the internal (e.g., process induces stresses, as in strained silicon) [25], [26], and external (e.g., uniaxial and biaxial bending) stresses and have presented models of devices [27]–[29]. In our previous work, we also reported the compact model of nMOS, its coding in Verilog-A and compilation in Cadence environment [30]. The model predicts the mobility and threshold-voltage variations under compressive and tensile bending stress (Fig. 1). However, as in conventional electronics this may change with device size. Furthermore, at circuit level the output may be different. For example, some of the transistors in a circuit may experience increase in mobility and others may have reduced mobility (depending on the type of stresses they experience) and the overall effect could be the cancellation of bending induced variations in the response. With this background, this paper presents advances in modeling and simulation of nMOS and pMOS transistors with different channel lengths and orientations and simple circuits such as inverters.

This paper is organized as follows: a brief state-of-the-art of the recently reported bendable devices and circuits, including strained silicon-based devices is presented in Section II. The description related to the layout design, process followed for ultrathin chip, and the characterization of bendable devices and circuits is given in Section III. A detailed discussion of the analytical model of the bendable n- and p-MOSFET as well as bendable inverter, along with model validation is presented in Section IV. Finally, the key outcomes are summarized in Section V.

II. STATE-OF-THE-ART

The fabrication and performance of the bendable silicon-based circuits along with their constitutive nMOS and pMOS response undergoing uniaxial and biaxial stress has been widely investigated in the past [21]–[23], [31]–[33]. Other techniques have also been explored with devices and circuits made from transferrable silicon nanomembranes or thin-film amorphous silicon [34], [35]. Some of the reported simple CMOS circuits on ultrathin silicon, including this paper, are summarized in Table I. Device level characterization complemented with theoretical modeling of bendable devices offers a great opportunity in the field of device modeling and simulation using CAD tools. However, despite the growing interest in the field of theoretical modeling of internally generated stresses, there are few papers on the effects of externally applied stresses, and the development of theoretical models for mechanically bendable silicon devices.

Stress engineering remains an important method to improve CMOS performance. Although, stress engineering has been extensively used in fabrication to enhance performance, the physical mechanisms behind change in carrier mobility (μ_e/μ_p) is yet to be fully understood. Starting with strained-induced changes in effective mass of carriers, a quantitative evaluation of stress-induced split of conduction band edge and experimental demonstration of changes in effective mass has been presented in [36]. There have been reports of analytical models defining the effect of stress on electronic transport of devices. The relation between normalized

variation in mobility as a function of stress, device orientation, and piezoresistive coefficient has been presented by Bradley *et al.* [37]. In another study, Dhar *et al.* [38] presented an electron mobility model of the strain effects resulting in variations in both effective mass and valley degeneration. Similar studies have been reported for the theoretical modeling of holes' mobility under variable stress [39]–[41]. Among them, Wang *et al.* [41] studied the energy-momentum curve to include arbitrary stress capabilities, and developed a model for quantum anisotropic transport of holes. Due to splitting of bands into subbands upon experiencing stress, the threshold voltage also experience shift from its unstressed value. Additionally, Lim *et al.* [42] compared the shift in the threshold voltage due to uniaxial and biaxial tensile stress.

As important as internally generated stresses are, which have been exploited to enhance the performance of silicon devices, studying the effect of externally applied bending stresses is also essential. However, there have been few works reported in this area, which have been also implemented using BSIM, PSP, and son on models. For example, Khagzar and Lueder [43] presented a static and dynamic model for amorphous silicon thin-film transistors implemented in SPICE. An exponential distribution of the deep and tail states in the energy gap has been used by taking also into account parasitic effects. A different way to perform simulations of bulk MOSFETs under uniaxial mechanical stress using BSIM3 stress-dependent parameters is presented in [27]. This paper extended and verified by ultrathin Si-chips experimental results in [28]. Mijalković [44] focused on the impact of different material properties on electrical characteristics and proposed a model, which considers the change of valence and conduction band edge energies during externally applied strain as an effective change in the semiconductor material. In another study, Alius *et al.* [45] included the effects of self-heating and stress in Verilog-A in order to enhance the library with the standard MOS model parameters (PSP 103.1) for IMS 0.5 μm CMOS. They modified the low- and high-field mobility, and threshold-voltage equations in order to include the contributions of bending and stress orientation versus the crystal orientation of the wafer.

Using the effective mobility and threshold-voltage parameters in the BSIM4 model, we have further extended the state-of-the-art and have developed the compact model in Verilog-A. The model is compatible with advanced standard CMOS technologies in Cadence Virtuoso. The proposed model predicts the mobility variations and threshold voltage in compressive and tensile bending stress conditions and orientations. Here, the model implemented for both the nMOS and pMOS devices using parameters extracted (e.g., oxide thickness, channel length modulation, saturation current, forward bias capacitance factor, and so on) from a standard CMOS 0.18 μm technology. Compiling the model during the schematic circuit simulation assists analog and digital designers to carry out circuit simulation under different bending stresses and orientation conditions. A detailed description of these models is presented in Section IV.

III. LAYOUT, FABRICATION, AND CHARACTERIZATION

To demonstrate the validity of the proposed models, we designed two chips in a standard 0.18 μm CMOS technology. The chips fabricated in an external foundry were thinned down to ∼20 μm using well-established grinding technique. The thinned chips were then integrated on flexible printed circuit boards (PCB) for further study involving characterization and comparison of simulation and experimental results as given in following sections.

A. Layout

In this paper, we have designed two chips for a wider analysis of chips under bending conditions. The first design includes nMOS and pMOS transistors with fixed channel width, but two different channel lengths (0.18 and 0.35 μm). Furthermore, these devices were designed to be fabricated along two different crystal axis i.e., 0° and 90° with respect to the wafer crystal orientation, to study the variations in carriers' mobility and threshold voltage and to include more sources of variations in our model. Channel width of nMOS and pMOS transistors are 4 and 8 μm, respectively, and the chip area is 0.9 mm × 0.8 mm. We have also designed a second chip to further advance our study of bendable compact device models toward their use in circuit simulation. This 0.9 mm × 0.788 mm size chip, shown in Fig. 2(c), includes inverter logic gates with different sizes and orientations.

B. Fabrication

The two chips discussed above were fabricated in a standard 0.18 μm CMOS technology in an external foundry using p-type wafers. The microphotograph of fabricated chips is shown in Fig. 2(a) and (b). As the thickness of chips after fabrication was about 480 μm, it is not possible to bend these chips. The bendability can be achieved by thinning down the bulk silicon from 500 μm to the ultrathin regime (<50 μm). The reduction in thickness can be achieved either by physically knocking off the material by grinding or by using chemically etching [18]. The thinning processes can be classified into chemical thinning [46], physical thinning [47], or physico-chemical thinning [48]. Among these, the physical thinning gives faster material removal rate and provides smooth thin silicon after stress relieving step. In particular, back grinding using abrasive particles and embedded grinders is widely used and established technique. To ensure maximum yield percentage, dicing before grinding (DBG) [47] has been used in this paper. The silicon die was partially diced by Half-Cut dicing tool along the dicing line, as shown in Fig. 2(d). Afterward, the front side of the precut die was placed on a back-grind protective tape, while the backside was grinded slowly with coarse and fine grinding. The chips separated automatically when the grinding level reached the dicing depth. In total ten fabricated chips were thinned down to 20-μm thickness. Five of these chips include differently sized and oriented nMOS and pMOS transistors, and five chips include inverter logic gates, as discussed in Section III-B. Following this step, the thinned chip was packaged over 120-μm polyimide-based flexible
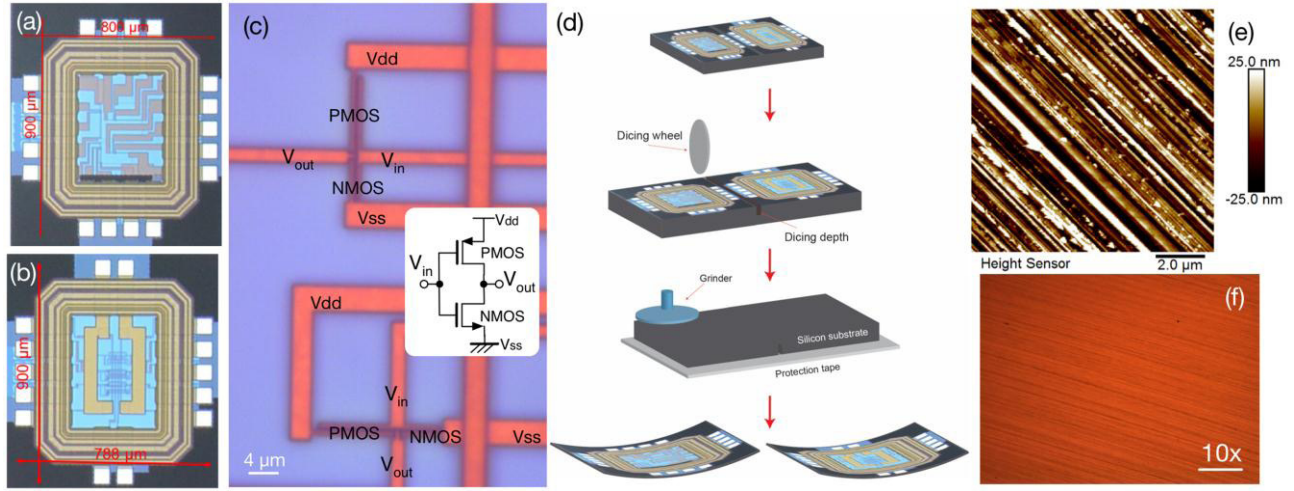
Fig. 2. Microphotograph of fabricated chips. (a) nMOS and pMOS transistors in different orientations. (b) Inverter logic gates. (c) Top view of the fabricated inverters using optical microscope (100 times). (d) Illustration of thinning process using DBG postprocessing technique. (e) AFM and break (f) microscopic images of backside thinned chip using DBG.
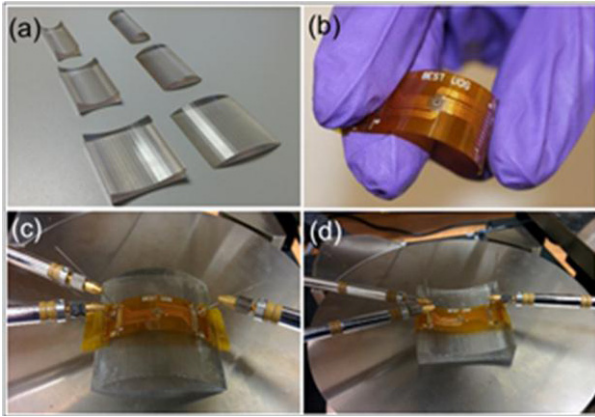

Fig. 3. (a) 3-D printed structures, (b) thin-chip on flexible PCB, and experimental setup for (c) tensile and (d) compressive mechanical bending stress.

PCB using ball to wedge wire bonding technique. The AFM and microscopic images of backside thinned chip are shown in Fig. 2(e) and (f), respectively.

C. Characterization and Experimental Results

The mechanical characterization of ultrathin Si dies is usually carried out using a three-point or four-point-bending setup [49], [50]. In this paper, due to the small size of the die we have used high-quality 3-D printed structures for compressive (downward direction) and tensile (upward direction) bending stress, as shown in Fig. 3(a). These structures have radii of curvature 20 and 40 mm. The nominal strain at the active area of the chip when is bent at these bending radii can be calculated using the following equation:

$$\varepsilon = \frac{d}{2R} \cdot 100\% \qquad (1)$$

where ε is the strain applied to the active area of the chip, d is the thickness of the sample, and R is the radius of bending.

Using (1), the percentage nominal strain on the surface of the chip was found to be 0.05% and 0.025% for 20 and 40 mm, respectively.

After packaging of thinned chips, the flexible PCBs were mounted on the 3-D printed structures, as is shown in Fig. 3(b)–(d). Using these structures, we evaluated the effects of bending on the transistors' mobility and threshold voltage. The output $(I_D - V_D)$ and transfer $(I_D - V_G)$ characteristics of 0.18-μm nMOS and pMOS in both channel orientation (0° and 90°) were measured at supply voltage $V_{DD} = 1.8$ V. In this paper, we have determined threshold voltage (V_{Th}) using the extrapolation in linear region method [51] from the I_D-V_{GS} characteristic at low V_{DS}. The charge carrier mobility of MOSFET devices were theoretically calculated using the output characteristic $(I_D - V_D)$ in the early saturation region. In this region, I_D is given by [52]

$$I_D = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{Th})^2 \qquad (2)$$

where C_{ox} is the oxide capacitance. For nMOS devices with 0.18- and 0.35-μm gate length C_{ox} values are ranging from 5.18–5.72 fF/μm^2 with typical value of 5.45 fF/μm^2. For pMOS devices with 0.18- and 0.35-μm gate length C_{ox} values are ranging from 9.43 to 10.21 fF/μm^2 with typical value of 9.82 fF/μm^2. The threshold voltage for planar devices with channel length of 0.35 μm was found to be 0.41 V for nMOS and −0.79 V for pMOS. For devices with channel length of 0.18 μm, the threshold voltage was found to be 0.6 V for nMOS and −0.5V for pMOS. The drain-current (I_D) depends both on the carrier's mobility (μ) and the threshold voltage (V_{Th}), and as reported by Lim *et al.* [42] shift in threshold voltage is observed upon experiencing strain. During characterization of devices with 0.35-μm channel length, we measured a change of ∼30 mV in threshold voltage as a result of bending.

The changes in charge carriers' mobility during compression and tension are given in Table II. The observed trend in Table II is in agreement with previously reported
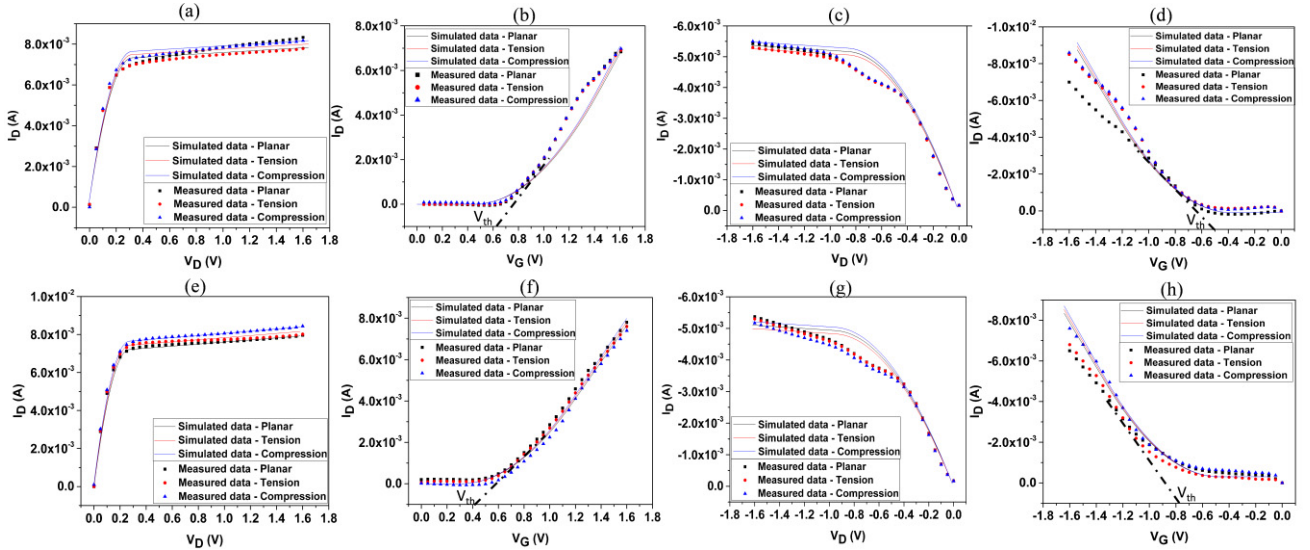
Fig. 4. Measured (symbols) and simulated (lines) transfer and output characteristic curves of nMOS and pMOS transistors in linear scale under planar, tensile, and compressive bending conditions. nMOS 0.18-μm transistor. (a) Output characteristic (I_D–V_D). (b) Transfer characteristics (I_D–V_G). pMOS 0.18-μm transistor. (c) Output characteristic (I_D–V_D). (d) Transfer characteristics (I_D–V_G). nMOS 0.35-μm transistor. (e) Output characteristic (I_D–V_D). (f) Transfer characteristics (I_D–V_G). pMOS 0.35-μm transistor. (g) Output characteristic (I_D–V_D). (h) Transfer characteristics (I_D–V_G).

TABLE II
CARRIERS' MOBILITIES UNDER DIFFERENT BENDING STRESSES

	Planar	Tension 40mm (0.025%)	Tension 20mm (0.05%)	Compression 40mm (0.025%)	Compression 20mm (0.05%)
NMOS	1229	1241	1251	1167	1159
PMOS	438	451	455	452	460

studies dealing with mobility change in strained conditions [21], [32], [53]. No measurable change was observed due to channel orientation. These results and the simulation results obtained using the proposed model under the same bending and orientation conditions are in agreement, as shown in Fig. 4(a)–(h).

The characteristics and performance of two inverters with the channel lengths of nMOS and pMOS of 0.18 and 0.35 μm in the same orientations were evaluated. Fig. 5(a)–(c) shows the switching behavior of inverter under planar, compressive, and tensile stress. We also analyzed the dc characteristic of the circuit in order to obtain the voltage transfer curve (VTC). A dc voltage sweep was applied to the input while keeping V_{DD} constant at 1.8 V and V_{SS} at 0 V. The midpoint voltage (V_M) was obtained from VTC at the point, where $V_{in} = V_{out}$. The obtained values of V_M, and small signal voltage gain (A_v) for the inverter with devices with channel length of 0.18 μm (Inverter 0.18 μm), and with device with channel length of 0.35 μm (Inverter 0.35 μm) are summarized in Table III. The relatively small change (<2.8%) in A_v confirms that the inverters presented in this paper can be used for applications requiring bendable logic circuits. During measurements, it was observed that channel orientation did not have significant effect on dc and ac response of the inverters. Finally, the input-high (V_{IH}) and input-low (V_{IL}) voltages
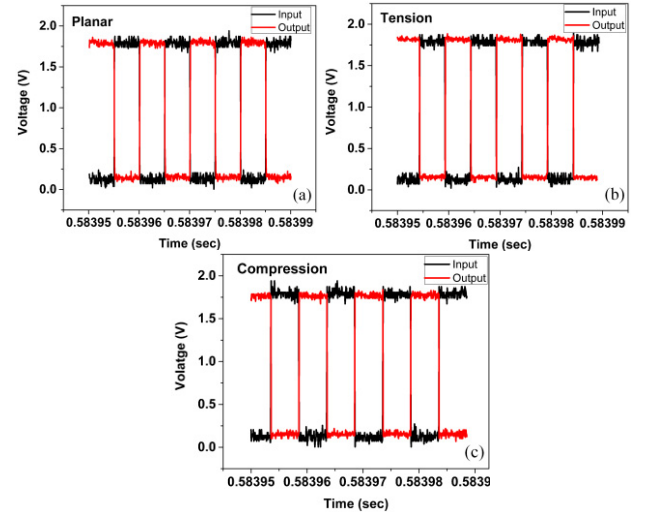

Fig. 5. Measurement results of inverter performance in (a) planar state, under (b) 40-mm (0.025%) tension and (b) 40-mm (0.025%) compression.

were calculated using following equations, and their values are given in Table III:

$$V_{IH} = V_M + \frac{V_{DD}}{2A_v} \qquad (3)$$

$$V_{IL} = V_M - \frac{V_{DD}}{2A_v}. \qquad (4)$$

It can be seen that the range between V_{IH} and V_{IL} is short in both compressive and tensile bending. This confirms that the inverters have high noise margin without compromising the performance.

IV. MODELING, SIMULATION, AND MODEL VALIDATION

Compact modeling aims to develop a numerically efficient representation of the device behavior under different modes

VALUES OF SWITCHING THRESHOLD, INPUT-HIGH, AND
INPUT-LOW VOLTAGE OF THE TWO INVERTERS

Inverter 0.18 μm	V_M (V)	A_V	V_{IH} (V)	V_{IL} (V)
Planar	1	6.09	1.148	0.852
Tension 40mm (0.025%)	1.03	5.92	1.182	0.878
Tension 20mm (0.05%)	1.04	5.97	1.191	0.889
Compression 40mm (0.025%)	0.99	6.01	1.139	0.840
Compression 20mm (0.05%)	0.98	5.98	1.131	0.829

Inverter 0.35 μm	V_M(V)	A_V	V_{IH} (V)	V_{IL} (V)
Planar	1	6.095	1.148	0.852
Tension 40mm (0.025%)	1.02	5.93	1.172	0.868
Tension 20mm (0.05%)	1.032	5.985	1.182	0.882
Compression 40mm (0.025%)	0.99	6.012	1.140	0.840
Compression 20mm (0.05%)	0.98	6.009	1.130	0.830

of operation. With flexible electronics, the compact device models should also include the effects of mechanical bending stress. Stress effects are not a new concept in compact modeling as the substrate-induced strain that has been exploited to improve device performances. Example includes Si/Si–Ge heterostructures, which create compressive biaxial tensile stress in the order of 700 MPa in the whole wafer substrate [54]. Likewise, layout-dependent stresses, like shallow trench isolation (STI) stress, can exert more than 750-MPa compressive stress in the vicinity area changing the charge carrier mobility of devices through the band structure modification, and thus alter the threshold voltage (V_{th}) depending the variation of the doping profile [55]. Existing MOS compact models typically consider such process and layout-induced stresses, but they do not consider the stress effects in flexible electronics in terms of bending radius or bending axis.

Externally applied stresses have a different impact on the effective carriers' mobility, and the threshold voltage with respect to other internally generated stresses discussed previously. The critical stress, at which most thin chips with thickness less than 20 μm break has been identified to be approximately 300 MPa [28]. The resistivity of silicon changes when it experiences stress, and the effect is termed as piezoresistive effect [56]. The mobility of carriers is also influenced by the crystal structure of material and the orientation of device channel [57]. In planar condition, the ellipsoidal shape of the six degenerated valleys of the conduction band structure of crystalline Si along [001], [010], and [100] crystal directions has two different curvatures and thus two effective masses [58]: longitudinal, $m_l = 0.97m_0$, and transversal, $m_t = 0.19m_0$, where m_0 is the free electron rest mass. The total effective mass can be written as, $m^* = [(1/6)((2/m_l) + (4/m_t))]^{-1} = 0.26 \cdot m_0$. As uniaxial or biaxial stress increases, electrons repopulate into the conduction subbands influencing the effective mass, m^*, and the momentum relaxation time, τ. Since the mobility of carrier is inversely proportional to its effective mass and popularly written as, $\mu = (|\vec{v}|/|\vec{E}|) = (q \cdot \tau)/(m_0 \cdot m^*)$, any change in effective mass changes the mobility and thus the resistivity. Along with mobility, the threshold voltage of MOSFETs also changes because of stress and eventually the drain current changes.

To understand and predict the behavior of bendable devices, it is essential to derive analytical equations describing their performance. Based on theoretical concepts described in Sections II and IV, the experimental results, and the use of mobility and threshold-voltage parameters from BSIM4, the modified drain-current, and threshold-voltage mathematical equations of MOSFETs under different bending conditions are [30], [45]

$$I_{D(\text{stress})} = I_{D_0}(1 \pm \Pi_{I_D} \cdot \sigma_{I_D}) \tag{5}$$

$$V_{\text{th(stress)}} = V_{\text{th}_0}(1 \pm \Pi_{V_{\text{th}}} \cdot \sigma_{V_{\text{th}}}) \tag{6}$$

where I_{D_0}, V_{th_0}, $I_{D(\text{stress})}$, and $V_{\text{th(stress)}}$ are the drain current and threshold voltage of the transistor under planar condition and the effective drain current and threshold voltage of the transistor under bending conditions, respectively. The piezoresistive coefficients proportional to the drain-current and threshold voltage, denoted as Π_{I_D} and $\Pi_{V_{\text{th}}}$ can be written as a function of channel orientation (θ) as

$$\Pi_{I_D} = 1 - 2 \times \pi_{I_D} \cdot \sin(\theta) \tag{7}$$

$$\Pi_{V_{\text{th}}} = 1 - 2 \times \pi_{V_{\text{th}}} \cdot \sin(\theta) \tag{8}$$

where π_{I_D} and $\pi_{V_{\text{th}}}$ are the contributions of the stress orientation versus the crystal orientation of the wafers. The proportional bending stress to drain-current and threshold voltage, are denoted as σ_{I_D} and $\sigma_{V_{\text{th}}}$, respectively. They can be written as a function of Young modulus (E), thickness of chip (h), radius of bending (R), and geometry variation factor (G), according to the following equations:

$$\sigma_{I_D} = E \cdot \frac{h}{2R} \cdot \Delta G_{I_{D0}} \left(1 + \frac{\Delta G_{I_D}}{G_{I_D}}\right) \tag{9}$$

$$\sigma_{V_{\text{th}}} = E \cdot \frac{h}{2R} \cdot \Delta G_{V_{th0}} \left(1 + \frac{\Delta G_{V_{\text{th}}}}{G_{V_{\text{th}}}}\right). \tag{10}$$

The extracted parameters and the above equations are implemented in Verilog-A to enable circuit simulation as in standard ASIC design process. Recently, we demonstrated the applicability of (3) and (4) in Verilog-A and compiled in the Cadence environment to model the behavior of n-MOSFET [30]. Further extending that study, the compact model here takes in to account the I–V characteristics of p-MOSFETs, which allows to simulate complementary digital gate circuits such as inverter. To validate our models, we compared the experimental data with the simulation results, as shown in Fig. 4(a)–(h).

To further advance this paper, both n- and p-MOSFETs with different or same channel orientation were used to model the behavior of inverters at different radii of bending curvature. Among the major logic gates, inverter is the most basic and widely studied circuit due to its low-power consumption, and relatively high speed. The externally applied bending stress causes changes of the switching behavior by shifting the midpoint voltage (V_M) of inverters, as is shown in Fig. 6(a)–(d). As discussed in Section III-C, the experimental value of midpoint voltage (V_M) for planar Inverter 0.18 μm and Inverter 0.35 μm was found 1 V, while the simulated values of V_M were 1.005 V and 1.01 V, respectively. The maximum experimental percentage differences of V_M during compressive and tensile stress were 2% and 4%, respectively, while the
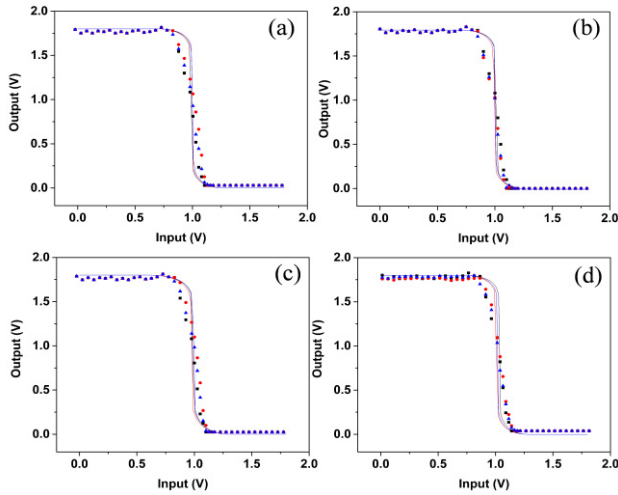
Fig. 6. Experimental and simulation data of voltage transfer curve of inverter with 0.18-μm channel length under (a) planar (black)/ tension 40 mm (0.025%) (red)/tension 20 mm (0.05%) (blue) and (b) planar (black)/compressi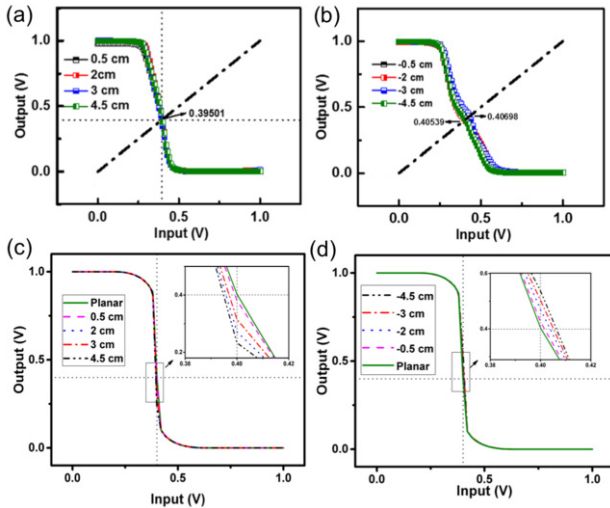on 40 mm (0.025%) (red)/compression 20 mm (0.05%) (blue). Experimental and simulation results of inverter with 0.35-μm channel length under (c) planar (black)/tension 40 mm (0.025%) (red)/tension 20 mm (0.05%) (blue) and (b) planar (black)/ compression 40 mm (0.025%) (red)/compression 20 mm (0.05%) (blue).

Fig. 7. Voltage transfer curve of flexible inverter at different bending (a) downward (tensile) and (b) upward (compressive) radii [21]. Simulation results based on the proposed compact model of inverter at different (c) downward and (d) upward radii corresponding to the characterizations shown in (a) and (b).

maximum percentage differences of V_M obtained from the simulations during compressive and tensile stress were found 1% and 3.4%, respectively.

To further validate our compact model, the simulated data have also been compared with other studies on flexible logic gates reported in literature. Fig. 7(a) and (b) show the experimental voltage transfer curve reported in [21], and the Fig. 7(c) and (d) show the simulated data using our models. In order to simulate the VTC of the inverter under different strained conditions, we extracted the parameters of nMOS and pMOS, such as channel width and length, threshold voltage, and mobility from [21] and we implemented them

in our proposed models for nMOS and pMOS in Verilog-A. Following that, we designed and simulated an inverting circuit in Cadence Virtuoso environment with the same operating voltage as in [21] using the modeled nMOS and pMOS transistors. In this paper, the reported midpoint voltage (V_M) for planar, downward (tensile), and upward (compressive) bending conditions was 0.40293 V, 0.39501 V, and 0.40539–0.40698 V, respectively. Our model validates the reported behavior of the inverter by showing similar V_M values, i.e., 0.4 V for planar, and similar decreases and increases in V_M for tensile and compressive bending stresses.

V. CONCLUSION AND OUTLOOK

With growing interest in flexible electronics, the need for device modeling and improved CAD tools has been felt. However, the area has been scarcely researched. The work presented in this paper will fill the gap with the improved models to predict the behavior of devices on bendable substrates. To capture many sources of variations and complexity the ultrathin chips developed with different channel length (L = 0.18 μm, 0.35 μm) and orientation ($\theta = 0°$, 90°) have been used. With bending, the change in mobility and shift in the threshold voltage has been observed. To simulate this change, a compact and Cadence-friendly model has been developed. The model itself is a combination of mathematical equations, and extracted parameters from the BSIM4, written in Verilog-A. The maximum observed percentage difference in drain-current during bending for nMOS was found ∼5.9%, while the percentage difference of simulated results was 4.4%. For pMOS it was found ∼2.4%, while the simulated difference was 2.17%. In the case of inverter, a maximum percentage difference of 2% for compressive and 4% for tensile stress was observed for the experimental midpoint voltage (V_M). The simulated results of V_M showed a close matching with percentage difference of 1% and 3.4%, respectively. Overall, this paper advances the state-of-the-art in the bendable silicon technology, by presenting high-performance devices and circuits with reliable functioning complemented with a compact model, which can simulate their response.

Future work will involve thinning down the chips with more complex circuits and integrating with sensors in a bendable ultrathin chip and further validate the proposed compact model. This provides the possibility of integration of ultrathin chips with sensors and readout circuits on a polymeric substrate, which could find an attractive application in electronic skin and flexible electronics.

REFERENCES

[1] G. E. Moore, "Cramming more components onto integrated circuits," *Readings Comput. Archit.*, vol. 56, no. 8, pp. 114–117, 2000.
[2] H. Sirringhaus, "25th anniversary article: Organic field-effect transistors: The path beyond amorphous silicon," *Adv. Mater.*, vol. 26, no. 9, pp. 1319–1335, 2014.
[3] A. Nathan *et al.*, "Flexible electronics: The next ubiquitous platform," *Proc. IEEE*, vol. 100, pp. 1486–1517, May 2012.
[4] T. Sekitani and T. Someya, "Human-friendly organic integrated circuits," *Mater. Today*, vol. 14, no. 9, pp. 398–407, Sep. 2011.
[5] E. O. Polat *et al.*, "Synthesis of large area graphene for high performance in flexible optoelectronic devices," *Sci. Rep.*, vol. 5, Nov. 2015, Art. no. 16744.

[6] D. Tobjörk and R. Österbacka, "Paper electronics," *Adv. Mater.*, vol. 23, no. 17, pp. 1935–1961, May 2011

[7] S. Bauer *et al.*, "25th anniversary article: A soft future: From robots and sensor skin to energy harvesters," *Adv. Mater.*, vol. 26, no. 1, pp. 149–162, 2014.

[8] D.-H. Kim *et al.*, "Epidermal electronics," *Science*, vol. 333, no. 6044, pp. 838–843, 2011.

[9] R. Dahiya *et al.*, "Developing electronic skin with the sense of touch," *Inf. Display*, vol. 31, no. 4, pp. 2–6, 2015.

[10] H. Heidari *et al.*, "CMOS vertical Hall magnetic sensors on flexible substrate," *IEEE Sensors J.*, vol. 16, no. 24, pp. 8736–8743, Dec. 2016.

[11] H. Sundmaeker *et al.*, "Vision and challenges for realising the Internet of Things," in *Cluster of European Research Projects on the Internet of Things*. Brussels, Belgium: European Commision, 2010.

[12] X. Duan, "Nanowire thin-film transistors: A new avenue to high-performance macroelectronics," *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 3056–3062, Nov. 2008.

[13] K. Myny *et al.*, "An 8b organic microprocessor on plastic foil," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2011, pp. 322–323.

[14] Y. Yuan *et al.*, "Ultra-high mobility transparent organic thin film transistors grown by an off-centre spin-coating method," *Nature Commun.*, vol. 5, Jan. 2014, Art. no. 94.

[15] S. Khan *et al.*, "Technologies for printing sensors and electronics over large flexible substrates: A review," *IEEE Sensors J.*, vol. 15, no. 6, pp. 3164–3185, Jun. 2015.

[16] K. Balasundaram *et al.*, "Porosity control in metal-assisted chemical etching of degenerately doped silicon nanowires," *Nanotechnology*, vol. 23, no. 30, p. 305304, Aug. 2012.

[17] K. Takei *et al.*, "Nanowire active-matrix circuitry for low-voltage macroscale artificial skin," *Nature Mater.*, vol. 9, no. 10, pp. 821–826, 2010.

[18] R. S. Dahiya and S. Gennaro, "Bendable ultra-thin chips on flexible foils," *IEEE Sensors J.*, vol. 13, no. 10, pp. 4030–4037, Oct. 2013.

[19] S. Khan *et al.*, "Flexible MISFET devices from transfer printed Si microwires and spray coating," *IEEE J. Electron Devices Soc.*, vol. 4, no. 4, pp. 189–196, Jul. 2016.

[20] W. Christiaens *et al.*, "UTCP: A novel polyimide-based ultra-thin chip packaging technology," *IEEE Trans. Compon. Packag. Technol.*, vol. 33, no. 4, pp. 754–760, Dec. 2010.

[21] G. T. Sevilla *et al.*, "High performance high-*k*/metal gate complementary metal oxide semiconductor circuit element on flexible silicon," *Appl. Phys. Lett.*, vol. 108, no. 9, p. 094102, 2016.

[22] H. Kino *et al.*, "Investigation of local bending stress effect on complementary metal–oxide–semiconductor characteristics in thinned Si chip for chip-to-wafer three-dimensional integration," *Jpn. J. Appl. Phys.*, vol. 52, no. 4S, p. 04CB11, 2013.

[23] F. Yuan, C.-F. Huang, M.-H. Yu, and C. W. Liu, "Performance enhancement of ring oscillators and transimpedance amplifiers by package strain," *IEEE Trans. Electron Devices*, vol. 53, no. 4, pp. 724–729, Apr. 2006.

[24] W. Zhang and J. G. Fossum, "On the threshold voltage of strained-Si-Si$_{1-x}$Ge$_x$ MOSFETs," *IEEE Trans. Electron Devices*, vol. 52, no. 2, pp. 263–268, Feb. 2006.

[25] H. M. Nayfeh, J. L. Hoyt, and D. A. Antoniadis, "A physically based analytical model for the threshold voltage of strained-Si n-MOSFETs," *IEEE Trans. Electron Devices*, vol. 51, no. 12, pp. 2069–2072, Dec. 2004.

[26] Y. Tan, X. Li, L. Tian, and Z. Yu, "Analytical electron-mobility model for arbitrarily stressed silicon," *IEEE Trans. Electron Devices*, vol. 55, no. 6, pp. 1386–1390, Jun. 2008.

[27] N. Wacker, H. Richter, M.-U. Hassan, H. Rempp, and J. N. Burghartz, "Compact modeling of CMOS transistors under variable uniaxial stress," *Solid-State Electron.*, vol. 57, no. 1, pp. 52–60, 2011.

[28] N. Wacker *et al.*, "Stress analysis of ultra-thin silicon chip-on-foil electronic assembly under bending," *Semicond. Sci. Technol.*, vol. 29, no. 9, p. 095007, 2014.

[29] S. Gupta *et al.*, "Device modelling for bendable piezoelectric FET-based touch sensing system," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 12, pp. 2200–2208, Dec. 2016.

[30] H. Heidari *et al.*, "Device modelling of bendable MOS transistors," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2016, pp. 1358–1361.

[31] D. Shahrjerdi *et al.*, "Mechanically flexible nanoscale silicon integrated circuits powered by photovoltaic energy harvesters," *Solid-State Electron.*, vol. 117, pp. 117–122, Mar. 2016.

[32] D.-H. Kim *et al.*, "Stretchable and foldable silicon integrated circuits," *Science*, vol. 320, no. 5875, pp. 507–511, 2008.

[33] S.-W. Hwang *et al.*, "Biodegradable elastomers and silicon nanomembranes/nanoribbons for stretchable, transient electronics, and biosensors," *Nano Lett.*, vol. 15, no. 5, pp. 2801–2808, 2015.

[34] H. Zhou *et al.*, "Fast flexible electronics with strained silicon nanomembranes," *Sci. Rep.*, vol. 3, p. 1291, Feb. 2013.

[35] M. Cho *et al.*, "Capacitance-voltage characteristics of Si and Ge nanomembrane based flexible metal-oxide-semiconductor devices under bending conditions," *Appl. Phys. Lett.*, vol. 108, p. 233505, May 2016.

[36] K. Uchida *et al.*, "Physical mechanisms of electron mobility enhancement in uniaxial stressed MOSFETs and impact of uniaxial stress engineering in ballistic regime," in *IEEE IEDM Dig*, Dec. 2005, pp. 129–132.

[37] A. T. Bradley, R. C. Jaeger, J. C. Suhling, and K. J. O'Connor, "Piezoresistive characteristics of short-channel MOSFETs on (100) silicon," *IEEE Trans. Electron Devices*, vol. 48, no. 9, pp. 2009–2015, Sep. 2001.

[38] S. Dhar, H. Kosina, V. Palankovski, S. E. Ungersboeck, and S. Selberherr, "Electron mobility model for strained-Si devices," *IEEE Trans. Electron Devices*, vol. 52, no. 4, pp. 527–533, Apr. 2005.

[39] Z. Shuo, "Impacts of additive uniaxial strain on hole mobility in bulk Si and strained-Si p-MOSFETs," *J. Semicond.*, vol. 30, no. 10, p. 104001, 2009.

[40] B. Obradovic *et al.*, "A physically-based analytic model for stress-induced hole mobility enhancement," *J. Comput. Electron.*, vol. 3, no. 3, pp. 161–164, 2004.

[41] E. Wang *et al.*, "Quantum mechanical calculation of hole mobility in silicon inversion layers under arbitrary stress," in *IEEE IEDM Tech. Dig.*, Dec. 2004, pp. 147–150.

[42] J.-S. Lim, S. E. Thompson, and J. G. Fossum, "Comparison of threshold-voltage shifts for uniaxial and biaxial tensile-stressed n-MOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 11, pp. 731–733, Nov. 2004.

[43] K. Khakzar and E. H. Lueder, "Modeling of amorphous-silicon thin-film transistors for circuit simulations with SPICE," *IEEE Trans. Electron Devices*, vol. 39, no. 6, pp. 1428–1434, Jun. 1992.

[44] S. Mijalković, "MOS compact modelling for flexible electronics," in *Ultra-thin Chip Technology and Applications*. New York, NY, USA: Springer, 2011, pp. 259–270.

[45] H. Alius *et al.*, "A new MOSFET model for the simulation of circuits under mechanical stress," presented at the MOS-AK Workshop, London, U.K., 2014.

[46] K. Biswas and S. Kal, "Etch characteristics of KOH, TMAH and dual doped TMAH for bulk micromachining of silicon," *Microelectron. J.*, vol. 37, no. 6, pp. 519–525, 2006.

[47] H. Yoo, "Dicing before grinding process for preparation of semiconductor," U.S. Patent 13 279 400, Oct. 28, 2011.

[48] A. Hu *et al.*, "Apparatus and method for polishing a flat surface using a belted polishing pad," U.S. Patent 6 059 643, Feb. 21, 2000.

[49] S. Endler *et al.*, "Mechanical characterisation of ultra-thin chips," in *Proc. Semiconductor Conf. Dresden (SCD)*, Sep. 2011, pp. 1–4.

[50] S. Schoenfelder *et al.*, "Mechanical characterisation and modelling of thin chips," in *Ultra-Thin Chip Technology and Applications*. Springer Science & Business Media, 2011, pp. 195–218.

[51] D. K. Schroder, *Semiconductor Material and Device Characterization*. Hoboken, NJ, USA: Wiley, 2006.

[52] Y. Tsividis and C. McAndrew, *Operation and Modeling of the MOS Transistor*. London, U.K.: Oxford Univ. Press, 2011.

[53] M. Fischetti *et al.*, "Six-band k·p calculation of the hole mobility in silicon inversion layers: Dependence on surface orientation, strain, and silicon thickness," *J. Appl. Phys.*, vol. 94, no. 2, pp. 1079–1095, 2003.

[54] J. Richter *et al.*, "Piezoresistance of silicon and strained Si$_{0.9}$Ge$_{0.1}$," *Sens. Actuators A, Phys.*, vol. 123, pp. 388–396, Sep. 2005.

[55] M. Miyamoto, H. Ohta, Y. Kumagai, Y. Sonobe, K. Ishibashi, and Y. Tainaka, "Impact of reducing STI-induced stress on layout dependence of MOSFET characteristics," *IEEE Trans. Electron Devices*, vol. 51, no. 3, pp. 440–443, Mar. 2004.

[56] C. S. Smith, "Piezoresistance effect in germanium and silicon," *Phys. Rev.*, vol. 94, no. 1, p. 42, 1954.

[57] M. Chu *et al.*, "Comparison between high-field piezoresistance coefficients of Si metal-oxide-semiconductor field-effect transistors and bulk Si under uniaxial and biaxial stress," *J. Appl. Phys.*, vol. 103, p. 3704, Mar. 2008.

[58] G. L. Bir, *Symmetry and Strain-Induced Effects in Semiconductors*, vol. 624. New York, NY, USA: Wiley, 1974.

Anastasios Vilouras (S'16) received the B.Sc. Degree in physics from the Aristotle University of Thessaloniki, Thessaloniki, Greece in 2014, and the M.Sc. degree in bioelectronics and biosensors from The University of Edinburgh, Edinburgh, U.K., in 2015. He is currently pursuing the Ph.D. degree with the Bendable Electronics and Sensing Technologies Group, University of Glasgow, Glasgow, U.K., with a focus on CMOS-based bendable sensors for chemical and biochemical measurements.

Shoubhik Gupta (S'15) received the B.Tech. degree in electrical engineering from IIT Kanpur, Kanpur, India, in 2014, with a focus on quantum electronics and theoretical modeling of electronic devices. He is currently pursuing the Ph.D. degree with the Bendable Electronics and Sensing Technologies Group, Electronics and Nanoscale Division, University of Glasgow, Glasgow, U.K.

His current research interests include ultrathin silicon chips and its application in flexible electronics, especially electronic skin.

Hadi Heidari (S'11–M'15) received the Ph.D. degree in microelectronics from the University of Pavia, Italy.

He is currently Lecturer in electronics and nanoscale engineering with the University of Glasgow, Glasgow, U.K. and Glasgow College UESTC. His research interests are focused on the magnetoelectronics, device modelling, CMOS sensors, sensor interfaces, ultra-thin chips and flexible electronics. He is IEEE Sensors Council Young Professional Representative.

Ravinder Dahiya (S'05–M'09–SM'12) received the Ph.D. degree from the Italian Institute of Technology, Genoa, Italy.

He is currently Reader in electronics and nanoscale engineering with the University of Glasgow, Glasgow, U.K. He has authored over 150 papers, four books (including 3 at various stages of publication), and nine patents (including 7 submitted). His current research interests include flexible and printable electronics, tactile sensing, electronic skin, and robotics.