UNIVERSIDADE FEDERAL DE SANTA CATARINA
ENGENHARIA ELÉTRICA

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CMOS MOBILITY-COMPENSATED TIME REFERENCE FOR CRYSTAL REPLACEMENT

Florianópolis

2015

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Dissertação submetida ao Programa de P ós-graduação em engenharia elétrica da Universidade Federal de Santa Catarina para a obtenção do grau de Mestre em engenharia Elétrica .
Advisor: Prof. Dr. Marcio Cherem Schneider

Florianópolis

2015

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Zomagboguelou, Agossou Wilfried
CMOS MOBILITY-COMPENSATED TIME REFERENCE FOR CRYSTAL REPLACEMENT / Agossou Wilfried Zomagboguelou ; orientador, Marcio Cherem Schneider - Florianópolis, SC, 2015.
p.

Dissertação (mestrado) - Universidade Federal de Santa Catarina, Centro Tecnológico. Programa de Pós-Graduação em Engenharia Elétrica.

Inclui referências

1. Engenharia Elétrica. 2. Relaxation Oscillator independent with Process, Voltage and Temeperature. 3. Time reference . 4. Zero-Vt MOSFET as resistor. 5. Current mode Schmitt trigger. I. Cherem Schneider, Marcio . II. Universidade Federal de Santa Catarina. Programa de Pós Graduação em Engenharia Elétrica. III. Título.

Agossou Wilfried Zomagboguelou

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Esta Dissertação foi julgada aprovada para a obtenção do Título de "Mestre", e aprovada em sua forma final pelo Programa de Pós-graduação em engenharia elétrica.

Florianópolis, 30 de November 2015.

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Ce Master thesis est dédié á mon frere Victorien Zomagboguelou.

ACKNOWLEDGEMENTS

Firstly, I would like to express my sincere gratitude to my advisor Prof. Marcio Schneider for the continuous support of my master degree study and related research, for his patience, motivation, and immense knowledge. His guidance helped me in all the time of research and writing of this master thesis. And also my sincere gratitude to Prof. Carlos Galup for the opportunity given to join LCI (Laboratório de Circuito Integrado) and his mentoring in this master thesis. I could not have imagined having a better advisor and mentor for my master degree study. And my sincere thanks to CNPQ Conselho Nacional de Desenvolvimento Científico e Tecnológico for the scholarship, and to MOSIS for fabricate my circuit through multi-project wafers (MPW).

My sincere thanks also go to Prof. Adroaldo Raizer, who gave access to the research facilities (MagLab-UFSC), and Dr. Arun Kumar Sinha, for the discussions about analog environment tool and support. I feel that without their precious support, it would not be possible to conduct this research work.

I would also like to thank Luiz Alberto Pasini Melek, and Dr. Marcio Bender for their advise in layout design and submitting design to the MOSIS. Also I would like to thanks, Ms. Nazide and to all the students working in LCI with their name listed as: Mr. Daniel Novak, Mr. Yuri, Mr. Anselmo, Mr. Fernando and Mr. Jefferson.

RESUMO

Apesar da existência de muitas alternativas para geração de base de tempo, não há ainda uma referência de tempo totalmente integrável que possa oferecer simultaneamente alta precisão, baixa potência e custo de produção reduzido; portanto, não há uma referência de tempo ideal capaz de ter performance melhor do que os osciladores a quartzo disponíveis no mercado. O objetivo principal desse trabalho é de tentar encontrar uma solução em tecnologia CMOS de uma referência de tempo capaz de substituir osciladores a quartzo na frequência de 32 kHz. Isso implica em projetar um oscilador de baixa potência, alta precisão e que seja pouco sensível as variações de processo, de tensão e de temperatura. Os elementos básicos do oscilador de relaxação deste trabalho são um transistor zero-Vt que opera como resistor e uma fonte de corrente especifica de transistor zero-Vt. Foi desenvolvido também um Schmitt trigger com entrada de corrente e uma fonte de corrente controlada por tensão capaz de acompanhar a variação de corrente devido as variações de processo, tensão e temperatura. As medidas do oscilador fabricados mostraram uma variacao de $+/-30ppm/^{\circ}C$ na faixa de temperatura de -20°C ate 80°C e uma variação menor do que $+/-500ppm/V$ para tensão de alimentação entre 0.7 V e 1.8 V. As medidas da estabilidade em frequência mostraram uma variação de $+/-500ppm$ para estabilidade de longo termo, e um jitter de 2 nanoseconds para estabilidade curto termo.

Palavras-chave: Time reference, Relaxation oscillator, Low-power design, Current comparator, Schmitt trigger, Zero-Vt transistor.

ABSTRACT

Despite many alternatives for time generation, no CMOS fully-integrated time reference offers simultaneously high accuracy, low power consumption, and low cost, and, thus, no ideal time reference suitable to replace the xtal-clock is available. The main aim of this work is to contribute to find a solution to this problem, which is to realize a low-cost, low-power CMOS time reference circuit that is insensitive to PVT (Process, Voltage, and Temperature) variations. The basic element of the relaxation oscillator is a zero-Vt MOSFET that operates as a resistor and a current source which tracks the specific current of the zero-Vt transistor. The design presented here uses a current mode Schmitt trigger and a voltage controlled current source, which can track the current variation due to PVT variations. The frequency of oscillation, proportional to the mobility, is compensated by the thermal voltage. The proposed time reference, fabricated in a 180 nm CMOS technology has been designed for 32 kHz. Test and measurement results show a variation of $+/-30ppm/^{\circ}C$ from -20°C to 80°C, and less than $+/-500ppm/V$ for a variation of the supply voltage between 0.7 V to 1.8 V. As regards frequency stability, measurements have shown a variation less than $+/-500ppm$ for long term stability, and an rms jitter of 2 nanoseconds (66 ppm) for short term stability.

Keywords: Time reference, Relaxation oscillator, Low-power design, Current comparator, Schmitt trigger, Zero-Vt transistor.

CONTENTS

1 INTRODUCTION

Many services running on modern digital telecommunications networks require accurate synchronization for correct operation [1], [2]. For example, if switches do not operate with the same clock rates, then slips will occur and will degrade performance. Also telecommunications networks rely on the use of highly accurate primary reference clocks, which are distributed over wide networks using synchronization links and synchronization supply units. Time reference is also used as a clock in watch when the time is precise and stable or in RF sleep mode in cellular [3] as shown in Fig.1, when the time reference is stable and consume low power.

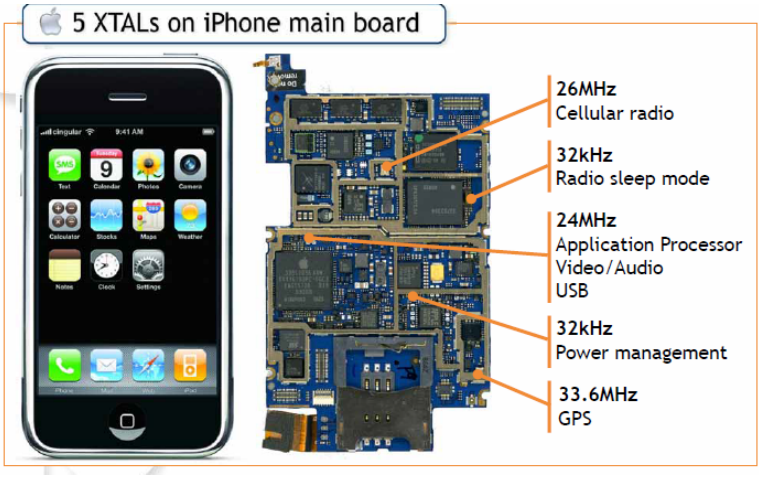

Figure 1 – Example of use of xtal oscillator in cell phone [3]

In this work we will present methods used to generate a time reference. We will design a time reference in CMOS technology that can be suitable to replace the most common time reference i.e., the crystal oscillator, in some applications where only stability and precision are required.

1.1 MOTIVATION

In the beginning of 1968 the concept of integrated time reference were explored [4], when oscillators of type ”Wien-bridge” as the one shown in Fig. 2 were presented.

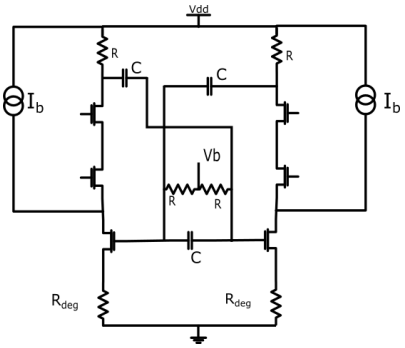

Figure 2 – Wien Bridge Oscillator [4]

That circuit was used as a time reference, in the case where precision, stability and accuracy of the clock does not matter. Ever since, a circuit that can be integrated and can replace the crystal oscillator has been searched. One of the main motivation of this search is that the crystal oscillator cannot be a part of the integrated circuit i.e. it has to be external, as shown in Fig.3.

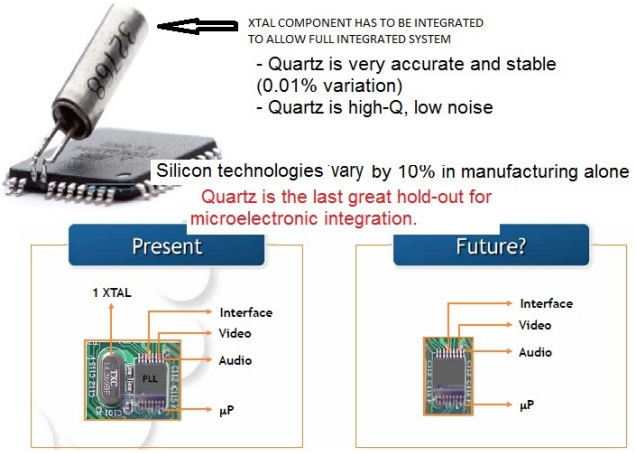

Figure 3 – Crystal Oscillator

1.2 CRYSTAL OSCILLATOR

The crystal resonator is the most important component of a crystal oscillator and the quartz crystal is the heart of it. A quartz crystal is an anisotropic crystal of silicon dioxide. The crystal structure consists of two pyramidal ends and is hexagonal in cross-section. Fig. 4 illustrates the physical structure of a quartz crystal.

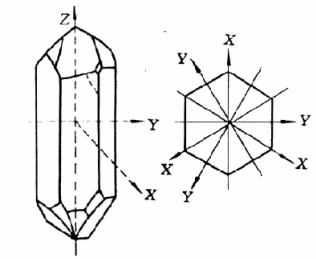

Figure 4 – Cuts of the crystal resonator [5]

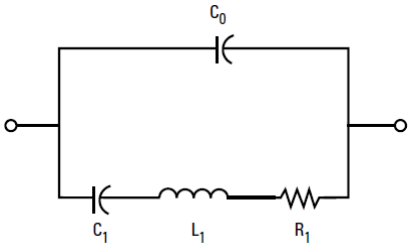

Figure 5 – Equivalent circuit of the crystal oscillator [6]

The equivalent circuit of the crystal oscillator, shown in Fig.5, provides the link between the physical property of the crystal and the area of application, the oscillator [7]. The physical constants of the crystal determine the equivalent values of R_1, C_1, L_1, and C_0. R_1 is a result of bulk losses, C_1, the motional capacitance, L_1 is determined by the mass, and C_0 is made up of the electrodes, and the leads [8]. When operated far off resonance, the structure is simply a capacitor C_0 but, at the precise resonant frequency the circuit becomes a capacitor and resistor in parallel, as shown in Fig.6. The reactance of the crystal approaches zero at the point of series resonance [8], and reaches a maximum at the anti-resonant frequency f_A, as Fig.6 shows.

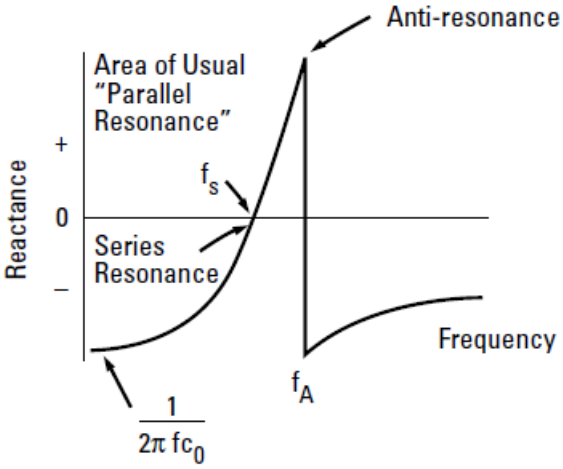

Figure 6 – The reactance of the crystal varies with the frequency of operation near resonance [5]

An area typically chosen for the operation of the oscillator is either near the series resonance or at the more inductive area of parallel resonance. The series resonant circuit Fig.6 utilizes the characteristics of the crystal where the reactance is just slightly inductive. Series capacitance is then added to obtain a tuned circuit [8]. The series capacitor is typically adjustable so that the phase of the feedback can be changed slightly, thus fine tuning the oscillator frequency. The parallel resonant mode adds capacitor in parallel or across the crystal Fig.7. This circuit typically operates in the upper part of the reactance curve, hence the crystal reactance is more inductive.

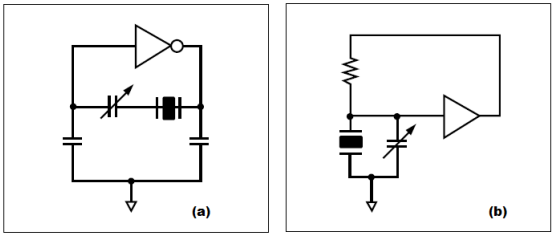

Figure 7 – (a) Series resonant oscillator (b) Parellel resonant circuit [5]

1.3 PHYSICAL AND ELECTRICAL FACTORS AFFECTING CRYSTAL OSCILLATOR FREQUENCY STABILITY AND ACCURACY

A small piece of quartz material is obtained by cutting the crystal at specific angles to the various axes. The choice of axis and angles determine the physical and electrical parameters of the resonator. The frequency, or rate of vibration, is determined by the cut, size, and shape of the resonator.

- Temperature
  Temperature is a significant factor which affects the frequency of resonators. Different crystal cuts have a different frequency-temperature characteristic as shown in Fig. 8. AT, XY, DT, CT, and BT represent different crystal cut methods. The primary frequency determining factor for the AT, XY, DT, CT, and BT cut is thickness since they vibrate in the thickness shear mode. The precision with which the thickness is controlled determines the frequency variation from crystal to crystal.

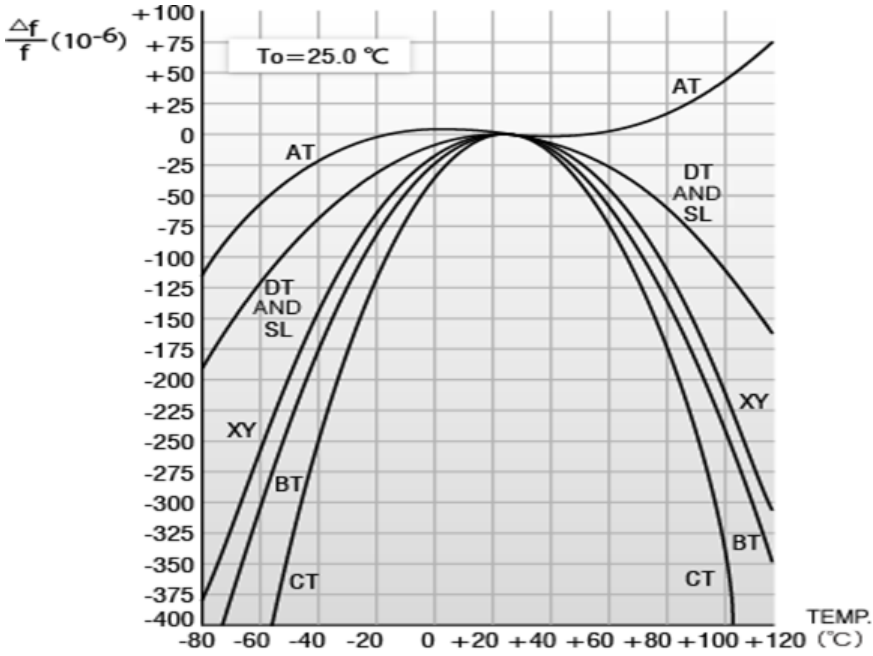

Figure 8 – Crystal with temperature variation at different fabrication process [5]

Figure 9 – Aging of crystal resonator over time [6]

- Aging
  The crystal resonator frequency will change according to the operation time. This physical phenomenon is termed as aging. It should be noted that although the plot in Fig.9 is monotonic, this is not always the case and the aging rate can reverse sign over time.

- Drive Level
  In a precise crystal resonator, the oscillator frequency also relies on the crystal electric current or drive level. The equation is:

$$\frac{\delta f}{f} = k.i^2 \tag{1.1}$$

  Here, "i" is the alternating-current which flows through the crystal, k is a constant which is dependent on the crystal, and $\frac{\delta f}{f}$ is the relative variation of the vibration frequency. When the drive electric current is high, the aging property and long-term frequency stability will be worse. But when the drive level is too small, the noise electric current

may be relatively high compared to the crystal electric current, and this will cause the worse short-term frequency stability.

- Retrace
  When power is removed from an oscillator for several hours, then re-applied on it again, the frequency of this oscillator will stabilize at a slightly different value. This frequency variation error is called retrace error. It usually occurs for twenty four or more hours off-time followed by a warm-up time which is enough to complete thermal equilibrium.

- Power supply noise
  The power supply noise is one of the sources of oscillator phase noise; especially, for ring-based voltage-controlled oscillators, it is the dominant noise source. Such noise typically appears as steps or impulses on the power supply of the oscillator, and it affects both frequency and phase, causing cycle-to-cycle jitter.

1.4 AVAILABLE TECHNIQUES TO REPLACE XTAL-OSCILLATORS

1.4.1 MEMS oscillator

Quartz crystal resonators are excited at their resonance frequency by an electrical oscillator circuit [9],[10],[11]. Their operation depends on the piezoelectric properties of a material that cannot be integrated in IC technology. Over the years, a lot of research has been done on the development of silicon MEMS-based (Micro Electro-Mechanical Systems-based) resonators with the aim of replacing quartz crystals. MEMS technology involves many of the processes used by the integrated circuit technology such as lithography, deposition, etching, etc. [10]. This technology has been applied in sensors such as accelerometer, gyroscopes, microphones, etc. MEMS resonators are micro-machined structures that can vibrate at their resonance frequency, if an external excitation is applied to them. The resonance property of such structures was first researched in 1967 [11], when a resonant gate transistor was presented as a micro-machined integrated time reference [10]. This excitation can be of the electrostatic, piezoelectric or electromagnetic type [12], [13]. MEMS resonators have faced many challenges in delivering a cost-effective and reliable solution that could compete commercially with quartz crystals. The major challenges included packaging, vibration and shock sensitivity, temperature drift and long term stability [14]. In recent years various commercial products have been introduced by two start-up

companies: Discera and SiTime. Today, MEMS-based time references produced by these companies are more compact than their quartz competitors and are more cost-effective due to the mass production allowed by the use of IC technology. However, their level of jitter (phase noise) is not (yet) low enough. Because of the special processing required by MEMS technology, a MEMS resonator has to be manufactured on a die which is separated from the die that holds the electronic circuitry exciting and controlling it [12], [13], [14]. Furthermore, the mass of a MEMS resonator is small, being on the order of $10^{(-14)} - 10^{(-11)}$ kg, which means that its resonance frequency and quality factor will be affected by any gas molecules surrounding it [15]. This means that silicon MEMS resonators should preferably be operated in vacuum, which is the reason why they have been fabricated within silicon cavities [12], [13],[14],[15] and wire-bonded to a CMOS die [16].

1.4.2 LC oscillator

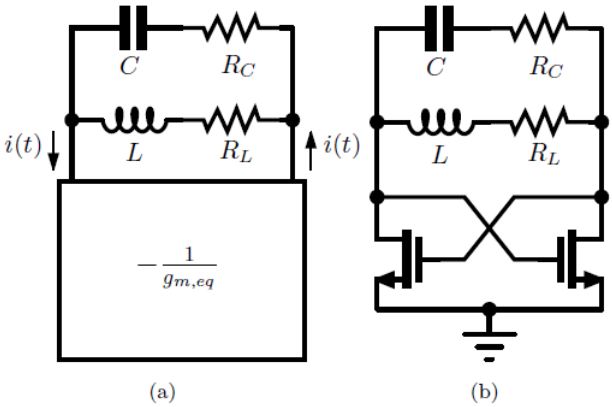

Figure 10 – (a) Generic LC Oscillator Block diagram (b) Typical CMOS implementation (bias not shown)

Another class of commercially available time references is the LC oscillator [17]. Such oscillator operate at the resonance frequency of an LC tank [18] and have been widely used in VCO that produce frequencies in the RF range [19]. The basic form of a typical integrated LC oscillator is shown in Fig.10. A parallel resonant tank is connected in parallel to an active circuit, whose equivalent resistance is negative and equal to $-\frac{1}{g_{m_{eq}}}$. The active circuit

compensates for the losses of the tank and sustains the oscillation. In the tank, both the coil of inductance L and the capacitor of capacitance C exhibit finite losses, modeled respectively by series resistances R_L and R_C. The frequency of oscillation is given by equation.(1.2),

$$f = f_0.\sqrt{\frac{1-\frac{C.R_L^2}{L}}{1-\frac{C.R_C^2}{L}}} = f_0\frac{\sqrt{1-\frac{1}{Q_L^2}}}{\sqrt{1-\frac{1}{Q_C^2}}} \tag{1.2}$$

where $Q_L = \frac{2.\pi.f.L}{R_L}$ and $Q_C = \frac{1}{2.\pi.L.R_C}$ are the inductor and the capacitor quality factor, respectively. f_0 is the tank natural resonant frequency given by equation.(1.3):

$$f_0 = \frac{1}{2.\pi.\sqrt{LC}} \tag{1.3}$$

The LC oscillator is usually used as a time reference. In this case, special attention needs to be paid to the stability of the output frequency as a function of process, temperature and voltage variations. As shown in Fig10, an LC oscillator is based on passive elements such as inductors and capacitors as well as active elements, i.e. transistors. Therefore, such an oscillator can be made in a standard CMOS process. The first steps towards commercializing self-referenced LC oscillators were taken at Mobius Microsystems, a fabless company founded in 2004 with the aim of developing all-silicon frequency sources that replace quartz crystal oscillators. The goal of Mobius Microsystems was to produce a monolithic free-running RF LC oscillator that did not require the frequency synthesizers used in MEMS time references. This was to avoid the effect of multiplication on the output frequency jitter. These efforts resulted in oscillators with output frequency ranges from 12 to 25 MHz and with initial target applications such as wire-line data communication, e.g., USB. An LC oscillator based on the resonant tank shown in Fig.10 not only suffers from frequency deviation due to the losses, but also due to variations in the absolute values of the passive elements due to process and temperature.

1.4.3 Relaxation oscillator with positive feedback

Oscillators with positive feedback as the one shown in Fig.11, have to satisfy the Barkhausen criteria which can be stated as follows:

If A is the gain of the amplifying element and $\beta(jw)$ is the transfer function of the feedback path, the circuit will sustain steady oscillations only at frequencies for which:

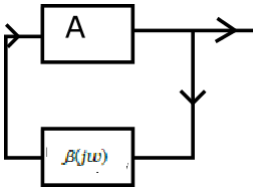

Figure 11 – Amplifier in close loop

- The loop gain is equal to unity in absolute magnitude, that is, $|A.\beta| = 1$
- The phase shift around the loop is zero or an integer multiple of 2π.

Barkhausen's criteria is a necessary condition for oscillation but not a sufficient condition: some circuits satisfy the criteria but do not oscillate.

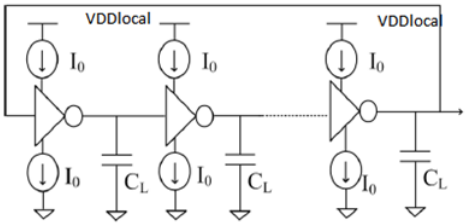

Figure 12 – Current-starved ring oscillator

In the case of the ring oscillator such as the one in Fig.12, the oscillation frequency depends on the delay τ_d in each stage and on the number of stages $\boldsymbol{m}$ in the ring oscillator, according to

$$f_d = \frac{1}{2.m.\tau_d} \tag{1.4}$$

In order to use a ring oscillator as time reference, some form of compensation of supply voltage variations must be employed locally. The use of a low drop-out (LDO) regulator which provides a stable local output voltage is one of the options [20].

In Fig.13 we have one example of ring oscillator with a specific circuit to generate a stable local supply voltage.

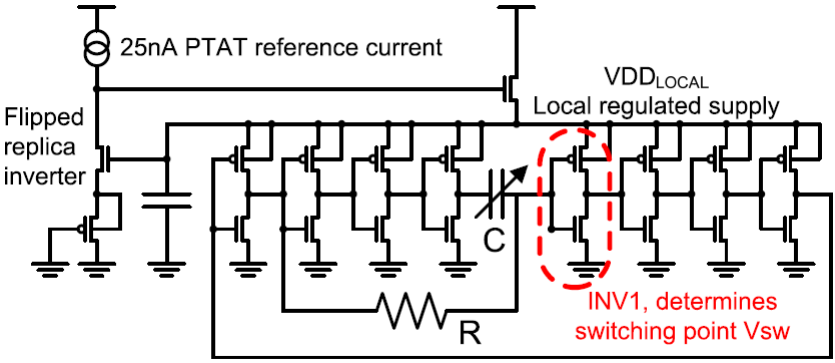

Figure 13 – RC + Ring Oscillator [20]

The period of oscillation is given by,

$$T_0 = RC.ln(\frac{(1+K_{SW})(2-K_{SW})}{K_{SW}(1-K_{SW})}) \tag{1.5}$$

where $K_{SW} = V_{SW}/V_{dd}$. V_{SW} is the switching point of the inverter one (INV1). In [20] the implemented RC oscillator consists of an RC network, and an inverting gain element from a resistor terminal to a capacitor terminal and another inverting gain element from the common resistor/capacitor terminal back to the resistor terminal. For high gain, the two inverting elements consist of three and five inverters, respectively. A simple regulator, consisting of an NMOS voltage follower and a replica inverter that is flipped and biased by a reference current, produces a local regulated supply for the inverters. The flipped replica of inverter is formed by a PMOS in diode configuration and a NMOS in saturation. Then the voltage at the drain of the NMOS in the flipped inverter is equal to, $V_{D_{flipped}} \approx \frac{I_{PTAT}}{V_E.L}$, where V_E is the early voltage which is linear function of the temperature. Then to make the voltage at the drain of the NMOS in the flipped inverter independent with temperature variation, the author polarized the flipped inverter with a PTAT current. Consequently the voltage at the drain of the NMOS in the flipped inverter is a voltage reference independent with temperature and using a NMOS voltage follower allows to bias the oscillator with local supply voltage. This local supply is well below the standard core voltage for the technology 65 nm, used in this relaxation oscillator. It is designed an RC circuit together with a Ring oscillator, where the oscillation period is defined by the period of the ring oscillator plus the period of the RC oscillator. But this topology is designed for the period of

the RC oscillator greater than the period of the ring oscillator. The threshold voltage V_{SW} is used as switch point of the charge and discharge of the capacitor. One disadvantage of this topology is that the switch point of the inverter depends strongly on process, supply voltage and temperature variations.

1.4.4 Relaxation oscillator using comparators

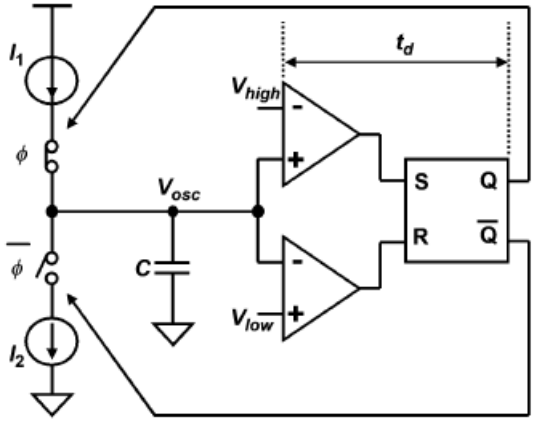

Figure 14 – Relaxation oscillator with 2 comparators [21]

Usually the design of a relaxation oscillator requires a comparator. Generally two comparators are used to set the high and the low voltage levels in the capacitor as shown in Fig. 14 and described in [21]. Sometimes, a single comparator is employed [22]; in this case, the discharge time is very small because a switch is used to discharge the capacitor [22]. The use of a flip-flop in the output to generate the output frequency, which will two times the charging time on the capacitor, is necessary.

The comparator offset affects directly the period of oscillation in Fig. 15. Then a compensated offset RC relaxation oscillator [23], as the one shown in Fig. 16 can be used. Fig. 17 shows another form of comparison, which is reported in [24]. In this case, the drain voltage of M2, is low when V_C is less than V_{ref}. When V_C becomes higher than V_{ref}, the drain voltage of M2 goes up and changes the output of the buffer to high level, which makes the switch to turn ON. The capacitor voltage becomes low, and as a result, the value of the drain of M2 becomes low.

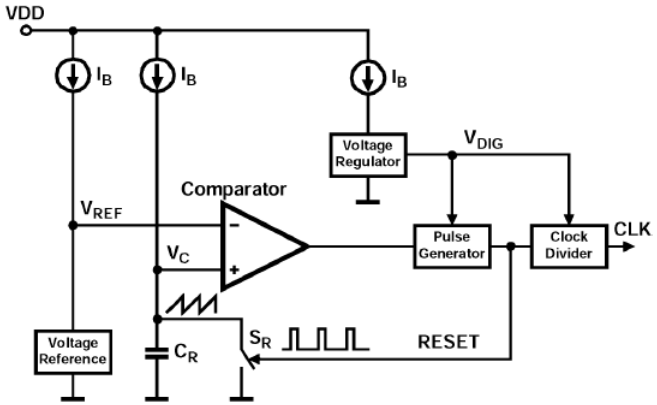

Figure 15 – Relaxation Oscillator using one comparator only [22]

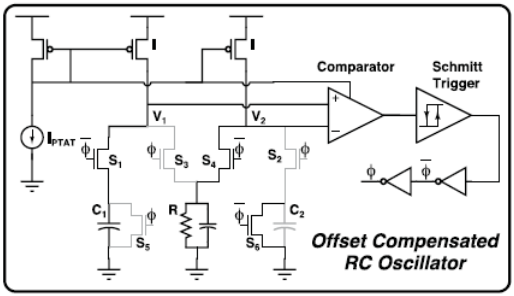

Figure 16 – Relaxation oscillator with one comparator and compensated Offset [23]

1.4.5 Mobility-based relaxation oscillator

Some authors have designed the period of oscillation directly proportional to the mobility. In [25], a class of low-power time references based on the mobility of MOS transistors has been introduced (Fig.18). Such reference dissipates micro watts of power and achieve inaccuracies of the order of a few percent.

The implementation described in [25] is targeted to wireless sensor networks. It has an output frequency of 150 kHz, dissipates 42.6 μW from

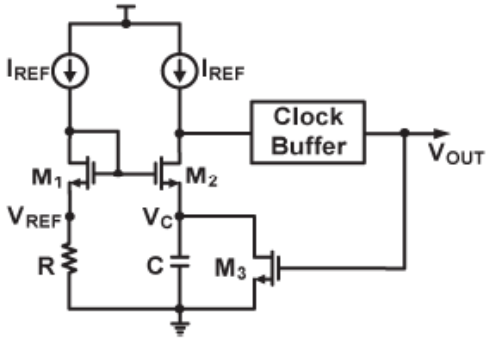

Figure 17 – Current mode relaxation oscillator [24]

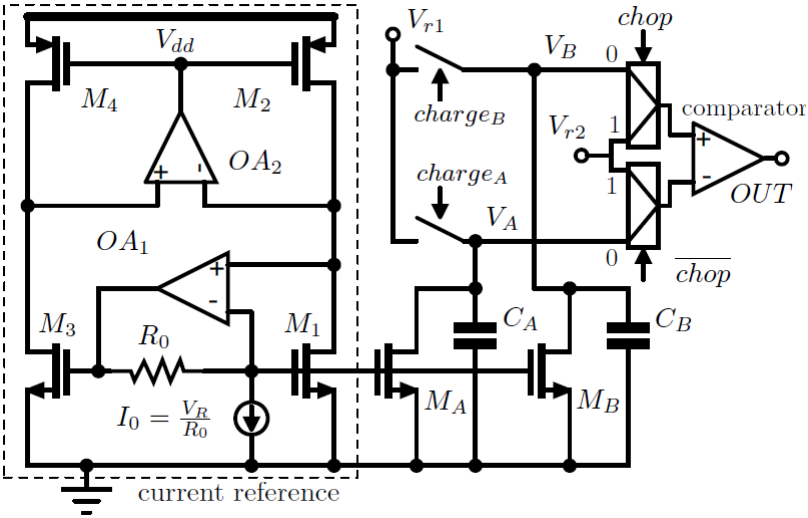

Figure 18 – Mobility-based time reference [25]

a 1.2 V supply, and is fabricated in a 65 nm standard CMOS process. For a temperature range of -55 °C to 125 °C, the reference achieves an output frequency stability of +/-0.5% when trimmed at two temperature points. With a single trim its inaccuracy is 2.7%. The schematic of the oscillator in [25] is shown in Fig.18. This schematic shows a current reference, comparator, and a switch system to charge and discharge the capacitors. Two levels of voltage reference are also represented which are V_{r1} and V_{r2}. C_A and C_B are

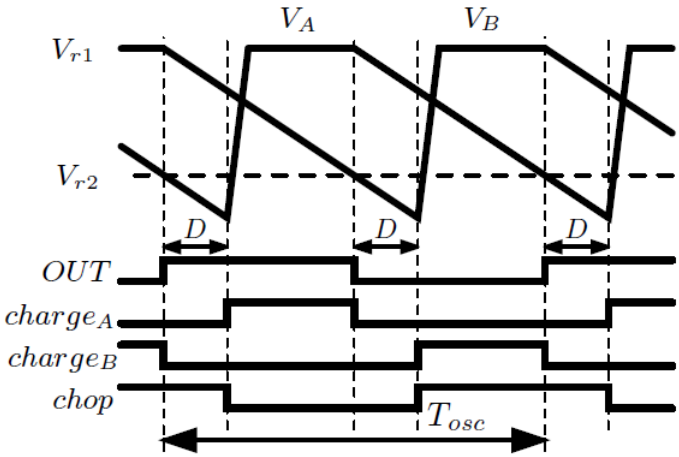

Figure 19 – Waveform of the mobility-based time reference [25]

alternatively pre-charged to V_{r1} and then linearly discharged by M_A and M_B. When the voltage on the discharging capacitor drops below V_{r2}, the output of the comparator switches and the linear discharge of the other capacitor starts immediately Fig.19. The author of this relaxation oscillator considers that the mobility is less sensitive with temperature variation at high doping level.

Another mobility-based oscillator [22] has been implemented in a 0.35 μm CMOS, and this oscillator has an output frequency of 3.3 kHz, and consumes 11 nW from 1 V supply voltage and a accuracy greater than 1% with temperature variation (-20 °C to 80 °C). In [22] the author considers that the mobility is inversely proportional to temperature variation, which could be compensated by the thermal voltage. But how does the mobility varies in term of the temperature in MOSFET devices ?

In the next section we present some theory about mobility dependence on temperature and, finally, we show the simulated behavior of the mobility with respect to temperature in the IBM 180 nm technology.

1.5 MOBILITY IN MOSFETS

Mobility was one of the most studied MOSFET parameters in the early 1980s. Fig.20 shows a summary of different models commonly used in electrical simulators for mobility in silicon.

The mobility can be written [26] as :

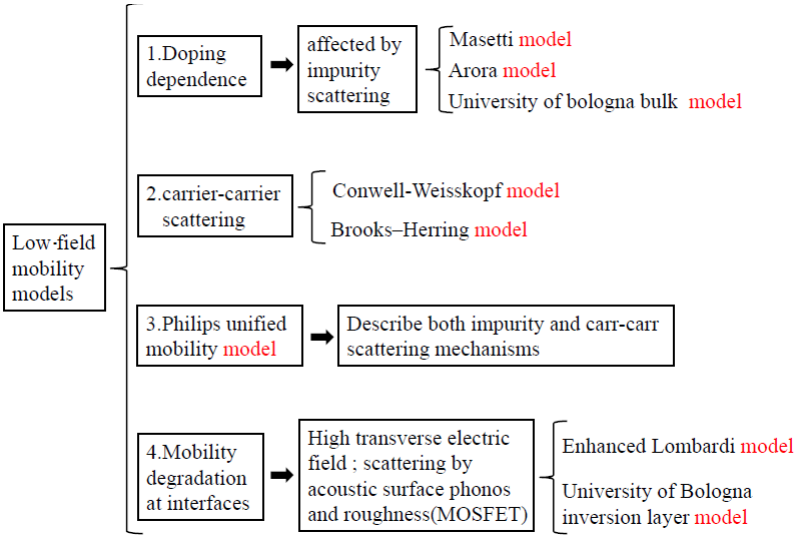

Figure 20 – Differents models of the mobility used in electrical simulator

$$\frac{1}{\mu} = \frac{1}{\mu_{ac}} + \frac{1}{\mu_b} + \frac{1}{\mu_c} + \frac{1}{\mu_{sr}} \tag{1.6}$$

where, μ_{ac} is the acoustic phonon mobility, μ_b is the bulk mobility, μ_c is the Coulomb mobility, and μ_{sr} is the surface roughness mobility. In MOSFET devices, surface mobility is defined by the effects of all 4 types of mobility in equation(1.6) which, in turn, are dependent of the MOSFET bias voltage. Bulk mobility is the main factor which defines the surface mobility when the devices operates at high temperatures (200 K ¡ T ¡ 370 K) [27] and low field.

1.5.1 Some theory on mobility with temperature variation

The temperature is one of the main factors which affects the mobility [26]. In [26], [28], [29] and [30], theory about the mobility variation with temperature is described. A diagram that describes this theory is summarized in Fig. 21. Now, let us briefly present some comments about the mobility components.

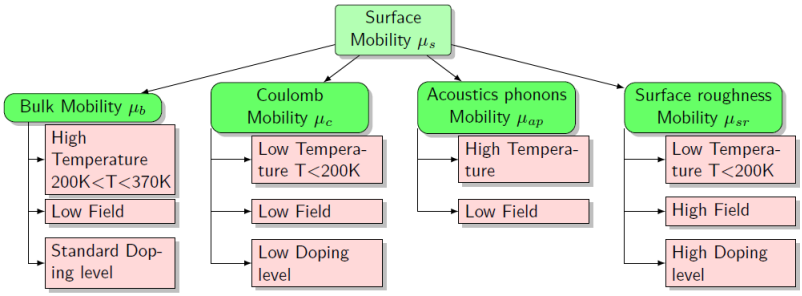

Figure 21 – Predominant factor on surface mobility in different conditions

1.5.2 Coulomb mobility $\mu_{coulomb}$

In [27], the Coulomb mobility in term of the temperature variation is :

$$\mu_{coulomb} \propto T^{\gamma} \int n(z)dz \tag{1.7}$$

where γ is close to 1, n(z) is the charge in the inversion layer, T is the absolute temperature, and 'z' is the thickness of the inversion layer.

In strong inversion and high temperature (T¿200 K) , $\mu_{coulomb}$ is very high and does not contribute to the total mobility.

1.5.3 Acoustic phonon mobility μ_{ac}

μ_{ac} is modeled as [26], [28] and [29]:

$$\mu_{ac} = \frac{K}{T} \tag{1.8}$$

where K is a constant defined by the technological parameters a elementary charge, and the thickness of the inversion layer.

1.5.4 Surface roughness mobility μ_{sr}

At low temperature and high electric field μ_{sr} degrades the mobility in the inversion layer and causes a negative transconductance. At high temperature the surface roughness mobility does not affect the surface mobility [26],

[28], [29], [30].

1.5.5 Bulk mobility μ_b

Fig. 21 summarizes the dominant effect in terms of the temperature and the doping level. In [30] the bulk mobility is modeled in function of the doping level and the temperature as,

$$\mu_b(N_A,T) \approx \mu_0 + \frac{\mu_{max} - \mu_0}{1 + (\frac{N_A}{C_r})^{\alpha}} \tag{1.9}$$

and

$$\mu_{max} = \mu_0 (\frac{T}{T_0})^{-\gamma} \tag{1.10}$$

C_r and C_l are constants N_A is the doping level of the bulk, μ_0 is the mobility at T_0, γ is a coefficient dependent of the doping level. Some authors [30] report that $1.5 < \gamma < 2.3$.

From equation.1.9, we can see that, at high doping level, the bulk mobility will be less sensitive to temperature variation. At low doping level the bulk mobility is more or less CTAT i.e., complementary to absolute temperature. In Fig.22 and Fig.23, we can see that at low doping level the mobility decreases linearly when the temperature increases, and is less dependent with process variation. At high doping level the mobility is more or less constant with respect to temperature variation but depends heavily on doping .

1.5.6 Simulation of mobility with respect to temperature variation

To measure carrier mobility in the inversion layer of the MOSFETs, large devices are commonly chosen to avoid short-channel and narrow-width effects. In this work we have used $W = 3\mu m$, $L = 20X3\mu m$ device to extract the mobility from simulation in 180 nm, which corresponds to the dimensions of the MOSFET used as a resistor in the voltage-controlled current source of the time reference. Generally two methods could be used to extract the mobility in MOSFET namely the DC current method and the split CV methods. The split CV method can overestimate the mobility due to parasite capacitances in MOSFET. We have used the drain current method to extract the mobility.

The DC current method allows the extraction of the mobility in strong

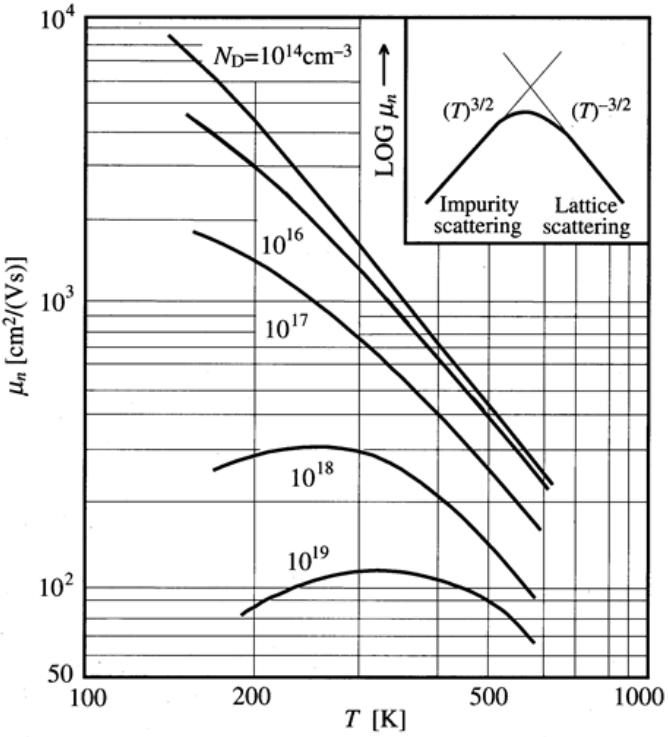

Figure 22 – : Bulk mobility variation with temperature at different doping levels

inversion. This mobility is called a conductivity mobility and is related to the channel conductance. The circuit for measuring the channel conductance is shown in Fig.24.

$$g_{ds} = \frac{\Delta I_d}{\Delta V_{ds}} \tag{1.11}$$

Using the UCCM from ACM [31] (Advanced Compact Model, see appendix for details) of MOSFET: yields:

$$V_p - V_{sb} = \phi_t(\sqrt{1+i_f} - 2 + ln(\sqrt{1+i_f} - 1)) \tag{1.12}$$

In strong inversion the logarithm term can be neglected; thus, equation(1.12) can be written as

$$V_p - V_{sb} \approx \phi_t \sqrt{(i_f)}. \tag{1.13}$$

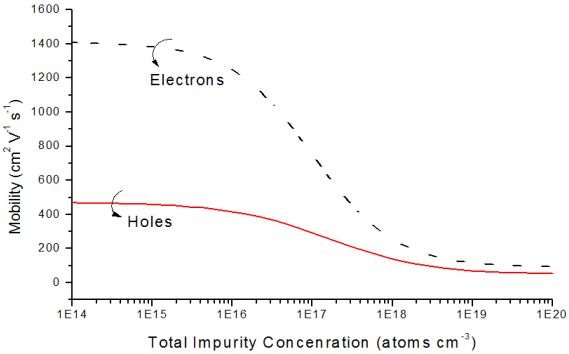

Figure 23 – Bulk mobility versus doping level

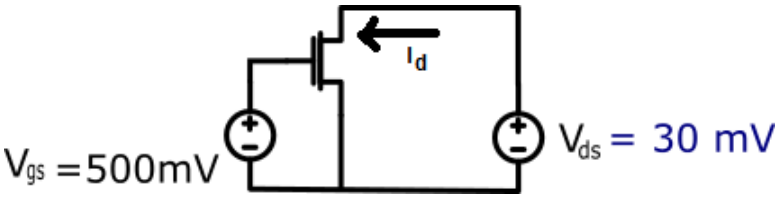

Figure 24 – Set-up to extract the mobility with respect to temperature variation for the zero-Vt MOSFET in 180 nm

The same simplification holds for the drain terminal, i.e.

$$V_p - V_{db} \approx \phi_t \sqrt{(i_r)} \tag{1.14}$$

The drain source voltage is,

$$\frac{V_{ds}}{\phi_t} \approx (\sqrt{(i_f)} - \sqrt{(i_r)}) \approx (\frac{i_f - i_r}{2\sqrt{i_f}}) \tag{1.15}$$

the last approximation holds since for $V_{ds} \approx 30mV$ we have $i_f \approx i_r$. Since $V_{sb} = 0$, the substitution of equation.(1.15) into equation.(1.13) yields

$$\frac{V_p.V_{ds}}{I_D} = \frac{\phi_t^2}{2.I_S} = \frac{L}{\mu_n.C_{ox}.W.n} \tag{1.16}$$

Which can be writen as,

$$\mu_n = \frac{L.I_D}{C_{ox}.W.V_p.V_{ds}.n}. \tag{1.17}$$

where $V_p = \frac{V_{gs}-V_{th}}{n}$ is called the pinch-off voltage. V_{th} is the threshold voltage as defined in appendix A. To extract the mobility and the threshold voltage we have fixed the value of $V_{ds} = 30mV$, we have plotted I_d vs V_{gs} for different temperature. For $V_{gs} = 500mV$, we have extrapolated a line for this point and tangent to I_d vs V_{gs} with a specific temperature. The point of intersection of this line and x-axis determine the threshold voltage at the specific temperature. From the curve I_d vs V_{gs} one can get the value of I_d which corresponds to $V_{gs} = 500mV$. After getting this threshold voltage and the value of the current using equation.(1.17), one can determine the mobility. In zero-Vt devices the threshold voltage is near zero but it will vary with the temperature. Fig.25 shows the simulated normalized mobility variation and the threshold voltage variation with respect to temperature variation. The normalized mobility variation is defined for the value of the mobility at temperature $T_0 = 27$ °C as reference.

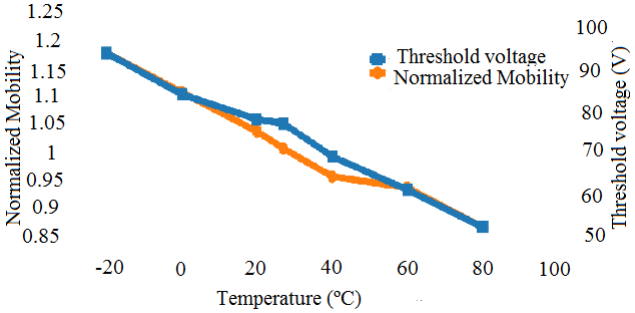

Figure 25 – Simulation result of the mobility with temperature in zero-Vt MOSFET device

1.6 COMPARISON BETWEEN TECHNIQUES AVAILABLE TO GENERATE TIME REFERENCES

This chapter provided an overview of various types of silicon-based time references and some theory about mobility variation with respect to temperature variation.

Table 1 – Comparison between techniques to generate time references

Oscillator	MEMS Oscillator [12]	LC Oscillator [32]	Crystal oscillator [33]	Relax oscillator [25]
Location	In-package	On-chip	On-Board	On-chip
F-Variation	$+/-10ppm$	$+/-100ppm$	$+/-1ppm/200ppm$	$+/-10000ppm$
Frequency-F	200KHz-200 MHz	GHz	1 KHz- 100 MHz	1KHz-10MHz
CURRENT(IQ)	5mA - 50 mA	10 mA	100 nA - 50 mA	10 nA - 100 μA
IQ/F	High @ KHz Medium @ MHz	Low	Medium @KHz High @ MHz	Low
COST	HIGH	Low	Medium	Low
Temp	-40°C to 85 °C	-40°C to 125°C	-20°C to 60 °C	-40°C to 100 °C

In the first part we presented the state-of-the-art of techniques available to generate time reference. These included crystal oscillator, MEMS-resonator-based oscillators, LC oscillators, RC harmonic oscillators, RC relaxation oscillators, ring oscillators and finally electron-mobility-based oscillators. Each approach has its own specific advantages and disadvantages. To make a comparison, it is helpful to summarize the performance characteristics for each type of time reference. One of the difficulties in providing a complete and fair comparison between published time references is that often insufficient data on their performance over process and temperature has been provided. There are references in which the performance of a single device has been reported as a measure of stability, which does not allow a fair comparison with references for which more samples have been characterized. From the previously described types of silicon-based time references, a performance summary of those with the most complete results is presented in Table 1. MEMS-resonator-based oscillators and LC oscillators have been commercialized, and thus their reported performance characteristics are at production level. The characteristics of other topologies are obtained mainly from publications. It can be seen that MEMS-based oscillators achieve the best accuracy over the widest temperature range. Their form factor has also been shrunk and they are physically smaller than crystal oscillators. However, their major disadvantage is the need for special MEMS processing. This requires a two-die solution, in which the MEMS resonator is wire bonded to another CMOS chip. The power consumption of MEMS oscillators is comparable to that of LC oscillators and is larger than the other types. Apart from the MEMS-based oscillators and crystal oscillator, all the other time references in Table. 1 are standard CMOS compatible, which is a great advantage as far as manufacturing, packaging costs and complexity are considered. Among these, LC oscillators achieve the best accuracy over process and temperature, as well as the best jitter performance. However, their power consumption is higher than that of the other oscillators and their temperature range is the narrowest. MEMS-based and LC-based oscillators are the only solutions in lit-

erature that can achieve accuracy better than 0.1% at a reasonable jitter level. For applications where the accuracy of the time reference is not so important, with stability requirements between 0.2% to 1% and with stringent power consumption requirements, RC or mobility-based relaxation oscillators can be used. These oscillators have very low chip area and can operate at the sub micro-Watt range. They are well suited for battery powered applications such as wireless sensor networks or biomedical implants in literature.

We have presented also a variation of the mobility with temperature. The surface mobility at high temperature is mainly determined by the bulk mobility, which can be approximated as ($T > 200K$),

$$\mu_n = \mu_0 (\frac{T}{T_0})^{-\beta} \tag{1.18}$$

where β is defined by the doping level and μ_0 is the mobility at the temperature T_0. In a zero-Vt MOSFET, where the doping level is usually low, we can assume that $\beta \approx 1.5$.

1.7 PROPOSED MOBILITY-COMPENSATED TIME REFERENCE

The proposed mobility-compensated time reference has three blocks, as shown in Fig.26:

- Zero-Vt self-biased current source
- Voltage controlled current source (VCCS)
- Current mode Schmitt trigger (CMST)

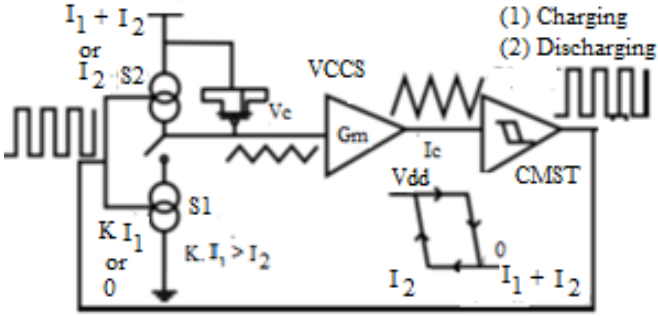

Figure 26 – Block's diagram of the proposed time reference

In chapter 2 to 4 we describe the main sub-circuits that are used in the proposed time reference which is presented in chapter 5. A self-biased current source with zero-Vt is presented in chapter 2. The subject of chapter 3 is a voltage-controlled current source, while a current mode Schmitt-trigger is the subject of the chapter 4. The time reference which makes use of the sub-circuits in chapter 2-4 is described in chapter 5.

2 ZERO-VT SELF-BIASED CURRENT SOURCE (SBCS)

A Self-biased current source can be implemented as an extractor circuit of the specific current of a MOSFET. The specific current generator was proposed in [34], as an alternative to have a stand-alone reference ultra-low power consumption. A design methodology using a transistor model of the MOSFET valid in all operating regions was also introduced in the paper.

This chapter is divided in three sections. In the first section we give some information about the design of the self-biased current source; in the second section we design a zero-Vt self-biased current source and, finally, we have the simulated results of the zero-Vt SBCS.

2.1 SELF-BIASED CURRENT SOURCE (SBCS) DESIGN

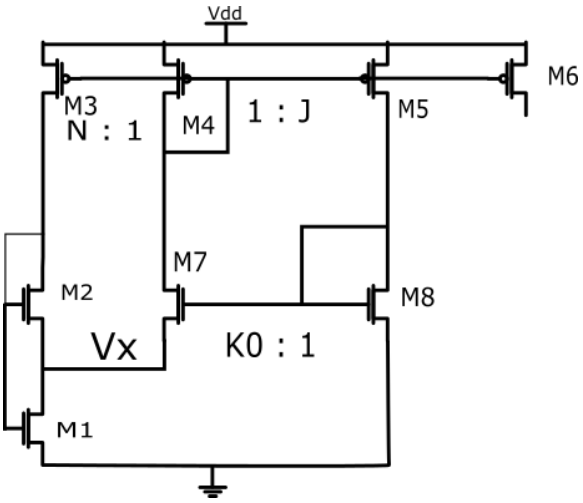

Figure 27 – Full schematic of the self-biased current source

In Fig.27 we show the schematic of the self-biased current source [31], which can be divided in two parts. One of them is the voltage-following current mirror M4, M5, M7 and M8, while the self-cascode MOSFET (SCM) composed by M1 and M2. The Advanced Compact Model (ACM) described in appendix A has been used to design the SBCS [34], [31].

- The design of the voltage following current mirror (VFCM)

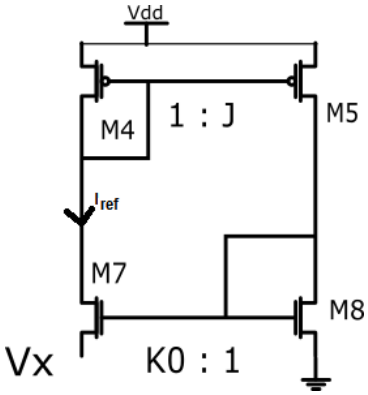

Figure 28 – Voltage following current mirror

The VFCM is composed of transistors M4, M5, M7 and M8. We have applied the Unified Charge Control Model (UCCM) from ACM model to M7 and M8. Then we have:

$$V_{p8} = \phi_t(\sqrt{1+i_{f8}} - 2 + ln(\sqrt{1+i_{f8}} - 1)) \tag{2.1}$$

$$V_{p7} - V_x = \phi_t(\sqrt{1+i_{f7}} - 2 + ln(\sqrt{1+i_{f7}} - 1)) \tag{2.2}$$

$i_{f8} = \frac{JI_{ref}}{I_{S8}}$, $i_{f7} = \frac{I_{ref}}{I_{S7}}$, $K_0 = \frac{I_{S7}}{I_{S8}}$, As reported in [31] M7 and M8 have to be designed to operate in deep weak inversion ($i_{f7} << 1$, $i_{f8} << 1$). Thus, equations (2.1) and (2.2) can be reduced to,

$$V_{p8} = \phi_t(ln(\frac{i_{f8}}{2})) \tag{2.3}$$

$$V_{p7} - V_x = \phi_t(ln(\frac{i_{f7}}{2})) \tag{2.4}$$

Since M7 and M8 have the same threshold voltage, $V_{p7} = V_{p8}$. As a result we have,

$$V_x = \phi_t(ln(J.K_0)) \tag{2.5}$$

The PMOS transistors were designed to operate in weak inversion to allow low voltage application.

- Design of the SCM composed of M1 and M2

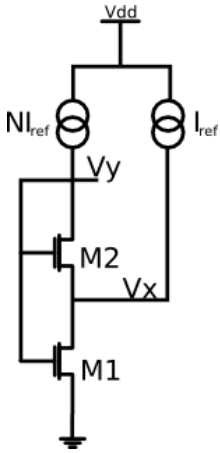

Figure 29 – Specific current generator block

The main block of the specific current generator is 2T-structure of M1 and M2. Fig.29 has been used for the analysis of the SCM. Transistor M2 is in saturation region while transistor M1 is in the triode region. The following equations, hold for Fig.29,

$$N.I_{ref} = I_{S2}.i_{f2} \tag{2.6}$$

$$(N+1).I_{ref} = I_{S1}.(i_{f1} - i_{r1}) \tag{2.7}$$

The pinch-off voltages of M1 and M2 are the same, one can conclude that $i_{f2} = i_{r1}$. After some manipulation of (2.6), (2.7) and (2.5) along with $i_{f2} = i_{r1}$, we have,

$$i_{f1} = i_{f2}.(\frac{S_2.(N+1)}{S_1.N} + 1) \tag{2.8}$$

where $i_{f1} = \frac{(N+1).I_{ref}}{I_{SH}.S_1}$, and $i_{f2} = \frac{N.I_{ref}}{I_{SH}.S_2}$, $I_{SH} = \mu_n, \frac{\phi_t^2}{2}.n.C_{ox}$, I_{SH} is the normalized specific current of MOSFET. Here we have used $S_i = \frac{W_i}{L_i}$.

From equation. (2.8), one can conclude that if V_x is PTAT, then I_{ref} is a copy of the specific current. Conversely, if I_{ref} is a copy of the specific current then V_x is PTAT.

2.2 ZERO-VT SELF-BIASED CURRENT SOURCE

The design of the zero-Vt current source use the scheme in Fig.27 with zero-Vt transistors M1 and M2. Contrary to the standard transistor in the SCM, in which the short circuit between drain and gate generally ensures that the device operates in saturation, the diode connection of the zero-Vt transistor does not ensure operation in saturation. In order to bias the zero-Vt transistor in saturation, we have included a diode-connected standard MOSFET Mn1, biased by a constant current-source, in order to produce a voltage drop between the drain and the gate of the zero-Vt as shown in Fig.30. If the current through the transistor Mn1, which is $K_c.I_{ref}$, increases, the voltage drops in the transistor M2 increases, but $K_c.I_{ref}$ has to be less than $N.I_{ref}$.

2.2.1 Proposed zero-Vt self-biased current source

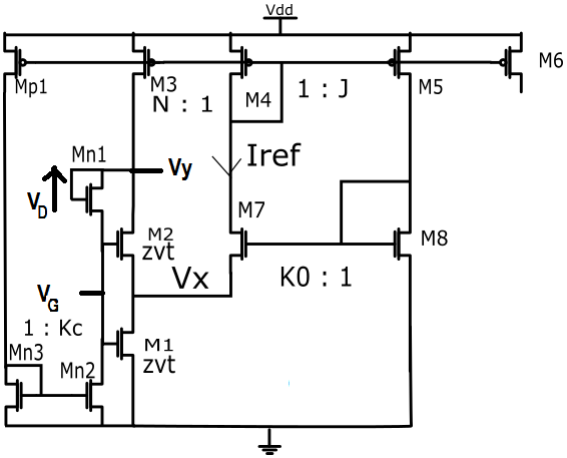

Figure 30 – Proposed zero-Vt specific current generator

In this sub-section we have proved that the transistor zero-Vt M2 remains in saturation and we have shown the dimensions of transistors used

in the zero-Vt self-biased current source. To prove that M2 will remain in saturation, we have applied UCCM to M2, in the source we have:

$$V_{p2} - V_x = \phi_t(\sqrt{1+i_{f2}} - 2 + ln(\sqrt{(1+i_{f2})} - 1)) \tag{2.9}$$

In the drain of M2 we have:

$$V_{p2} - V_y = \phi_t(\sqrt{1+i_{r2}} - 2 + ln(\sqrt{(1+i_{r2})} - 1)) \tag{2.10}$$

To keep the transistor M2 in saturation we have to design V_y and V_x to satisfy the condition $V_y - V_x > V_{dsat_{M2}}$ and $V_y = V_D + V_G$. Then V_D and V_G are designed such away to allow that $V_D + V_G - V_x > V_{dsat_{M2}}$, With $V_D \approx 200mV$, $V_G \approx 200mV$ and $V_x \approx 60mV$. We have considered that M2 is in saturation when the drain-source voltage of M2 is greater than $V_{dsat_{M2}} = 200mV$, consequently one can consider that the transistor M2 is in saturation since $V_{dsat_{M2}} < (V_D + V_G - V_x = 340mV)$. Using the same logic in section.2.1 equation.(2.8) but considering that the current through the transistor M2 is $(N - K_c).I_{ref}$, one can deduce that,

$$i_{f_2}[(\frac{N - K_c + 1}{N - K_c}).\frac{S_2}{S_1} + 1] = i_{f_1}. \tag{2.11}$$

From equation.(2.5) $V_x = \phi_t ln(J.K_0)$, then we can apply UCCM to M1 and M2,

$$\phi_t.F(i_{f_1}) - \phi_t.F(i_{f_2}) = V_x. \tag{2.12}$$

where $F(i_{fi}) = \phi_t(\sqrt{1+i_{fi}} - 2 + ln(\sqrt{1+i_{fi}} - 1))$
Combining equations.(2.11) and (2.12) we got,

$$\phi_t.F(i_{f2}[(\frac{N - K_c + 1}{N - K_c}).\frac{S_2}{S_1} + 1]) - \phi_t.F(i_{f2}) = V_x \tag{2.13}$$

We have fixed the parameters $N = 2$, $K_c = 1$, $J = 0.5$, $K_0 = 8$ and $\frac{S_2}{S_1} = 2.5$.

As we have fixed $J = 0.5$ and $K_0 = 8$ then $V_x = \phi_t.ln(J.K_0) = 1.38.\phi_t$. From equation.(2.13) we can determine the value of $i_{f2} = 26$. From equation.(2.11) we can determine the inversion level of $i_{f1} = 40$. Table 2 resume the width and the length of the zero-Vt self-biased current source. M7 and M8 are designed in deep weak inversion then i have used a wide width, and M3, M4, M5, are designed in deep weak inversion.

Table 2 – Width and length of the zero-Vt Self-Biased current source

	Width	Length
M1	3 μm	3 μm x 5
M2	3 μm	3 μm x 5
M3	5 μm x 2	3 μm
M4	5 μm	3 μm
M5	5 μm	3 μm x 2
M7	13 μm x 8	3 μm
M8	13 μm	3 μm
Mn1	10 μm	3 μm
Mn2	10 μm	3 μm
Mn3	10 μm	3 μm
Mp1	5 μm	3 μm

2.2.2 Simulation result of the zero-Vt Self-Biased current source

The simulation result of the self-biased current source using analog environment 180 nm CMOS technology is shown in Fig.31 and Fig.32. Fig.31 shows the simulation result of the current reference with respect to temperature variation. We can see that at -20° C the current reference is around 10 nA and at 80 ° C the current reaches almost linearly the value of 20 nA. This current reference is the specific current of the zero-Vt. The variation of the specific current with respect to the temperature variation is defined by the term $\mu_n.\phi_t^2$, where $\mu_n = \mu_0(\frac{T}{T_0})^{-\beta}$, one can conclude that the value of β should be less than 1 and greater than 0.6 to obtain the variation with respect to temperature as shown in Fig.31 (we have considered that the slope factor and the oxide capacitance are temperature independent). Fig.32 shows the current reference with respect to supply voltage variation. the minimum supply voltage is around 0.4 V and the maximum is 1.8 V. A global variation of 1 nA can be observed in Fig.32.

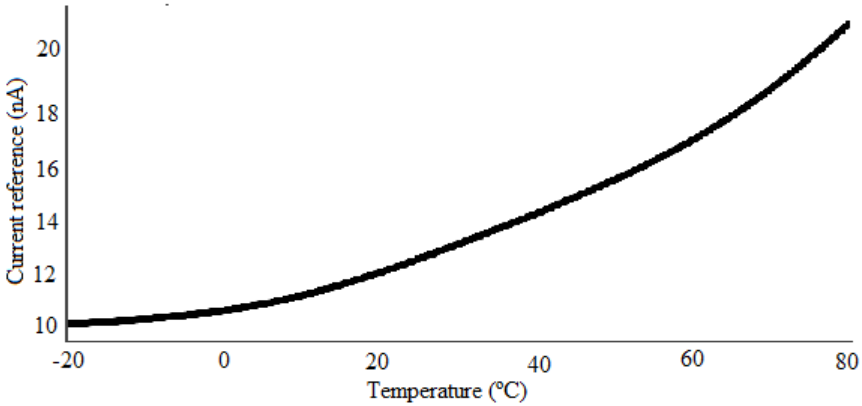

Figure 31 – Zero-Vt specific current generator vs temperature (°C)

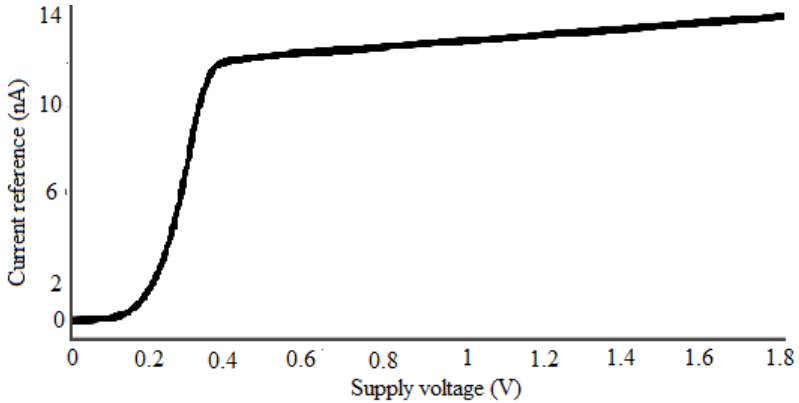

Figure 32 – Simulation Zero-Vt specific current generator vs supply voltage

3 VOLTAGE-CONTROLLED CURRENT SOURCE

A voltage-controlled current source is an electronic component which converts linearly a voltage to a current. The voltage controlled current source that we have used, can be divided in 2 basic building blocks, an operational transconductance amplifier (OTA) and a common source amplifier with diode connected load. This chapter is divided in three sections, in the first section we present the OTA design, in the second section the common source amplifier and, finally, the voltage controlled current source.

3.1 OPERATIONAL TRANSCONDUCTANCE AMPLIFIER DESIGN

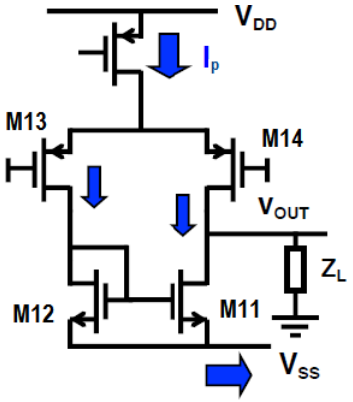

Figure 33 – Operational transconductance amplifier

The operational transconductance amplifier, shown in Fig.33, is a device that generates at its output a current that is a linear function of the differential input voltage.

Ideally, the output current is given by

$$I_{out} = V_{diff}.G_m \tag{3.1}$$

G_m is the equivalent transconductance of the OTA.

When the load of the OTA is a capacitance we have in this case, the

output impedance is given by,

$$\frac{1}{r_{out}} = g_{md11} + g_{md14} \tag{3.2}$$

and the band-width of the OTA is,

$$BW = \frac{1}{2.\pi.r_{out}.C_{load}} \tag{3.3}$$

the gain A_1 of the OTA is ,

$$A_1 = \frac{g_{m14}}{g_{md14} + g_{md11}} \tag{3.4}$$

and the gain band-width is,

$$GBW = \frac{g_{m13}}{2.\pi.C_{load}} \tag{3.5}$$

The OTA has to be high gain, then we have designed the transistors M13 and M14 in weak inversion, in this case $g_{m14} \approx \frac{I_p}{\phi_t}$, and we have used long length in the transistors M11 and M12 then the output resistance $\frac{1}{r_{out}} = \frac{I_p}{V_E.L}$, where the V_E is the early voltage and $L = 3\mu m$ is the length of the transistor and $I_p = 20nA$ is the polarization current of the OTA.

3.2 COMMON SOURCE AMPLIFIER WITH ACTIVE LOAD

In common source amplifier, the input is connected to the gate and the output taken from the drain

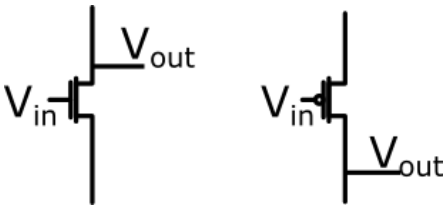

Figure 34 – Common source amplifier

In Fig.34, we have the simple topology of the common source amplifier. We can divide a common source amplifier into two groups:

- Without source degeneration as shown in Fig.35, then we have no body

effect for the main transistor.

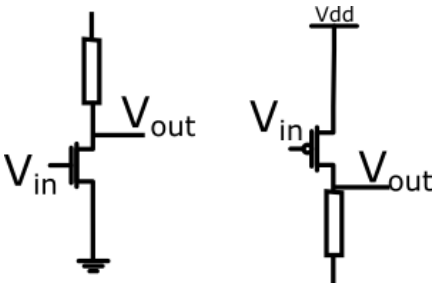

Figure 35 – Common source amplifier with load

- With source degeneration as shown in Fig.36, then we have to take the body effect into account for the main transistor.

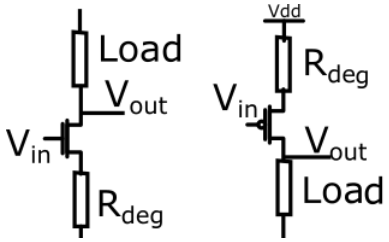

Figure 36 – Common source amplifier with load and degeneration

In a simple common source amplifiers without source degeneration, the gate voltage variations times g_m gives the drain current variation, and the drain current variations times the load gives the output voltage variations. Therefore, one can expect the small-signal gain to be:

$$A_v = r_{out}.g_m \tag{3.6}$$

where g_m is the transconductance in relation to the gate voltage and r_{out} is the output impedance. The loads used in the common source amplifier, could be, a resistive load, current source load, diode connected load and triode load. The last two types of load which are diode connected load and triode load (Fig.37) were used in the design of the VCCS.

The small-signal gain for the common source amplifier in Fig.37(a) is given by equation.(3.7),

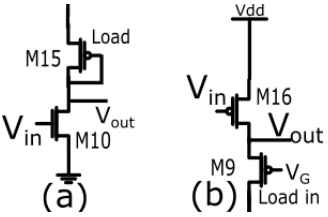

Figure 37 – (a)NMOS common source amplifier with diode connected load (b) PMOS common source amplifier with NMOS load in triode

$$A_2 = \frac{g_{m10}}{g_{m15} + g_{md15} + g_{md10}} \tag{3.7}$$

and the small signal for the common source amplifier in Fig.37(b) is given by equation.(3.8)

$$A_3 = \frac{g_{m16}}{g_{md16} + g_{md9}} \tag{3.8}$$

3.3 VOLTAGE CONTROLLED CURRENT SOURCE

The simple voltage controlled current source (VCCS), formed by the OTA , and the common source amplifier is shown in Fig.38.

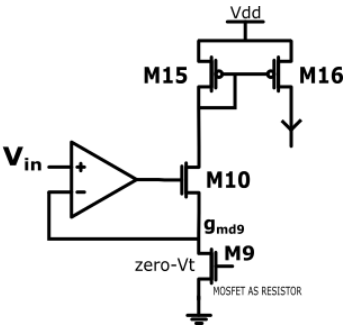

Figure 38 – Schematic of the voltage controlled current source block

But this topology has the body effect on the main transistor of the common source amplifier which is represented by M10. This body effect reduces the small-signal gain of the transistor M10. To avoid this fact, we have done some modifications on the topology in Fig.38 as shown in Fig.39.

We have transformed the transistor M10 in common source amplifier without body effect. Then we can emulate high value of resistor in M9 increasing the value of K_r.

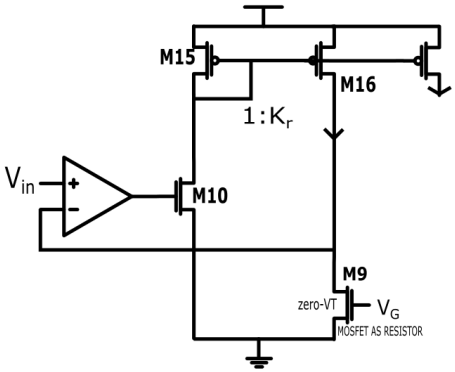

Figure 39 – Schematic of the voltage controlled current source block

Fig.40 shows the full schematic of the voltage controlled current source. The capacitor C is used for overall stability and its value is 500 fF. A_1 is the OTA gain, A_2 is the gain of the common source amplifier with diode connected load and, A_3 is the gain of the common source amplifier with load in triode.

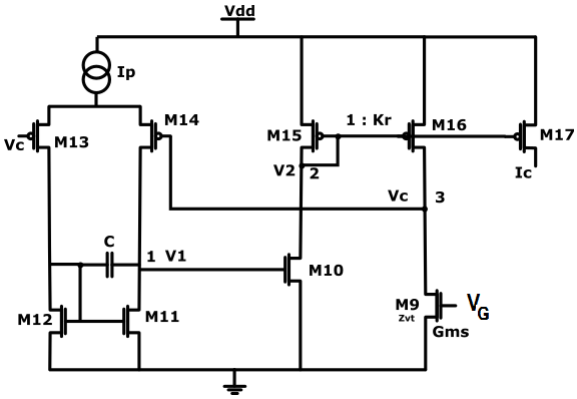

Figure 40 – Voltage controlled current source (the capacitor C is for overall stability)

One can express the open loop gain as follow,

$$V_1 = A_1(V_c - V_3) \tag{3.9}$$
$$V_2 = A_2.V_1 \tag{3.10}$$
$$V_3 = A_3.V_2 \tag{3.11}$$

From equations (3.9), (3.10) and (3.11), we have:

$$V_3.(1 + A_3.A_2.A_1) = A_3.A_2.A_1.V_c \tag{3.12}$$
$$V_3(\frac{1}{A_3.A_2.A_1} + 1) = V_c \tag{3.13}$$

From equation.(3.13) we can say that, if the open loop gain defined as $A_1.A_2.A_3 >> 1$ then,

$$V_c \approx V_3. \tag{3.14}$$

Where A_1, A_2 and A_3 are defined previously.

We have used zero-Vt MOSFET as resistor then the current in this resistor will be defined by V_c as, $I_c = V_c.g_{md9}$.

3.3.0.1 Comments on the nonlinear characteristic of the MOSFET

The output characteristic I-V_{DS} of the MOSFET shows two regions [31]. The MOSFET operates as current source in saturation and as a resistor in the triode region. When a MOSFET is used as a resistor we have a non-linear behavior at some drain-source voltage of the resistor. This limits the range of V_c that we can operate the MOSFET as resistor. The MOSFET as resistor is modeled and reported in [31],

$$g_{md9} = \frac{2.I_S}{\phi_t}.(\sqrt{1 + i_{r9}} - 1) \tag{3.15}$$

In Fig.40, the transistor M9 is biased by a gate voltage V_G as defined in Fig.30. In the chapter.5 we have explained the reason of the use of this V_G. From equation.(3.15), the stability of the MOSFET as resistor g_{md9}, depends strongly with the variation of the specific current of the MOSFET. In chapter 1, we have discussed about mobility variation with temperature and process variations due to the fact that the specific current depends strongly with the mobility variation. Fig.23 and Fig.22 show the mobility variation with process and temperature variations. And one can interpret that at low doping level the bulk mobility is independent with process variation and its value decreases linearly when the temperature increases. To verify this in-

terpretation we have plotted the output I-V characteristic of the MOSFET at different temperature for the native (zero-Vt) MOSFET, for the case where $V_{GB} = V_{th}$ Fig.41 shows the set up,

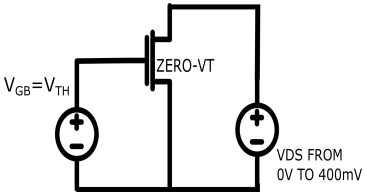

Figure 41 – Setup to plot the output characteristic of the zero-Vt ($I_d vs V_{ds}$)

V_{th} is the threshold voltage of the zero-Vt MOSFET. We have extracted the threshold voltage using $\frac{gm}{I_d}$ method at different temperatures as shown in Fig.25. When $V_{GB} = V_{th}$, the equivalent inversion level is $i_r = 3$, then we can write that [31], $g_{md} = \frac{2.I_S}{\phi_t} = \frac{\mu_n.\phi_t.C'_{ox}.n.W}{L}$. Table.3 summarize the length and width used in this voltage controlled current source.

Table 3 – Width and length of the voltage controlled current source

	Width (μm)	Length(μm)
M9	3	$20x3$
M10	3	3
M11	3	3
M12	3	3
M13	10	3
M14	10	3
M15	3	3
M16	3	3

4 CURRENT MODE SCHMITT TRIGGER (CMST)

The current-mode Schmitt trigger is composed of switches and a current comparator. In this chapter we present some state-of-the-art of current comparators and the proposed current-mode Schmitt trigger.

4.1 STATE-OF-THE-ART OF CURRENT COMPARATORS

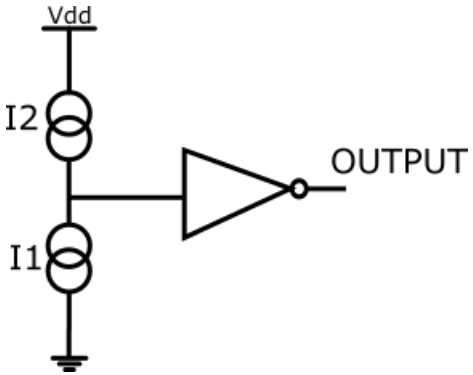

Figure 42 – Freita's comparator [35]

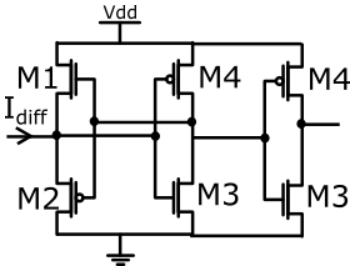

Figure 43 – Traff's comparator [36]

In many cases, the signals from sensors are currents [37], [38], [39]. Also, the output signal from a transistor is a current. Thus a current comparator is often required to process directly the signal from sensors or from transistors. As in any decision circuitry, accuracy, power, and high speed

are important parameters of comparators. Additionally, current comparators must work over a wide range of supply voltages, wide range of temperatures, and not be sensitive to process variation. Also it should not have a dead zone in the transfer characteristic. A very simple current comparator is shown in Fig.42 [35], but this current comparator has long delay when operated at low currents.

Reference [36] presents the most referenced current comparator, known as Traff's comparator and shown in Fig. 43. This current comparator is high speed and has low input impedance. The feedback operation of this circuit does not allow the input node to rise from rail to rail, and this increases the speed of the comparator. But Traff's comparator has a dead zone. Since the publication of the Traff's comparator a number of designs [40], [41], [42] has been tried to achieve the high speed, low power and no dead zone. In [43], [44], two different classes of AB current comparator, free of dead zone, were published. But the minimum supply voltage has to be one threshold voltage of NMOS plus two saturation levels, which is not suitable for low voltage application. Also these current comparators, shown in Fig.44, Fig.45, need a clock to operate .

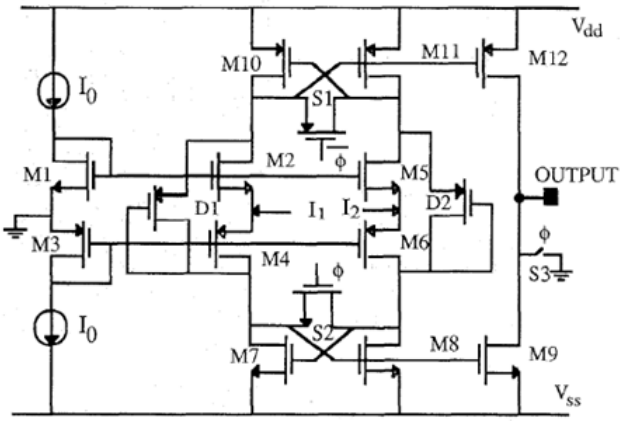

Figure 44 – Class AB current comparator with switch [43]

The comparator in Fig.44 [43], has two inputs; I_1, and I_2. When the clock signal ϕ is high, the circuit works as a current conveyor which is a combination of voltage and current follower. Transistors from M1 to M6 form a translinear loop, which fixes the quiescent current of the branches and the input node voltage at the ground potential. Transistors M7, M8, M10 and

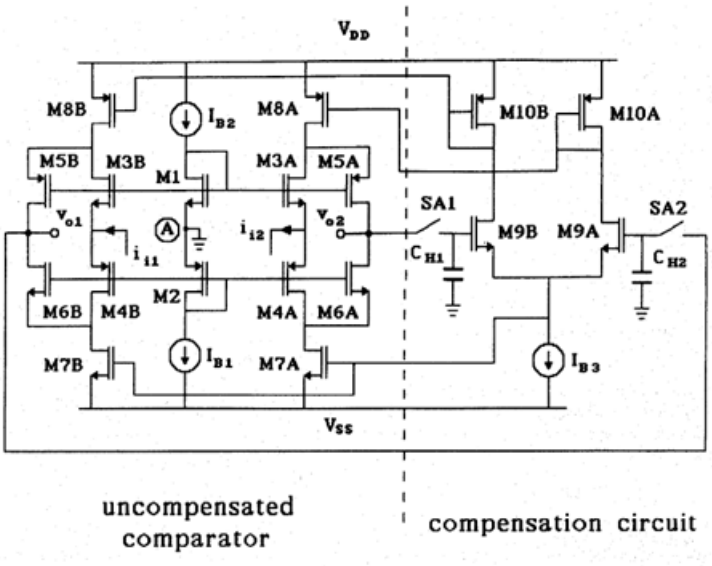

Figure 45 – Class AB current comparator with compensation circuit [44]

M11 constitute two latches and they have a regenerative operation when ϕ goes down. Transistors M7, M9 and M10, M12 operate as current mirror. To explain how the topology in Fig.44 works, we have considered following cases with $V_{dd} = -V_{ss}$,

- $\phi = 0$, then switches S1 and S2 are opened and S3 is closed.
  - $I_1 = 0$ and $I_2 = 0$, The current through the transistors M2, M4, M5 and M6 is I_0. The diodes D1 and D2 limit the voltage in the drain-source of the transistor M2, M4 and M5, M6 respectively. This allows that the increase of the current $I_1(I_2)$ does not increase so much the drain-source of M4 and M2(M5 and M6).
  - $I_1 > I_2$, the drain-source voltage of the transistor M7 increases and the drain-source voltage of the transistor M8 decreases. The source-drain voltage of M10 increases and the source-drain voltage of M11 decreases. This results in the fact that the transistor M9 is ON and the transistor M12 is OFF. Consequently the output goes to V_{ss}.
  - $I_1 < I_2$, the drain-source voltage of M8 increases and the drain-source voltage of M7 decreases and the source-drain voltage of

M11 increases and the source-drain voltage of M10 decreases. This results in the fact that transistor M12 is ON and transistor M9 is OFF. Consequently the output goes to V_{dd}.

- $\phi = 1$ then switches S1 and S2 are closed and S3 is opened. Due to the perfect symmetric of the topology considering that we have not mismatch, one can consider that the current through M7 and M8 for the NMOS latch and the current through M10 and M11 for PMOS latch are equal. As $I_1 + I_2 + 2.I_0$ is the total current through the branch formed by M2, M4, M5, M6, M7, M8, M10 and M11, then one can consider in case of equilibrium of the current and perfect symmetric of the topology that the current through M8 and M11 is $\frac{I_1+I_2}{2} + I_0$. This current is mirrored in M9 and M12 and the output is near to zero Volt.

The comparator in Fig.45 [44] is based on the double folded cascode structure and includes a compensation circuit which provides offset and charge-injection compensation as well as common-mode output voltage control. The uncompensated comparator is made up of transistors M3 - M6 and current source transistors M7, M8. Diode connected transistors M1 and M2, and current sources I_{B1} and I_{B2}, set the input bias current and the input bias voltage. The offset compensation circuit is provided by the differential stage M9-Ml0, the current generator I_{B3}, the storage capacitors C_{H1}, C_{H2}, and the switches SA1 and SA2. The diode connected transistors M_{10A}, M_{10B} set the bias current in M8A and M8B to I_{B3}/2. Moreover the gate-source voltage of M9 together with the gate-source voltage of M7 provide the output bias voltage. When switches SA1 and SA2 are closed, the uncompensated comparator, and the compensation circuit are connected through two different loops, one for the differential signal and other for the common-mode signal. When switches SA1 and SA2 are opened, the two loops are disconnected and the common-mode output level and the output offset voltage are both frozen in the hold capacitors.

Another circuit reported in the technical literature [45] is shown in Fig.46. This circuit can work at low voltage below 500 mV without dead zone, but the input node rises from rail to rail. In fact, The circuit in Fig.46 does not work as current comparator but as current level detector. In Fig.47 the waveform of the current level detector proposed in [45]. In this example the output voltage changes from high to low when the input crosses a certain level. The output remains low for a while, after some time, it goes up and remains up until $I_{sensor} = I_{ref}$ (see Fig.47).

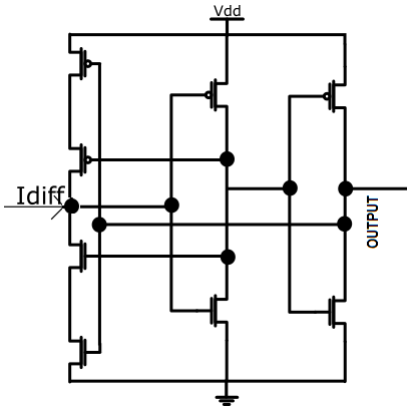

Figure 46 – Toumazou's current comparator [45]

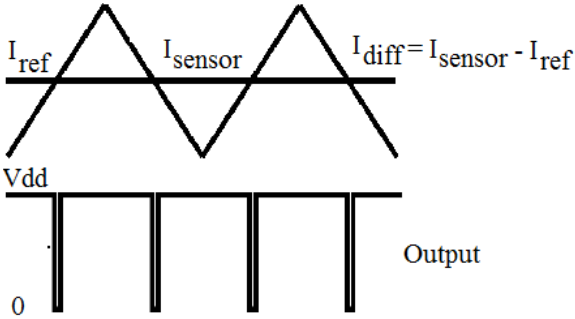

Figure 47 – Waveform from toumazou current comparator

4.2 PROPOSED CURRENT-MODE SCHMITT TRIGGER (CMST)

The current-mode Schmitt trigger proposed in this work is divided in 2 blocks, a current switch system and a current comparator [46], [47], [48].

4.2.1 Current comparator

We have used a modified topology of [45], that operates as a zero-current level detector, rather than as a current comparator. We have shifted the negative feedback in Fig.46 by one gate-source voltage V_{GS} down for

the NMOS and one source-gate voltage V_{SG} up for the PMOS. This increase the input impedance and reduce the resolution current, the minimum current necessary at the input to rise from low to high. The modification has to goal to force the topology in Fig.46 to have the small current resolution, when used with switch system to form the CMST. As any current comparator this zero-current detector level is divided in 3 blocks as shown in Fig.48. In the

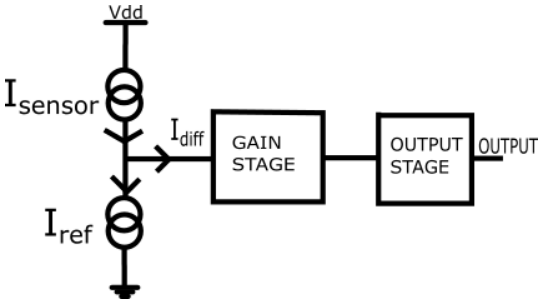

Figure 48 – General topology of current comparator

next paragraph we have discussed, each block.

4.2.1.1 Current difference stage

A simple current difference stage is shown in Fig.48. We have the current $I_{diff} = I_{sens} - I_{ref}$, if the current $I_{diff} > 0$ then we have some current entering in the gain stage and if $I_{diff} < 0$, we have some current from the gain stage to the difference stage.

4.2.1.2 Proposed gain stage

The proposed gain stage is shown in Fig.49 and has two feedbacks, a positive feedback and a negative feedback. Initially we consider that the current in the input node of the gain stage is zero. Then the input node voltage is designed to some value close to $\frac{V_{dd}}{2}$.

When some current entering in the gain stage ($I_{diff} > 0$), the input voltage rises to high level, then the voltage at the output of the inverter formed by M8 and M5 goes to low level. This voltage is shifted one gate-source voltage down and up through M6 and M7 respectively and forms a negative feedback through M2 and M3. This feedback increases the input resistance

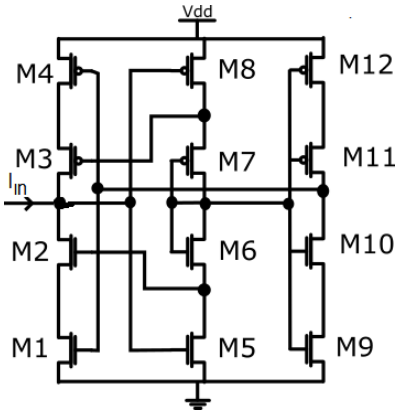

Figure 49 – Proposed gain stage for current detector level (All NMOS has the same width and length and all PMOS has the same width and length)$W_p = 500nm\ W_n = 600nm\ L = 180nm$

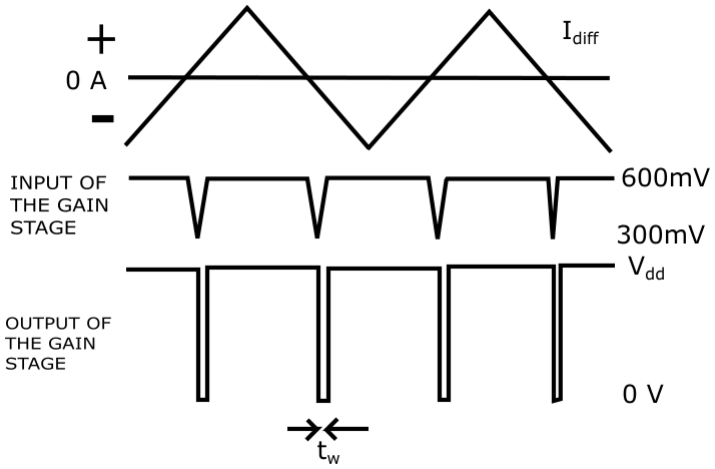

Figure 50 – Wave form in the input and output of the proposed gain stage

of the gain stage, which allows a small resolution of the gain stage. After some nanosecond delay the positive feedback acts on M1 and M4 to reduce the swing at the input of the gain stage as shown in the Fig.49, when some current goes from the gain stage to the difference stage ($I_{diff} < 0$) the input of the gain stage increases and the gain stage acts exactly as the case of $I_{diff} > 0$.

Then if $I_{diff} = 0$ the input remains at some voltage close to $\frac{V_{dd}}{2}$. The gain voltage is designed such a way that when the input of the gain stage is closed to $\frac{V_{dd}}{2}$ the output is goes low level.

Fig.50 shows the expected waveform of the proposed current detector level. One can see that when the current $I_{diff} = 0$ the output switches from high to low level and return to high level when $I_{diff} \neq 0$ after some delay t_w, t_w represents the delay through the inverter formed by M9-M12. We can see that the output waveform in Fig.50, is a zero-current level detector. This does not represent the real logic of a current comparator. But to form a current comparator we can use a flip-flop D in its output.

4.2.1.3 Output stage

The true current comparator logic is $I_{diff} > 0$ the output of the gain stage at high level and when $I_{diff} < 0$ the output of the gain stage at low level. Which is not the same logic with the current level detector in Fig.49. Then to recover the current comparator logic from the gain stage (current level detector) in Fig.49, with output waveform presented in Fig.50. We can use at the output of the gain stage a simple flip-flop D as shown in FIg.51.

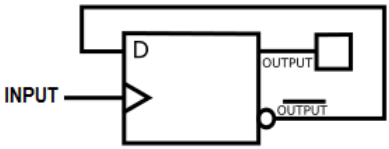

Figure 51 – Flip-Flop D logic

Fig.52 shows the full schematic of the current comparator.

Fig.53 shows the input and output waveform of the flip-flop D, when we have used a flip-flop D in the output of the gain stage to recover a current comparator logic. We can see that when the current I_{diff} is close to zero, the output of the gain stage of the current level detector (output1) switches from high to low level and if the current $I_{diff} \neq 0$ the output of the gain stage (output1) switches from low to high level. the output (output1) of the gain stage is the input of the flip-flop D. When the output1 Fig.52 goes from high to low, the output of the flip-flop does not change. And some nanosecond, when the output1 goes from low to high the output of the flip-flop changes its state (High-low or low-high). Then using a flip-flop D in the output of the gain stage (current level detector) allows to recover the current comparator

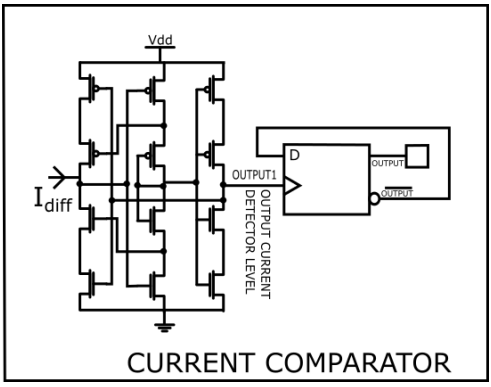

Figure 52 – Proposed current comparator

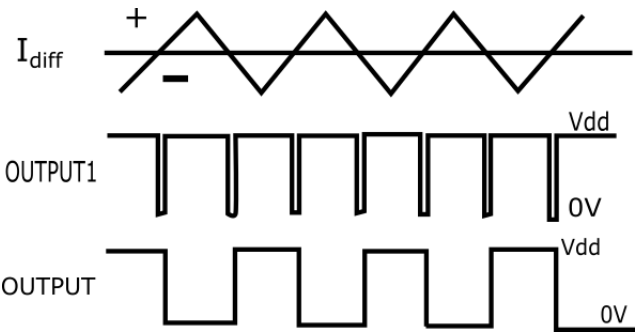

Figure 53 – Output waveform of the proposed current comparator

signal as shown in Fig.53. In resume the proposed gain stage together with the flip-flop forms a current comparator.

The input of the gain stage rises from low voltage to high voltage (ground to supply voltage). Then we can limit this variation at the input using together to the previous current comparator a current switch system to form a current mode Schmitt trigger where we can reduce the hysteresis width to allow that the input does not rise from high to low voltage.

4.2.2 Current mode Schmitt trigger

In Fig.54, the schematic of the proposed current mode Schmitt trigger is shown. We consider initially that M_{s1} is OFF, M_{s2} is ON and the input node

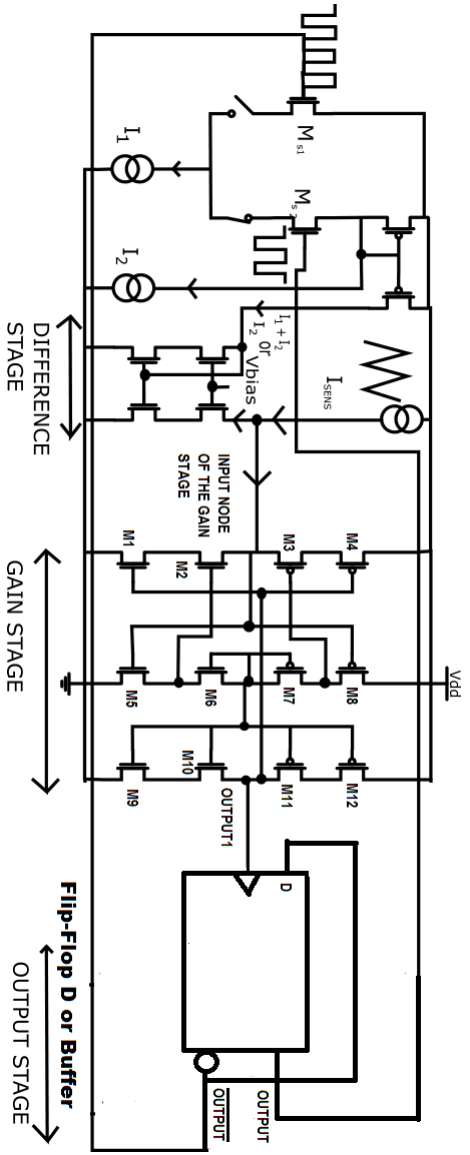

Figure 54 – Full schematic of the current mode schmitt trigger

voltage of the gain stage is at initial value greater than $V_{dd}/2$ and the output of the flip-flop is at high level. The current reference is equal to $I_1 + I_2$, then we

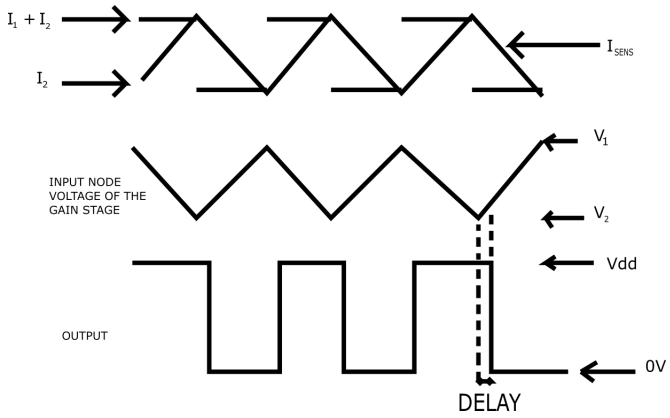

Figure 55 – Waveform of the current mode Schmitt trigger

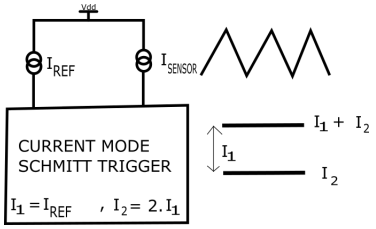

Figure 56 – Configuration to simulate the current mode Schmitt trigger

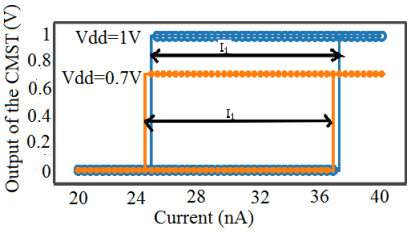

Figure 57 – DC simulation of the hysteresis of the current mode Schmitt trigger

consider that the current in the sensor I_{sens} rises from some value below $I_1 + I_2$. As $I_{sens} < I_1 + I_2$ the input node voltage of the gain stage discharge with the current $I_1 + I_2 - I_{sens}$, when I_{sens} is close to $I_1 + I_2$, the input node voltage is at some voltage below the threshold voltage of the inverter formed by M5 and

M8 in the gain stage and the output (output1) switches from high to low level and return to high level after some nanosecond delay when $I_{sens} \neq I_1 + I_2$, as shown in Fig.55, this transition makes the output of the flip-flop switches from high to low level, consequently the transistor M_{s1} will be ON and the transistor M_{s2} will be OFF. The current reference is equal to I_2 in this case. Then the input node of the gain stage is discharged by the difference current of $I_{sens} - I_2$. When $I_{sens} = I_2$ the input of the gain stage is at some value below below the threshold voltage of the inverter formed by M5 and M8, consequently the output of the gain stage (output1) switches from high to low and return to high level, this transition makes the output of the flip-flop switches from low level to high level, and M_{s1} is OFF, M_{s2} is ON, the current reference is $I_1 + I_2$ and the input of the gain stage discharges another time.

The input node of the proposed gain stage is resistive. Then it rises from low voltage to high, and the current reference for the difference stage is affected directly by this variation. To avoid this fact at the input node of the gain stage, we have reduced the hysteresis of the current mode Schmitt trigger to 20 mV, this is $V_1 - V_2 = 20mV$ in Fig.55, then we have operated the input node around 150 mV (150 mV +/- 20 mV), and the input node has a small variation.

For simulation purposes we configure the setup in Fig.56, we have the DC simulation of the current mode Schmitt trigger at two different supply voltages $V_{dd} = 0.7V$ and $V_{dd} = 1V$ Fig.57. To avoid that the input node discharge completely and make the input swing from zero volt to supply voltage, we have to reduce the hysteresis to 20 mV with equivalent current in nano-Ampere (13 nA). We can see that when we increase the supply voltage we have some DC offset. This DC offset is due to the fact that when we increase the supply voltage we have increased the level of the input node voltage. But this does not affect the hysteresis of the current mode Schmitt trigger which depends only on the current reference as shown in Fig.57. Then the hysteresis of the current mode Schmitt trigger depends only with the variation of the current reference with process, voltage and temperature (PVT).

In the current mode Schmitt trigger we have used high swing current mirror to copy the current reference. In the next section we have shown the design of the high swing current mirror.

4.3 HIGH SWING CURRENT MIRROR

One way to increase the output impedance of a current mirror is through the use of self-biased cascode current mirror, but the main drawback of self biased cascode current mirrors is a very loss of signal swing, which is criti-

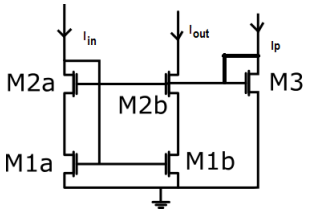

Figure 58 – High swing current mirror

cal for low supply voltage. Then to decrease the supply voltage and operate at low voltage we have used the high-swing current mirror [31]. The output impedance is given by equation. (4.1). [1].

$$r_{out} = r_{DS2b}.gm_{2b}.r_{DS1b} \tag{4.1}$$

The transistor M3 allows to bias properly the source of the transistor M2b at some value greater than the saturation voltage of M1b.

Then using UCCM (Unified Charge Controlled Model) we have:

$$V_{p3} = \phi_t(\sqrt{1+i_{f3}} - 2 + ln(\sqrt{1+i_{f3}} - 1)) \tag{4.2}$$

$$V_{p2} = V_{S2} + \phi_t(\sqrt{1+i_{f2}} - 2 + ln(\sqrt{1+i_{f2}} - 1)) \tag{4.3}$$

We suppose that M3 and M2 are identical transistors, then the same threshold voltage and the same pinch-off voltage V_p. Then from equations (4.2) and (4.3) we have:

$$V_{S2b} = \phi_t(F(i_{f3}) - F(i_{f2})) \tag{4.4}$$

where $F(i_{fi}) = \sqrt{1+i_{fi}} - 2 + ln(\sqrt{1+i_{fi}} - 1)$. Then to guarantee that the transistor M1 remains in saturation, we have $V_{S_{M1}} > \phi_t(\sqrt{1+i_{f2}} + 3) = V_{S2b}$.

From (4.2), (4.3), (4.4) we have:

$$\phi_t(\sqrt{1+i_{f2}} + 3) = \phi_t(F(i_{f3}) - F(i_{f2})) \tag{4.5}$$

Transistors M1, M2, M3 have designed in moderate inversion then we have $5 = F(i_{f3}) - F(i_{f2})$. We fix $i_{f2} = 3$ and one can obtain, $5 = F(i_{f3})$ and $i_{f3} = 26$. In this design we chose k = 1, and M1, M2 as identical transistor. Then we have $I_{S1} = I_{S2} = \frac{I_{S3}}{7}$.

[1] More information about the design of the current mirror is given in [31]

To reduce the mismatch, we have to increase the total area [31]. Increasing so much the width and the length of the transistor reduces the frequency transition [31]. Then we have a trade-off between the mismatch and the frequency transition. This results of the value of the width and length of M1a, M1b, M2a, M2b and M3 as shown in table4.

Table 4 – Width and length of the high swing current mirror shown in Fig. 58

	W	L
M1a	1 μm x2	L = 3μm
M1b	1 μm x2	L = 3μm
M2a	1 μm x2	L = 3μm
M2b	1 μm x2	L = 3μm
M3	1 μm x12	L = 3μm

5 MOBILITY-COMPENSATED TIME REFERENCE

Mobility-compensated time reference is a new approach to design a time reference which can be independent with process, voltage and temperature (PVT) variations. This chapter is divided in two parts, the design of the mobility-compensated time reference, and the experimental results of the fabricated integrated circuit in 180 nm. To design the mobility-compensated time reference generator, we have used a zero-Vt self-biased current source (chapter 2), a Voltage controlled current source (chapter 3), and a current mode Schmitt trigger (chapter 4). Measurements of the time reference were taken for the characterization of the figure of merit (FOM) described in appendix B.

The proposed mobility-compensated time reference is shown in Fig.59.

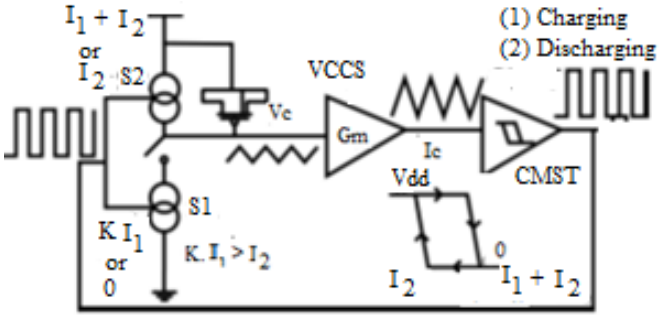

Figure 59 – Block's diagram of the proposed time reference

5.1 PRINCIPLE OF THE MOBILITY-COMPENSATED TIME REFERENCE

- Charging:

  Initially, suppose that the output of the current-mode Schmitt trigger is high. In this case, the current through S1 is zero and that through S2 is $I_1 + I_2$ Fig.59, thus, the capacitor is charged by the current $I_1 + I_2$. The capacitor voltage is converted into a current by the voltage-controlled current source (VCCS) Fig.60. The voltage-to current conversion is achieved through MOSFET operating as resistor. This current, I_c, is compared to $I_1 + I_2$. When I_c greater than $I_1 + I_2$ the output of the CMST switches from high to low.

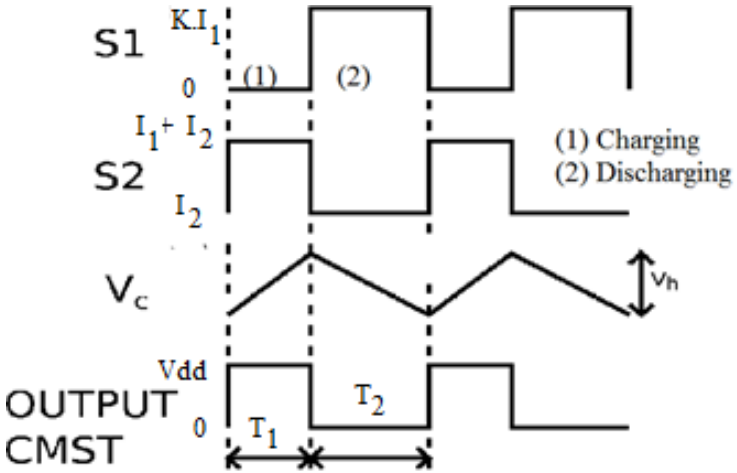

Figure 60 – Waveform of the proposed time reference

- Discharging:

  After the output of the CMST switches from high to low level, the current in S1 switches from 0 to $K.I_1$ and the current of S2 switches from I_1+I_2 to I_2. K is such that $K.I_1 > I_2$; thus, $K.I_1 - I_2$ is the discharging current of the capacitor. The capacitor voltage is converted to I_c which, in turn, is compared to I_2. When the current I_c becomes less than I_2, the output of the CMST goes from low to high and the capacitor is charged once again by the current I_1+I_2.

The hysteresis width is equal to I_1 and the slope factor of the current I_c is proportional to I_1, due to the fact that the capacitor is charged by I_1+I_2. Then if we have some variation in the current reference due to process, voltage and temperature (PVT), the hysteresis of the Schmitt trigger will increase or decrease according to the variation of the current reference, but the slope factor of the current I_c will increase or decrease proportionally with the hysteresis current I_1 and the period of charging or discharging will not be affected.

At this point we can conclude that if the zero-Vt current source varies due to PVT, the period of oscillation will remain the same due to the fact that the current I_c will track the variation of the current reference, increasing or decreasing the slope factor of I_c. The current $I_c = V_c.g_{md16}$ where g_{md16} (see Fig.61) is the conductance of the zero-Vt MOSFET as resistor M16 in the

voltage controlled current source Fig.62.

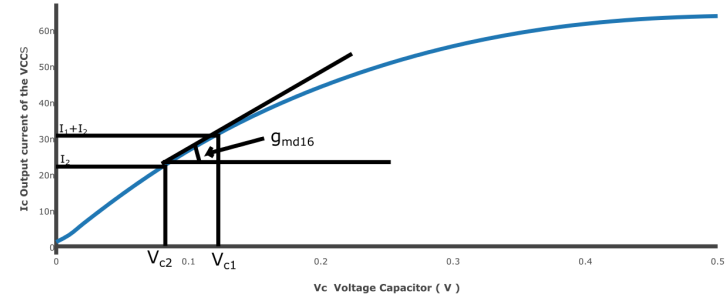

Figure 61 – Conductance of the MOSFET as resitor

Then this resistor varies too, with PVT. It is for this reason that we have designed the zero-Vt self-biased current source which is a copy of the specific current of the zero-Vt and we have biased all zero-Vt MOSFET used in this topology by the same voltage gate which is V_G. This means that if the zero-Vt as resistor varies, the current reference will vary proportionally to compensate the variation of the zero-Vt MOSFET as resistor, increasing or decreasing the current reference according to the variation of the zero-Vt as resistor. In Fig.62 we have the full schematic of the proposed mobility-compensated time reference. The zero-Vt self-biased current source is shown in chapter 2. The voltage controlled current source in chapter 3 and the current-mode Schmitt trigger is shown in chapter 4. The V_{bias} in Fig.62 is defined in the high swing current mirror section 4.3 and the V_G is defined in chapter 2.

Initially we suppose that M1 is OFF and M2 is ON, thus, the current through M5 is $I_1 + I_2$. This current is mirrored to one of the current comparator input through M6. Since M1 is OFF, the current through M13 and M14 is zero, consequently the capacitor is charged by the current $I_1 + I_2$. The voltage across the capacitor is converted into a current by means of the zero-Vt transistor M16. This current labeled I_c, a copy of I_c will be compared to $I_1 + I_2$ in the current comparator. If $I_c > I_1 + I_2$, the output of the current comparator will switch from high to low, This means that the transistor M1 will turn ON and M2 will turn OFF, the current through M5 is now I_2 and the current through M13 and M14 is $K.I_1$. Thus, the current I_2 is mirrored through M6 to the current comparator input and also to the capacitor node through M7. The capacitor discharges with a rate equal to the current $K.I_1 - I_2$. The capacitor voltage is converted into current I_c by the voltage controlled current source

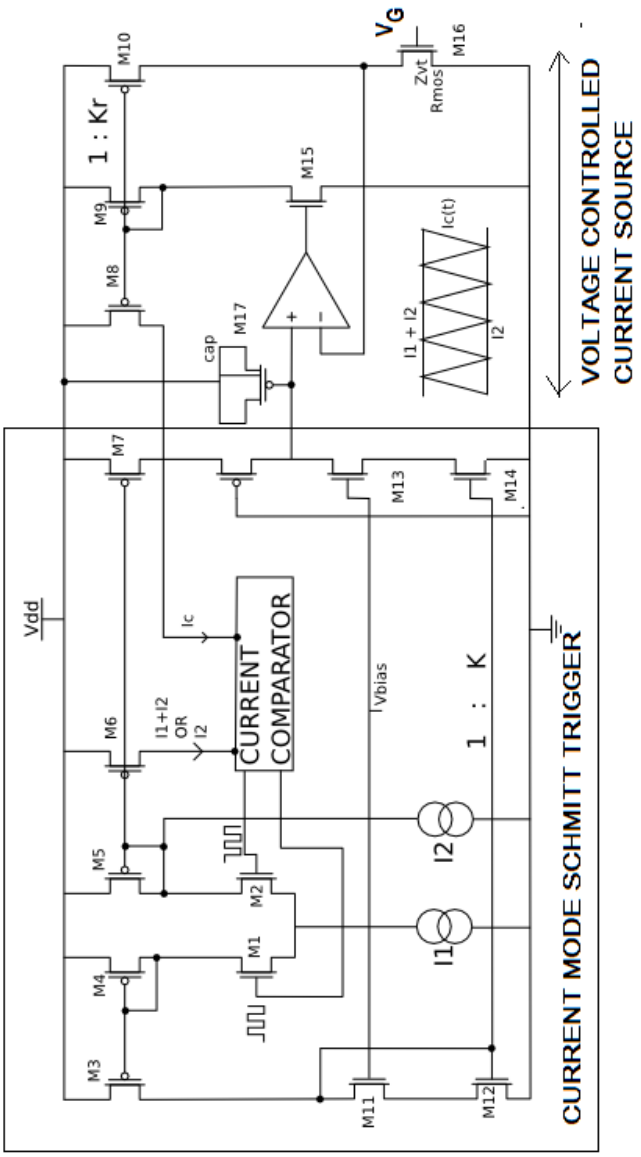

Figure 62 – Full schematic of the proposed mobility-compensated time reference

and compared to I_2. If $I_c < I_2$, the output will switch from low to high.

5.1.1 The MOSFET as a capacitor

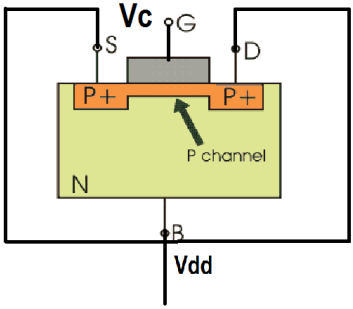

Figure 63 – PMOS device as capacitor

The structure of the MOSFET as a capacitor [49], is shown in Fig.63. In our design, the voltage range of the MOSFET that operates as a capacitor is within V_{C1} and V_{C2} which, in turn, are a function of the charging/discharging currents according to $g_{md9}(V_{C1} - V_{C2}) = I_1$. The value of the V_{C1} must be less than the saturation voltage of the zero-Vt MOSFET, while the capacitor has to operates in a linear region, either the accumulation or the inversion region.

We have plotted the graph C- V_{GB}. In our design we have used a PMOS transistor as a capacitor and biased the bulk with the supply voltage, which is supposed to vary within wide range, from 700mV to 1.8V. We have to guarantee that the capacitor remains in the inversion region, when the supply voltage varies. In the range of operation of the supply voltage in our time reference, the MOS capacitor remains in inversion region. Fig.65 shows the variation of the capacitance with the supply voltage. This simulation was run with the setup of Fig.64.

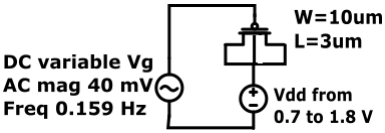

Figure 64 – setup for simulation of the non linear capacitor under different bias bulk level

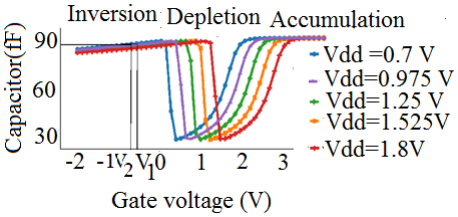

Figure 65 – Oxide capacitance C'_{ox} at different bias voltage

From Fig.65, one can see that for a bulk voltage equal to 700 mV, and a gate voltage equal 100 mV, the gate-bulk voltage will be -600 mV. When the bulk voltage is 1.8 V and the gate voltage at 100 mV the equivalent gate-bulk voltage will be -1.7 V and the MOSFET as capacitor will remain in inversion. The range of operation is shown by V_1 and V_2, where $V_1 - V_2 = 20mV$ as shown Fig.65. Thus, We can conclude that the non linearity observed in Fig,65 does not affect the period of oscillation.

In [49] the value of the MOSFET as capacitance is modeled as:

$$C = K_C.C'_{ox}.W.L \tag{5.1}$$

where in strong inversion and accumulation $K_c \approx 1$.

5.2 MATHEMATICAL MODEL OF THE PROPOSED MOBILITY-COMPENSATED TIME REFERENCE

The capacitor is charged by constant current then we have,

$$V_c = \frac{(I_1 + I_2).T_1}{W.L.C'_{ox}} \tag{5.2}$$

The hysteresis of the current mode Schmitt trigger is I_1. And the resistor in the voltage controlled current source is g_{md16}. Then we have $V_c = \frac{I_1}{gm_{d16}}$, from equation.(5.2),

$$T_1 = \frac{I_1.W.L.C'_{ox}}{(I_1 + I_2).g_{md16}} \tag{5.3}$$

with $g_{md16} = \frac{2.I_S}{\phi_t}(\sqrt{1 + i_{r16}} - 1)$ the non-linear resistor. The charging period can be expressed as,

$$T_1 = \frac{I_1.W.L.C_{ox}^{'}}{(I_1+I_2).\frac{2.I_S}{\phi_t}(\sqrt{1+i_{r16}}-1)} \tag{5.4}$$

where $I_S = \frac{W}{2.L}\mu_n n.C_{ox}^{'}\phi_t^2$ is the specific current of the zero-Vt MOSFET as resitor. The charging period is given by,

$$T_1 = \frac{I_1.W.L.C_{ox}^{'}}{(I_1+I_2).(\frac{W}{L}\mu_n n.C_{ox}^{'}\phi_t)(\sqrt{1+i_{r16}}-1)} \tag{5.5}$$

One can observe that the oscillation period is independent of the oxide capacitance. The period oscillation is given by:

$$T_0 = T_1 + T_2 \tag{5.6}$$

where $T_1 = \frac{T_2}{D}$, T_2 is the discharging period as shown in Fig.60. D is the duty cycle. This duty cycle is given by $D = \frac{I_1+I_2}{K.I_1-I_2}$.

$$T_0 = T_1(D+1) = \frac{(D+1)I_1.L}{(I_1+I_2).(\frac{1}{L}\mu_n n.\phi_t)(\sqrt{1+i_{r16}}-1)} \tag{5.7}$$

After some simplification one can come to the result of the frequency of oscillation,

$$f_0 = [\frac{(K.I_1-I_2)(I_1+I_2)(n(\sqrt{1+i_{r16}}-1))}{I_1^2(K+1).L^2}].\mu_n.\phi_t \tag{5.8}$$

Then we can simplify the frequency of oscillation in two terms, the design parameter $A = \frac{(K.I_1-I_2)(I_1+I_2)(n(\sqrt{1+i_{r16}}-1))}{I_1^2(K+1).L^2}$ and the technology parameter $\mu_n.\phi_t$. And the frequency of oscillation can be reduced to.

$$f_0 = A.\mu_n.\phi_t \tag{5.9}$$

In chapter 2 we have proved that the inversion level of the transistor $M_{2_{zvt}}$ in the zero-Vt self-biased current source is constant with respect to process and temperature variations due to the fact that it is a specific current extractor, then as the transistor zero-Vt M17 used as resistor in the voltage controlled current source is biased by the same voltage gate V_G of the transistor $M_{1_{zvt}}$ and $M_{2_{zvt}}$, Fig.30, one can consider that the reverse inversion level of the transistor M16 in Fig.62 is more or less constant and $i_{r16} \approx i_{f2_{zvt}} \approx i_{r1_{zvt}}$. $i_{f2_{zvt}}$ and $i_{r1_{zvt}}$ represent the forward inversion and the reverse inversion level of M2 and M1 respectively in Fig.30. Therefore the design parameter 'A' is

also independent with process and temperature variations, since we consider that the slope factor is independent with temperature variation.

$$f_0 = [\frac{(K.I_1 - I_2)(I_1 + I_2)(n(\sqrt{1 + i_{f2_{zvt}}} - 1))}{I_1^2(K+1).L^2}].\mu_n.\phi_t \tag{5.10}$$

The variation of the frequency with respect to temperature is,

$$\frac{\delta f_0}{\delta T} = A(\frac{k}{q}.\mu_n + \phi_t.\frac{\delta \mu_n}{\delta T}) \tag{5.11}$$

in chapter 1 we have given some theory about the mobility variation with respect to temperature variation and we can resume that the surface mobility in MOSFET device can be approximated to the mobility of the bulk in high temperature and low field. the bulk mobility is defined as $\mu_n = \mu_0(\frac{T}{T_0})^{-\beta}$ where β is a constant(chapter 1).

After some manipulation of equation(5.11), we have,

$$\frac{\delta f_0/f_0}{\delta T} = \frac{(1-\beta)}{T} \tag{5.12}$$

From equation.(5.12) we can interpret that if $\beta = 1$ the frequency f_0 will be independent of temperature variation. The percent variation of the frequency with respect to temperature is independent of frequency. From equation.(5.12) we can interpret too, that at high temperature the percent variation of the frequency is very small.

5.3 SIMULATION RESULTS

Fig.66 shows the layout of the proposed mobility-compensated time reference, where the total area is approximately 0.01 mm^2. without output buffer.

Fig.67 shows the output simulation of the mobility-compensated time reference and Fig.68, shows the layout and the bonding diagram of the chip. The triangular waveform is the output of the capacitor. The output of the CMST shows the width of the hysteresis, which is close to 25 mV in simulation. The period of oscillation is close to 32 kHz. The Monte Carlo simulation for 247 samples resulted in the histogram shown in Fig.69 with a mean value of 32,5 kHz and a standard deviation of 2.33 kHz. This standard deviation is due to the mismatch in the current mirror and differential pair.

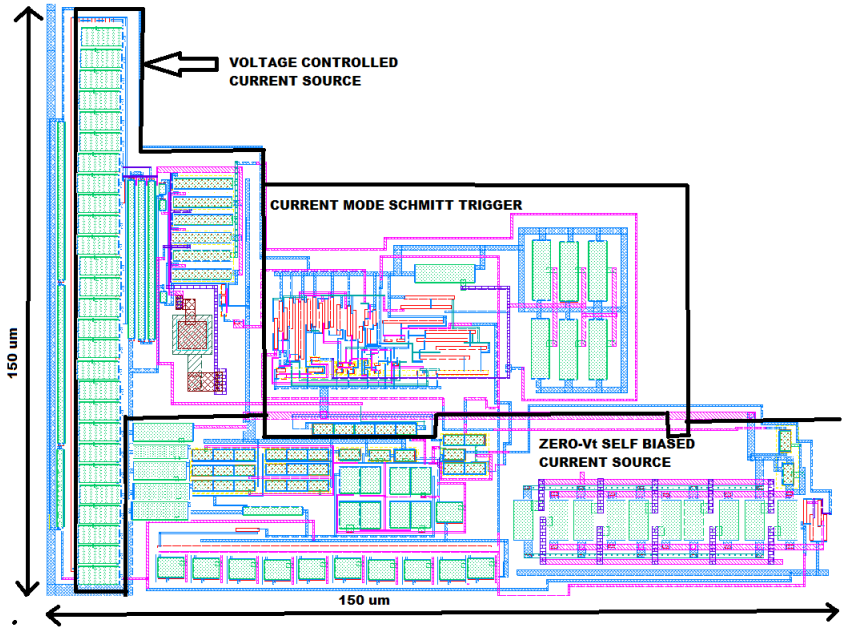

Figure 66 – Layout of the proposed time reference

5.4 TEST AND MEASUREMENT RESULTS

The proposed time reference was designed in the 180 nm bulk CMOS technology under the MPW (MultiProject Wafer) program by the MOSIS service. We received 40 integrated circuits (ICs). In each ICs we have 8 oscillators, with the goal to check the process variation in the same die and process variation in different dies. Fig.70 shows the die photo of the chip. Fig.71 shows the setup of the measurement system, in which the prototype ICs is placed in a PCB and supplied by a voltage source.

To access the DC transfer characteristic, which is the hysteresis, of the fabricated oscillator we have applied the DC voltage at the input of the voltage controlled current source. This voltage varies from 70 mV to 280 mV,

The DC transfer characteristic of the current mode Schmitt trigger is shown in Fig.72. This measurement was done using Agilent precision instrument analyzer 4156C. Fig.72 shows a hysteresis width which is in turn of 17 mV, the calculated hysteresis width is 20 mV, this is a offset voltage in turn of

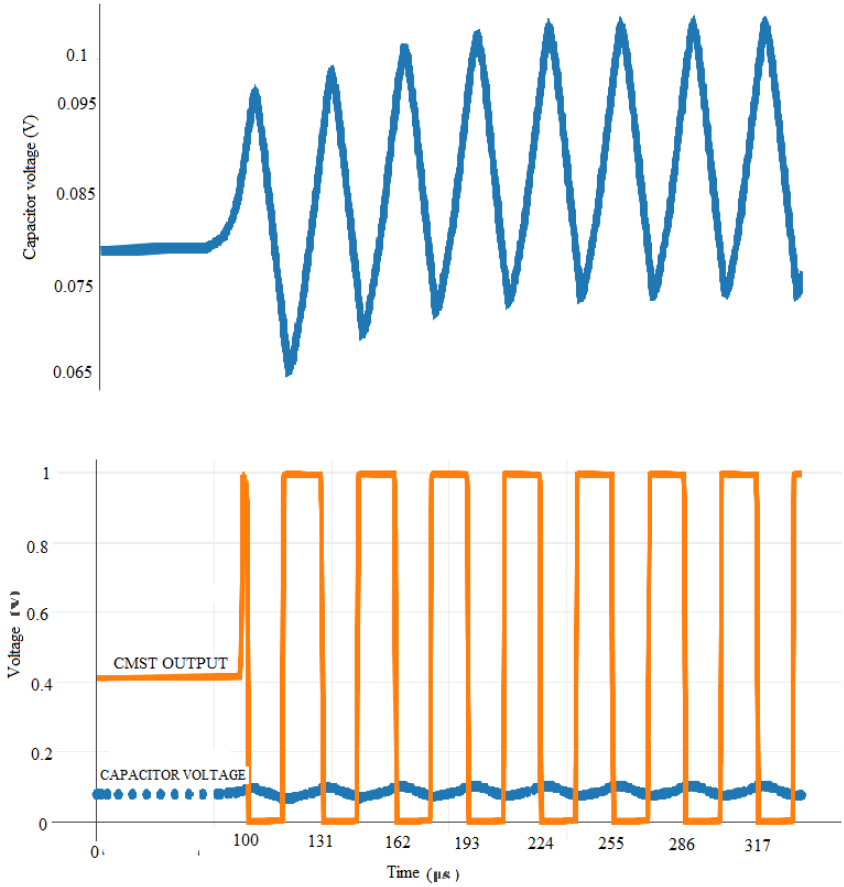

Figure 67 – Simulation result of the proposed time reference : the triangular waveform is the capacitor voltage and rectangular wave form is the output of the CMST, for Vdd = 1 V Temp = 27°C

3 mV, this offset voltage is due to mismatch in differential pair and/or current mirror.

We have tested a total of 280 circuits (8 circuits in 35 ICs). The range of the output frequency was from 29 kHz to 34kHz. Fig.73 shows the frequency variation versus percentage of the total number of tested oscillator with a supply voltage of 1 V. From this figure one can observe that more than 20% of all the tested oscillators are accurate. The lower value of frequency is

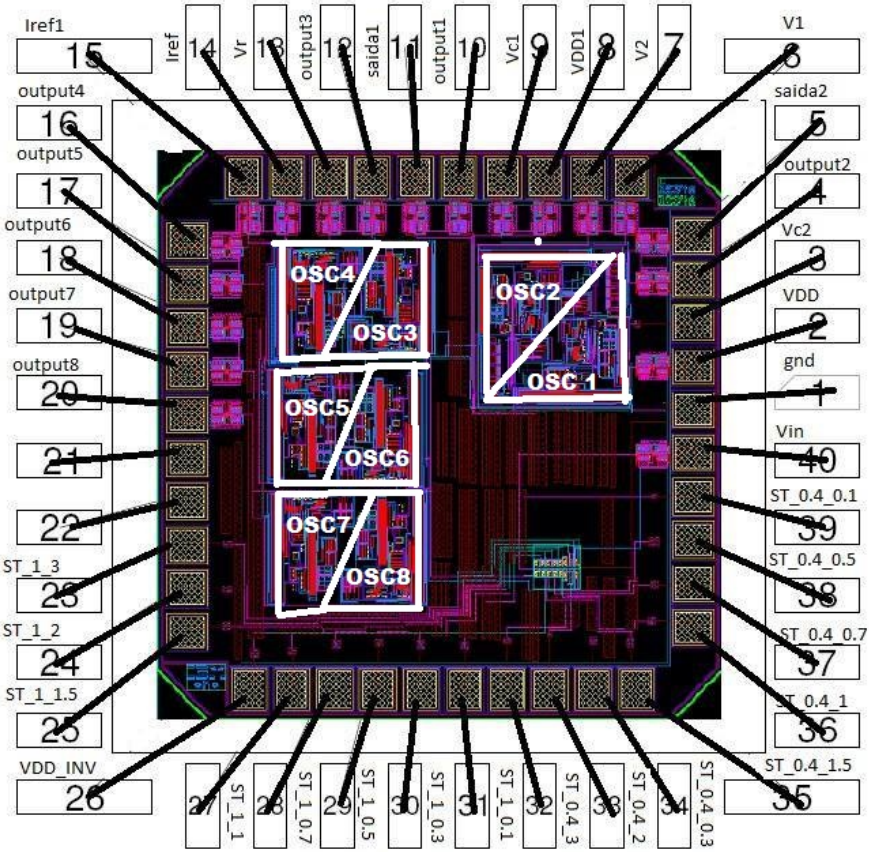

Figure 68 – Layout and the bonding diagram of the proposed time reference

around 29 kHz and the higher value is around 34 kHz, this is due to mismatch and process variation.

Fig.74 shows the output waveform of the device under test, for a supply voltage equal to 1V and temperature 20°C. We can interpret that from the standard deviation measurement over time of 0 value, ascertain about preciseness and stability of this oscillator. The oscilloscope used in measurement has a large bandwidth of 2 GHz. As oscilloscopes are broadband measurement instruments, the higher the bandwidth of the scope, the higher will be the vertical noise.

Therefore another set of measurement was done using a low band-

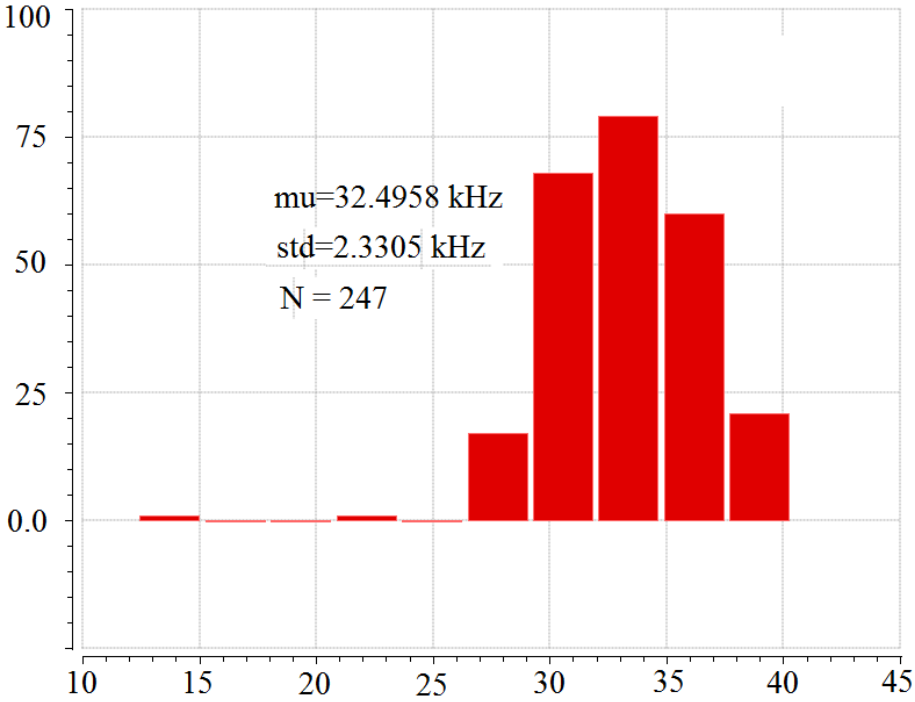

Figure 69 – Monte Carlo Simulation for the proposed mobility-compensated time reference

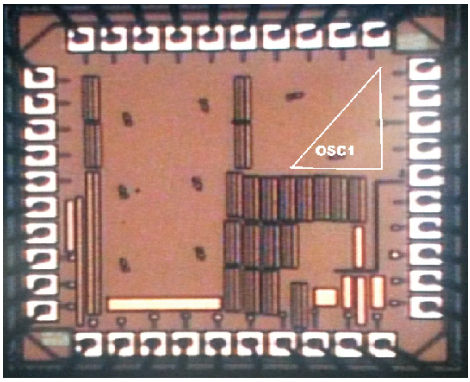

Figure 70 – Die photo of the time reference

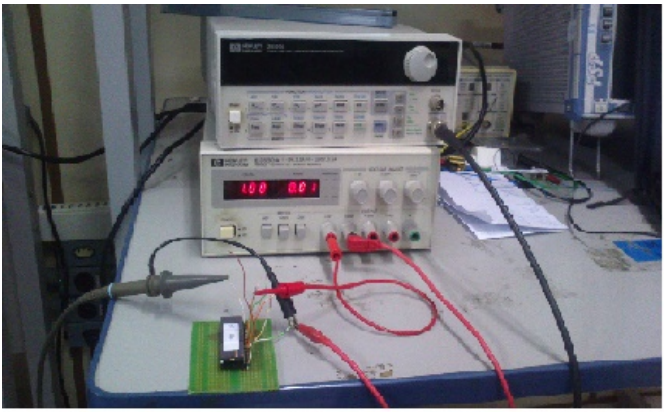

Figure 71 – Device under test

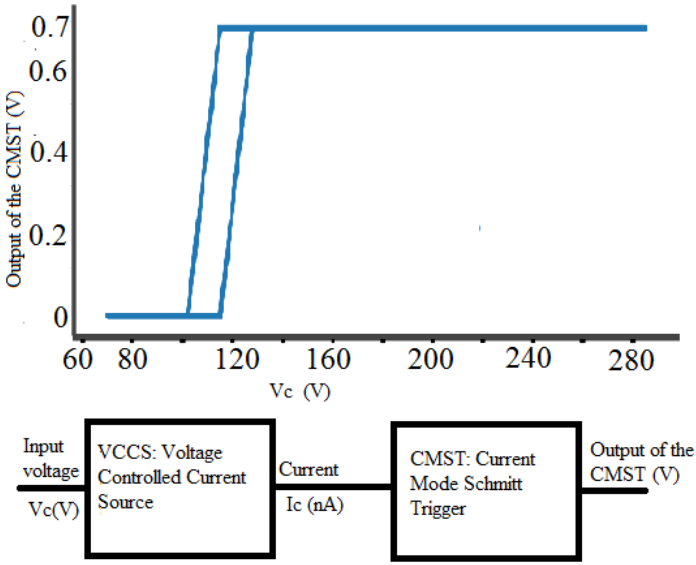

Figure 72 – (a)Experimental result of the hysteresis in the current mode schmitt trigger with Vdd= 700 mV and T = 20 °C (b) Block diagram of the setup of the measurement

width (300 MHz, 9 bit resolution) digital oscilloscope namely, *Tektronix*® TDS3032B. The use of this oscilloscope to measure the response of oscillator

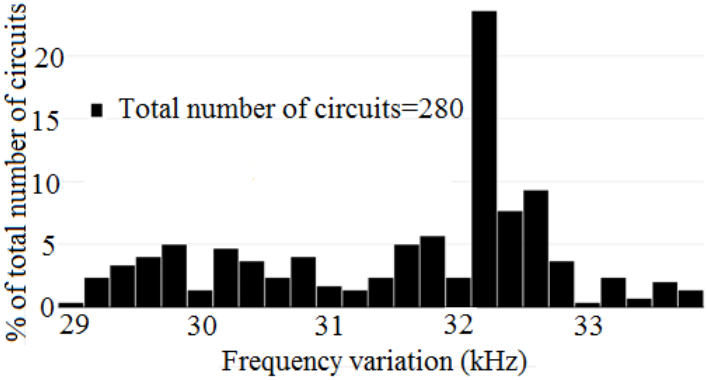

Figure 73 – Results of all the thirty five prototype chips (eight oscillator per die)

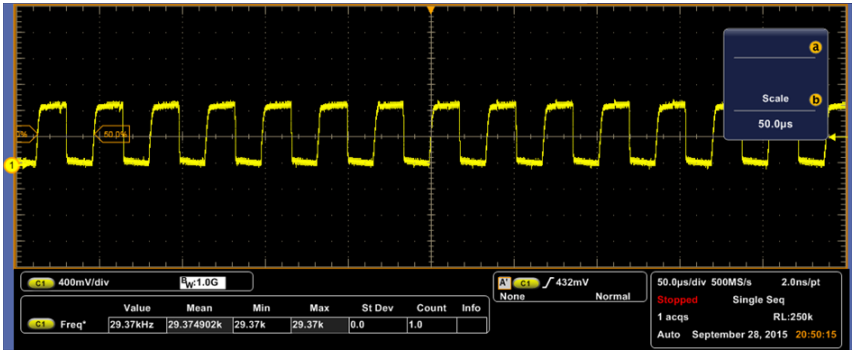

Figure 74 – The output measurement result of one of the oscillator. Vdd = 1 V , Temp = 20 °C, using *Tektronix*® DPO 52000.

shows that, the amplitude noise in the waveform is considerably reduced. The result of one such measurement is shown in Fig.75.

5.4.1 Variation of oscillation frequency with supply voltage

We have varied the supply voltage from 0.7 V - 1.8 V, to test the dependence of the frequency with the supply voltage. Fig.76, shows the oscillation frequency for different oscillators in the same die. The minimum variation

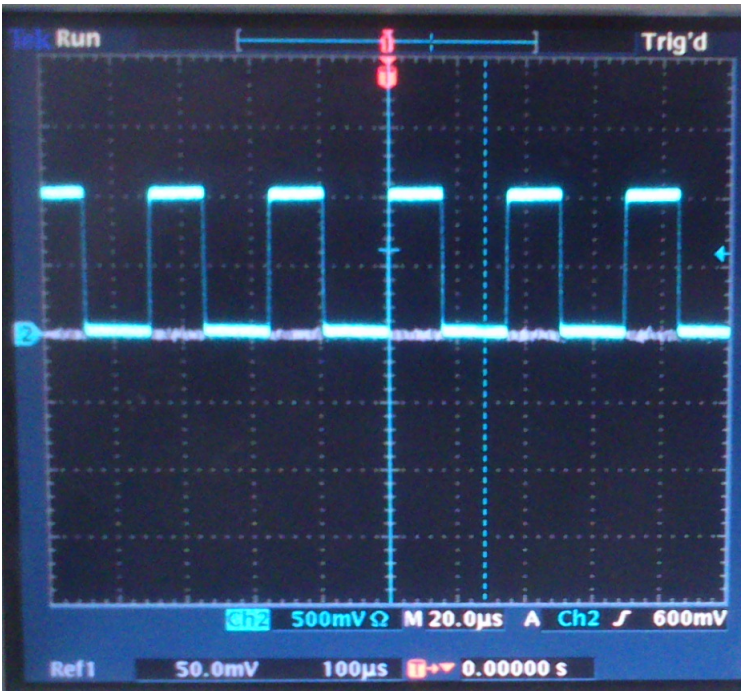

Figure 75 – The output of one of device which is accurate, precise and stable, in horizontal scale each division correspond to 20 μs and in vertical scale each division correspond to 500 mV, Vdd = 1 V, T = 20 °C.

that we got with supply voltage variation is 0.05 %/V, with the above range of the supply voltage and the maximum is 0.7%/V.

Table 5 – Current consumption of the time reference at Vdd = 1 V and T = 20 °C (Internal temperature of the Lab environment)

BLOCKS	POWER
SELF BIASED CURRENT SOURCE	42 nW
VOLTAGE CONTROLLED CURRENT SOURCE	40 nW
CURRENT MODE SCHMITT TRIGGER	70 nW
Total	152 nW

The table5 shows the total current consumption at supply voltage 1 V and temperature 20°C. The bias voltage V_G of the zero-Vt as resistor M16

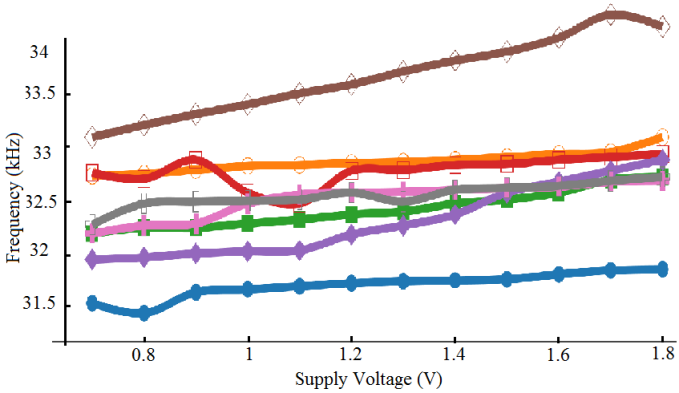

Figure 76 – Result of the supply voltage variation from 700 mV to 1.8V for all height circuits in one die,(each die contains height relaxations oscillators)

in Fig.62 varies with the supply voltage. This means that at different supply voltage the equivalent transconductance of the transistor M16 could vary and this affects the oscillation period. This is the main reason of the variation of the oscillation with the supply voltage. But this variation is in turn on 0.1 % and present in simulation a total variation of the oscillation period of 0.02%/V. In test and measurement result we got a total variation of 0.05%/V for the good case and the worst case 0.7%/V.

5.4.2 Temperature variation

To test the oscillator response with respect to (i.e., w.r.t) temperature, we have varied the temperature from -20 °C to 80 °C. This test was done using a thermal chamber, and the response was observed on an oscilloscope. Throughout the test we have used a supply voltage of 1 V; the setup is shown in Fig.77. The variation of frequency response w.r.t., temperature is shown in Fig.78. We tested 5 oscillators from different dies. The minimum variation in the range of -20 °C to 80 °C, is around 30 ppm/°C and the maximum variation is 90 ppm/°C. At temperatures $>$ 40°C, the frequency is stable with respect to temperature variation.

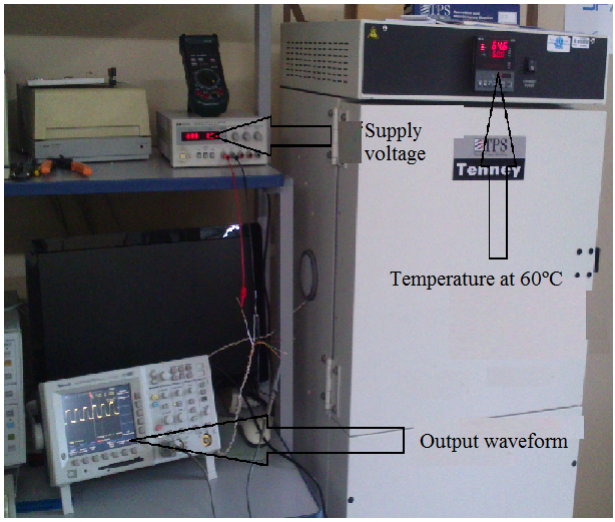

Figure 77 – Temperature variation setup for device under test

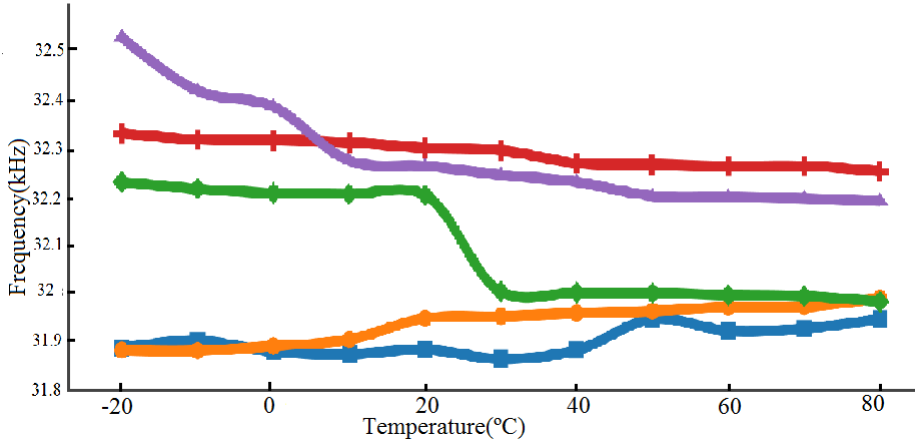

Figure 78 – Oscillation frequency versus temperature variation from -20 °C to 80 ° C for five different dies.

5.4.3 Short term noise analysis

For short term noise analysis, we have used the jitter as the criterion to characterize the oscillator. Typically, in commercial crystal oscillators, at 32

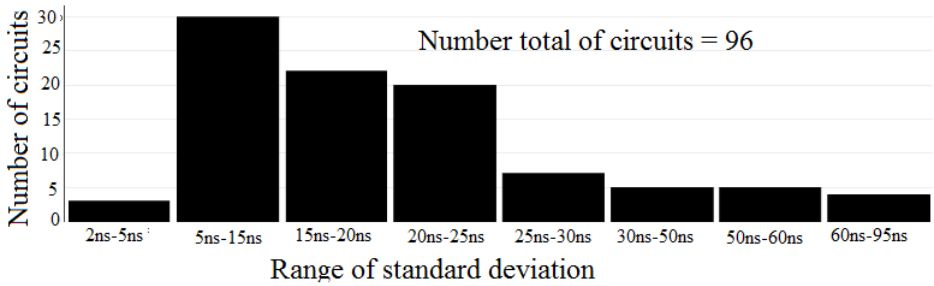

Figure 79 – Histogram of the distribution of the jitter for 96 oscillators

kHz there is a jitter of 100 ps [50] . We have tested 96 oscillators for jitter, and the distribution of the standard deviation of the jitter is shown in Fig.79. the jitter in the case of the smallest deviation of 2 ns which is 66 ppm is shown in Fig.80.

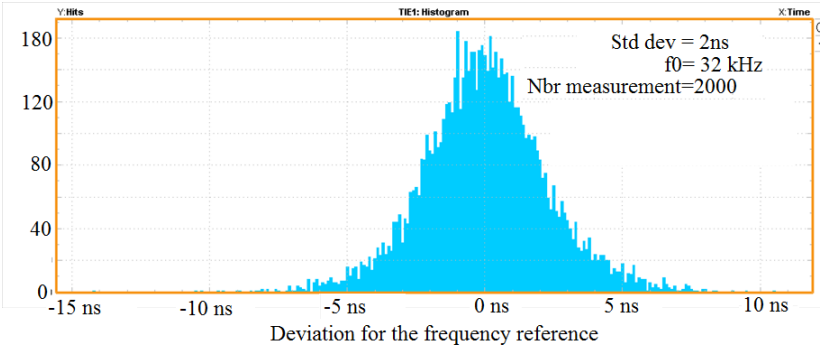

Figure 80 – Jitter measurement using *Tektronix*® DPO series 52000

5.4.4 Long term analysis

The standard deviation does not provide a direct way to distinguish types of noise or variation and thus to distinguish sources or causes of measurement variability it is used the Allan deviation. Then the Allan deviation inherently provides a measure of the behavior of the variability of a quantity, as it is averaged over different measurement time periods, which allows it to

directly quantify and to simply differentiate between different types of signal variation. Long term stability was analyzed using Allan deviation. An introduction to Allan deviation is presented in appendix B. The Allan variance or Allan deviation basically defines two types of noise which can increase or decrease the frequency drift over time,

- White noise process: White phase noise and White frequency noise falls in this type
- Flicker noise process : Flicker phase noise and Flicker frequency noise falls in this type

Fig.81 shows the Allan deviation of one of the time reference after 3 hours of test. One can interpret that after 100 ms the Allan deviation in part-per-million (ppm) is less than 500 and after 10 s is less than 20. And also in Fig.81, the Allan deviation plot shows that our time reference will be affected by the white noise process on the short term. But, on long term, the flicker noise process will affect the time reference and its value after 100 ms is 500 ppm and fall to 20 ppm after 10 seconds.

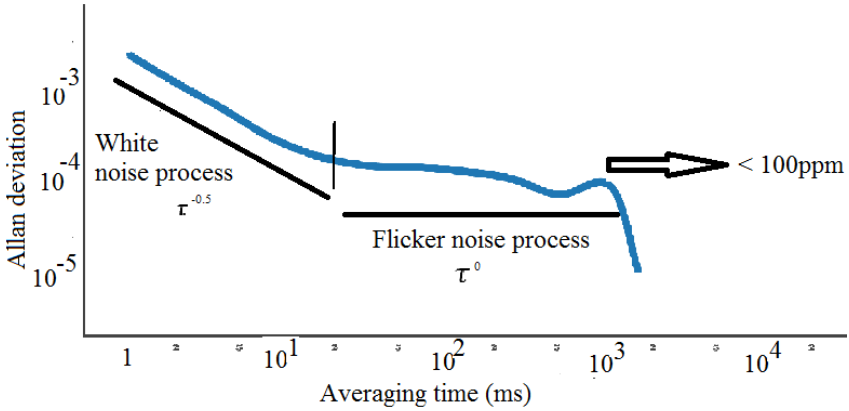

Figure 81 – Allan deviation plot for three hours run of device under test.

In Table6 we have compared our work with the work reported in literature, according to standard specifications. The main problem in literature is that generally the result of only one oscillator is reported in relation to supply voltage and temperature variation, And many of the relaxation oscillator does not show the study of the jitter. Our design shows a good stability with supply voltage variation (500 ppm/V) compared to others works in literature.

the temperature accuracy is turn on 0.3% with 152 nW of power consumption and only 66 ppm of jitter.

NI = Not Informed

Table 6 – Summary of measured result and comparison to previous work

Prev work	Process(nm)	Area (mm^2)	Freq (kHz)	Power (μW)	Temp Acc(%)	Temp range °C	Voltage accuracy(ppm/V)	Jitter(ppm)
[23]ISSCC'13	65	0.032	18.5	0.12	+/-0.25	-40 to 90	10000 ppm/V	NI [1]
[25] ESSCIRC'08	65	0.11	100	20.8	+/-1.1	-22 to 85	23000 ppm/V	NI
[51]VLSI'12	90	0.12	10^2	0.28	+/-0.68	-40 to 90	57000 ppm/V	NI
[52]ISSCC'09	180	0.04	14.10^3	45	+/-0.19	-40 to 125	16000 ppm/V	NI
[53]ISSCC'11	130	0.01	$3.7.10^{-4}$	0.00066	+/-0.14	-20 to 60	4700 ppm/V	2000
[54]VLSI'12	60	0.048	32.7	4.48	+/-0.1	-20 to 100	600 ppm/V	NI
[55]ISSCC'09	130	0.073	3200	38.2	+/-0.25	20 to 60	40000 ppm /V	NI
[56]ISSCC'10	180	0.016	31.25	0.36	+/-0.4	NI	50000 ppm /V	NI
This work	180	0.1	32	0.15	+/-0.3	-20 to 80	500 ppm/V	66

6 CONCLUSION

This final chapter presents a summary of the main findings of this work and a short overview of the possible applications and research topics originating from this work that could be investigated in the future.

6.1 MAIN RESULT

- Low-doping MOSFET used as resistor shows a small variation with process and temperature variation when compensated by thermal voltage, compared to a standard MOSFET. In the proposed time reference the use of the zero-Vt self-biased current source allows to generate some current source which in turn has the same PVT variation with the zero-Vt MOSFET used as resistor. This allows that we can track the variation of the MOSFET as resistor. Thus, the variation of zero-Vt as resistor does not affect our time reference.

- Mobility-Compensated time reference can be used as time reference in some range of temperature (30 ppm /°C) and wide range of supply voltage with 66 ppm of Jitter. At high temperature (Temp $\geq$ 27 °C), the proposed time reference is stable and precise, due to the fact that the mobility is stable at high temperature. The long term study with Allan variance shows some 500 ppm variation due to white noise process at long term. Thus, the proposed time reference could be used in place of crystal oscillators in applications where only precision and stability are required(e.g Clock for power management).

- Used a current comparator, instead of voltage comparator in relaxation oscillator, can allow to track the PVT variation of the current reference and consequently produce more stable frequency, and achieve some precise time reference.

6.2 FUTURE WORK

We can improve the performance of the relaxation oscillator in relation to mismatch, temperature and jitter. To increase the performance in relation to mismatch we have to increase the total area in the voltage controlled current source and the high swing current mirror. To increase the performance in relation to the short term stability, it will be necessary to increase the power

consumption, this will reduce the jitter. One problem in the design of the relaxation oscillator using a current comparator, is that he has a few publications of current comparator with good performance in literature. Then, it is necessary to improve the topology of the current comparator to achieve, high speed and small input current resolution, which can work also at low supply voltage without a dead zone.

APPENDIX A – Advanced Compact Model

Main equation using Advanced Compact Model (ACM):

$$I_D = I_F - I_R \tag{A.1}$$

I_D is the drain-source current, I_F is the forward current and I_R is the reverse current.

$$I_F = I_S.i_f \tag{A.2}$$

$$I_R = I_S.i_r \tag{A.3}$$

I_S is the specific current, i_f is the forward inversion level, i_r is the reverse inversion level.

$$I_D = I_S(i_f - i_r) \tag{A.4}$$

Unified Charge Control Model (UCCM)

$$V_{pi} - V_{sbi} = \phi_t(\sqrt{1+i_{fi}} - 2 + ln(\sqrt{1+i_{fi}} - 1)) \tag{A.5}$$

$$V_{pi} - V_{dbi} = \phi_t(\sqrt{1+i_{ri}} - 2 + ln(\sqrt{1+i_{ri}} - 1)) \tag{A.6}$$

where $V_{pi} = \frac{V_{gbi} - V_{th}}{n}$ is the pinch-off voltage, $V_t h$ is the threshold voltage. n is the slope factor.

$$gm_s = \frac{2.I_S}{\phi_t}(\sqrt{1+i_{fi}} - 1)) \tag{A.7}$$

$$gm_r = \frac{2.I_S}{\phi_t}(\sqrt{1+i_{ri}} - 1)) \tag{A.8}$$

gm_s and gm_r are transconductance related to the source and the drain respectively.

APPENDIX B – Figure of Merit of the oscillator as time reference

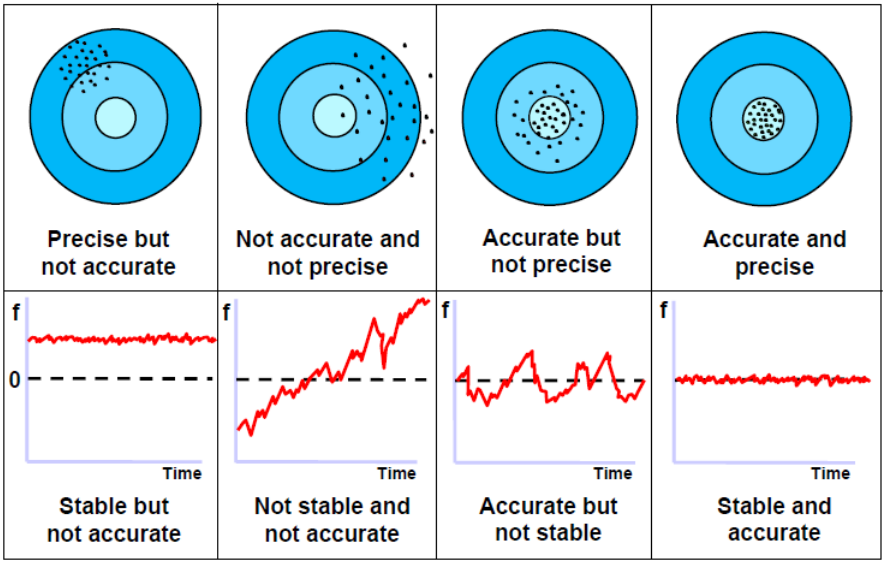

Figure 82 – Illustration of Precision-Stability-Accuracy

The FOM used in this work is divided in, 1 Accuracy, 2 Stability, 3 Precision. Fig.82 illustrates the accuracy, precision and stability that we will discuss in the next section.

B.1.1 Accuracy

Accuracy is the degree of conformity of a measured or calculated value to its definition. Accuracy is also related with the offset from an ideal value. For example, a time offset is the difference between a measured on-time pulse and an ideal on-time pulse. Frequency offset is the difference between a measured frequency and an ideal frequency with zero uncertainty as shown in equation.B.1. This ideal frequency is called the nominal frequency. In this work this nominal value is 32 kHz.

$$f_{offset} = \frac{f_{measured} - f_{nominal}}{f_{nominal}} \tag{B.1}$$

This frequency offset is defined in part-per million this is

$$\alpha = f_{offset} x 10^6 (ppm) \tag{B.2}$$

B.1.2 Precision

Precision is the random uncertainty of a measured value, expressed by the standard deviation or by a multiple of the standard deviation. Then we can say that the accuracy is the closeness of the agreement between the result of a measurement and a true value.

B.1.3 Stability

Stability indicates how well an oscillator can produce the same time or frequency offset over a given time interval, it doesn't indicate whether the time or frequency is "right" or "wrong". Stability and accuracy are two different terms because, accuracy indicates how well an oscillator has been set on time or on frequency. To understand this difference, consider that a stable oscillator that needs adjustment might produce a frequency with a large offset. Or an unstable oscillator that was just adjusted might temporarily produce a frequency near its nominal value. Fig.82 shows the relationship between accuracy and stability.

Stability can be divided into: 1. Short-term stability that refers to fluctuations over intervals less than 100 s. and 2. Long-term stability usually refers to measurement intervals greater than 100 s, but for robust behavior it should be greater than 1 day for an oscillator [57].

Mathematically stability is defined as the statistical estimate of the frequency or time fluctuations of a signal over a given time interval. These fluctuations are measured with respect to a mean frequency or time offset as shown in equation.(B.1). Stability estimates can be made in either the frequency domain or time domain, and can be calculated from a set of either frequency offset or time interval measurements. In some fields of measurement, stability is estimated by taking the standard deviation of the data set. However, standard deviation only works with stationary data, where the results are time independent, and the noise is white, meaning that it is evenly distributed across the frequency band of the measurement. Oscillator data is usually non-stationary, since it contains time dependent noise contributed by the frequency offset. With the stationary data, the mean and standard deviation will converge to a particular value. As more measurements are made

with non-stationary data, the mean and standard deviation never converge to any particular value. Instead, there is a moving mean that changes each time we add a measurement. For these reasons, a non-classical statistic like Allan variance can be used to estimate long term stability in the time domain. The Allan variance is a two-sample variance formed by the average of the squared differences between successive values of a regularly measured quantity taken over sampling periods from the measuring interval up to half the maximum measurement time. But since it is the square root of the variance, its proper name is the Allan deviation. The equation of Allan deviation is,

$$\sigma_f(\tau) = \sqrt{\frac{1}{2.(M-1)} \Sigma_{i=1}^{M-1} (f_{i+1} - f_i)^2} \tag{B.3}$$

M is the number of sample and f_i is the frequency at the time τ_i. The stability is again divided in two parts: long term stability and short term stability.

Also, standard deviation does not provide a direct way to distinguish types of noise or variation, and thus to distinguish sources or causes of measurement variability, we can use the Allan deviation. Because Allan deviation can measure the behavior of the variability of a quantity over different measurements of time period, which allows it to directly quantify and differentiate between different types of signal variation, [57], [58].

LIST OF FIGURES

LIST OF TABLES

REFERÊNCIAS BIBLIOGRÁFICAS

1 L. Han and N. Hua, “A Distributed Time Synchronization Solution without Satellite Time Reference for Mobile Communication”, *IEEE Communications Letters*, vol. 17, no. 7, pp. 1447 - 1450, Jul. 2013.

2 J.-L. Ferrant, M. Gilson, S. Jobert, M. Mayer, L. Montini, M. Ouellette, S. Rodrigues, and S. Ruffini, “Synchronous Ethernet and IEEE 1588 in Telecoms”, May 2013.

3 mccorquodale, “CMOS challenge quartz”, 21-Mar-2006. [Online]. Available: *www.ewh.ieee.org/r7/toronto/chapters/ssc/mccorquodaleUToronto*09.*pdf*. [Accessed: 26-Oct-2015]

4 K. Clarke, “Wien bridge oscillator design”, Proceedings of the IRE, vol. 41, no. 2, pp. 246 - 249, Feb. 1953.

5 ”CrystalOscillators.pdf”,[Online]. Available: *http* : *//kunz* − *pc.sce.carleton.ca/thesis/CrystalOscillators.pdf*. [Accessed: 28-Oct-2015].

6 Jauch Quartz GmbH, “Quartz Crystal Theory”, www.jauch.de/. [Online]. [Accessed: 28-Oct-2015].

7 CITIZEN FINETECH MIYOTA CO., “Cutting direction and frequency Temperature characteristics, CITIZEN FINETECH MIYOTA CO.,LTD.” [Online]. Available: *http* : *//cfm.citizen.co.jp/english/product/cvo*$_c$*haracter.html*. [Accessed: 09-Oct-2015].

8 MICAS, “Crystal oscillator design”, http://iroi.seu.edu.cn, 2008. [Online]. Available: http://iroi.seu.edu.cn/teachers/chym/analog/22.pdf. [Accessed: 12-Oct-2015].

9 “Fastest Wireless On-ramp to the Internet of Things”, 10-Aug-2015. [Online]. Available: http://www.silabs.com. [Accessed: 09-Oct-2015].

10 H. C. Nathanson and R. A. Wickstrom, “A resonant-gate silicon surface transistor with high-Q band-pass properties”, *Applied Physics Letters*, vol. 7, no. 4, p. 84, 1965.

11 M. Sadiku, “MEMS”, *IEEE Potentials*, vol. 21, no. 1, pp. 4-5, 2002.

12 S. Tabatabaei and A. Partridge, “Silicon MEMS Oscillators for High-Speed Digital Systems”, *IEEE Micro*, vol. 30, no. 2, pp. 80?89, Mar. 2010.

13 Si-Time, “MEMS replacing Quartz oscillator Application note”, 2009. [Online]. Available: www.sitime.com. [Accessed: 02-Oct-2015].

14 M. Lutz, A. Partridge, P. Gupta, N. Buchan, E. Klaassen, J. McDonald, and K. Petersen, “MEMS Oscillators for High Volume Commercial Applications”, TRANSDUCERS 2007 - 2007 International Solid-State Sensors, Actuators and Microsystems Conference, 2007.

15 D. Ruffieux, F. Krummenacher, A. Pezous, and G. Spinola-Durante, “Silicon Resonator Based 3.2 μW Real Time Clock With 10 ppm Frequency Accuracy”, IEEE Journal of Solid-State Circuits, vol. 45, no. 1, pp. 224-234, Jan. 2010.

16 Perrott MH, “A low-area switched-resistor loop-filter technique for fractional-N synthesizers applied to a MEMS based programmable oscillator”, IEEE international solidstate circuits conference, ISSCC, 2010.

17 IDT, “IDT data sheets of MM8102, MM8103, and MM8103”, IDT product, 2014. [Online]. Available: http://www.idt.com. [Accessed: 09-Oct-2015].

18 A. Hajimiri and T. H. Lee, “Design issues in CMOS differential LC oscillators”, IEEE Journal of Solid-State Circuits, vol. 34, no. 5, pp. 717-724, May 1999

19] M. Zannoth, B. Kolb, J. Fenk, and R. Weigel, “A fully integrated VCO at 2 GHz”, 1998 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, ISSCC. First Edition (Cat. No.98CH36156), 1998.

20 D. Griffith, P. T. Roine, J. Murdock, and R. Smith, “17.8 A 190nW 33kHz RC oscillator with +/-0.21% temperature stability and 4ppm long-term stability”, 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), Feb. 2014.

21 Y. Lu, G. Yuan, L. Der, W.-H. Ki, and C. P. Yue, "A 0.5% Precision On-Chip Frequency Reference With Programmable Switch Array for Crystal-Less Applications", IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 60, no. 10, pp. 642-646, Oct. 2013.

22 U. Denier, "Analysis and Design of an Ultralow-Power CMOS Relaxation Oscillator", IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 57, no. 8, pp. 1973-1982, Aug. 2010.

23 A. Paidimarri, D. Griffith, A. Wang, A. P. Chandrakasan, and G. Burra, "A 120nW 18.5kHz RC oscillator with comparator offset cancellation for +/-0.25% temperature stability", 2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers, Feb. 2013.

24 Y.-H. Chiang and S.-I. Liu, "A Submicrowatt 1.1-MHz CMOS relaxation oscillator with temperature compensation", IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 60, no. 12, pp. 837-841, Dec. 2013.

25 F. Sebastiano, L. Breems, K. M. S. Drago, D. Leenaerts, and B. Nauta, "A low-voltage mobility-based frequency reference for crystal-less ULP radios", ESSCIRC 2008 - 34th European Solid-State Circuits Conference, Sep. 2008.

26 S. A. Mujtaba, "Advanced mobility models for design and simulation of deep submicrometer MOSFETs", PHD, STANFOR UNIVERSITY

27 F. Gamiz, J. A. Lopez-Villanueva, J. B. Roldan, and J. E. Carceller, "Influence of the doping profile on electron mobility in a MOSFET", IEEE Transactions on Electron Devices, vol. 43, no. 11, pp. 2023-2025, 1996.

28 S. Reggiani, M. Valdinoci, L. Colalongo, M. Rudan, G. Baccarani, A. D. Stricker, F. Illien, N. Felber, W. Fichtner, and L. Zullino, "Electron and hole mobility in silicon at large operating temperatures. I. bulk mobility", IEEE Transactions on Electron Devices, vol. 49, no. 3, pp. 490-499, Mar. 2002.

29 S. Reggiani, M. Valdinoci, L. Colalongo, M. Rudan, and G. Baccarani, "An Analytical, Temperature-dependent model for majority- and minority-carrier mobility in silicon devices", VLSI Design, vol. 10, no. 4, pp. 467-483, 2000.

30 N. D. Arora, J. R. Hauser, and D. J. Roulston, “Electron and hole mobilities in silicon as a function of concentration and temperature”,IEEE Transactions on Electron Devices, vol. 29, no. 2, pp. 292-295, Feb. 1982.

31 M. S. McCorquodale, S. M. Pernia, S. Kubba, G. Carichner, J. D. O?Day, E. Marsman, J. Kuhn, and R. B. Brown, “A 25MHz all-CMOS reference clock generator for XO-replacement in serial wire interfaces”, 2008 IEEE International Symposium on Circuits and Systems, May 2008.

32 K. K. Lee, K. Granhaug, and N. Andersen, “A study of low-power crystal oscillator design”, 2013 NORCHIP, Nov. 2013.

33 E. M. Camacho-Galeano, C. Galup-Montoro, and M. C. Schneider, “A 2-nW 1.1-V self-biased current reference in CMOS technology”, IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 52, no. 2, pp. 61-65, Feb. 2005.

34 M. C. Schneider and C. Galup-Montoro, “CMOS analog design Using all-Region MOSFET modeling”, -Infinity, 2010.

35 D. A. Freitas and K. W. Current, “CMOS current comparator circuit”, Electronics Letters, vol. 19, no. 17, p. 695, 1983.

36 H. Traff, “Novel approach to high speed CMOS current comparators”, Electronics Letters, vol. 28, no. 3, p. 310, 1992.

37 A. El Gamal and H. Eltoukhy, “CMOS image sensors”, IEEE Circuits and Devices Magazine, vol. 21, no. 3, pp. 6-20, May 2005.

38 R. Fontaine, “Recent innovations in CMOS image sensors”, 2011 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, May 2011.

39 D. McCarthy, S. O?Keeffe, E. Lewis, D. G. Sporea, A. Sporea, I. Tiseanu, P. Woulfe, and J. Cronin, “Radiation dosimeter using an extrinsic fiber optic sensor”, IEEE Sensors Journal, vol. 14, no. 3, pp. 673-685, Mar. 2014.

40 R. Sridhar, N. Pandey, V. Bhatia, and A. Bhattacharyya, “On improving the performance of Traff’s comparator”, 2012 IEEE 5th India International Conference on Power Electronics (IICPE), Dec. 2012.

41 C. B. Kushwah, D. Soni, and R. S. Gamad, "New Design of CMOS Current Comparator", 2009 Second International Conference on Emerging Trends in Engineering & Technology, 2009.

42 L. Ravezzi, D. Stoppa, and G.-F. Dalla Betta, "Simple high-speed CMOS current comparator", Electronics Letters, vol. 33, no. 22, p. 1829, 1997.

43 O. Oliaei, P. Loumeau, and H. Recoules, "A class AB current comparator", Proceedings of 40th Midwest Symposium on Circuits and Systems, 1998.

44 G. Palmisano and G. Palumbo, "High performance CMOS current comparator design", IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 43, no. 12, pp. 785-790, 1996.

45 D. Banks and C. Toumazou, "Low-power high-speed current comparator design", Electronics Letters, vol. 44, no. 3, p. 171, 2008.

46 P. Silapan and M. Siripruchyanun, "A simple current-mode Schmitt trigger employing only single MO-CTTA", 2009 6th International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology, May 2009.

47 T. Srivyshnavi and A. Srinivasulu, "A current mode Schmitt trigger based on Current Differencing Transconductance Amplifier", 2015 3rd International Conference on Signal Processing, Communication and Networking (ICSCN), Mar. 2015.

48 S. G. Shankar and A. M. Shariz, "Current-mode electronically-tunable Schmitt Trigger using single 65nm +/-0.75V CMOS CDTA", pp. 137-141, Jul. 2013.

49 C. Galup-Montoro and M. C. Schneider, "Mosfet Modeling For Circuit Analysis And Design". Singapore: World Scientific, 2007.

50 Stmicroelectronics, "www.st.com", [Online]. Available: http://www.st.com/web/en/resource/technical/document/datasheet/CD00162498. [Accessed: 03-Nov-2015].

51 T. Tokairin, K. Nose, K. Takeda, K. Noguchi, T. Maeda, K. Kawai, and M. Mizuno, "A 280nW, 100kHz, 1-cycle start-up time, on-chip

CMOS relaxation oscillator employing a feedforward period control scheme", 2012 Symposium on VLSI Circuits (VLSIC), Jun. 2012.

52 Y. Tokunaga, S. Sakiyama, A. Matsumoto, and S. Dosho, "An on-chip CMOS relaxation oscillator with power averaging feedback using a reference proportional to supply voltage", 2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers, Feb. 2009.

53 Y. Lee, B. Giridhar, Z. Foo, D. Sylvester, and D. Blaauw, "A 660pW multi-stage temperature-compensated timer for ultra-low-power wireless sensor node synchronization", 2011 IEEE International Solid-State Circuits Conference, Feb. 2011.

54 K.-J. Hsiao, "A 32.4 ppm/C 3.2-1.6V self-chopped relaxation oscillator with adaptive supply generation", 2012 Symposium on VLSI Circuits (VLSIC), Jun. 2012.

55 K. Choe, D. Nuttman, and O. D. Bernal, "A Precision Relaxation Oscillator with a Self-Clocked Offset-Cancellation Scheme for Implantable Biomedical SoCs", in ISSCC, 2009, pp. pp. 402?403.

56 L. Joonhyung, L. Kwangmook, and C. Koonsik, "Ultra low power RC oscillator for system wake-up using highly precise auto-calibration technique", 2010 Proceedings of ESSCIRC, Sep. 2010.

57 A modified Allan variance for oscillator design,tf.nist.gov/general/tn1337/Tn254.pdf, 1990. [Online]. Available: http://tf.nist.gov/general/. [Accessed: 09-Oct-2015].

58 A modified Allan variance, http://tf.nist.gov/general/tn1337/Tn254.pdf, 1982. [Online]. Available: http://tf.nist.gov/general/. [Accessed: 09-Oct-2015].