Channel-hot-carrier degradation of strained MOSFETs: A device level and nanoscale combined approach

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(Received 30 September 2014; accepted 20 February 2015; published 4 March 2015)

Strained MOSFETs with SiGe at the source/drain regions and different channel lengths have been studied at the nanoscale with a conductive atomic force microscope (CAFM) and at device level, before and after channel-hot-carrier (CHC) stress. The results show that although strained devices have a larger mobility, they are more sensitive to CHC stress. This effect has been observed to be larger in short channel devices. The higher susceptibility of strained MOSFETs to the stress has been related to a larger density of defects close to the diffusions, as suggested by CAFM data. [http://dx.doi.org/10.1116/1.4913950]

I. INTRODUCTION

With the introduction of alternative materials in CMOS technology, some challenges such as large carrier mobility (μ) in the channel must be confronted.[1] In this respect, strain techniques have been presented as an alternative, which can increase the channel mobility[2] and, to a lesser degree, can lead to lower external resistance (making the internal bias of the strained device higher for the same external voltages).[3] Recently, different techniques to introduce strain into the channel of a MOSFET have been developed and can be classified into two main categories:[4] global strain techniques and local strain techniques. In global techniques, the strain is introduced across the entire substrate; however, in local strain techniques, the strain is inserted locally at certain regions. One method of introducing local strain consists in the selective growth of a local epitaxial film in the source and drain regions of a transistor. In n-MOSFETs, a $Si_{1-x}C_x$ layer is epitaxially grown in source/drain (S/D) regions to achieve tensile stress and in p-MOSFETs selective epitaxial growth of SiGe is used to create uniaxial compressive stress.[5] The implementation of strained SiGe in the S/D areas, with a given Ge concentration, leads to an improvement of the drive current in short channel transistors.[2] This improvement is attributed first to the presence of uniaxial compressive stress in the silicon channel, which favorably alters the band structure, enhancing the hole mobility and second to the presence of the highly activated SiGe source/drain regions, which provides a reduced resistivity and series resistance.[6] However, one concern is the possible presence of defects at the SiGe/Si interface and the larger sensitivity of strained MOSFETs to electrical stresses as channel-hot-carrier (CHC) degradation and bias temperature instability.[7]

Since defect generation is a very local phenomenon that takes place in nanoscale areas, high resolution techniques as conductive atomic force microscopy (CAFM) can be very useful to investigate how strain affects the electrical properties of gate stacks. Actually, CAFM has been extensively used to investigate the MOS structures that are subjected to different fabrication processes, as high temperature annealings, which can induce the high-k polycrystallization.[8,9] CAFM has also been used to study the electrical properties of gate dielectrics (SiO_2) and high-k materials.[10–13] In particular, in a recent investigation,[14] it was demonstrated that CAFM is able to study separately the impact of CHC stress on the different regions of the channel of MOSFETs. However, in that case, nonstrained substrates were investigated only. In this work, p-MOSFETs with epitaxially grown SiGe at S/D regions have been subjected to CHC stress and their electrical characteristics have been compared to reference devices without strained channels. In particular, the impact of the stress on the drain current, I_D (measured at device level), and on the gate current, I_G, at different regions of the channel (measured at the nanoscale with CAFM) has been studied on devices with different channel lengths.

II. EXPERIMENT

In this work, p-MOS transistors with a 1.4 nm thick SiON layer as gate dielectric and 60 nm polysilicon/40 nm NiSi stack as gate electrode have been studied. In strained devices, the SiGe at S/D regions were selectively deposited with a 15% Ge content [Fig. 1(a)]. These devices were compared to identical p-MOSFETs without strained silicon [reference devices, Fig. 1(b)]. Transistors with different channel lengths ($L = 0.13$, 0.5, 1, and 3 μm) and 1 μm width were considered. Some samples were subjected to CHC stress by applying $V_G = V_D = -2.6$ V for 200 s keeping the other terminals grounded[15] and some other samples were not stressed (fresh samples). Although strain can result in lower external resistance leading to higher internal bias for the same external voltages (compared to nonstrained devices), since the focus of the work is to perform a reliability comparison between both technologies, CHC degradation was induced at the same voltages. Using the same biases allow to evaluate which technology suffers from larger degradation when operation under the same conditions.

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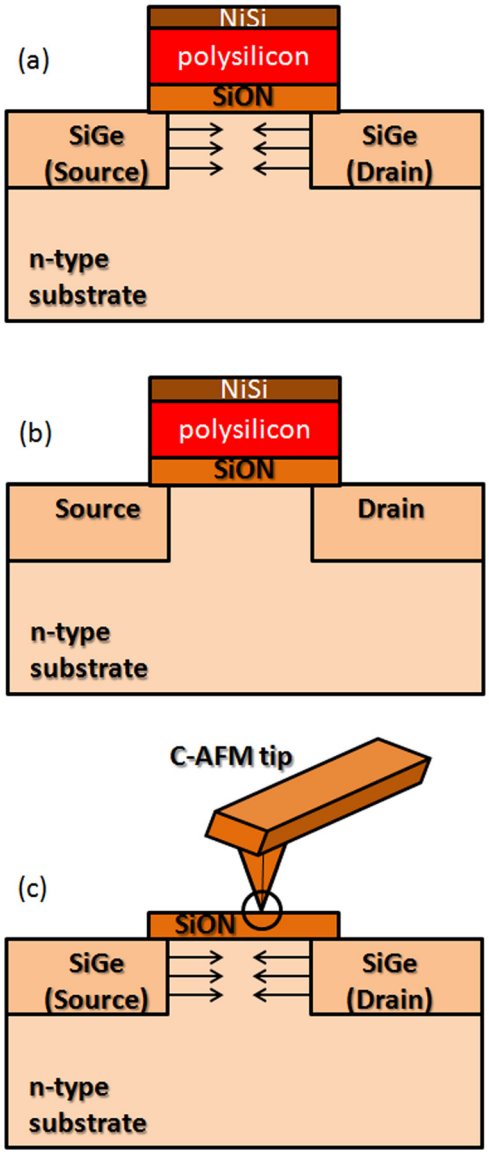

FIG. 1. (Color online) Schematics of strained (a) and unstrained (b) pMOSFETs measured at device level (c). Experimental configuration when the strained devices are studied with CAFM.

Before and after the CHC stress, device level measurements were performed (to get the I_D–V_G, I_D–V_D characteristics), and the device aging was characterized. After the device level analysis, the polysilicon and NiSi layers on top of the gate dielectric were removed with a very selective wet etch to expose the gate dielectric and make it accessible to nanoscale electrical measurements with the CAFM tip [Fig. 1(c)]. The etching consisted of immersing of the sample in a solution of phosphoric acid, 85%, at 125 °C, during 90 s.[14] After the etching, the gate oxide was scanned with the AFM tip to investigate its morphology and electrical properties. When the structure is polarized, current can flow through the gate and the electrical properties of nanometer sized regions of the dielectric can be evaluated. Due to the saturation of the electronics of the CAFM setup, maximum currents of 10 nA can be measured. In this work, PtIr coated Si tips with a nominal tip radius of 20 nm were used.

III. DEVICE LEVEL MEASUREMENT

Since CAFM can only measure the gate current through the dielectric, the device level analysis will allow to investigate the effect of the strain and the stress on the current along the channel, that is, the drain current, I_D. In this section, the electrical characteristics of fresh (before any electrical stress) and CHC stressed devices have been compared on strained and nonstrained MOSFETs at device level. Several channel lengths were also studied. Figure 2 shows typical I_D–V_G [(a), (d), and (g)], I_D–V_D [(b), (e), and (h)], and transconductance (g_m) [(c), (f), and (i)] characteristics of MOSFETs with a 0.13 μm [(a)–(c)], 1 μm [(d)–(f)], and 3 μm [(g)–(i)] channel length. In all plots, solid symbols correspond to strained devices and open symbols to unstrained transistors. Squares and circles correspond to fresh (unstressed) and CHC stressed devices, respectively. The I_D–V_G characteristics were measured at $V_{DS} = -50$ mV and the I_D–V_D curves at $V_{GS} = -0.6$ V.

First, the effect of the strain on the electrical characteristics of fresh devices (squares in Fig. 2) is compared. A clear increase of the drain current, I_D, is observed in strained transistors, which is attributed to an increment of the carrier mobility due to the channel strain.[2] This increase of μ is confirmed in Figs. 2(c), 2(f), and 2(i), which shows the transconductance (g_m) as a function of V_G for the different channel length MOSFETs. A larger g_m is observed in strained (solid) transistors, which indicates a higher mobility in these devices for all lengths. However, when comparing short and long channel devices, the I_D increase is much larger in short channel devices (see Table I, which shows the percentage increment of I_D, at $V_D = -0.6$ V, in strained MOSFETs compared to nonstrained devices for different lengths, called from now on α_D). This effect could be related to the fact that the induced strain is not uniformly distributed. Near source and drain regions, the induced strain is larger and decreases as we move to the center of the channel. As a consequence, the total strain in the channel depends on the channel length. For shorter devices, the source and drain regions are closer, and, therefore, the strained gate region (compared to the total gate area) is larger, leading to an enlargement of the average mobility and, thus, a higher I_D.[16]

The impact of a CHC stress on both kinds of MOSFETs (strained and nonstrained) was also studied. Note that, after the stress (Fig. 2, circles), I_D is reduced in both, strained (solid symbols) and nonstrained devices (open symbols). Table II shows the I_D reduction ($I_{D,red}$) at $V_D = -0.6$ V, in percentage, for the different MOSFETs. Note that the reduction depends on L and on the strain in the channel. In particular, $I_{D,red}$ is larger in strained devices (for a given L),[7] demonstrating that strained MOSFETs are more sensitive to a CHC electrical stress. When different lengths are compared, we can observe that the stress impact in short channel devices is larger, as expected, since higher electrical fields were applied along the channel. To eliminate the effect of the different stress conditions so that the strain effect is only considered, Table I shows, for a given L (and, therefore, for the same stress conditions), how large is the I_D reduction in

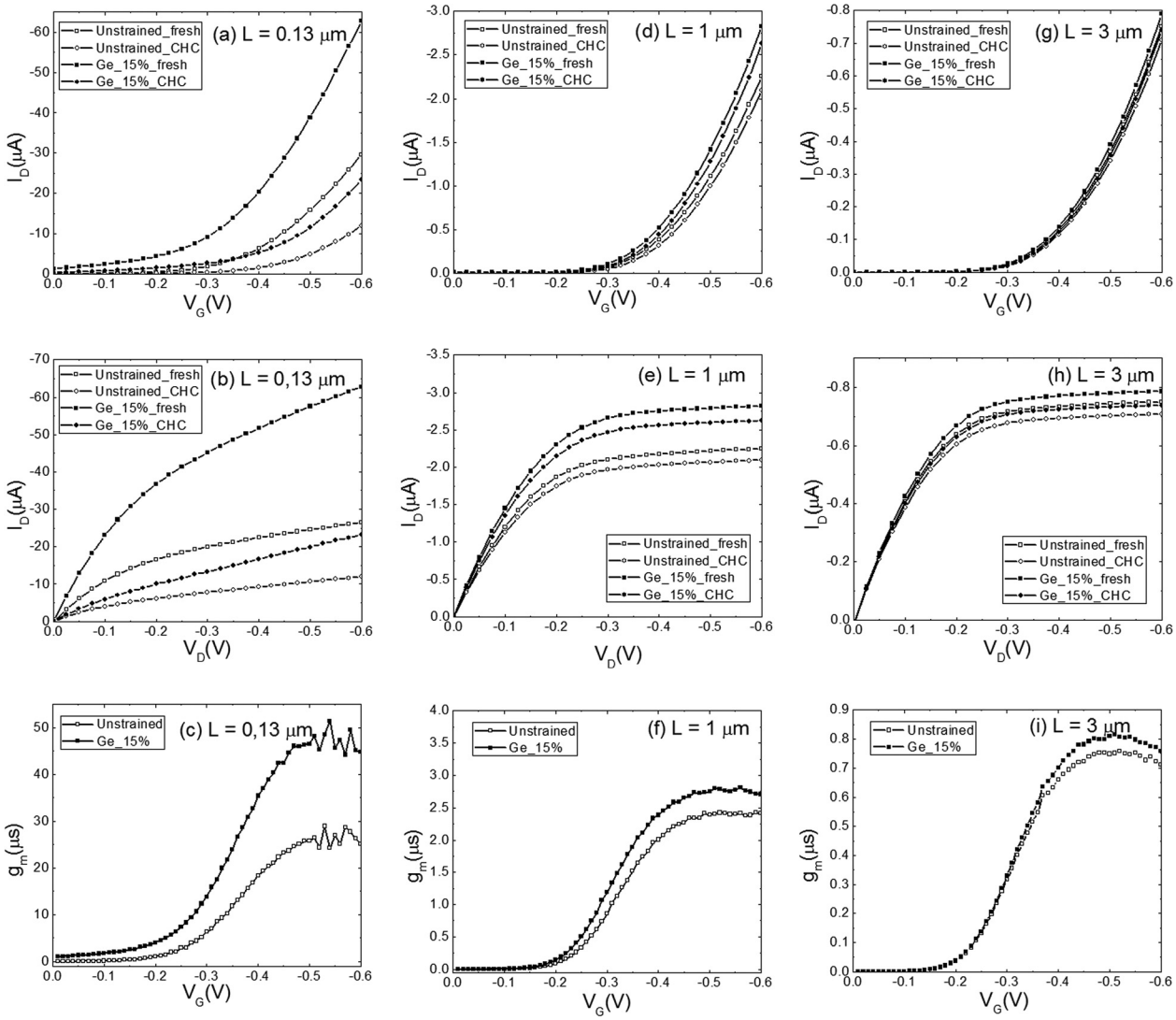

FIG. 2. I_D–V_G [(a), (d), and (g)], I_D–V_D [(b), (e), and (h)], and g_m–V_G [(c), (f), and (i)] curves of fresh (squares) and CHC (circles) stressed MOSFETs with strained (solid symbols) and unstrained (open symbols) channels. Channel length is 0.13 μm [(a)–(c)], 1 μm [(d)–(f)], and 3 μm [(g)–(i)].

strained MOSFETs compared to nonstrained devices (in percentage, β_D), defined as

$$\beta_D = (I_{D,red,\,strain} - I_{D,red,\,non\text{-}strain}) / I_{D,red,\,non\text{-}strain} \times 100. \quad (1)$$

Note that in short channel devices, β_D is larger, indicating that, for the same electric field, strained MOSFETs with short channel lengths are more sensitive to a CHC stress than those with large L. This can be explained again by considering that strain affects a larger portion of the global gate area of the device. So, from this analysis, we can conclude that the drain current (I_D) measured in strained devices, although larger, is more susceptible to be affected by CHC stress: a larger decrease than in nonstrained MOSFETs is observed, especially in short channel transistors.

TABLE I. α_D is the percentage increment of I_D in strained MOSFETs compared to nonstrained devices for different L. β_D indicates how large is the I_D reduction (and, therefore, the stress effect) in strained MOSFETs compared to nonstrained devices (in percentage) for a given L.

	L = 0.13 μm (%)	L = 1 μm (%)	L = 3 μm (%)
α_D	111.57	25.42	4.94
β_D	18.59	11.74	8.89

IV. NANOSCALE MEASUREMENT

In this section, a nanoscale analysis of the gate oxide properties of strained and unstrained MOSFETs (with different lengths) has been performed with CAFM. The gate current (I_G) has been measured with the CAFM tip on fresh and

TABLE II. I_D reduction after stress, $I_{D,red}$, in percentage, in CHC stressed MOSFETs compared to fresh devices for different lengths and substrates.

	Unstrained devices			Strained devices		
L (channel length)	0.13 μm	1 μm	3 μm	0.13 μm	1 μm	3 μm
$I_{D,red}$	55.37%	6.82%	6.05%	68.02%	7.73%	6.64%

stressed transistors and it has been considered as an indicative magnitude of the degradation induced by the stress.[14] Figures 3(a) and 3(b) show typical current images obtained at $V_G = -4$ V on the gate area of a fresh unstrained (a) and strained (b) MOSFET (with $L = 3\ \mu$m in this case). Note that before the stress [Figs. 3(a) and 3(b)] no currents are detected in the image. In both maps, only the instrumental noise from the CAFM preamplifier can be observed. Figure 3 also shows the current maps of the gate area measured at -4 V on nonstrained [(c) and (e)] and strained [(d) and (f)] MOSFETs after a CHC stress, with $L = 3\ \mu$m [(c) and (d)], and $L = 0.13\ \mu$m [(e) and (f)]. Note that, after the stress, brighter areas, which correspond to regions with a higher conductivity and were not present in fresh devices at the same voltage, are measured. This is indicative of the induced degradation by the stress in the device.

In the $0.13\ \mu$m channel length MOSFET, the measured currents reach the maximum measurable value, indicating that breakdown (BD) could have been triggered during the CAFM scan probably due to the large degradation induced by the CHC stress. Although breakdown was not triggered during the device level measurements (see Fig. 2), the stress could have damaged the gate oxide in such a way that when voltage was applied to the tip, breakdown could have been triggered. Even in the case that BD was not induced by the CAFM scan, currents are very large, which are indicative of a larger degradation. However, since I_G reaches the maximum allowed current by the setup, no quantitative analysis is possible in these short channel devices.

Contrarily, in the $3\ \mu$m channel length MOSFET [Figs. 3(c) and 3(d)], the leaky sites show lower currents, clearly indicating that BD was not induced in this case. The same kind of behavior is observed in devices with $L = 1\ \mu$m channel length (not shown). The leaky sites can be related to trap assisted tunneling through the defects generated during the stress. Therefore, these sites can be used to analyze the impact of the CHC degradation on the electrical properties of the gate oxide area. Note that the number of leaky sites in strained samples is considerably larger than in unstrained transistors, which indicates a larger CHC damage in strained devices. These results are consistent with the device level measurements. Moreover, thanks to the possibility of this technique to analyze very small areas along the channel, the CAFM images, also give us the possibility to study the impact of the stress in different regions of the channel. A quantitative analysis of the current images obtained in different MOSFETs ($L = 1\ \mu$m) is summarized in Table III. This table shows the average gate current $\langle I_G \rangle$ measured on six devices ($L = 1\ \mu$m) in a $0.25\ \mu m^2$ region close to the S, D and in the center of the channel (C), obtained from current images as those shown in Fig. 3. Note that, in both kind of transistors (unstrained and strained), regions close to S and D show larger currents, demonstrating the nonuniform degradation of CHC stress, as previously observed in Ref. 14 (Table III). To quantitatively compare the impact of the CHC stress in different regions of the channel between strained and nonstrained devices, the β_G parameter was calculated (Table III)

$$\beta_G = (I_{G,\text{increase, strain}} - I_{G,\text{increase, nonstrain}}) / I_{G,\text{increase, nonstrain}} \times 100, \quad (2)$$

which corresponds to the increment of the gate current in strained devices compared to nonstrained ones. Note that β_G, which is indicative of the impact of the stress, is larger close to S and D. Therefore, these results demonstrate that, besides the nonuniformity of the CHC stress itself, in strained devices, source and drain are more sensitive to the stress than nonstrained MOSFETs. Because of this higher susceptibility, the generation of defects in these areas is favored (compared to unstrained devices) and is detected by measuring a larger number of leaky sites and higher currents with the tip of the CAFM.

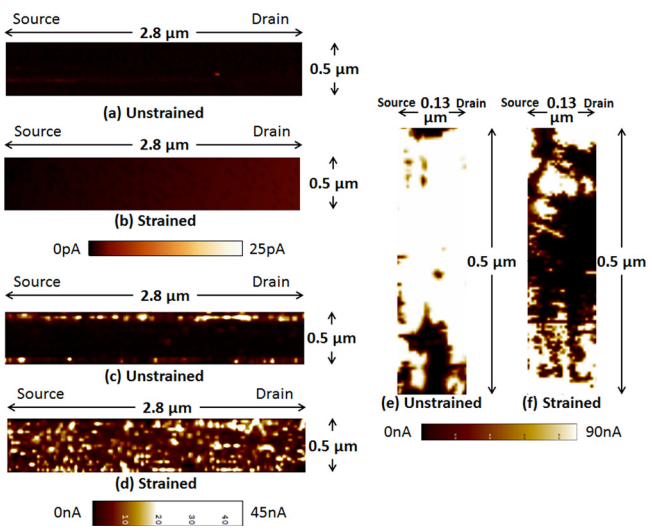

FIG. 3. (Color online) Current images obtained at a gate voltage of -4 V in fresh [(a) and (b)] and CHC stressed [(c)–(f)] MOSFETs with channel length $3\ \mu$m [(a)–(d)] and $0.13\ \mu$m [(e) and (f)]. Note that (a), (c), and (e) corresponds to unstrained devices and (b), (d), and (f) corresponds to strained devices.

V. CONCLUSIONS

In this work, the impact of a CHC stress on strained MOSFETs has been investigated and compared to unstrained devices by combining device level and nanometer scale characterization techniques. The nanoscale resolution of the CAFM has allowed investigating the spatial distribution of the damage after the stress. The results show that, with the introduction of strain, the channel mobility increases in both

TABLE III. Average I_G and β_G values obtained with CAFM close to S/D and in the center of the channel (C) for 1 μm strained and unstrained devices.

	$\langle I_G$ (nA)$\rangle$		
	Unstrained	Strained	β_G (%)
Source	2.67	10.54	294
Channel	1.43	4.92	244
Drain	2.01	9.51	373

long and short channel devices, being the increment larger in short devices. However, the transistors subjected to local strain are more sensitive to CHC degradation, leading to a higher reduction of I_D after the stress. This reduction could be related to a higher defect generation in strained devices, especially at the channel regions close to source and drain, since a larger increase of the gate current was detected with CAFM in these regions compared to nonstrained devices.

ACKNOWLEDGMENTS

This work has been partially supported by the Spanish MINECO and ERDF (TEC2013-45638-C3-1-R) and the Generalitat de Catalunya (2014 SGR-384). Qian Wu is financially supported by China Scholarship Council (CSC) with No. 201408390030.

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