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Reversible Dielectric Breakdown in ultrathin Hf based high-k stacks under current limited stresses.

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Abstract. The effects of a current-limited breakdown (BD) on the post-BD current of MOS capacitors with a thin high-k dielectric stack have been analysed. A strong current reduction after BD and, consequently, a partial recovery of the insulating properties of the dielectric stack is observed. The similarities with the Resistive Switching phenomenon observed in MIM structures for memory applications are discussed.

Keywords: Dielectric breakdown, Resistive switching, high-k reliability, CMOS process.

1. Introduction.

Deep submicron technologies, which contain high-k dielectrics as gate oxide in MOSFETs, are prone to several failure mechanisms. Among them, dielectric breakdown (BD) could be the cause of a strong circuit lifetime limitation and/or power consumption increase. Although the phenomenon has been extensively studied [1, 2], its implications from the circuit point of view are not well established yet [3, 4]. In this regard, current limited stresses (CLS) have been suggested to better reproduce the operation conditions of devices within a circuit, since they can take into account the limited current capability of MOSFETs, who, within a circuit, will actually supply the post-BD gate leakage. When SiO_2 based devices were subjected to CLS, (i) the post-BD current was found to be lower than under an equivalent non-limited current stress [5] and (ii) BD was demonstrated to be a reversible phenomenon [6]. However, in the last decade, BD has been always treated as an irreversible mechanism.

In this work, high-k based MOS structures have been subjected to CLS and the post-BD gate current analysed. We have observed that the dielectric conductivity after BD can be switched from a high conductivity state to a low conductivity state. The phenomenology of the BD reversibility has been described in detail. In particular, the influence of the stress current limit, and the gate voltage polarity

involved in the BD reversibility process has been analysed. Finally, the similarities with the Resistive Switching (RS) effects in Metal-Insulator-Metal structures for memory applications [7] are discussed.

2. Experimental.

The samples used in this work were MOS capacitors (n and p type Si substrate) with an area of $25um^2$. The gate dielectric stack (EOT= 1.4 nm) was formed by a HfSiON film (physical thickness of 2.9 nm, 60% Hf) on top of a 1.2 nm thick SiO_2 interfacial layer. FUSI was used as gate electrode. Another set of n-type MOS capacitors with aluminium gate and dielectric stack formed by 3.5 nm HfO_2 and 1.4 nm SiO_2 interfacial layer (EOT=1.9 nm) was also used. The samples were stressed until BD by applying ramped voltage stresses (RVS) or Constant Voltage Stresses (CVS). In both cases, the stress voltage was applied to the gate, with the substrate terminal grounded. During the stresses, the current was limited using the compliance of the measurement equipment. For comparison, in some devices the BD was provoked without current limit. Before the CVS stresses, a low ramped voltage was applied to measure the I-V curve of the fresh device (note that during the RVS, the fresh I-V characteristics is simultaneously obtained). After the stress, two monitoring post-BD I-V curves, obtained without current limitation, were measured to study the post-BD current properties. The observed phenomenology was found to be independent of the MOS structure materials, so that we will focus our attention on the FUSI/HfSiON/SiO_2/Si structures.

3. BD reversibility.

First we have analysed the post-BD behaviour of the device when current-limited RVS (CL-RVS) were used to induce the stack BD. Fig.1 shows typical I-V curves measured on a n-type substrate capacitor (similar behaviour is observed on p-type substrate structures). Curve I_F corresponds to the I-V characteristic measured during the CL-RVS. In this case, the voltage was swept until 4V and the instrument current compliance was set to 500μA. The BD event can be detected as a fast current increase at ~3.6V (obviously, below this voltage, the I-V characteristic is indicative of the electrical properties of the fresh device). After BD, two consecutive post-BD I-V curves (I_{BD} and I_R) were registered without limiting the current. Curve I_{BD} (open circles in Fig.1) corresponds to the first measured post-BD I-V curve. As expected, for low enough gate voltages, the current is much larger than the one obtained in the fresh sample (approx. 6 orders of magnitude at 1V) due to the BD induced during the previous CL-RVS.

However, surprisingly, at a given voltage (~2.4V), the current starts decreasing and, at 2.65V, it is two orders of magnitude lower, recovering the current level observed before BD (curve I_F). Curve I_R corresponds to the second measured post-BD I-V curve. For voltages below 2.4V, the current is larger than in the fresh capacitor (I_F), but much lower than the one shown in the first post-BD I-V characteristic (I_{BD}), which indicates a partial recovery of the dielectric insulating properties. For larger voltages, I_R, I_{BD} and I_F overlap, suggesting that tunnelling through the whole device area controls the gate current.

In conclusion, after the stack BD, below 2.4V, two different states are distinguished: a high (I_{BD}) and a low (I_R) conductivity state. In our measurements, the change between the high to the low conductivity state takes place when I_{BD} slightly exceeds the current compliance value of the current-limited stress. On the other hand, the dielectric BD, that brings the sample to the high conductivity state, is always produced at a voltage larger than the one for which the decay of the current from I_{BD} to I_R is observed. If the stress-monitor sequence is repeated, the switching between the two conductivity states is again obtained. However, if BD is induced by RVS without fixing a current limit, the BD reversibility is not observed. This result indicates that the current compliance set during the stress that creates the BD path is a fundamental factor to observe the current recovery. Fig.1 represents the typical behaviour of a set of samples, although the particular voltages at which the conductivity states changes (from low-to-high or high-to-low) vary from sample to sample.

4. Current limit dependence.

The dependence of the post-BD conduction on the current limit fixed during the stress has been analysed. To do so, the BD was induced during a current limited CVS stress (CL-CVS). The current compliance was varied from 50μA to 500μA and a stress voltage of 3V was used. The time-to-breakdown measured on 30 devices was in the ~10-1000s range. Two consecutive post-BD I-V curves, without current limitation, were measured afterwards. The current values at 1V on the two post-BD characteristics (I_{BD} and I_R, as those in Fig. 1) have been chosen as the parameters which are indicative of the conductivity of the two states. No correlation between these currents and the time-to-breakdown has been found. Fig.2 shows I_{BD} (high conductivity state) and I_R (low conductivity state) measured at 1V after the 3V CL-CVS, as a function of the compliance limit. For comparison, the current measured after non-limited stresses is also included. The dotted line indicates the fresh current value, I_F, at 1V. On average,

the high post-BD current, I_{BD} (crosses in Fig.2), slightly increases with the current compliance, showing a small data dispersion. Contrarily, the variability of I_R (low conductivity) is much larger. In addition, no clear dependence of I_R with the stress current limit can be inferred.

The results plotted in Fig. 2 confirm the presence of two conductivity states in the gate dielectric, whose conductivity differs, on the average, in approx. 2 orders of magnitude at 1V, between I_{BD} and I_R. In some cases, differences of four orders of magnitude are observed. Note that, when the BD is induced during a non-limited current stress the two conductivity states can not be distinguished and the measured current is larger than I_{BD} obtained under CL-CVS.

It must be emphasized that the high conductivity state is very stable, since it does not depend on the time elapsed between the BD event and the measurement of the I_{BD} post-BD curve. This can be concluded from Fig. 3, where the voltage applied by the equipment during the CL-CVS stress (450s long) is shown. When BD takes place and the percolation path [8] is created, the voltage decreases to maintain the current at the value fixed by the compliance. So that, after the BD the CL_CVS stress automatically turns to a Constant Current Stress (CCS) in which the stress current is imposed by the compliance. Note that, despite the different duration of the CCS stress (determined by the time-to-breakdown of the sample and the time until the I_{BD} measurement) during this CCS the gate voltage remains constant with the stress time (Fig. 3) suggesting that no or negligible degradation is being induced in the percolative path previously created. This can be observed for different current compliance values.

5. Voltage polarity dependence.

In the previous experiments, CL-RVS or CL-CVS positive stresses were applied to create the BD path, and the post-BD I-V curves were obtained at positive voltage too. In this section, we have analysed the dependence of the post-BD conduction on the polarities of the stress-sense voltages. Fig. 4 shows I_{BD} and I_R measured on n-type MOS capacitors subjected to a positive CL-CVS (3.2V, 500 μA) until BD, followed by a negative (solid circles) and positive (open circles) post-BD ramped voltages. The fresh currents for both monitor polarities, I_F (continuous lines), are also shown, for comparison.

Fig. 4 shows that if the CL-CVS and the subsequent post-BD ramped voltage are positive, the BD

reversibility is observed: I_{BD} suddenly drops and the current during the following ramped voltage is smaller (dashed line, I_R). However, when a negative post-BD ramped voltage is applied, i.e., stress and sense voltage polarities are opposite (I_{BD}, solid circles) no reversibility is observed and the sample reaches the final BD, as the subsequent I-V curve (I_{BD2}, solid squares) confirms. If the polarity of the CL-CVS is negative (Fig. 5), independently of the polarity of the post-BD ramp voltage (negative or positive) the BD reversibility is observed (Fig. 5). The results shown in Fig. 4 and 5 have been observed in around 20 devices at different combination of stress/post-BD ramp polarities.

Therefore, we can conclude that the BD reversibility depends on the polarities of the stress and sense voltages (Table 1): whereas for the case of same polarity, the BD reversibility is always observed, in one of the opposite cases, BD is found to be irreversible. The MOS capacitors with p-type substrate behave equivalently (not shown here) to those with n-type substrate.

6. Discussion.

The results described above have shown that, as observed for SiO_2 devices, BD in high-k gate stacks could be a reversible phenomenon. However, this reversibility can be only observed when the current during the BD transient is externally limited (as would happen in a circuit environment). This is, to our knowledge, the first time that BD reversibility is reported in ultrathin MOS structures based in high-k, so that, a lot of work will be needed to understand the physical mechanisms involved. As a starting point in this direction the BD reversibility has been compared with other phenomenon observed in Metal-(thick) Insulator-Metal structures: the Resistive Switching (RS) [9]. The RS has gained recently a lot of interest in the scientific community because of its possible application in future memory devices. In the RS, as for the BD reversibility observed here, two different conductivity states are distinguished: a low resistivity state (LRS, I_{BD} in our case) and a high resistivity state (HRS, I_R in this work). However, this is not the only similarity observed between the RS and BD reversibility: [9]. Using the resistive switching terminology, (i) in both phenomena a 'forming process' is needed, which brings the structure to the low-resistivity state by applying a high-voltage stress. In our case, this forming process would correspond to the percolation path creation during the stress (related to generated traps), which qualitatively can be understood as the formation of a filamentary conductive path though the dielectric proposed by some authors for the RS phenomena.[9](ii) The switching between the low and high conductivity states states is

achieved by applying a threshold voltage. The threshold voltage needed to switch from the HRS (I_R) to the LRS (I_{BD}) is larger than the one needed for the switching form LRS (I_{BD}) to HRS (I_R) change. (iii) The set of a current limitation during the stress is a key parameter to observe the current switching in both RS [9] and BD reversibility. (iv) The switching is always possible when the two applied voltages (stress and sense) have the same polarity, as in unipolar RS, which is compatible with a filamentary conducting mechanism [7]. In our case, the HRS is associated to the opening of the BD conducting path, but further work is needed to determine the origin of the LRS. In particular, the analysis of the stability of the two conductivity states can help to clarify the mechanisms involved in the BD of the high-k stack. The RS phenomenon has been observed in a wide variety of transition metal oxides in MIM structures [10], and only very recently it has been observed in thick (22nm) HfO_2 MIS structures [11]. However, to our knowledge this is the first time that this phenomenon is reported in standard Hf based ultrathin high-k MOS structures for logic applications and discussed in the context of reliability.

From the circuit point of view, it has been demonstrated that to consider one BD as device failure criterion can be too much restrictive [3]. For this reason the leakage current increase is commonly used [12] to evaluate the device reliability. In this sense, the observed BD reversibility implies that, after BD, the dielectric conductivity can be considerably decreased. Therefore, an appropriate monitoring and control of the conductivity state of the thin high-k stacks could reduce the leakage current after BD and increase the circuit lifetime.

Acknowledgements.

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Figure captions

Fig.1: I-V curve measured during a current-limited ramped voltage stress that induces the BD (I_F) and two consecutive post-BD I-V characteristic (I_{BD} and I_R). At a determined voltage, the current in the first post-BD I-V curve (I_{BD}) decreases suddenly. At low fields, the current in the second post-BD I-V curve (I_R) is lower than in the first post-BD one (I_{BD}) but larger than in the fresh device (I_F). However, at high field, the three curves overlap.

Fig 2: I_{BD} (crosses) and I_R (circles) measured at 1V after a 3V CL-CVS as a function of the current compliance. The dotted line indicates the fresh current at the same voltage. The currents after non-limited current stresses are also shown.

Fig. 3: Gate voltage evolution with time during CL-CVS stresses. The sudden voltage drop indicates the creation of the BD percolation path. Afterwards, the stress turns to CCS with a stress current imposed by the compliance. During the CCS the gate voltage remains stable, and no additional degradation is induced of the percolative path.

Fig. 4: I_{BD} and I_R curves measured after a positive CL-CVS during positive (right) and negative (left) ramped voltages. BD reversibility is observed when a positive ramp voltage is used (open circles) but, when the voltage ramp is negative (solid circles), BD becomes irreversible.

Fig. 5: I_{BD} and I_R curves measured after subjecting n-type MOS capacitors to a negative CL-CVS. In this case, the BD reversibility is observed independently of the monitor voltage polarity (open and solid circles).

Table 1: The observation of the BD reversibility depends on the polarities of the current-limited stress and the post-BD monitor ramp voltage. The ticks indicate the cases that show BD reversibility.

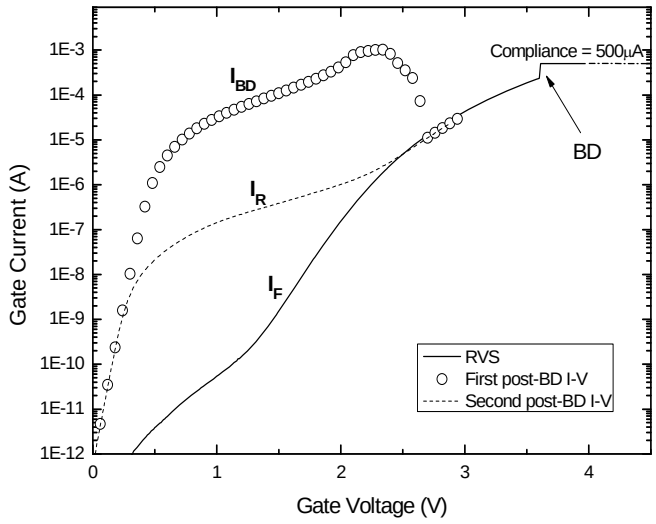

Figure 1

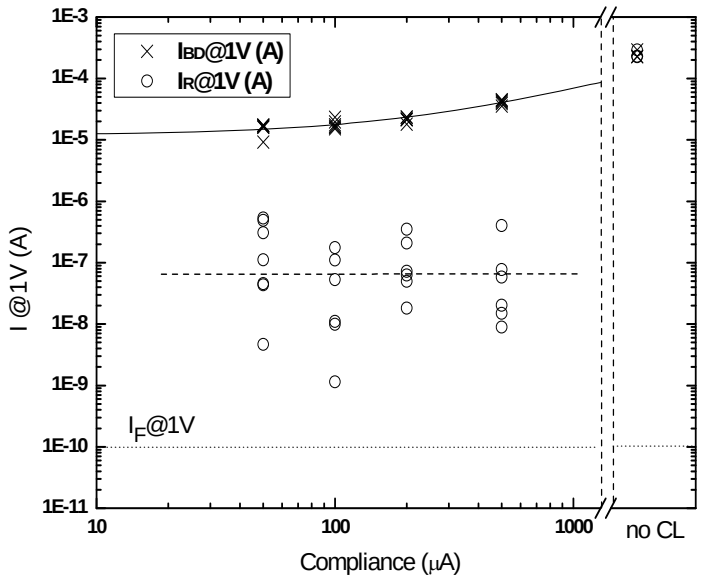

Figure 2

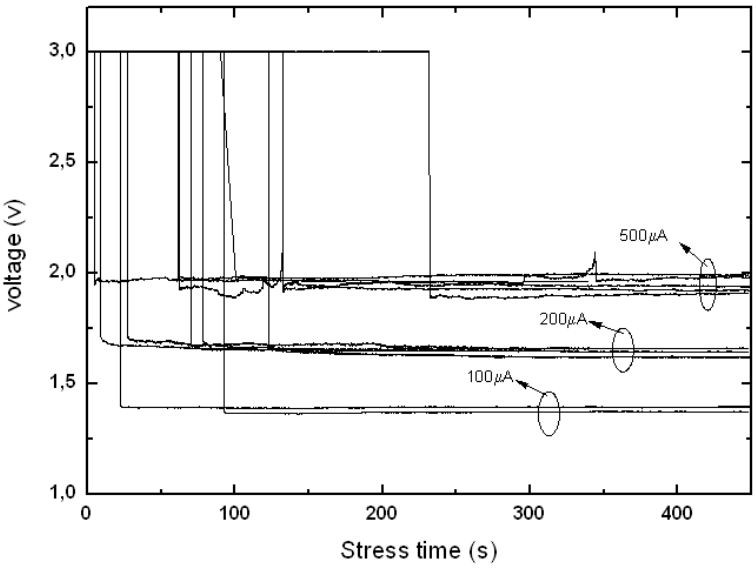

Figure 3

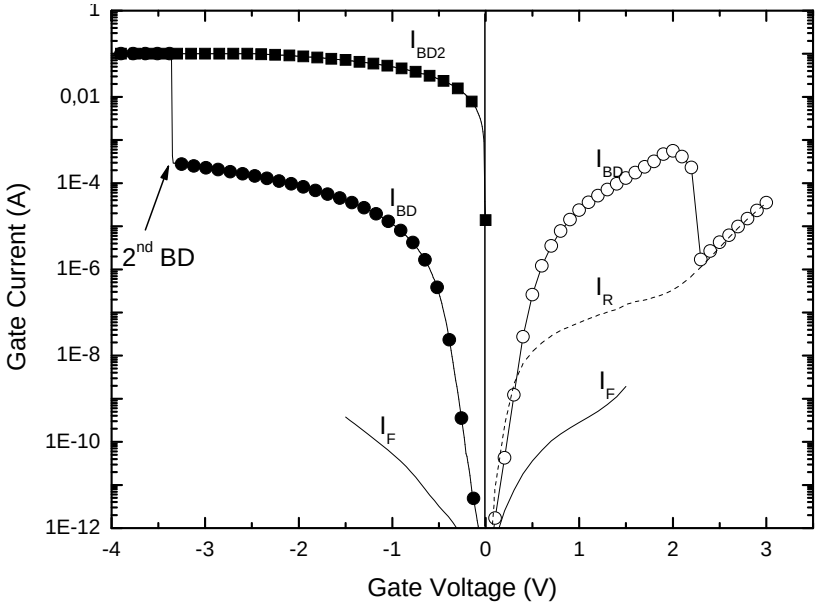

Figure 4

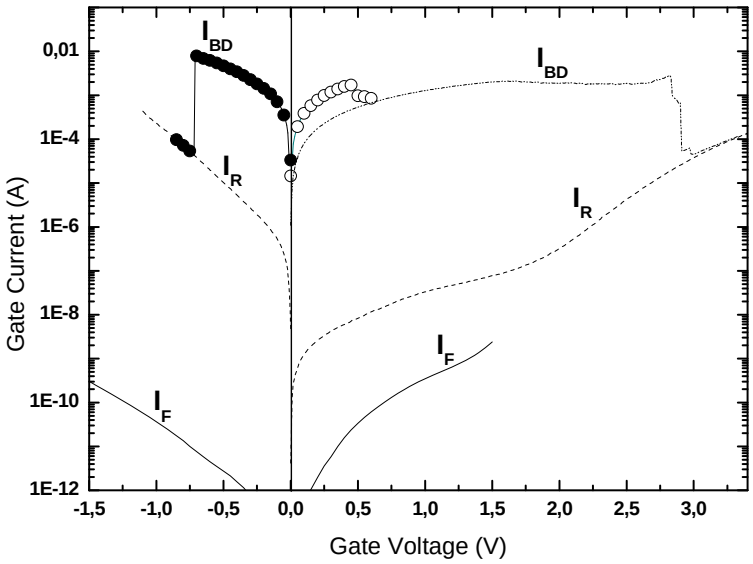

Figure 5

		Stress polarity	
		Positive	Negative
Post-BD ramp polarity	Positive	✓	✓
	Negative	X	✓

Table 1