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RESISTIVE SWITCHING-LIKE BEHAVIOUR OF THE DIELECTRIC BREAKDOWN IN ULTRA-THIN HF BASED GATE STACKS IN MOSFETS.

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Abstract

The gate dielectric breakdown (BD) reversibility in MOSFETs with ultra-thin hafnium based high-k dielectric is studied. The phenomenology is analyzed in detail and the similarities with the resistive switching phenomenon emphasized. The results suggest that the conductive path in the dielectric after BD can be 'opened' and 'closed' many times and that the BD recovery partially restores not only the current through the gate, but also the MOSFET channel related electrical characteristics.

Keywords

MOS devices, High-k, Dielectric Breakdown Reversibility, Leakage Current, Reliability, Resistive Switching.

Main Text

I. INTRODUCTION

The capability of some materials to switch between two conductivity states, namely Low Resistive State (LRS) and High Resistive State (HRS), is known as Resistive Switching (RS) [1]. Devices based on the RS phenomenon have recently acquired an increasing importance for non volatile storage applications since the resulting devices combine fast operation, and huge scaling potential [2]. The phenomenon has been usually studied in Metal-Insulator-Metal (MIM) structures with a thick insulator (several tenths of nm), based on non standard CMOS chemical elements [3]. On the other hand, in the field of device reliability, the gate dielectric breakdown (BD) in MOSFETs, one of the most relevant failure mechanisms in CMOS technologies [4], is also characterized by the loss of the insulating properties, changing from a low conductivity state (pre-BD) to a high conductivity one (post-BD), whose currents can differ in several orders of magnitude. BD is attributed to the creation of a conductive path through the gate dielectric [5,6] and can have a very detrimental effect on the device performance [7,8] Traditionally, and contrarily to the RS phenomenon, the conductivity change due to the BD has been considered to be irreversible, i.e., after the BD, the gate dielectric reach a

permanent high conductivity state that can lead to the device failure. However, several years ago it was shown that in SiO_2, in some occasions, BD could be reversible [9], i.e., a lower conductivity state could be reached after a BD event. More recently, the presence of two interchangeable conductivity states after BD in MOSFETs with ultrathin Hf based gate dielectric stacks has been reported [10,11], so that the insulator properties of the dielectric can be at least partially recovered [10, 12]. However BD reversibility phenomenon in ultrathin dielectrics, as those used in ultrascalled MOSFETs, is not well understood yet and consequently modeling and characterization efforts are needed.

In this work, BD reversibility is studied in MOSFETs with ultra-thin Hf-based high-k dielectric and the similarities with the RS phenomenon are exposed. The procedure to induce two interchangeable conductivity states in these samples and the statistical distribution of voltage and current parameters that characterize the BD reversibility are described. Using the common BD characterization methods (derived from the local nature of BD [13]), the conductive path features for both conduction states are also studied. Finally, the effect of BD and BD recovery on the transistor performance when different paths are created at different sample locations has also been analyzed.

II. SAMPLES AND EXPERIMENTAL

The samples used in this work were pMOSFETs with FUSI gate electrode and a dielectric stack formed of a (2.9nm) HfSiON film on top of a 1.2 nm SiO_2 interfacial layer (EOT=1.9 nm). Different combinations of channel width and length have been studied, ranging between W/L=0.25µm/0.15µm and W/L=1µm/0.5µm. The samples were subjected to a sequence of current limited ramped voltage stress (CL-RVS) to induce the BD (high conductivity state), plus ramped voltage stress (RVS) without current limitation, to switch to the low conductivity state, following a measurement-stress-measurement scheme, as shown in Figure 1. Though this work is focused in the characterization of the phenomenon by means of ramp voltage tests, the BD recovery can be also observed if the gate voltage is kept constant during the stresses [6]. The stresses were applied to the gate with the rest of the transistor terminals grounded and I_G, I_D, and I_S were simultaneously registered. To observe the changes in the device performance after the different stresses, the I_D-V_D and I_D-V_G characteristics of the fresh sample and those after the successive CL-RVS and RVS steps of the sequence were registered.

III. BD REVERSIBILITY PHENOMENOLOGY

Figure 2 shows typical gate currents measured in the same sample during the CL-RVS and RVS for the initial cycles of the measurement sequence illustrated in Figure 1. Curve I_F (thick line) corresponds to the gate current registered during the first CL-RVS (fresh device). When dielectric BD takes place, at V_{BD}, a fast increase of the current through the oxide is observed until reaching the current limit (in this case 500µA). At low voltages, the post-BD gate current (I_{BD}) obtained during the next RVS without current limit is, as expected, much larger than I_F. This large current indicates that the oxide losses its insulator properties, due to the formation of a conductive path through the oxide, that behaves as a low resistance. However, if the gate voltage further increases, at a given voltage (V_R), the I_{BD} current suddenly decreases several orders of magnitude. During the CL-RVS in the next cycle, at low voltages, the gate current (I_R) is

larger than the fresh current, but lower than I_{BD}. This indicates a partial recovery of the insulator properties of the gate dielectric, suggesting that, in some conditions, BD in ultra-thin Hf-based high-k oxides is a reversible phenomenon, i.e., the BD path that was 'opened' can be 'closed'. If V_G continues increasing during the CL-RVS and V_{BD} is reached, BD is observed, so that a high current level is measured once again. However, in the following RVS, after V_R, the current decreases once more. This behavior can be observed for many iterations of the stress sequence (more than 250 cycles in this work). Moreover, the phenomenon is qualitatively repetitive from sample to sample. These results indicate that, after a current limited BD, two conduction states are allowed in the dielectric, a high conductivity one (BD state, with gate current I_{BD}) and a low one (R state, with gate current I_R). Switching between both states occurs when the two threshold voltages are reached (V_{BD} and V_R). All of our experiments point out that if BD is induced without apply any current limit then BD becomes irreversible and switching does not occur anymore [11].

The described phenomenology has strong similarities with the RS phenomenon as can be observed by comparing the plots in Figure 3, where typical I-V characteristic for RS in MIM structures is schematically reproduced [1] (left) and experimental I-V curves obtained in our measurements are shown. In both graphs the existence of the two conductivity states (LRS and HRS in RS terminology, or BD and R, in the terminology adopted for dielectric breakdown) are evident. More similarities can be found between RS and BD phenomena: (i) in both cases a 'forming process' is needed. In the case of BD, this forming process would correspond to the creation of the conductive path through the oxide during the first stress, which would be equivalent to the formation of a filamentary conductive path through the dielectric, as proposed by some researchers for the RS phenomenon [2]. (ii) The switching between the LRS and HRS states in the RS phenomenon is achieved by applying two threshold voltages. From the BD point of view, these two voltages are identified as V_R and V_{BD} (as marked in Fig. 2). (iii) In both phenomena the set of a current limitation (CL-RVS) is a key parameter to observe the switching between both states. The main difference between RS and BD concerns to the samples used for their characterization: RS is typically studied in MIM structures with thick insulators whereas BD is usually analyzed in high-performance logic devices.

IV. VOLTAGES AND CURRENTS DISTRIBUTIONS

Although in the last decades a lot of work has been done to analyze the dielectric BD [4-8], its reversibility is not well understood. For this reason a detailed characterization of the phenomenon is still needed. In this section, the currents at both conductivity states and the threshold voltages are analyzed, as parameters that describe the dielectric behavior. Figure 4 (a) shows the V_{BD} and V_R values obtained on a single device subjected to more than 250 cycles of the stress sequence. The values of V_{BD} and V_R rapidly decrease (in absolute value) in the first cycles but their mean values remain constant in the following ones. The dashed line in Figure 4 (a) indicates the maximum voltage value imposed (|1.3V|) to the RVS after the transient in order to avoid irreversible BD events. Figure 4 (b) shows the cumulative distribution of V_{BD} and V_R (in this representation, a normal distribution corresponds to a straight line). As can be observed, the mean values of the distributions are separated around 1.2V and the spread is larger for V_{BD}.

The cumulative probability distributions of I_{BD} and I_R measured at -0.5V are shown in Figure 5. In this case the transient behavior during the first cycles, as observed in the voltage distributions, is not so evident, and the tail observed in I_R corresponds to values randomly measured between the 1st and the 120th cycles. Concerning to the I_{BD} distribution, two regions can be clearly distinguished: on the one hand, a region with a larger slope which corresponds to higher post-BD gate currents and, on the other hand, a second region with a lower slope which corresponds to lower post-BD gate currents. Note that these lower current levels correspond to the BD state. Attending to the measured current levels, the tails of the I_{BD} distribution shown in Figure 5 have been attributed to SBD events, whereas the larger currents in the larger slope region correspond to HBD. Note that we have used the terms SBD and HBD to refer to the different BD modes observed during the BD state and that the HBD current is limited by the external current limitation imposed during the CL-RVS [11].

V. AREA DEPENDENCE AND CONDUCTION PATH LOCATION

Dielectric BD, is known to be a local phenomenon, that is, the current after BD mainly flows through a small portion of the dielectric area [5,6]. However, the nature of the dielectric conduction during the R state is still an open question. To investigate this point, transistors with different areas have been analyzed to obtain more information about the nature of the R state. Figure 6 shows I_{BD} and I_R as a function of the transistor area. No area dependence of I_{BD} and I_R is observed, which indicates that the current through the oxide after the first BD is a localized phenomenon, whatever the state of the oxide conduction: BD or R. However, the results shown in figure 6 do not provide information of whether the current flows through the same path in both states. To check this point the location of the conductive path in the dielectric along the channel [13] has been studied. To do so, the magnitude α, defined as $I_D/(I_D+I_S)$, has been calculated for all the cycles at the BD and R states. α values close to 1 or 0 indicate that the conductive path is located close to the drain or source, respectively. Figure 7 shows the α evolution with during cycling for the R (top) and BD (bottom) states for two MOSFETs. In each sample, the location of the conductive path through the oxide during the BD and R states is the same and does not change during the successive measuring cycles. This confirms the local nature of the BD state, but also of the R state, and indicates that the conduction in both states should be attributed to the same path, i.e. the conductive path is 'opened' during the BD state and 'closed' during the R state. So that, the partial recovery of the high-k insulator properties in the R state should be attributed to changes in the atomic structure of the conductive path [14].

VI. IMPACT ON THE TRANSISTOR CHARACTERISTICS

BD can lead to the device failure not only due to the large increment of the gate leakage current, but also because, after BD, the transistor characteristics can be completely distorted and the circuit can loss its functionality [8]. However, the partial recovery of the insulating properties when the BD path 'closes' could also imply the restoration of the MOSFET/circuit functionality. Therefore, to evaluate if BD reversibility can introduce an improvement of the device reliability, the transistor conduction along the channel when the dielectric is at the R state must be studied. To do so, the transistor characteristics related to the channel conduction have been analyzed for both states, BD and R, and for two cases of the conductive path location along the transistor channel:

close to the drain or close to the source. Continuous lines in Figure 8a and 8b show the typical I_D-V_D and I_D-V_G characteristics, respectively, obtained in fresh pMOS transistors. Figures 8c and 8d show the curves when the conductive path has been formed close to the drain and the device is at the BD state. In this case, the transistor characteristics are completely distorted due to the large current through the oxide from the gate to the drain terminal. Moreover, I_D-V_G changes its sign being impossible to evaluate basic parameters such as the threshold voltage and the saturation current [15]. If the conduction path is located close to the source, at the BD state, the drain current is of the order of nA (fig. 8e and 8f), because most of the current flows between source and gate. However, when the gate dielectric is switched to the R state, the I_D-V_D and I_D-V_G curves are partially recovered (solid circles and open triangles in figure 8a and 8b, respectively), suggesting that the transistor functionality has been restored, although with a large increase of the threshold voltage and a decrease of the saturation current. In summary, a catastrophic change in the channel conduction is observed when the dielectric is at the BD state. However the channel electric properties can be partially restored when the conductive path is switched to the R state, with a larger threshold voltage and smaller saturation current. Ref [12] shows the effectiveness of using a combination of the BSIM4 MOSFET model plus the D-R gate current model to simulate the experimental transistor characteristics when the dielectric is at BD an R states.

VII. CONCLUSIONS

In MOSFETs with ultra-thin high-k Hf based dielectrics, after the BD path has been created, two conductivity states are allowed in the insulator, BD and R, being the current during the BD state (I_{BD}) larger than during the R state (I_R). Switching between the two states is possible when two threshold voltages are reached, V_{BD} and V_R, and only if the current was limited during the BD transient. The effect has strong similarities with the resistive switching phenomenon observed in MIM structures. The value of V_{BD} and V_R (that decreases quickly in the first cycles of switching between the BD and R states) shows a transient behavior, not so clearly observed in the distributions of I_{BD} and I_R. In the I_{BD} distributions, two BD modes are distinguished, that have been classified here as SBD and HBD, attending to the measured current. The area dependence of the I_{BD} and I_R currents and their location along the transistor channel suggest that the conduction in both states is local and controlled by the same BD path. Finally, the electrical characteristics of MOSFETs show that, when the oxide conductivity returns to the R state, not only the gate current (I_G-V_G characteristics) is recovered but also the channel current (I_D-V_D curves). The restoration of the MOSFET performance could have an impact in the circuit functionality, which will have to be analyzed to make accurate reliability predictions.

Acknowledgement

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Figure Captions

[1] Stress sequence for the analysis of the dielectric BD reversibility. The compliance of the measuring equipment (Keithley 4200-SCS) was used to limit the current during the CL-RVS.

[2] I_G-V_G curves measured in a pMOSFET with W/L=1μm/0.5μm after successive CLR-RVS + RVS iterations. A high current is registered after the current limited BD (I_{BD}), which suddenly drops after V_R. During the CL-RVS in the next cycle, at low voltages, the gate current (I_R) is larger than the fresh current, but lower than I_{BD}, which indicates a partial recovery of the dielectric properties. The switching between both conductivity states can be provoked in successive cycles of CL-RVS + RVS.

[3] Left: schematic picture of the typical I-V characteristic related to the RS phenomenon obtained in MIM structures [1]. Right: I-V characteristics obtained in MOS devices based in ultrathin high-k during BD reversibility. Both RS and BD phenomena present qualitatively similar I-V curves with two clearly different and interchangeable conductivity states.

[4] (a) BD voltage (V_{BD}) and R voltage (V_R) evolution during cycling. A transient behaviour is observed at the initial cycles, later the mean values of V_{BD} and V_R remain stable. (b) Cumulative probability of V_{BD} and V_R registered during cycling on the same device.

[5] The cumulative probability function of I_{BD} (solid circles) and I_R (open circles) registered at V_G = -0.5V during more than 250 measuring cycles on the same device.

[6] I_{BD} and I_R measured at V_G=-0.9V as a function of the transistor area. No area dependence is observed in any of the two conductivity states.

[7] The quotient $\alpha=I_D/(I_D+I_S)$ allows to locate the conduction path in the dielectric along the channel [7]. Two samples, with BD located at the extremes of the channel, are

considered. For each sample, the location of the conduction path in the BD (bottom) and R (top) states is the same and does not change during successive cycles.

[8] (a) I_D-V_D characteristics for a fresh transistor (solid lines) and at the R state (dots). (b) I_D-V_G characteristics for a fresh (solid lines) and recovered (dots) transistor. (c) I_D-V_D characteristics when the BD path is located at drain, and (e) when located at source. (d) I_D-V_G characteristics of the transistors with BD located at drain, and (f) with BD located at source.

Figures

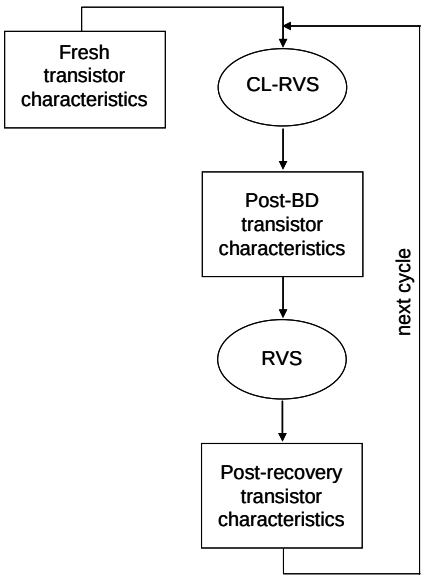


Figure 1

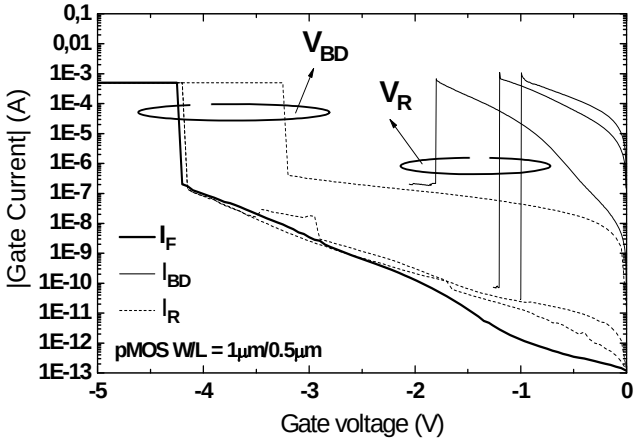


Figure 2

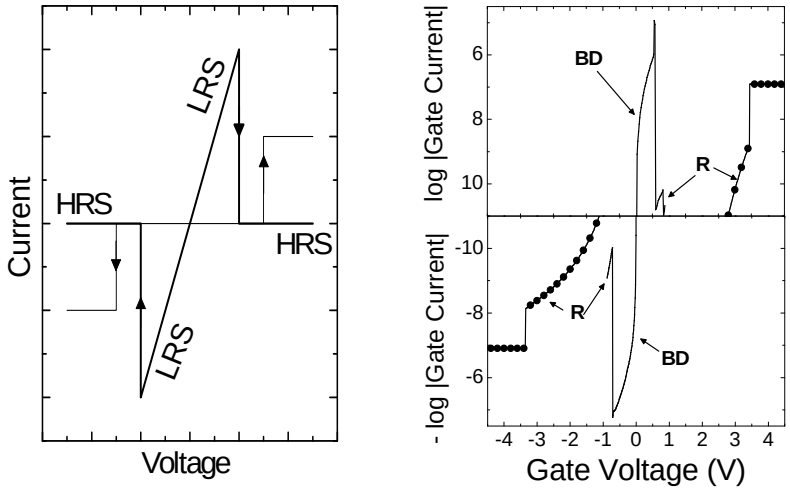


Figure 3

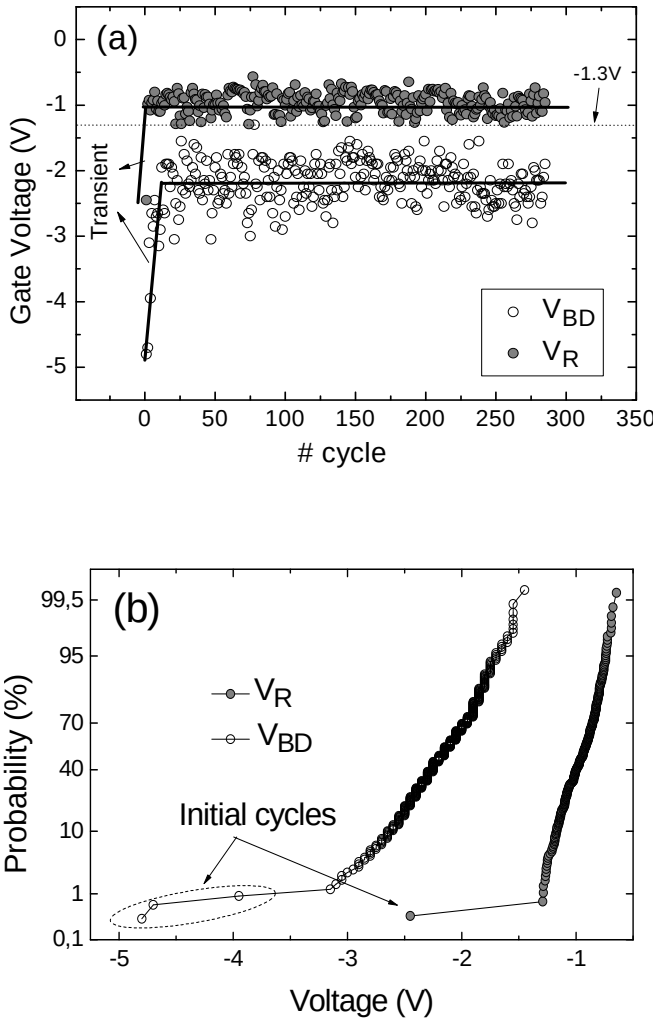


Figure 4

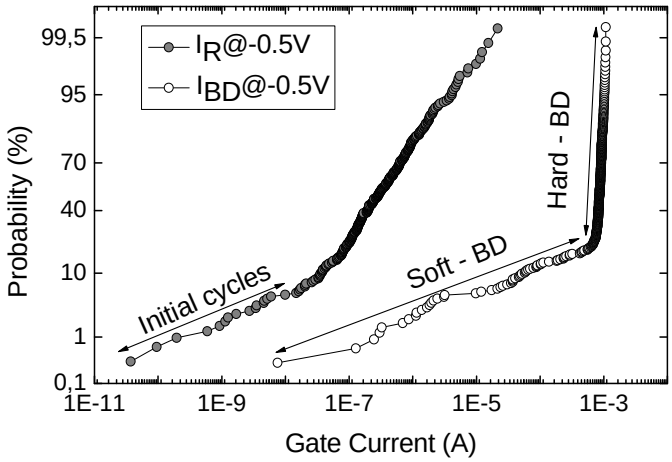


Figure 5

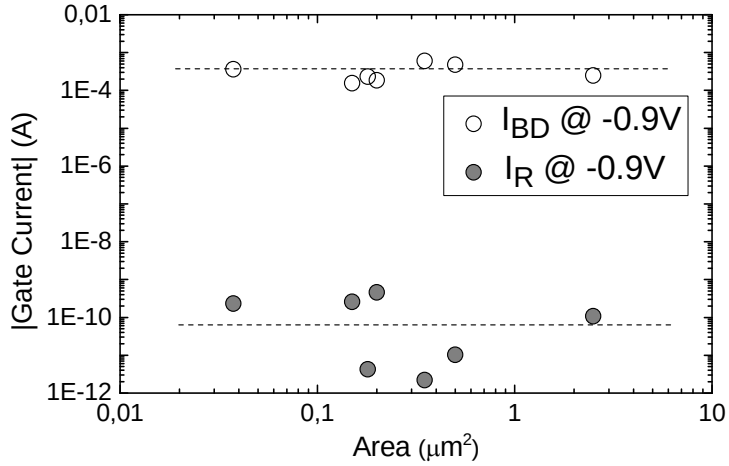


Figure 6

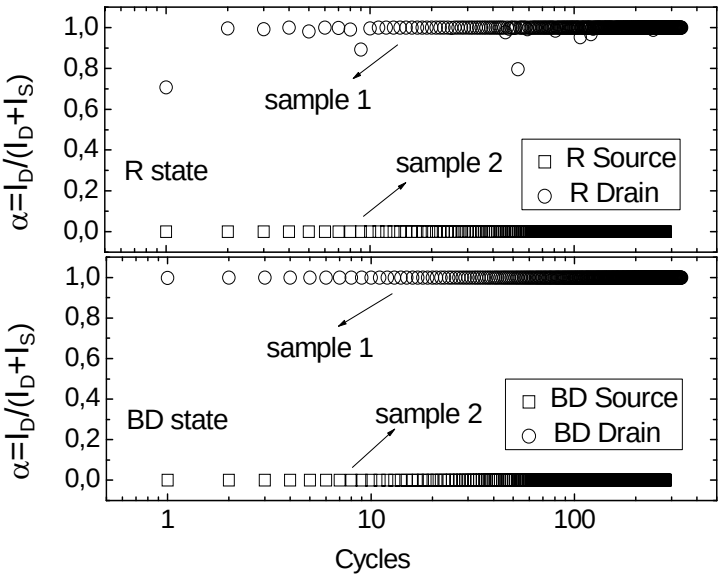
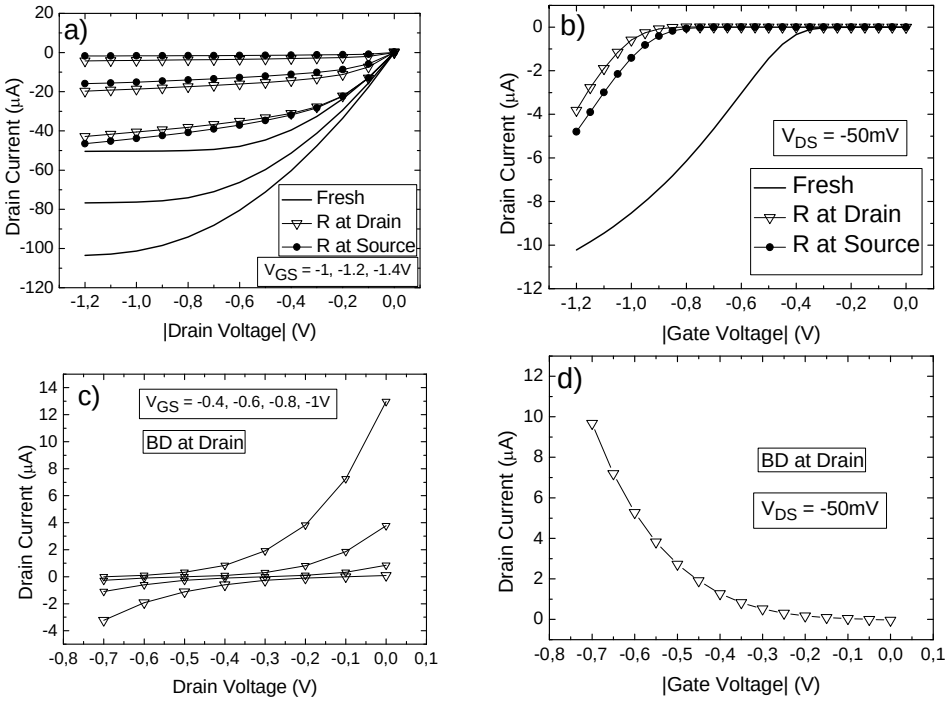

α=I_D/(I_D+I_S)
1,0
0,8
0,6
0,4
0,2
0,0
sample 1
R state
sample 2
R Source
R Drain
BD state
BD Source
BD Drain
1
10
100
Cycles

Figure 7


a)
Drain Current (μA)
|Drain Voltage| (V)
Fresh
R at Drain
R at Source
V_GS = -1, -1.2, -1.4V
b)
V_DS = -50mV
|Gate Voltage| (V)
c)
V_GS = -0.4, -0.6, -0.8, -1V
BD at Drain
Drain Voltage (V)
d)
BD at Drain
V_DS = -50mV

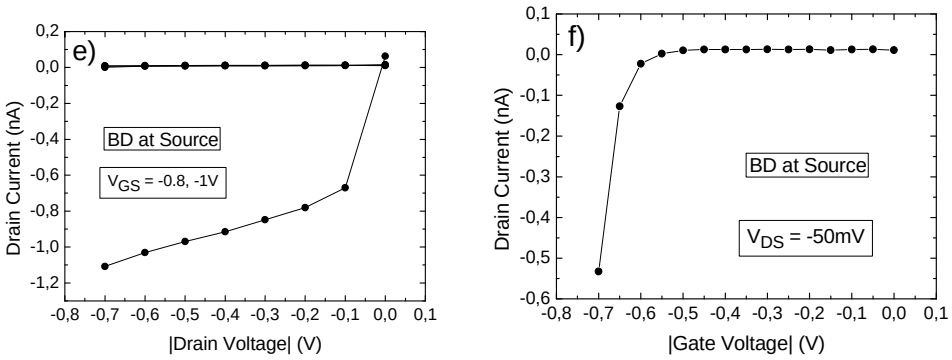

e)
BD at Source
V_{GS} = -0.8, -1V
Drain Current (nA)
|Drain Voltage| (V)
f)
BD at Source
V_{DS} = -50mV
Drain Current (nA)
|Gate Voltage| (V)

Figure 8