Dielectric Breakdown In Ultra-thin Hf Based Gate Stacks: A Resistive Switching Phenomenon.

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ABSTRACT

The gate dielectric breakdown (BD) reversibility in MOSFETs with ultra-thin hafnium based high-k dielectric is studied. The phenomenology is analyzed in detail and the similarities with the resistive switching phenomenon emphasized. The results show that after BD, the switch between two different conductive states in the dielectric is possible. We have demonstrated that the conduction in both states is local, which has been verified through CAFM measurements. Additionally, the injected charge to the first recovery (Q_R) has been proposed as a parameter to describe the BD reversibility phenomenon. The BD recovery partially restores not only the current through the gate, but also the MOSFET channel related characteristics. The electrical performance of MOSFETs after the dielectric recovery has been modeled and introduced in a circuit simulator. The simulation of several digital circuits shows that their functionality, though somehow affected, can be restored after BD recovery.

Introduction

In ultra-scaled CMOS technologies, the gate dielectric breakdown (BD) is one of the most relevant failure mechanisms, which is characterized by a change of the dielectric conductivity from a low to a high conductivity state (whose currents can differ in several orders of magnitude) (1). BD is attributed to the creation of a conductive path through the gate dielectric (2,3) and can have a very detrimental effect on the device performance (4,5). From the BD statistical results, BD was estimated to be an extremely local phenomenon (2), which takes place in areas of about 10-100nm^2. Experimental results obtained with CAFM (Conductive Atomic Force Microscope), which can provide topographical and electrical information of gate dielectrics with a resolution of about 10nm, confirmed this hypothesis (6). Traditionally, the conductivity change due to the BD has been considered to be irreversible, i.e., after the BD, the gate dielectric reaches a permanent high conductivity state leading to the device failure. However, several years ago it was shown that in SiO_2, in some occasions, BD could be reversible (7), i.e., a lower conductivity state could be reached after a BD event. In this regard, CAFM measurements have also shown the SiO_2 BD reversibility (6).

Recently, high-k dielectrics have been introduced to overcome the leakage problems associated to the scaling of SiO_2 as gate dielectric and, therefore, it is necessary a complete analysis of the dielectric BD in these high-k materials (8,9). As for SiO_2, BD has been related to the creation of a conductive path in the dielectric, as a consequence of the generation of defects during stress, that connects both electrodes (2,3). Recently, it has been reported that dielectric BD in ultrathin Hf based high-k gate dielectric stacks can be a reversible phenomenon, and two interchangeable conductivity states can be reached in the

dielectric when applying the correct stress scheme and the current during the BD transient is limited (10, 11). Therefore, the resistance of the conductive path can be changed. However, the BD reversibility phenomenon in ultrathin dielectrics, as those used in ultrascaled MOSFETs, is not well understood yet and, consequently, additional modeling and characterization efforts are needed. The change between different conduction states in the dielectric material also characterizes the resistive switching (RS) phenomenon, usually observed in MIM/MIS structures with rare earth thick oxides (several tenths of nanometers), which nowadays is being widely investigated as operating principle of resistive random access memory (RRAM) (12,13). Therefore, the exhaustive characterization of the RS phenomenon in ultra-thin high-k dielectrics has a twofold interest: on the one hand, for the development of memory devices based in this phenomenon and, on the other, from a reliability point of view, for the development of models that can help to evaluate the device and circuit performance and reliability taking into account the reversible nature of BD.

In this work, BD reversibility is studied in MOS structures (capacitors and transistors) with ultra-thin Hf-based high-k dielectric. The similarities with the RS phenomenon are also exposed. The procedure to induce two interchangeable conductivity states in these samples and the statistical distribution of voltage and current parameters that characterize the BD reversibility are described. Using the common BD characterization methods (derived from the local nature of BD (14)) combined with CAFM, the conductive path features for both conduction states are studied. The charge to recovery (Q_R) parameter is also presented as a magnitude to characterize the BD reversibility phenomenon. Finally, the effect of BD and BD recovery on the transistor performance and several circuits functionality has also been analyzed.

BD Reversibility Phenomenology

The samples used to describe the BD reversibility phenomenology were pMOSFETs with FUlly SIlicide (FUSI) gate electrode and a dielectric stack formed of a (2.9nm) HfSiON film on top of a 1.2 nm SiO_2 interfacial layer (EOT=1.9 nm). Different combinations of channel width and length have been studied, ranging between W/L=0.25μm/0.15μm and W/L=1μm/0.5μm. Unless stated, the results shown in the paper correspond to these samples. The samples were subjected to a sequence of current limited ramped voltage stress (CL-RVS) to induce the BD (high conductivity state), plus ramped voltage stress (RVS) without current limitation, to switch to the low conductivity state, following a measurement-stress-measurement scheme, as shown in Figure 1. Though this work is focused in the characterization of the phenomenon by means of ramp voltage tests, the BD recovery can be also observed if the gate voltage is kept constant during the stresses (15). In fact, to calculate the injected charge until BD recovery, a stepped ramp voltage (S-RVS) without current limitation instead of a RVS was applied (Figure 1). S-RVS can be viewed as a series of short CVS with increasing voltage. During the S-RVS, the gate voltage is increased in aprox. 0.1 V every ~150 seconds and the duration of the S-RVS in all the cases was 1200s (Figure 9). S-RVS were chosen instead of a standard constant gate voltage stress to warrant the BD recovery in a reasonable testing time, because the selection of the voltage at which the recovery can be observed is critical. The stresses were applied to the gate with the rest of the transistor terminals grounded and I_G, I_D, and I_S were simultaneously registered. To observe the changes in the device performance after the different stresses, the I_D-V_D and I_D-V_G characteristics of the fresh sample and those after the successive CL-RVS and RVS or S-RVS steps of the sequence were measured.

Figure 2 shows typical gate currents measured on the same sample during the CL-RVS and RVS for the initial cycles of the measurement sequence illustrated in Figure 1. Curve I_F (thick line) corresponds to the gate current registered during the first CL-RVS (fresh device). When dielectric BD takes place, at V_{BD}, a fast increase of the current through the oxide is observed until reaching the current limit (in this case 500μA). Once BD is reached, the CL-RVS is stopped and a RVS without current limit is applied. At low voltages, the post-BD gate current (I_{BD}) obtained during the RVS is, as expected, much larger than I_F. This large current indicates that the oxide losses its insulator properties, due to the formation of a conductive path through the oxide, that behaves as a low resistance. However, if the gate voltage further increases, at a given voltage (V_R), the I_{BD} current suddenly decreases several orders of magnitude. During the CL-RVS in the next cycle, at low voltages, the gate current (I_R) is larger than the fresh current, but lower than I_{BD}. This indicates a partial recovery of the insulator properties of the gate dielectric, suggesting that, in some conditions, BD in ultra-thin Hf-based high-k oxides is a reversible phenomenon, i.e., the BD path that was 'opened' can be 'closed'. If V_G continues increasing during the CL-RVS and V_{BD} is reached, BD is observed, so that a high current level is measured once again. However, in the following RVS, after V_R, the current decreases once more. This behavior can be observed for many iterations of the stress sequence (more than 250 cycles in this work). In each cycle, the CL-RVS and RVS are stopped once V_{BD} and V_R are reached respectively. This stop process can take few seconds but this delay is irrelevant for the conclusions obtained in the paper. Moreover, the phenomenon is qualitatively repetitive from sample to sample. These results indicate that, after a current limited BD, two conduction states are allowed in the dielectric, a high conductivity one (BD state, with gate current I_{BD}) and a low one (R state, with gate current

I_R). Switching between both states occurs when the two threshold voltages are reached (V_{BD} and V_R). All our experiments point out that if BD is induced without applying any current limit BD becomes irreversible and switching does not occur anymore (11).

Area Dependence and Conduction Path Location

Dielectric BD is known to be a local phenomenon, that is, the current after BD mainly flows through a small portion of the dielectric area (2,3). However, the nature of the dielectric conduction during the R state is still an open question. To investigate this point, the transistors described in the previous section with different areas have been analyzed to obtain more information about the nature of the R state. Figure 3 shows I_{BD} and I_R as a function of the transistor area. No area dependence of I_{BD} and I_R is observed, which indicates that the current through the oxide after the first BD is a localized phenomenon, whatever the state of the oxide conduction: BD or R. However, the results shown in Figure 3 do not provide information whether the current flows through the same path in both states. To check this point the location of the conductive path in the dielectric along the channel (14) has been studied. To do so, the magnitude α, defined as $I_D/(I_D+I_S)$, has been calculated for all the cycles at the BD and R states. α values close to 1 or 0 indicate that the conductive path is located close to the drain or source, respectively. Figure 4 shows the α evolution during cycling for the R (top) and BD (bottom) states for two MOSFETs. In each sample, the location of the conductive path through the oxide during the BD and R states is the same and does not change during the successive measuring cycles. This confirms the local nature of the BD state, but also of the R state, and indicates that the conduction in both states should be attributed to the same path, i.e. the conductive path is ‘opened’ during the BD state and ‘closed’ during the R state. So that,

the partial recovery of the high-k stack properties in the R state should be attributed to changes in the atomic structure of the conductive path (16).

To further support the hypothesis that the BD reversibility observed in Figure 2 can be related to changes in the conduction properties of a conductive path with very reduced dimensions, high-k gate stacks have been analyzed with CAFM. Since the CAFM has a nanometer spatial resolution, it allows to (i), trigger BD events at given locations (area ~ 300 nm^2(17)) of the stack by applying a RVS and (ii), study the electrical properties of those broken down locations with nanometer resolution. Therefore, any change detected in the electrical conduction of the studied positions can be clearly related to the BD spots triggered with the CAFM and not to other positions of the gate stack.

In this analysis, the samples consisted of a gate stack of a 2.5-nm-thick HfO_2 layer grown by atomic layer chemical vapour deposition on a nominal 0.6nm SiO_2 interface layer. P-type silicon wafers ($N_A=10^{15}$ cm^{-3}) were used as substrate. Note that no gate electrode was deposited on top of the stack. The tip will play the role of gate electrode (see Figure 5). This analysis has been performed with a modified CAFM (Figure 5), where the common means to bias the tip-sample system and to measure the current through the sample have been substituted by source monitor units (SMUs). With this setup (ECAFM, from enhanced CAFM (17)) the standard electrical tests on gated devices can be reproduced at the nanoscale (areas of ~ 300 nm^2). Moreover, larger current ranges than in standard CAFM configurations are possible: currents from 100 fA up to 1 mA can be repetitively measured, which is very suitable to study post-BD currents.

To measure the electrical properties of the gate stack (before and after the dielectric BD), series of ramped voltage stresses (RVS) were applied on a fixed site to obtain consecutive I–V characteristics. As an example, Figure 6 shows five consecutive I-V

curves measured on a given position of the gate stack. The first I-V curve (before BD) shows different conduction regimes associated to carrier injection through the different layers of the stack, which in these measurements, contrarily to those on MIS structures (Figure 2) and due to the high lateral resolution of the technique (Figure 5), can be clearly distinguished. (17). At high fields, however, current increases progressively due to the degradation of the gate stack. Because of the electrical stress applied during the RVS sequence, the following I-V curves (# 2 and 3), progressively show larger currents at low fields, related to the degradation of the high-k layer (17). Once BD is triggered, typical post-BD curve is measured during the subsequent RVS and lower currents are not measured anymore, i.e. BD is irreversible (fifth I-V curve). However, sometimes, the pre-BD electrical conduction can be recovered and switchings between different conduction states are observed. As an example, the 4th I-V curve in Figure 6 corresponds to a typical post-BD I-V up to 4 V. At this voltage, the stack recovers the conductivity of the fresh location. As the voltage increases, current increases again showing several conduction switchings until the final post-BD characteristic is reached. The phenomenology described in Figure 6 for the high-k gate stack is similar to that observed in single SiO_2 layers stressed with a series resistance, which points out that the SiO_2 layer can actually control the stack BD (17). By extrapolating the SiO_2 results interpretation, switchings can be explained by a reversibility of the BD event, i.e., a BD path has been created, but it can be switched ON and OFF, demonstrating the extremely local nature of the BD recovery phenomenon. The results also suggest that the HfO_2 layer and/or the AFM tip could act in a similar way to a series resistance that impedes the fully development of the BD path, allowing the observation of the BD reversibility. This series resistance could be somehow equivalent to the current limit applied at device level to ensure the reversibility of the BD

phenomenon. However, if stress is continued, the BD path is completely formed and BD becomes irreversible.

Therefore, the qualitative equivalent results obtained in large area (Figure 2) and nanometer sized structures (Figure 6) confirms the local nature of the BD and BD reversibility process in high-K dielectrics.

The described BD reversibility phenomenology has strong similarities with the RS phenomenon: (i) in both cases two conductivity states in the dielectric exist (LRS and HRS in RS terminology, or BD and R respectively, in the terminology adopted for the dielectric breakdown) (ii) in both cases a 'forming process' is needed. In the case of BD, this forming process would correspond to the creation of the conductive path through the oxide during the first stress, which would be equivalent to the formation of a filamentary conductive path through the dielectric, as proposed by some researchers for the RS phenomenon (12). (iii) The switching between the LRS and HRS states in the RS phenomenon is achieved by applying two threshold voltages. From the BD point of view, these two voltages are identified as V_R and V_{BD} (as marked in Fig. 2). (iv) In both phenomena, the set of a current limitation (CL-RVS) is a key parameter to observe the switching between both states. The main difference between RS and BD concerns to the samples used for their characterization: RS is typically studied in MIM structures with thick insulators whereas BD is usually analyzed in high-performance logic devices.

Voltages and Currents Distributions

In this section, the currents at both conductivity states and the threshold voltages needed to switch between the two conductivity states are analyzed, as parameters that

describe the dielectric behavior. Figure 7 (a) shows the V_{BD} and V_R values (defined in Figure 1) obtained on a single device subjected to more than 250 cycles of the stress sequence. The values of V_{BD} and V_R rapidly decrease (in absolute value) in the first cycles but their mean values remain approximately constant in the following ones. The dashed line in Figure 7 (a) indicates the maximum voltage value imposed (|1.3V|) to the RVS after the transient in order to avoid irreversible BD events. Figure 7 (b) shows the cumulative distribution of V_{BD} and V_R (in this representation, a normal distribution corresponds to a straight line). As can be observed, the mean values of the distributions are separated around 1.2V and the spread is larger for V_{BD}.

The cumulative probability distributions of I_{BD} and I_R measured at -0.5V are shown in Figure 8. In this case, the transient behavior during the first cycles, as observed in the voltage distributions, is not so evident, and the tail observed in the I_R distribution corresponds to values randomly measured between the 1^{st} and the 120^{th} cycles. Concerning to the I_{BD} distribution, two regions can be clearly distinguished: on the one hand, a region with a larger slope which corresponds to higher post-BD gate currents and, on the other hand, a second region with a lower slope which corresponds to lower post-BD gate currents. Note that these lower current levels correspond to the BD state. Attending to the measured current levels, the tails of the I_{BD} distribution shown in Figure 8 have been attributed to soft breakdown (SBD) events, whereas the larger currents in the larger slope region correspond to hard breakdown (HBD). Note that we have used the terms SBD and HBD to refer to the different BD modes observed during the BD state and that the HBD current is limited by the external current limitation imposed during the CL-RVS (11)

Charge-to-Recovery Analysis

In this section, the results obtained when a S-RVS is applied (instead of a RVS) to recover the low conductivity state are presented. In order to characterize the BD reversibility, in analogy to the charge-to-BD as the parameter to characterize the BD events (1), we propose to use the charge-to-recovery, Q_R, defined as the charge injected in the dielectric during the BD state until the first recovery event is observed (R in Figure 9). During the S-RVS, the gate voltage is increased in aprox. 0.1 V every ~150 seconds (Figure 9), so that Q_R can be obtained as the addition until the first recovery event of the injected charge during the different steps of the S-RVS, that is, as the integral of the current (in absolute value) until the time in which the first recovery event is detected. In Figure 9, after the BD reversibility (R state) the gate current seems to be independent of the gate voltage and shows fluctuations that could be caused by electronic instabilities in the previously opened conductive path. The appearance of these instabilities is a random process, so that Q_R has been defined as the injected charge until the first recovery event to avoid the influence of these instabilities in the Q_R calculation. In the next paragraphs, the dependence of Q_R on the polarity of the S-RVS and the current limit during the previous CL-RVS will be analysed.

S-RVS Polarity Dependence of Q_R

To analyse the dependence of Q_R on the S-RVS polarity, BD was always produced by a negative CL-RVS whereas positive or negative S-RVS were applied to reverse BD. Figure 10 shows the Q_R values (calculated as it is explained in the previous paragraph) obtained after successive cycles in two samples, one of them subjected to positive S-RVS

(open symbols) and the other to negative S-RVS (solid symbols). In the case of positive S-RVS, the BD-recovery sequence was reproducible during more than 600 cycles. From our measurements, no dependence of Q_R on the number of stress cycles was inferred, independently of the polarity of the S-RVS. However, lower dispersion of Q_R values is obtained when the polarity of the CL-RVS and the S-RVS are opposite. To show more clearly this result, the Q_R distributions of the data shown in Figure 10 were drawn in a Weibull plot (Figure 11). A larger dispersion of Q_R can be clearly observed for the samples subjected to negative voltage S-RVS (same polarity as the CL-RVS).

Dependence of Q_R on the CL-RVS Current Limit

The dependence of Q_R on the current limit fixed during the CL-RVS that lead to BD has been analyzed. In this study, the samples were subjected to negative CL-RVS to provoke BD (changing the current limit from sample to sample) followed by a positive S-RVS to reverse BD. Figure 12 shows the Q_R distributions obtained in three different samples after successive cycles, whose BD was induced using different current limits. A clear increase of the average value of Q_R with the current limit can be observed.

Dependence of Post-BD and Post-recovery I_G on the CL-RVS Current Limit

We have also investigated the dependence of the post-BD and recovered gate currents on the CL-RVS current limit, from the I_G-V_G characteristic registered after each CL-RVS (BD state) and S-RVS (R state). The post-BD and recovered gate currents were measured at V_G = -0,5V in the same samples where the Q_R distributions in Figure 12 were obtained. Figure 13 and Figure 14 show the post-BD and recovered gate current distributions,

respectively, for CL-RVS current limits of 0.5, 1 and 2 mA. At the BD state (Figure 13), the gate current clearly increases with the current limit established during the CL-RVS, as has been observed for Q_R (Figure 12). Two regions can be clearly distinguished in Figure 13 for the distributions with the lower current limits of the CL-RVS: on one hand a region with a larger slope which corresponds to higher post-BD gate currents and on the other hand a second region with a lower slope which corresponds to lower post-BD gate currents. As it was previously explained, the current levels in the tails of the distribution shown in Figure 13 have been attributed to SBD events, whereas larger currents in the higher slope regions correspond to HBD. Therefore, from Figure 13, it can be deduced that the probability to get HBD events increases with the current limit used to provoke the BD, as expected. On the contrary, at the R state (Figure 14) no relevant dependences of the gate current with the current limit are inferred. In summary, the current limit used to switch the sample to the BD state will influence Q_R, the BD mode and, consequently, the post-BD gate current, but it will not affect the current at the R state.

Impact of BD Recovery on the Transistor Characteristics

BD can lead to the device failure not only because of the large increment of the gate leakage current, but also because, after BD, the transistor characteristics can be completely distorted and the circuit can loss its functionality (5). However, the partial recovery of the insulating properties when the BD path ‘closes’ could also imply the restoration of the MOSFET/circuit functionality. Therefore, to evaluate if BD reversibility can introduce an improvement of the device reliability, the transistor conduction along the channel when the dielectric is at the R state must be studied. To do so, the transistor characteristics related to the channel conduction have been analyzed for

both dielectric states, BD and R. The BD reversibility effect on the performance of the transistor has been evaluated from the I_D-V_D and I_D-V_G monitor curves. Figure 15a (solid circles) shows the I_D-V_D characteristic of a fresh transistor, for different V_G. The I_D-V_D curve of the same transistor after a very hard dielectric BD located close to the drain (Figure 15b) shows that, during the BD state, the transistor characteristics are completely distorted. However, if the sample is switched to the R state, the I_D-V_D curve is partially recovered (open circles in Figure 15a). Similar conclusions can be drawn for the I_D-V_G curves (not shown). These results indicate that switching to the R state restores the device functionality, although degraded.

BD Recovery effect on Circuit Performance

In order to transfer the BD reversibility effects on the transistor up to circuit levels, they have been included in the SPICE model that describes the MOSFET performance. The modified model has been used to study the effects of BD/BD recovery on the circuit performance. A ring oscillator and simple logic gates have been considered as examples.

The fresh, BD and recovered transistor characteristics have been described using a combination of the BSIM4 MOSFET compact model (to describe the channel current) plus the D-R gate current model (to account for the BD gate current) (5) (zoom in Figure 16. top), with model parameters extracted from the experimental data. The modeled characteristics of transistors at the BD and R states (lines in Fig. 15) have been introduced in a circuit simulator to study the performance of a five stage ring oscillator. The BD path has been considered to be located at the drain of the third stage pMOS (Fig 16 top). The circuit output (Figure 16 bottom) shows that, when at BD, the circuit does

not oscillate anymore. However, when back to the R state, the circuit oscillates again, but with a ~2 times lower frequency, which indicates that, after the dielectric recovery, the functionality of the circuit can be restored, although damaged. The functional recovery of logic gates has been also observed. Table 1 summarizes the results obtained in inverters, NAND and NOR gates, always considering that BD takes place in the drain of a pMOS transistor. For all the circuits under study, some of the outputs are erroneous after dielectric BD (shaded cells). However, the correct logic outputs are always restored when the transistor is switched to the R state.

Conclusions

In MOSFETs with ultra-thin high-k Hf based dielectrics, after the BD path has been created, two conductivity states are observed in the insulator, BD and R, being the current during the BD state (I_{BD}) larger than during the R state (I_R). Switching between the two states is possible when two threshold voltages are reached, V_{BD} and V_R, and only if the current was limited during the BD transient. The effect has strong similarities with the resistive switching phenomenon observed in MIM structures with thick oxides. The area dependence of the I_{BD} and I_R currents and their location along the transistor channel shows that the conduction in both states is local and controlled by the same BD path. This local behavior of the phenomena has been verified through CAFM characterization. The value of V_{BD} and V_R shows a transient behavior (that decrease quickly in the first cycles of switching between the BD and R states), not so clearly observed in the distributions of I_{BD} and I_R. In the I_{BD} distributions, two BD modes are distinguished, that have been associated here to SBD and HBD, attending to the measured current. The injected charge

to the first recovery (Q_R) during the S-RVS has been proposed as parameter to describe the BD reversibility phenomenon, and has been used to study some details of the BD-recovery process. No dependence of Q_R with the number of iterations of the BD-recovery sequence has been observed. In addition, lower Q_R dispersion is obtained when the polarities of the CL-RVS and the S-RVS are opposite. On the other hand, Q_R and the BD state current increase with the current limit fixed during the CL-RVS. At the BD state, the probability of HBD increases with the current limit. However, a negligible dependence of the current during the R state with the CL-RVS current limit has been measured. Finally, the electrical characteristics of MOSFETs show that, when the oxide conductivity returns to the R state, not only the gate current (I_G-V_G characteristics) is recovered but also the channel current (I_D-V_D curves) though with reduced current drive capability. The MOSFET can be modeled, independently of the dielectric conductivity state (BD or R) using a combination of the BSIM4 SPICE compact model and BD D-R models, with the adequate parameter set. This description has been included in a circuit simulator to analyze the effect of the dielectric BD recovery on the functionality of different logic gates. The simulations show that the circuit response, which sometimes can be wrong after BD, can be restored though somehow affected if the gate conductivity is switched to the R state. This result suggests that, after a gate BD event, the circuit functionality could be recovered and, consequently, depending on the failure criteria, the circuit lifetime increased.

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FIGURE CAPTIONS

Figure 1. Stress sequence for the analysis of the dielectric BD reversibility. The compliance of the measuring equipment (Keithley 4200-SCS) was used to limit the current during the CL-RVS. RVS or Stepped-RVS were applied to reverse BD.

Figure 2. I_G-V_G curves measured in a pMOSFET with W/L=1μm/0.5μm after successive CLR-RVS + RVS iterations. A high current is registered after the current limited BD (I_{BD}), which suddenly drops after V_R. During the CL-RVS in the next cycle, at low voltages, the gate current (I_R) is larger than the fresh current, but lower than I_{BD}, which indicates a partial recovery of the dielectric properties. The switching between both conductivity states can be provoked in successive cycles of CL-RVS + RVS.

Figure 3. I_{BD} and I_R measured at V_G=-0.9V as a function of the transistor area. No area dependence is observed in any of the two conductivity states.

Figure 4. The quotient $\alpha=I_D/(I_D+I_S)$ allows to locate the conduction path in the dielectric along the channel [7]. Two samples, with BD located at the extremes of the channel, are considered. For each sample, the location of the conduction path in the BD (bottom) and R (top) states is the same and does not change during successive cycles.

Figure 5. Schematics of an ECAFM. Shadowed modules (SMU) indicate the extra components with respect to a standard AFM.

Figure 6. I-V curves measured with a CAFM during a RVS sequence on a location of the HfO_2/SiO_2 stack (without gate electrode on top). Note that with this technique, only the current through the BD path is measured, revealing details which are hidden to the

standard techniques. The successive ramps continuously evolve from the virgin curve (first I–V) to the final post-BD characteristic.

Figure 7. (a) BD voltage (V_{BD}) and R voltage (V_R) evolution during cycling on the high-K MOSFETs. A transient behaviour is observed at the initial cycles, later the mean values of V_{BD} and V_R remain stable. (b) Cumulative probability of V_{BD} and V_R registered during cycling on the same device.

Figure 8. The cumulative probability function of I_{BD} (solid circles) and I_R (open circles) registered at V_G = -0.5V during more than 250 measuring cycles on the same MOSFET.

Figure 9. I_G obtained during the 13th cycle S-RVS of the sequence shown in Fig. 1. BD was provoked during the previous CL-RVS. Different recoveries (R and R') can be clearly observed.

Figure 10. Q_R as a function of the number of CL-RVS + S-RVS cycles. BD state was reached applying a negative CL-RVS in all the cases. However, positive (open cycles) or negative (close circles) S-RVS were applied to induce BD recovery. Q_R was evaluated during the S-RVS tests.

Figure 11. Weibull plot of the Q_R data shown in Figure 10. Samples were subjected to negative CL-RVS followed by positive (open symbols) or negative (solid symbols) S-RVS. Lower dispersion is observed when the polarities of the CL-RVS and S-RVS are opposite.

Figure 12. Q_R distributions obtained in samples broken down during CL-RVS with three different current limits. The polarity of the CL-RVS and the S-RVS was negative and positive, respectively. Higher current limit means larger average Q_R.

Figure 13. Post-BD I_G distributions, obtained after each CL-RVS for three different current limits, in the same samples of Figure 12.

Figure 14. Recovered I_G distributions, obtained after each S-RVS, in the same samples of Figure 12 and Figure 13.

Figure 15. (a) Experimental (circles) and simulated (lines) I_D-V_D characteristic, for a fresh (solid circles) and recovered (open circles) pMOS transistor. (b) Experimental (symbols) and simulated (lines) I_D-V_D curves of the same device at the BD state. Dielectric BD took place close to the drain.

Figure 16. Top: A 5 stage ring oscillator was simulated to analyse the effects of dielectric BD and recovery on the circuit functionality. BD has been considered to be located at the drain of the third stage pMOS transistor. The pMOS electrical characteristics have been described using BSIM4 and D-R models (zoom) (5). Bottom: Circuit response when the dielectric of the third stage pMOS transistor is fresh (■), and working at BD (▲), or at R states (●).

Table 1: Output logic states obtained for inverters, NAND and NOR gates for fresh transistors (F), after the dielectric BD in one of the pMOS transistors of the circuit (BD) and after switching to the R state of the broken transistors (R). The shaded cells indicate

wrong values of the output as a consequence of the BD. Correct logic states are restored when the gate is switched to the R state.

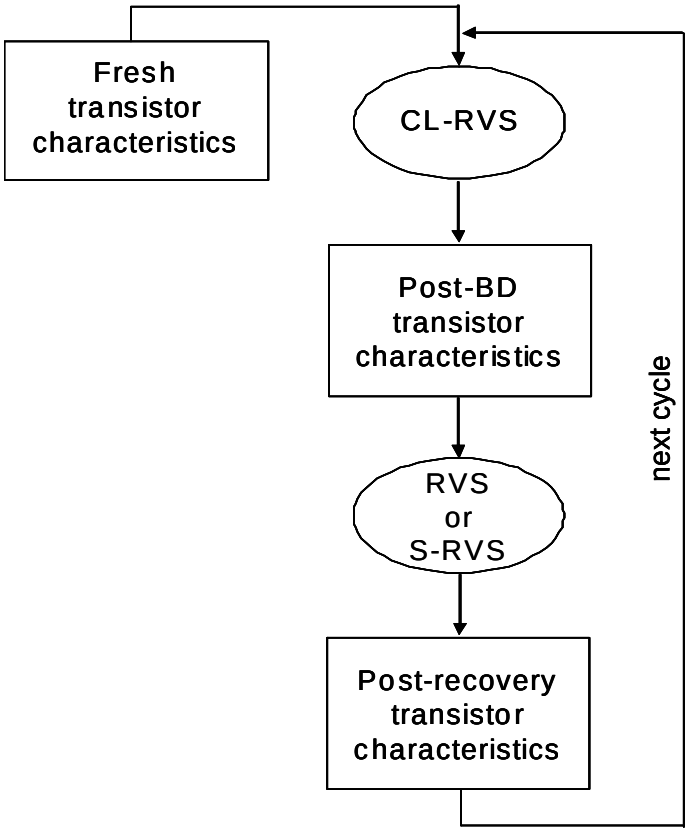
Fresh
transistor
characteristics
CL-RVS
Post-BD
transistor
characteristics
RVS
or
S-RVS
Post-recovery
transistor
characteristics
next cycle

Figure 1

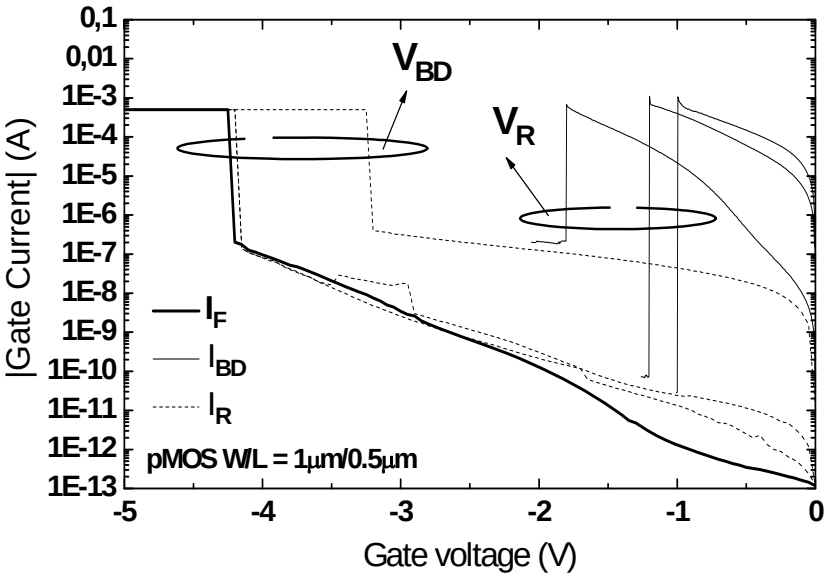
0,1
0,01
1E-3
1E-4
1E-5
1E-6
1E-7
1E-8
1E-9
1E-10
1E-11
1E-12
1E-13
|Gate Current| (A)
-5
-4
-3
-2
-1
0
Gate voltage (V)
V_BD
V_R
I_F
I_BD
I_R
pMOS W/L = 1μm/0.5μm

Figure 2

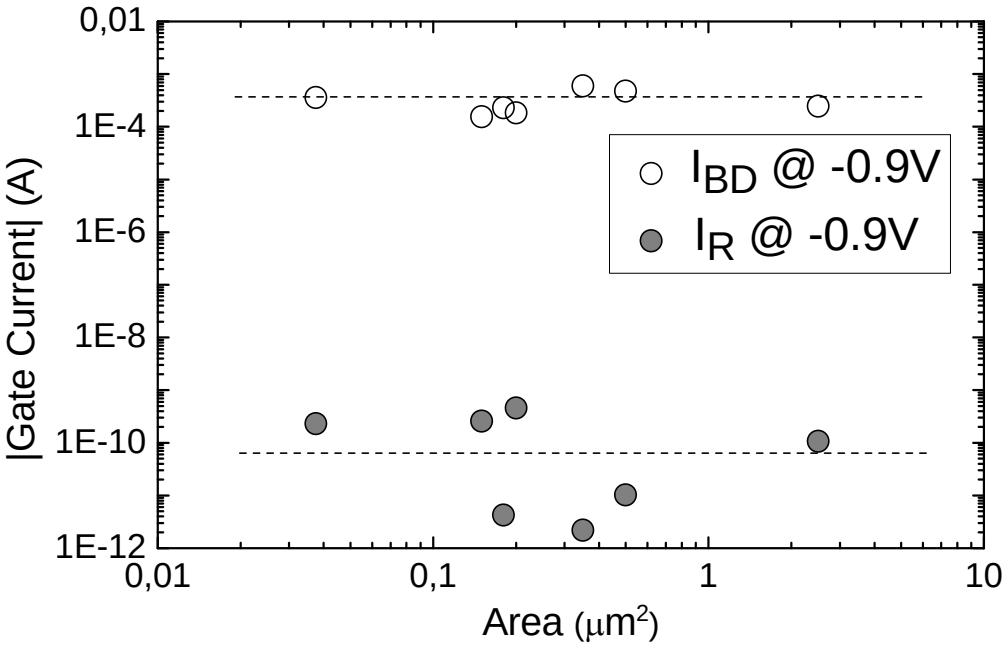
0,01
1E-4
1E-6
1E-8
1E-10
1E-12
|Gate Current| (A)
0,01
0,1
1
10
Area (μm²)
I_BD @ -0.9V
I_R @ -0.9V

Figure 3

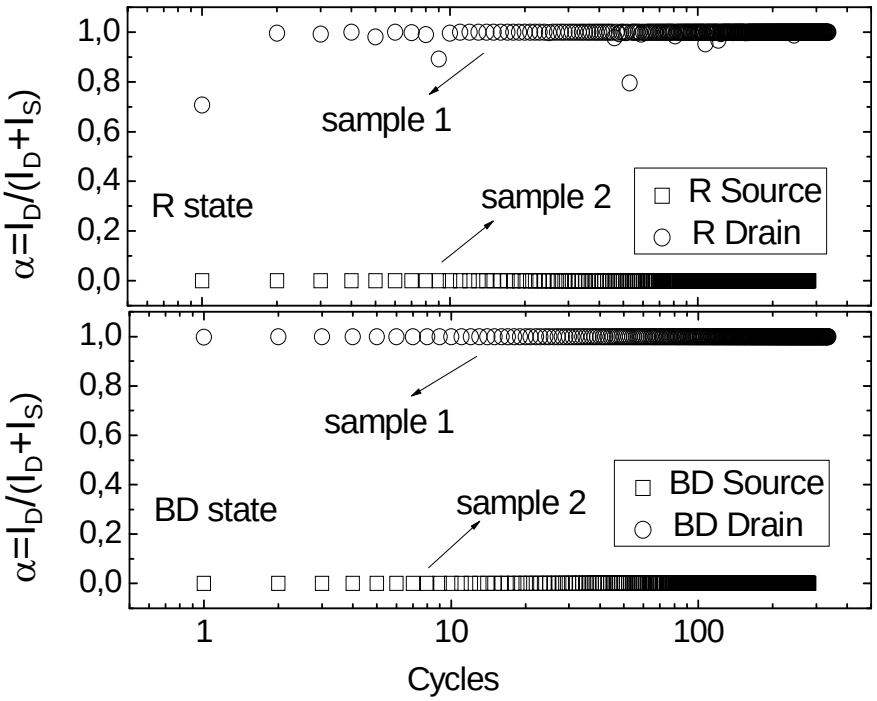
1,0
0,8
0,6
0,4
0,2
0,0
α=I_D/(I_D+I_S)
sample 1
R state
sample 2
R Source
R Drain
BD state
BD Source
BD Drain
1
10
100
Cycles

Figure 4

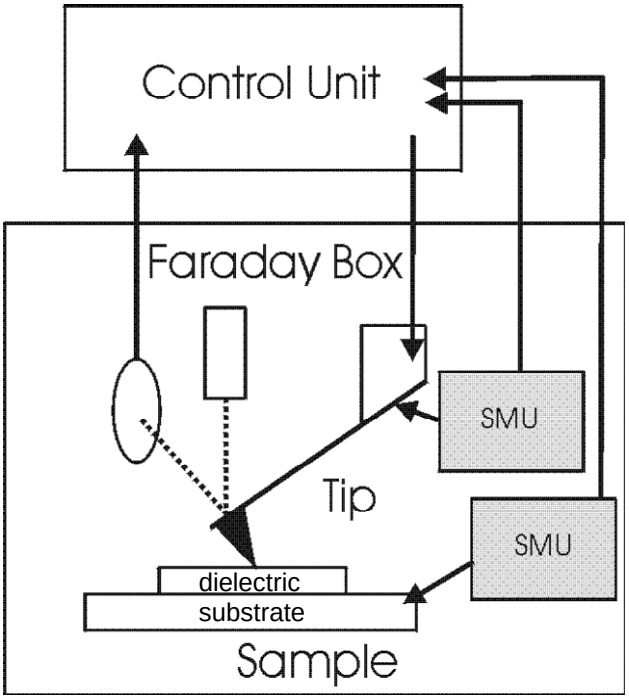
Control Unit
Faraday Box
SMU
Tip
SMU
dielectric
substrate
Sample

Figure 5

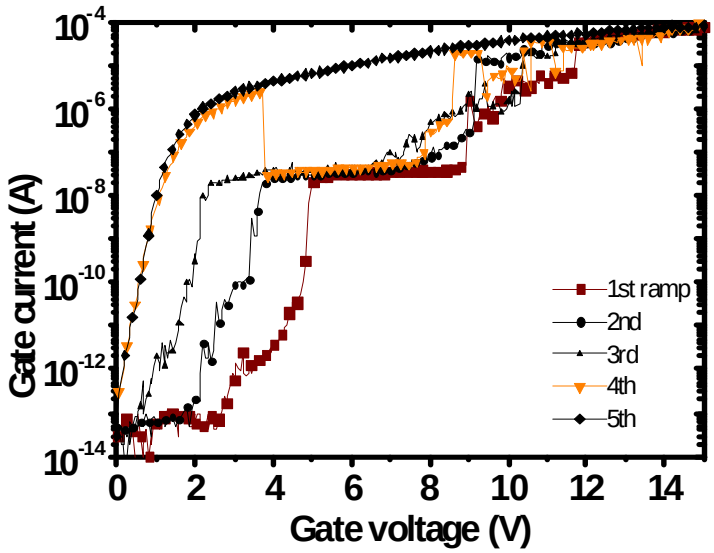
Gate current (A)
10^-4
10^-6
10^-8
10^-10
10^-12
10^-14
0
2
4
6
8
10
12
14
Gate voltage (V)
1st ramp
2nd
3rd
4th
5th

Figure 6

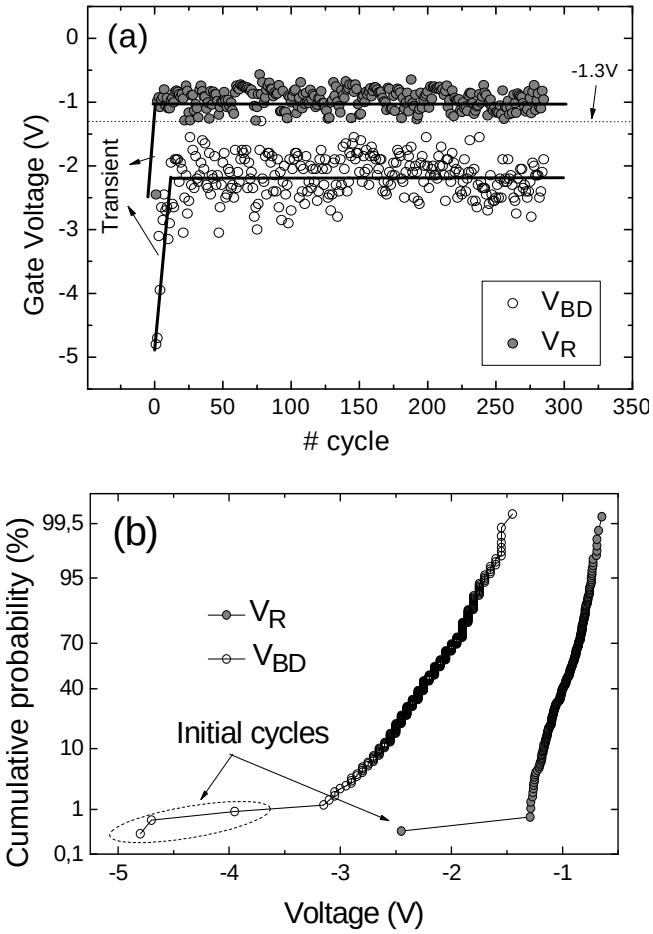
(a)
-1.3V
Transient
Gate Voltage (V)
cycle
V_{BD}
V_R
(b)
Cumulative probability (%)
Voltage (V)
V_R
V_{BD}
Initial cycles

Figure 7

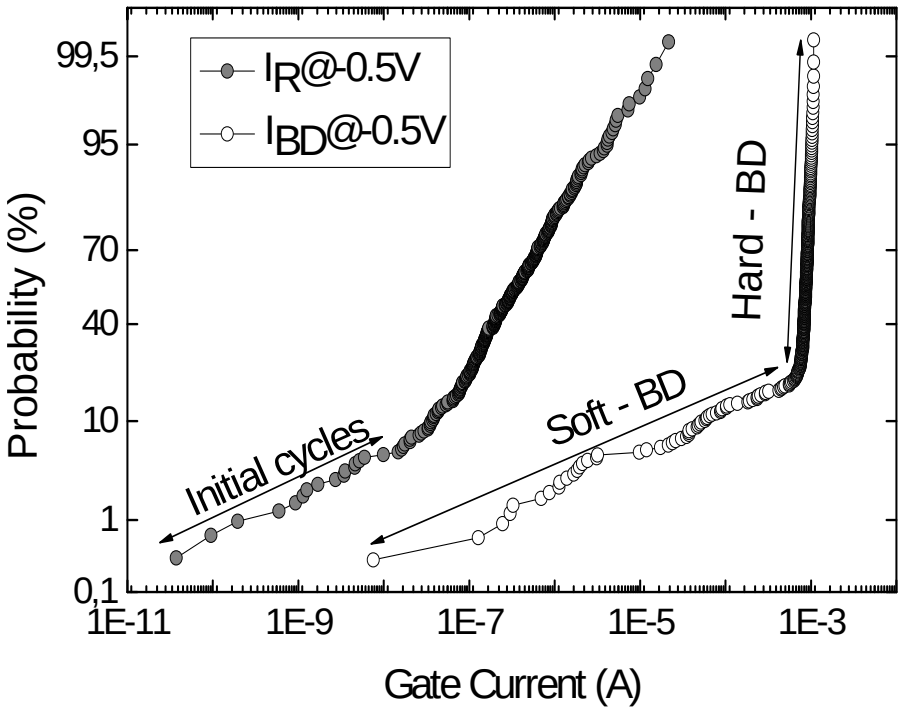
99,5
95
70
40
10
1
0,1
Probability (%)
1E-11
1E-9
1E-7
1E-5
1E-3
Gate Current (A)
I_R@-0.5V
I_BD@-0.5V
Initial cycles
Soft - BD
Hard - BD

Figure 8

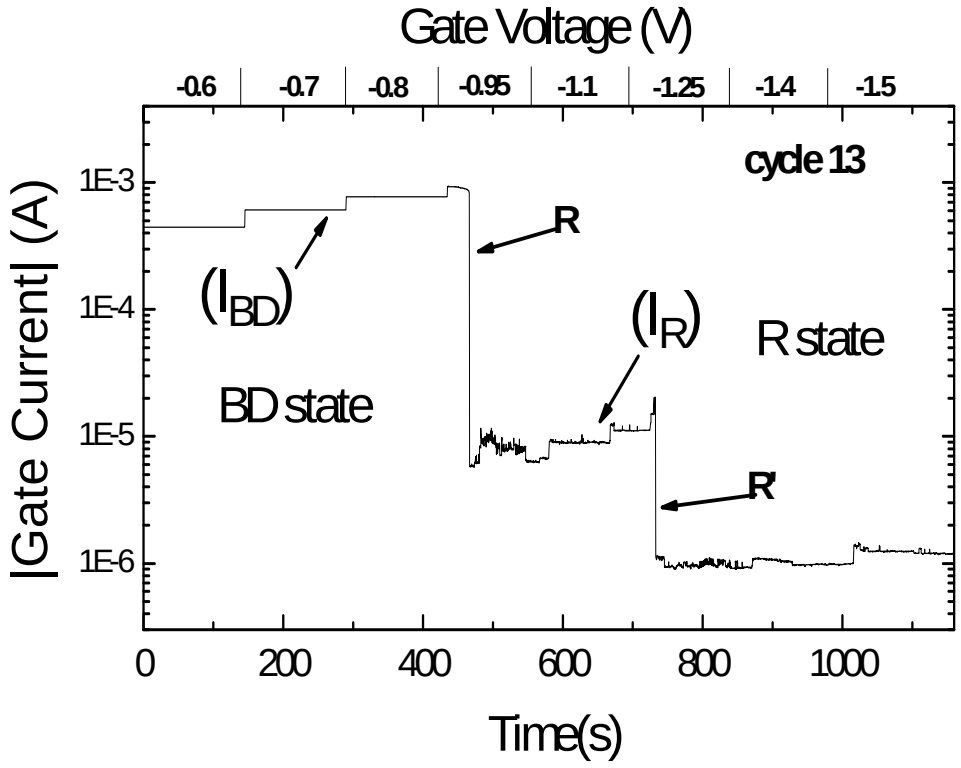
Gate Voltage (V)
-0.6
-0.7
-0.8
-0.95
-1.1
-1.25
-1.4
-1.5
cycle 13
|Gate Current| (A)
1E-3
1E-4
1E-5
1E-6
R
(I_BD)
(I_R)
R state
BD state
R'
0
200
400
600
800
1000
Time(s)

Figure 9

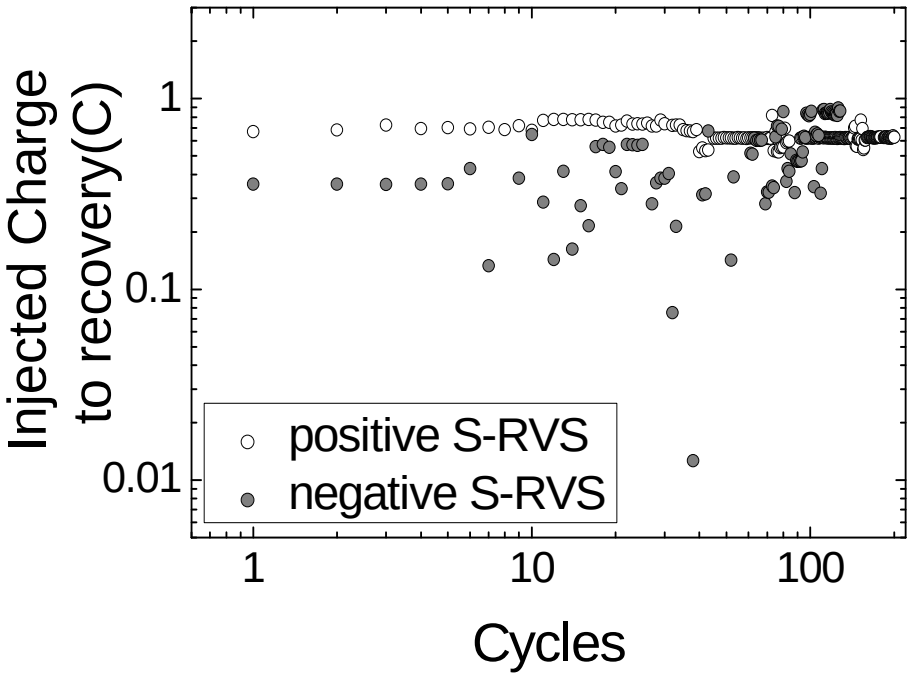
Injected Charge
to recovery(C)
1
0.1
0.01
1
10
100
Cycles
positive S-RVS
negative S-RVS

Figure 10

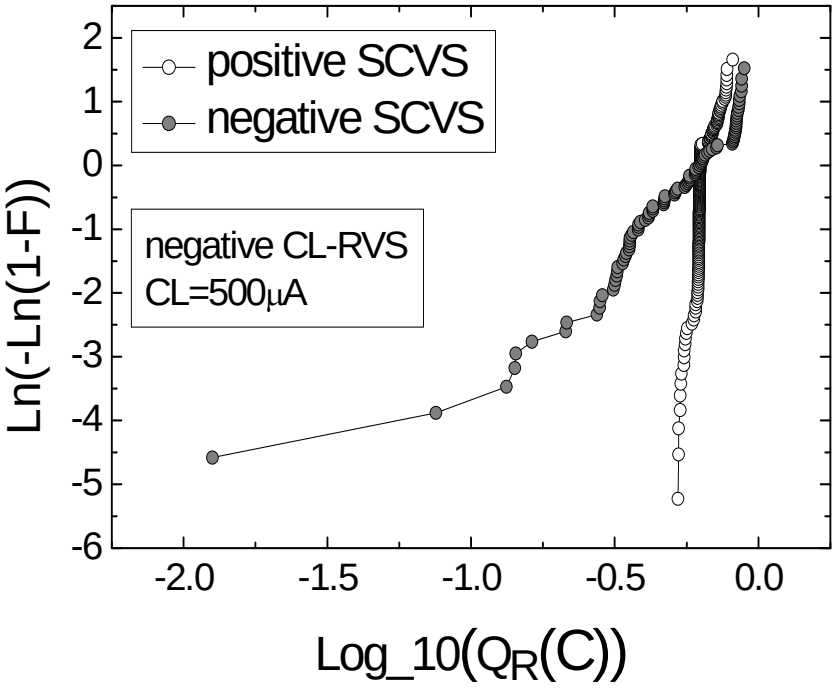
positive SCVS
negative SCVS
negative CL-RVS
CL=500μA
Ln(-Ln(1-F))
Log_10(Q_R(C))
2
1
0
-1
-2
-3
-4
-5
-6
-2.0
-1.5
-1.0
-0.5
0.0

Figure 11

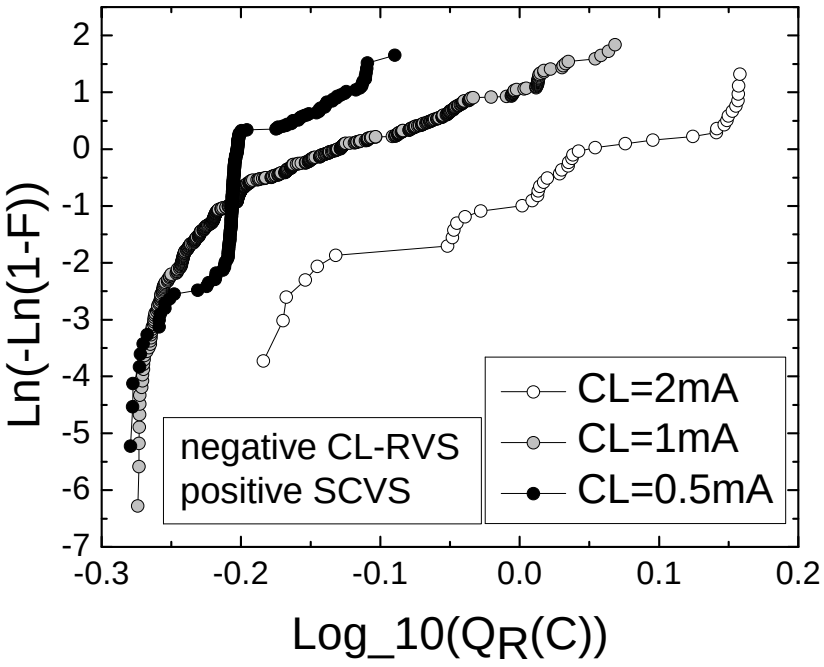
Ln(-Ln(1-F))
Log_10(Q_R(C))
negative CL-RVS
positive SCVS
CL=2mA
CL=1mA
CL=0.5mA

Figure 12

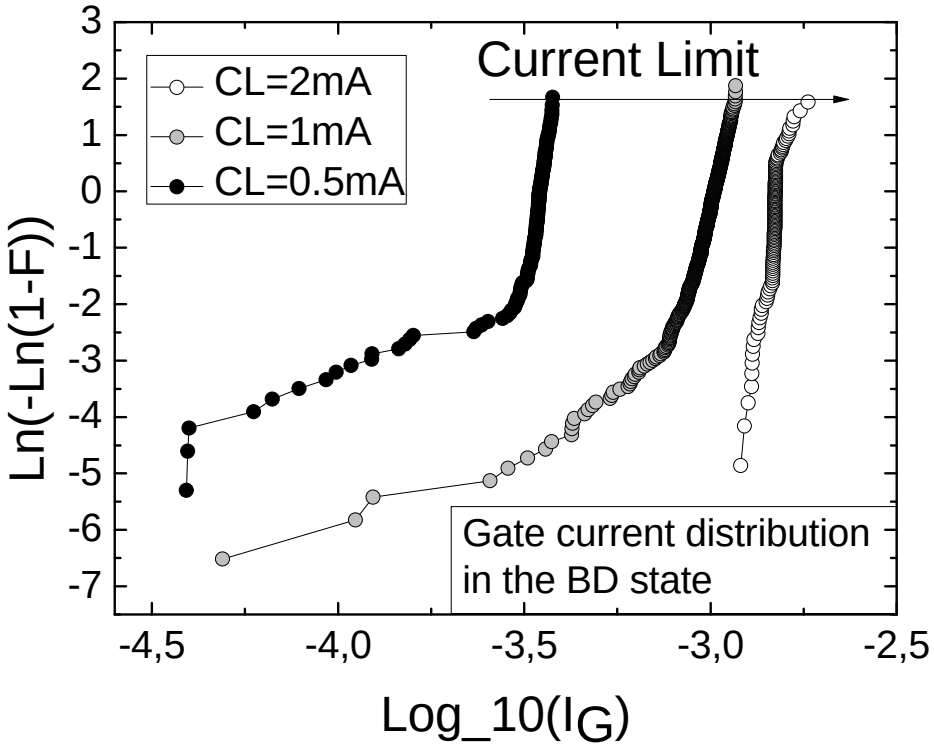
Current Limit
CL=2mA
CL=1mA
CL=0.5mA
Gate current distribution
in the BD state
Ln(-Ln(1-F))
Log_10(I_G)
3
2
1
0
-1
-2
-3
-4
-5
-6
-7
-4,5
-4,0
-3,5
-3,0
-2,5

Figure 13

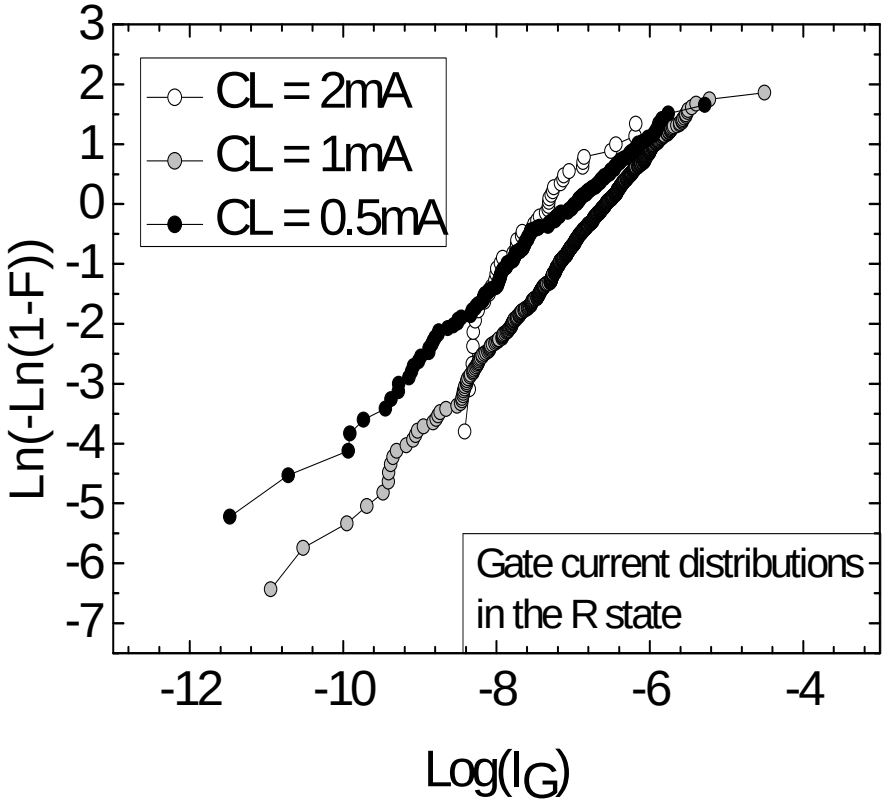
CL = 2mA
CL = 1mA
CL = 0.5mA
Gate current distributions
in the R state
Ln(-Ln(1-F))
Log(I_G)
3
2
1
0
-1
-2
-3
-4
-5
-6
-7
-12
-10
-8
-6
-4

Figure 14

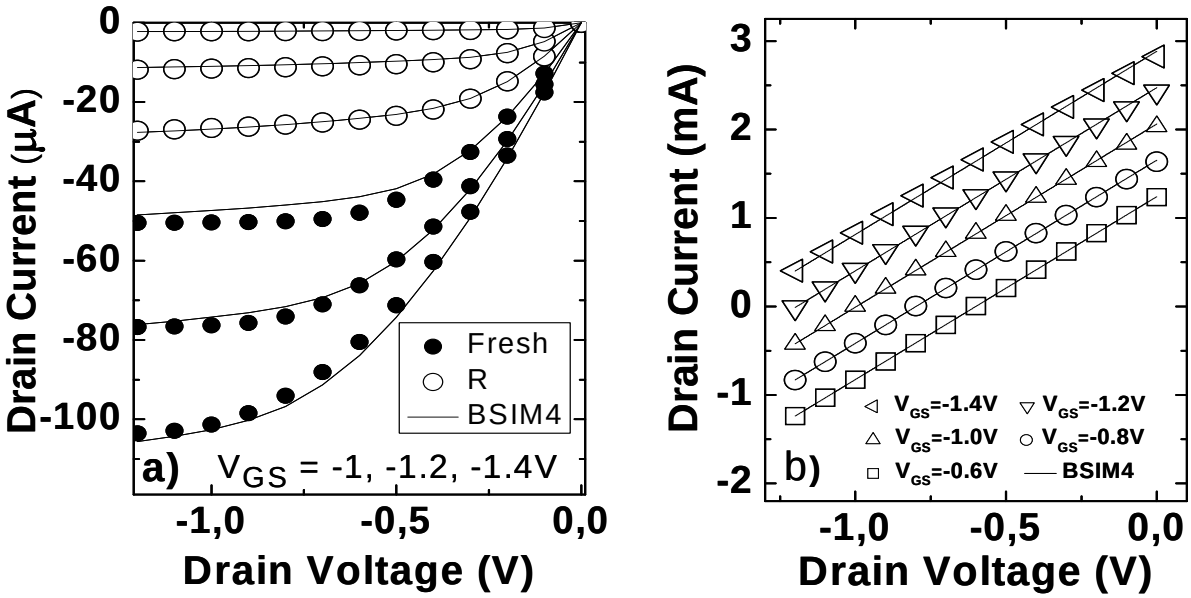
Drain Current (μA)
0
-20
-40
-60
-80
-100
-1,0
-0,5
0,0
Drain Voltage (V)
Fresh
R
BSIM4
a)
V_GS = -1, -1.2, -1.4V
Drain Current (mA)
3
2
1
0
-1
-2
V_GS=-1.4V
V_GS=-1.2V
V_GS=-1.0V
V_GS=-0.8V
V_GS=-0.6V
BSIM4
b)
-1,0
-0,5
0,0
Drain Voltage (V)

Figure 15

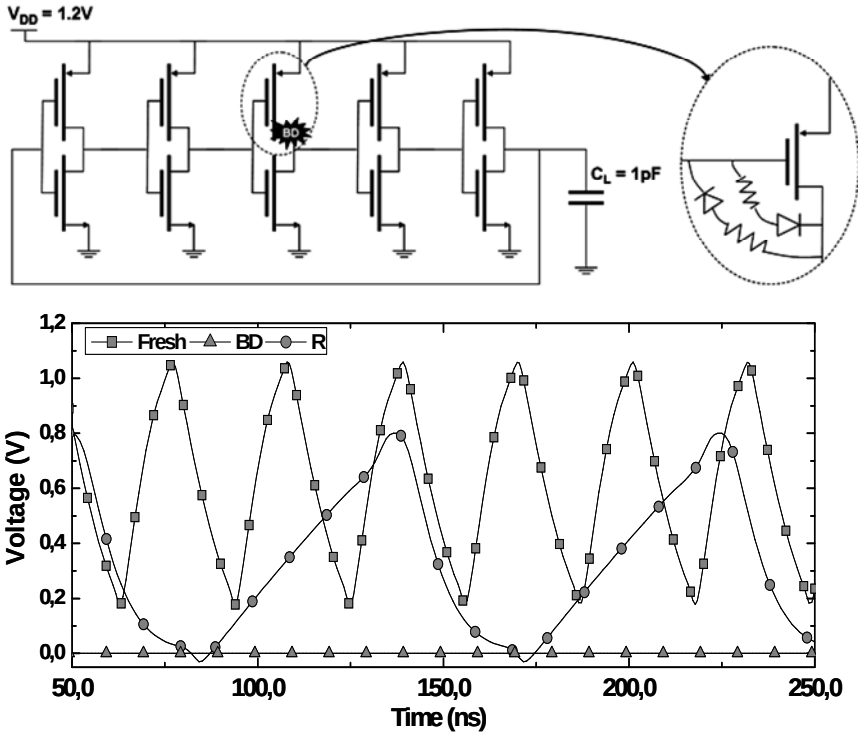
V_{DD} = 1.2V
BD
C_L = 1pF
Fresh
BD
R
Voltage (V)
1,2
1,0
0,8
0,6
0,4
0,2
0,0
50,0
100,0
150,0
200,0
250,0
Time (ns)

Figure 16

Table 1

Input		INV			NAND			NOR		
A	B	F	BD	R	F	BD	R	F	BD	R
0	0	1	0	1	1	0	1	1	0	1
1	0	0	1	0	1	1	1	0	0	0
0	1	-	-	-	1	0	1	0	1	0
1	1	-	-	-	0	0	0	0	0	0