Development of Digital Application Specific Printed Electronics Circuits: From Specification to Final Prototypes

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***Abstract*— This paper presents a global proposal and methodology for developing digital Printed Electronics (PE) prototypes, circuits and Application Specific Printed Electronics Circuits (ASPECs). We start from a circuit specification using standard Hardware Description Languages (HDL) and executing its functional simulation. Then we perform logic synthesis that includes logic gate minimization by applying state-of-the-art algorithms embedded in our proposed Electronic Design Automation (EDA) tools to minimize the number of transistors required to implement the circuit. Later technology mapping is applied, taking into account the available technology, (i.e. PMOS only technologies) and the cell design style (either Standard Cells or Inkjet Gate Array). These layout strategies are equivalent to those available in Application Specific Integrated Circuits (ASICs) flows but adapting them to Printed Electronics, which vary greatly depending on the targeted technology. Then Place & Route tools perform floorplan, placement and wiring of cells, which will be checked by the corresponding Layout Versus Schematic (LVS). Afterwards we execute an electrical simulation including parasitic capacitances and relevant parameters. And finally, we obtain the prototypes which will be characterized and tested. The most important aspect of the proposed methodology is that it is portable to different Printed Electronics processes, so that considerations and variations between different fabrication processes do not affect the validity of our approach. As final results, we present fabricated prototypes that are currently being characterized and tested.**

Keywords*— *Printed Electronics; ASPEC; HDL; EDA; digital circuits; prototypes; logic synthesis; minimization; technology mapping; Standard Cells; Inkjet Gate Array; layout; characterization; ASIC.

I. Introduction

Besides other important factors such as low costs and integration possibilities one of the main characteristics in Printed Electronics at this moment is the wide variety of processes available. Each one of them has its own characteristics, advantages and issues. Still, most of the circuits are being designed at full-custom level, that is to say using layout editors and electrical simulations. Silicon industry demonstrated that ASIC design methodologies using pre-characterized cell libraries allow a high degree of automation, increase design productivity and helps bridging the gap between applications and technology.

Our ASPEC (Application Specific Printed Electronics Circuits) approach is intended to reuse the ASIC models used in industry in terms of designs flows and towards industrial manufacturing foundries. This methodology applied to digital is complementary to the use of existing design methodologies to develop complementary circuitry such as OLEDs, drivers, pressure sensors, analog circuitry, etc.

Anyhow, silicon and printed electronics industries have undeniable differences that need to be taken into account, especially concerning fabrication processes, which affect the whole development strategies and decision making. PE production costs are much lower than for silicon-based clean room facilities. The number and variety of private/public companies/institutions offering their own processes is quite large even that most of those processes are not publically offered. This is one main difference that, in our opinion, limits the widespread of the technology. Differences among processes rely on technological choice, application domain orientation, volume production capabilities, but also in functional devices, performance, variability and yield. There is not yet sufficient standardization to allow an easier classification.

Therefore, we claim that digital design should be abstracted from fabrication processes and this is what is promoted by the ASPEC (and ASIC) design methodology, that is composed by technology-independent steps, specification and logic synthesis; and technology dependent ones, library generation (one per process), technology mapping and placement and routing. All those steps can be automated to obtain prototypes through the methodology that we propose in this paper demonstrated by examples.

II. Complete Flow and Tools

The methodology is composed of a sequence of steps followed by the corresponding optimization loop. All those steps and their related EDA tools are shown in Fig. 1.

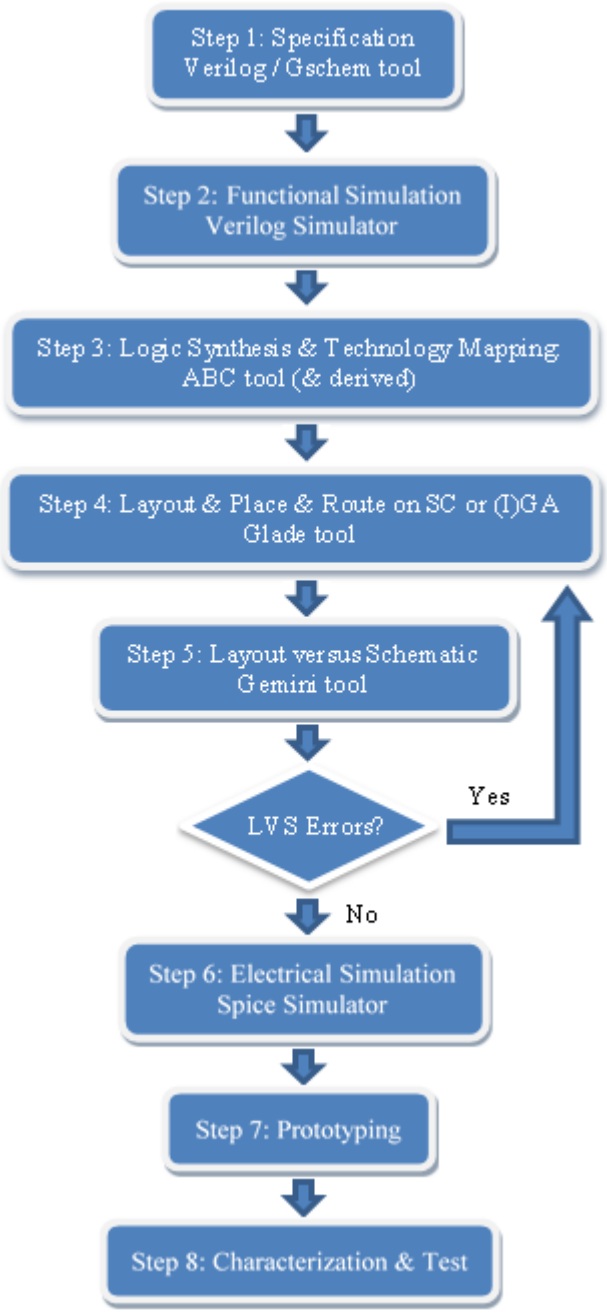

Fig. 1. Complete development flow.

1) *Step 1:*
We begin with the specification of the circuit that we want to implement. This specification will define the functionality of the circuit. We use Verilog [1] as HDL. If the circuit is purely combinational the specification could be merely a Verilog netlist while if it's more complicated it should be a structural or behavioral Verilog description.
Using an HDL for its specification allows tools portability when compared with schematic entry; while schematics representation of the circuit allows a more visual comprehension of each circuit. In the case of schematic entry we use the EDA tool Gschem [2]. Other tools with equivalent functionalities can be used in both cases.

2) *Step 2:*
In this step we implement a tailored test-bench for the circuit that we want to validate using a Verilog simulator such as, for example, Icarus Verilog [3]. We check if the intended functionality was correctly developed. At this stage, performance estimation accuracy will depend on the accuracy of the simulation models.

3) *Step 3:*
Logic Synthesis and Technology Mapping are key points in our methodology. We use the state-of-the-art tool ABC [4] for this step. In ASPEC technologies, due to its low integration density, it is important to minimize the number of gates (and therefore the transistor count) so that circuits can fit into the available substrate space. This depends on the library to which the circuits will be mapped and on the tools.
In our PE case we use a library of pseudo-PMOS logic gates (mainly because conductivity reasons explained in [5]), only using Inverters and NANDs with several inputs. With these gates we can achieve any functionality given by the circuit specification, while reducing library design efforts (primarily on layout) and time-related development costs.
ABC tool applies its technology independent and (after mapping) technology dependent minimization algorithms which are based in And-Inverter-Graphs (AIG [6]) reductions in combination with transformations to other types of representations (such as Binary-Decision-Diagrams BDD and others).

4) *Step 4:*
When we have a minimized circuit already mapped to the proposed library we can start with the layout step. In this case we use the EDA tool Glade [7].
Our strategy allows both Standard Cell and Gate Array approaches. Designs could be targeted, for example, for inkjet PE technologies, like the one that we have in our laboratory.
Designs must be customized to the PE technology addressed. Hence each technology will have its own Standard Cell library and its own Gate Array structure generation, layers and design rules. Details on Standard Cell library designs and PCell library designs can be found in [8].
Place & Route tools implement the floorplan, placement of standard cells or assignment of gates to specific gate array location, and the routing between gates.

5) *Step 5:*
After Place & Route we must check if the final layout netlist obtained by extracting the generated layout (provided by the Glade tool) corresponds to the initial circuit netlist which defines the circuit properly. We use the Gemini [9] tool that will detect the connectivity errors in the layout netlist by comparing them to the initial (or schematic) netlist.
If the tool finds errors it will be necessary to correct them going back to the Place & Route step.

6) *Step 6:*
The final netlist includes parasitic capacitances so that it can be simulated again to obtain performance estimations such as speed and power. The accuracy of the estimation will depend on the accuracy of the simulation models and on the related information on variability. For that we translate descriptions into Spice language. At this point we can simulate using

NGspice [10], AIMSpice [11] or any other Spice [12] simulator that supports the referred model.

7) *Step 7:*
Prototyping will be implemented in one single process for standard cells and in two steps for the gate array, where first the bulk transistors are fabricated and afterwards they are customized by printing the corresponding connectivity layers.

8) *Step 8:*
Once we have fabricated the prototypes we perform the corresponding characterization and test. From the obtained data and curves we identify which of the devices are working properly and which of them should be avoided. Also this will serve to develop / improve the corresponding electrical models that will be used for simulating in forthcoming runs on that particular technology.

III. Examples of the Methodology

In this section we show examples of the methodology explained before, and how this can successfully produce PE prototypes.

We have demonstrated the validity of our methodology with demonstrators of limited complexity. For instance, for a full inkjet process we limited our area to foils of 10x5cm that can hold around approximately 200 transistors (depending on their dimensions). This limits the functionality that we can implement in the substrates. Some of the characteristics and properties of this technology including promising results and findings are detailed in [13].

Moreover variability and yield are also important issues. For instance, this fully inkjet process (developed in the framework of the TDK4PE [14] project), which is using a Drop on Demand (DoD) inkjet printer Dimatix DMP 3000 with commercial materials, has a maximum OTFT yield of around 85%. So the number of good working transistors (what we call KGO – Known Good OTFTs) is far from optimal in some technologies. Other technologies such as the evaporation technologies provided by the Centre for Process Innovation (CPI), reach a more conventional ASIC-like yield of 99%, which gives us more flexibility (in terms of available space) to work on.

Nevertheless next examples show how logic synthesis and technology mapping are key issues in order to fit circuits in the available transistors, regardless of the fabrication process selected. We can evaluate the ABC tool for the minimization of the number of gates required to implement a function (and consequently OTFT count) by using very small well-known benchmark circuits such as the ones in ISCAS-89 and ICT-99 [15]. Verilog specification can be used as input netlist for ABC. The following tables I and II show the optimization results on those circuits when mapping to a pseudo PMOS library which only may contain Inverters / NAND2 / NAND3).

TABLE I. Benchmark gates and OTFT count before logic synthesis.

Cell-library Gates & Costs	ISCAS-89		ICT-99		
	s27	s208.1	b01	b02	b06
# INV1	9	32	11	5	11
# NAND2	6	34	21	13	21
# NAND3	1	23	11	4	13
TOTAL # Gates	16	89	43	22	45
Cost (#OTFT)	40	258	129	65	137

TABLE II. Benchmark gates and OTFT count after ABC optimization.

Cell-library Gates & Costs	ISCAS-89		ICT-99		
	s27	s208.1	b01	b02	b06
# INV1	8	28	11	6	7
# NAND2	6	38	16	10	23
# NAND3	1	6	11	5	9
TOTAL # Gates	15	72	38	21	39
Cost (#OTFT)	38	194	114	62	119
Cost reduction %	5%	24,8%	11,6%	4,6%	13,1%

The analysis of this table shows that ABC optimizations are usually more notable on large circuits than for small ones. A maximum of ~25% is reached what means a reduction of 64 out of 258 transistors.

Since the yield obtained is reduced and we have size limitations, some of these circuits might not fit in the substrates or they could be risky to implement. In our case, if we considered, as mentioned earlier, a substrate foil with around 200 OTFTs capacity and a yield reaching only 85% (so in best scenarios for that particular technology we can have 170 transistors working), then only s208.1 could not fulfil this space requirement.

The Place and Route step will provide the functionality to the PE prototype or circuit. The target technology will determine the specific design rules of the different layers representing the materials used in each fabrication process. In our case so far we have addressed two PE technologies with very different characteristics: the ones provided by CPI and TUC. CPI is based on glass or plastic substrates with high yield which can later be customized via inkjet, aerosol or Super-fine Inkjet (SIJ); while TUC is based on plastic foils and all-inkjet printing which can also be customized after fabrication. In Fig. 2, we show a complete floorplanned wafer fabricated by CPI. Details about CPI process can be found in [16, 17].

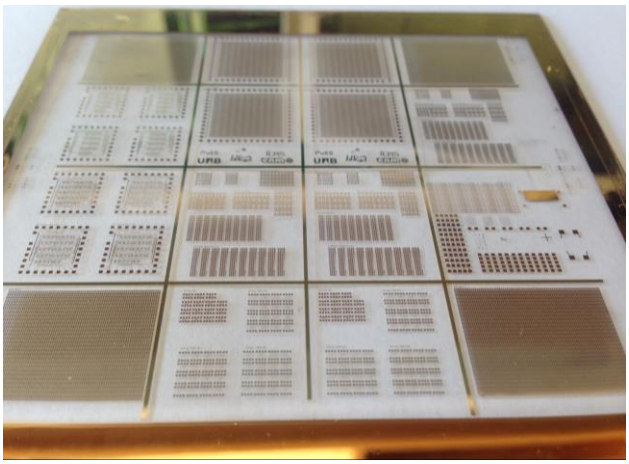

Fig. 2. PE complete wafer fabricated by CPI.

In the different regions of the floorplan we have included DRC structures, Ring Oscillators showed in Fig. 3, Inkjet Gate Array structures (Fig. 4) but without any circuit mapped onto them (which can be done in a later customization process), and our own combinational ASPEC demonstrator (Fig. 5).

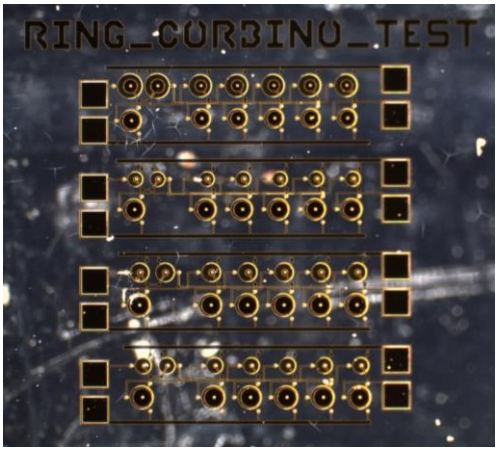

Fig. 3. Ring Oscillators within CPI wafer.

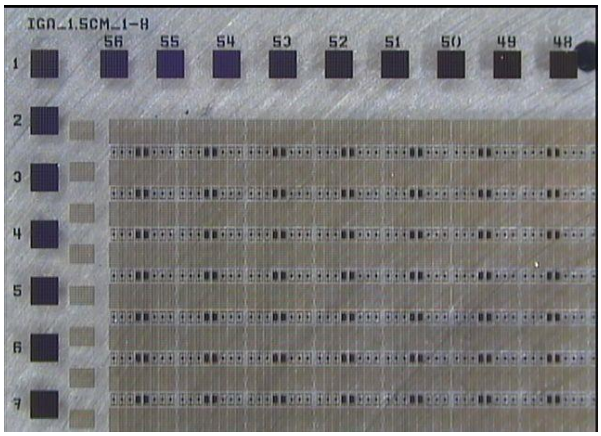

Fig. 4. IGA structure within CPI wafer.

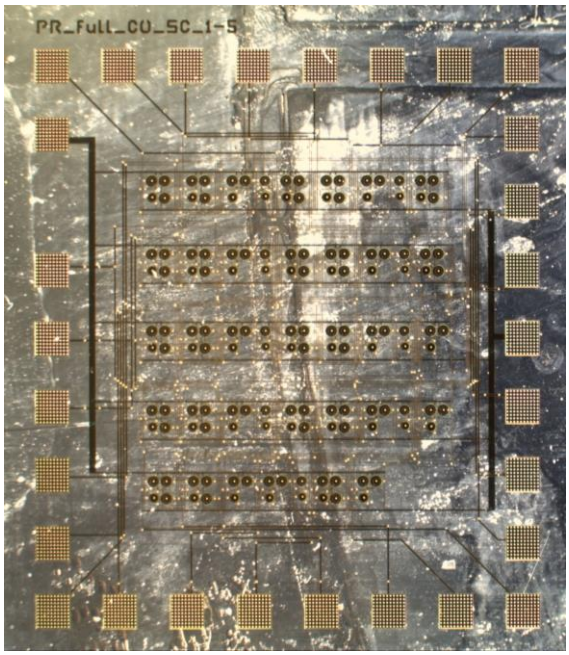

Fig. 5. ASPEC example within CPI wafer.

As mentioned before some of the proposed structures are meant to be post-processed in order to provide them with their own connectivity. In Fig. 6, we show an inverter chain example. First the characterization of each inverter was done in order to determine which ones were good enough to be part of the chain, and afterwards they were connected accordingly in this post-process customized wire printing.

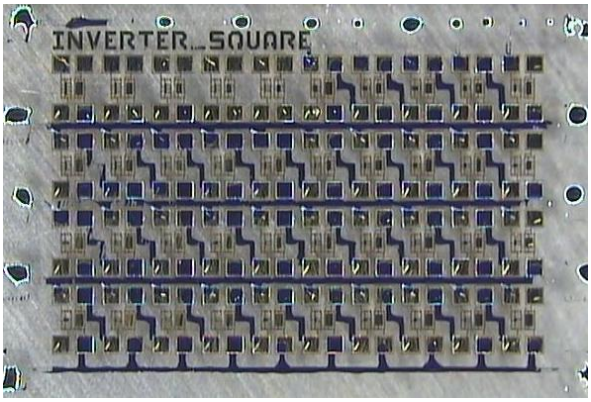

Fig. 6. Inverter chains customized connectivity within CPI wafer.

Fig. 7 and Fig. 8 show the results from the DC characterization. The approach followed to connect the inverters to build the chain allows analyzing the output of each stage, while exciting the input of the chain. The test has shown that the output gain tends to increase after each stage.

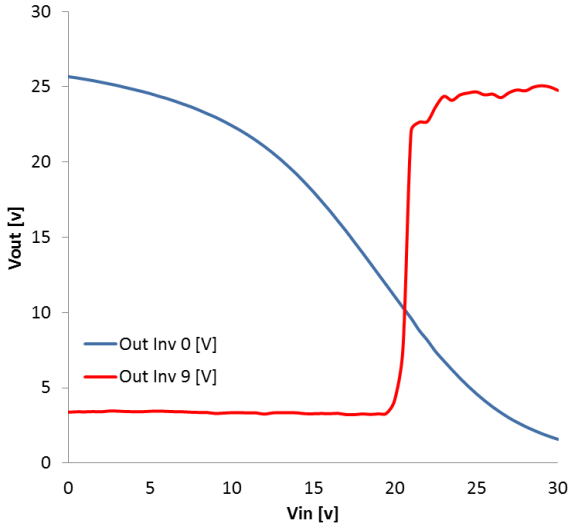

Fig. 7. DC analysis of the inverters chain showing the output of the first inverter stage (Out Inv 0) and the output of the last one (Out Inv 9).

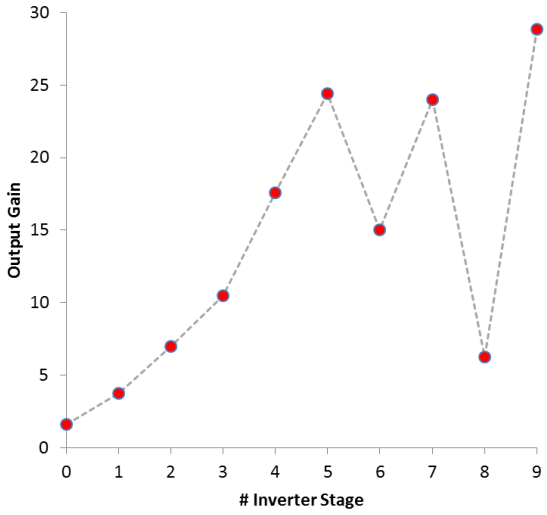

Fig. 8. Inverter output gain after each stage of the inverter chain.

Another interesting point is that even the fact of having some poor stages (6 and 8 in Fig. 8), if the last inverter of the chain is good enough, the output signal is rebuilt.

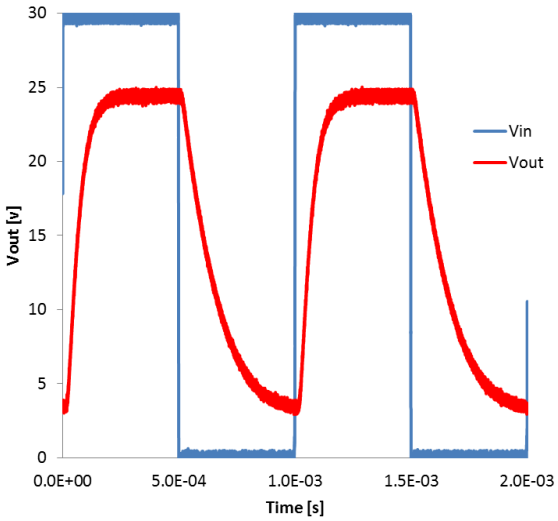

Fig. 9. Transient analysis of the inverter chain.

Fig. 9 shows the transient characterization, where it can be seen that the inverter chain is able to work perfectly at a frequency of 1kHz.

The input voltage range is from 0 to 30 V and the output varies depending on the characteristics of each inverter in the chain, but usually it can be expected around 26 to 3 V. Considering that all the inverters in the chain have an aspect ratio of 1/3, but with different dimensions, it's a good indicator of the scalability of their performance (given their variability).

Also a set of IGAs have been fabricated on plastic foils using all-inkjet deposition processes with different horizontal and vertical dimensions by our technological partner TUC. An example can be observed in Fig. 10.

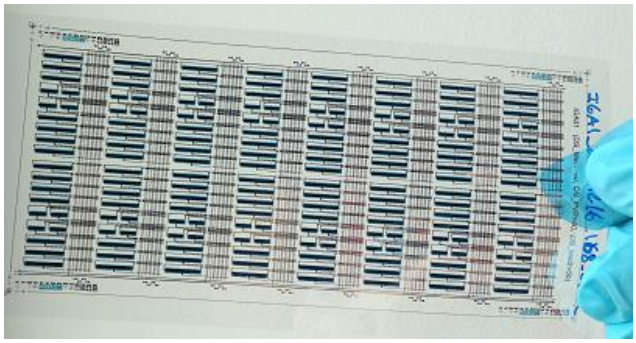

Fig. 10. IGA foil fabricated by TUC.

As mentioned earlier circuits can be mapped onto these IGAs but taking into account which are the OTFTs that are working properly and which of them have to be avoided / discarded. This is done by characterizing all of them and deciding which of them can be considered as KGOs according to the yield dependency.

IV. Conclusions

We have presented in this paper a methodology for obtaining Printed Electronics prototypes / circuits / ASPECs. We have followed similar procedures to the ASIC industry and foundry models, but adapting them to the PE specific technological processes we have worked on, with their own characteristics, advantages (primarily the lower costs) and issues (mainly related to materials, variability and yield).

We propose a flow that goes from specification of the circuit itself in HDL; through simulation using tailored testbenches and the proper model provided by the technological foundry; logic synthesis minimization and technology mapping to our proposed pseudo PMOS library, although it could be other libraries depending on the PE targeted processes; Layout & Place & Route following either a Standard Cell or Inkjet Gate Array strategy; and a final LVS check to compare netlists so that they satisfy the functionality requirements.

To demonstrate the validity of our approach we have presented as examples the different prototypes that we have built addressing the technologies of some of our partners; in this particular case CPI and TUC. This way it's clarified that the methodology can be used targeting other PE technologies in a flexible manner.

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Lluís Terés was born in Soriana-Estolanyà, Aragón, Spain, he got the Engineering (1981) and PhD (1986) degrees in Computer Sciences from the Autonoma University of Barcelona (UAB). He is with the National Centre for Microelectronics (CSIC), Barcelona Institute, since its creation in 1985. He is head of Integrated Circuits & Systems (ICAS) group, with research activities ranging from hardware description languages, flexible platform based design, up-to low power analogue-digital-mixed CMOS circuits design, N/MEMS sensors interface and organic/printed/flexible electronics. He has been participated and managed a large number of industrial and research projects resulting on a number of papers, patents and spin-offs. He is also part time Assistant Prof. at the UAB.