

Monitoring defects in III-V materials: A nanoscale CAFM study

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Abstract

The implementation of high mobility devices requires growing III-V materials on silicon substrates. However, due to the lattice mismatch between these materials, III-V semiconductors tend to develop structural defects affecting device electrical characteristics. In this study, the CAFM technique is employed for identification and analysis of nanoscale defects, in particular, Threading Dislocations (TD), Stacking faults (SF) and Anti-phase Boundaries (APB), in III-V materials grown over silicon wafers.

Keywords: *High mobility substrates; III-V semiconductors; Threading dislocations; CAFM.*

1. Introduction

The introduction of III-V materials for the fabrication of devices having high mobility substrates is one of the most promising developments in the electronic technology. However, due to mismatch between the III-V materials and silicon lattices, the grown III-V films tend to have significantly high density of structural defects [1], which affects the device electrical characteristics. Therefore, monitoring and identification of these defects is critically important for the successful device fabrication. Traditionally, the electrical properties of III-V substrates have been studied by measuring I-V characteristics in fully processed devices, such as MOS capacitors, MOSFETs and Schottky diodes (device level analysis) [1-3]. However, the device level tests measure the overall current through the entire device area and, therefore, these data are not specific to the substrate structure. Some of these defects may be of less than few nanometers cross-section. Therefore, their analysis require using the tools with nanoscale resolutions for both structural and electrical characteristics. Conductive Atomic Force Microscope (CAFM), and KPFM (Kelvin Probe Force Microscope) meet these requirements for measuring defects conductivity and contact potential. In particular, CAFM has been widely used for the nanoscale electrical characterization of the defects in gate dielectrics either grown [4, 5] or generated under the applied electrical stress or irradiation [6-11]. Threading Dislocations (TDs) in III-V semiconductors have also been investigated at the nanoscale [12–16]. Structurally defective sites (detected as pits in the topography maps) were reported to exhibit lower turn-on voltages and higher leakage currents measured under the forward and reverse biases [12-16]. Forward currents through TDs, for instance, were attributed either to

Poole-Frenkel (PF) conduction mechanism [14, 16] or to a lowering of the barrier height of the Schottky contact between the tip and the sample [15]. However, most of these studies have been exclusively focused on the analysis of TDs. This study demonstrates the capability of the CAFM technique [2] to identify and analyze, at the nanoscale, a wide range of defects in the III-V substrates, in particular, Threading Dislocations (TD), Stacking faults (SF) and Anti-phase Boundaries (APB), by correlating topographical and current maps measured on varieties of areas, as well as I-V dependencies collected on the targeted defect sites.

2. Experimental

Samples consisting of III-V materials stacks grown over a silicon substrate under different conditions have been studied. The morphology and electrical characteristics of these samples have been analyzed by measuring topography and current maps with the CAFM tip contacting the III-V surface on randomly selected locations. The I-V curves on targeted surface sites were also collected by applying a ramped voltage test. In this work, CAFM measurements were performed in ambient conditions and ambient light. Silicon tips coated either with doped diamond (to make tips conductive) or with a metallic alloy were used.

3. Results and Discussion

3.1. Detection and identification of defects.

The goal of this section is to evaluate the capability of the CAFM tool to detect and identify variety of defects in III-V materials. For this purpose, samples with different characteristics have been analyzed employing the CAFM technique.

First, two samples with the Te:InGaAs 30nm/InGaAs 120 nm/InP 600nm/GaAs 500nm/Si stack grown under different buffer conditions (sample A and B) have been compared. Sample A has additional graded buffers between the InGaAs active layer and InP layer, which likely help to reduce the defect density. Fig. 1 shows, as an example, the cross section (a) and planar (b) TEM images of the sample B (the one with a higher density of defects). Fig. 1a shows the presence of TDs in the InGaAs layer. Some of these defects can propagate starting from the substrate interface and continuing through the entire III-V material thickness up to the surface, where they are detected as pits. Therefore, the observed pits can be related to deep defect regions. In Fig. 1b, other types of defects can be observed. Stacking Faults (gray

squares) are sometimes bounded by dark lines (dislocations). Surface defects (yellow arrows), possibly pits, are also present in the image. Some of them (red arrows), but not all, are associated with the intersection of two Stacking Faults.

The topography and electrical properties of samples A and B were also studied with CAFM. Fig. 2 shows topographical (a) and current, measured at 2V (injection from the tip), (b) maps of the sample A. Note that a pit (circle in Fig. 2a) is also seen in the topographical map. This pit, with a depth and diameter of approx. 1.5nm and 30nm, respectively, could be attributed to a TD. The TD exhibits higher conductivity as can be seen in the current map in Fig. 2b. Other conductive sites (circles) were not registered as pits in the topography image. These sites could be related either to the pits, which were not detected by the CAFM, or to TDs, which didn't reach the surface, as demonstrated by the TEM images.

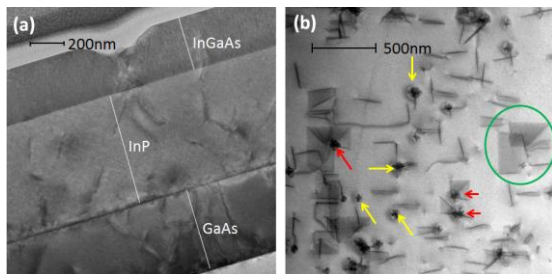


Fig. 1. Cross section (a) and top view (b) TEM image of a Te:InGaAs 30nm/InGaAs 120 nm/InP 600nm/ GaAs 500nm/Si stack.

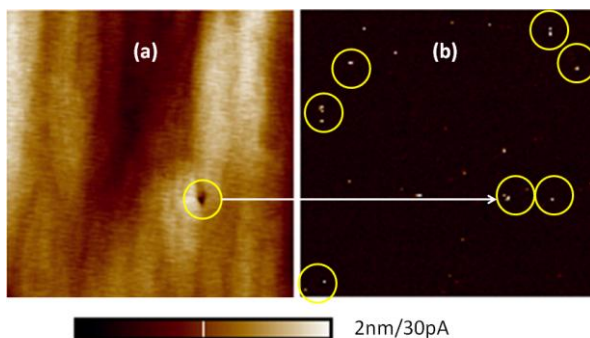


Fig. 2. (a) Topographical and (b) current images measured on sample A. The pit (yellow circle in (a)) depth and diameter are 1.5nm and 30nm, respectively. Image area: $2 \times 2 \mu\text{m}^2$, voltage (in (b)): 2V.

CAFM not only allows correlating topographic and conductivity data (possibly related to TDs), but also analyzing and comparing the properties of defect sites in different samples. As an example, Fig. 3 shows topographical (a) and current, measured at 1V, (b) images in sample B. Note that the structural pits observed in the topographical map are similar to those shown in Fig. 2a but they have larger depth and diameter (approx. 90nm and 200nm, respectively). The density of pits (which can be also attributed to TDs) in the sample B is higher than

that in the sample A, and these pits exhibit larger leakage currents. Thus, these data show that CAFM is capable to differentiate the impact of different technological processes on structural and conductive properties of the fabricated material. Besides TDs, other topographical features (as those shown in Fig. 4a), which correlate to leakage currents (Fig. 4b), have been detected. Since the morphology of such sites is different from those of TDs, they may be related to other kind of defects, for instance, Stacking Faults, which are also present in these samples, as shown in Fig. 1b. SF were also identified with CAFM in other materials [17].

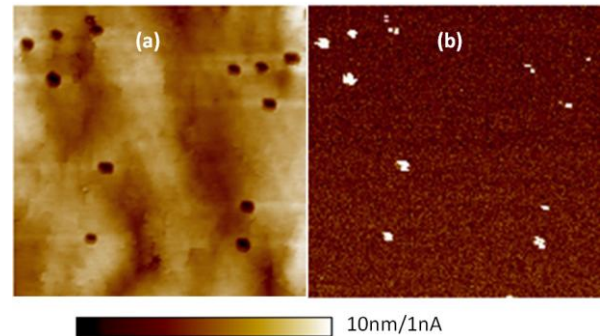


Fig. 3. Topographical (a) and current (b) images obtained on sample B. Area: $10 \times 10 \mu\text{m}^2$, voltage (in (b)): 1V. The pit depth and diameter are $\sim 90\text{nm}$ and $\sim 200\text{nm}$, respectively.

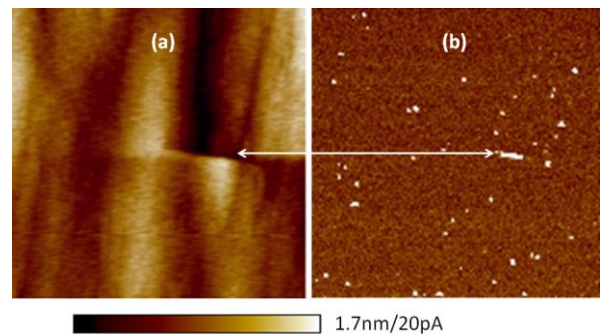


Fig. 4. Topographical (a) and current (b) maps measured in sample A. Conduction through a topographical feature presumably related to a Stacking Fault (connected by an arrow) differs from that of the pits observed in Figs. 2, 3. Image area: $2 \times 2 \mu\text{m}^2$.

Samples with other kinds of defects were also studied. As an example, Fig. 5a shows a TEM image measured in the InAlAs 300nm/InP 800nm/GaAs 300nm/Si sample containing anti-phase boundaries (APB) and TDs. A CAFM study of the same sample shows that the topographical map (Fig. 5b) contains a pattern of traces, which are very similar to those shown in Fig. 5a. Therefore, the topographical pattern can be related to the APB features. Certain pits measured in both, Fig. 5a and 5b, are also associated with TDs (circles in (a) and (b)). Note that in this case, the current images (Fig. 5c) measured inside the green square in Fig. 5b indicate that the APB features are less conductive than the features in the surrounding areas.

Finally, a preliminary analysis of a patterned sample fabricated using Aspect Ratio Trapping (ART) approach [18, 19] was performed. In this fabrication method, threading dislocations are confined within high aspect ratio sub-micron trenches that prevents TDs from reaching the surface of III-V materials. Fig. 6 shows cross-section (a) and top-view (b) SEM images of a sample with 65 nm wide InP/SiO₂ trenches. CAFM topographical and current maps are shown in (c) and (d), respectively. Note that current was observed to flow preferentially through InP regions, and these regions exhibit inhomogeneous conductivity.

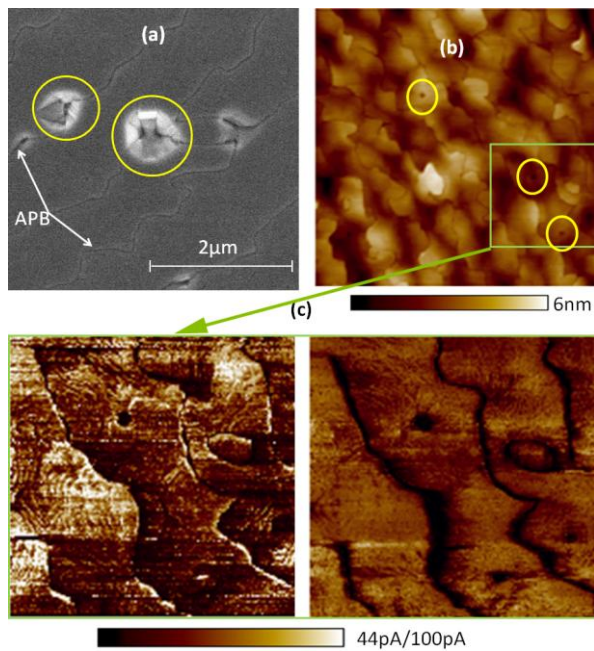


Fig. 5. (a) TEM, (b) topographical and (c) current images measured on a stack with APBs and TDs. Images size is, respectively, (a) 5x5, (b) 7x7 and (c) 3x3 μm².

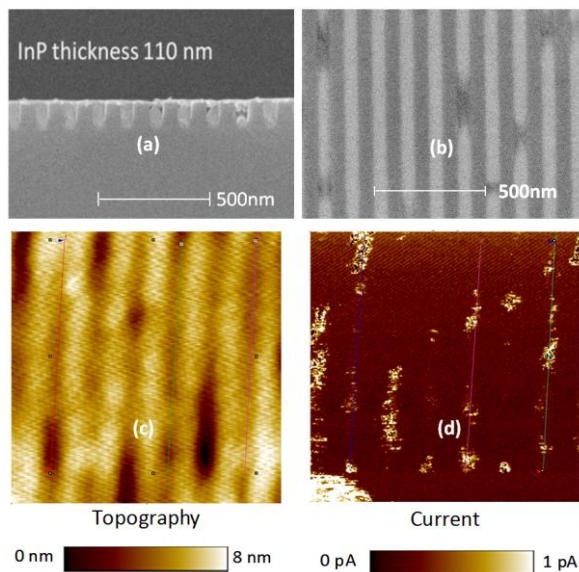


Fig. 6. SEM (a and b) and CAFM (topography, c, and current, d) images obtained on a patterned sample with 65 nm wide InP / 65 nm wide SiO₂ trenches. AFM image size: 0.5x0.5 μm².

In conclusion, the data presented in this section demonstrate that the CAFM technique is capable to identify, distinguish and characterize different kinds of III-V defects in blanket or patterned structures and to evaluate the impact of fabrication processes on the samples properties.

3.2. Electrical conduction analysis of TDs in III-V materials.

The TDs detected in samples A and B have been further analyzed by combining current maps and I-V data. Fig. 7 shows a sequence of 3 current maps with increased scanned areas collected (at V= 1V) on the same region in a sample A. A statistical analysis of the leaky sites shows that their conductivity tends to decrease with each subsequent measurement indicating that the conduction decreases with longer stress times. Some studies have reported that this phenomenon could be attributed to the growth of a thin insulating layer [20]. However, in our case, since the current maps were taken at small voltages, these morphological changes apparently didn't occur. In certain cases, transient currents through the TDs sites were observed even at very low voltages. A topographical image is shown in Fig. 8a, and a sequence of three current maps measured at 0V is presented in Fig. 8(b-d). Data in (b) and (c) were collected consecutively while scans at different voltages were applied between the measurements presented in (c) and (d). Note that a current through the pits decreases slightly in the (b)-(c) measurement sequence and, much stronger in the (c)-(d) sequence. These data reflect on the transient characteristics of the current, which could be related to the presence of trapped charges in the TD regions. These charges can be progressively discharged [12] through the contacting CAFM tip. This discharge can proceed faster when a bias is applied to the tip, as the (c)-(d) measurement sequence shows.

I-V curves were also measured to analyze the conduction through III-V materials. Fig. 9 shows two examples of the forward (negative V) and reverse (positive V) I-V curves measured in (squares) and out-of (triangles) TD sites (sample A). Note that the current is larger in the forward bias case suggesting that the tip-sample contact is of a Schottky type (although current under the reverse bias partially hides the rectifying features). Under the forward bias, the conduction in and out-of the TD is similar (although slightly larger in the TD). However, under the reverse bias, the electrical conduction in the in-TDs case (squares) is higher than that in the out-of TDs (triangles), demonstrating again the leakage characteristics of these defective sites. Since the current under the reverse bias is smaller (although not negligible) than under the forward bias, the conduction differences between the in- and out-of TDs cases

are more pronounced. In [21] it is demonstrated that the excess of current measured at TDs is compatible with Poole-Frenkel emission.

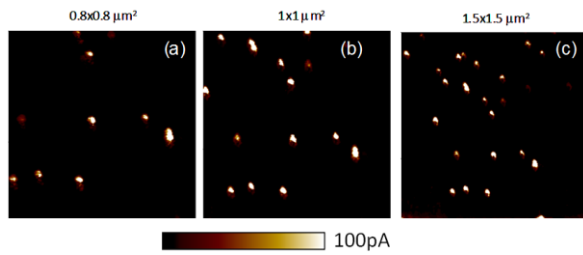


Fig. 7. Series of current maps obtained at 1V on the same region of sample A, but increasing the scanned area.

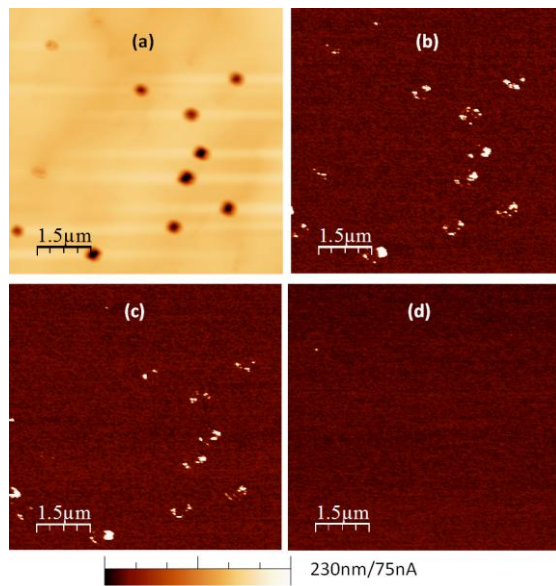


Fig. 8. (a) Topographical and (b-d) sequence of current maps measured on the same area of sample A at $V=0V$. Image area: $5 \times 5 \mu\text{m}^2$.

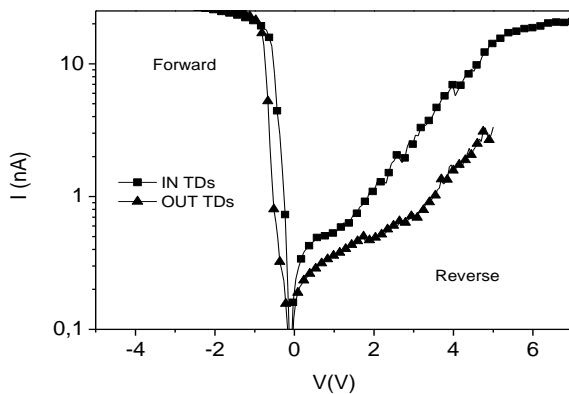


Fig. 9. I-V curves measured in- (squares) and out-of (triangles) TDs in sample A, under forward (negative V) and reverse (positive V) biases.

4. Conclusions

The presented results show that the CAFM can help to identify various types of structural defects in III-V materials, as well as measure their conductive characteristics and analyzing their evolution under electrical stress on both blanket and patterned III-V

structures. In particular, in the observed Schottky type AFM tip-sample contact, a larger current under the reverse bias (especially in the TDs) tends to hide the contact rectifying feature.

Acknowledgements

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