Resistive Switching like-behaviour in MOSFETs with ultra-thin HfSiON dielectric gate stack: pMOS and nMOS comparison and reliability implications

A. Crespo-Yepes *, J. Martín-Martínez, R. Rodríguez, M. Nafría, X. Aymerich.

Department of Electronic Engineering, Universitat Autònoma de Barcelona (UAB), 08193 Bellaterra, Barcelona (Spain)

Abstract

In this work, the Resistive Switching (RS) phenomenon is studied in n and pMOSFETs with ultrathin Hf based high-k dielectric. Two different conductive levels, a high (HRS) and a low (LRS) resistance states can be distinguished in the dielectric. The influence of the voltage polarities applied to reach the HRS and the LRS on the RS phenomenology is analysed. The drain current - drain voltage and drain current – gate voltage transistor characteristic during the HRS has been also analysed in those cases where the RS has been observed. The results can be useful to understand the effect of the RS on the MOSFETs performance from a reliability point of view.

1. Introduction

The gate dielectric breakdown (BD) is one of the most important failure mechanisms studied in reliability issues, characterized by the loss of the insulating properties of the gate dielectric stack, which changes the oxide conductivity from a low to a high conductivity state [1] that could have a very detrimental effect on the device performance [2]. This mechanism is associated to a conductive path formed through the oxide stack and was traditionally considered an irreversible phenomenon [3]. However, several years ago it was shown that in SiO_2 stacks, sometimes, the high conduction after BD could be a reversible phenomenon [4]. Recently, It has been observed that in high-k Hf based gate stacks the dielectric BD is a reversible phenomenon with a strong post-BD conductivity reduction, being possible to change between a low to a high conductivity state several times [5,6] when appropriate voltages are applied. BD reversibility has strong similarities with the Resistive Switching phenomenon (RS) used in MIM/MIS (Metal-Insulator-Metal/Metal-Insulator-Semiconductor) structures for memory applications, that is also characterized by two interchangeable conductivity states, a high one (Low Resistive State, LRS) and a low one (High Resistive State, HRS) [7,8]. Moreover, when BD reversibility is observed, not only the insulator properties are recovered but also the transistor performance is partially recovered [5,6], that could have a strong impact on the reliability of these devices [9,10]. In that sense, this work is focused on the study of BD Reversibility in p and nMOSFETs from a Resistive Switching point of view. The influence of the voltage polarity to reach the HRS and LRS on the RS phenomenology has been evaluated.

*Corresponding author: albert.crespo@uab.cat
Tel: +34 (93) 581 3521; Fax: +34 (93) 581 2600

Implications in the transistor functionality, particularly, the effect of the HRS on the drain current has been also analyzed.

2. Samples and experimental setup

The samples were pMOSFETs and nMOSFETs with NiSi gate electrode and high-k dielectric stack formed by a 2.9nm HfSiON film on top of a 1.2nm SiO_2 interfacial layer (1.9nm of EOT). Different channel length (from 0.15µm to 1µm) and width (from 0.15µm to 1µm) were chosen to study the RS in devices with different geometric dimensions.

The samples were subjected to the measurement scheme shown in figure 1: a Current Limited-Ramped Voltage Stress (CL-RVS) was applied to the gate terminal with the rest of terminals grounded to provoke the BD (Set process) under current limited conditions, and a Ramped Voltage Stress (RVS) without current limit to induce the BD Reversibility (Reset process).

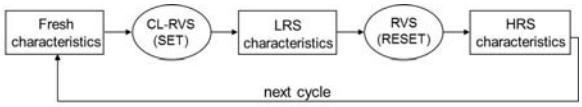

Fig. 1: Stress-measurement sequence designed to analyse the RS. The compliance of the measurement equipment was used to limit the current (1mA in this work) during the current limited stress (CL-RVS).

Different polarities for both CL-RVS and RVS were applied. The transistor characteristics of the fresh sample and after each stress were registered to evaluate the oxide damage and the device performance.

3. Resistive switching phenomenology

Figure 2-CaseA shows the typical gate current evolution measured during the observation of the RS phenomenon. During the first CL-RVS (thick line) a low gate current is registered that corresponds to the fresh device (I_F). When gate voltage reaches the Set voltage (V_{SET}) a sudden increase of the current through the oxide is registered at the gate terminal indicating that BD has been reached and the conductive filament (CF) that controls the current through the gate has been created [3,5]. When the following RVS (circles) is applied a high current is measured (I_{LRS}) that is several orders of magnitude higher than the fresh device, indicating that the oxide is in a high conductivity state (LRS). If the voltage applied to the gate terminal still increases, at some Reset voltage (V_{RESET}) the current droops several orders of magnitude reaching a lower conductive state (HRS state). During the next CL-RVS (thin black line) the current registered at the gate terminal (I_{HRS}) is several orders of magnitude lower than I_{LRS}, but larger than fresh case.

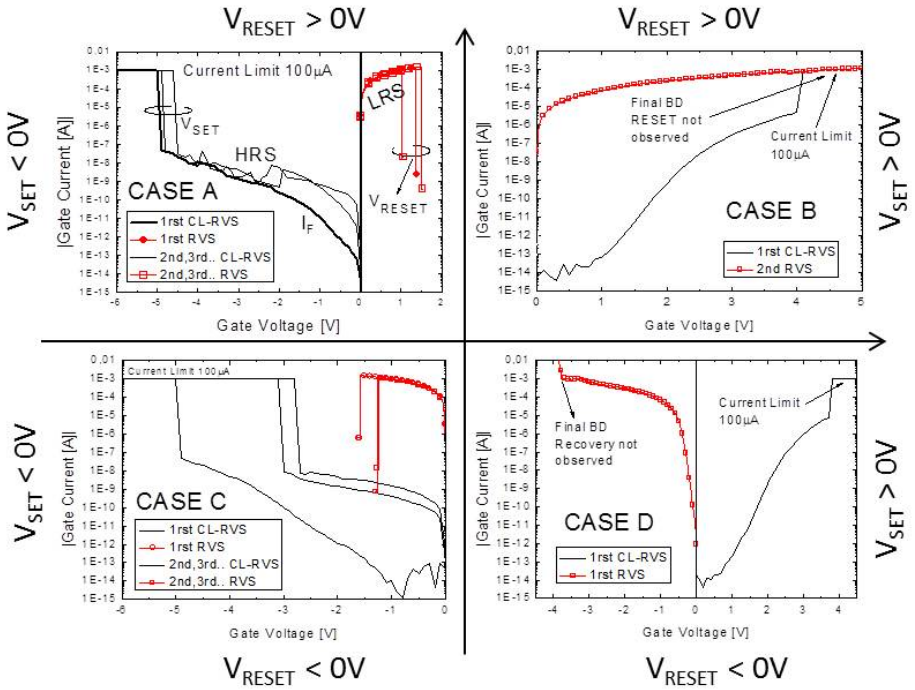

Fig. 2: RS in pMOSFETs for both polarities of stress to produce Set and Reset processes. When the Set is provoked with a negative bias, Reset is observed for both RVS polarity. But when Set is provoked with a positive bias, Reset is not observed, neither for positive or negative RVS bias.

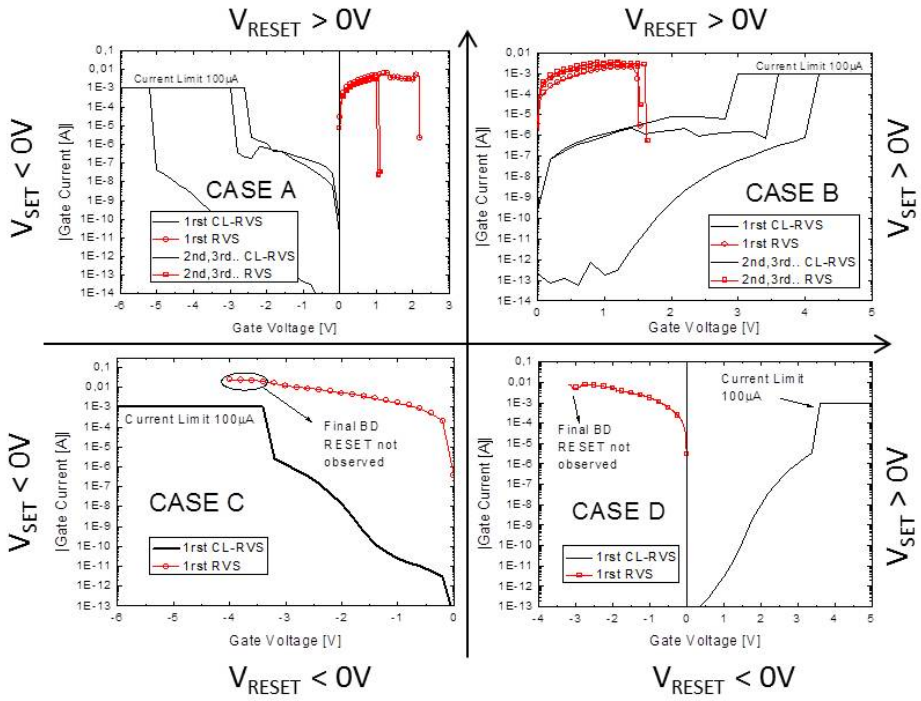

Fig. 3: RS in nMOSFETs for both polarities of stress to produce Set and Reset processes. Reset is only observed when a positive bias is applied to recover the sample, independently of Set polarity.

The conductivity change observed between the HRS and LRS can be observed for many iterations of the stress sequence of figure 1. In addition, the phenomenon is qualitatively repetitive from sample to sample, and can be observed either in p or n type MOSFETs. Note that the current is limited (at 1mA) to limit the degradation of the oxide created during the Set process. If no current limit is applied during Set, the Reset process is not possible any more [10]. Moreover, the phenomenology can be observed for different bias polarity stress, either to provoke the HRS either to induce the LRS.

4. Polarity dependence of the RS phenomenon

The samples were subjected to the stress sequence of figure 1 with different combinations of the bias polarity during the stresses (CL-RVS and RVS) to evaluate the influence of the stress polarity on the RS phenomenology. Figure 2 shows the I_G-V_G curves of the RS observed in pMOSFETs subjected to different combinations of stress polarity during Set and Reset processes. As can be observed, bipolar (case A) and unipolar (case C) is observed, but only when the Set process is performed at negative bias.

The I_G-V_G curves obtained in nMOSFETs (Figure 3) shows that RS is only observed when the Reset is produced at positive bias, being possible again to obtain bipolar (case A) and unipolar (case B) RS. The cases in which the RS phenomenon was successfully achieved are repetitive for at least 10 cycles. Some studies have reported that while the unipolar switching is related to the Ni diffusion from the gate electrode, the bipolar switching is mainly dominated by diffusion of oxygen vacancies in the conductive filament [11, 12]. However, recent works have shown that when RS is studied in transistors, the diffusion of Ni atoms into the dielectric can occur from the gate electrode or from the NiSi electrodes of drain and source (Figure 4) leading to the observation of unipolar and bipolar switching [13]. Nevertheless, the nature and the quality of the interface in MIS structures play a key role in the switching process [14]. Then, the interface properties could affect to those cases in which the RS is not observed, such as cases B and D of figure 2 and cases C and D of figure 3.

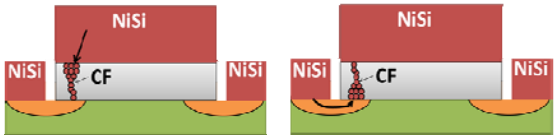

Fig. 4: In transistors, the conductive filament through the oxide can be formed by Ni atoms that diffuse into the dielectric from the gate electrode (a) or from the drain/source electrodes (b). Then, unipolar and bipolar switching due to the same mechanism can be observed [13].

5. Impact on the transistor characteristics

Previous works have shown that during the LRS the transistor characteristics are completely distorted [9]. However, the device functionality is restored when the HRS is reached. In this work, the performance of the p and nMOSFETs during the HRS has been analyzed in detail for the cases where the RS is observed.

5.1. I_D-V_G characteristics

Figure 5 shows the I_D-V_G characteristics registered for fresh devices (squares) and at HRS during bipolar RS measurements (circles).The left hand side of figure 5 corresponds to the case A of figure 2 (pMOSFET). At the HRS, larger threshold voltage than in the fresh device is observed. The right hand side of figure 5 corresponds to case A of figure 3 (nMOSFET). At the HRS, the threshold voltage is lower than for the fresh case. Then, for bipolar RS a negative threshold voltage shift is observed which suggests a positive charge trapping in the dielectric bulk at the HRS in both cases [15].

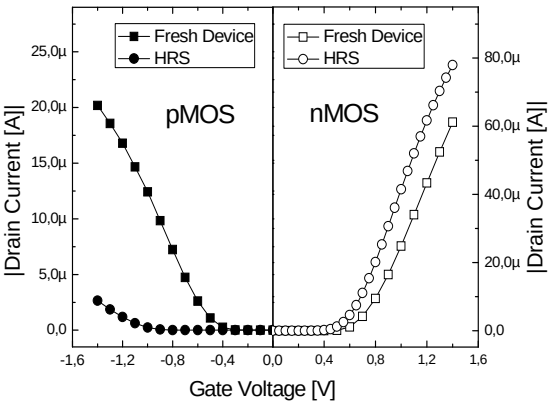

Fig. 5: pMOSFET (closed symbols) and nMOSFET (open symbols) I_D-V_G characteristics of a fresh device (squares) and at HRS (circles). Stress polarity corresponds to the bipolar RS (case A in figures 2 and 3).

5.2. I_D-V_D characteristics

Figure 6 shows the fresh (open symbols) and HRS (closed symbols) I_D-V_D characteristics registered in pMOSFETs of figure 2 for bipolar RS (case A, circles in Fig. 6) and unipolar RS (case C, squares in Fig. 6). During the HRS, although the shape of the curves is not lost, the drain currents are reduced respect the fresh ones, being this reduction larger for the bipolar RS. This drain current reduction indicates that some damage remains in the dielectric during the HRS in comparison with the fresh device.

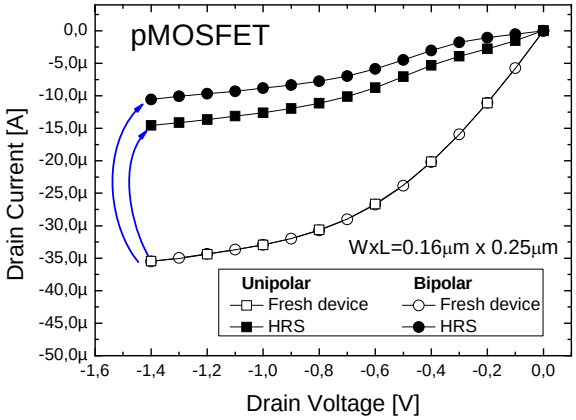

Fig. 6: pMOSFET I_D-V_D characteristic of the fresh device (open symbols), and during the HRS (closed symbols) for the bipolar (circles) and unipolar (squares) cases of Figure 2. When the sample is at the HRS the shape of the transistor characteristics is not lost but with a strong drain current reduction.

On the other hand, figure 7 shows the fresh (open symbols) and HRS (closed symbols) I_D-V_D characteristics of nMOSFETs of figure 3 for the bipolar RS (case A, circles in fig.7) and unipolar RS (case B, squares in fig.7). For unipolar RS, a small reduction in the drain current during HRS is observed respect the fresh device. However, for the bipolar case, the HRS drain current registered is larger than the fresh case (increment of ~75% in this measure). Then, for unipolar and bipolar switching in pMOSFET transistors and bipolar in nMOSFETs a positive charge trapping in the bulk dielectric at the HRS is observed, in agreement with [11, 16]. This positive charge trapping produces a positive drain current shift respect the fresh one in these cases, in accordance with the negative threshold voltage shifts observed in fig. 5. In the unipolar case of nMOSFETs, the observed drain current reduction respect the fresh case could be related

to negative charge trapping induced during the electrical characterization that has a predominant role in front of the positive charge trapping.

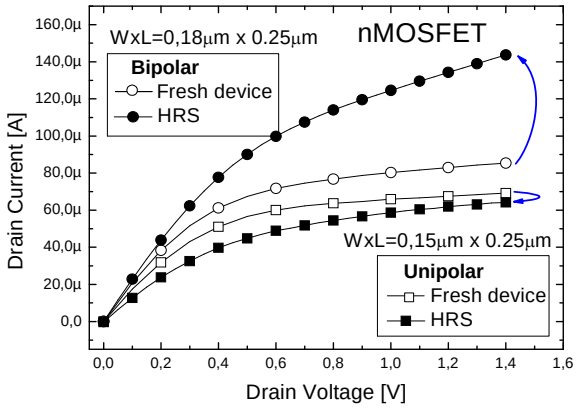

Fig. 7: nMOSFET I_D-V_D characteristic of the fresh device (open symbols) and during the HRS (closed symbols) for the unipolar (squares) and bipolar (circles) cases of Figure 3. When the sample is at the HRS the transistor characteristics are not lost and the device can still be functional. For the bipolar case, a drain current increase is observed respect the fresh one.

5. Conclusions

Resistive Switching phenomenology is studied in n and pMOSFETs with ultrathin Hf based dielectric. The influence of the voltage polarity to reach the HRS and LRS on the RS phenomenology has been evaluated. Unipolar and bipolar RS is observed for n-type and p-type transistors. However, for pMOSFETs, RS is possible only when the Set process is performed at negative bias. For nMOSFETs, the RS has been observed only when the Reset is produced at positive bias. The effect of the HRS on the transistor threshold voltage and drain current have been also analyzed. For unipolar and bipolar RS in pMOSFETS or bipolar RS in nMOSFETs, we have observed a negative shift of threshold voltage (and consequently a positive drain current shift) at the HRS. This will suggest a positive charge trapping in the bulk oxide as a consequence of the conductive filament created in the dielectric. For unipolar RS in nMOSFETs a positive shift of the threshold voltage and drain current reduction is obtained, which could be related to negative trapping during the characterization process. The results can be useful for a deeper understanding of the RS effect on the MOSFETs performance from a reliability point of view.

Acknowledgements

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