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STUDY OF SILICON CARBIDE POWER MOSFETS BEHAVIOUR IN OUT-OF-SOA CONDITIONS

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“Experience is what you get
when you didn't get what you wanted”
(Randy Pausch)

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Introduction

Power semiconductor devices are fundamental components of all electronic systems that generate, manage and distribute energy. Nowadays electronics is widely used in many different application fields, such as industrial, consumer, automotive, aerospace, etc. The increasingly demand for reduction in size and cost, as well as higher efficiency and power capability are common for all these applications.

Silicon has dominated power semiconductor industry for several decades, thanks to many years of development and well-established fabrication technology leading to high manufacturing capability and extremely low cost. Nevertheless, Si-based devices have almost approached their performance limits; consequently, a different strategy is needed to overcome this issue. The use of wide band gap semiconductors could provide enhancement of power devices performances.

Silicon Carbide (SiC), in particular, is a promising material for the realization of high voltage, high power devices, offering improved efficiency, reduced size, and lower overall system cost. The major upsides come from several material features such as elevated critical electric field, low leakage current, high thermal conductivity, etc., which result in reduced on-resistance, fast switching frequency and considerable temperature capability for SiC devices.

Indeed, in recent years, Silicon Carbide Power devices, mainly power diodes and MOSFETs, have become commercially available and have begun to replace their Silicon counterpart in many application areas. Despite the fast progress in device technology experienced recently, which allowed the fabrication of devices with increasing performances, there is still margin for quality and cost improvements. In fact, a wider spread of these devices could not be achieved without a deep analysis of the elements that might affect their reliability.

Usually, a key feature of power devices is their ability of withstanding current, voltage and temperature conditions well in excess of their nominal continuous ratings. In order to define their limit to withstand

the most demanding working operations, devices are usually investigated during critical stressful conditions. Most commonly, during avalanche and short-circuit (SC) operations. Therefore, it is mandatory for a device to be designed with a reasonable out-of-SOA robustness. Nevertheless, this could not be accomplished without an understanding of the underlying physical mechanisms of the failure event.

In this context, the main aim of this thesis work is the analysis of aspects regarding SiC Power MOSFETs reliability, with particular focus on short-circuit operation, through both physical simulations and experimental characterizations.

Thesis Contents

The thesis illustrates, after a theoretical background, simulation and experimental results performed to investigate SiC Power MOSFETs short-circuit capability. It is divided in five chapters and three appendices with the following outline:

Chapter 1 briefly recalls the main physical properties of Silicon Carbide that are mostly suitable for the realization of power devices. After short historical evolution of SiC devices, the energy band gap, the intrinsic carrier concentration, the critical electric field, the thermal conductivity and the electron mobility are illustrated and compared to Silicon. Moreover, definition of figures of merit commonly used to associate material features with device performances are given.

Chapter 2 deals with power MOSFETs in terms of basic structure and theory. Static and dynamic electrical behaviour are qualitatively recalled. The chapter concludes with the illustration of device blocking mode and Safe Operating Area.

Chapter 3 deals with TCAD simulations. First, an overview of TCAD simulator is reported together with brief description of tool used to generate the structure and simulate the device. Afterwards, the steps followed to reproduce device structure and the adopted physical models are illustrated. Simulation results are then reported. In particular, the static calibration of the structure on measured I_D-V_{GS} curves of a

commercial device is shown. Then, results for short-circuit simulations are reported, highlighting the physical mechanisms involved during short circuit and failure event. In addition, analysis of variation in design parameters on short-circuit capability is also described. Finally, simulations during avalanche operation are shown.

Chapter 4 deals with experimental characterization. After recalling the basic concepts of short-circuit test and after illustrating the used experimental system, the obtained outcomes are shown. They are divided in two groups: short pulse duration test and long pulse duration test. It is shown that two different failure types can occur. In addition, verification of thermal instability is also experimentally demonstrated.

Chapter 5 concludes the work analysing all the results obtained. Two separate phenomena might happen when a device fails. It is possible to identify in the temperature the origin of these mechanisms.

Chapter 1

Silicon Carbide as New Material for Power Electronics

Silicon Carbide (SiC) is a wide band gap semiconductor material that has experienced rapid development in recent years and it is slowly replacing Silicon devices in many power electronic applications. Research on Silicon Carbide started already before 1960s, even though difficulties in fabricating high-quality crystals and the increasing success of Silicon technology put SiC studies apart [1]. Subsequent technology improvements and new fabrication techniques [2]-[3], which allowed the fabrication of higher quality SiC wafers, renewed the interest in this material, especially its applicability in the power electronics area. Silicon-based power semiconductor devices have almost reached material theoretical limits; therefore, new alternatives are needed to satisfy high-performance power systems requirements. As it will be illustrated in this chapter, many advantages might arise from the use of SiC semiconductor thanks to its inherent physical properties, such as wide band gap, high critical electric field, high thermal conductivity, etc.

First SiC high voltage devices to be demonstrated were Schottky barrier diodes [4]-[6] or PiN diodes [7]-[8]. Active devices were demonstrated as well, such as SiC vertical JFETs [9]-[11] and high voltage MOSFETs [12]-[16]. The main problem associated with power MOSFETs in Silicon Carbide was the very poor quality of the oxide/semiconductor interface, which turned in low channel mobility and device reliability issues [17]-[18].

Initially, the diffusion and the development of those devices were hindered by the quality of the material and the size of defect-free areas on SiC wafers [19]. In fact, following the market evolution of past years (Figure 1.1), almost a decade passed between the first commercial SiC

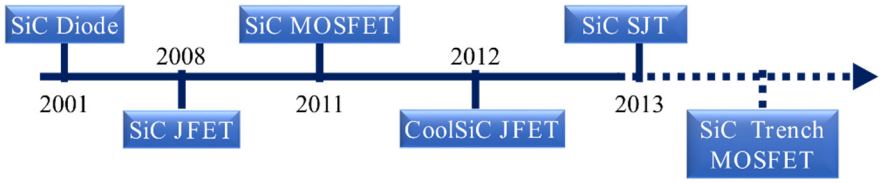

Figure 1.1: Milestones of commercialization of SiC power devices

power device in 2001, which was a Schottky diode, and the first affordable mass produced Power MOSFET in Silicon Carbide in 2011 ([20]-[23]).

Silicon Carbide has different polytypes, i.e. it can have more than one crystal structure different for the stacking order of succeeding layers of Carbon and Silicon atoms. Each polytype has its characteristic physical features. Among all possible polytypes, 3C-SiC, 4H-SiC and 6H-SiC (Figure 1.2) are the most studied for electronic applications, even though the preferred choice for power devices is the 4H-SiC polytype due to higher mobility [24]. Detailed description of SiC crystal structure can be found in specialized literature (e.g. [25]).

In the following a brief description of 4H-SiC main physical properties, as can be found in literature [26]-[27], will be reported.

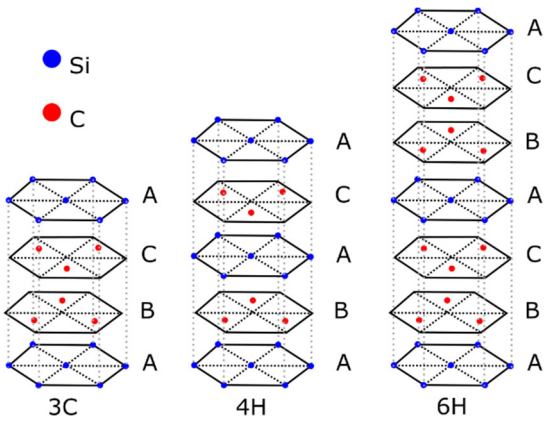

Figure 1.2: Stacking sequence for 3C-SiC, 4H-SiC and 6H-SiC

1.1 Energy band gap and intrinsic carrier concentration

As already said, Silicon Carbide is a wide band gap semiconductor. This means that the energy gap between the valence band and the conduction band is wider than other semiconductors materials (e.g. Silicon or Gallium Arsenide). For 4H-SiC the band gap is equal to about 3.26 *eV*, almost three times higher than Silicon. The intrinsic carrier concentration can be calculated in function of temperature *T* and energy band gap E_G as:

$$n_i = \sqrt{N_C N_V}\, e^{\frac{-E_G}{2kT}} \tag{1.1}$$

with $N_{C,V}$ conduction and valence bands density of states and *k* Boltzmann's constant. The (1.1) can be written for Silicon and SiC as:

$$n_{i\_\mathrm{Si}} = 3.87 \cdot 10^{16} T^{3/2} e^{\frac{-7.02 \cdot 10^3}{T}} \tag{1.2}$$

$$n_{i\_4\mathrm{HSiC}} = 1.7 \cdot 10^{16} T^{3/2} e^{\frac{-2.08 \cdot 10^4}{T}} \tag{1.3}$$

At room temperature T_0=300 *K* the intrinsic carrier concentrations for Si and 4H-SiC are respectively $1.4 \cdot 10^{10}$ cm^{-3} and $6.7 \cdot 10^{-11}$ cm^{-3}. The intrinsic carrier concentration as a function of temperature is plotted in Figure 1.3.

Low intrinsic carrier density allows device operations at higher temperature. Indeed, n_i is determined by bulk electron-hole pairs thermal generation. The leakage current of a device is dependent from the intrinsic concentration, and obviously it should be minimized for reliable and efficient devices operation. Silicon operating temperature is usually limited at about 150 °*C* before intrinsic concentration becomes comparable to typical doping concentration of 10^{14} cm^{-3}, while SiC devices do not suffer this issue for temperature even above 500 °*C*. Obviously, in this case, device operating temperature is limited by other factor such as packaging, contact/bond wires metal, etc.

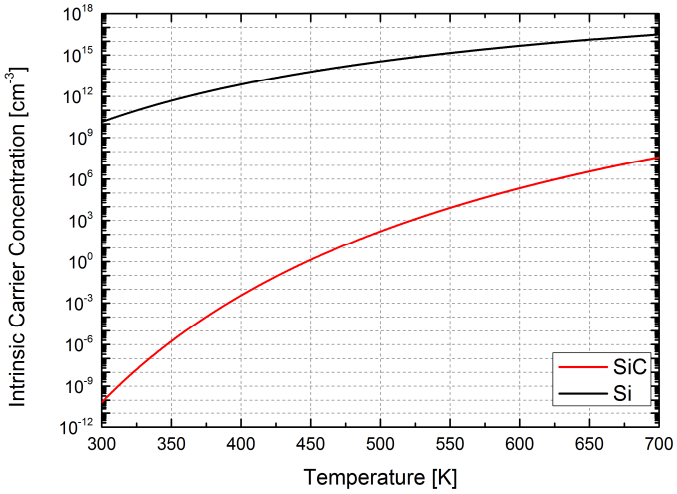

Figure 1.3: Intrinsic carrier concentration as a function of temperature

1.2 Critical electric field

One of the most celebrated feature of Silicon Carbide is its elevated critical electric field E_{cr}. It corresponds to the electric field for which impact ionization takes place. This property is due to higher impact ionization coefficient compared to other materials, direct consequence of the wide band gap energy. If Silicon has a critical electric field of about $3 \cdot 10^5$ *V/cm*, in Silicon Carbide it is approximately one order of magnitude higher, $2\text{-}3 \cdot 10^6$ *V/cm*. E_{cr} is a function of the semiconductor doping concentration, and different analytical formulas were proposed to model its behaviour. A simple power law was suggested in [26]:

$$E_{cr} = 3.3 \cdot 10^4 N_D^{1/8} \tag{1.4}$$

According to [28] it could be also expressed as:

$$E_{cr} = \frac{2.49 \cdot 10^6}{1 - 0.25 \log_{10}\left(N_D / 10^{16}\right)} \tag{1.5}$$

The critical electric field for SiC can be compared in Figure 1.4 with that of Silicon (calculated according to [29]). As it is clearly visible in the case of Silicon Carbide E_{cr} is much larger. This feature results in a thinner and higher doped drift layer compared to that of Silicon devices for the same breakdown voltage. In fact, the relations between E_{cr}, V_{BR} and W_D are:

$$V_{BR} = \frac{1}{2}\frac{E_{cr}^2 \varepsilon_s}{qN_D} \tag{1.6}$$

$$W_D = \frac{2V_{BR}}{E_{cr}} \tag{1.7}$$

Thus, given a desired V_{BR}, the doping concentration N_D can be increased and the thickness W_D can be reduced respect to equivalent Si device. The major upside of having a thin, high-doped layer is to reduce the specific ON-resistance $R_{ON,sp}$ of drift region. The same result can be inferred relating directly $R_{ON,sp}$ to the critical electric field:

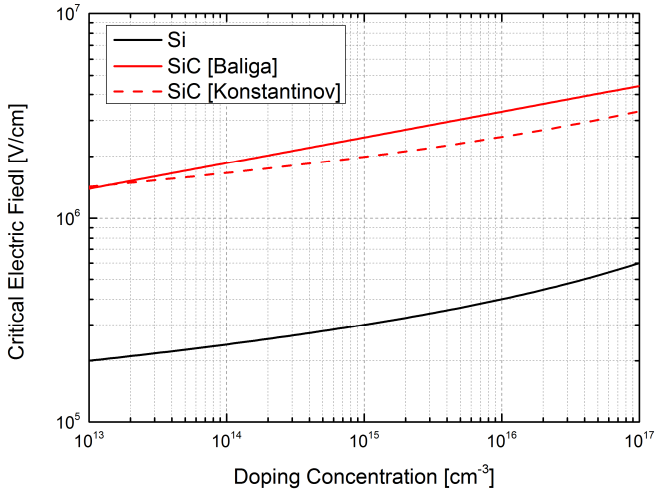

Figure 1.4: Critical electric field as a function of doping concentration

$$R_{ON,sp} = \frac{4V_{BR}^2}{\varepsilon_s \mu_n E_{cr}^3} \tag{1.8}$$

Since this parameter defines how much resistive loss a device generates while operating in conduction, it can easily be understood the great advantage in using wide band gap semiconductors.

1.3 Thermal conductivity and electron mobility

Silicon Carbide features a thermal conductivity λ about three times higher compared to Silicon, with its value approximately equal to 3.7 *W/cmK*. The high thermal conductivity allows a better diffusion of heat generated inside the material. Consequently, it could be possible to increase the device operating power level or to simplify cooling strategies (heatsink, fans, etc.) reducing system cost and volume.

Electron mobility for SiC is usually lower than Silicon, and it strongly depends material characteristics such as doping and direction of epitaxially grown crystals [30]-[32]. Moreover, for metal-oxide-semiconductor structure mobility is extremely dependent on interface quality, being affected by defects and traps density [33]-[34]. As an example, Figure 1.5 depicts the mobility in function of doping concentration following the model reported in [26].

Finally, SiC also exhibits a saturation velocity v_{sat} almost twice as high as Silicon, approximately of $2 \cdot 10^7$ *cm/s*.

Some values of the main SiC properties are listed in Table 1.1:

Properties	Si	4H-SiC
E_G [*eV*]	1.12	3.26
ε_r	11.7	9.7
λ [*W/cmK*]	1.5	3-5
E_{cr} [*V/cm*]	$3 \cdot 10^5$	$2\text{-}3 \cdot 10^6$
v_{sat} [*cm/s*]	10^7	$2 \cdot 10^7$

Table 1.1: Main material properties

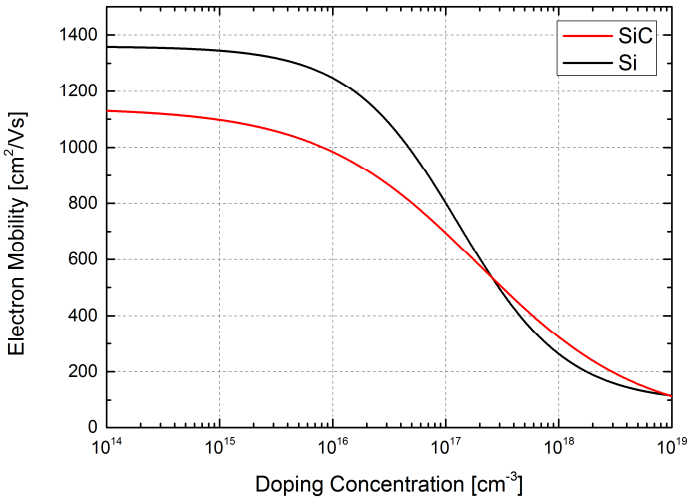

Figure 1.5: Electron mobility as a function of doping concentration

1.4 Figures of merit

Several investigations on the relation between the performances of semiconductor devices and material parameters have been performed in the past. Figures of merit have been derived to compare different material theoretical performances. Here, some of the most common figures of merit are briefly recalled.

Johnson's figure of merit (*JFM*) is defined as [35]:

$$JFM = \left(\frac{E_{cr} v_{sat}}{2\pi} \right)^2 \tag{1.9}$$

which defines the high frequency and high power capability of transistors.

Thermal limitation on high-frequency switching behaviour is considered with the Keyes' figure of merit (*KFM*) [36]:

$$KFM = \lambda \left(\frac{c v_{sat}}{4\pi\varepsilon_r} \right)^{1/2} \tag{1.10}$$

Baliga related material characteristic to conduction losses in field effect transistors, defining two figures of merit for both low-frequency and high-frequency operations [37]-[38]:

$$BFM = \varepsilon_r \mu E_G^3 \tag{1.11}$$

$$BHFFM = \mu E_{cr}^2 \left(\frac{V_G}{4V_{BR}} \right)^{1/2} \tag{1.12}$$

with V_G and V_{BR} gate and breakdown voltage, respectively.

Regardless of the particular values of those figures of merit, which obviously depend on the numerical parameters used, it comes clear the great advantages of using Silicon Carbide or more generally wide band gap semiconductors. Thanks to their excellent physical properties, their figures of merit result higher when compared to Silicon with consequent benefits in high temperature, high power, fast switching applications.

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Chapter 2

Power MOSFET: Principles of Operation

Since the first introduction in late 1970s of the Power MOSFET (*metal-oxide-semiconductor field effect transistor*), its improved performances compared to power BJTs were evident. Having a high input impedance and being a voltage-controlled device, power MOFESTs became immediately preferable respect to BJTs for their ease of control. Moreover, since power MOSFETs are not affected by stored charge in the drift region, they can feature high commutation frequency making them preferred device for high power, high frequency systems. Nevertheless, the application of MOSFETs is limited to operating voltages of about 600 V because the on-state resistance has an increasing trend with the maximum blocking voltage. In fact current handling capability is dictated by the power dissipated on the internal resistance during conduction.

The first commercially diffused device was the V-groove structure (VMOSFETS) subsequently replaced by the double-diffused structure (DMOSFET) due to manufacturing difficulties. Technology improvements brought to the realization of the trench-gate MOSFET (or UMOSFET) in which the channel was created vertically reducing the internal resistance by removing the parasitic resistance of the JFET region [1].

Introduction of Silicon Carbide (SiC) power devices, made it possible to considerably increase the maximum blocking voltage, letting power MOSFETs to spread in application areas where usually IGBTs are used. It is a consequence of material features that enabled to considerably reduce the resistance of the drift region and fabricating very high voltage devices. SiC Power MOSFET commercially available have the planar MOSFET structure, even though Trench SiC MOSFETs have

been demonstrated [2]-[3] and near to mass production diffusion [4]. Hence, in the following, the planar structure will be illustrated.

In this chapter, the fundamental principles of operation of a power MOSFET will be recalled. First, the basic structure of a planar MOSFET will be illustrated; afterwards, conduction and switching behaviour will be analysed. Finally, some aspects regarding the Safe Operating Area (SOA) and the reverse bias operation will be discussed.

2.1 MOSFET Basic Structure

The cross section of a planar MOSFET half-cell is depicted in Figure 2.1. The main characteristic is its vertical structure that allows supporting high voltages thanks to the thick low-doped drift layer.

Starting from an N^+ doped substrate, the N^- drift layer is fabricated by epitaxial grown. P-type base (or body) and N^+ source regions are then implanted and the channel length is defined by difference in lateral extension of these two regions. Unfortunately, this structure developed for Silicon devices cannot be directly applied to fabricate reliable SiC power MOSFETs. The doping concentration of the base region to obtain reasonable values for the threshold voltage should be so low that the device cannot sustain high blocking voltages due to reach-through phenomenon. Another important issue that has to be tackled is the high electric field the gate oxide is subjected to, which could exceed the

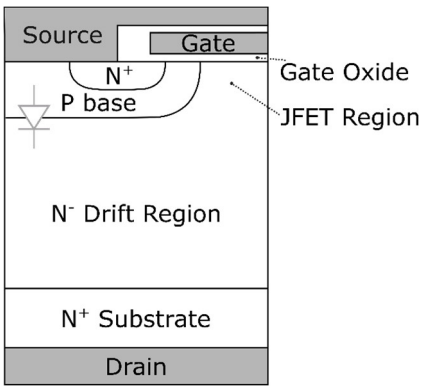

Figure 2.1: Planar MOSFET half-cell cross section

oxide breakdown strength leading to failure of devices while blocking high voltages. In fact, the electric field within the oxide is linked to the field present in the semiconductor by Gauss's Law [5]:

$$E_{ox} = \frac{\varepsilon_{semi}}{\varepsilon_{ox}} E_{semi} \tag{2.1}$$

The dielectric constant of Silicon Carbide is approximately three times larger than the one of Silicon Dioxide, therefore the electric field in the oxide could approach the critical limit for reliable device operation (~10^6 *V/cm*). A possible solution to overcome this issue is to employ dielectric materials with high permittivity [6]. An alternative approach is to modify the classical cell structure to screen the gate oxide from the elevated field within the semiconductor. This led to the concept of *shielded planar structure* [7]. It is characterized by a buried P^+ region extending beneath source and base diffusions that forms a shielding barrier for the electric field. The shielding region could even slightly go beyond the P-base edge extending in the JFET region (Figure 2.2). In this way, it is possible to lower the value of the electric field reaching the gate oxide. Moreover, the channel is shielded as well, thus it is possible to select the P-base doping concentration to obtain a suitable threshold voltage and, at the same time, keeping a high blockage capability properly designing the shielding diffusion.

Considering the electrons path from source to drain terminals, the total resistance is given by the sum of different components, as depicted in Figure 2.3.

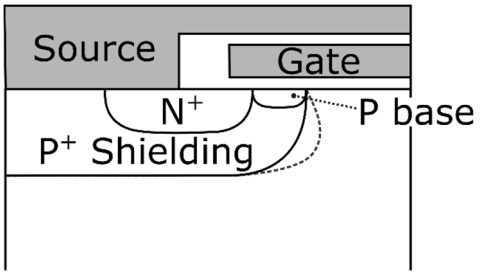

Figure 2.2: Detail of the shielding MOSFET structure

R_{CH} is the resistance due to electron flowing in the channel, function of channel length and applied gate voltage. In SiC MOSFET this resistance is also affected by semiconductor/oxide interface roughness and defects. Electrons injected from the channel in the drift region spread in the JFET region. Two resistances are associated therein: R_{JFET} dependent from N^- doping concentration and body/drift depletion width; R_A given by an accumulation layer below the gate oxide, which is formed by the positive applied gate voltage. Then, electrons flowing in the epitaxial layer encounter resistance R_{DRIFT} of the low-doped drift region of thickness W_D. Its value, as said before, depends on the device blocking capability and strongly limits maximum rated voltage. In SiC MOSFTEs, as will be shown later, drift layer doping concentration is much higher and its dimension lower compared to Silicon devices, thus it results in a reasonable value for R_{DRIFT} even when reaching high breakdown voltage. Finally, resistances of the heavily doped source and substrate regions, as well as contact resistances, can be neglected for high voltage devices. Total ON-state resistance R_{ON} is the sum of the aforementioned components. This resistance limits the maximum power handling capability, since the ON-state dissipated power can be expressed as:

$$P_D = I_D V_D = I_D^2 R_{ON} \tag{2.2}$$

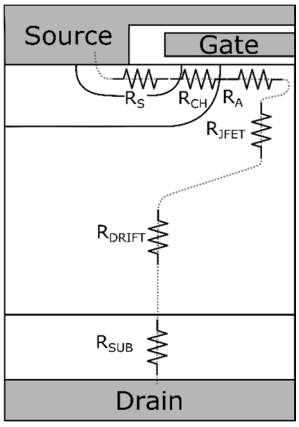

Figure 2.3: Different components of power MOSFET internal resistance

As already explained, due to power dissipation constraints, Silicon Power MOSFETs diffusion is limited up to 600 *V* applications. Above this value, IGBTs are the preferable choice. However, introduction of Silicon Carbide allowed Power MOSFETs to enter new application fields and to realize high performance and efficient systems.

Finally, it has to be noted that power MOSFETs have an intrinsic *pn* diode, called *body diode*, formed by the base/drift regions (Figure 2.1).

2.2 Static Characteristics

Upon application of positive gate-to-source voltage, a current conducting channel is formed in the P body region underneath the gate electrode. Voltage for which the electron concentration under gate contact becomes equal to P-base doping concentration (i.e. inversion layer is produced) is defined as the *threshold voltage* V_{TH}. Usually, for a Power MOSFET the threshold voltage is typically 2-4 *V*. Electrons are then free to flow when applying a drain-to-source potential. The current-voltage characteristics are determined by behaviour of channel layer as a function of gate and drain bias voltages [9].

For $V_{GS}<V_{TH}$ there is no channel formed, thus no flow of charge is present in the structure. Just a certain amount of subthreshold leakage current flows through the device, which depends exponentially on V_{GS}.

For $V_{GS}>V_{TH}$ but for small drain bias voltages compared to gate voltage ($V_{DS}<V_{GS}-V_{TH}$) an electron current flows between drain and source, where the current can be analytically expressed as:

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[\left(V_{GS} - V_{TH}\right)V_{DS} - \frac{1}{2}V_{DS}^2 \right] \tag{2.3}$$

with *W*, *L* channel width and length respectively, $C_{ox}=\varepsilon_{ox}/t_{ox}$.

For $V_{GS}>V_{TH}$ and with drain voltages comparable or greater than gate bias ($V_{DS}>V_{GS}-V_{TH}$) the electric potential "pinches off" the channel and the inversion layer no longer continues till the drift region, then the resistance to current flow increases. The saturation current is:

$$I_{Dsat} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}\left(V_{GS} - V_{TH}\right)^2 \tag{2.4}$$

An example of power MOSFET I_D-V_{DS} characteristics is reported in Figure 2.4 for different gate bias voltages.

Figure 2.5 depicts the I_D-V_{GS} curves, also known as trans-characteristics, for a fixed V_{DS}=20 V and at two different temperatures. The effect of temperature is of particular interest. Current can exhibit either a positive or a negative temperature coefficient depending on the value of the applied V_{GS}. This behaviour is due to the different dependence the drain current has on threshold voltage and electron mobility, which both decreases with temperature. The current would increase if the variation of V_{TH} with temperature is predominant. It would decrease, on the other hand, if the effect of mobility prevails. The boundary value that distinguishes the two regions is the crossover point (or temperature compensation point). Biasing the gate below this point could result in uneven current distribution and unstable behaviour, as it will be explained later in Chapter 4 (§4.2.3).

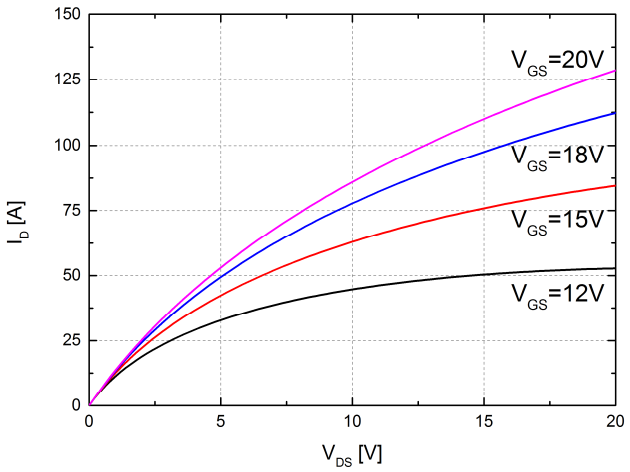

Figure 2.4: Typical I_D-V_{DS} curves for a Power MOSFET at different V_{GS}

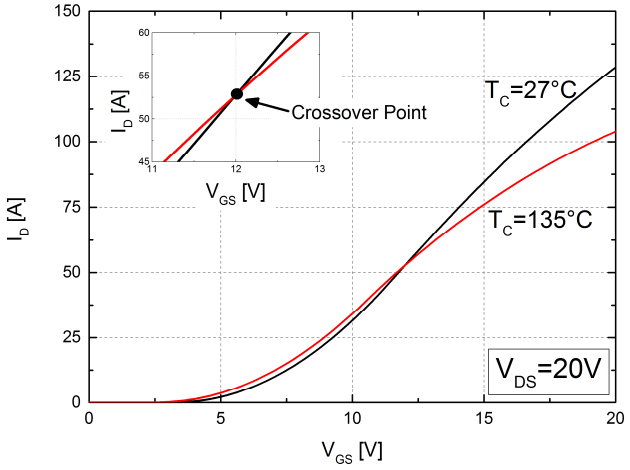

Figure 2.5: Typical I_D-V_{GS} curves for a Power MOSFET at different temperatures

2.3 Transient Characteristics

The main feature of Power MOSFETs, compared to IGBTs, is their high commutation speed, since no minority carrier injection in the drift region is needed. This is a key characteristic in developing systems for high frequency applications. Switching behaviour is determined by MOSFETs intrinsic capacitances, as well as parasitic resistances and inductances. An equivalent circuit representing the different internal device capacitances between output terminals is reported in Figure 2.6. The input capacitance (indicated as C_{iss} on datasheets) is the sum of the gate/source capacitance C_{GS} and the gate/drain capacitance C_{GD}. The latter, also known as Miller capacitance, has a nonlinear behaviour with voltage and it can be considered as the series of the oxide capacitance and a depletion layer capacitance. In blocking state, i.e. with high voltage applied, the depletion capacitance is the predominant factor, and the C_{GD} value is low due to the thickness of the depletion region. On the other hand, during conduction C_{GD} is determined by the oxide capacitance, having a much higher value. Therefore, device transients are largely affected by the large variation of this capacitance with the applied voltage. The described behaviour is shown in Figure 2.7.

In most of applications, power MOSFETs have to control an inductive load. Therefore, to qualitatively analyse the device switching behaviour the simple circuit of Figure 2.8 is considered [10]-[11], where the device load is an inductor L with a freewheeling diode D.

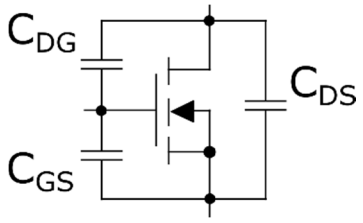

Figure 2.6: Capacitances for a Power MOSFET

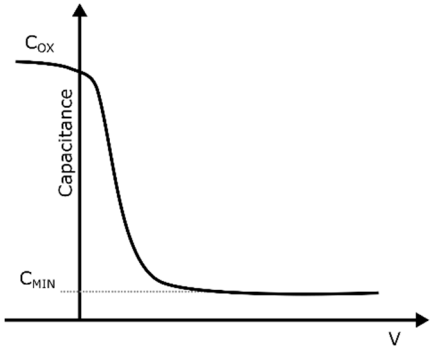

Figure 2.7: Dependence of C_{GD} on bias voltage

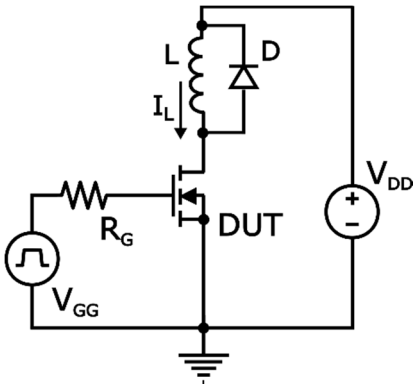

Figure 2.8: Simplified circuit for power MOSFET switching analysis

2.3.1 Turn-on Transient

Typical electrical waveforms time evolution is depicted in Figure 2.9. The device is initially in off-state, characterized by $i_D(t)=0$, $v_{GS}(t)=0$ and $v_{DS}(t)=V_{DD}$ and the load current I_L is flowing into the freewheeling diode. At time t_0 the driver applies a gate voltage V_{GG} that starts to charge the input capacitance and the turn-on transient begins. During the time interval t_0-t_1 no current flows through the device since the gate voltage is lower than the threshold voltage. The gate current charges the input capacitance and the V_{GS} rises exponentially with a time constant given by $R_G \cdot [C_{GS}+C_{GD}(v_{DS})]$. For $t>t_1$ the device starts to conduct, while the gate voltage keeps on increasing exponentially. At time instant t_2 the device carries the entire load current, the diode switches off and the voltage across the device starts to decrease. During t_2-t_3 V_{GS} remains constant since I_D is constant and the gate current is charging C_{GD}, which is changing with the drain voltage (this phase is known as *Miller plateau*). For $t>t_3$ the device enters the linear region with v_{DS} approaching the ON-state voltage drops, and the gate voltage exponentially increases until it reaches the value V_{GG}. The highest power dissipation during the turn-on transient occurs when both drain current and drain voltage have large values (time interval t_1-t_3).

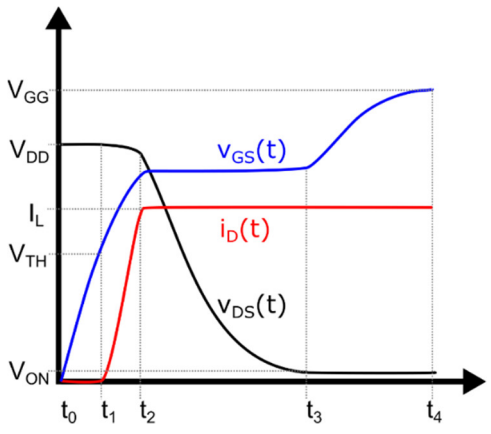

Figure 2.9: Turn-on waveforms for a power MOSFET

2.3.2 Turn-off Transient

Turn-off waveforms are depicted in Figure 2.10. The device is in ON-state carrying the entire load current I_L with a small voltage drop V_{ON}, while the diode is in OFF-state. As the driving circuit brings the voltage from V_{GG} to zero, a current is extracted from gate terminal to discharge the input capacitance. The gate voltage starts to exponentially decrease, until the device exits the linear region (instant t_1). During the time interval t_1-t_2 the drain voltage rises while the device is still carrying the full load current. The gate voltage is constant equal to the plateau value and the current sunk by the drive circuit discharges the gate-drain capacitance, which again is changing with the drain voltage. When the drain voltage is high enough, the freewheeling diode becomes forward biased and its current increases. As consequence, the MOSFET current begins to decrease. The gate voltage falls exponentially to zero and the device completely turns off when it becomes lower than the threshold voltage (time instant t_3). Finally, the load current flows completely in the diode. Even in this case, a significant power dissipation is present when both drain current and voltage are high (time interval t_1-t_3).

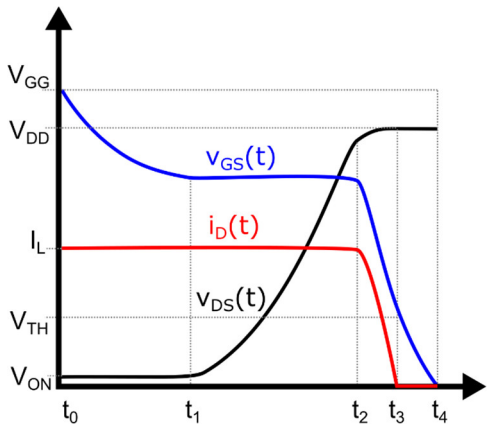

Figure 2.10: Turn-off waveforms for a power MOSFET

2.4 Safe Operating Area

The Safe Operating Area (SOA) defines the space within the *I-V* plane in which a power MOSFET can safely operate. If the device operative trajectory is completely located in the SOA, no destructive failures should occur. An example of SOA is reproduced in Figure 2.11.

Different limiting factors can be identified [10], [12]:

- $I_{D,MAX}$: indicated by an horizontal line, it is the maximum drain current the MOSFET can sustain, limited by device manufacturer (e.g. bonding-wires fusing);
- BV: limit imposed by the device breakdown voltage (vertical line);
- $R_{DS,ON}$: a portion of the operating area is limited by device ON-state voltage drop during conduction state. The limit depends on the ON-state resistance and can be expressed as:

$$\frac{V_{DS}}{I_D} \leq R_{DS,ON} \tag{2.5}$$

- P_{MAX}: this limit is dictated by the maximum sustainable junction temperature. During DC bias operations (solid lines in Figure 2.11) the limiting line is:

$$I_D = \frac{T_{J,MAX} - T_A}{V_{DS} Z_{th}} \tag{2.6}$$

When the device works under pulsed conditions (dashed lines in Figure 2.11) a larger drain current can be sustained due to reduced power dissipation. As the duty cycle (i.e. the pulse width) becomes small, the SOA enlarges approaching the ideal square-shaped SOA.

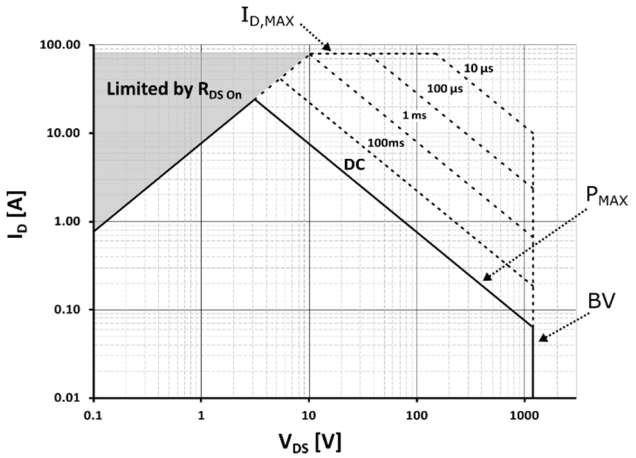

Figure 2.11: Safe Operating Area of a Power MOSFET

2.5 Blocking Mode

When the gate bias is zero, no current flows through the device and the applied voltage is supported by the depletion region across the body/drift *pn* junction *J1* (Figure 2.12). Supposing that the parasitic *npn* (source/body/drift) transistor is completely suppressed by short-circuiting with the metal layer the source/body regions, the maximum sustainable blocking voltage is determined by the critical electric field on the body/drift junction. For a shielded structure, the P^+ high doping concentration prevents the reach-through phenomenon of the P-base. Moreover, the high doping of the shielding region accentuates the depletion of the JFET area, increasing the gate oxide screening from elevated electric field.

Following the classical analysis considering a one-dimensional abrupt junction, it is possible to calculate the maximum of the electric field E_{MAX} and the width W of the depletion region (extending in the drift layer):

$$W = \sqrt{\frac{2\varepsilon_s V_D}{qN_D}} \tag{2.7}$$

$$E_{MAX} = \sqrt{\frac{2qN_D V_D}{\varepsilon_s}} \tag{2.8}$$

When applied voltage increases, E_{MAX} approaches the critical value for which impact ionization occurs.

Finally, if the voltage on the power MOSFET is reversed, the device will conduct a current through the intrinsic body diode.

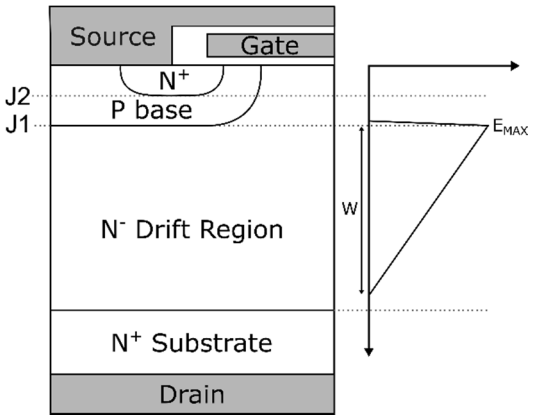

Figure 2.12: Schematic representation of electric field in blocking mode

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Chapter 3

Physical Electro-thermal Simulations

Deep investigation of semiconductor devices could be achieved if a complete knowledge of physical quantities evolution inside their structure is known. Since electronic components and systems have become more and more complex, use of numerical simulators is mandatory in modern applications. Simulation approach not only provides information on electronic systems operations prior to their realization, but it is an essential aid to devices and circuits design. Moreover, through simulations outcomes, failure causes can be analysed. Full understanding of failure mechanisms could have positive impact on future design of more reliable devices. For example, in application such as electrical vehicles or railway traction, where operating environment is extremely harsh, efforts are focused on the development of more rugged devices, which might be subjected to high power and high thermal stress. To this purpose, a careful simulation stage is needed.

Electron devices experience temperature increase due to heat generated inside. This is especially true for power devices since a considerable amount of heat is dissipated and they usually operate in high-temperature environments. The heat generation could be even more critical when handling large currents, as for example during short-circuit [1]. Hence, for a correct modelling of semiconductor devices temperature-dependent equations must be incorporated [2], as temperature strongly affects current transport phenomena and device behaviour.

Electro-thermal (ET) simulations could be performed using compact models to reproduce device behaviour [3]-[4]. Even though they can well reproduce devices operations, they could hardly report the exact evolution of physical quantities (e.g. temperature or carrier density distribution). On the other hand, Technology CAD (TCAD) simulators

are purely physics-based and allow to investigate electrical, thermal and optical properties of semiconductor devices [5]. TCAD simulations are a valuable tool for the design and the analysis of new devices, widely used in both industry and research semiconductor field. They has been proven to be of paramount importance for the analysis of power devices [6] and the investigation of their failure mechanisms [7]-[10].

In this chapter, after a brief overview of the TCAD simulator, the simulated structure of a SiC Power MOSFET will be presented along with some models used for the calibration procedure. Afterwards, simulation strategy and results will be illustrated.

3.1 TCAD Simulator

Technology Computer Aided Design (TCAD) refers to using computer simulations for designing and optimizing semiconductor processing technologies and devices. TCAD tools solve fundamental, physical, partial differential equations (e.g. diffusion and transport equations) for discretized geometries, representing the semiconductor device.

Thanks to their deep physical approach and predictive accuracy, TCAD simulations are widely used in the semiconductor industry. It is possible to substitute TCAD computer simulations for costly and time-consuming test wafer runs, in order to cut costs and speed up the research and development process of a new semiconductor device or technology. A rigorous explanation of TCAD simulators can be found in specialized literature (e.g. [5]).

Among all different simulators present on the market, for this work Synopsys Sentaurus TCAD suite [11] has been adopted.

Figure 3.1 depicts the typical flow-chart to run a simulation in Sentaurus TCAD.

The first step is to virtually fabricate the device that has to be simulated, defining geometry and doping profiles. To this purpose, process simulations can be performed, where technology steps such as etching, deposition, ion implantation, thermal annealing, and oxidation are simulated based on physical equations. It is a reliable and accurate method for reproducing real device structure, but the main drawback is that parametric simulations cannot be easily performed. A valid alternative could be reconstructing the structure knowing the

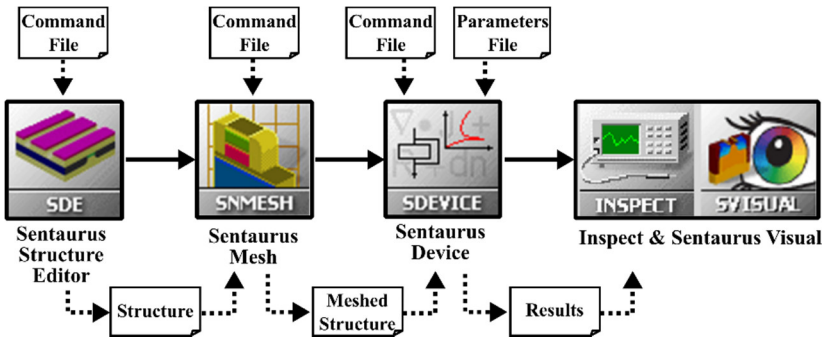


Figure 3.1: Simulation flow in Sentaurus TCAD

geometrical dimensions (e.g. from SEM sections) and creating the doping profile as superposition of elementary analytical expressions (e.g. Gaussian or Error-function). The latter approach has been adopted in this work, using the software *Sentaurus Structure Editor*. This tool allows to define geometry, materials and doping profiles, both for 2D and 3D structures.

The realized structure is discretized onto a nonuniform *grid* (or *mesh*) of nodes. That is, the device is represented as a meshed finite-element structure, where each node of the device has physical properties associated with it. For each node physical equations are solved and the carrier concentration, current densities, electric field, generation and recombination rates, etc., are computed. Thus, an efficient mesh is compulsory to obtain valid results, and therefore the number of points has to be carefully chosen as compromise between results accuracy and simulation time. A suitable mesh can be obtained by trial and error, even though some practical rules can be applied. Usually, number of nodes should be increased in areas where some physical parameters could have a significant spatial gradient. It means, for example, that the mesh should be denser where it is expected to have high current density or high electric field. Considering a Power MOSFET, critical sections usually are the channel, the body/drift depletion region, the interface oxide/semiconductor, the JFET region. *Sentaurus MESH* is the tool provided with Sentaurus TCAD to discretize spatial domains. Its axis-aligned mesh generator engine produces triangles in the case of 2D devices and tetrahedra in the case of 3D devices.

Once a proper mesh has been completed, the device can be simulated with *Sentaurus Device*. In order to run a simulation (which can be

thought of as virtual measurements of the electrical behaviour of a semiconductor device) different sections in the command file have to be specified. In the *physics* section adopted models describing physical mechanisms are listed. Solver configuration and settings helping convergence are defined in a *math* section. The *solve* section specifies which type of simulation has to be computed (quasistationary, transient, etc.) using the boundary conditions specified in the *electrode* statement. Parameter values for different activated models are reported in an external **.par* file. Output data such as terminal characteristics, physical quantities (specified in a *plot* section) can be then visualized by *Sentaurus Visual* or by *Inspect*.

The simulation of a device implies the computation of terminal currents and voltages using a set of physical equations that describes the carrier distribution and conduction mechanisms [12].

The very first step to simulate a device is to compute the initial condition, i.e. the electrostatic potential. It can be done solving the Poisson's equation:

$$\nabla \cdot \left(\varepsilon \nabla \phi \right) = -q\left(p - n + N_D - N_A \right) - \rho_{trap} \tag{3.1}$$

where ε is the electrical permittivity, q is the electronic charge, n and p are the electron and hole densities, N_D is the concentration of ionized donors, N_A the concentration of ionized acceptors and ρ_{trap} is the charge density due to traps and fixed charges. Assuming valid the Boltzmann statistics and given the quasi-Fermi potentials, the electron and hole densities can be obtained as follow:

$$n = N_C \exp\left(\frac{E_{F,n} - E_C}{kT} \right) \tag{3.2}$$

$$p = N_V \exp\left(\frac{E_V - E_{F,p}}{kT} \right) \tag{3.3}$$

where N_C and N_V are the effective density-of-state, $E_{F,n}$ and $E_{F,p}$ the quasi-Fermi energy levels for electron and hole, E_C and E_V the conduction and valence band edges. Continuity equations are further

fundamental equations used to describe a semiconductor. They express the charge conservation and can be written as:

$$\nabla \cdot \boldsymbol{J_n} = qR_{net} + q\frac{\partial n}{\partial t} \tag{3.4}$$

$$-\nabla \cdot \boldsymbol{J_p} = qR_{net} + q\frac{\partial p}{\partial t} \tag{3.5}$$

where $\boldsymbol{J_n}$ and $\boldsymbol{J_p}$ are the electron and hole current densities respectively, R_{net} is the net recombination.

The analytical expressions of $\boldsymbol{J_n}$ and $\boldsymbol{J_p}$ differ according to the transport model used to compute them. Different models are included in Sentaurus, but power devices can be accurately described using just the *drift-diffusion model* and the *thermodynamic model*.

- **Drift-diffusion model**

It is the default transport model in Sentaurus. The general expressions for electron and hole current densities, valid both for Fermi and Boltzmann statistics, are:

$$\boldsymbol{J_n} = \mu_n\left(n\nabla E_C - 1.5nkT\nabla \ln m_n\right) + D_n\left(\nabla n - n\nabla \ln \gamma_n\right) \tag{3.6}$$

$$\boldsymbol{J_p} = \mu_p\left(p\nabla E_V - 1.5pkT\nabla \ln m_p\right) - D_p\left(\nabla p - p\nabla \ln \gamma_p\right) \tag{3.7}$$

Contribution due to the spatial variations of the electrostatic potential, the electron affinity, and the band gap is taken into account in the first term. The remaining terms take into account the contribution due to the gradient of concentration, and the spatial variation of the effective masses. Since Boltzmann statistic is considered, $\gamma_n = \gamma_p = 1$. Diffusivity coefficients can be calculated through mobilities by the Einstein's relation:

$$\frac{D_{n,p}}{\mu_{n,p}} = \frac{kT}{q} \tag{3.8}$$

In this case, (3.6) and (3.7) can be simplified to:

$$\boldsymbol{J_n} = -nq\mu_n \nabla \Phi_n \tag{3.9}$$

$$\boldsymbol{J_p} = -pq\mu_p \nabla \Phi_p \tag{3.10}$$

where Φ_n and Φ_p are the electron and hole quasi-Fermi potentials.

- **Thermodynamic model**

Current densities equations (3.9) and (3.10) are generalized in the thermodynamic model [13] to include temperature gradient as a driving term:

$$\boldsymbol{J_n} = -nq\mu_n \left(\nabla \Phi_n + P_n \nabla T \right) \tag{3.11}$$

$$\boldsymbol{J_p} = -pq\mu_p \left(\nabla \Phi_p + P_p \nabla T \right) \tag{3.12}$$

where $P_{n,p}$ are the absolute thermoelectric powers [14] and T is the lattice temperature.

- **Boundary conditions**

Boundary conditions must be defined at the borders of a domain to correctly solve differential equations and to obtain a unique solution. All contacts on semiconductors are, by default, Ohmic with a 1 $m\Omega$ resistance when connected to a circuit node. Moreover, charge neutrality and equilibrium are assumed:

$$n_0 - p_0 = N_D - N_A \tag{3.13}$$

$$n_0 p_0 = n_{i,eff}^2 \tag{3.14}$$

In the case of Boltzmann statistics:

$$\phi = \phi_F + \frac{kT}{q}\operatorname{asinh}\left(\frac{N_D - N_A}{2n_{i,eff}}\right) \tag{3.15}$$

$$n_0 = \sqrt{\frac{\left(N_D - N_A\right)^2}{4} + n_{i,eff}^2} + \frac{N_D - N_A}{2} \tag{3.16}$$

$$p_0 = \sqrt{\frac{\left(N_D - N_A\right)^2}{4} + n_{i,eff}^2} - \frac{N_D - N_A}{2} \tag{3.17}$$

where n_0 and p_0 are the electron and hole concentration at equilibrium and ϕ_F the Fermi potential. In the case of contacts on insulators (as gate contacts) electron potential is expressed as:

$$\phi = \phi_F - \Phi_{MS} \tag{3.18}$$

where Φ_{MS} is the work function difference between the metal and an the intrinsic level in the semiconductor.

Neumann condition is applied to all boundaries that are not contacts:

$$\varepsilon \nabla \phi = 0 \tag{3.19}$$

$$\boldsymbol{J}_{n,p} \cdot \hat{n} = 0 \tag{3.20}$$

As regards the boundary conditions for the thermal problem, for thermally insulated surfaces the following condition is applied:

$$k\hat{n} \cdot \nabla T = 0 \tag{3.21}$$

On the other hand, at thermally conducting interfaces the condition become:

$$k\hat{n} \cdot \nabla T = \frac{T_{ext} - T}{R_{th}} \tag{3.22}$$

with R_{th} external thermal resistance characterizing the thermal contact between semiconductor and adjacent material.

3.2 Structure and Physical Models

As explained before, device structure has to be reproduced in order to perform numerical simulations. After that, as it will be illustrated in the following, a phase to calibrate the structure is mandatory to match the simulated structure behaviour with the one of a real device.

The structure analysed is the one of a planar power MOSFET. Thanks to device inherent symmetry, just half elementary cell was reproduced.

Approximate geometrical dimensions were extracted from available SEM cross sections [15]-[17], depicted in Figure 3.2. Doping profiles were defined using common data reported in literature (e.g. [18]). The drift region thickness and its doping concentration were calculated from the breakdown voltage and supposing triangular electric field profile. According to [19] the critical electric field E_{cr} can be expressed as:

$$E_{cr} = \frac{2.49 \cdot 10^6}{1 - 0.25 \log_{10}\left(N_D / 10^{16}\right)} \tag{3.23}$$

and with the triangular shape for the electric field:

$$V_{BR} = \frac{1}{2} \frac{E_{cr}^2 \varepsilon_s}{q N_D} \tag{3.24}$$

$$W_D = \frac{E_{cr} \varepsilon_s}{q N_D} \tag{3.25}$$

Considering the actual breakdown voltage of approximately 1750 V for the 1.2 kV device analysed, it results: $N_D \sim 1.1 \cdot 10^{16}\ cm^{-3}$ and $W_D \sim 13 \mu m$.

The obtained structure, with its geometrical features, is reported in Figure 3.3.

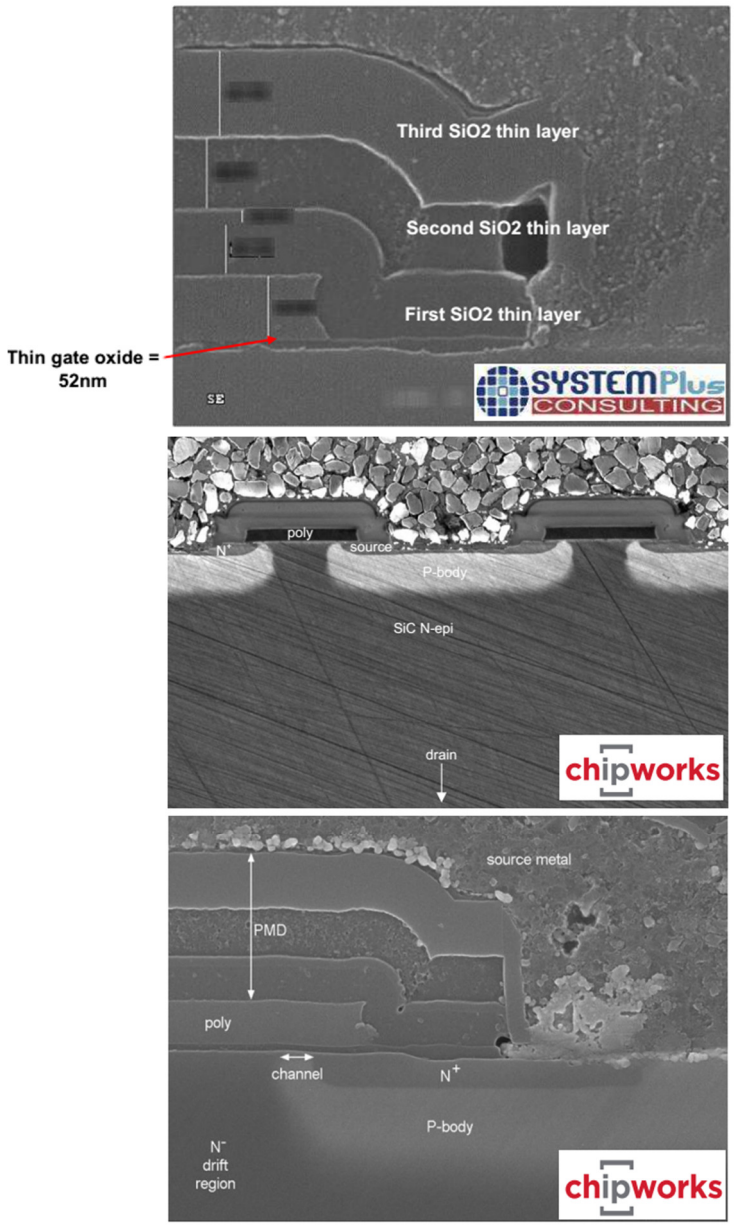


Figure 3.2: SEM cross sections used to evaluate device geometry

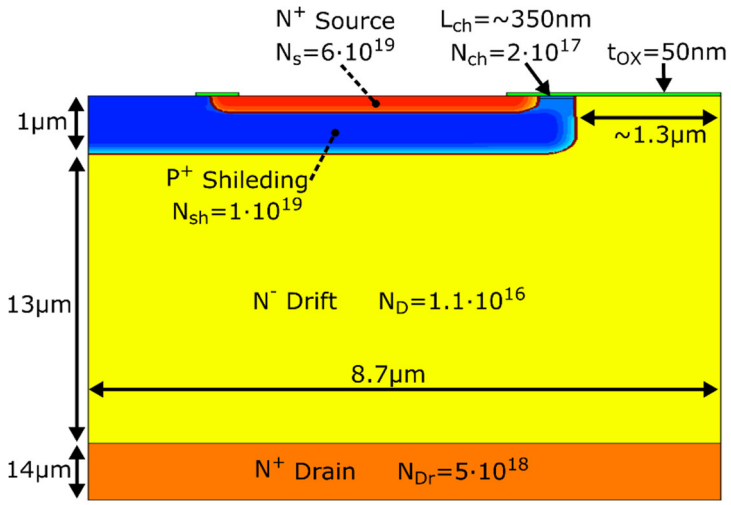


Figure 3.3: Simulated structure (not in scale)

The calibration procedure implied the choice of suitable physical models (e.g. mobility doping dependence, carrier recombination, etc.) and the proper tuning of their parameters. The approach followed [20] was to include models commonly used for Silicon but with parameters suitable for Silicon Carbide [20]-[22]. However, SiC has the specific feature of being an anisotropic compound, i.e. physical properties are different according to the crystal direction considered.

The simulator allows to take into account this particular aspect either defining different parameters set, or assigning an anisotropy ratio for the principal and the anisotropic directions.

Carrier mobility can be degraded by different mechanisms, such as temperature, doping concentration, interface degradation, electric field, etc. Several models are available in Sentaurus TCAD to account for these phenomena.

In this work, the doping dependence of the channel mobility has been taken into account enabling the Arora model [23]:

$$\mu_{Arora} = \mu_{\min} + \frac{\mu_d}{1+\left(\frac{N_D+N_A}{N_0}\right)^{A^*}} \tag{3.26}$$

$$\mu_{\min} = A_{\min}\left(\frac{T}{300K}\right)^{\alpha_m} \tag{3.27}$$

$$\mu_d = A_d\left(\frac{T}{300K}\right)^{\alpha_d} \tag{3.28}$$

$$N_0 = A_N\left(\frac{T}{300K}\right)^{\alpha_N} \tag{3.29}$$

$$A^* = A_a\left(\frac{T}{300K}\right)^{\alpha_a} \tag{3.30}$$

Channel mobility is particularly critical for SiC MOSFET devices since it is affected by the density of defects at the semiconductor/oxide interface [24]. Amount of fixed charges and traps levels can vary within orders of magnitude and depends on the technology processes [25]-[28]. Traps are usually considered to be acceptor type above midgap and donor type below it [29].

Traps and fixed charges strongly affect device performances acting on both channel mobility and threshold voltage. These defects not only influence channel mobility and threshold voltage values, but also their behaviour with temperature. Many works have reported effects of interface defects and dislocations on SiC MOSFET devices, characterizing their behaviour and modelling their temperature dependence [30]-[33]. Filled interface traps give rise to Coulomb scattering with inversion layer electrons, turning into poor channel mobility. Moreover, they cause a positive shift in the threshold voltage, which can be analytically expressed in function of the interface traps density D_{it} as [34]:

$$V_{TH} = V_{FB} + 2\phi_B + \frac{1}{C_{OX}}\left(\sqrt{2\varepsilon_s q N_A (2\phi_B)} + q\int_{E_i}^{E_i+q\phi_B} D_{it}(E)\,dE\right) \qquad (3.31)$$

As temperature increases the number of filled traps decreases since trapped electrons tend to be emitted. This leads to opposing effects on the drain current. There is a fast threshold voltage reduction due to the emission of inversion electrons that results in a positive temperature coefficient for drain current. Due to traps levels, the variation of V_{TH} with temperature it is usually greater compared to Silicon devices [35]. At the same time, traps discharging turns into a reduction of Coulomb scattering and a higher number of free carriers, improving the channel mobility. On the other hand, increasing of phonon scattering with temperature tends to reduce channel mobility. Therefore, in a range of temperature mobility actually increases until all electrons are released, while it decreases again for higher temperatures [35]-[36].

To account for the described phenomena, both positive fixed charges Q_F and acceptor type traps Q_A were introduced at the SiO_2/SiC interface of the simulated structure. Traps were described with a uniform energetic distribution [12]:

$$E_0 - 0.5E_S < E < E_0 + 0.5E_S \qquad (3.32)$$

where E_0 is the centre of the energy distribution from the conduction band level E_C.

Coulomb scattering has been considered using a proper degradation model [12]:

$$\mu_{coulomb} = \frac{\mu_1\left(\frac{T}{300K}\right)^k \left\{1+\left[c\Big/\left(c_{trans}\left(\frac{N_{A,D}+N_1}{10^{18}cm^{-3}}\right)^{\gamma_1}\left(\frac{N_{coulomb}}{10^{11}cm^{-2}}\right)^{\eta_1}\right)\right]^{\nu}\right\}}{\left(\frac{N_{A,D}+N_2}{10^{18}cm^{-3}}\right)^{\gamma_2}\left(\frac{N_{coulomb}}{10^{11}cm^{-2}}\right)^{\eta_2}\cdot D\cdot f(\mathrm{F}_\perp)} \qquad (3.33)$$

$$f(\mathrm{F}_\perp) = 1 - \exp\left[-\left(\mathrm{F}_\perp/E_0\right)^{\gamma}\right] \qquad (3.34)$$

$$D = \exp\left(-x / l_{crit}\right) \tag{3.35}$$

where $N_{Coulomb}$ is the negative interface charge density, c is the electron density (for electron mobility) or the hole density (for hole mobility) and $F_{\perp}$ is the electric field perpendicular to the interface.

In addition, the Canali model [37] accounting for carrier velocity saturation at high electric fields, and the Lombardi model [38] accounting for acoustic surface phonon scattering have been included.

Combination of different dependences is achieved by the Mattthiessen's rule:

$$\frac{1}{\mu} = \frac{1}{\mu_1} + \frac{1}{\mu_2} + \frac{1}{\mu_3} + \ldots \tag{3.36}$$

Finally, to simulate the device during breakdown, impact ionization generation has been taken into account. The avalanche generation is modelled by the simulator calculating the generation coefficient as [12]:

$$G_{ii} = \alpha_n n v_n + \alpha_p p v_p \tag{3.37}$$

where $\alpha_{n,p}$ are the ionization coefficients for electron and hole. Sentaurus Device implements different models to evaluate ionization coefficients, and the Okuto-Crowell has been adopted [12]:

$$\alpha\left(F_{ava}, T\right) = a\left(1 + c\left(T - T_0\right)\right) F_{ava}^{\gamma} \exp\left[-\left(\frac{b\left[1 + d\left(T - T_0\right)\right]}{F_{ava}}\right)^{\delta}\right] \tag{3.38}$$

where F_{ava} is the driving force and T_0=300 K.

3.3 Simulation Results

In this section, results obtained through TCAD simulations will be reported. First, static calibration of the structure will be proven. Afterwards, extended analysis on short-circuit behaviour and failure

mechanism will be presented. Finally, outcomes of unclamped inductive switching simulations will be shown.

3.3.1 Static Calibration

As explained before, the calibration phase is needed to have a virtual structure well resembling the operation of an actual device. Even though the structure was created and calibrated using data of a commercial device, it does not represent the structure of an actual device. Hence it could be taken as a more general case-study and the showed results could be considered to be broadly valid.

By trial and error, proper parameters for main adopted models were chosen, whose values are listed in Appendix B.

The result of the calibration is depicted in Figure 3.4 where simulated I_D-V_{GS} characteristics match the isothermal curves of a 1.2 *kV*, 36 *A*, 80 *mΩ* commercial device [39]. The curves were measured at V_{DS}=20 *V* by means of a pulsed curve tracer for backside temperatures of 300 *K* and 410 *K*.

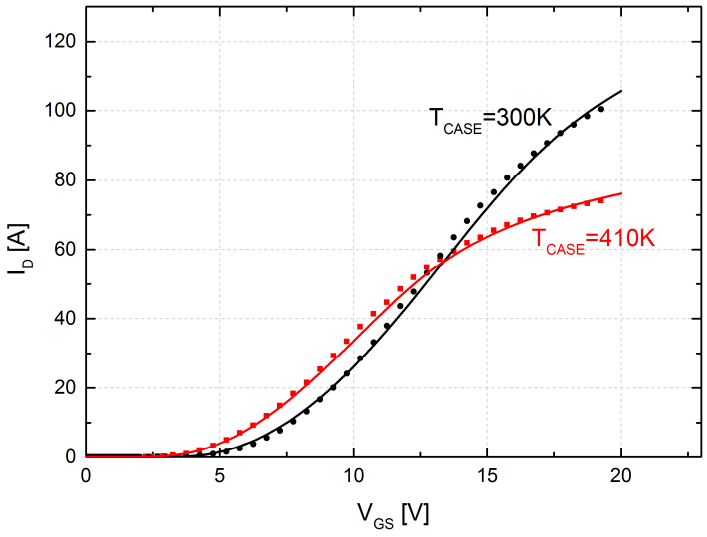


Figure 3.4: Measured (symbols) and simulated (solid) isothermal I_D-V_{GS} characteristics (V_{DS}=20V)

3.3.2 Short-circuit Simulations

Short-circuit mixed-mode simulations were performed, in which physically-based device was placed alongside a circuit description (in a SPICE netlist format) as depicted in Figure 3.5. Additional components were included to consider the parasitic elements introduced in a real circuit by wires and connections. Specifically, stray inductance and parasitic resistance on the source loop (L_S, R_S) create a negative feedback on the drain current and they affect the *di/dt* during turn-on phase; stray inductance on the drain (L_D) is responsible of voltage spikes during switching transients. It has to be pointed out that, just for simulation purposes, the reproduced structure has the body terminal physically separated from the source but they are connected at the same potential. In this way, it is possible to have full access to all electrical characteristics of device four terminals.

As described previously, temperature has significant impact on current transport phenomena and device operations. Hence temperature-dependent equations have been incorporated. The heat generation and transport equations were activated and consistently solved together with semiconductor equations (using the mentioned *thermodynamic* model). Boundary condition was imposed by fixing initial backside temperature value (T_{CASE}).

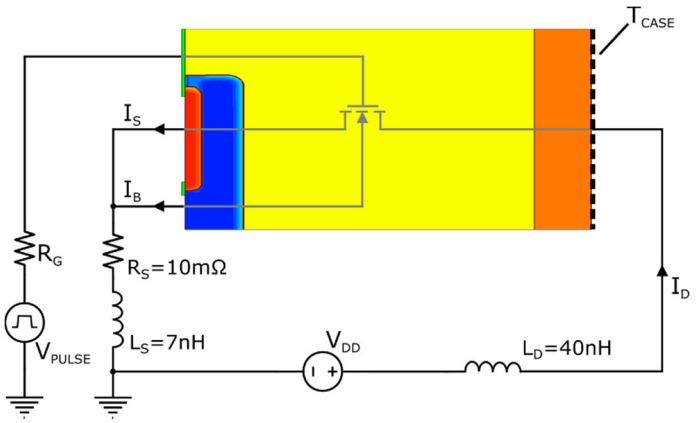


Figure 3.5: Mixed-mode simulated schematic

Figure 3.6 depicts the simulated drain current waveforms, along with average surface temperature, for different SC pulse durations (17 μs, 18 μs, 18.5 μs) and V_{DS}=400 V. The usual decrease of the current, due to the reduction of mobility, is reproduced in simulation.

The surface temperature reaches maximum value at the end of the SC pulse, and its peak is above 1000 K. Using 1D numerical simulations and compact model, other works [40]-[41] report values close to the one obtained.

Two more phenomena can be pointed out: the change of current slope at the end of pulse and the appearance of current tails originating after turn-off. These effects, demonstrated also experimentally in Chapter 4, are uncommon for a Power MOSFET. It can be noted that, when these effects start to be visible, there is an increasing hole current flowing out the body terminal, as reproduced in Figure 3.7. The appearance of hole current and its increase are dictated by the temperature rise, since as the pulse duration enlarges they become more evident. Investigation of physical data can better clarify the phenomenon. Figure 3.8 shows the temperature distribution at the end of a 18.5 μs pulse. The heat is mainly generated in the JFET region as it is the location where the product current density and electric field is higher, therefore the maximum temperature peak (of about 2000 K) is reached therein [42].

In the same area where the temperature is more localised, the Shockley-Read-Hall recombination distribution (Figure 3.9) has negative value, i.e. a certain amount of carrier is generated. This following interpretation of the dynamic occurring in the device can then be drawn.

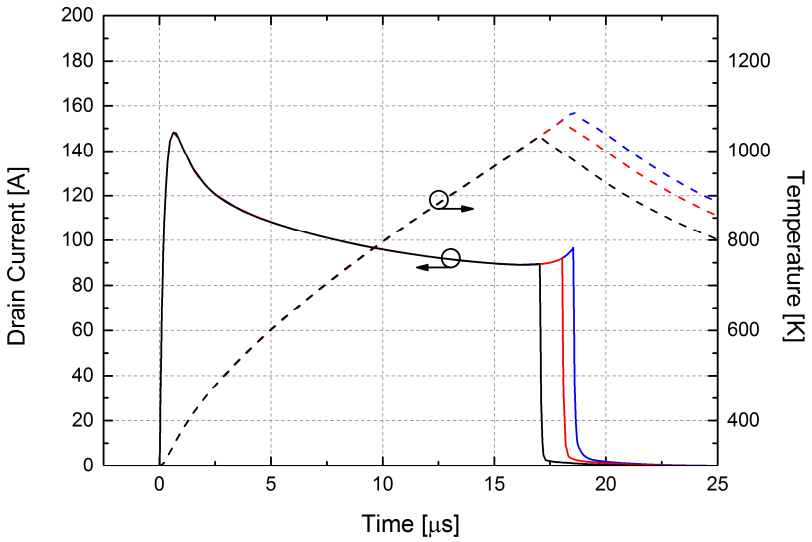


Figure 3.6: Simulated drain current and surface temperature (V_{DS}=400V; V_{GS}=18V; T_{CASE}=27°C)

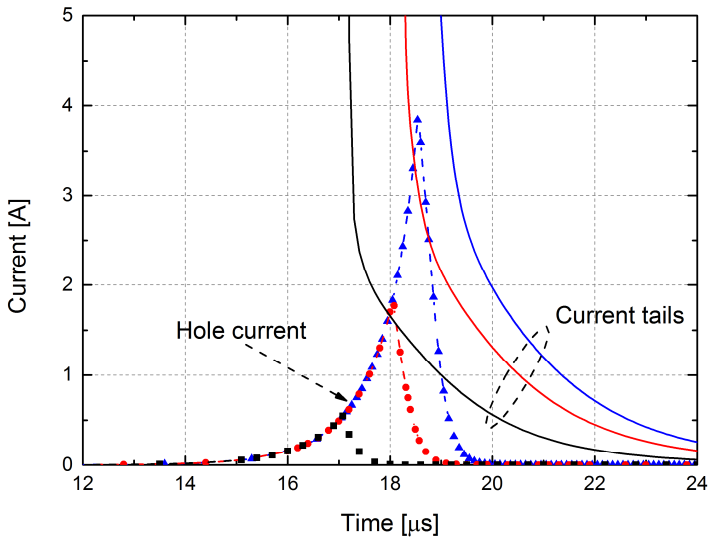


Figure 3.7: Detail of current tails (solid) and hole current (dashed)

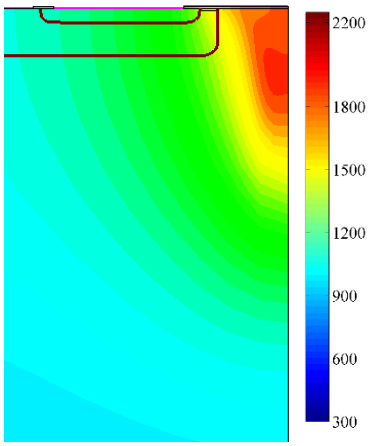


Figure 3.8: Temperature distribution at t=18.5µs
Peak value ~2000K
(V_{DS}=400V; V_{GS}=18V; T_{CASE}=27°C)

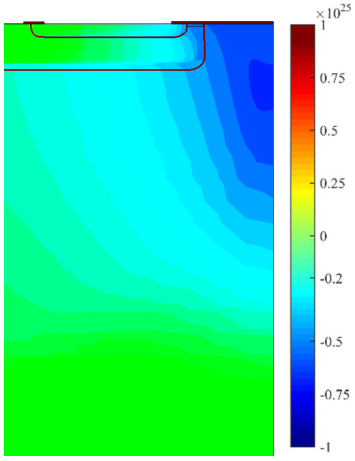


Figure 3.9: SRH recombination at t =18.5µs
Negative values correspond to carrier generation
(V_{DS}=400V; V_{GS}=18V; T_{CASE}=27°C)

Holes are thermally generated due to locally elevated temperature increase, and the electric field in the drift region drags the generated carriers toward the top of the device. They give rise to leakage current of the body/drift *pn* junction that flows out the body terminal. Figure 3.10 reports the hole current density in different time instants along the short-circuit pulse. In the beginning the hole concentration has very low value and therefore the leakage current is negligible. As the temperature grows, generation increments the hole level and consequently leakage current keeps on growing gradually and flowing through the body/drift junction. Obviously, electrons are thermally generated at the same time and are free to flow from source to drain even when the applied gate voltage is zero. The current tail is indeed built up by the merging of the aforementioned leakage currents. The tail then slowly decreases to zero within a time linked to the one needed to remove all the generated carriers. Nevertheless, if the temperature inside the device reaches a critical value, the leakage current could approach a level for that thermal runaway takes place leading to device failure. This is a positive feedback phenomenon inducing an uncontrollable increase of the drain current up to MOSFET catastrophic destruction, as can be seen from simulated waveforms of Figure 3.11.

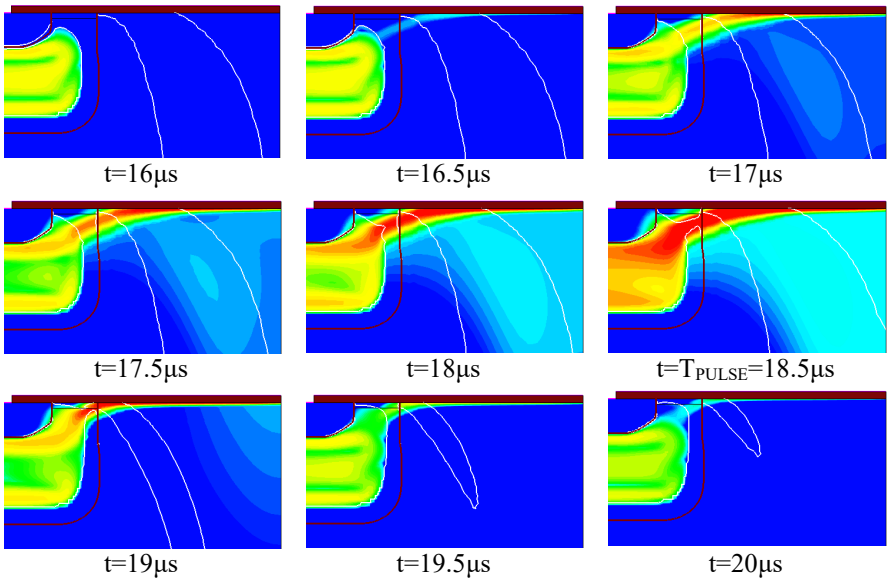


Figure 3.10: Simulated hole current density (V_{DS}=400V; V_{GS}=18V; T_{CASE}=27°C)

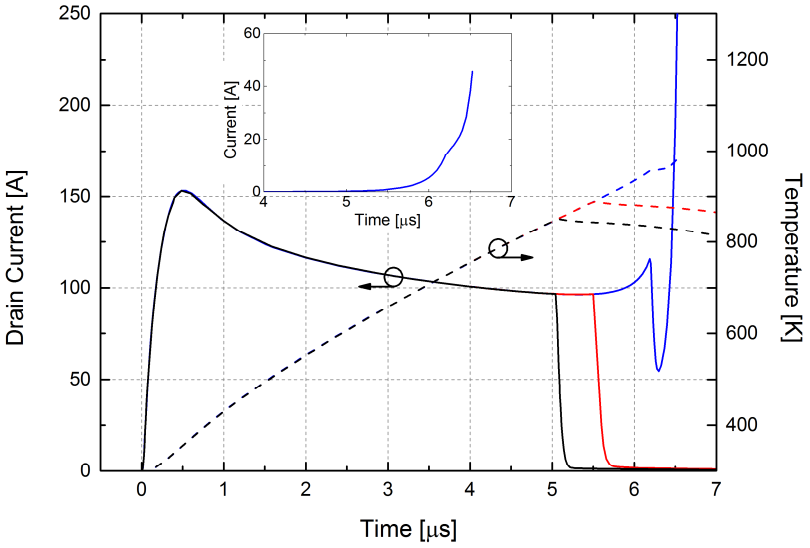


Figure 3.11: Simulated drain current and surface temperature.
The inset shows the body terminal hole current for T_{PUSLE}=18.5µs
(V_{DS}=800V; V_{GS}=18V; T_{CASE}=27°C)

Using basic formulas it is possible to carry out an approximate calculation of the leakage current as a function of temperature. Following [43]:

$$j_s = qn_i^2 \left(\frac{D_p}{L_p N_D} \right) \tag{3.39}$$

where D_P and L_P are the diffusivity and the diffusion length respectively, and n_i for SiC is given by [18]:

$$n_i = 1.7 \cdot 10^{16} T^{3/2} e^{-2.08 \cdot 10^4 / T} \tag{3.40}$$

D_P can be calculated from the mobility μ_n [18]:

$$\mu_n = 1140 \left(\frac{T}{300} \right)^{-2.7} \tag{3.41}$$

Combining (3.39)-(3.41) with the assumption of a device approximately $3\times3mm^2$ and with L_p=1-2 μm (from [18]) the leakage current can roughly be estimated to be ~50 A at T=2000 K, i.e. comparable to the ON-state current. On the other hand, if a lower temperature is considered the leakage current falls rapidly down, reaching values of tens of μA at T=1200 K. This very approximate calculation allows to have information on the actual temperature present inside the structure. Even though 2D simulations could not give accurate temperature results, since the thermal problem is not correctly solved, the actual device temperature could not be much far from the one obtained, otherwise the leakage current could never reach a value such critical to trigger the thermal runaway mechanism.

It has to be specified that thermal runaway, being a positive feedback process, makes the current be focalized in a limited area. A local increase of temperature induces an increase of the leakage current. Higher current, of course, entails a further temperature increment, thus building up a self-sustained mechanism. Therefore, almost all the short-circuit current tends to be crowded in a limited portion of the overall area when thermal runaway occurs. In an actual device, during ON-state the current spreads nearly uniformly all over the active area, but unavoidably there will be some portions with slightly higher current density than other. As an example, the current is moderately more condensed beneath and around the bonded wires, while outer areas present smaller density. Therefore, temperature distribution is uniform over a large area, with minor gradients defined by top device structure (pads, metallization, bond wires, etc.). Inside that area, a cluster of cells could be weaker due to inevitably differences created during manufacturing process, being prone to drain more current. Described situation was analysed in simulation, with the devices modelled by two parallel cells (*cell1* and *cell2*) as depicted in Figure 3.12 [44].

In *cell2* a mismatch in some structure parameters was introduced so that it could become “weak”. A cell can be considered weak if, for any reason, it carries even slightly more current than other cells, hence being more likely to give rise to thermal runaway. It is thus expected that the short-circuit failure current would flow entirely in *cell2* when thermal runaway sets on. Moreover, to model the current shrinking in a small fraction of the device, the ratio of the area factors of the two cells was chosen such that:

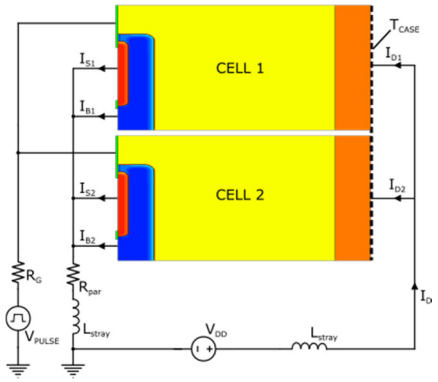


Figure 3.12: Diagram of mixed-mode simulated circuit.
Total device is modelled with two independent parallel cells

$$\begin{cases} AF_1 + AF_2 = AF_{TOT} \\ \dfrac{AF_1}{AF_2} = 10^4 \end{cases} \tag{3.42}$$

It means that *cell1* represents almost the total device active area, while *cell2* reproduces the modest cluster of cells where current might be focalized. For this analysis three main parameters have been selected: channel peak doping, channel length and interface traps density. They directly affect current conduction acting both on channel resistance and threshold voltage. Simulations have been repeated, applying the same conditions, changing each time one of the aforementioned parameters in *cell2*.

Figure 3.13 shows the current waveforms resulting from simulation with channel doping mismatch, as well as the drain current of a reference single-cell device. Peak doping concentration in this case has been decreased of fixed amount. It corresponds to a lowering of the threshold voltage, that is a higher current density. As the leakage current reaches a critical value, the short-circuit current moves from *cell1*, which safely turns off, to flow entirely in *cell2*, until the device fails. The described situation is represented in Figure 3.14 where current densities of both cells are illustrated. At the turn-off edge (Figure 3.14a), current density is divided equally between the two cells.

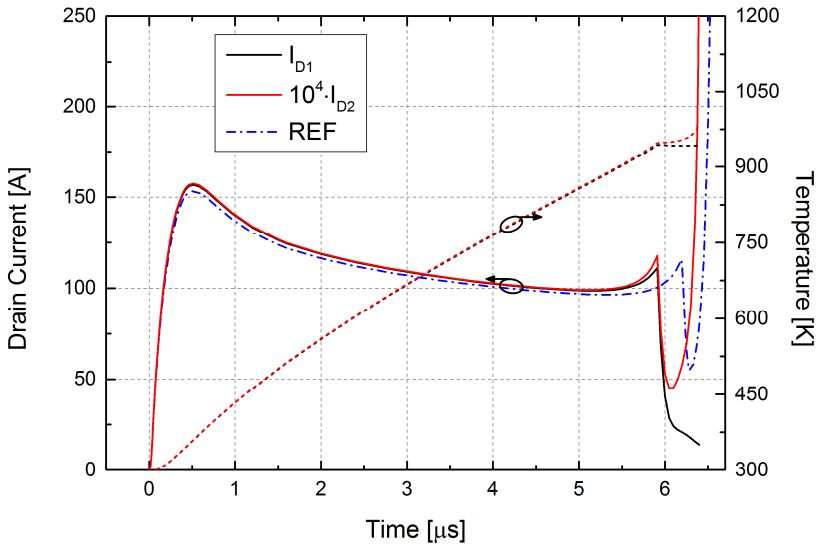
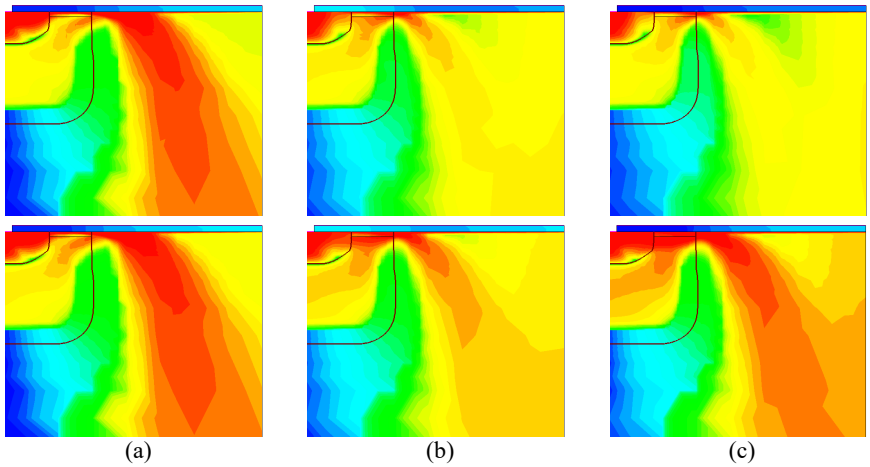


Figure 3.13: Simulated drain current and surface temperature – channel doping mismatch (V_{DS}=800V; V_{GS}=18V; T_{CASE}=27°C)



(a) (b) (c)

Figure 3.14: Current density of *cell1* (top images) and *cell2* (bottom images) – channel doping mismatch

Afterwards, *cell1* is in the decreasing phase of current tail, while *cell2* exhibits a higher current density (Figure 3.14b). Finally, the weak cell carries all the failure current (Figure 3.14c). It can be also noted that, as expected, the leakage current is partially formed by hole flowing through the body region. The reference cell is able to sustain about 280 *ns* longer SC pulse.

Same simulation has been repeated considering an inhomogeneity in channel length and then a different density of interface traps. Resulting waveforms are reported in Figure 3.15 and Figure 3.16. The reduction of the maximum sustainable short-circuit time is 300 *ns* and 315 *ns*, respectively.

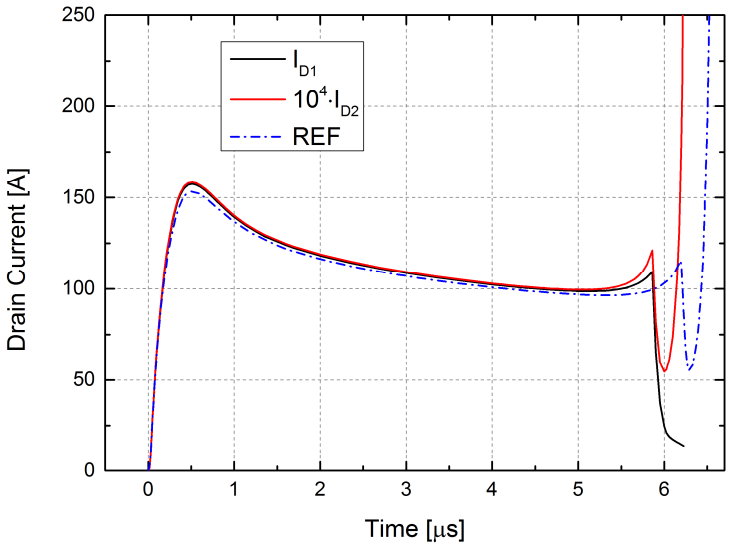


Figure 3.15: Simulated drain current – channel length mismatch (V_{DS}=800V; V_{GS}=18V; T_{CASE}=27°C)

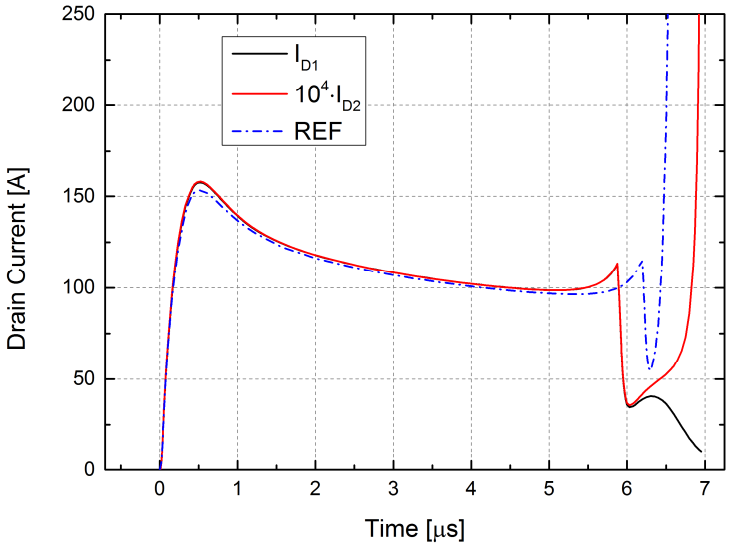
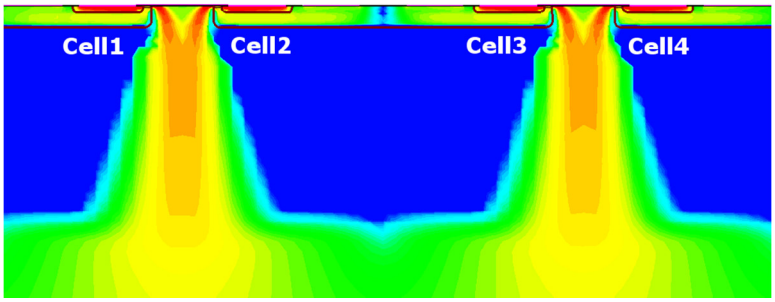
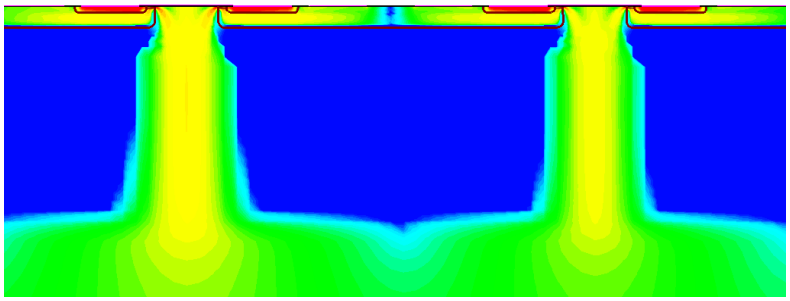


Figure 3.16: Simulated drain current – interface traps mismatch (V_{DS}=800V; V_{GS}=18V; T_{CASE}=27°C)

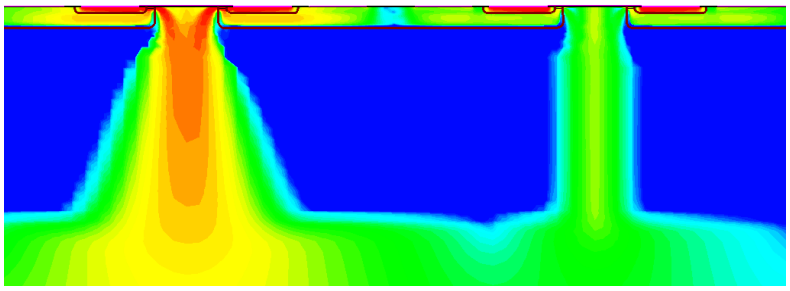
A further simulation was performed considering a structure formed by four cells, where one of the channel has the same doping mismatch of the previously showed case. The reason is to also include the interaction and the electro-thermal feedback of adjacent cells. Obviously, as the leakage current rises, the weak cell sinks the total device current. As expected, the effects of adjacent cells, exacerbate the formation of current filament leading to a greater reduction of SC capability compared to the case of independent cells. Current density and current waveforms are visible in Figure 3.17 and Figure 3.18.



(a) t=5.8µs

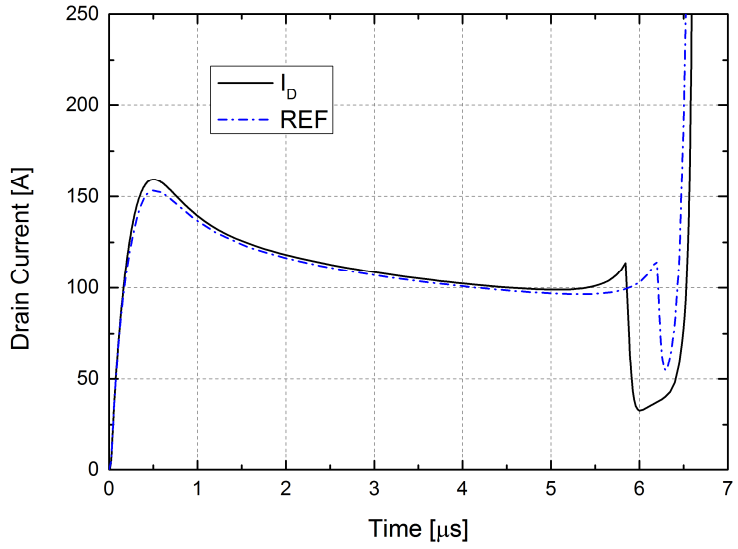


(b) t=6.1µs

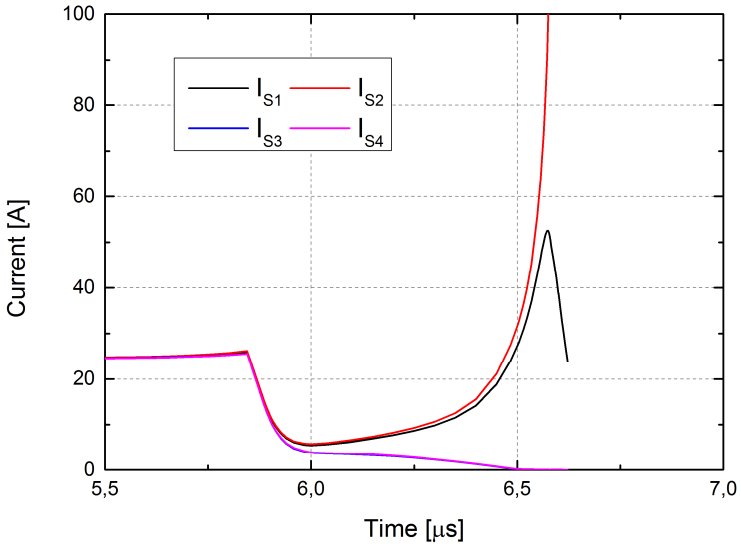


(c) t=6.8µs

Figure 3.17: Current density –
channel doping mismatch, four cells structure
(V_{DS}=800V; V_{GS}=18V; T_{CASE}=27°C)



(a)



(b)

Figure 3.18: Simulated drain current (a) and detail of cells current at turn-off (b) – channel doping mismatch, four cells structure (V_{DS}=800V; V_{GS}=18V; T_{CASE}=27°C)

Obtained results are summarised in Table 3.1, which reports the mismatch percentage together with the reduction of maximum sustainable short-circuit pulse Δt_{SC} (compared with the reference cell).

Introduced fluctuations on selected design parameters have such small values that they are likely unfeasible for current fabrication technology. As an example, channel peak doping variation is extremely dependent on technology process, but in this case, a barely 0.75% difference is enough to create a weak area reducing maximum time sustainable in short-circuit. This is especially true in the case of interface traps concentration considered. Traps density could vary within some orders of magnitude depending on the quality of fabrication process, but here a change of just 2.5% triggers the failure mechanism.

Process improvements are generally of paramount importance to develop devices with better and better performances, but an accurate investigation of some new design strategies should be taken into account to increase devices short-circuit reliability.

Parameter	Variation	Δt_{SC}
Channel Doping	0.75%	280ns
Channel Doping (four cells structure)	0.75%	345ns
Channel Length	1%	300ns
Interface Traps	2.5%	315ns

Table 3.1: Obtained results

3.3.3 Avalanche Simulations

Along with short-circuit capability, another important factor characterizing power devices robustness is their ability to withstand a certain amount of energy during avalanche operation. Maximum sustainable energy is linked to device structural parameters and it is strongly affected by electro-thermal effects within the device [45]-[46]. Impact ionization generation occurs when the electric field across a *pn* junction reaches a critical value E_{cr} and the voltage drop across the device at which this happens is called the *Breakdown Voltage* V_{BR} [47]. Avalanche breakdown phenomenon can accidentally occur during devices operations in a variety of industrial applications.

To fully analyse devices avalanche behaviour, the most important tool used is the *Unclamped Inductive Switching* (UIS) test [48]-[50]. The schematic diagram of the circuit used to perform this test is depicted in Figure 3.19a formed by a DUT with a load inductor *L* without any freewheeling diode (unclamped). The conceptual voltage and current waveforms associated with the device are illustrated in Figure 3.19b.

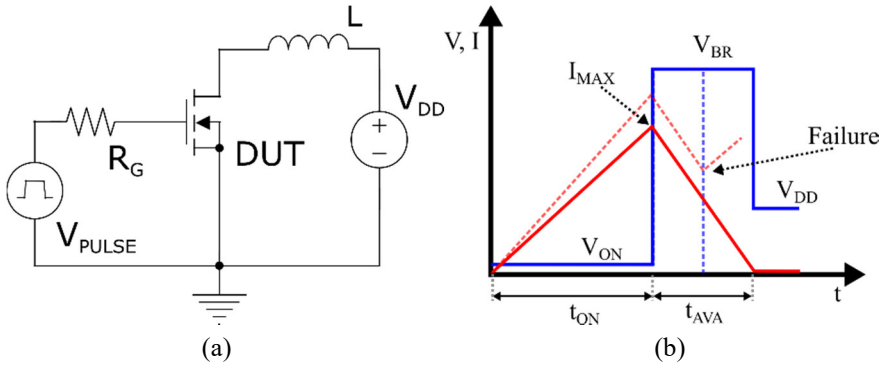


Figure 3.19: UIS test circuit (a) and schematic electrical waveforms (b)

During the time interval in which the active device is in ON-state (t_{ON}) a current flows into it with a linear slope given by:

$$\frac{di_D}{dt} = \frac{V_{DD}}{L} \tag{3.43}$$

The current reaches at the end of the pulse the maximum value I_{MAX}.

After the DUT is switched off, the current stored in the inductor (in the form of magnetic field) forces the device into breakdown condition. The current linearly decreases with slope:

$$\frac{di_D}{dt} = \frac{V_{BR} - V_{DD}}{L} \tag{3.44}$$

The DUT is forced to work in avalanche mode for a time:

$$t_{AVA} = \frac{I_{MAX} L}{V_{BR} - V_{DD}} \tag{3.45}$$

during which the device has to dissipate an energy equal to:

$$E_{AVA} = \frac{1}{2} L I_{MAX}^2 \frac{V_{BR}}{V_{BR} - V_{DD}} \tag{3.46}$$

The power dissipation during the t_{AVA} interval follows the current profile, i.e. is maximum at the beginning of the transient and zero at the end, while the junction temperature reaches its maximum somewhere during avalanche time. Because of the two peaks do not overlap, it is not possible to determine the instant of maximum stress and the exact shape of this curve in advance. However, the electro-thermal stress the device is subjected strongly depends on the inductor value. For small inductance the discharging time is fast leading to a high electrical stress while temperature does not reach critical values. On the other hand, when high inductance value is used, the time needed to dissipate all the energy is long, with subsequent critical rise of device temperature and associated high thermal stress.

The realised structure has been simulated during UIS transient to find out possible failure mechanism during avalanche. Parameters for Okuto-Crowell model have been modified to obtain V_{BR} similar to the actual breakdown voltage of the real device (~1800 *V*). A first result is reported in Figure 3.20 for an inductor value L=2.8 *mH* and a maximum drain current of I_{MAX}~19 *A*. From Figure 3.21 it is possible to note that, as expectable, the impact ionization occurs in the curvature of the body/drift junction, where the electric field reaches critical value. In addition, as for short-circuit operation, main heat generation and temperature increase is localised in the JFET region.

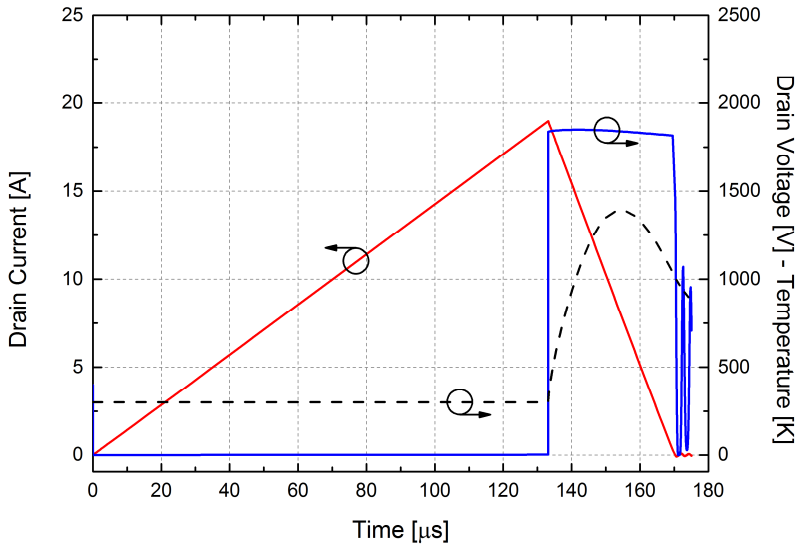
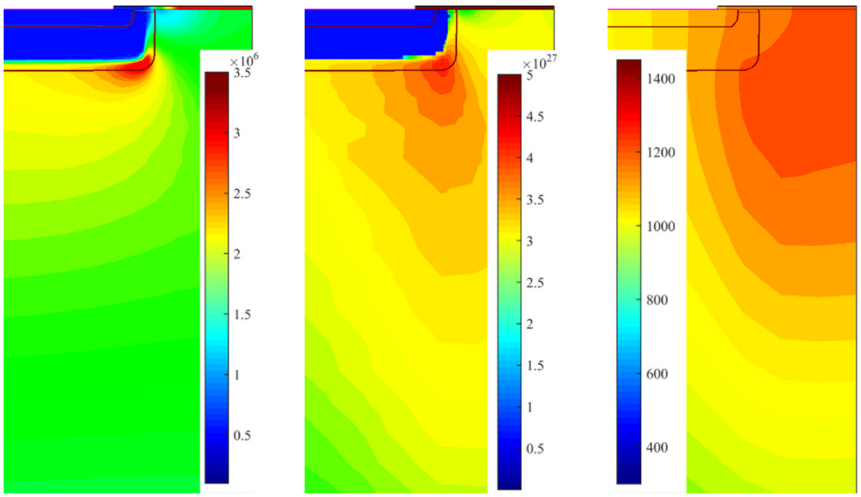


Figure 3.20: Simulated UIS I_D and V_D waveforms (solid) and T_{MAX} (dashed) (L=2.8mH; I_{MAX}~19A)



(a) (b) (c)

Figure 3.21: Distribution of electric field (a), impact ionization (b) and temperature (c)

The value of I_{MAX} was increased until the onset of the failure mechanism (I_{MAX}~27 A). It is possible to figure out that the failure is due to device latch-up subsequent to the activation of the parasitic *npn* transistor, as clearly visible from Figure 3.22. A parasitic bipolar transistor is distributed across source/body/drift regions. At the beginning of the breakdown phenomenon, the current density mainly flows through the corner of the body/drift region, corresponding to the location where avalanche occurs. However, as the temperature increases, the current starts to flow below the channel area until parasitic *npn* is activated and latch-up failure takes place. As the case of thermal runaway, latch-up is a self-sustaining mechanism that once triggered leads to device catastrophic destruction.

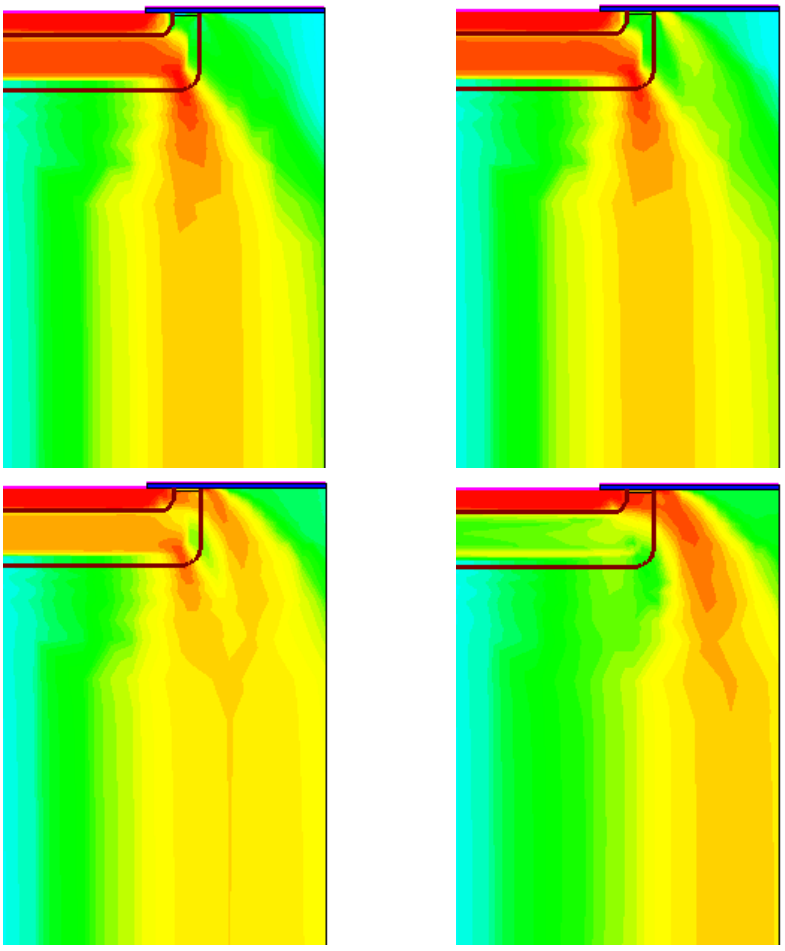


Figure 3.22: Current density distribution during a failed UIS test

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Chapter 4

Experimental Analysis

Complete information of power devices behaviour, cannot be obtained without extensive experimental characterization. It holds even more true if reliable data have to be gathered on operation in stressful conditions and on devices robustness.
Usually, manufacturers provide both static and switching performances specifications, along with limiting values for applied voltage, load current and dissipated power. Datasheets might even report values regarding the avalanche capability (in terms of maximum energy safely dissipated, E_{AS}) or the short-circuit capability (in terms of maximum short-circuit withstanding time, t_{SC}). Although these data are surely valid, they might not reflect the actual conditions a device could be subjected to. Moreover, robustness information are reported for just some particular applied conditions and are hardly exhaustive.

In order to acquire rigorous details on devices reliability broad set of experiments has to be performed, testing devices in different operation modes that enhance electro-thermal stress. Among all possible test, short-circuit (SC) test and unclamped inductive switching test (UIS) are most commonly used to get quantitative information on devices ruggedness.

This chapter is focused on showing outcomes for several tests during short-circuit. First, a brief description of the test itself and the adopted methodology will be shown. After that, the principal obtained results will be illustrated and commented, demonstrating that two separate failure phenomena might occur.

4.1 On the Short-circuit

Short-circuit condition occurs when an active semiconductor device (IGBTs, MOSFETs, etc.) is unintentionally subjected to the voltage of the main power source, mostly resulting from the occurrence of faults at the load end. As a consequence, the device current is only limited by its internal resistance, therefore the current flowing in the device itself could be several times the nominal rated current. It is an extremely critical condition a device could operate, and should be promptly removed to avoid device failure.

Short-circuit can happen while the device is normally working and it is usually divided in two main types [1]-[3]. In the first case the device is turned on when short circuit already exists with the full supply voltage V_{Supply} applied, usually indicated as *Hard Switching Fault* (HSF). The *di/dt* is dependent on the stray inductance and the current profile is defined by the temperature increase inside the device. The latter is referred as *Fault Under Load* (FUL) and corresponds to the occurrence of a SC event during conducting state, with the device carrying the load current I_{Load}. The voltage drop on the device is the on-state voltage V_{ON}, thus the elevated *dv/dt* induce a displacement current through the Miller capacitance that increases the gate voltage causing high short-circuit current peak. Typical SC waveforms are represented in Figure 4.1.

When a SC event occurs, different failure modes were identified depending on when the device fails during the short circuit [1], [4]-[6]:

- *Power limited*, usually occurring near the peak current shortly after turn on;
- *Energy limited*, occurring during the short-circuit pulse due to exceeding the maximum energy device can sustain;
- Failure during turn-off, linked to overvoltage and power surge caused by high *di/dt* when turning the device off, or to inhomogeneous operation;
- During the blocking state after the turn-off, caused by elevated leakage currents exceeding maximum power dissipation of the device.

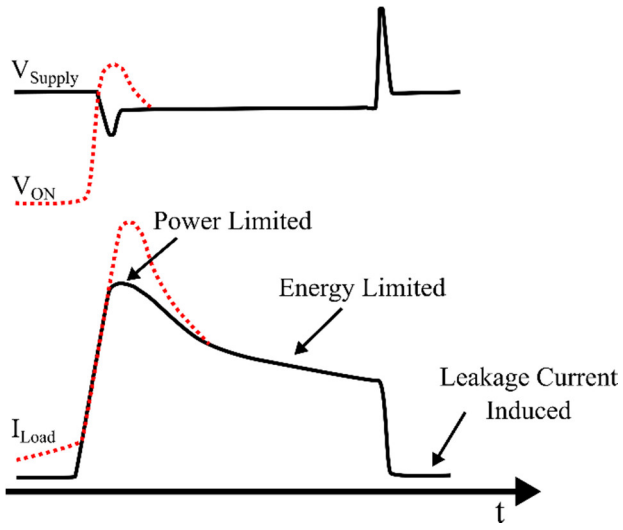


Figure 4.1: Typical short-circuit current and voltage waveforms
HSF (solid) – FUL (dashed)

The SC test is used to quantitatively evaluate the robustness of a power device in its conduction mode, extracting energy E_{SC} dissipated on the device itself with the expression:

$$E_{SC} = \int_{t_0}^{t_{PULSE}} v_{DS}(t) \cdot i_D(t)\,\mathrm{dt} \tag{4.1}$$

Short-circuit capability is an important figure of merit for a power device. SC events, even if are an undesired working condition, can occur in a variety of ways in an industrial environment, especially in motor driving systems. Hence, the ability of withstanding a number of abnormal conditions is a strong requirement for power devices. The conventional requirement for Silicon devices [7] is a short-circuit withstanding capability of 10 μs with 2/3 of maximum rated voltage applied.

Schematic representation of the test circuit for the short-circuit capability of power devices, used for this work, is shown in Figure 4.2. The gate driving system provides, through a gate resistor R_G, an adjustable voltage going from 0 V to 20 V. Voltage is applied on the

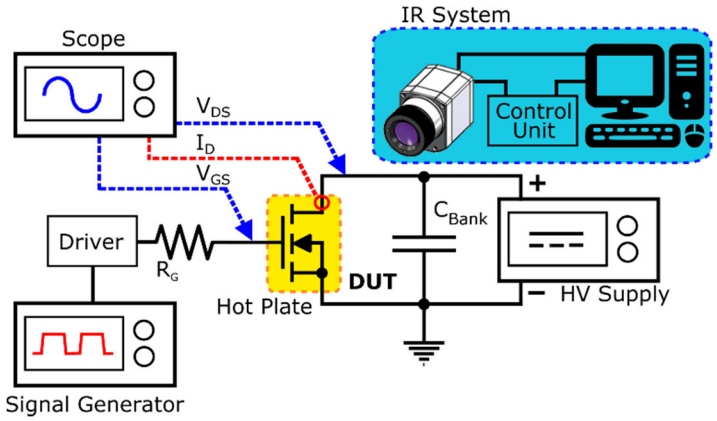


Figure 4.2: Test set-up diagram

device under test (DUT) by a HV DC power supply, and it is held during the SC pulse by a 1 *mF* capacitors bank. The DUT is placed on a hot plate through which it is possible to set the case temperature.

A custom advanced Infrared Thermography system [8] was used to acquire the surface temperature of the device, allowing thus thermal characterization of the DUT. The systems allows to track the temperature evolution, and therefore the current distribution, during the applied SC pulse. In addition, it is possible to acquire a single-shot capture of the temperature map in any desired time instant along the test. This feature was used, as it will be shown later, to catch the heat spreading at its maximum, i.e. at the pulse turn-off edge. Emissivity contrast has been compensated with a two-point calibration procedure [9]. It has to be specified that, due to high temperature reached during experiment exceeding the camera calibration range, thermal images were elaborated in post-processing to represent the normalized temperature increase:

$$T_n = \frac{T - T_0}{T_{\max} - T_0} \tag{4.2}$$

where T_0 is the case temperature and T_{max} the maximum temperature for each thermal maps.

Description of the IR system and some basic principles of Infrared Thermography are reported in Appendix A.

4.2 Experimental Results

In recent years, many works reported test results for SiC power devices. Evaluation of robustness and performances of commercial available devices was given in [10]-[13]. The reported results showed the weakness of the gate under short-circuit tests and different failure modes. Experiments on SiC Power MOSFET and JFET were carried out in [14] during SC fault condition. The device temperature was also estimated to be very high, leading to the melting point of Aluminium and finally to device failure. Wide experimental data on different commercial devices and numerical investigations through electrical and thermal coupled models were exploited to analyse the temperature dependence of SC withstanding capability in [15].

Several experiments were carried out on a 1.2 kV, 80 $m\Omega$ rated commercial device [16] taken as case-study. In order to have a widespread validation of the results, other manufactures' devices with same ratings were tested [17]-[18].

Single pulse short-circuit tests were performed, starting from low value of pulse duration t_{PULSE}, increasing it each step, and applying different operating conditions (i.e. V_{DS}, V_{GS}, T_{CASE}). The obtained results will then be used to understand device failures modes.

4.2.1 Behaviour for Short Pulse Duration

In the following, the most relevant results are summarized, for device subjected to high voltage ($\geq$400 V) and short duration ($\leq$20 μs) of SC pulses.

From Figure 4.3-Figure 4.5 two particular observations, already reported in [19], can be made: (i) there is a change in the current slope approaching the end of the pulse, (ii) after turn-off current tails appear. Generally, it is an uncommon behaviour for a Power MOSFET. As a unipolar device, it does not suffer from bipolar carrier accumulation in the drift region and it should not have any current tails. Moreover, it should have a negative current slope if no unstable behaviour is present. Results obtained in Chapter 3 allow to link the occurrence of the observed effects to the increase of the leakage current with temperature.

The same behaviour is spotted in other manufacturers' devices as well, as visible in Figure 4.6 and Figure 4.7. Proof of the temperature

dependence of the aforementioned effects can be also drawn from Figure 4.8 where current tails in function of T_{CASE} is reported.

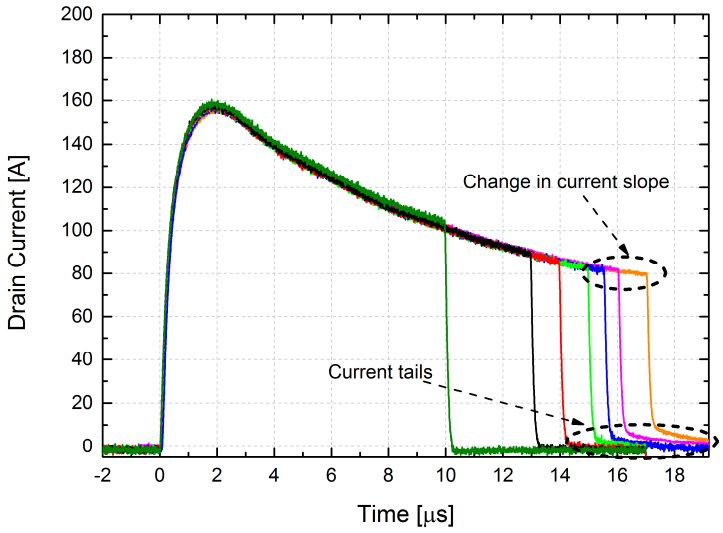


Figure 4.3: I_D short-circuit waveforms – C2M0080120D device (V_{DS}=400V; V_{GS}=18V; T_{CASE}=27°C)

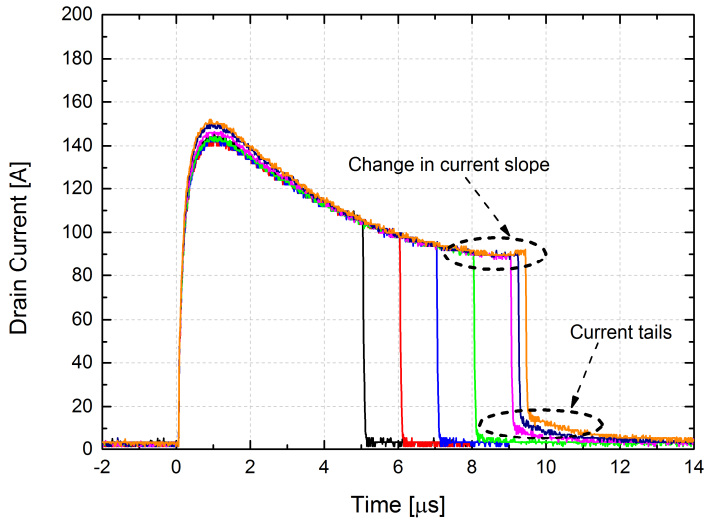


Figure 4.4: I_D short-circuit waveforms – C2M0080120D device (V_{DS}=600V; V_{GS}=16V; T_{CASE}=75°C)

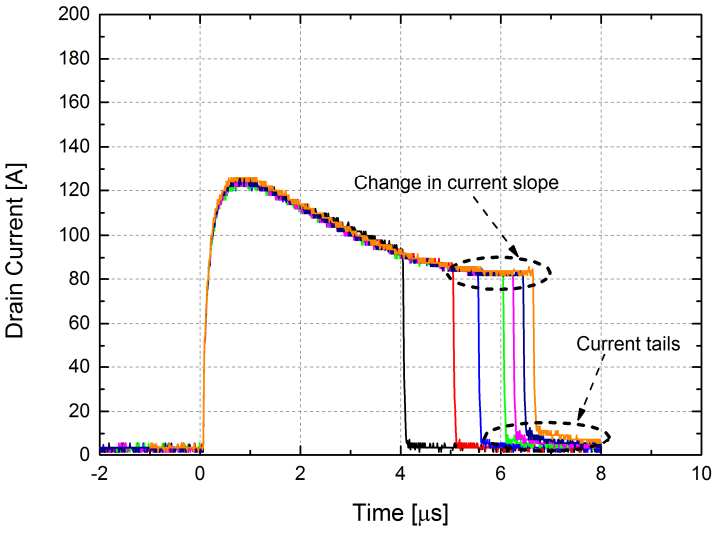


Figure 4.5: I_D short-circuit waveforms – C2M0080120D device (V_{DS}=800V; V_{GS}=18V; T_{CASE}=150°C)

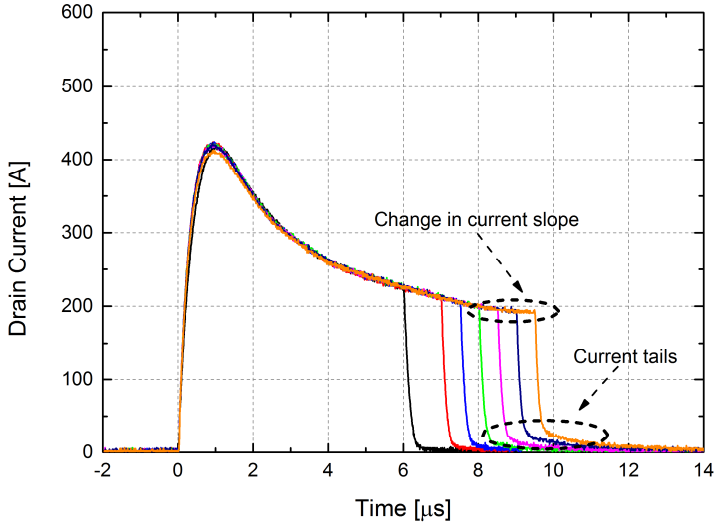


Figure 4.6: I_D short-circuit waveforms – SCT30N120 device (V_{DS}=400V; V_{GS}=20V; T_{CASE}=27°C)

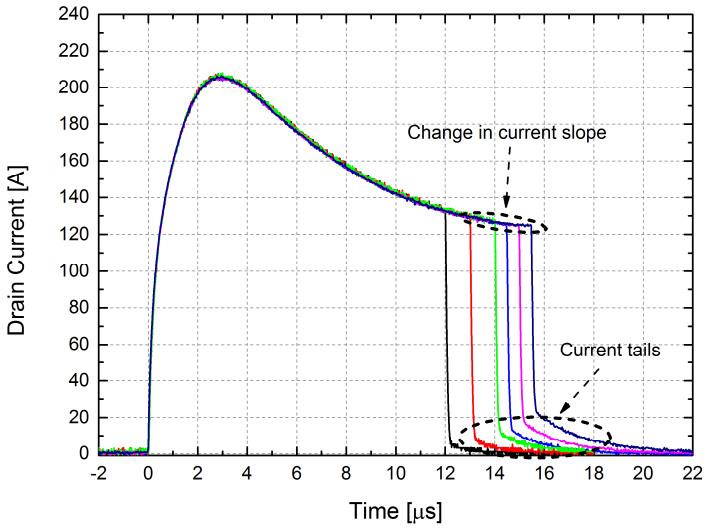


Figure 4.7: I_D short-circuit waveforms – SCT2080KE device (V_{DS}=400V; V_{GS}=20V; T_{CASE}=27°C)

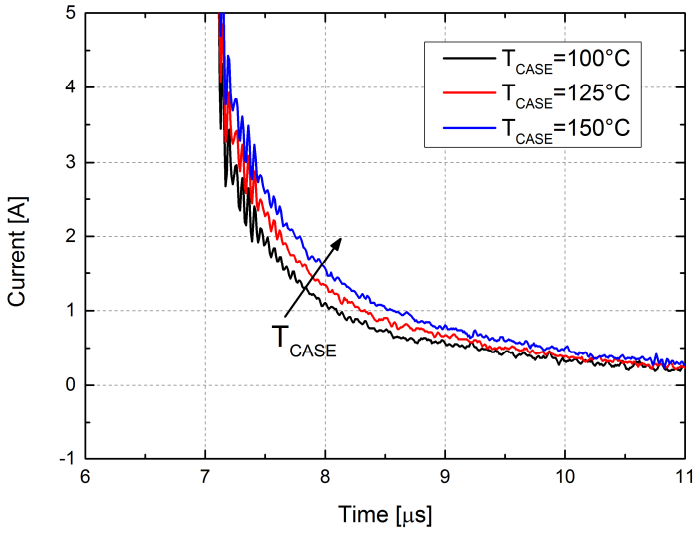


Figure 4.8: Current tails as a function of T_{CASE} – C2M0080120D device (V_{DS}=600V; V_{GS}=18V)

With the worsening of the conditions the device operates, the uncontrollable increase of the leakage current causes the triggering of the thermal runaway failure. Similar to already shown simulations results, the experimental current waveforms are depicted in Figure 4.9 - Figure 4.11. With eq. (4.1) it is possible to calculate the short-circuit energy leading to failure, reported in Table 4.1.

It is worth noting that the failure can occur during turn-off or even during current tail a certain time after turn-off. This is again another proof for the thermal runaway failure type linked to leakage current. Temperature reaches a peak at the end of the pulse and slowly decreases after turn-off. Nevertheless, current tail causes a local heating that finally brings to the onset of thermal runaway.

V_{DD} [V]	Device	t_{PULSE} [µs]	E_{SC} [J]
600	C2M0080120D	8	0.60
600	SCT30N120	4.5	0.79
800	C2M0080120D	5.5	0.54

Table 4.1: Short-circuit failure energy for experiments of Figure 4.9-Figure 4.11

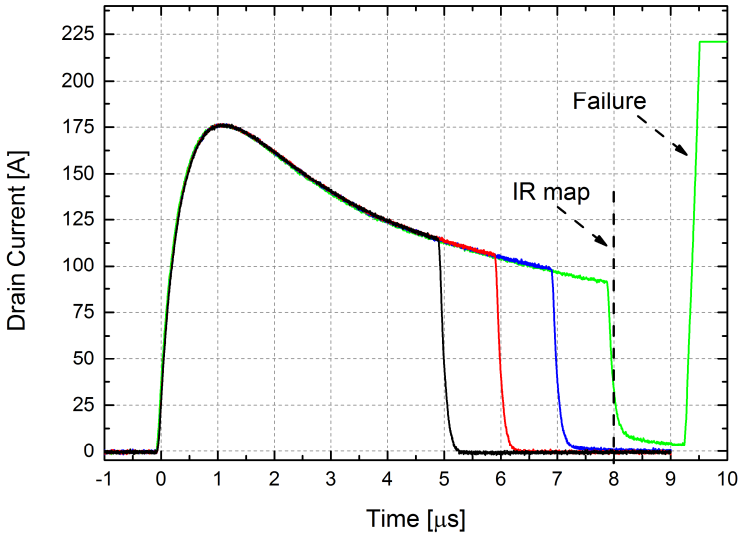


Figure 4.9: I_D short-circuit waveforms – C2M0080120D device (V_{DS}=600V; V_{GS}=18V; T_{CASE}=27°C)

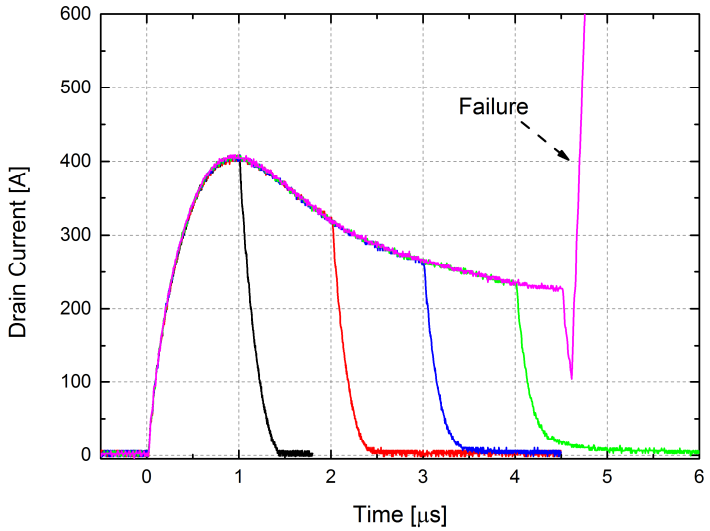


Figure 4.10: I_D short-circuit waveforms – SCT30N120 device (V_{DS}=600V; V_{GS}=20V; T_{CASE}=27°C)

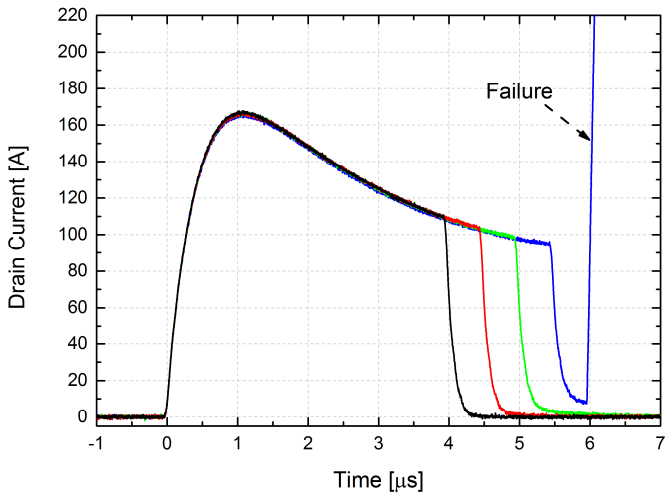


Figure 4.11: I_D short-circuit waveforms – C2M0080120D device (V_{DS}=800V; V_{GS}=18V; T_{CASE}=27°C)

To complete the experimental characterization, most relevant results obtained by means of the IR thermography system are reported in the following.

The first valuable outcome is illustrated in Figure 4.12 and it represents the thermal map for experimental waveforms of Figure 4.9 taken at the turn-off edge of an 8 μs pulse. It corresponds to the current

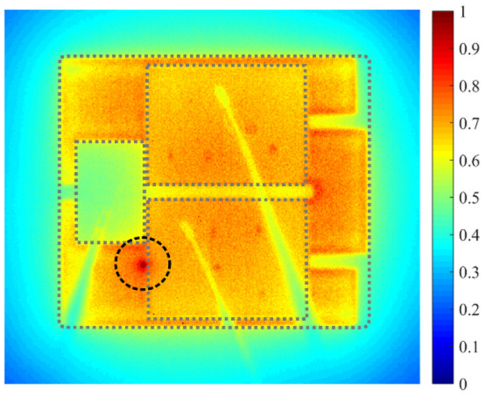
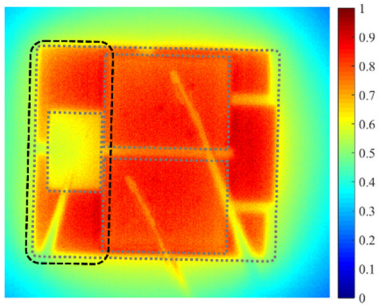


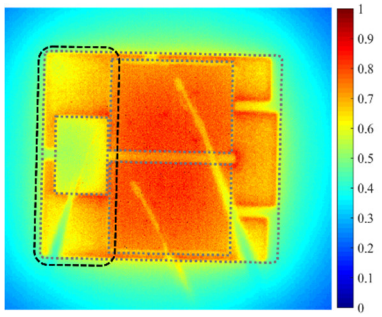
Figure 4.12: Normalized temperature increase at t=8µs for experiment of Figure 4.9

distribution at the turn-off, thus just before the failure event. It clearly reveals that the failure arises from an excessive high power density shrunk in an extremely confined area corresponding to the formation of a hot spot (encircled red dot in Figure 4.12). It was already explained that the appearance of hot spot is consequence of self-sustained mechanism entailed by thermal runaway.

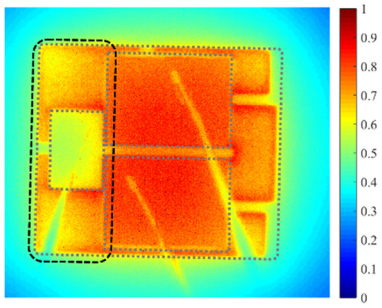
Another important result can be obtained by IR maps of Figure 4.13.



(a) t=10μs



(b) t=15μs



(c) t=17μs

Figure 4.13: Normalized temperature increase for experiment of Figure 4.3

They depict the temperature profile acquired at the end of different pulses for experimental waveforms of Figure 4.3. In those particular conditions, for which the power applied is lower, current tails still appear but the device experiences a different phenomenon. After a certain pulse length (17 μs for this case), the device does not turn on anymore. From inspection of the temperature distribution it is possible to spot areas on the device surface that are activated partially (encircled areas in figure). It is visible a transition from an almost uniform current spreading to a less homogeneous one. Since for a MOSFET without any unstable behaviour the current should expand on all active area, it could be assumed that those areas were subjected to a degradation process that reduced their ability to carry current, eventually making them inoperative. It could be supposed that the degradation affects the top metallization and/or passivation layers of the gate/source structure. As a matter of fact, a residual resistance of tens of ohms was measured between gate-source.

Same failure mode was found for a previous devices family [20] (1.2 kV, 160 $m\Omega$ rated) for similar conditions and illustrated in [21], whose results are recalled here:

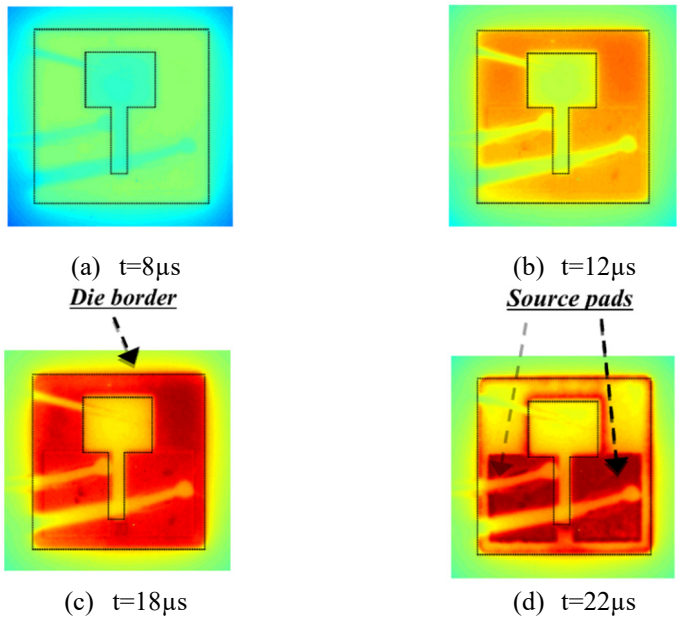


Figure 4.14: Normalized temperature increase
(V_{DS}=400V; V_{GS}=18V; T_{CASE}=27°C)

4.2.2 Behaviour for Long Pulse Duration

A type of experiment different from the one illustrated in the previous section has been carried out. Devices were subjected to short-circuit for long pulse width (100 μs) but with low applied voltage (<250 V). The reason is to slow down the temperature dynamic, and hence to analyse the device response to long thermal stress. The pulse length was kept constant and the voltage was increased in each step. Moreover, applying low voltage, that is applying low power, prevents the temperature to reach the critical runaway value.

Resulting waveforms are shown in Figure 4.15. When a certain voltage value is reached (175 V in this case), the device is not able to withstand the entire pulse duration and fails after approximately 85 μs, corresponding to the time instant in which the drain current drops to zero. In addition, at the same time, the gate-source voltage falls down to zero as well, and the gate current suddenly increases. It is then straightforward to assume that the device turned off because a short circuit had happened between gate and source terminals, indeed confirmed by following measure of R_{GS} (<1 Ω). It supports the speculation about the top gate/source materials degradation. No damage is involved between gate/source and drain as can be inferred from the V_{DS} waveforms of Figure 4.16.

Hence in this case the device experiences a totally different failure mechanism. It does not undergo to a catastrophic failure as for the thermal runaway mechanism, but simply it is not operative anymore because of damaging of the gate/source structure.

The observed damage to the top device surface can be still explained referring to simulation results. The heat generates inside the structure making temperature increase and it is able to spread inside the structure due to long pulse duration. Temperature can therefore reach values high enough to degrade the device, mostly melting aluminium layers [22].

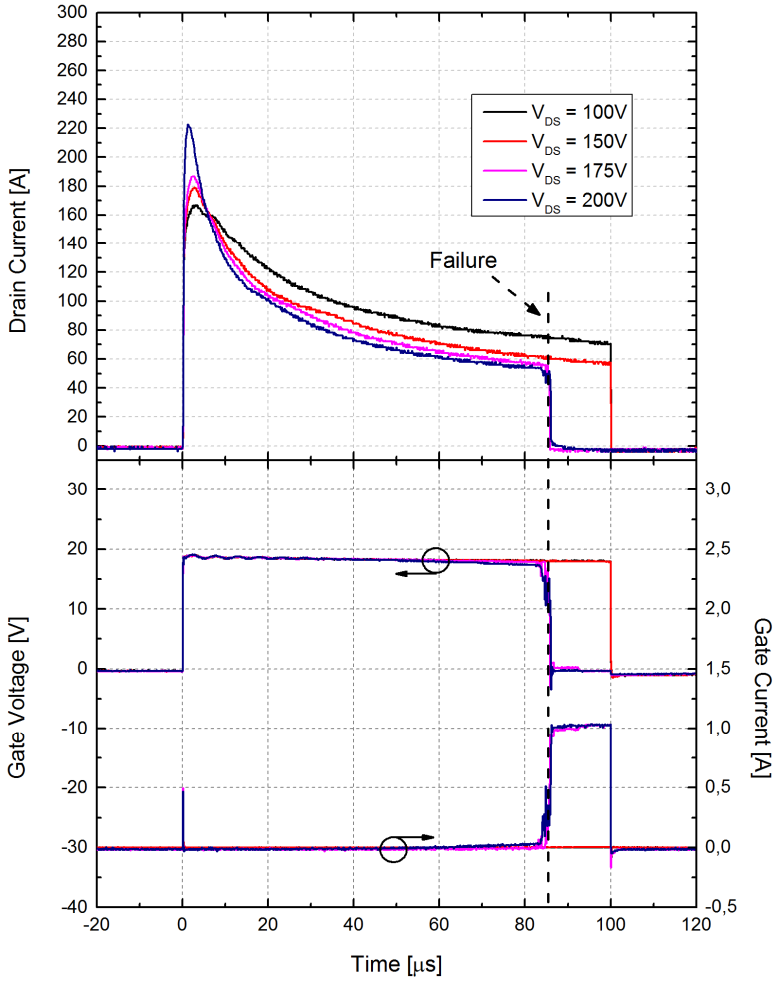


Figure 4.15: I_D,V_{GS}, I_G waveforms for 100µs pulse test

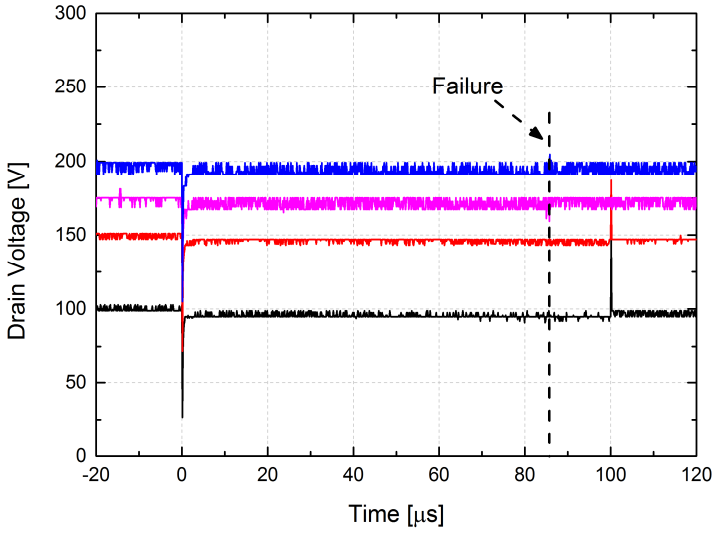


Figure 4.16: V_{DS} waveforms for 100µs pulse test

4.2.3 Unstable Behaviour

Silicon Power MOSFETs might present an unstable behaviour that drastically affects the device SOA and can lead to hot-spot formation with early device failure. It is a well-studied phenomenon [23]-[25] and it can be analytically modelled considering that instability arises when the following condition is met:

$$\frac{\partial P_G}{\partial T} > \frac{\partial P_D}{\partial T} \tag{4.3}$$

with P_G electrical generated power and P_D thermal dissipated power. It can be rewritten in the case of a MOSFET as:

$$\frac{\partial I_D}{\partial T} = \alpha_T > \frac{1}{V_{DS} Z_{TH}} \tag{4.4}$$

The temperature coefficient α_T for the drain current is dictated by the mobility and threshold voltage temperature behaviour [26].

The condition for the onset of thermal instability can then be expressed as:

$$S = \alpha_T Z_{th}(t) V_{DS} = 1 \tag{4.5}$$

This condition leads the temperature to diverge exponentially [27]:

$$\begin{cases} T_J(t) - T_0 = Z_{th}(t) V_{DS} I_D(t, T_J) \\ I_D(T) = I_D(T_0) + \alpha_T (T_J - T_0) \end{cases} \Rightarrow T_J(T) = T_0 + \frac{Z_{th}(t) V_{DS} I_D(T_0)}{1 - Z_{th}(t) V_{DS} \alpha_T} \tag{4.6}$$

Graphical representation of the thermal instability condition is depicted in Figure 4.17. As V_{DS} increases, the device approaches an unstable region within two boundary currents (I_1, I_2). If the current exceeds a certain value, the device could enter again in the stable area. Therefore, the value of the gate-source voltage influences the device operation; usually it can be defined a *temperature compensation point* (TCP) that discriminates between unstable (V_{GS}<TCP) and stable (V_{GS}>TCP) behaviour. This is a consequence of the dependence of the current on both the threshold voltage and the mobility [24]. The first induces a positive temperature coefficient with current increasing with temperature, while the second has the opposite effect. Which one is predominant defines MOSFET operation.

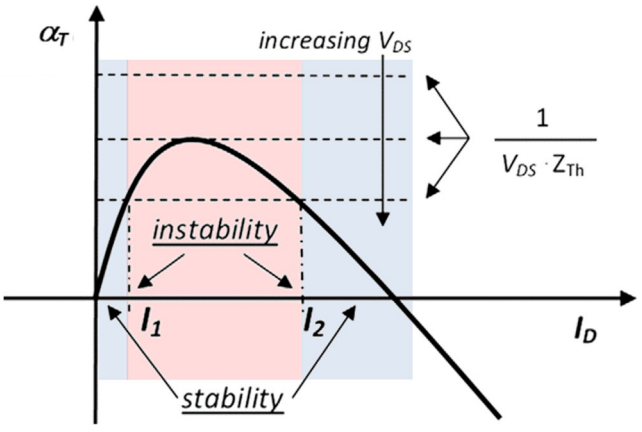


Figure 4.17: Stability graph for a power MOSFET

Experimentally investigation on the unstable mode of SiC Power MSOFETs have been carried out [28]-[29] showing that SiC devices could experience thermal instability as well.

Such behaviour can be inferred from current waveform (Figure 4.18) during a SC test. Properly biasing the device beneath the TCP, the current, exhibiting a positive temperature coefficient, increases constantly for all the pulse duration. The unstable regime can be also observed by inspection of temperature distribution along the SC pulse (Figure 4.19). As the electro-thermal effect becomes dominant, the drain current is confined in a small area with the formation of a stable hot spot.

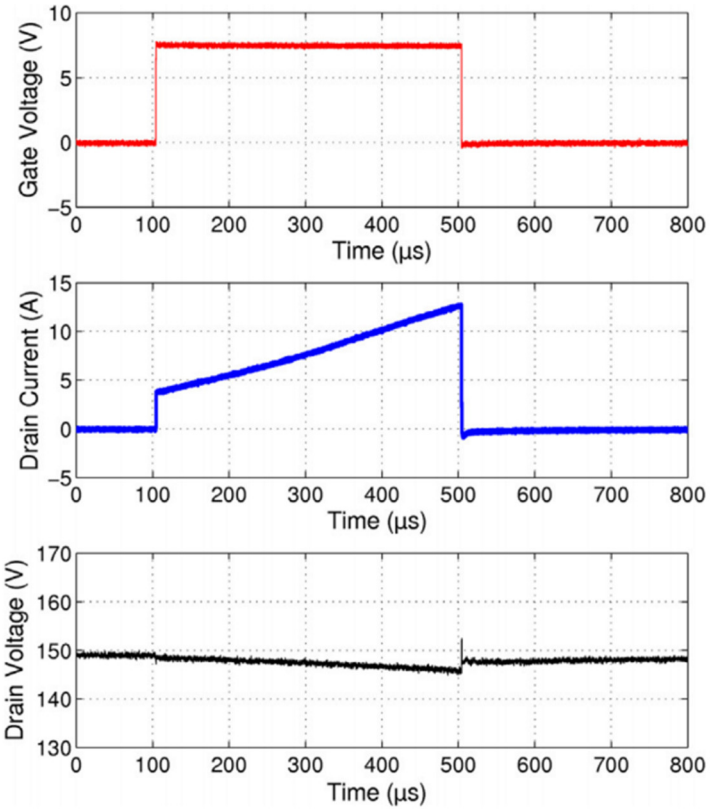
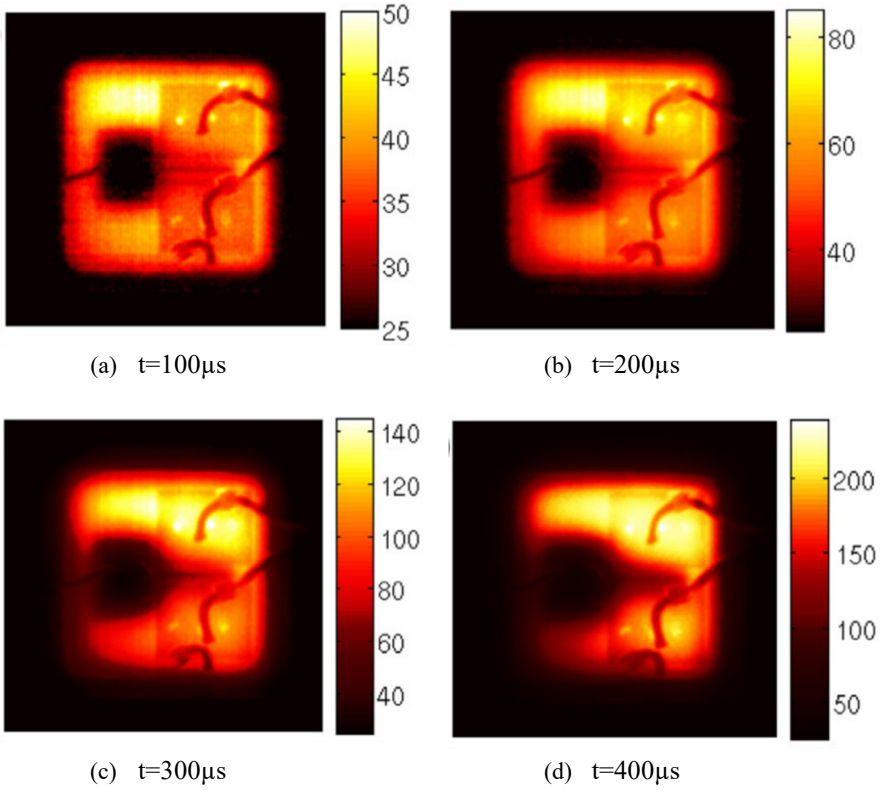


Figure 4.18: V_{GS}, I_D, V_{DS} waveforms during short-circuit unstable behaviour (V_{GS}=7.5V, V_{DS}=150V; t_{PULSE}=400µs)



(a) t=100µs (b) t=200µs

(c) t=300µs (d) t=400µs

Figure 4.19: Temperature distribution revealing unstable operation (scale in °C)

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Chapter 5

Results Discussion and Conclusion

Thanks to the results gained both with simulations and experimental investigations, it is possible to infer the underlying mechanism involved in SiC Power MOSFETs failure during short-circuit. Before going into detailed discussion of failure modes it is worth recalling the key points derived from analyses of Chapter 3 and Chapter 4.

TCAD simulations have allowed to observe the temperature distribution inside device structure during the SC pulse. It reaches extremely high value, with a peak confined in the JFET region. Moreover, thermally generated carriers can be associated to this temperature increase, which turn into an increment of the leakage current through the body/drift *pn* junction. Finally, if the leakage current reaches a critical value, it triggers the thermal runaway phenomenon.

Experimental outcomes showed that devices could either catastrophically fail or lose their ability to conduct current. In the first case, device experiences a destructive mechanism due to exponential rise of drain current subsequent to thermal runaway triggering. IR thermography investigations showed that the current focalises into a hot spot. On the other hand, the latter mechanism is considered to be caused by critical degradation of the top layers, resulting in a short circuit between gate and source terminals with subsequent inability of turning the device on.

Therefore, it is clear that two separate phenomena might happen when a device fails. It is convenient to indicate them as *failure mode I* and *failure mode II*. Both are regulated by the temperature increase inside the device, and more precisely by its growth rate. Since both failures are set on by temperature it is useful to define two different values:

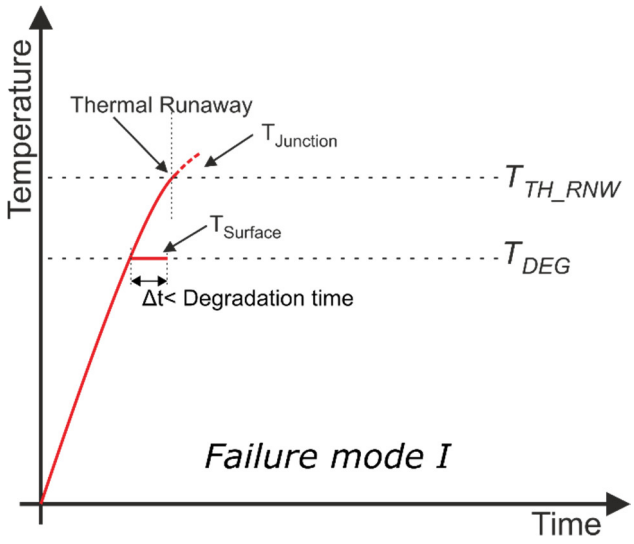
- T_{DEG}, when surface degradation occurs
- T_{TH_RNW}, when thermal runaway takes place

The value for which top materials get corrupted is related to the temperature at which melting or changing in properties happens to passivation and metallization layers, and it is obviously lower than the critical value needed to trigger on the thermal runaway. The graphical interpretation of the two mechanisms is illustrated in Figure 5.1.

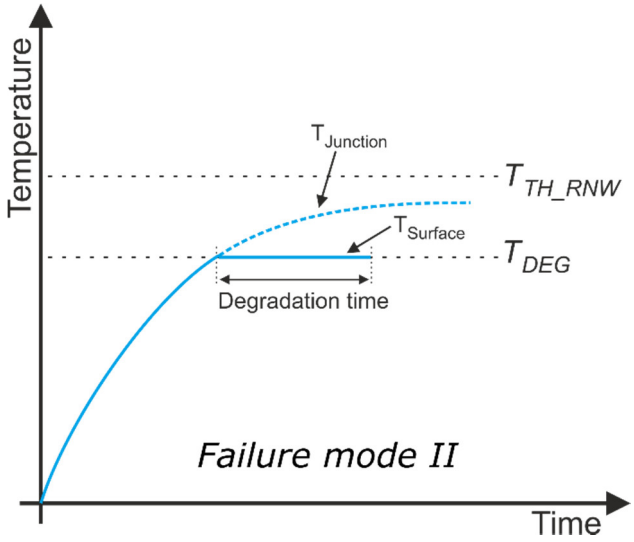
Temperature rise is, of course, related to the amount of power that device is subjected to, and therefore to the applied voltage. High applied power generates elevated heat in the device, which turns into a prompt temperature increase (as in the case of experiments at 600 V and 800 V in §4.2.1). Temperature suddenly reaches T_{TH_RNW}, a huge amount of carriers is then generated and the leakage current goes up to a value for which thermal runaway is activated (Figure 5.1a). Drain current rises uncontrollably and device blows up (*failure mode I*). Due to device blowing up, this failure type can be considered as "hard" failure. In this case, even though temperature is greater than T_{DEG}, the time device is subjected to this value is not enough for the surface to be fully damaged.

On the other hand, when the power applied is low (as in the case of experiments in §4.2.2), the amount of generated heat is moderate, temperature has a slow dynamic and might reach T_{DEG}, but could not arrive up to T_{TH_RNW} (Figure 5.1b). If the device surface is exposed to T_{DEG} for enough time, permanent damage occurs (*failure mode II*). The gate/source structure is permanently compromised and therefore the device loses partially or totally its ability to conduct current. This mechanism can be considered as a "soft" failure.

In all other conditions, for moderate applied power, the failure is regulated by the time needed to degrade the device and the one needed to reach the thermal runaway point (Figure 5.2). When the former is higher, even if the temperature has a value able to produce detrimental degradation, thermal runaway is the predominant mechanism.



(a)



(b)

Figure 5.1: Interpretation of two failure modes hard failure (a) and soft failure (b)

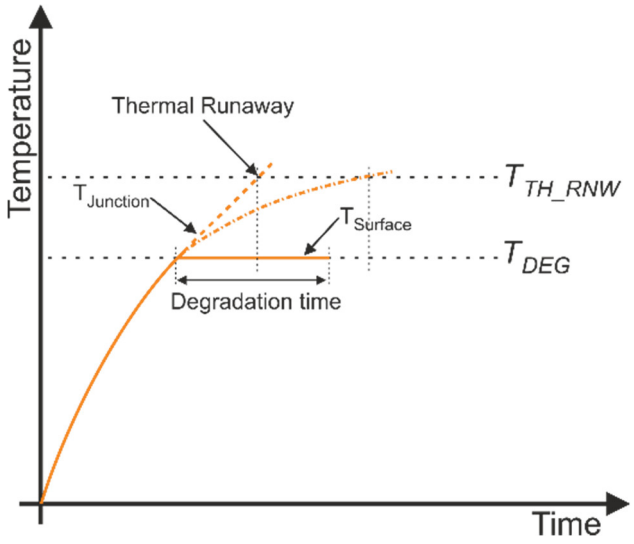


Figure 5.2: Failure for general applied power.
The smallest between degradation time and the time to trigger thermal runaway determines which failure might occur

Therefore, in this dissertation a comprehensive analysis of short-circuit failure mechanisms for Silicon Carbide Power MOSFETs has been given. The issue has been addressed by means of experimental approach in order to observe actual devices behaviour, and using a TCAD simulator to deeply investigate physical mechanisms evolution. *Separate failure modes has been observed and theoretically explained, identifying in the temperature the most limiting factor for SiC Power MOSFETs short-circuit capability*. Even though one of the most marked properties of Silicon Carbide is the material elevated thermal conductivity, SiC devices have usually reduced volume compared to same rated Silicon ones. Consequently, it results in extremely high temperature increase, which drastically reduces devices short-circuit ruggedness.

Moreover, numerical simulations have been used to analyse the unavoidably variations of design parameters on the creation of weak areas in the device. It has been shown that even very small mismatch are enough to make a portion of the device prone to carry more current, thus being more likely to give rise to the thermal runaway positive effect.

Finally, simulation during breakdown operation has demonstrated that avalanche robustness of these devices is limited by latch-up phenomenon due to triggering of parasitic *npn* BJT.

Appendix A

Infrared Thermal Characterization of Power Devices

Power semiconductor devices could be fully characterized if, along with electrical data, surface temperature distribution is known, so that information about possible unusual working conditions could be gathered. This task could be easily achieved by means of Infrared (IR) Thermography [1]. Many attractive features make it a preferable choice, among other contactless techniques, for quantitative thermal measurements. Thanks to commercial availability and increasing performances of IR cameras, that completely replaced single IR sensor systems [2], [3], it has begun a powerful investigation method in a variety of research fields [4].

When a semiconductor device operates, it suffers of a self-heating mechanism due to the Joule's effect, leading to temperature increase. Therefore, detecting the heat generated by device under test (DUT) and evaluating the temperature map is a useful method to observe the current distribution within an electron device. This information could be used for functional testing [5], robustness evaluation of power devices [6] or to analyse unusual working conditions, such as hotspots or non-uniform current distribution [7]. IR cameras are equipped with high performance bi-dimensional sensors array (Focal Plane Array, FPA) that allows capturing in one shot the whole device area. Nevertheless, the main limit of camera-based systems is the high time the readout circuit needs to process the signals coming from the sensors array. This time affects the maximum camera real time sampling frequency, nowadays usually limited at some hundreds of *Hz*, for a 640×512 pixels FPA size.

In this section, an experimental set-up for IR thermal characterization of power semiconductor devices is described.

A.1 Thermal Radiation Principles

The whole electromagnetic spectrum could be divided into sections based on wavelength. Infrared radiation covers a portion from approximately 0.9–14 μm and usually the range involved in thermography study lies in the 1–10 μm range (referred as thermal infrared). All objects at temperatures above absolute zero emit IR radiation, which is converted by IR cameras to a visual image displaying temperature variations across an object.

Radiation emitted by a blackbody is described by Plank's law:

$$W_{\lambda b}(\lambda, \mathrm{T}) = \frac{2\pi hc^3}{\lambda^5 \left(e^{hc/\lambda kT} - 1\right)} \cdot 10^{-6} \left[\frac{W}{m^2 \mu m}\right] \tag{A.1}$$

where $W_{\lambda b}$ is the spectral radiance, T is the absolute temperature, h is the Plank's constant, k is the Boltzmann's constant, c is the speed of light and λ is the wavelength (μm).

The total radiated energy of a blackbody can be calculated by integration of (A.1), obtaining the Stefan-Boltzmann law:

$$W_b = \sigma T^4 \left[\frac{W}{m^2}\right] \tag{A.2}$$

σ=5.67·10^{-8} W/m^2K^4 is the Stefan-Boltzmann's constant. According to this law, the total emitted power of a blackbody is proportional to the fourth power of its absolute temperature. Most of real objects are not ideal blackbodies, and they react differently to incident radiation from their surroundings. Thus, other processes have to be taken into account: a fraction of the incident radiation α might be absorbed, a portion ρ might be reflected and a quantity τ might be transmitted. All these factors (called respectively absorption, reflection and transmission coefficient) are wavelength dependent and their sum must always equal to one:

$$\alpha_\lambda + \rho_\lambda + \tau_\lambda = 1 \tag{A.3}$$

Moreover, energy radiated by objects is usually described in relation to a perfect blackbody. It is then introduced a factor, called the emissivity coefficient ε, defined as the ratio of the spectral radiant power of an object to the spectral radiant power of a blackbody, at same temperature and wavelength. Analytically, it can be expressed as follows:

$$\varepsilon = \frac{W_{\lambda o}}{W_{\lambda b}} \tag{A.4}$$

If the emissivity is constant for all wavelengths, an object is called greybody and the Stefan-Boltzmann's expression takes the form:

$$W_b = \varepsilon \sigma T^4 \left[\frac{W}{m^2} \right] \tag{A.5}$$

Beside the given basic theoretical concepts, a detailed description of infrared thermography can be found in specialized literature (e.g. [8], [9]).

A.2 IR Thermography System

This section presents a camera-based IR thermography system, developed for monitoring temperature distribution of semiconductor devices [10]. Thermal dynamic of electron devices usually experiences fast transient evolutions, below the milliseconds scale. This holds especially true for SiC devices that could undergo a large temperature rise in tens of microseconds, or even less. As said before, IR cameras are limited by frame rates inadequate to monitor the fast heating/cooling processes power devices could present, especially when they are subjected to stressful conditions (e.g. short-circuit). The best possible approach to overcome this constraint is to use the equivalent time sampling technique, successfully adopted for the first time in [11]. The only requirement to apply this method is that the phenomenon to be observed has to be repeatable.

The equivalent time sampling method is widely used every time the signal to acquire is faster than the sampling rate. As said, the signal has to be periodic. It means that, as an example, if the temperature evolution

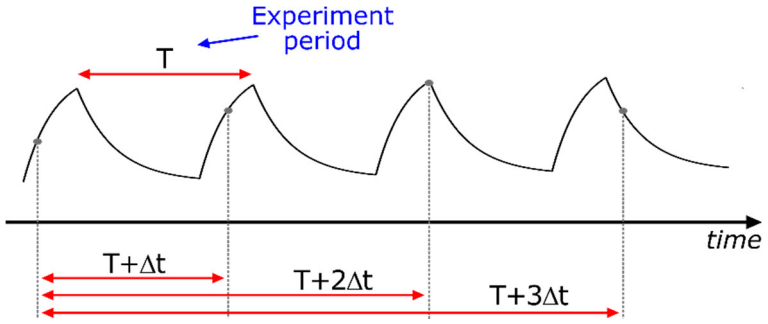


Figure A.1: Representation of the equivalent time sampling technique

of a power MOSFET during short-circuit has to be analysed, then multiple SC pulses have to be sent. The repetition time has to be chosen long enough to make the device cool down and assure the same initial condition. Taking advantage of the introduced periodicity it is possible to reconstruct the signal using a certain number of samples taken in different consecutive periods, shifting the acquisition instant by a fixed time Δt each period (Figure A.1). In this way, very high equivalent sampling frequency can be obtained. The minimum delay between two consecutive sampling instants is imposed by the minimum settable camera integration time, which means that the maximum equivalent frame rate potentially achievable is given by:

$$f_{eq\_\max} = \frac{1}{IT_{\min}} \tag{A.6}$$

The implemented system is based on a SC7650 IR camera produced by FLIR Systems. It is equipped with a cooled *InSb* FPA of 640×512 pixels. The pixel pitch is 15 μm and the maximum real time frame-rate is limited to 100 *Hz* in full-frame acquisition mode. The sensor spectral response is in the 1.5–5.1 μm range with a minimum temperature resolution of 25 *mK*, while the integration time (IT) can be set between 1 μs and 20 *ms*. Given the minimum settable integration time, the maximum equivalent sampling frequency potentially achievable is 1 *MHz*.

Figure A.2 depicts a schematic view of the experimental set-up, where the IR camera along with connections between different parts of the system are shown. Timing of all signals is of crucial importance to

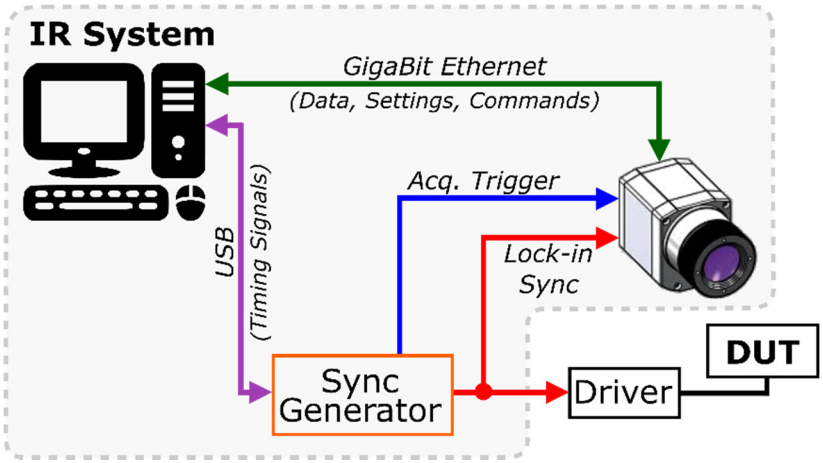


Figure A.2: Diagram of the experimental IR system

implement correctly the equivalent time method. An experiment has to be repeat *n* times with a fix period. The number of times *n* simply equals the number of frames desired to reconstruct the temperature profile during the experiment.

A stable time base and a perfect synchronization of the experiment with the acquiring instants are needed. The IR camera communicates through Gigabit Ethernet with a computer. Two Agilent waveform generators provide trigger signals for the IR camera and the DUT driving circuit. They are synchronized with externally generated trigger in order to assure the same time base. All the instruments are controlled via MATLAB® through a Graphical User Interface (GUI) where all the parameters of the experiment are fully settable by the user. The frames acquired during the experiment are shown in real time and they are stored in memory for the post-processing stage. Moreover, the used IR camera has a dedicated trigger-in connector. This is a key point to implement the equivalent time technique, but also allows to fire a thermal map acquisition at a desired time instant along the experiment. It might be useful, for instance, to get the temperature distribution exactly when the device fails.

Thermal images are usually affected by the emissivity contrast. Top device materials present different values for emissivity coefficient, i.e. different infrared emission properties. In order to extract quantitative information on the temperature distribution, there is the need to evaluate

the emissivity map calibrate the acquired images. This could be achieved using the "two-point calibration" method [5], [12]. To this purpose, the device has to be heated up at two temperature T_1 and T_2, and extracting the emissivity as:

$$\varepsilon(x,y) = \frac{S_{T_2} - S_{T_1}}{T_2 - T_1} \tag{A.7}$$

where $S_{T_{1,2}}$ are the IR radiance read by camera and $T_{1,2}$ the two chosen temperatures. This process should be repeated for different temperature range to obtain better accuracy.

The main system features are summarised in Table A.1.

Parameter	Value
Camera Detector Material	InSb
Number of Pixels	640×512
Spectral Response	1.5–5.1µm
f_{MAX} **(real time)**	100Hz
f_{EQ_MAX} **(equivalent time)**	1MHz
Pixel Pitch	15µm×15µm
NETD	<25mK @ 25°C
Integration Time	1µs–20ms
Calibrated Temp. Range	10–350°C
Trigger Jitter	~220ns

Table A.1: System parameters

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Appendix B

Models Parameters

Parameters values for the main physical models used for TCAD simulations are reported here. Some default values for 4H-SiC included in the simulator were modified to obtain the desired fitting with I_D-V_{GS} characteristics of a commercial device, as already explained in Chapter 3.

ARORA MOBILITY MODEL PARAMETERS		
	ELECTRONS	HOLES
A_{min} [cm^2/Vs]	22.83	0
α_m	-0.536	-0.57
A_d [cm^2/Vs]	53.92	113.5
α_d	-2.2	-2.6
A_N [cm^{-3}]	$2 \cdot 10^{17}$	$2.4 \cdot 10^{18}$
α_N	0.72	2.9
A_a	0.76	0.69
α_a	0.722	-0.2

Table B.1: Arora mobility model parameters

INTERFACE DEFECTS PARAMETERS	
Q_F $[cm^{-2}]$	$2.68 \cdot 10^{12}$
Q_A $[cm^{-2}]$	$7 \cdot 10^{11}$
E_0 $[eV]$	0.18
E_S $[eV]$	0.1

Table B.2: Interface defects parameters

COULOMB SCATTERING MOBILITY MODEL PARAMETERS		
	ELECTRONS	HOLES
μ_1 $[cm^2/Vs]$	9	5
k	10	10
c_{trans} $[cm^2/Vs]$	$1 \cdot 10^{18}$	$1 \cdot 10^{18}$
v	1.5	1.5
η_1	1	1
η_2	0.5	0.5
N_1 $[cm^{-3}]$	1	1
N_2 $[cm^{-3}]$	1	1
γ_1	0	0
γ_2	0	0
l_{crit} $[cm]$	$1 \cdot 10^{-6}$	$1 \cdot 10^{-6}$
E_0 $[V/cm]$	$1 \cdot 10^{6}$	$1 \cdot 10^{6}$
γ	2	2

Table B.3: Coulomb scattering mobility model parameters

Appendix C

Short-circuit Protection

Protection of power devices against failures due to undesired short circuit event is an issue in several applications, especially for motor-driving systems where short circuit could occur in different ways. A protection circuit has to detect the possible short-circuit condition during normal device operation and subsequently it has to safely turn off the device itself to avoid failure vent. For Silicon devices many solutions have been proposed [1]-[7], requiring a fast intervention of the protection circuit before failure occurrence (usually <10 μs). The easiest and most commonly adopted method to detect SC condition is the *de-saturation* technique [8]-[11]. It is based on the use of a *de-sat diode D* connected to the drain as shown in Figure C.1. When the device is conducting the diode is forward biased and the capacitor C is discharged. If a short circuit occurs the voltage on the drain rises until the de-sat diode goes into blocking mode. The capacitor will charge with a time constant $R_{tot} \cdot C$; when its voltage is higher than a given threshold, and at the same time the gate voltage is high, the short circuit is detected. A detailed description of this technique can be found in literature.

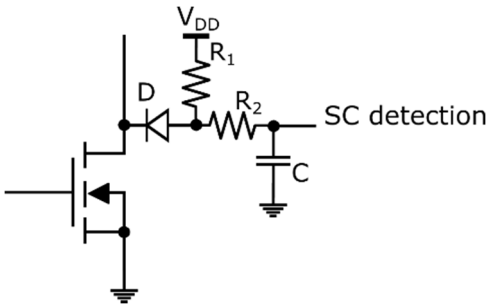

Figure C.1: Basic diagram of de-saturation technique

For SiC devices the overcurrent protection is more challenging due to reduced SC capability of these devices. Protection circuits have to act as fast as possible not only to avoid catastrophic failure but also to prevent compromising degradation of the structure. Different works have analysed and proposed protection schemes for SiC devices [12]-[13].

Here a simple circuit based on the de-saturation technique is developed. The block diagram and the PCB of the realized circuit are depicted in Figure C.2. The power section is optically decoupled from the logic and control section. When the SC condition is detected (capacitor voltage greater than fixed threshold) the control logic acts to safely remove the short circuit. First it disables the driver circuit and clamps the gate voltage using a Zener diode (12-15 *V*), in order to reduce the overcurrent peak. Subsequently, the device is softly turned off applying a high resistance (50-100 *Ω*) between gate and source, in order to avoid dangerous voltage spikes due to high *di/dt*.

The circuit was tested during *Fault Under Load* (FUL) and *Hard Switching Fault* (HSF) short circuit conditions [14]. The results are reported in Figure C.3 and Figure C.4. The circuit correctly detects the undesired operation mode and safely removes the short circuit condition. The total time required is approximately 550 *ns* in the FUL case and 200 *ns* in the HSF case.

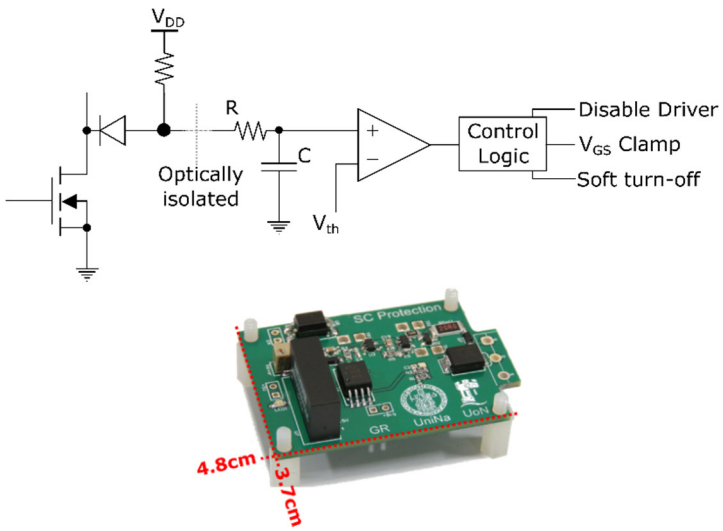

Figure C.2: Block diagram and PCB of the realized protection circuit

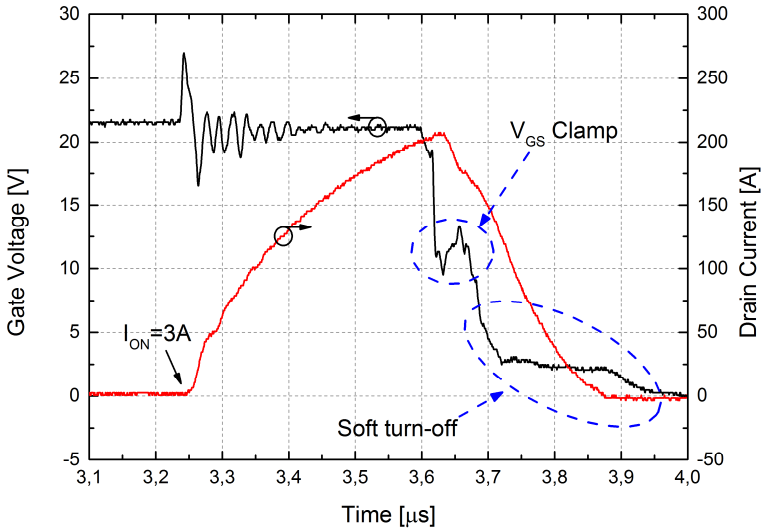

Figure C.3: FUL, CREE C2M0080120D device
(V_{DS}=800V; V_{GS}=18V; T_{CASE}=27°C)

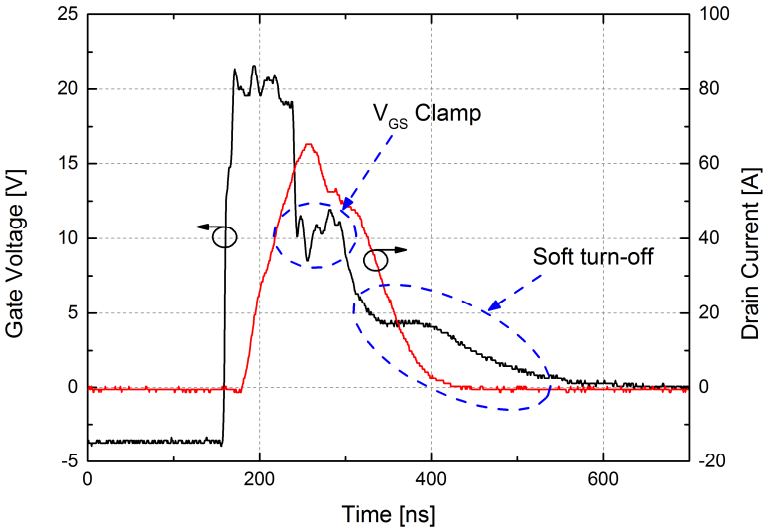

Figure C.4: HSF, ROHM SCT2080KE device
(V_{DS}=800V; V_{GS}=18V; T_{CASE}=27°C)

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