



Open Archive TOULOUSE Archive Ouverte (OATAO)

OATAO is an open access repository that collects the work of Toulouse researchers and makes it freely available over the web where possible.

This is an author-deposited version published in: <http://oatao.univ-toulouse.fr/>
Eprints ID: 17300

To link this article: <http://dx.doi.org/10.1016/j.sse.2016.05.009>

To cite this version: Pelamatti, Alice and Goiffon, Vincent and Chabane, Aziouz and Magnan, Pierre and Virmontois, Cédric and Saint-Pé, Olivier and Breart de Boisanger, Michel *Charge Transfer Inefficiency in Pinned Photodiode CMOS image sensors: Simple Montecarlo modeling and experimental measurement based on a pulsed storage-gate method.* (2016) Solid-State Electronics, vol. 125. pp. 227-233. ISSN 0038-1101

Any correspondence concerning this service should be sent to the repository administrator: staff-oatao@listes-diff.inp-toulouse.fr



Charge Transfer Inefficiency in Pinned Photodiode CMOS image sensors: Simple Montecarlo modeling and experimental measurement based on a pulsed storage-gate method

Alice Pelamatti ^{a,*}, Vincent Goiffon ^a, Aziouz Chabane ^a, Pierre Magnan ^a, Cédric Virmontois ^b, Olivier Saint-Pé ^c, Michel Breart de Boisanger ^c

^a ISAE-Supaero, Université de Toulouse, Image Sensor Research Team, Toulouse 31055, France

^b Centre National d'Etudes Spatiales (CNES), Toulouse 31400, France

^c Airbus Defence and Space, Toulouse 31030, France

A B S T R A C T

The charge transfer time represents the bottleneck in terms of temporal resolution in Pinned Photodiode (PPD) CMOS image sensors. This work focuses on the modeling and estimation of this key parameter. A simple numerical model of charge transfer in PPDs is presented. The model is based on a Montecarlo simulation and takes into account both charge diffusion in the PPD and the effect of potential obstacles along the charge transfer path. This work also presents a new experimental approach for the estimation of the charge transfer time, called pulsed Storage Gate (SG) method. This method, which allows reproduction of a "worst-case" transfer condition, is based on dedicated SG pixel structures and is particularly suitable to compare transfer efficiency performances for different pixel geometries.

Keywords:

CMOS image sensor
Pinned Photodiode
Charge Transfer Inefficiency
Transfer time

1. Introduction

Thanks to their outstanding performances, Pinned Photodiode CMOS Image Sensors (PPD CIS) [1] are currently the main image sensors technology for both commercial and scientific applications. A schematic drawing of a four-transistors PPD pixel is shown in Fig. 1. The Pinned Photodiode (PPD) [2,3] is a buried channel photodiode, formed by a double $p + np$ junction, where the $p+$ implant, also referred to as pinning-implant, pins the surface at the substrate potential. The PPD is associated to a Floating Diffusion (FD), to a Transfer Gate (TG) and to three other transistors (T1, T2 and T3, respectively). The FD is responsible for the conversion of the signal from the charge domain to the voltage domain, the TG is used to isolate/connect the PPD from/to the FD (depending on the applied TG biasing voltage), T1 is used to reset the FD potential, T2 is in source follower configuration, enabling a low impedance readout of the pixel output, whereas T3 corresponds to the column selection transistor.

PPD CIS are based on a transfer of charge. During light integration, the TG is turned off and the photo-generated carriers are col-

lected and stored in the PPD. At the end of integration, the TG is turned on and the PPD charge is transferred to the FD, resulting in a decrease of the FD potential which is proportional to the amount of transferred charge. The TG is then turned off again and a new light integration phase can start. The peculiar structure of the PPD does not only result in a very low dark current (by isolating the PPD from the SiO_2 -Si interface-states), but also limits the maximum deviation of the PPD potential from equilibrium, which is reached at the end of the transfer phase. The presence of this "potential floor", often referred to as pinning voltage [4,5] enables true charge transfer from the PPD to the FD (or to another buried channel), whereas in standard photodiodes (formed by a simple pn junction) only charge sharing between two capacitances is possible [2]. Typical readout timing diagrams and an exhaustive description of PPD CIS operation principle are detailed in [1].

If the TG "on-time" is not long enough to ensure that all photo-carriers have been successfully transferred to the FD, the charge remaining in the PPD results either in charge lag [6], or in charge loss² (and therefore in non-linearities). As discussed in this work, the efficiency of the charge transfer process is a key performance parameter, which can be critical for applications which require pixel pitches of several tens of μm . Examples of such applications are

* Corresponding author.

E-mail address: alice.pelamatti@gmail.com (A. Pelamatti).

¹ The authors would like to thank CNES and Airbus Defence and Space for supporting the Ph.D of A. Pelamatti.

² For example if the timing diagram includes a "dump phase".

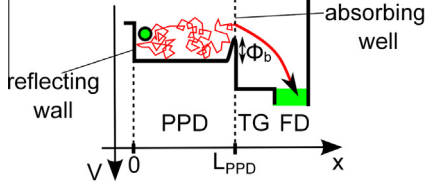
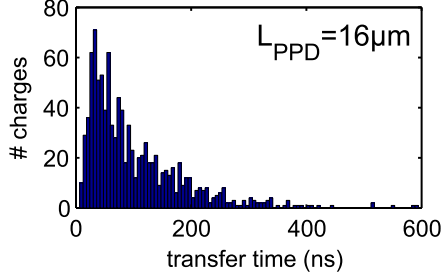
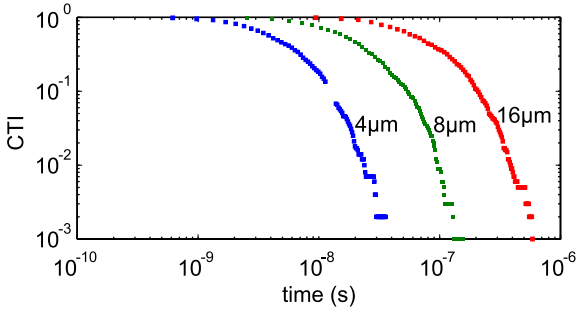


Fig. 2. Schematic potential diagram of a PPD pixel. The drawing also includes initial conditions and boundary conditions used in the Monte Carlo simulation of the random walk of carriers in the PPD. L_{PPD} corresponds to the PPD length.



(a)



(b)

Fig. 3. (a) Histogram of the time required to transfer 1000 electrons in a 16 μm PPD (Monte Carlo simulation) assuming a diffusion coefficient. (b) Simulated CTI curves for different PPD lengths. In both simulations, $D_n = 19 \text{ cm}^2/\text{s}$ and $\Phi_b = 0 \text{ V}$ (no potential barrier at the PPD-TG interface).

Fig. 2 shows a schematic potential diagram of a PPD pixel, with the initial conditions and boundary conditions used in the Monte Carlo simulation. In particular, the model is based on the following hypothesis:

- In order to reproduce a “worst-case” charge transfer condition, it is assumed that electrons are initially located at the far end of the PPD with respect to the TG ($x = 0$).
- It is also assumed that the PPD end wall and the PPD-TG interface behave as a perfect reflecting wall and a perfect absorbing wall, respectively.
- The model also takes into account the presence of a potential obstacle (potential barrier) of height Φ_b at the PPD-TG interface ($x = L_{PPD}$). In particular it is assumed that when reaching the absorbing wall $x = L_{PPD}$, electrons can either cross the barrier by thermionic emission [29] (and therefore be considered as “transferred”), or “bounce” on the barrier and continue their random walk in the PPD. The probability p_{cross} of having a sufficiently high energy to cross the barrier is an exponential function of Φ_b [29]:

$$p_{\text{cross}} = \exp(-\Phi_b/u_{\text{th}}) \quad (2)$$

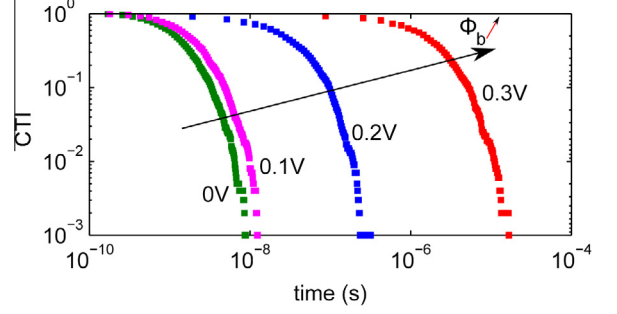


Fig. 4. Simulated CTI for a 2 μm long PPD for increasing potential barrier heights Φ_b (the potential obstacle is located at $x = L_{PPD}$).

with u_{th} the thermal voltage.

- Finally, for simplicity reasons, the PPD potential is assumed to remain constant during transfer, which is a valid hypothesis when considering the transfer of the last electrons, which represents the slowest and most critical phase of charge transfer. PPD potential variations should however be included in the model when modeling the transfer of the first transferred electrons.

2.1. Definition of Charge Transfer Inefficiency and charge transfer time

Ideally one would like to estimate the time required to transfer an electron to the FD as a function of its initial position, obtaining a “mapping” of the transfer time. **Fig. 3a** shows the histogram of the transfer times obtained from the simulation of the random walk of 1000 electrons (all starting from the end of the PPD at $x = 0$) in a 16 μm long PPD (assuming $\Phi_b = 0 \text{ V}$). As can be observed, it is not possible to identify a unique transfer time value for the simulated structure, as it is not a deterministic parameter. It is important to keep in mind this statistical behavior, especially when single photon resolution is targeted. In particular, one should be aware that, even if the device enables a sensitivity of a few electrons and has a 100% quantum efficiency, the collected carriers, when considered singularly, might all reach the FD in one frame, and not in the following frame. This charge transfer uncertainty (noise) is an additional contribution with respect to the noise sources studied in [6]. For this reason, charge transfer performances are usually studied in terms of Charge Transfer Inefficiency (CTI), which is defined as:

$$\text{CTI} = 1 - \frac{Q_{\text{out}}}{Q_{\text{PPD}}} \quad (3)$$

with Q_{out} the charge that is successfully transferred (on average) from the PPD to the FD and Q_{PPD} the charge in the PPD before transfer. Example of simulated CTI curves are shown in **Fig. 3b**. Based on this definition, in this work the “transfer time” of a PPD pixel is defined as the minimum TG “on-time” required to reach a given CTI level.

2.2. Effect of potential obstacles

Fig. 4 shows the CTI curve simulated for a 2 μm PPD in a pure diffusion regime, with and without the presence of a potential barrier Φ_b at the PPD-TG interface.⁴ As shown in the figure, the presence of a potential obstacle results in a worsening of the transfer time of several orders of magnitude. It can also be observed that at small Φ_b values (0.1 V), there is only a limited CTI shift with respect

⁴ Here, only a short PPD is simulated due to the very long simulation times for large Φ_b values.

to the zero barrier condition, since transfer is still mainly limited by diffusion. A non-optimum tuning of the TG and PPD doping implants can therefore strongly limit temporal resolution performances of PPD CIS. Note that in this simulation the PPD potential (and therefore the potential barrier seen by electrons) is considered constant during transfer. As discussed at the beginning of this section this assumption is valid when the initial PPD charge density is low (a few tens/hundreds of electrons per μm^2), if not, a more realistic modeling of the effect of potential obstacles can be obtained by means of an iterative recalculation of the PPD potential such as in [19].

3. Experimental measurement of Charge Transfer Inefficiency

Comparing temporal resolution performances of pixels with different sizes and geometries is not a trivial task, as the outcome can be very different depending on how measurements are performed. A common solution to measure CTI consists in measuring the output charge as a function of the TG pulse width [30]. This approach has two main limitations: first, very short TG pulses can hardly be implemented without distorting the TG signal (therefore CTI can often not be observed for transfer times of the order of a few ns); secondly, the initial PPD charge distribution is strongly affected by the pixel geometry. As a result, different pixel designs might not always be “comparable”. For example, designing triangular/trapezoidal PPDs is a particularly widespread solution to induce a drift field in the PPD (by geometrical modulation of the PPD potential [22]). In order to correctly size the device, one might wish to monitor the transfer time as a function of the PPD geometry (e.g. to identify the maximum PPD width for which the PPD local potential can be modulated). However, as schematized in Fig. 5, in trapezoidal PPDs, charge will be always, on average, closer to the TG with respect to rectangular PPDs. Therefore, one can observe an enhancement of the transfer speed with the PPD geometry even when the PPD electric field is zero.

3.1. Pulsed Storage Gate method

In order to “fairly” compare these structures, in this work it is proposed to measure CTI performances based on Storage Gate (SG) pixels such as the one schematized in Fig. 6a. These pixels are very similar to standard 4T PPD CIS pixels except for an additional SG located at opposite side of the PPD with respect to the TG. The timing diagram used during the measurements is shown in Fig. 7. During the charge integration phase, electrons are accumulated under the SG by applying a positive biasing potential ($V_{SG} = 3.3\text{ V}$ here). To modulate the charge stored under the SG, the experimental set-up also includes a LED (here $\lambda_{LED} = 540\text{ nm}$), which is pulsed-on during charge integration (Fig. 6b). The amount of stored electrons can therefore be tuned depending on the SG size, on the SG biasing potential and on the

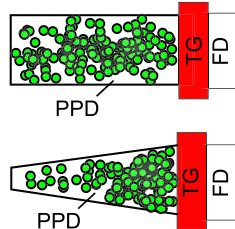


Fig. 5. Schematic drawing of the charge distribution in a rectangular PPD and in a trapezoidal PPD. Depending on the pixel shape, charge can be, on average, more or less close to the TG, resulting in an enhancement of the transfer efficiency even for a zero drift field.

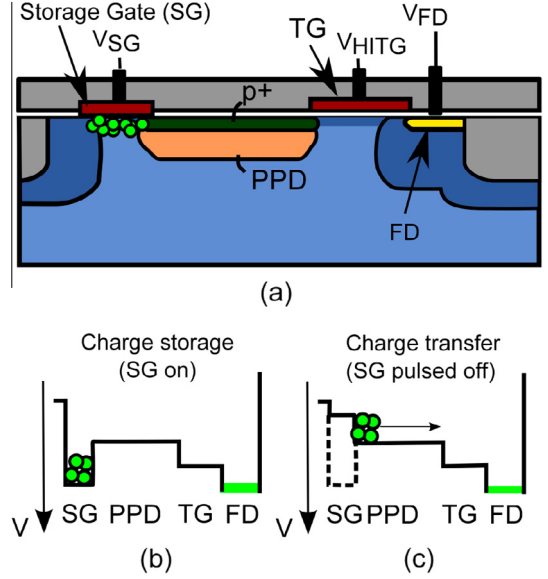


Fig. 6. (a) Schematic drawing of a Storage Gate (SG) pixel. For simplicity, the reset transistor, the source follower transistor and the column selection transistor are not represented. (b) Schematic potential diagram of the SG during charge integration phase. (c) Schematic potential diagram of the SG at the beginning of charge transfer (charge injection phase).

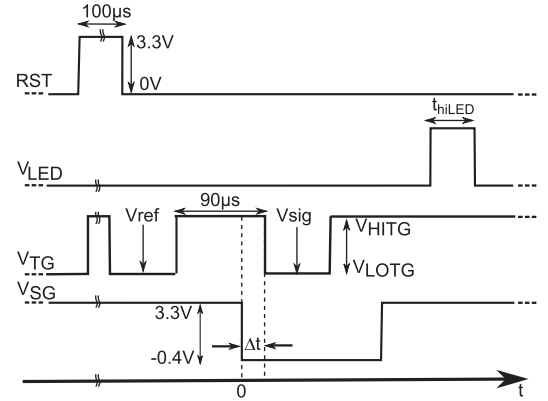


Fig. 7. Timing diagram for the proposed CTI estimation method. T_{INT} represents the integration time during which charges can be stored under the SG.

intensity and width (t_{hiLED}) of the LED pulse. Before the transfer phase, the TG is turned-on for $100\ \mu\text{s}$ to fully empty the PPD, then is turned-off to sample the reference (V_{ref}) and pulsed on again. The charge stored under the SG is then injected in the PPD by pulsing the SG off (Fig. 6c). In order to reproduce the confinement effect of the PPD end-wall, during transfer the SG is biased in accumulation mode ($V_{SG} = -0.4\text{ V}$ here). As long as the TG is on, injected electrons can diffuse in the PPD and reach the FD. Then the TG is turned off and the signal (V_{sig}) is sampled. The amount of transferred charge Q_{out} is estimated as:

$$Q_{out} = \frac{V_{ref} - V_{sig}}{CVF} \quad (4)$$

with CVF the charge to voltage conversion factor.

To measure Q_{out} as a function of the transfer time, one can simply vary the delay Δt between the falling edges of the SG signal and the TG signal, respectively (Fig. 7). To estimate the CTI, one also needs to estimate the total charge in the PPD before transfer. In this

work the reference charge Q_{PPD} corresponds to the Q_{out} measured for a delay of $\Delta t = 90 \mu s$.

The pulsed SG method has several advantages with respect to the measurement based on the sweeping of the TG pulse width:

- It reproduces a worst case transfer conditions (as carriers are initially located at the far end of the PPD with respect to the TG).
- The initial amount of injected charge does not depend on the PPD geometry (only on the SG geometry).
- It does not require very short TG pulses (as transfer time is swept changing the delay between two falling edges). Therefore the CTI can be observed down to transfer times as short as the minimum SG and TG signals fall time.

3.2. Device under test

A 32×1 SG pixel array has been realized in a commercially available $0.18 \mu m$ PPD CIS technology. The array is divided into four 1×8 sub-arrays with increasing PPD lengths: $4 \mu m$, $8 \mu m$, $16 \mu m$ and $32 \mu m$. All PPDs are $5 \mu m$ wide. The CVF is about $10 \mu V/e^-$ for all the tested pixels. The TG is $5 \mu m$ wide and $0.7 \mu m$ long. The SG size is $0.3 \mu m \times 5 \mu m$.

3.3. Experimental results

Fig. 8 shows the CTI experimental curves obtained for different PPD lengths. Both the V_{TG} and V_{SG} signals vary between $3.3 V$ (pulse high level) and $-0.4 V$ (pulse low level). The LED pulse is $100 \mu s$ long. Data have been averaged over 400 acquisitions on the 8 pixels forming each sub-array. Measurements have been obtained at room temperature in the dark. As expected from simulations, we observe a shift of the CTI curve toward higher transfer times when L_{PPD} is increased. Furthermore, as shown in Fig. 9, the transfer time corresponding to a 0.01 CTI⁵ increases as the square of the PPD lengths, which is in accordance with the diffusion law. However, by looking at the absolute value of the transfer time, it can be observed that charge transfer is much slower than the one predicted by the MC model in a pure diffusion regime (two orders of magnitude larger here).

Based on several iterations of the RW MC model for different initial conditions (such as for different diffusion coefficients and potential barrier heights) it has been concluded that this slow transfer can only be explained by the presence of a potential obstacle along the charge transfer path (as no realistic diffusion coefficients could slow down the transfer that much). In the following section, this hypothesis is investigated by presenting CTI curves measured for different experimental conditions.

3.4. Effect of PPD charge density

During transfer, as the PPD is being emptied of carriers, its potential increases, until reaching the pinning voltage. As a result, the barrier seen by electrons also increases as a function of the electron density in the PPD (Fig. 10a). In particular, the larger the charge density, the faster the transfer in the first instants. Since CTI is a normalized quantity, for a given CTI level and given SG pixel geometry, a smaller transfer time is expected for a larger initial PPD charge in the presence of potential obstacle. The hypothesis of potential barrier-limited transfer is supported by the experimental curves in Fig. 10b, which show the average CTI measured on $16 \mu m$ and $32 \mu m$ long SG pixels for two different initial PPD charges $Q_{PPD2} \approx 2 \times Q_{PPD1}$. As can be observed, in the $16 \mu m$

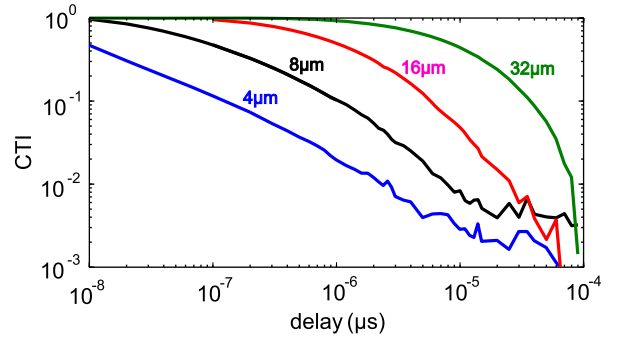


Fig. 8. Measured CTI curves as a function of the delay between the falling edges of the SG and TG signals for different PPD lengths on dedicated SG pixels.

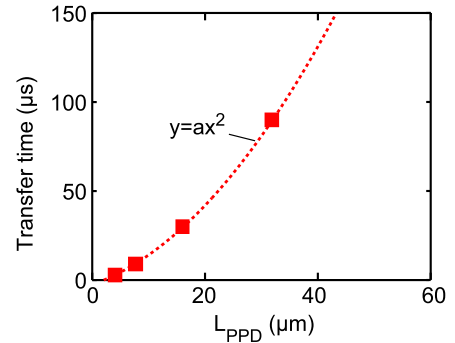


Fig. 9. Charge transfer time estimated from the measurements in Fig. 8 to reach a CTI of 0.01 as a function of the PPD length.

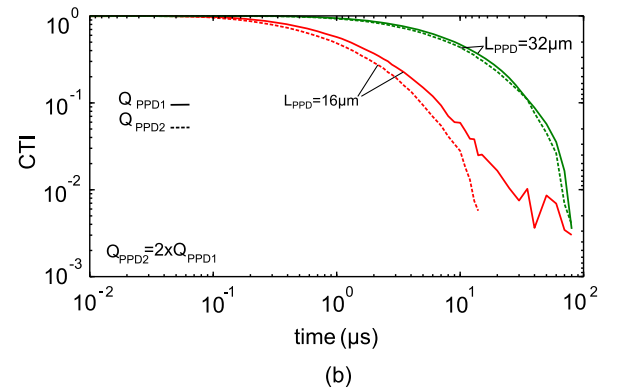
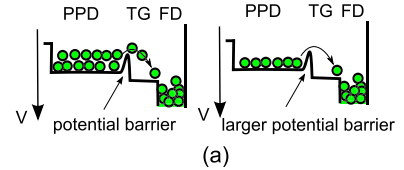


Fig. 10. (a) Schematic PPD potential diagram representing the effect of the PPD charge density on the potential barrier experienced by electrons during transfer. (b) Measured CTI curves as a function of the delay between the falling edges of the SG and TG signals for $L_{PPD} = 16 \mu m$ and $L_{PPD} = 32 \mu m$ for two different initial PPD charges $Q_{PPD2} \approx 2 \times Q_{PPD1}$ (corresponding to two different LED pulse widths, t_{hiLED}).

pixels the difference in the PPD charge density for Q_{PPD1} and Q_{PPD2} is large enough to affect the potential barrier experienced by carriers during transfer, whereas the CTI behavior is almost unchanged in the $32 \mu m$ long pixels. Note that a transfer speed enhancement measured at a higher charge density could also be

⁵ For noise reasons transfer time cannot be correctly estimated here at a CTI level of 0.001.

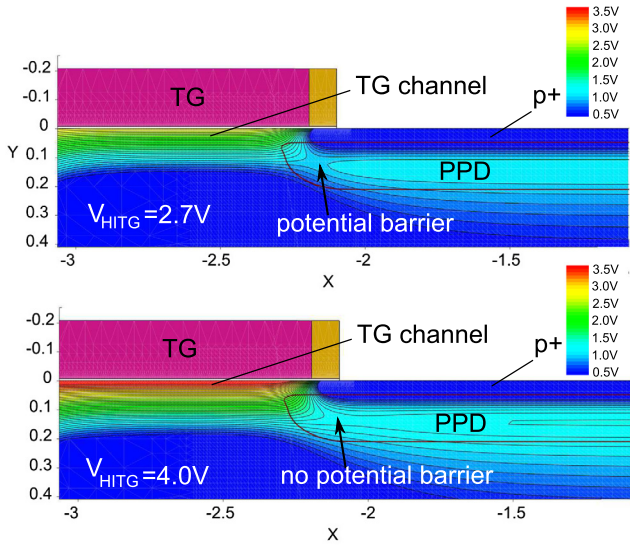


Fig. 11. TCAD simulation of the potential distribution at the PPD-TG interface for two different V_{HITG} biasing levels (2.7 V and 4 V, respectively). As it can be observed, increasing the TG biasing potential results in a reduction of the potential barrier between the PPD and the TG channel.

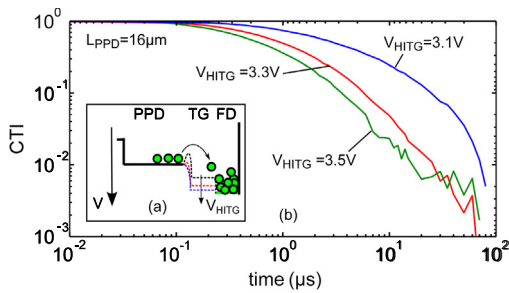


Fig. 12. (a) Schematic PPD potential diagram representing the effect of the TG channel potential on the potential barrier at the PPD-TG interface. (b) Measured CTI curves as a function of the delay between the falling edges of the SG and TG signals for three different V_{HITG} values.

due to the contribution of the electrostatic repulsion between carriers (self-induced drift). However, the charge densities involved in these measurements (a few hundreds of electrons per μm^2) are low enough to neglect these additional phenomena.

3.5. Effect of TG biasing potential

Fig. 11 shows the potential distribution at the PPD-TG interface simulated in TCAD for two different V_{HITG} levels. In particular, it is shown that the potential barrier observed at the PPD-TG interface for $V_{\text{HITG}} = 2.7$ V becomes negligible if a larger potential is applied to the TG ($V_{\text{HITG}} = 4$ V here). Therefore, the effect of potential obstacles can be reduced by modulating the TG channel potential (a schematic representation of this leveling effect is shown in Fig. 12a). As a result, a possible approach to verify whether in a specific device charge transfer is mainly limited by the presence of a potential obstacle, consists in measuring the CTI at different V_{HITG} values. Fig. 12b shows the CTI curve measured on 8 μm long SG pixels for different TG biasing potentials during transfer. As can be observed, charge transfer efficiency is enhanced for larger V_{HITG} even at typical TG biasing values (around 3.3 V here). These results, together with the ones presented in Section 3.4, both support the hypothesis of a potential barrier limited transfer.

4. Conclusions

Understanding the mechanisms that limit charge transfer is particularly critical for the design of high temporal resolution PPD CIS detectors, where the maximum sampling frequency is limited by the time required to transfer the charge packet from the PPD to the FD. This work presented a study on the estimation and measurement of charge transfer time in PPD CIS. A simple Montecarlo model of the random walk of carriers in the PPD has been proposed. As this work focused on the phenomena limiting charge transfer in long PPD pixels, only carrier diffusion within the PPD and the effect of potential obstacles along the charge transfer path have been included in the simulations. In small PPD pixels, electron drift (induced by fringing fields, self-induced fields or engineered drift fields) should also be taken into account by introducing a drift component at each time step of the simulation.

This work also presented a new experimental method to measure transfer time on dedicated Storage Gate pixel arrays. The proposed method enables CTI measurement with the same initial amount of charge and initial charge distribution, regardless of the PPD geometry. Based on this method, the effect of the PPD length and of potential obstacles on the experimental charge transfer behavior have been investigated. In this work only rectangular PPDs have been tested, however this method can help comparing CTI performances for more exotic PPD shapes, for different biasing voltages and different charge levels.

References

- [1] Fossum E, Hondongwa D. A review of the pinned photodiode for CCD and CMOS image sensors. *IEEE J Electron Dev Soc* 2014;2(3):33–43.
- [2] Teranishi N, Kohono A, Ishihara Y, Oda E, Arai K. No image lag photodiode structure in the interline CCD image sensor. In: *Electron devices meeting, 1982 international*, vol. 28; 1982. p. 324–7.
- [3] Burkey B, Chang W, Littlehale J, Lee T, Tredwell T, Lavine J, Trabka E. The pinned photodiode for an interline-transfer CCD image sensor. In: *Electron devices meeting, 1984 international*, vol. 30; 1984. p. 28–31.
- [4] Krymski A, Feklistov K. Estimates for scaling of pinned photodiodes. In: *Image sensor workshop*; 2005.
- [5] Pelamatti A, Goiffon V, de Ipanema Moreira A, Magnan P, Virmondois C, Saint-Pé O, et al. Comparison of pinning voltage estimation methods in pinned photodiode CMOS image sensors. *IEEE J Electron Dev Soc* 2016;99–108. <http://dx.doi.org/10.1109/JEDS.2015.2509606>.
- [6] Fossum ER. Charge transfer noise and lag in CMOS active pixel sensors. In: *Proc 2003 IEEE workshop on CCDs and advanced image sensors*, Elmau, Bavaria, Germany; 2003.
- [7] Kraft S, Del Bello U, Drusch M, Gabriele A, Harnisch B, Moreno J. On the demands on imaging spectrometry for the monitoring of global vegetation fluorescence from space, vol. 8870; 2013. p. 88700N–88700N–12.
- [8] Knoll GF. *Radiation detection and measurement*. John Wiley & Sons; 2010.
- [9] Pelamatti A, Goiffon V, Chabane A, Magnan P, Virmondois C, Saint-Pé O, et al. Charge transfer speed analysis in pinned photodiode CMOS image sensors based on a pulsed storage-gate method. In: *Solid state device research conference (ESSDERC), 2015 45th European*, Gratz; 2015.
- [10] Carnes JE, Kosonocky WF, Ramberg E. Free charge transfer in charge-coupled devices. *IEEE Trans Electron Dev* 1972;19(6):798–808.
- [11] Barbe DF. Imaging devices using the charge-coupled concept. *Proc IEEE* 1975;63(1):38–67.
- [12] Mohsen A, McGill T, Mead C. Charge transfer in overlapping gate charge-coupled devices. *IEEE J Solid-State Circ* 1973;8(3):191–207.
- [13] Banghart E, Lavine J, Trabka E, Nelson E, Burkey B. A model for charge transfer in buried-channel charge-coupled devices at low temperature. *IEEE Trans Electron Dev* 1991;38(5):1162–74.
- [14] Janesick JR. *Scientific charge-coupled devices*. SPIE Press; 2001.
- [15] Stevens E, Komori H, Doan H, Fujita H, Kyan J, Parks C, et al. Low-crosstalk and low-dark-current CMOS image-sensor technology using a hole-based detector. In: *IEEE international solid-state circuits conference, 2008. ISSCC 2008. Digest of technical papers*; 2008. p. 60–595.
- [16] Yasutomi K, Sadanaga Y, Takasawa T, Itoh S, Kawahito S. Dark current characterization of CMOS global shutter pixels using pinned storage diodes. In: *Proceedings of international image sensor workshop*, Wu Liyou; 2011.
- [17] Janesick JR, Elliott T, Andrews J, Tower J. Fundamental performance differences of CMOS and CCD imagers: Part VI. In: *SPIE*, vol. 9591; 2015.
- [18] Fowler B, Liu X. Charge transfer noise in image sensors. In: *2007 International image sensor workshop*, Ogunquit, Maine, USA Mean (DN) Pixel: NPS6-OD20 Slope, vol. 2; 2007.

- [19] Han L, Yao S, Theuwissen AJP. A charge transfer model for CMOS image sensors. *IEEE Trans Electron Dev* 2015; 1–1.
- [20] Janesick JR, Elliott T, Andrews J, Tower J, Pinter J. Fundamental performance differences of CMOS and CCD imagers: part V, vol. 8659; 2013. p. 865902–865902-35.
- [21] Zhou Y, Cao Z, Li Q, Qin Q, Wu N. Image lag optimization of four-transistor pixel for high speed CMOS image; 2011. p. 819435–819435.
- [22] Takeshita H, Sawada T, Iida T, Yasutomi K, Kawahito S. High-speed charge transfer pinned-photodiode for a CMOS time-of-flight range image sensor. In: *IS&T/SPIE electronic imaging*; 2010. p. 75360R–75360R.
- [23] Ratti L, Gaioni L, Traversi G, Zucca S, Bettarini S, Morsani F, et al. Modeling charge loss in CMOS maps exposed to non-ionizing radiation. *IEEE Trans Nucl Sci* 2013;60(4):2574–82.
- [24] Durini D, Spickermann A, Mahdi R, Brockherde W, Vogt H, Grabmaier A, et al. Lateral drift-field photodiode for low noise, high-speed, large photoactive-area CMOS imaging applications. *Nucl Instrum Meth Phys Res Sect a: Accel Spectrom Detect Assoc Equip* 2010;624(2):470–5.
- [25] Han S-M, Takasawa T, Yasutomi K, Aoyama S, Kagawa K, Kawahito S. A time-of-flight range image sensor with background cancelling lock-in pixels based on lateral electric field charge modulation. *IEEE J Electron Dev Soc* 2014;PP(99). 1–1.
- [26] Tubert C, Simony L, Roy F, Tournier A, Pinzelli L, Magnan P. High speed dual port pinned-photodiode for time-of-flight imaging. *Proc IISW* 2009:249–51.
- [27] Shin B, Park S, Shin H. The effect of photodiode shape on charge transfer in CMOS image sensors. *Solid-State Electron* 2010;54(11):1416–20.
- [28] Yang X, Theuwissen A. Image lag analysis and photodiode shape optimization of 4t CMOS pixels; 2013.
- [29] Sze SM. *Semiconductor devices, physics and technology*. Wiley; 1985.
- [30] Bonjour L, Blanc N, Kayal M. Experimental analysis of lag sources in pinned photodiodes. *IEEE Electron Dev Lett* 2012;33(12):1735–7.