CMOS Image Sensors in Harsh Radiation Environments

Vincent Goiffon, *ISAE-SUPAERO, Université de Toulouse, France*

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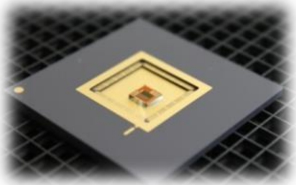
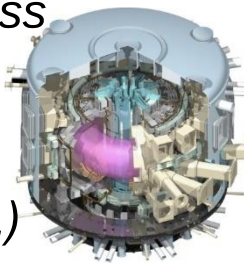
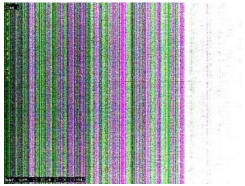
Purpose/Scope of the presentation

- **Present the basic radiation effects on CMOS Image Sensors**
  - Only **CIS specific** radiation effects
    - *Typical technology node for the discussion: 180 nm CIS process*
    - *No discussion about irrelevant effects for CIS*
      - *e.g. SEU, MBU in highly integrated digital circuits*
      - *e.g. Advanced CMOS (FinFETs, FDSOI, beyond 90 nm…)*





  - Mainly for harsh radiation environments
    - *High TID levels (MGy – Grad)*
    - *High hadron flux (> 10^{18} $cm^{-2}.s^{-1}$)*
    - *High hadron fluence (> 10^{12} cm^{-2})*



- **Illustrate these basics degradation mechanisms by presenting results achieved in recent developments**

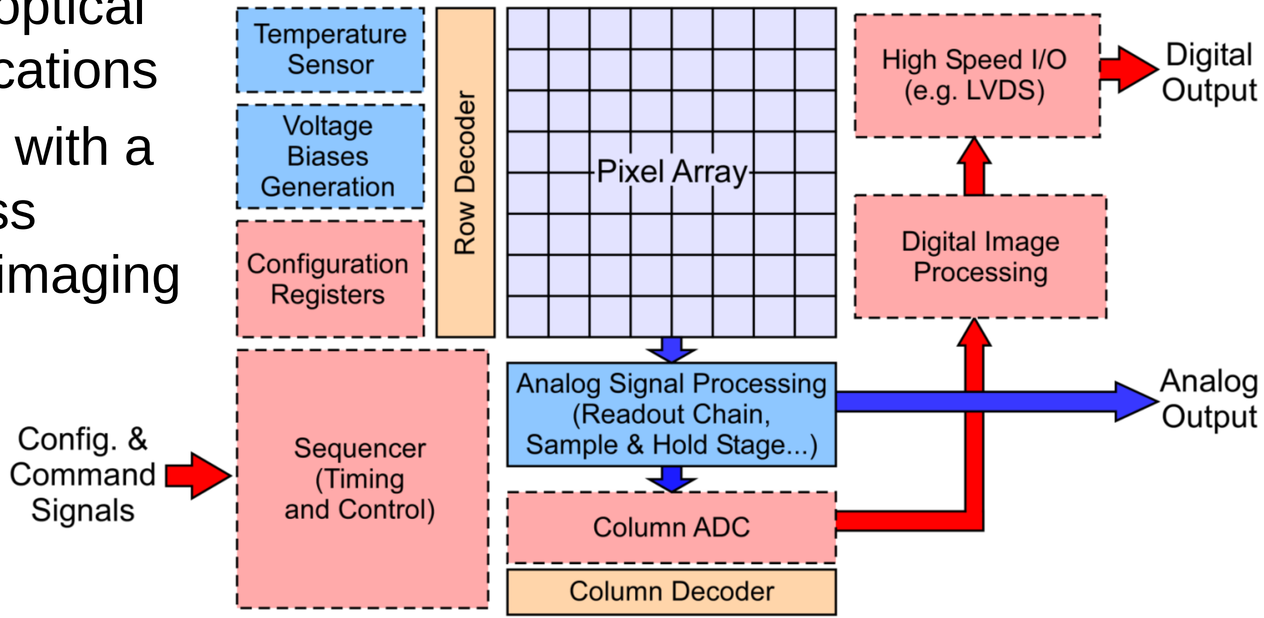
Outline

- **CMOS Image Sensor (CIS) technology: a brief overview**
- **Basic radiation induced degradation mechanisms and illustrations**
  - Total Ionizing Dose (TID) effects
    - *Hardening and use of CIS for ITER remote handling operations*
  - Single Event Effects (SEE)
    - *Use of CIS for Megajoule class Inertial Confinement Fusion (ICF) experiments*
  - Displacement Damage (DD) effects
    - *Prediction of DD effects for high fluence environment*

CIS technology: an overview

- **CMOS Image Sensors (CIS)**
  - Most popular solid state imager technology (95% of the market)
- **CIS = CMOS Integrated Circuit**
  - Designed for optical imaging applications
  - Manufactured with a CMOS process optimized for imaging

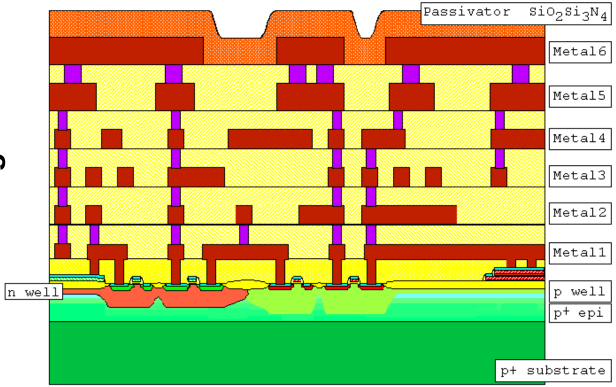
Typical CIS architecture



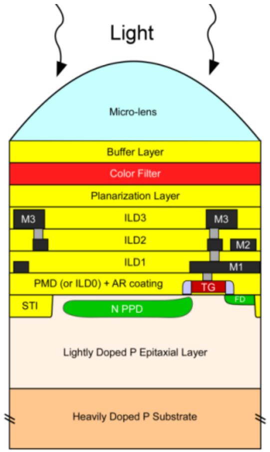
CIS manufacturing process: CMOS vs CIS

- **Compared to standard CMOS, CIS processes have:**
  - Optimized dielectric stack (reduced number of metal levels, planarization, anti-reflection coating, color filters, microlenses...)
  - Optimized epitaxial layer and doping profiles (for photo-detection)
    - *Dedicated photodiode doping profiles*
    - *Optimized threshold voltages…*

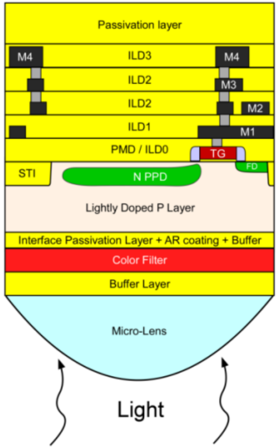
http://www2.imm.dtu.dk/courses/02216/rules018/graphics/018CrossSection.gif



Classical CMOS Process



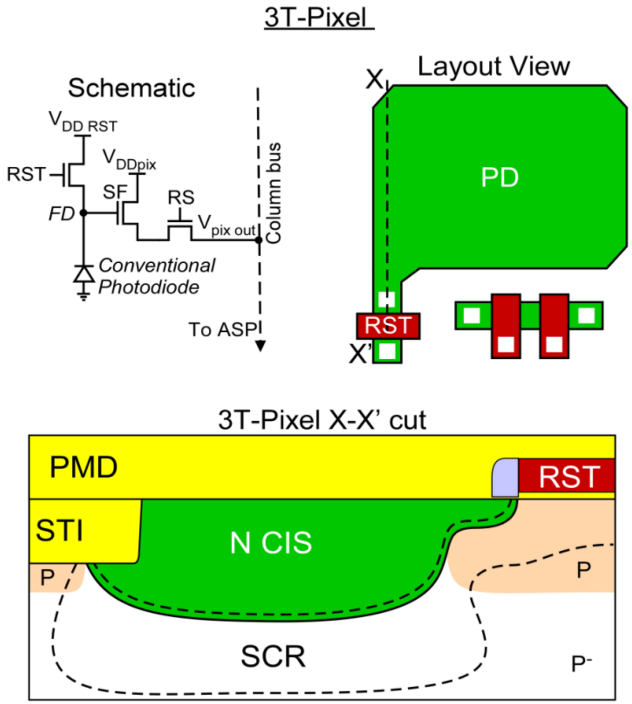
Front-side illuminated CIS process



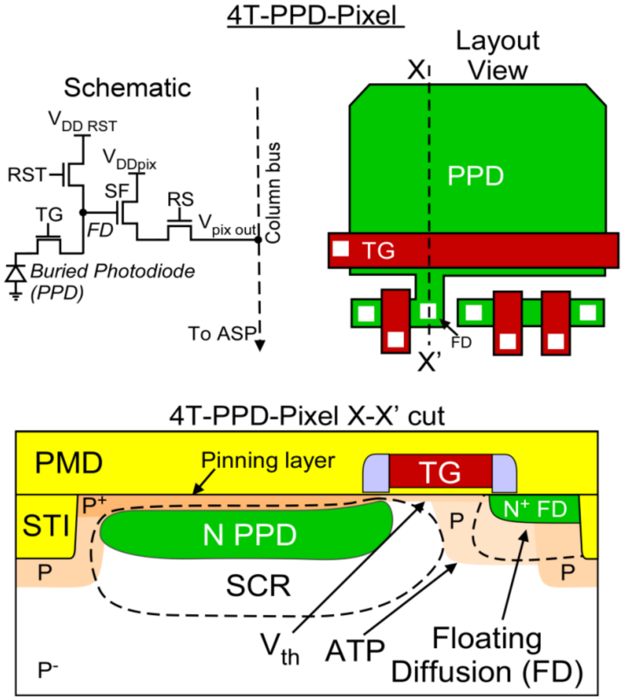
Back-side illuminated CIS process

CIS technology: pixel architecture

- **Two basic pixel designs used in most of CIS**



Conventional photodiode



Pinned (buried) PhotoDiode (PPD)

CIS, APS & MAPS?

Outline
CIS overview
Over view
Pixel
APS/ CIS/ MAPS
Rad. Effects

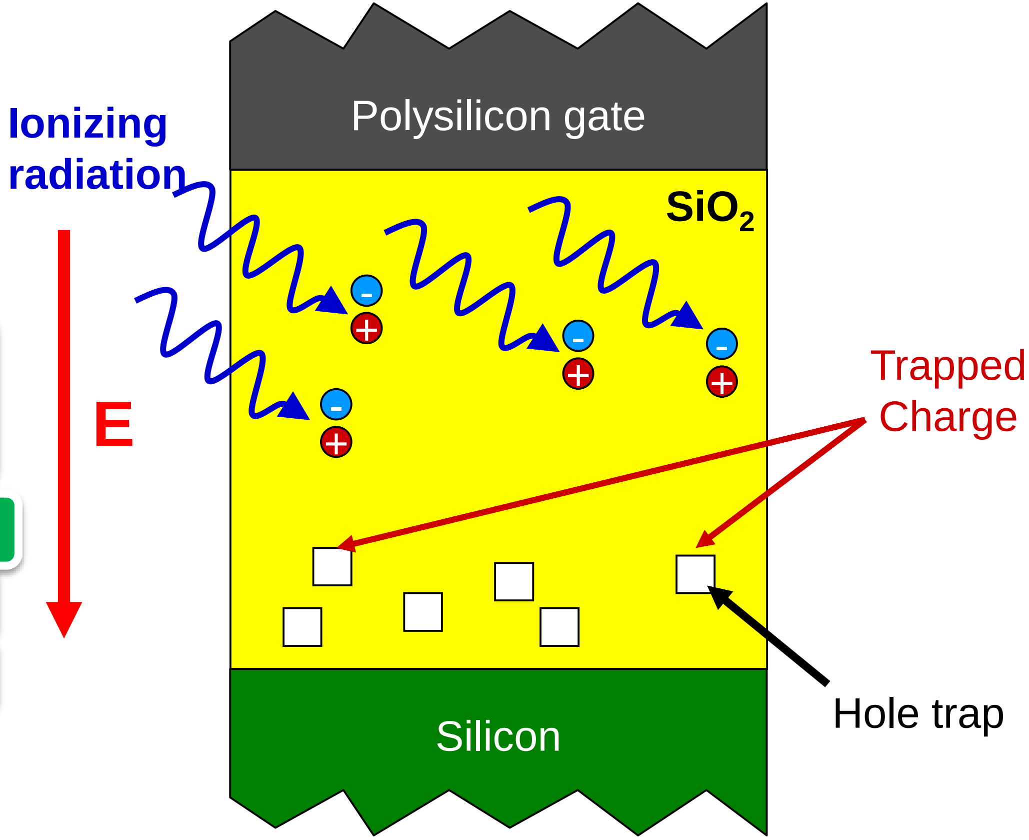
Feature	CIS	MAPS
Active Pixel Sensor*	Yes	Yes
CMOS Integrated Circuit	Yes	Yes
Monolithic	Yes	Yes
Dedicated CMOS process	Yes	No
Optimized/dedicated photodiode doping profiles	Yes	No
Optimized/dedicated optical interfaces (AR coating / color filters / microlenses / light-guide…)	Yes	No
Usual purpose	**Optical imaging**	**Particle detection**

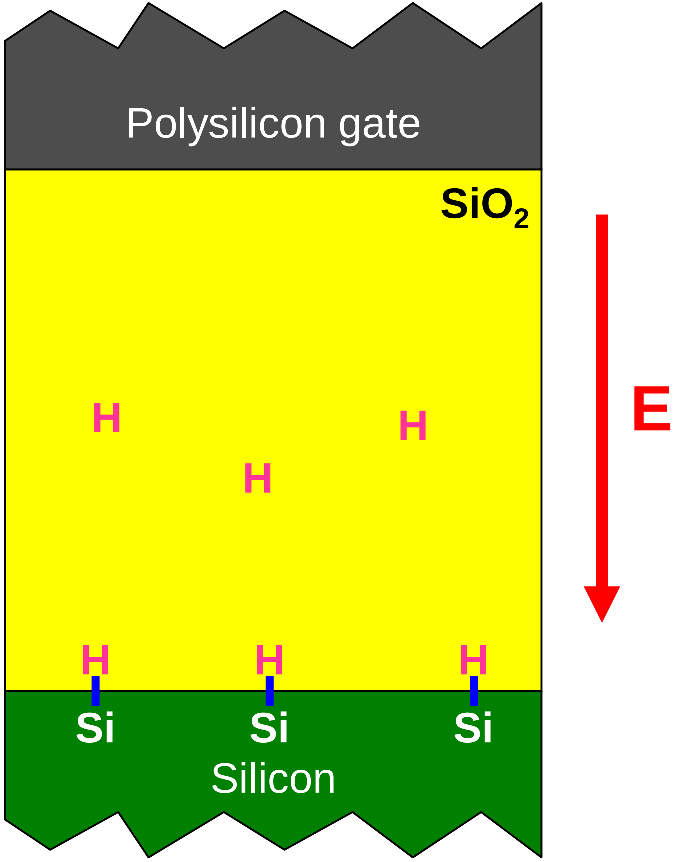
CMOS Image Sensor =
CMOS APS + optical imager design
+ dedicated CIS process

***E. R. Fossum, Proc SPIE, vol. 1900, 1993**

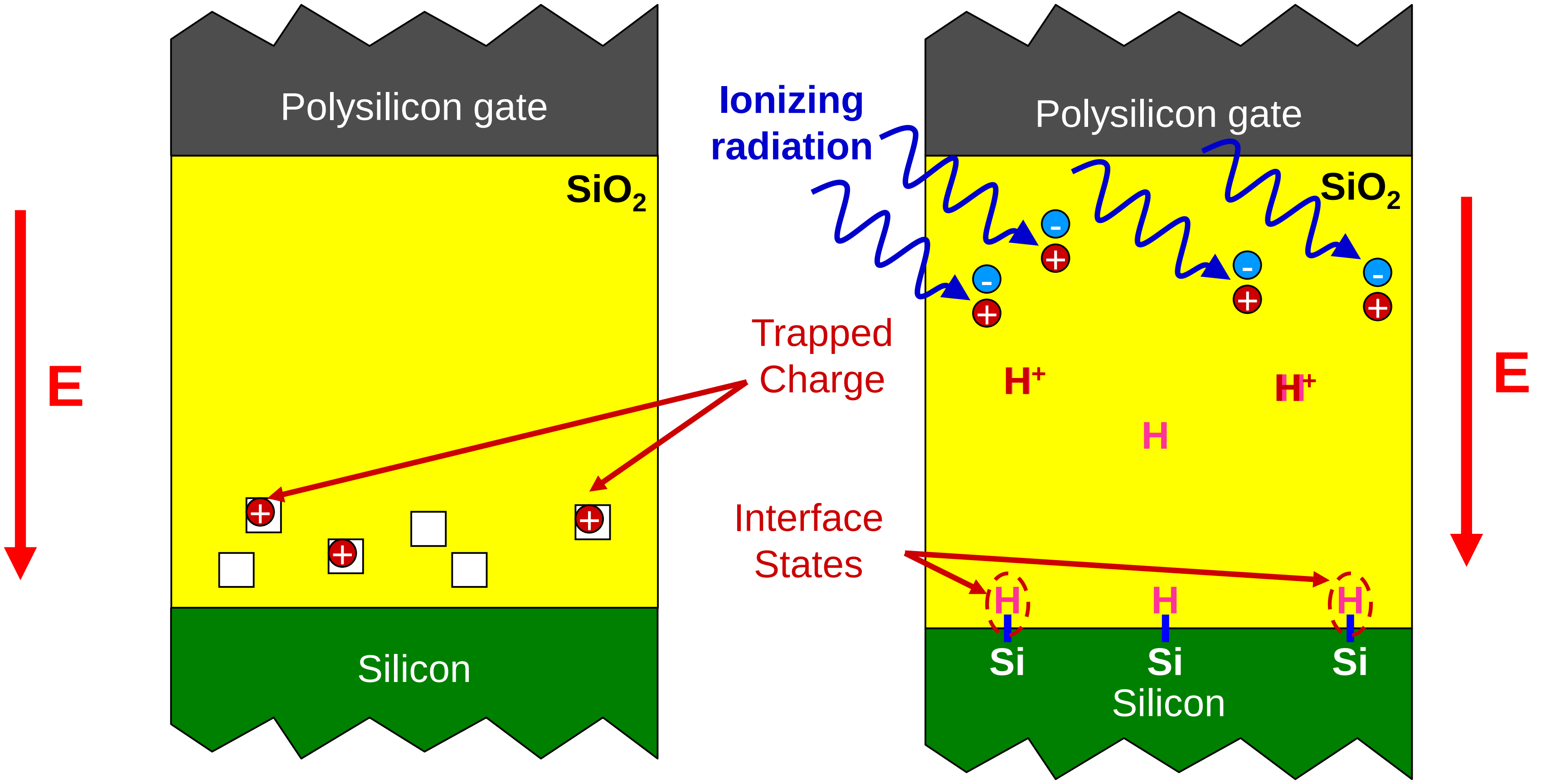
Total Ionizing Dose (TID) effects

Basic radiation effects: TID



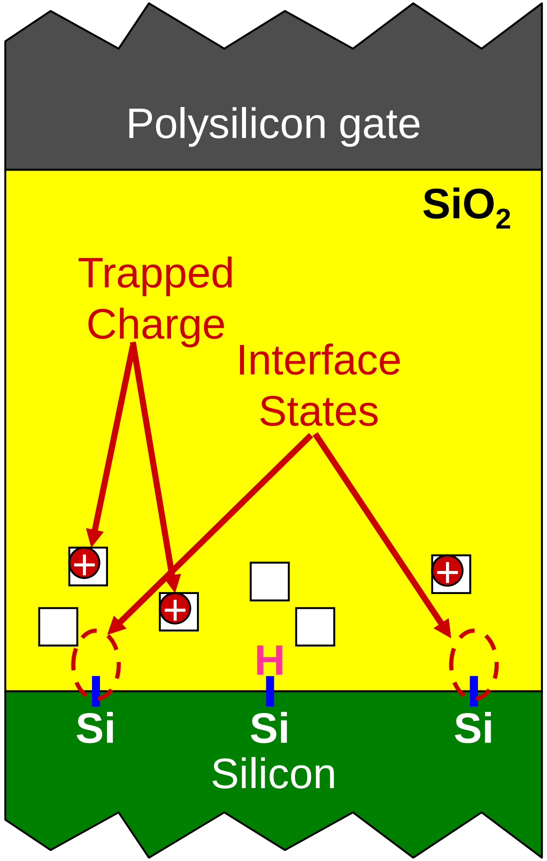


Basic radiation effects: TID



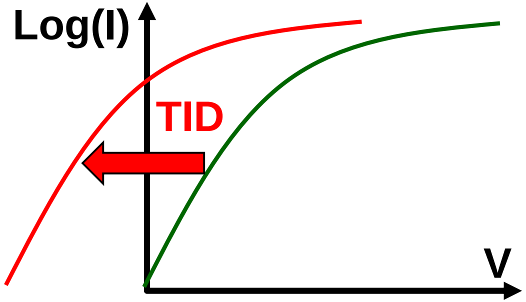
Basic radiation effects: TID

- **Ionizing radiation (X, γ, charged particles…)**
  - Generate electron-hole pairs in dielectrics
  - Leading to the buildup of permanent defects:
    - ***Oxide Trapped (OT) charge*** *(positive in most cases)*
    - ***Interface states (IT)*** *at Si/Oxide interface*

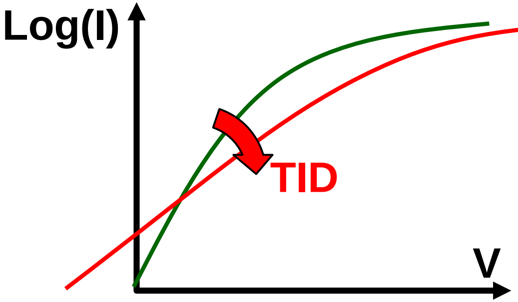


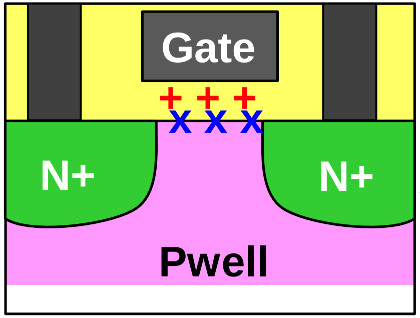
TID effects in CIS MOSFETs: gate oxide

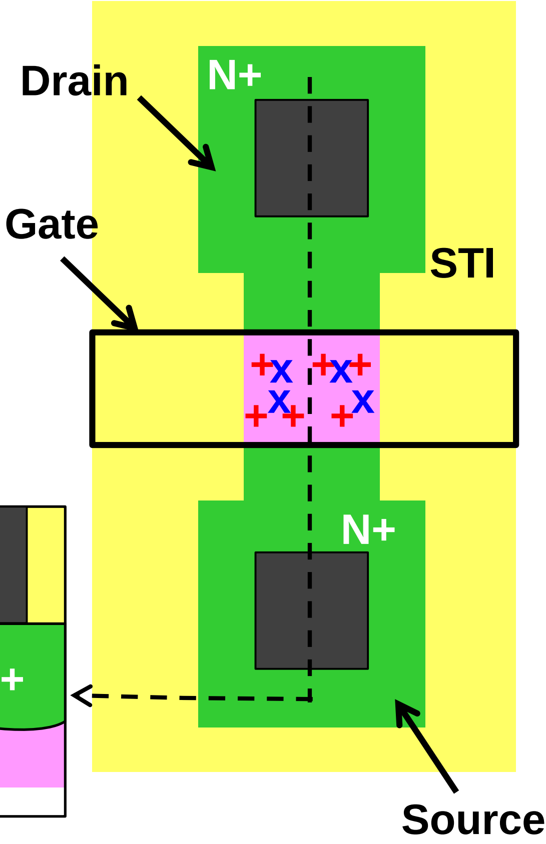
- **Gate oxide trapped charge (+):**
  - Negative threshold voltage shift ($\Delta V_{th}<0$)



- **Gate oxide interface states (x):**
  - Subthreshold slope decrease

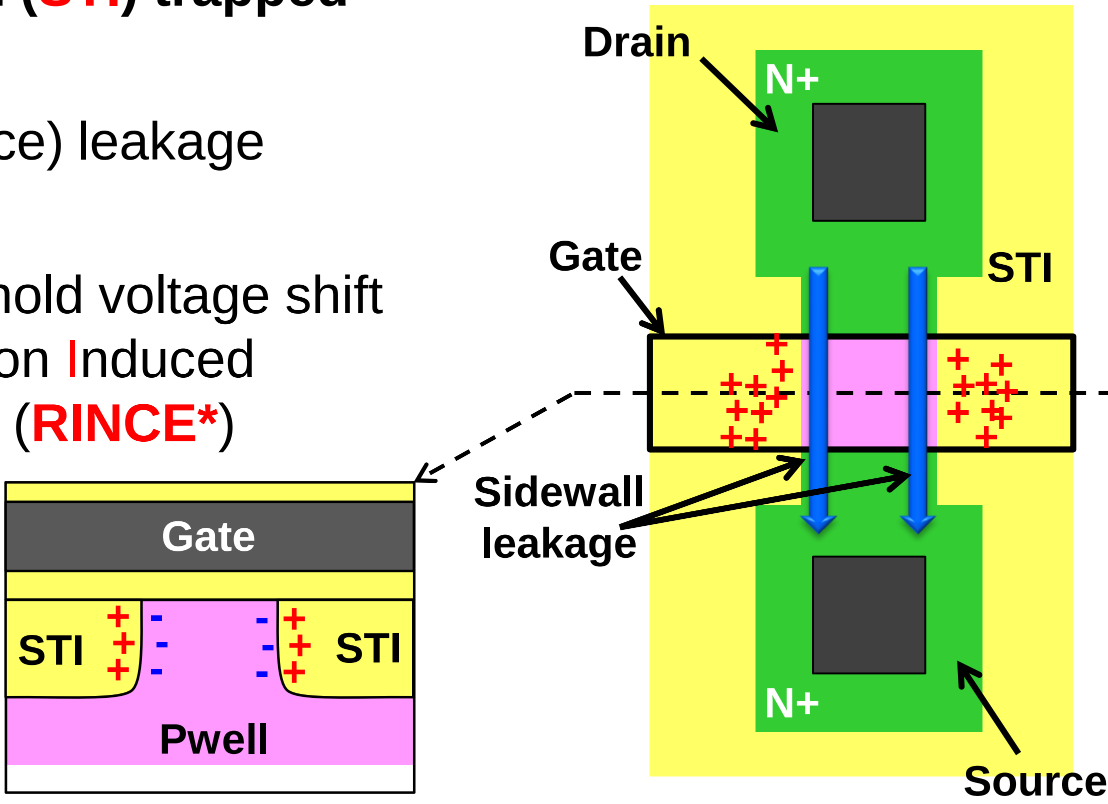






TID effects in CIS MOSFETs: STI

- **Shallow Trench Isolation (STI) trapped charge (+):**
  - Sidewall (drain to source) leakage
  - Further negative threshold voltage shift ($\Delta V_{th}<0$) called Radiation Induced Narrow Channel Effect (**RINCE***)
  - (Inter-device leakage)

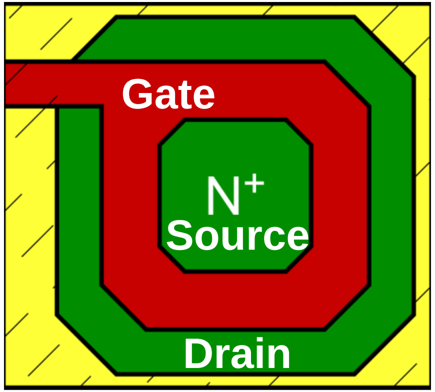


*F. Faccio et al., IEEE TNS, Dec. 2005

Enclosed Geometry: example of the ELT

- **Enclosed Layout Transistor (ELT)***
  - Circular gate design
  - No more channel edges

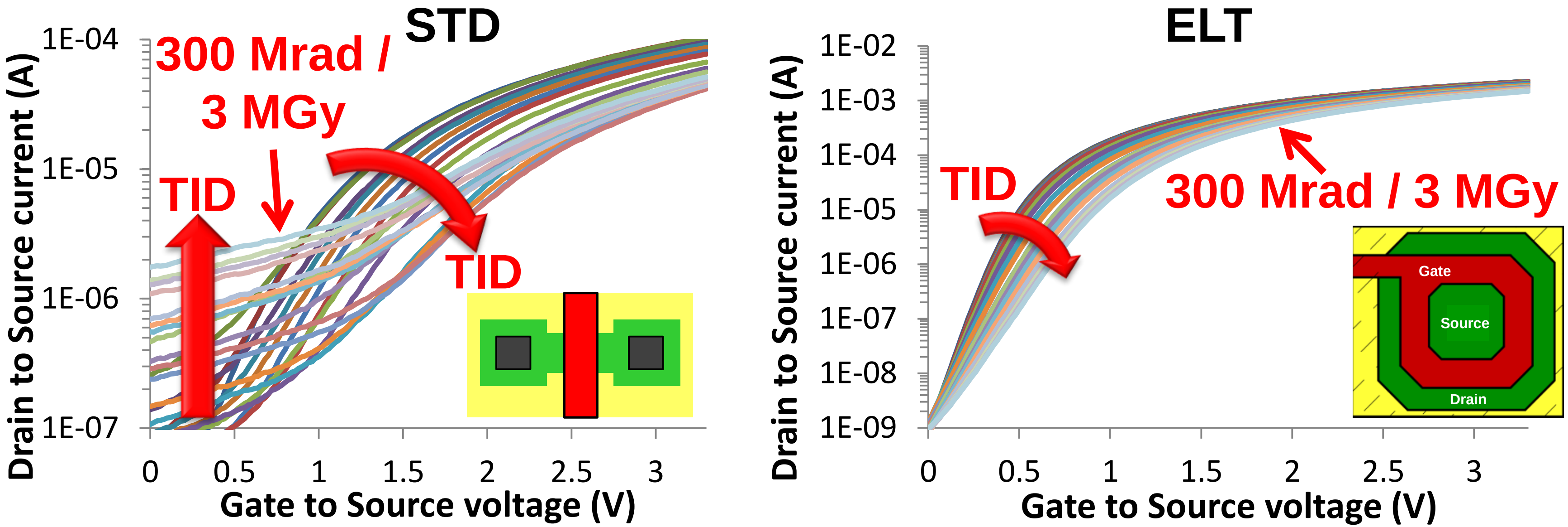
    → **no more STI related effects**
    - *No more RINCE*
    - *No more sidewall leakage*



- **Other enclosed geometry designs exist (see for exemple W. Snoeys et al, IEEE TNS, Aug. 2002.)**

***G. Anelli et al., IEEE TNS, 1999.**

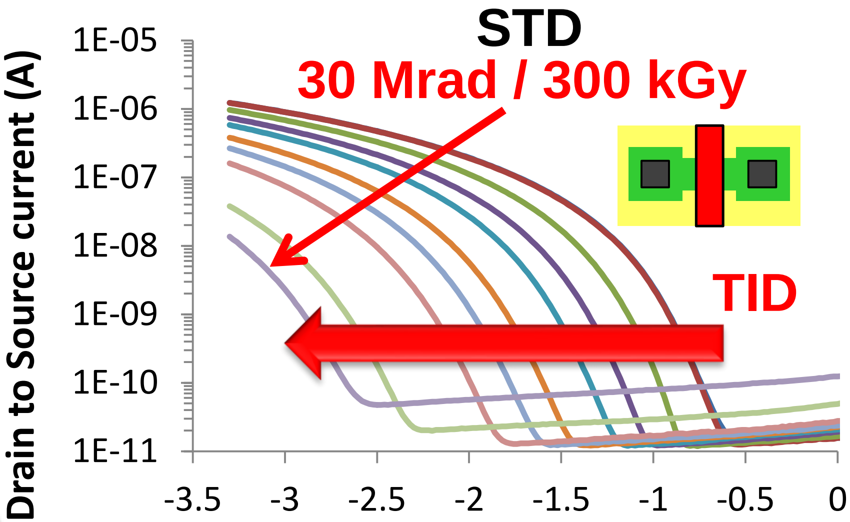
MGy/Grad irradiation effects on N-MOSFETs (180 nm CIS)

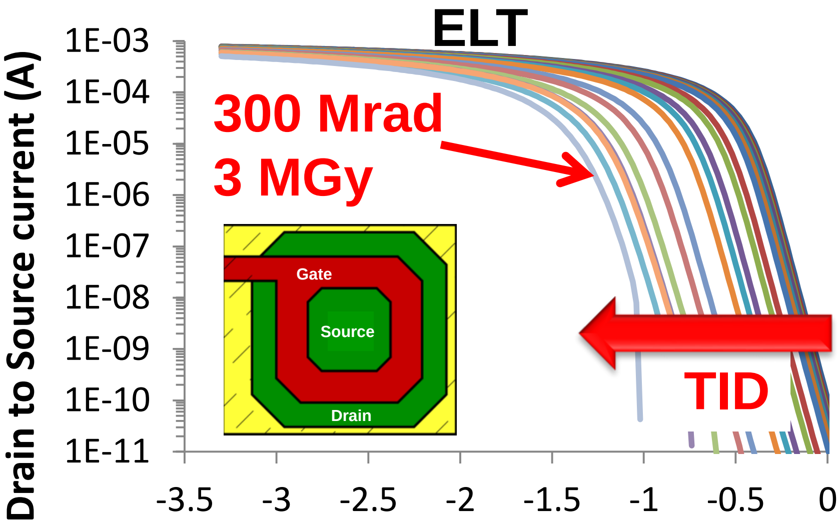


Courtesy of Marc Gaillardin (CEA DAM)

- **Standard N-MOSFET seriously degraded @ 100 Mrad / 1 MGy**
- **ELT mandatory to avoid RINCE and sidewall leakage**

MGy/Grad irradiation effects on P-MOSFETs (180 nm CIS)





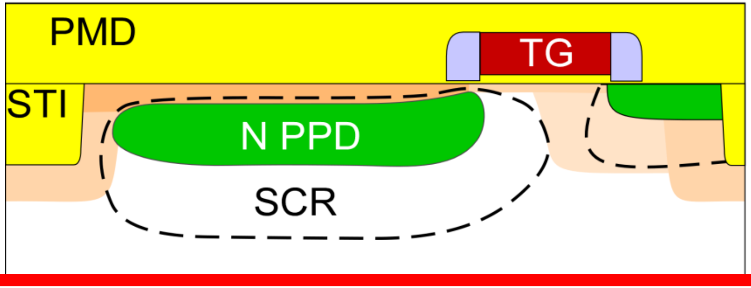
Courtesy of Marc Gaillardin (CEA DAM)

- **Standard P-MOSFET unusable after ≈ 10 Mrad / 100 kGy**
- **ELT mandatory to avoid RINCE**

MGy/Grad irradiation effects: Pinned PhotoDiode (PPD) (4T pixel)

Before Irradiation

- Depleted region well protected from the interfaces
- Ultra low dark current
- High Charge Transfer Efficiency (CTE)

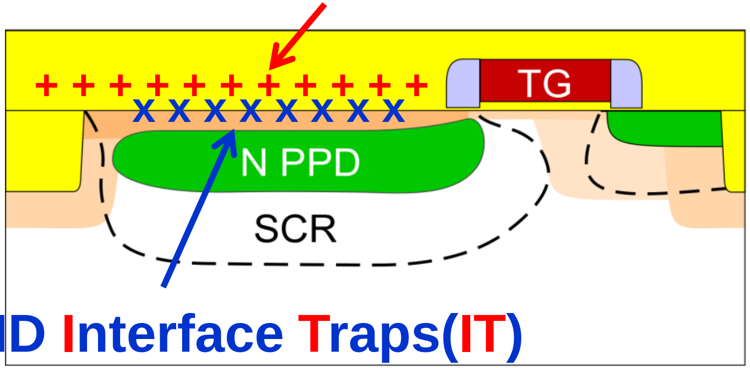


No Radiation-Hardening-By-Design Solution (thus far)

After Irradiation (high TID)

- Intense dark current
- Very poor CTE

PMD Oxide Trapped charge (OT)
➔Pinning layer depletion

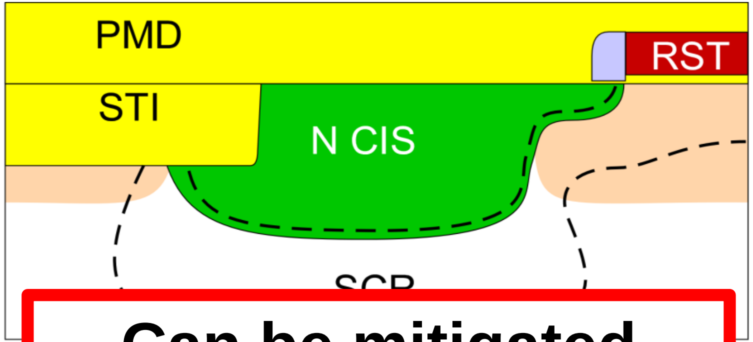


PMD Interface Traps(IT)
➔ Large dark current

MGy/Grad irradiation effects: Conventional Photodiode (3T pixel)

Before Irradiation

- Depletion region in contact with Si/SiO2 interface
- Higher dark current than PPD
- No CTE issue (no transfer)

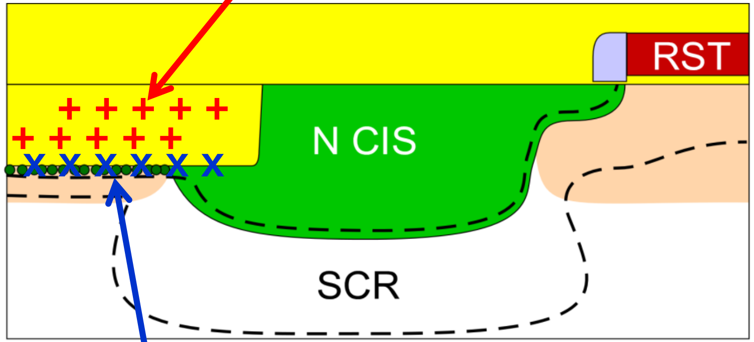


Can be mitigated by design!

After Irradiation (high TID)

- Short-circuit between diodes
- Intense dark current
- No CTE issue (no transfer)

STI OT
- ➔ **Large dark current**
- ➔ **STI inversion (short circuit)**



STI IT ➔ **Large dark current**

Basic TID radiation effects on CIS : a summary

- **For MGy range CIS design Enclosed Geometries are mandatory for both N and P MOSFETs**
  - But gate oxide can still induce a threshold voltage shift
    - *Due to OT or IT*
    - *In both N and P channel MOSFETs*
- **Both photodiodes (pinned and conventional) are serioulsy degraded by high levels of TID**
  - Large dark current increase
  - Loss of functionality

Conventional photodiode recommended for high TID!

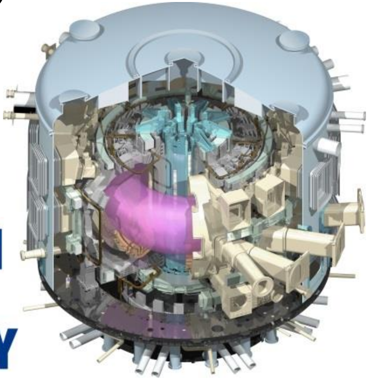
- **Radiation-Hardened-By-Design photodiodes are required:**
  - Solutions **only** exist **for conventional photodiodes**

TID effects/hardening illustration: ITER remote handling imaging system

ISAE SUPAERO

- **ITER remote handling operations require imaging systems**
  - Compact, lightweight and low power/voltage
  - Radiation hard (failure TID **>> 1MGy(SiO_2)**)
    - ***Gamma radiation only*** *(plasma OFF)*
  - Color and high definition (≥ 1Mpix)
- **Tube camera, not suitable because of**
  - Size, cabling, voltage, resolution and reliability
- **Existing solid-state image sensor based camera**
  - **Limited** by their radiation **hardness: ≤100 kGy**

FUSION FOR ENERGY

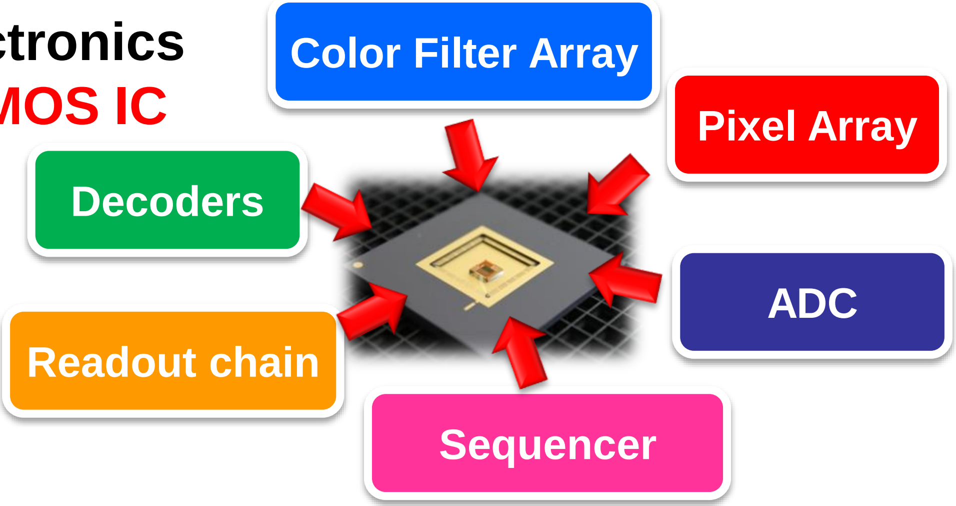


Dedicated development required

Camera Radiation Hardening Strategy

- **Integrate all the required electronics on a single Rad Hard (RH) CMOS IC**

RH Camera-on-a-Chip



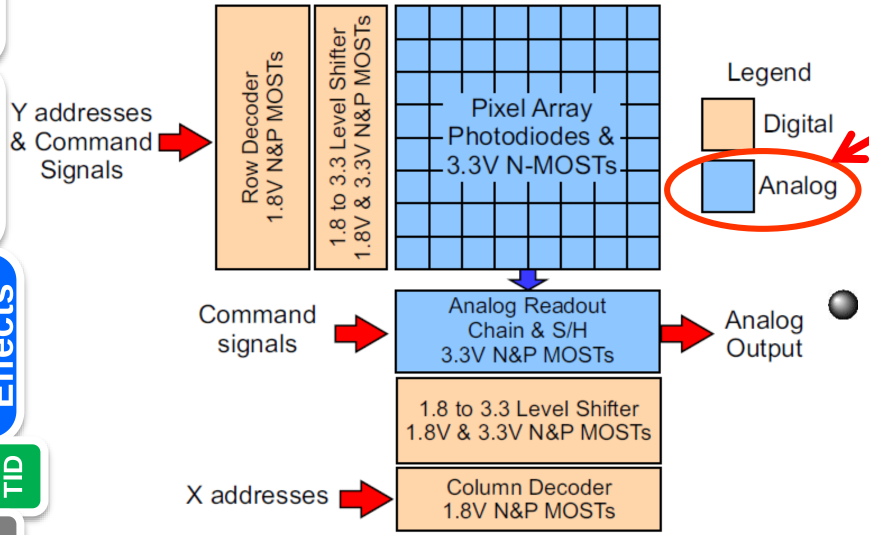
  - No need for additional MGy RH electronics
  - Very compact
  - Complete control of the radiation hardness

- **Associated RH developments**

  - Rad-Hard **optical system** (led by Univ. Saint-Etienne)
  - Rad-Hard LED based **illumination system** (led by CEA)

First technology evaluation demonstrator*

128x128 10µm pitch pixels



Most sensitive part: 3.3V analog circuits

FULL ELT DESIGN (N&P MOSTs)

180 nm commercial CIS technology (Europractice MPW)

- **Pure 1.8V digital and I/O pads: imec DARE 180 nm platform**

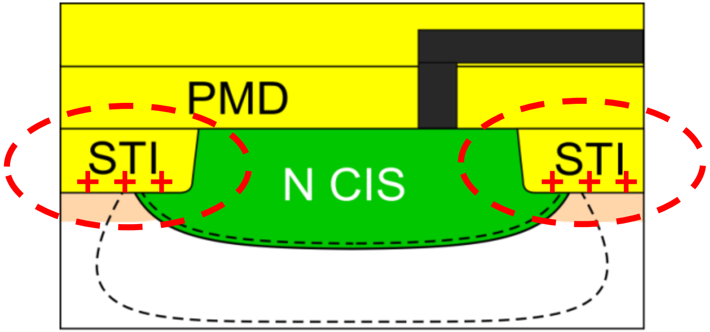
EUROPRACTICE imec

- **3.3V Analog/Mixed signal circuits and pixels ← Rad-Hard by ISAE**

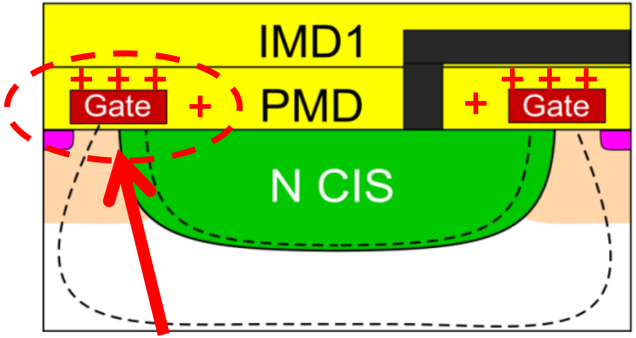
*V. Goiffon et al., IEEE TNS, Dec. 2015

CMOS Image Sensor (CIS) Design : photodiode radiation hardening

- **Issue with standard diode: peripheral oxide (STI here):**



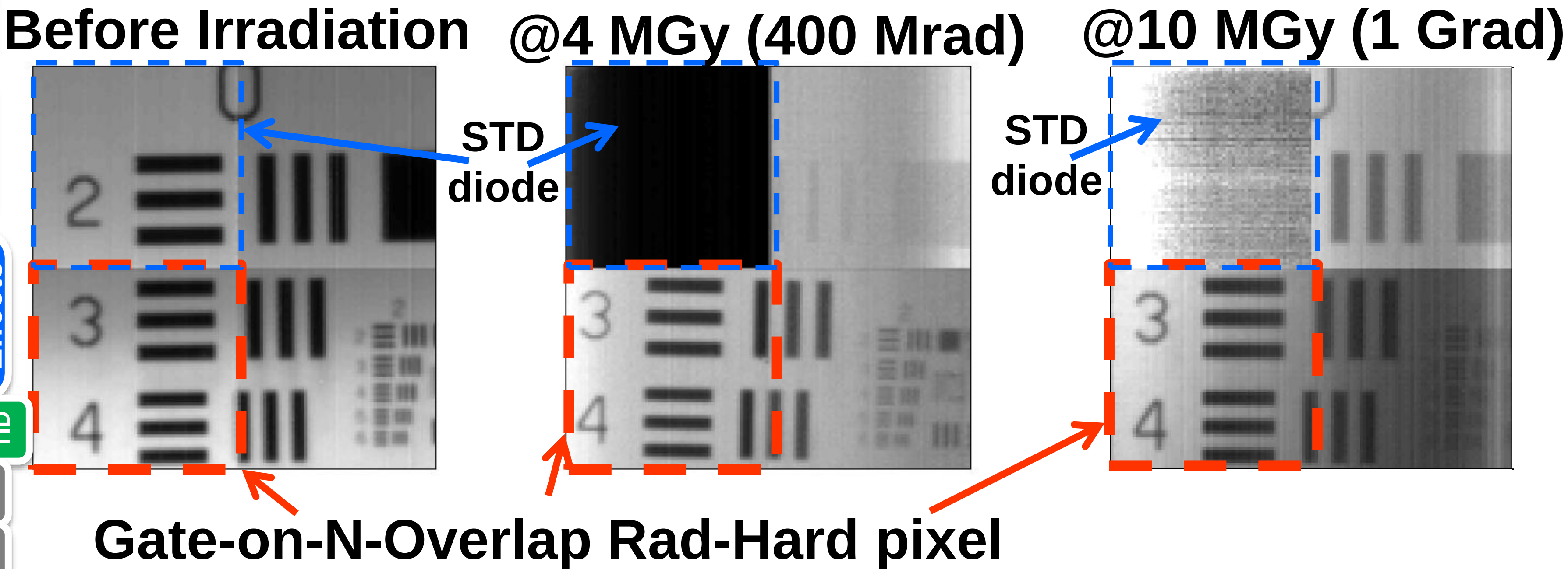
- **Selected RHBD technique: use of a polysilicon gate to shield the junction from the trapped positive charge:**
  - Principle of the gate diode



+ voluntary gate-to-N overlap to shield the junction

***V. Goiffon et al., IEEE TNS, Dec. 2015**

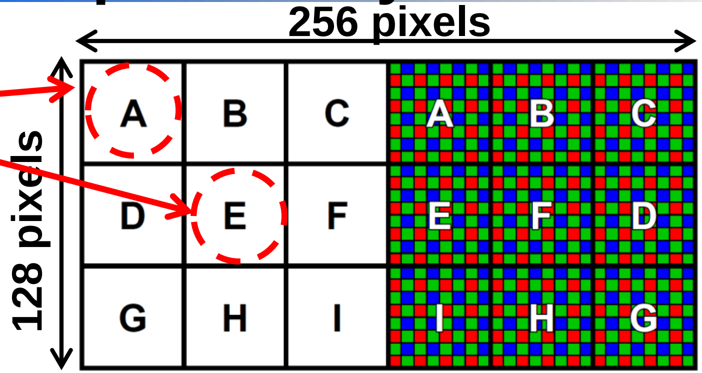
Post Irradiation Results: Raw Images (no image correction)



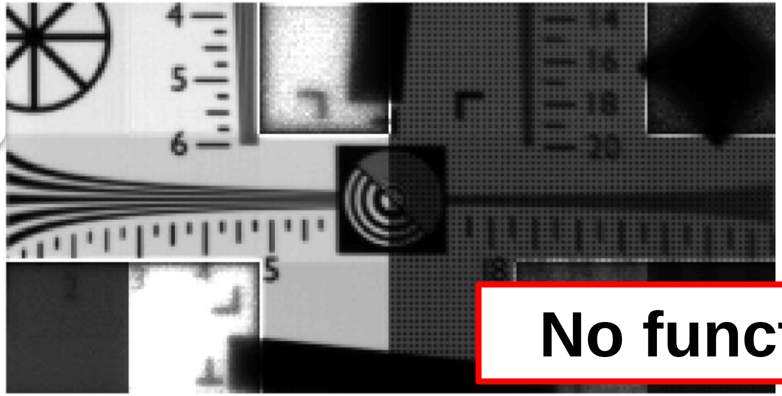
Acceptable image degradation even after 1 Grad (10 MGy)!

Second technology evaluation demonstrator: 1.8V RHBD pixel array

- Full 1.8V instead of 1.8/3.3V
- 9 pixel design variations
- Half of the sensor covered by a Color Filter Array (CFA)

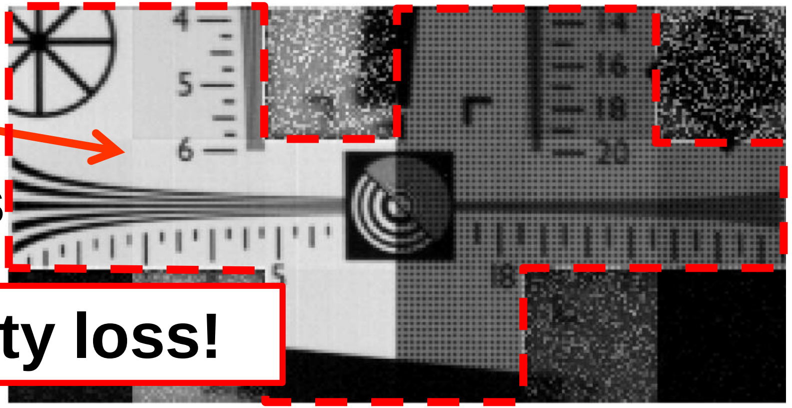


Raw images captured by the manufactured CMOS image sensor:



Rad-Hard pixels

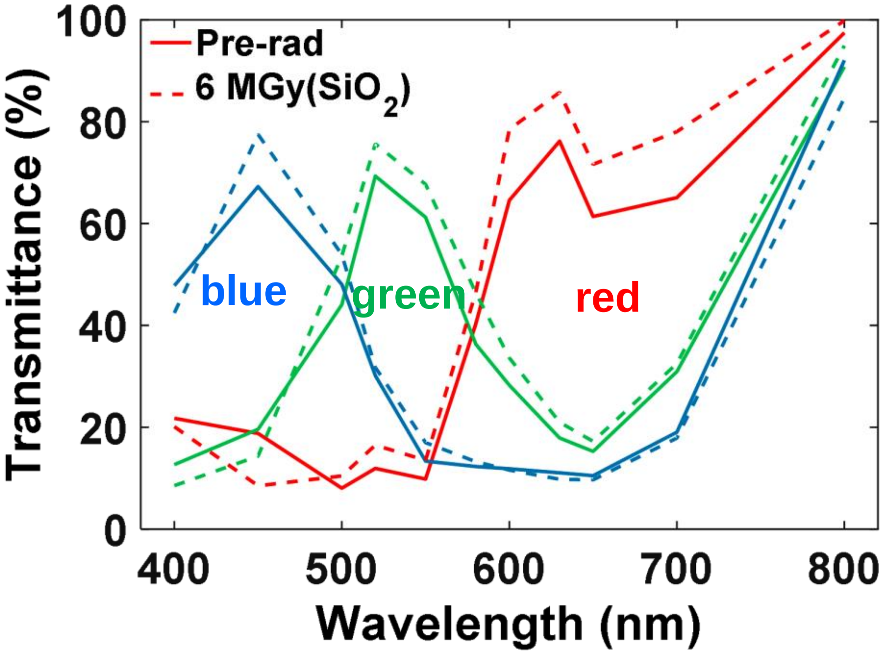
No functionality loss!



Unirradiated

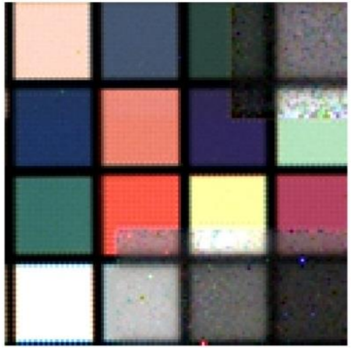
6 MGy(SiO_2) / 600 Mrad

Color Filter Array: Radiation Hardness Evaluation



Color images captured by the manufactured CMOS image sensor:

Unirradiated



6 MGy(SiO_2)

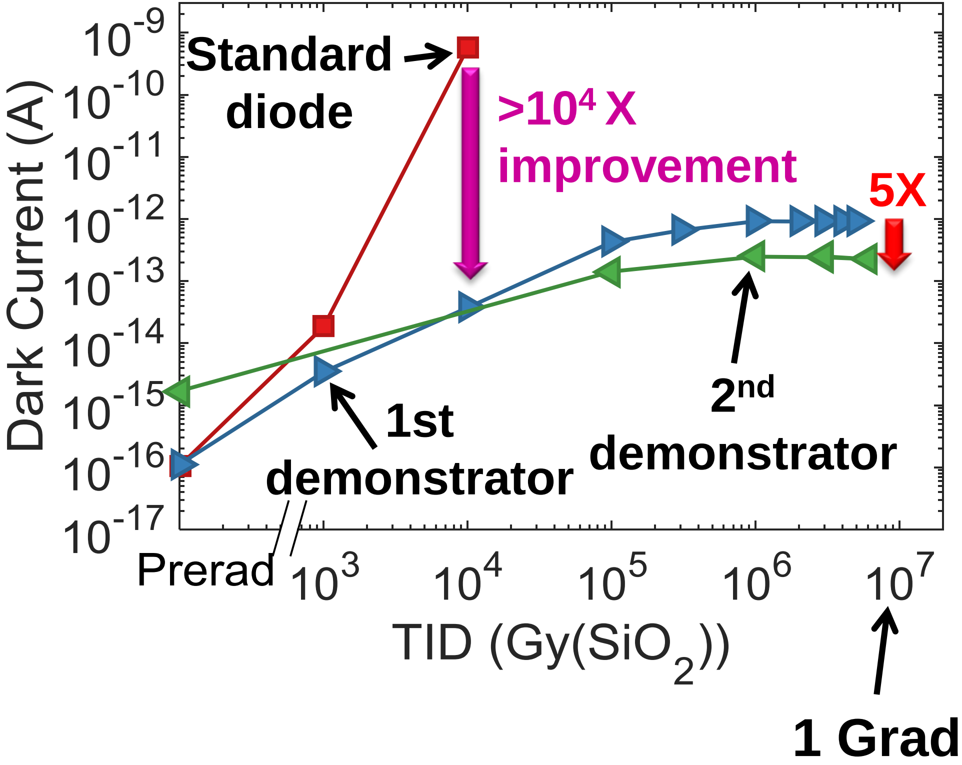
- **No significant color filter degradation**

***V. Goiffon et al., IEEE NSREC 2016**

Main Radiation Effects: Dark Current Increase

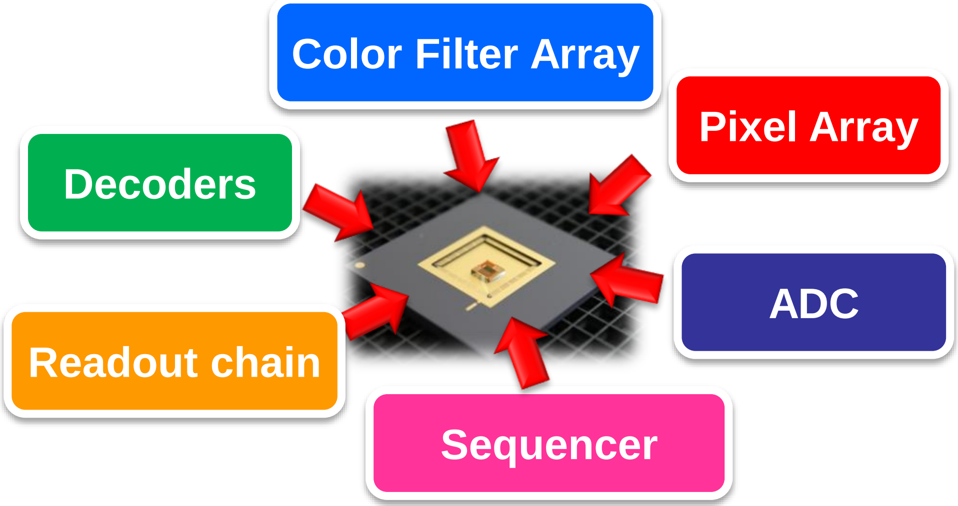
- Standard PD: 10^7X dark current rise @10kGy (1Mrad)
  - no longer functional at higher radiation dose
- Rad-Hard diodes **functional @ 6 MGy/600 Mrad**
- Factor of 5 improvement between the first and second demonstrator (5X dark current reduction)

22°C



*V. Goiffon et al., IEEE NSREC 2016

ITER Remote Handling Demonstrator

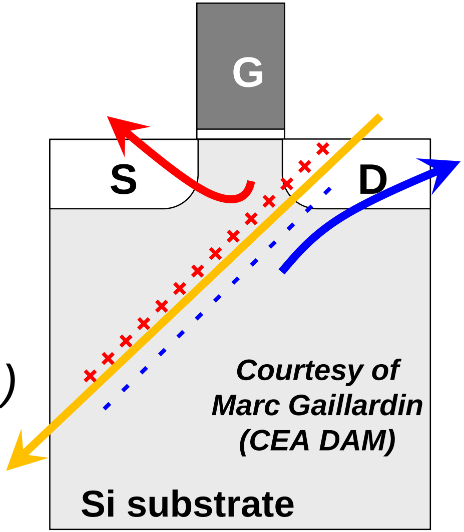


- **Multi MGy Rad-Hard Color Digital Camera-on-a-chip appears feasible**
- **First results are promising but development shall continue:**
  - **Integrate all the functions** in a single Rad-Hard HD sensor

Single Event Effects (SEE)

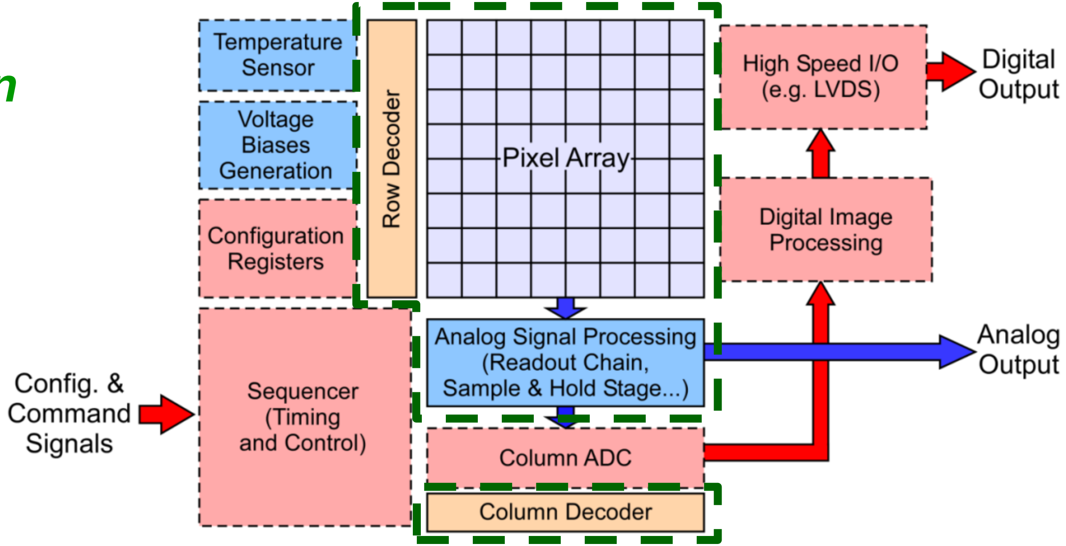
Single Event Effects in CIS: Basics

- **Single Event Effect (SEE) = perturbation/degradation caused by a single energetic particle**
- **Main mechanism:**
  - Generation of a high density of e^-/h^+ pairs along the particle track
  - Leading to:
    - *Transient perturbation (**Single Event Transient (SET)**)*
    - *Permanent change of a digital value (**Single Event Upset (SEU)**)*
    - *Triggering of a parasitic thyristor (**Single Event Lacthup**)*
    - *…and many other possible parasitic effects!*



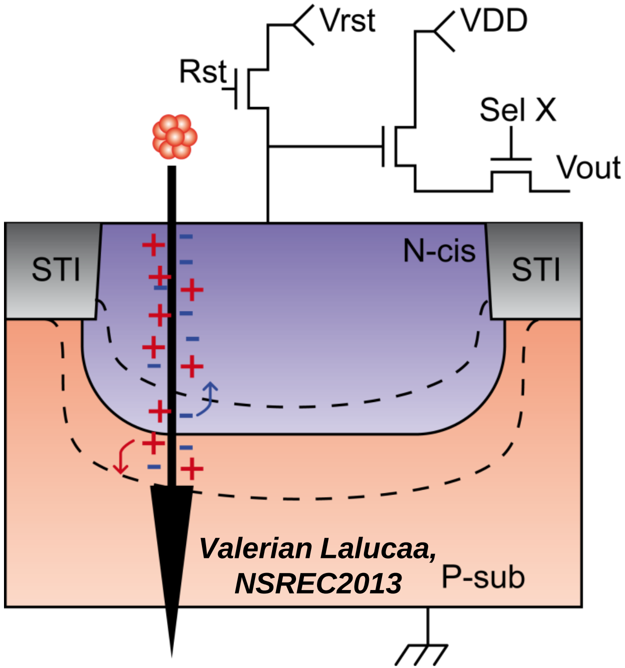
Single Event Effects in CIS: Basics

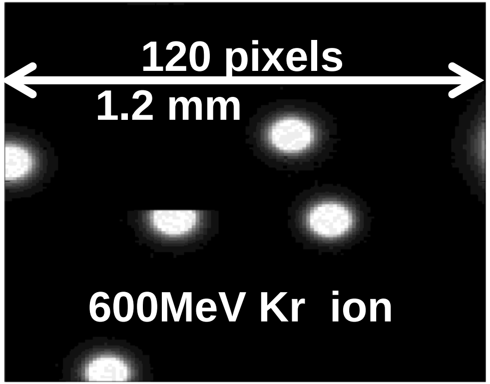
- **What kind of SEE CIS are sensitive to?**
  - **In theory: all kind**, as any CMOS Mixed-Signal Integrated Circuit
- **For this presentation, focus only on SEEs**
  - That are specific to CIS, i.e. SEEs in:
    - ***Pixel arrays***
    - ***Analog readout chain***
    - ***Decoders***
  - Other optional integrated functions are not discussed here

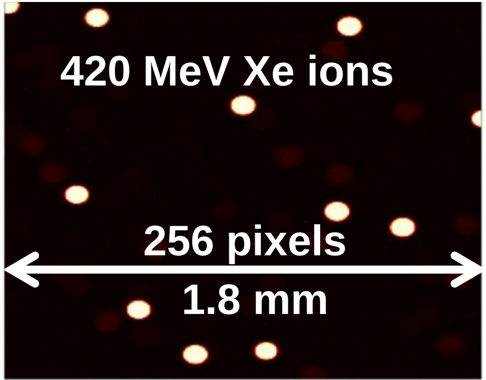


Single Event Effects in CIS: pixel array

- **For basic pixel architecture (3T/4T):**
  - No SEL (no in-pixel PMOSFET)
  - No SEU (no in-pixel memory)
  - **Only Single Event Transient (SET)**
- **SET: the ion induced charge is collected by the photodiodes leading to a parasitic signal :**
  - Spreading over several pixels
  - Lasting a single frame

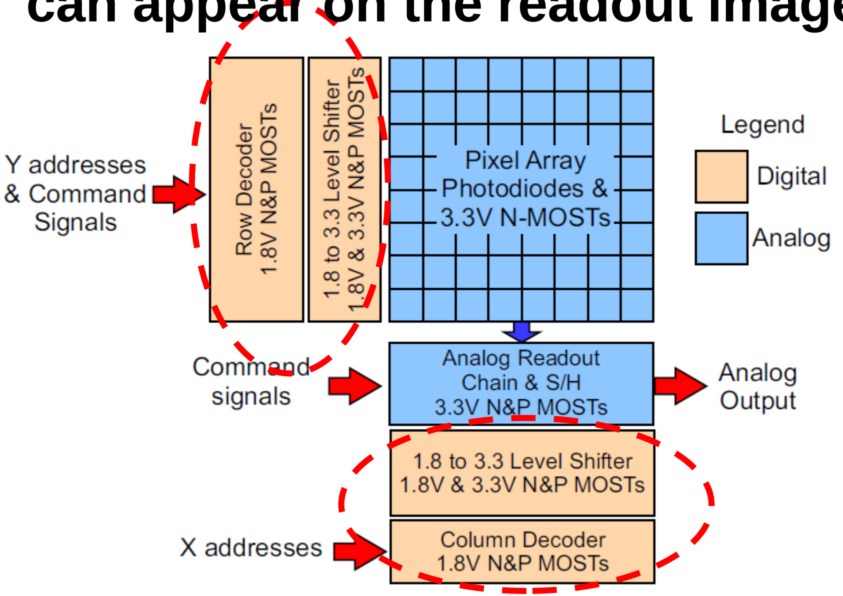


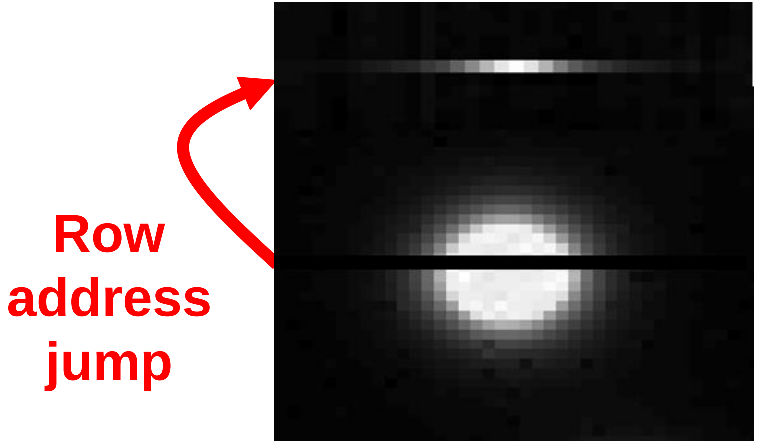




Single Event Effects in CIS: SET in decoders

- If an ion strike the decoders **during readout**, a transient artefact can appear on the readout image



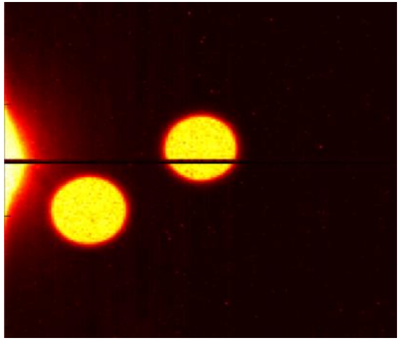


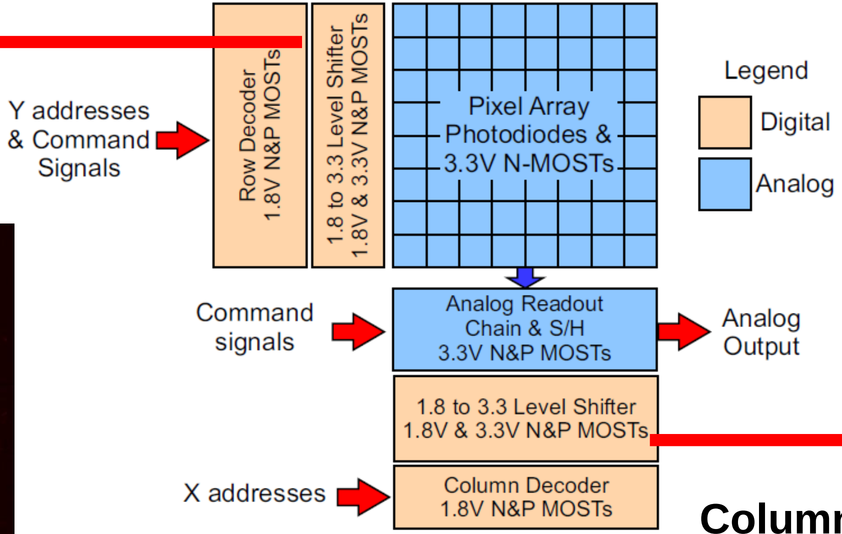
- Usually not an issue:
  - Low occurrence probability (compared to pixel SET)
  - Transient effect that disappears on the next frame

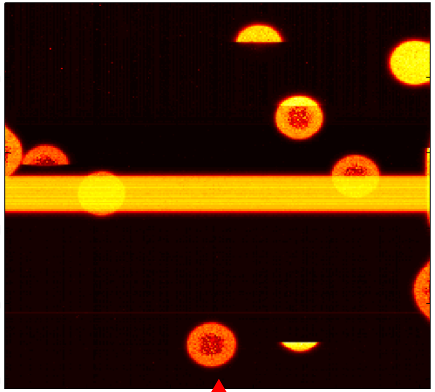
Single Event Effects in CIS: SEL in decoders

- **Latchup can also occur in decoders leading to permanent artefact**
  - CIS are often immune to such SEL thanks to thin epitaxial layer
  - Generally disappears after powering OFF and ON the sensor (no permanent damage)

Row decoder SEL



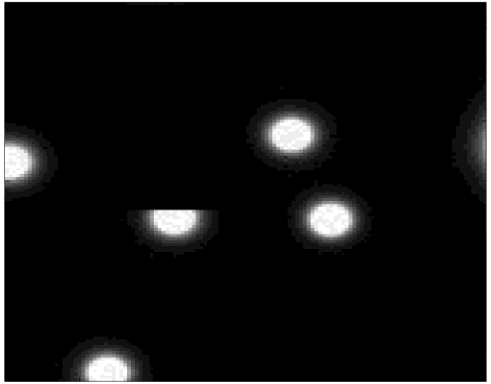




Column decoder SEL

Single Event Effects in CIS: a summary

- **In CIS required integrated functions :**
  - The **main SEE** are **Single Event Transients** (SET) in **pixel array**

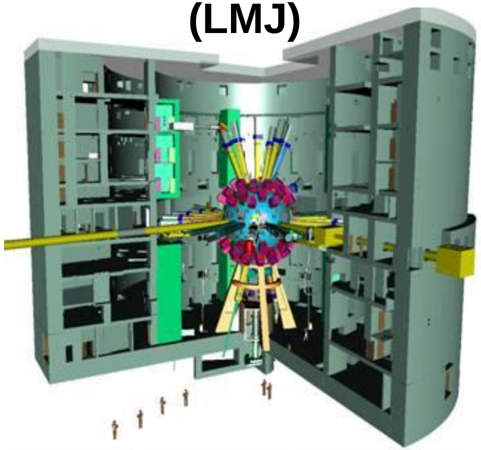


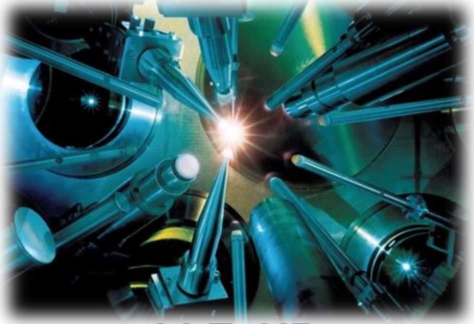
  - Other effects are **generally not an issue**:
    - *SET in decoders or readout chain are infrequent and only corrupt one pixel or one row of a single frame*
    - *CIS are generally immune to SEL and if not:*
      - *Can be powered OFF to recover (if non-destructive)*
      - *Can be hardened-by-design*
  - **SEE in additional integrated functions** (e.g. SEU in on-chip sequencers) **can be an issue**
    - *Requires a specific analysis of each additional CMOS function*
    - ***Not a problem for basic CIS*** *without such functions*

Illustration: MegaJoule (MJ) Class Inertial Confinement Fusion (ICF) Plasma Diagnostic

- **Plasma diagnostics in MJ class ICF facilities radiation environment during each laser shot:**
  - 14 MeV neutrons
  - Expected fluence: 10^{12} n.cm^{-2}
  - Estimated flux > 10^{18} n.cm^{-2}.s^{-1}
- **Existing Plasma Diagnostics cannot withstand these conditions**
- **A X-ray Plasma Diagnostic demonstrator has been developed (with CEA DAM and UJM) to demonstrate the potential of CIS for this application**

LaserMegaJoule (LMJ)

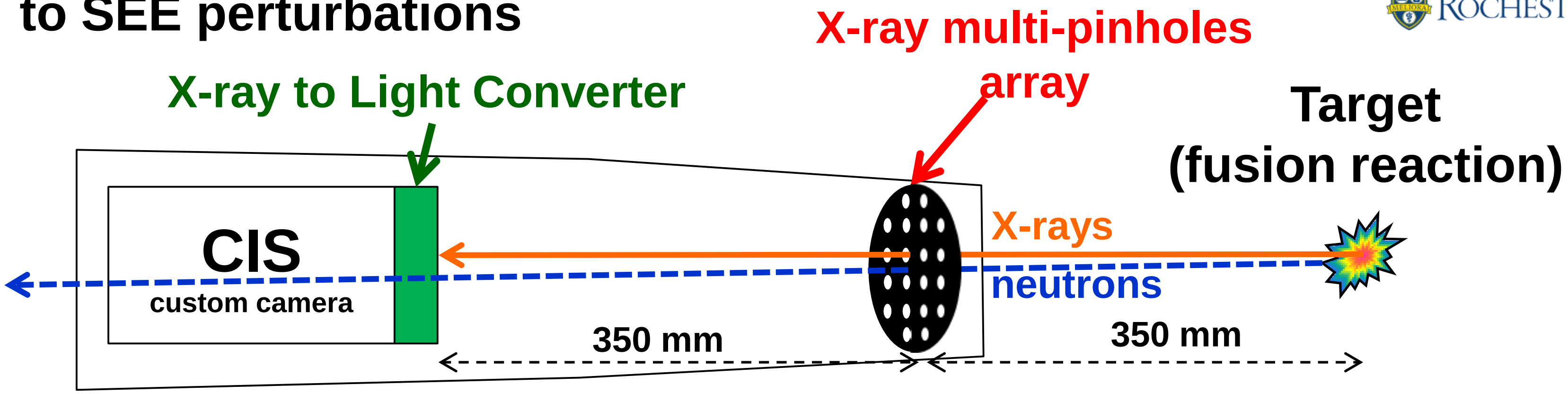




LLE, UR

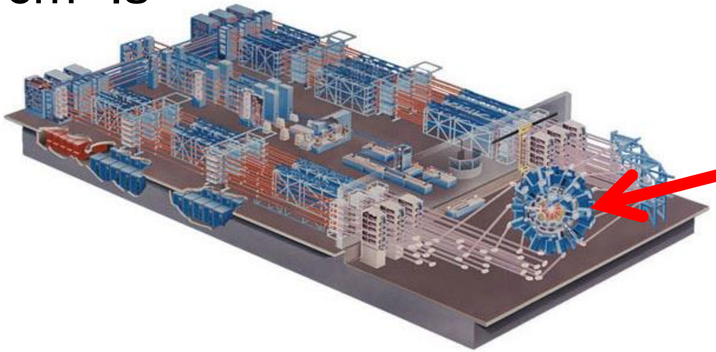
ICF X-ray Plasma Diagnostic principle

- **At LLE OMEGA facility: 60 laser beams (40kJ) focus on a 1 mm target during 1 ps leading to a fusion reaction**
- **The X-ray signal emitted by the fusion plasma is imaged through:**
  - A Multi-pinholes array thanks to an X-ray-to-light converter deposited on top of the CIS
- **An intense neutron pulse is also generated leading to SEE perturbations**



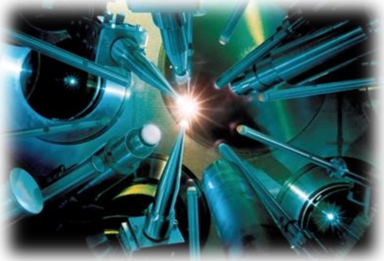
ICF X-ray Plasma Diagnostic principle

- Several experiments performed since 2010 at the Laboratory for Laser Energetics of Univ. Rochester, NY
- To approach MegaJoule class ICF experiment conditions, the diagnostic demonstrator is inserted directly inside the target chamber
  - As close as possible to the target (35 cm)
  - Maximum neutron flux reached at CIS level $\approx$ a few 10^{18} $cm^{-2}.s^{-1}$

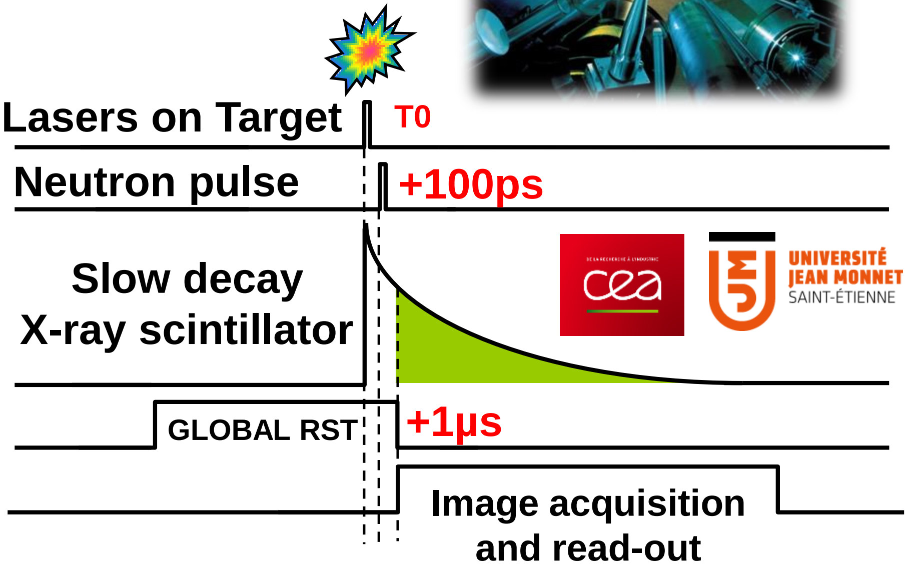


ICF X-ray Plasma Diagnostic Demonstrator: Hardening Approach

- **Hardening at the sensor level:**
  - Selection of a **simple and robust CIS architecture** with only the required on-chip functions **to reduce SEE sensitivity**
  - No real use of RHBD technique for this application

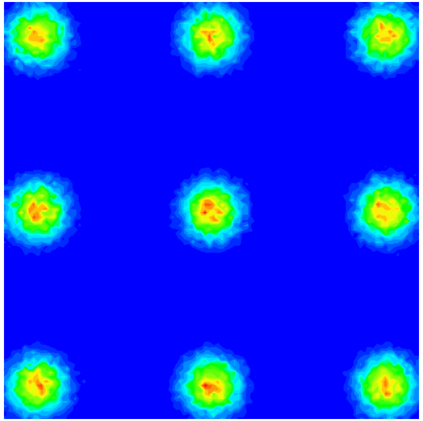


- **System level hardening:**
  - Delay the acquisition of the X-ray plasma image to avoid the neutron pulse perturbation
  - Use of a slow Radiation-to-Light Convertor
  - **Dump all the parasitic charge** with a global reset feature
  - Only perform **critical operations** (ADC, data transmission) **after the neutron pulse**

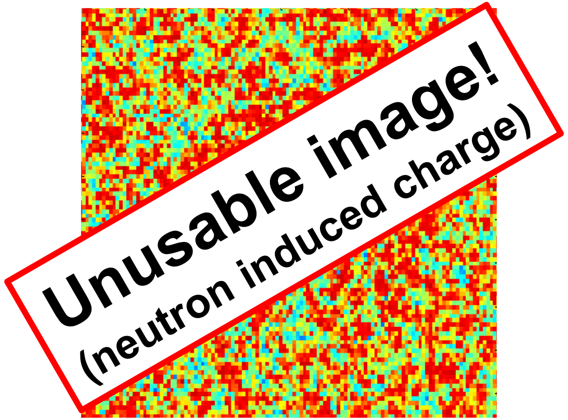


ICF X-ray Plasma Diagnostic Demonstrator: Results

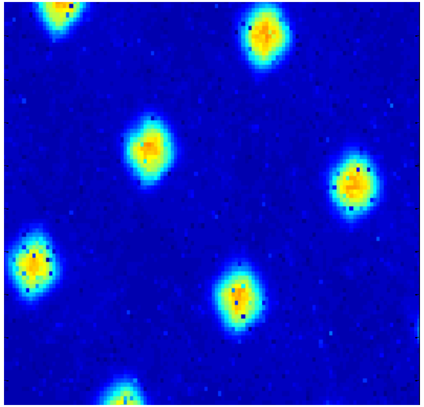
Expected result (simulation)



Without "global reset" mode



With "global reset" mode



- **No SEE, no functionality loss:**
  - full camera design **robust to several 10^{18} cm^{-2}.s^{-1}**
- **GR mode efficiently removes the neutron induce parasitic signal**
- **Ability of CIS based camera to capture an image at such a high neutron flux demonstrated**

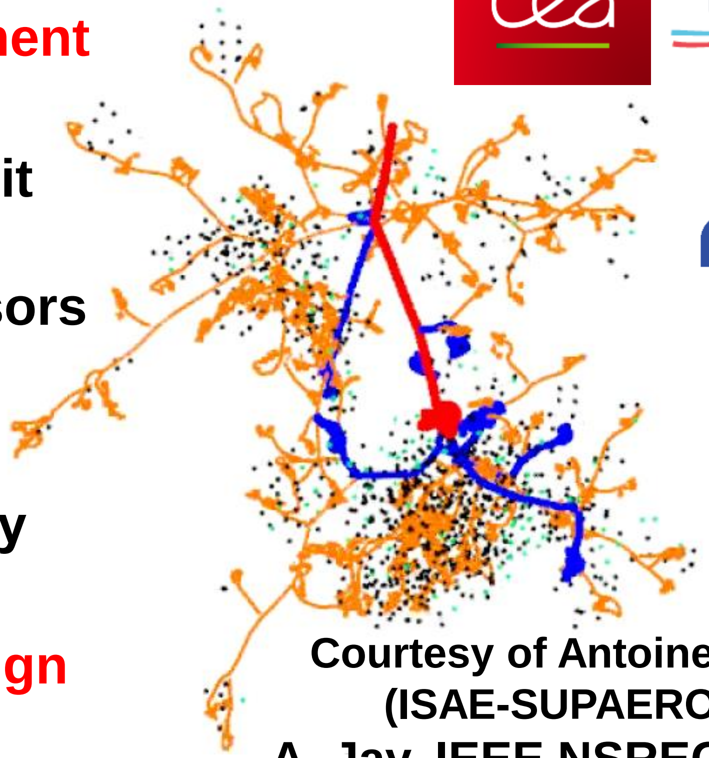
Displacement Damage (DD) effects

Displacement Damage (DD) Effects on CIS

- **DD = result of non-ionizing interactions leading to displacement of silicon atoms**
- **Contrary to TID, DD effects exhibit an almost universal behavior in silicon based detectors and sensors**

➡ DD effects **can be anticipated** accurately in most CIS

- **DD effects can be "modulated" by design optimization…**
- **…but not really mitigated by design**

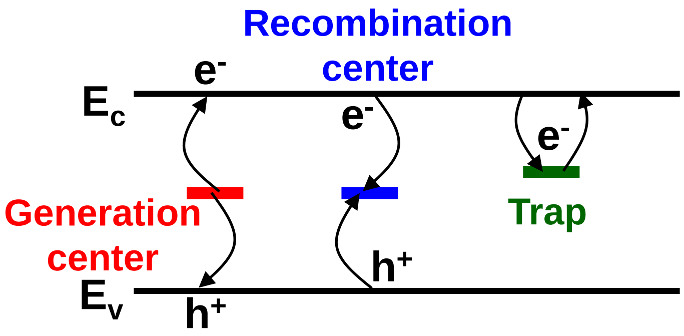


Courtesy of Antoine JAY (ISAE-SUPAERO)

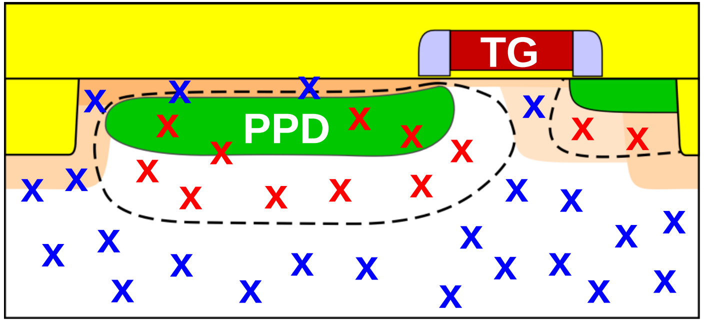
A. Jay, IEEE NSREC 2016

Displacement Damage Effects on CIS: Basics

- **DD effects lead to the creation of SRH centers**
  - Can act as **generation/recombination** centers or as charge trap



- **Main effects originating from the photodiodes:**
  - Dark current increase (defect x in depletion region)
  - Possible quantum efficiency reduction due to recombination centers x (usually not observed)



x **SRH generation centers**

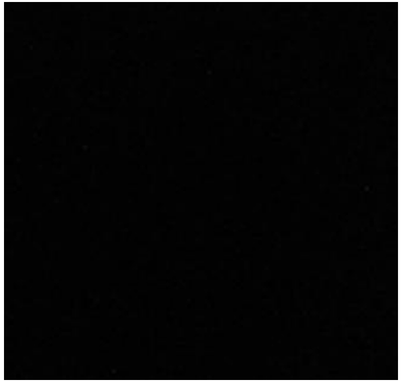
x **SRH recombination centers**

- **Not considered:**
  - Charge trapping : no proven effect in CIS
  - Type inversion* : not likely in CIS for typical fluences (<10^{14} n/cm²)

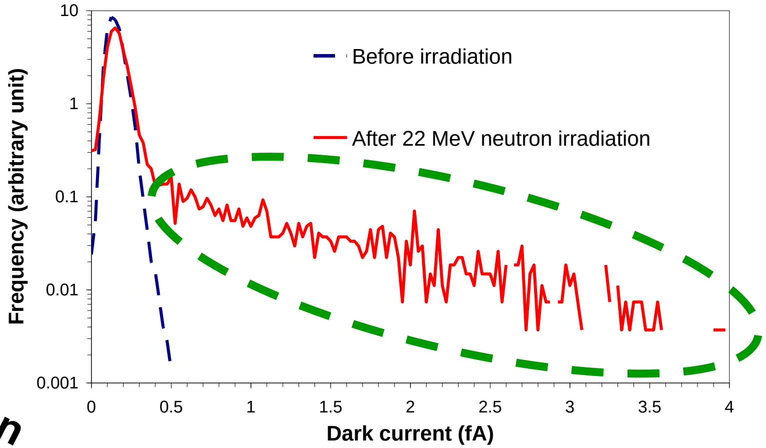
***M. Moll PhD. Thesis, 1999**

Displacement Damage Induced Dark Current Increase

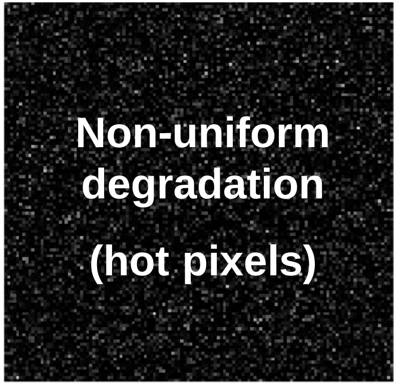
Dark frame no irradiation



Neutron irradiation (DD effects only)



^{60}Co γ-ray irradiation (TID effects only)



Displacement Damage Effects on CIS: Universal Damage Factor

- **Srour et al. 2000* Universal Damage Factor applied to CIS**

$$\Delta I_{obs} = q \cdot K \cdot V_{dep} \cdot D_{dd}$$

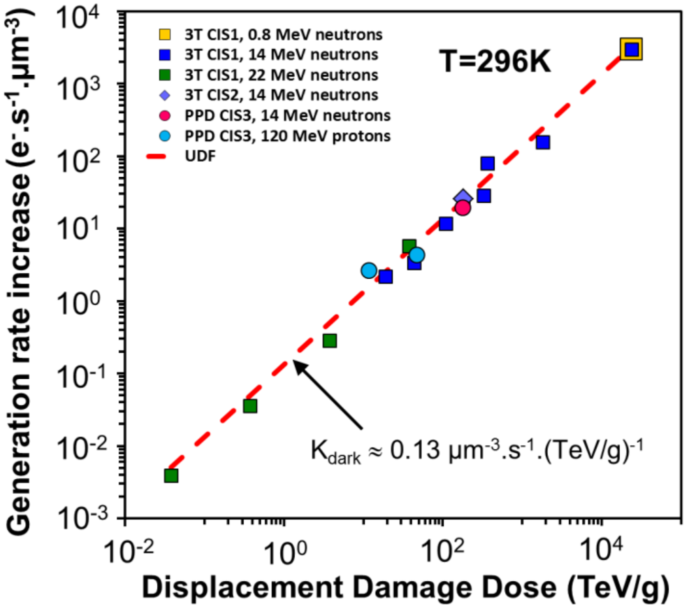
Damage Factor (K)

Displacement Damage Dose (D_{dd})

Mean dark current increase (ΔI_{obs})

Depletion volume (V_{dep})

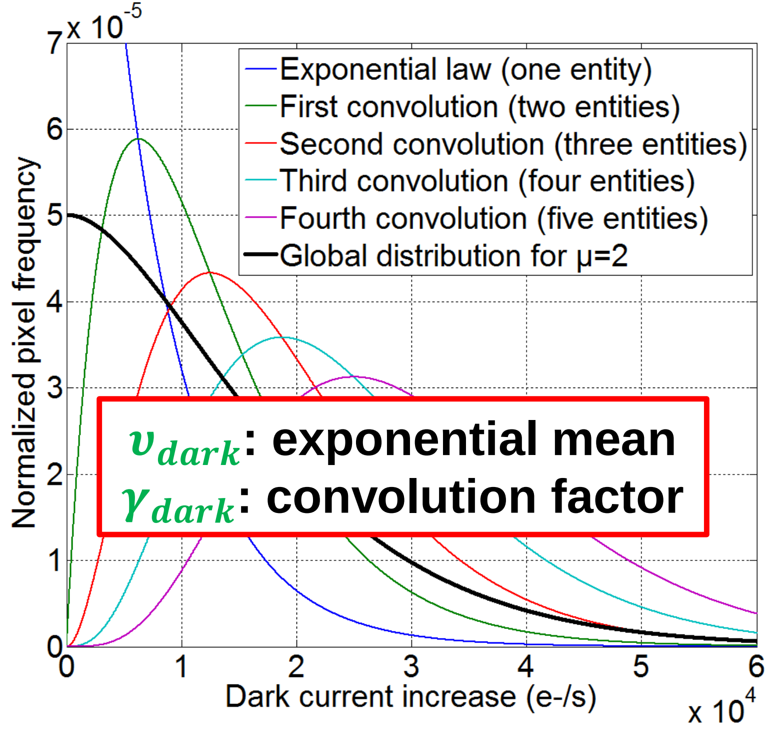
- **No fitting parameter**
- **At 23°C:** $K = 1.4 \pm 0.5 \ \mathrm{cm}^{-3} \cdot \mathrm{s}^{-1} \cdot (\mathrm{MeV/g})^{-1}$
- **Verified on CIS from many foundries up to 10^{13} n/cm²**



C. Virmontois et al., IEEE TNS Aug. 2012

***J.R. Srour and D. H. Lo, IEEE TNS, Dec. 2000.**

Displacement Damage Effects on CIS: Empirical Prediction Model*



υ_{dark}: exponential mean
γ_{dark}: convolution factor

- **Exponential** dark current **Probability Density Function (PDF)** for low doses and small volumes (one dark current source per pixel):

$$f_{\upsilon_{dark}}(x) = \frac{1}{\upsilon_{dark}} \exp\left(-\frac{x}{\upsilon_{dark}}\right)$$

- **Convolution** of the PDF at higher doses and larger volumes (superimposition of several dark current sources per pixel):

$$f_{\Delta I_{obs}}(x) = Poisson(k=1,\mu) \times f_{\upsilon_{dark}}(x) + Poisson(k=2,\mu) \times f_{\upsilon_{dark}}(x) * f_{\upsilon_{dark}}(x) + \cdots$$

- $\boldsymbol{\mu = \gamma_{dark} \times V_{dep} \times DDD}$ is the convolution parameter and represents the **mean number of sources per pixel**

***Virmontois et al., IEEE TNS, Aug. 2012**
***Belloir et al., Optics Express, Feb. 2016**

Displacement Damage Effects on CIS: Empirical Prediction Model

- **In the same way as the Universal Damage Factor, the two parameters of this empirical model υ_{dark} and γ_{dark} :**
  - Appear to be constant for neutron/protons/ions of a few MeV to 500 MeV
- **In practice, this empirical model can be used to anticipate the absolute DD induced dark current distribution**
  - Without any parameter adjustment
- **Parameter values**

Average dark current per source

$\upsilon_{dark} \approx$ **5000 e-/s @ 23°C**

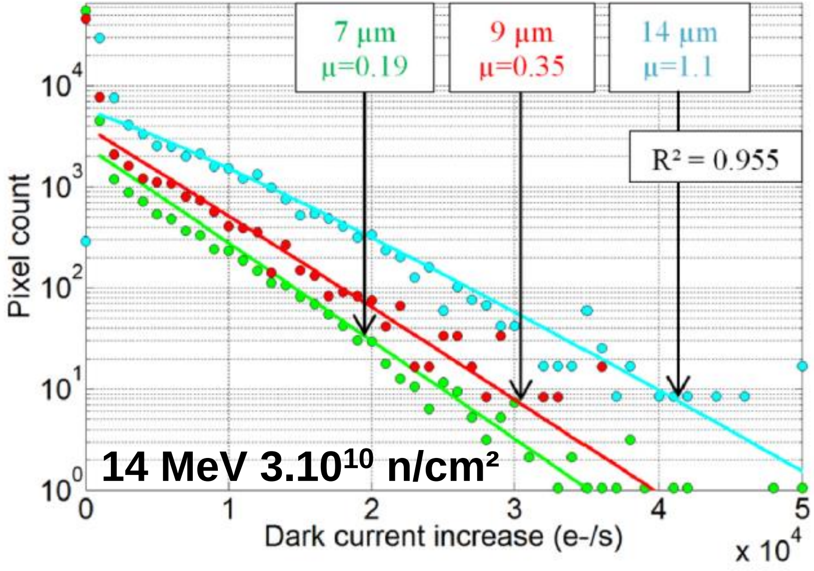
$\gamma_{dark} \approx \frac{1}{50{,}000}$ **µm^{-3} (TeV/g)$^{-1}$**

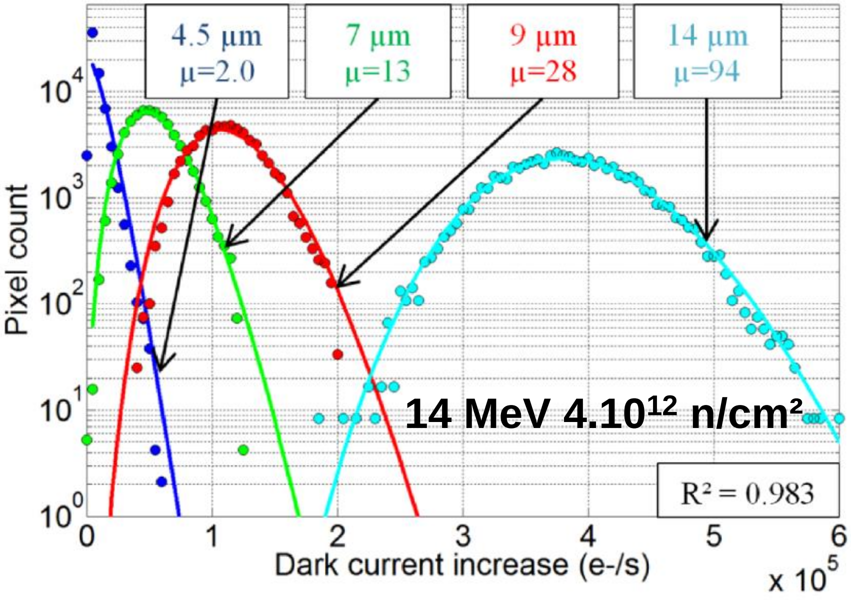
1 source per pixel for a dose of 500 TeV/g in a 100 µm^3 depleted volume

***Belloir et al., Optics Express, Feb. 2016**

Displacement Damage Effects on CIS: Empirical Prediction Model

- **Typical results of the prediction model:**
  - 4 CIS with 4 different pixel pitches (4.5 / 7 / 9 and 14 µm)
  - At low (3.10^{10}) and high (4.10^{12}) fluence





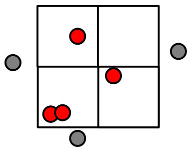
***Belloir et al., Optics Express, Feb. 2016**

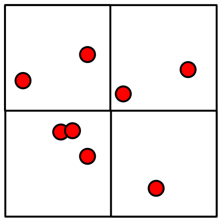
Displacement Damage (DD) Effects on CIS: A summary

- **Main DD effects in CIS up to 10^{13}-10^{14} n/cm²:**

Dark Current Increase

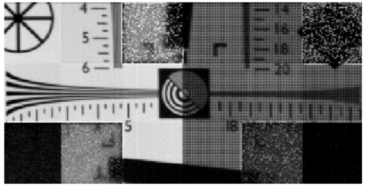
- **DD induced Dark Current increase can be anticipated by using:**
  - Srour Universal Damage Factor for the mean value
  - The presented empirical model for the full distribution
- **These models can be used to optimize the design to modulate the effects (no real mitigation possible by design):**
  - Small depletion volume ➔ lower mean dark current, larger non-uniformities
  - Large depletion volume ➔ higher mean dark current but less non-uniformity





System level mitigation: cooling!

Talk Summary



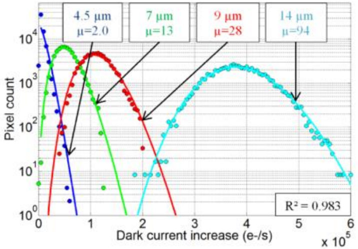
- **MGy-Grad Total Ionizing Dose effects on CIS**
  - Large dark current increase and MOSFET voltage shifts
  - All these effects can be partially mitigated by design
    - *Use of ELT and conventional photodiode recommended*

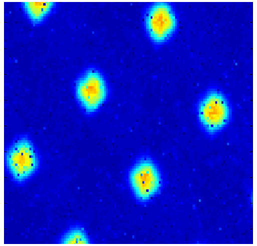
➡ **Radiation hardened CIS can provide useful images** after several MGy

- **High flux Single Event Effects (SEE) in CIS :**
  - Main issue: transient deposited parasitic charge (SET)
  - Other SEEs can be avoided by sensor or system design

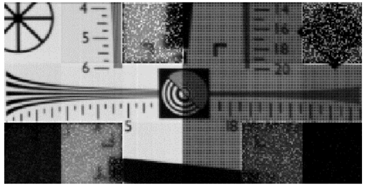
➡ CIS based camera can stand neutron flux up to 10^{18} n.cm^{-2}.s^{-1}

- **High fluence displacement damage effects in CIS**
  - Main effect : dark current increase
  - Can be predicted up to 10^{14} n/cm² and mitigated at system level (e.g. cooling)





Talk Summary



- **MGy-Grad Total Ionizing Dose effects on CIS**
  - Large dark current increase and MOSFET voltage shifts
  - All these effects can be partially mitigated by design
    - *Use of EL*

→ **Radiation ha** … after several MGy

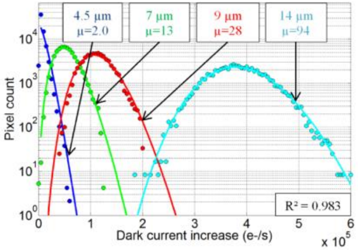
- **High flux Single**
  - Main issue: t
  - Other SEEs … n

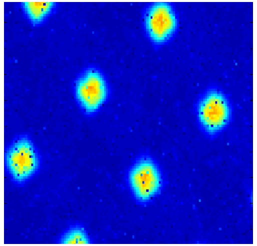
→ CIS based camera can stand neutron flux up to 10^{18} n.cm^{-2}.s^{-1}

In a nutshell:

- **The main issues (TID/SEE/DD) come from the photodiode**
- **CIS are a good choice for harsh radiation environments!**

- **High fluence displacement damage effects in CIS**
  - Main effect : dark current increase
  - Can be predicted up to 10^{14} n/cm² and mitigated at system level (e.g. cooling)





contact: vincent.goiffon@isae.fr

Thank you!

want to know more?

V. Goiffon, "Radiation Effects on CMOS Active Pixel Image Sensors," in Ionizing Radiation Effects in Electronics: From Memories to Imagers (CRC Press, 2015), ch. 11, pp. 295–332.