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Miniaturized Low-Voltage Power Converters with Fast Dynamic Response

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Abstract - This paper demonstrates a two-stage approach for power conversion that combines the strengths of variable-topology switched capacitor (SC) techniques (small size, light-load performance) with the regulation capability of magnetic switch-mode power converters. The proposed approach takes advantage of the characteristics of CMOS semiconductor processes, and the resulting designs provide excellent efficiency and power density for low-voltage power conversion. These power converters can provide low-voltage outputs over a wide input voltage range with very fast dynamic response. Both design and fabrication considerations for highly-integrated CMOS power converters using this architecture are addressed. The results are demonstrated in a 2.4 W dc-dc converter implemented in a 180 nm CMOS IC process and co-packaged with its passive components for high performance. The power converter operates from an input voltage of 2.7 V to 5.5 V with an output voltage of ≤ 1.2 V, and achieves a 2210 W/inch^3 power density with ≥ 80% efficiency.

I. INTRODUCTION

The advent of portable electronics and low-voltage digital circuitry has created a need for improved dc-dc converters. Power converters that can provide a low-voltage output (< 2.0 V) regulated at high bandwidth while drawing energy from a wide-ranging (≥ 2:1 range), higher-voltage input are particularly useful for supplying battery-powered portable electronics. Unfortunately, the power converters for these applications often account for an undue portion of system size, owing especially to the passive energy storage components needed for the conversion process. Moreover, the size, cost, and performance advantages of integration make it desirable to integrate as much of the dc-dc converter as possible, including control circuits, power switches, and even passive components, on die and/or into a surface-mount package. In this paper, we treat the design and packaging of low-voltage power converters to address these

issues. The proposed approach is based on a two-stage power conversion architecture integrated on a single CMOS die and co-packaged with the passive components to form a miniaturized, integrated surface mountable power converter.

Two-stage converters have recently been developed to try to address the fundamental limitations of single-stage converters in this general space. We begin by reviewing examples of this general approach, some of which have only been published in academic journals while others are in commercial products. To be consistent, we focus on low-voltage step-down versions of such two-stage converters. The most basic type of two-stage converter is a cascade of two switched-mode power converters, such as a higher-voltage buck converter followed by a lower-voltage buck converter [1]. This alleviates the issues with large step-down ratios, but increases the solution size by requiring the use of two large inductors rather than one large inductor as in the single-stage solution. To address this issue, Sun introduced the idea of using an unregulated and very efficient SC voltage divider in place of the front-end buck converter [2]. The SC voltage divider had a fixed two to one voltage transformation ratio allowing the use of lower-voltage switches in the second-stage buck converter. Unfortunately, with a fixed voltage divider, the power converter is not efficient over a wide input voltage range. As proposed in [3], [4] and [5], this can be solved by utilizing a SC converter with multiple distinct voltage conversion ratios that are selected based upon the input voltage.

It has also been shown that performance in SC/magnetic two-stage converters can be enhanced beyond that of a simple cascade of stages. As shown in [3], [4], [6] and [7], merging the structure and operation of the SC and magnetic stages (e.g., by eliminating or greatly reducing the capacitor between the two stages and controlling the circuit appropriately) can be highly advantageous. In a well-formed design of a “merged two-stage” converter, the capacitors within the SC converter can be soft charged, thereby reducing the charge redistribution losses among the capacitors within the SC portion of the converter, enabling reductions in capacitor size and/or improvements in efficiency.

Other two-stage or quasi-two-stage converters are also possible. Instead of placing an unregulated voltage divider (such as an SC converter) in front of a switching regulator, it is also possible to place the unregulated voltage divider after the switching regulator. Vicor Corporation has developed such a system [8]. Instead of connecting two stages in series, it is also possible to

connect the two stages in parallel as in the Quasi-parallel or Sigma architecture [9]. Each of these approaches has benefit in some applications. However, designs that are amenable to implementation with the semiconductor devices and controls on a single CMOS die with co-packaged passive components may offer the greatest benefit in many modern battery-powered applications.

This paper investigates and demonstrates a two-stage power conversion approach suitable for "power supply in package" (PSIP) converters for powering logic devices in battery-operated applications. The proposed approach addresses the need for achieving extremely high power density, wide input voltage range, low-voltage output, and high control bandwidth. We consider a two-stage design approach incorporating a variable-conversion-ratio SC stage and a high-frequency (HF) synchronous buck converter stage implemented on a single die, and co-packaged with the power converter passives. The paper addresses both design techniques and packaging methods, and demonstrates the proposed approach in a 2.4 W dc-dc converter implemented in a 180 nm CMOS IC process and co-packaged with its passive components for high performance. The prototype power converter operates from an input voltage of 2.7 V to 5.5 V with an output voltage of $\leq$ 1.2 V, and achieves a 2210 W/inch^3 power density with $\geq$ 80% efficiency. A key contribution of this work is the development and demonstration of a fully package-integrated two-stage SC/magnetic power converter design. This includes *both* semiconductor integration of the conversion stages and methods to achieve overall package integration including co-packaging of the requisite passive elements to achieve extreme high power density. Moreover, we experimentally demonstrate the combination of multiple voltage conversion ratios in the SC stage in conjunction with the operation of the HF regulation stage to achieve a wide input voltage range for the first time.

Section II of the paper presents an overview of the power converter architecture and its characteristics as compared to conventional synchronous buck converters. Section III presents details of the circuit design and control for the proposed system. Section IV describes the implementation and packaging strategy, and section V shows experimental results for the prototype design. Finally, section VI concludes the paper.

II. ARCHITECTURE

A dc-dc converter can be thought of serving two functions. First, it provides voltage transformation from an input to an output (e.g., a step-down voltage transformation). Second, it provides a mechanism to actively regulate the output to compensate for deviations in the input voltage and load. A synchronous buck converter provides both of these functions using only two switches. However, the two switches must be rated for both the high input voltage and the high output current, limiting achievable switching frequency, power density, efficiency, and control bandwidth.

Figure 1 illustrates a two-stage power conversion architecture in which the transformation and regulation functions of the power converter are separated. In this architecture, the transformation stage and the regulation stage are highly optimized for their specific functions.

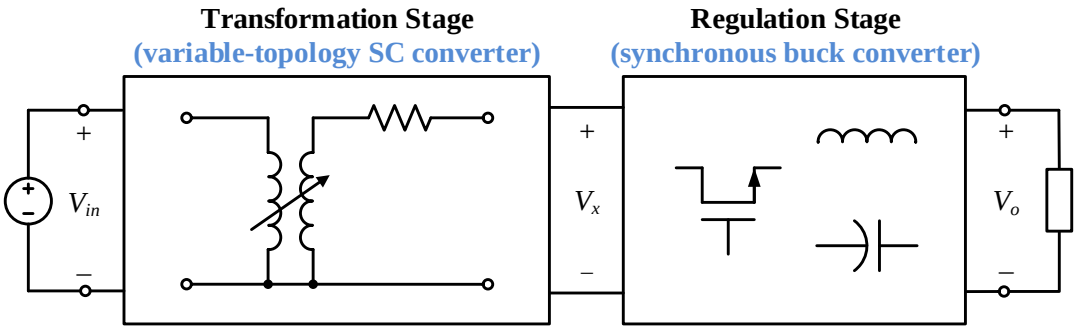

Figure 1 – Block diagram of the two-stage architecture; the semiconductor components of the architecture can be implemented on a single CMOS die, with the transformation stage implemented using slow high-voltage devices, and the regulation stage implemented using fast low-voltage "core" devices

The first stage is a variable-topology (variable-conversion-ratio) SC converter operating at low-to-moderate switching frequency (e.g., hundreds of kHz to low MHz range). Owing to its use of capacitive energy transfer, it can achieve very high efficiency and power density using only small capacitors as energy storage components [10, 11]. This first stage provides a voltage step down to an intermediate voltage whose value varies over a narrow range as the system input voltage varies over a wide range (by varying the SC stage operating mode among a discrete set of states as a function of input voltage). The second stage is a synchronous buck converter that operates at high frequency (e.g., 10 MHz and above) to regulate the output voltage from the small, narrow-range intermediate voltage.

The two stages can be realized on a single CMOS die, with the slow SC stage realized using extended-voltage devices and the fast regulation stage realized using low-voltage "core" devices. This power conversion architecture is thus well-suited to leveraging the device types available in modern CMOS processes. As compared to a synchronous buck converter, (the most common topology for low-output-voltage conversion from wide-range battery inputs and "power systems in package" [12]) this approach can benefit power density, efficiency, and bandwidth.

Traditional switch-mode power converters consist of a combination of magnetic and electric storage elements. The amount of energy storage required in this type of power converter is a function of the switching frequency; the higher the switching frequency, the lower the energy storage requirement and the higher the potential control bandwidth. For very low and narrow-range input voltages, it is possible to design synchronous buck converters that operate efficiently at very high frequencies – even at up to hundreds of megahertz [13,14]. This is a result of complementary metal-oxide-semiconductor (CMOS) scaling and low device voltage stresses. As shown in the appendix, the optimal switching frequency of a synchronous buck converter with CMOS devices follows a power law:

$$f_{opt} = \alpha V_{in}^{\beta} \quad \textbf{(1)}$$

with β ranging from -3.0 to -2.5. Thus, at quite low input voltages (e.g., 1 – 3 V) it is feasible to create power converters operating at quite high frequencies with high-bandwidth control and small passive components (e.g., inductors and capacitors). However, as input voltage increases, the achievable switching frequency – and hence size and bandwidth – rapidly deteriorates. Moreover, as the range of input voltages for which the buck converter must operate widens, one is less able to optimize the design, reducing achievable performance for some portions of the operating range [15]. These factors limit the miniaturization and performance of buck converters for battery-powered inputs. (For example, 2.7 – 5.5 V input range and ~1.0 V output, is common for power converters supplying low-voltage devices from Li-Ion batteries.)

The architecture of Figure 1 utilizes two approaches to achieve higher performance. First, the SC stage provides the bulk of the voltage transformation function. As typical multilayer ceramic capacitors provide energy storage densities at least two orders of magnitude higher than inductors given present technological constraints, this voltage transformation can be achieved in much smaller volume with the first SC stage than can be accomplished with a conventional buck

stage [3,6,10]. Second, since the first stage provides a variable-conversion ratio step-down, it yields a low and narrow-range intermediate voltage for the second synchronous buck regulation stage. Owing to the large magnitude of exponent β in eqn. (1) and the narrow range of its input voltage, the second stage can be designed for efficient operation at very high frequency, yielding reduced passive component size (especially of the inductor) and high achievable control bandwidth. As will be shown, this results in a step-down power conversion system providing extremely high power density and control bandwidth.

III. DESIGN

A prototype dc-dc converter IC has been created to demonstrate the performance and power density of the proposed power converter architecture. All of the power devices and control circuits are monolithically integrated onto a single IC (180 nm CMOS process) to minimize the size of the silicon real estate while also maximizing the electrical performance of the prototype power converter. Figure 2 illustrates a block diagram of the power converter.

Inside the prototype power converter, the transformation stage efficiently provides an intermediate voltage V_x rail that varies over a narrow range of low voltages as the input voltage V_{in} varies over a wider range of higher voltages. To achieve this behavior, a reconfigurable series-parallel SC converter was selected. As illustrated in Figure 2, the SC converter is composed of power MOSFETs $M_1 - M_7$ and energy storage capacitors $C_1 - C_3$. Its operation can be reconfigured for two distinct voltage step-down ratios (1/3 and 1/2) with its voltage conversion ratio dynamically selected based on V_{in}.

The regulation stage converts the intermediate voltage V_x to create a regulated output voltage V_o. It is implemented using a synchronous buck converter. Alternatively, a different type of switch-mode power converter or even a linear regulator could have been selected. Unfortunately, if a linear regulator is used, then the efficiency would be lower and produce larger thermals than a synchronous buck converter at a large number of V_{in} and V_o combinations. For example, if the input voltage is 5.0 V and the output voltage is 0.8 V then the linear regulator would need to convert 1.66 V to 0.8 V, which is at best 48% efficient.

Within the synchronous buck converter, the high-side device M_H is a core PMOS transistor while the low-side device M_L is a core NMOS transistor. These devices were selected for easy

drivability and driven by simple tapered inverters. A driver tapering factor in the 8 to 10 range was chosen to minimize the combined switching and gate driver loss. Care was taken to match the delay of the drivers. Furthermore, to prevent the shoot-through condition in M_L and M_H, two non-overlapping clock signals Φ_p and Φ_n are fed into the drivers. The non-overlapping period is a few hundred picoseconds, approximately two to three times longer than the turn-on and turn-off time of the main power devices.

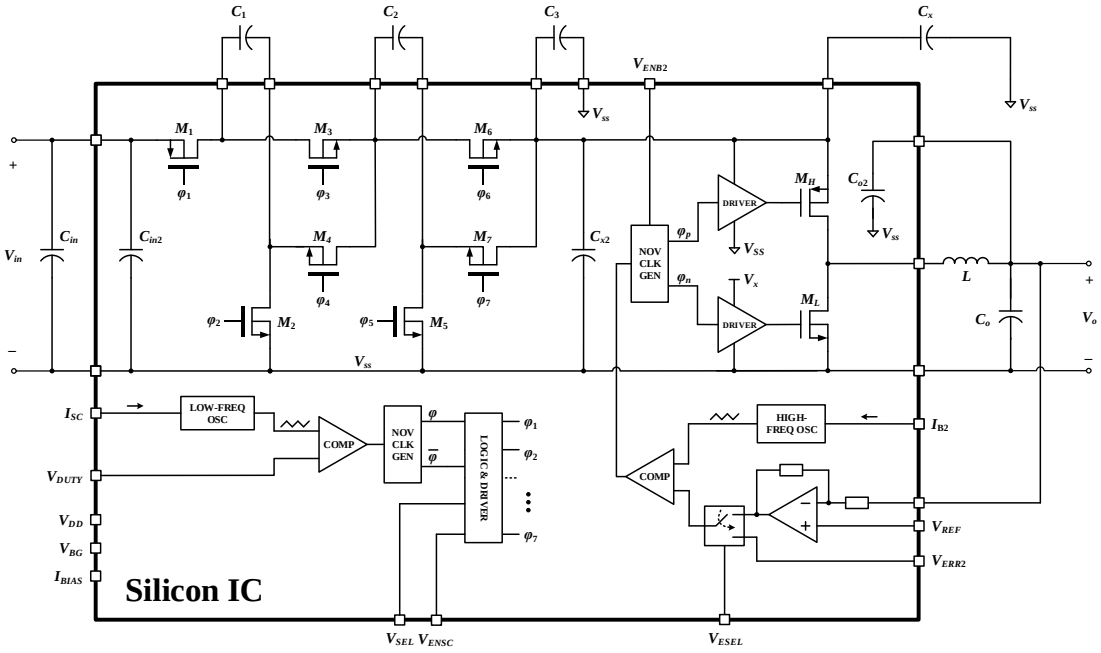

Figure 2 – Block diagram of the prototype power converter showing the IC within the package

The prototype power converter was designed to operate over the ranges given in Table 1. The voltage and power levels were chosen so the power converter could be used in a wide variety of applications. For example, the input voltage V_{in} range of 2.7 V – 5.5 V allows the power converter to work with most lithium-ion battery chemistries. Likewise, the allowed range of the output voltage V_o and the output power P_o are suitable for a wide range of digital electronics, such as mobile application processors and digital signal processors (DSP).

Parameter	Operating Range
V_{in}	2.7 V – 5.5 V
V_o	≤ 1.2 V
P_o	≤ 2.4 W

Table 1 – Prototype power converter operating range

Figure 3 shows the two different SC network configurations for each voltage conversion ratio of the transformation stage. In case (a) and case (c), the capacitors are charged, while in case (b) and case (d), the capacitors are discharged.

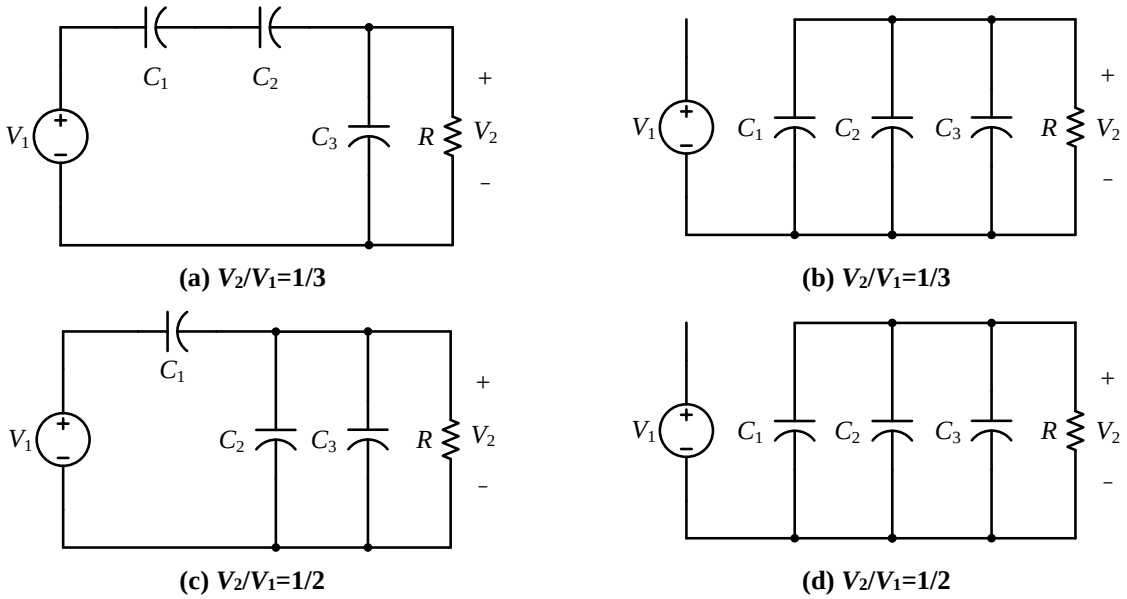

Figure 3 – Charge and discharge configurations of the SC stage for the two step-down ratios. For a voltage conversion ratio of 1/3, the capacitor configuration is alternated between the states shown in (a) and (b), while for a voltage conversion ratio of 1/2 the capacitor configuration is alternated between the states shown in (c) and (d)

The maximum designed V_{in} of the prototype power converter is 5.5 V, so considering the SC circuit topology, the IC process must have devices with a voltage rating of at least 3.66 V. Therefore, a 180 nm CMOS process with two different device flavors was selected. It has low-voltage core devices with a maximum rated voltage of 2.0 V and high-voltage IO devices with a maximum rated voltage of 6.0 V. The low-voltage devices are ideally suited for the regulation stage, while the high-voltage devices are suitable for use in the transformation stage. For simplicity, all of the power devices within the SC transformation stage utilize the high-voltage device flavor, even though switches M_3, M_4, M_6, and M_7 (indicated in Fig. 2) could have been implemented using lower voltage devices.

The transformation stage is controlled such that V_x never exceeds 2.0 V and is never below 1.5 V. The voltage conversion ratio of the SC stage is dynamically set to 2:1 when V_{in} is below 4.0 V and 3:1 when V_{in} is in the 4.0 V – 5.5 V range. This is important because the regulation stage, which follows the transformation stage, is built using low-voltage core devices with a maximum rating of 2.0 V. Also, the lower 1.5 V specification ensures that the regulation stage will have

enough headroom to regulate a V_o of at least 1.2 V. With appropriate control, the regulation stage is able to operate effectively up to at least a 90% duty cycle, yielding a maximum V_o of 1.35 V.

To control V_o, a feedback loop is wrapped around the regulation stage while the transformation stage is run in open loop. (The transformation stage is operated at a fixed frequency in the prototype, though dynamic selection of the SC switching frequency based on V_{in} and/or the load would provide efficiency benefits.) A controller is required to determine the duty cycle of the power devices within the regulation stage such that V_o is regulated in spite of variations at the input or output port of the prototype power converter. A linear voltage-mode controller was used for this task because it is straightforward to design and implement.

In the controller, V_o is compared with a reference voltage and the residual is conditioned by a type-three voltage compensator. The design of the compensator sets the bandwidth and steady-state accuracy of the control loop. The output of the compensator is a control signal, which is fed into a pulse-width modulator in which the control signal is compared with a triangular waveform, thereby producing a double-sided PWM gate signal for the power stage. The PWM signal is further conditioned by a dead-time control circuit. Figure 4 illustrates the small signal loop gain response of the power converter when V_x is equal 1.8 V and V_o is equal to 1.0 V.

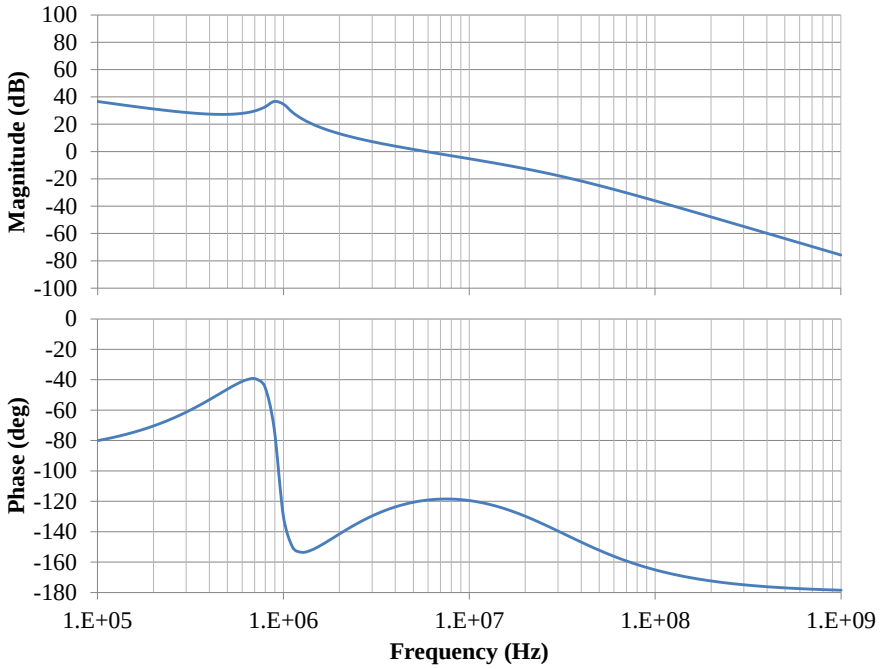

Figure 4 – Small signal loop gain response of the prototype power converter

In order to respond to large slew rates imposed by digital logic, the prototype power converter must have either a large control bandwidth or a large amount of output capacitance. Since the goal of this design is to create a high power density design, we have chosen to push up the control bandwidth instead. The power converter's control loop was designed to be closed at 6 MHz with a 60 degree phase margin as shown in Figure 4.

As described in detail in [16], the circuit design and operating parameters were carefully optimized to achieve a good tradeoff between power density and efficiency given the selected semiconductor process and available passive component technologies. Table 2 shows the optimized parameters for the transformation stage and the regulation stage.

Parameter	Value	Parameter	Value
f_{sc}	1.0 MHz	f_{b2}	20 MHz
W_1	288 mm	W_L	37.80 mm
$W_{2\text{-}7}$	160 mm	W_H	76.02 mm
$C_{1\text{-}3}$	4.7 μF	L	33 nH
C_x	100 nF	C_o	220 nF

Table 2 – Parameters for the transformation stage and regulation stage

As can be seen, the component values and device sizes are commensurate with the switching frequencies and conversion requirements of each stage. The energy density of MLCCs are a few orders of magnitude higher than that of ferrite inductors, and consequently, the volume consumed by the passive components within the transformation stage is roughly similar to the volume consumed by the passive components within the regulation stage.

IV. IMPLEMENTATION

In power electronics, packaging is often one of the most critical aspects to achieving high power density. As power density increases, a given amount of power is processed in a smaller space. This can lead to both electrical and thermal issues that need to be managed. (Packaging was a limiting factor in both efficiency and power density of the power converter in [6], for example.) As a result, we developed a packaging scheme that enabled us to achieve both a high power density and excellent electrical performance. The goal of the package was to create a self-contained power converter module that did not require any external passive components, with

solder bumps for surface mounting to a target board. The resulting module could then be soldered directly onto a standard PCB as an SMT package. The prototype IC is the heart of the power converter module. Figure 5 shows a die image of the fabricated IC.

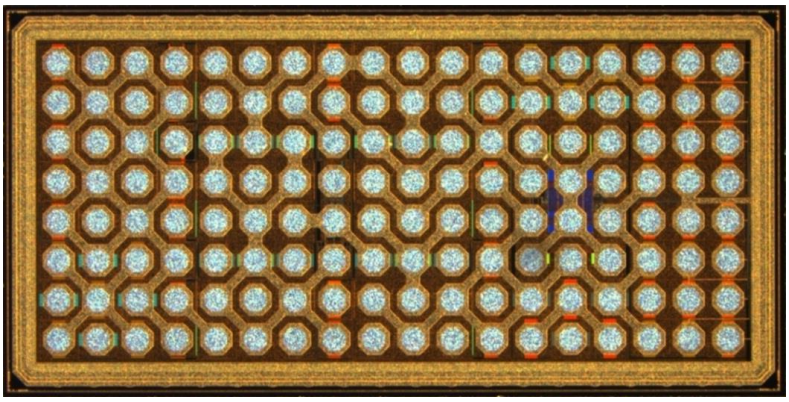

Figure 5 – Image of the fabricated prototype IC The device and interconnect positions are selected to provide low-parasitic connection to the passive components through the interposer board

The overall packaging scheme of the prototype power converter is illustrated in Figure 6. In this packaging scheme, the silicon IC, which is thinned to a thickness of 200 μm, is flipped over with its device layer facing upwards. A first level of bumps (3 mil gold stud bumps with a 220 μm pitch) connects the IC to a high-density interconnect (HDI) interposer, which has 4 metal layers and a total thickness of 250 μm. The passive components, such as the capacitors and inductors, are then soldered onto the opposite side of the interposer.

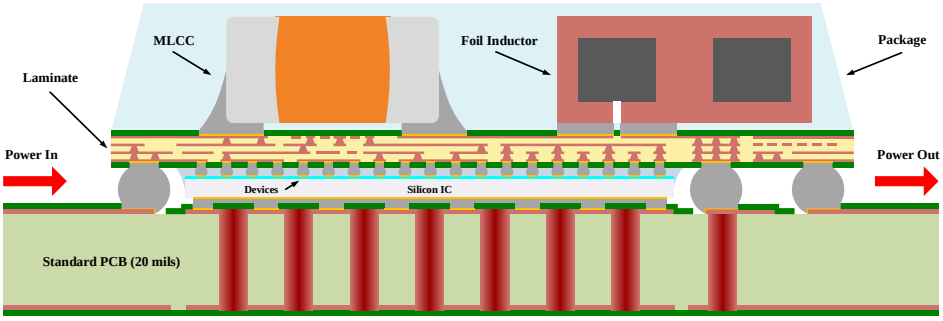

Figure 6 – Cross section of an initial power converter module, also showing the bump interconnect to the target board

The IC and interposer are laid out such that each passive component is oriented directly above the particular location on the silicon IC to which it is to be electrically connected. This ensures that the electrical path between the transistors and their respective passive components is very short. Furthermore, a large number of parallel interconnects are utilized to widen the electrical

path. Both of these techniques reduce the inductance and resistance between the silicon IC and its passive components, thereby reducing energy loss. (Much more detail about the design and layout of both the IC and the interposer can be found in [16].)

To complete the package, a second level of bumps (i.e., C5) is formed on the interposer on the same side as the IC is mounted. These bumps provide electrical connections of the system to the outside world. The pitch of the second level of bumps is 500 μm, which allows the module to be mounted on a standard PCB. Note that with the packaging structure of Figure 6, there is also the opportunity to remove heat directly from the back side of the thinned IC die into the target board.

Figure 7 illustrates a close up photograph of the module with three 100 nH Coilcraft inductors (PFL1005-101MRU) placed in parallel to form the buck inductor. To prevent damaging the IC during testing, we decided to place the Coilcraft inductors off to the side of the interposer. However, there is adequate space to place the inductors on top of the interposer.

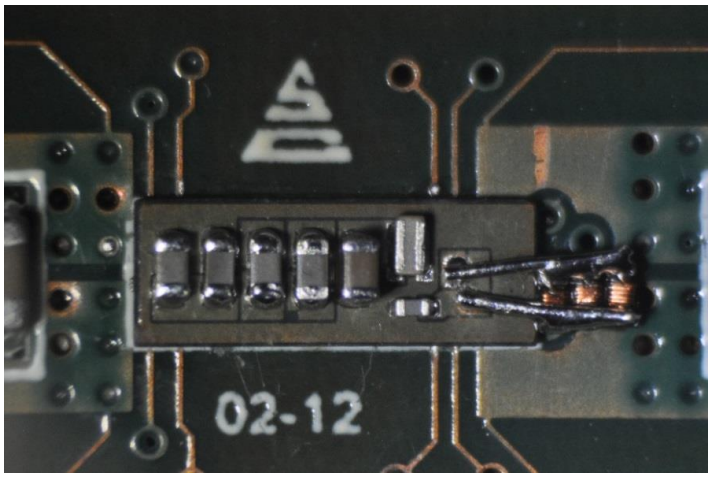

Figure 7 – Top view of a completed prototype module mounted to a target board

Figure 8 illustrates a cross section of a completed prototype module (inductors not shown).

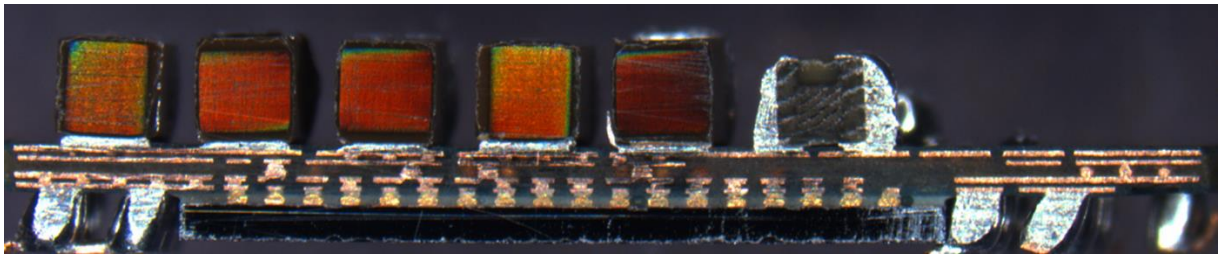

Figure 8 – Cross section of a completed prototype module (without inductor)

Component	Part Number	Count	Volume (mm^3)
C_{in}	C1005X5R0J106M050BC	2	0.50
C_1	C1005X5R0J106M050BC	1	0.25
C_2	C1005X5R0J106M050BC	1	0.25
C_3	C1005X5R0J106M050BC	1	0.25
C_x	LG126Z104MAT2S1	1	0.25
C_o	JMK063BJ224MP-F	1	0.06
L	PFL1005-101MRU	3	1.54
IC	MITDG001	1	2.15
		Total	5.25

Table 3 – Bill of materials for the prototype module

The prototype module is quite small – it has a width of 6.96 mm, a length of 2.56 mm and a height of 1.0 mm, thereby yielding a footprint of 17.80 mm^2 and a total volume of 17.80 mm^3. Based upon Table 3 above, the components consume 29.5% of the total package. Consequently, to improve the power density further, the components could be packed closer together, thereby reducing the wasted space.

V. EXPERIMENTAL RESULTS

In this section, we introduce test results from two different prototype modules. The first module has superior electrical performance to that of the second module. A few of the bumps within the first level of bumps in the second module are missing, thereby increasing the resistive losses. It is also worth noting that the data in Figure 9 - Figure 13 were taken when the filter inductor L was replaced by a 27.3 nH air-core inductor from Coilcraft (0908SQ-27NJLB). This substitution was made because the core loss parameters for the PFL1005-101MRU inductors were unknown and therefore difficult to correlate the measured losses with the simulated losses. Furthermore, two different SC stage switching frequencies were tested (580 kHz and 1 MHz); dynamic control of the SC stage switching frequency would have yielded higher performance, but was not implemented.

Figure 9 shows the measured efficiency of the first module across input voltage at an output voltage of 1.0 V and an output current of 0.5 A with the SC stage operated at 580 kHz and the buck stage operated at 20 MHz. It can be seen that the action of the first stage enables relatively flat efficiency to be maintained across a wide input voltage range. (The voltage conversion ratio of

the SC stage is 2:1 when the input voltage is below 4.0 V and 3:1 when the input voltage is in the 4.0 V – 5.5 V range.)

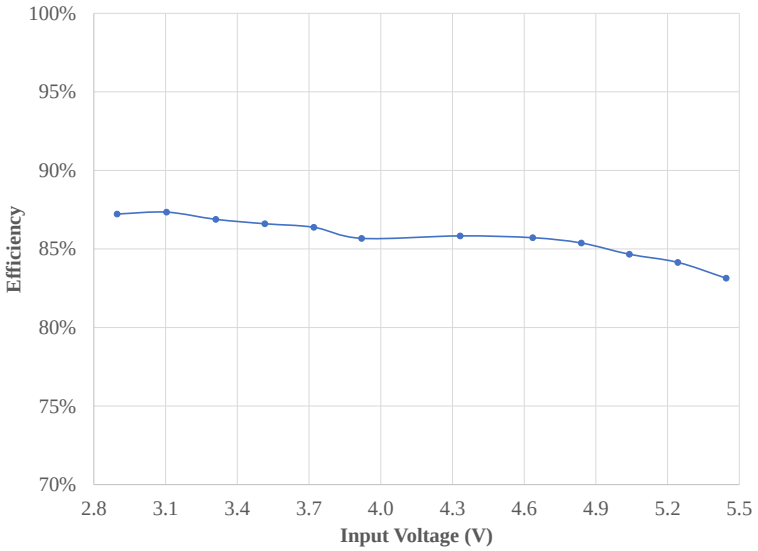

Figure 9 – Measured efficiency vs. input voltage of 1st module (V_o=1V, I_o=0.5 A, f_{sc}=580kHz, f_{b2}=20MHz)

Figure 10 illustrates how the efficiency of the first module varies with output voltage for an input voltage of 5.0 V; it can be seen that the design operates well over a reasonable output voltage range corresponding to the needs of low-voltage electronics. (In this test, the SC stage was operated at 1 MHz, and the buck stage was operated at 20 MHz.)

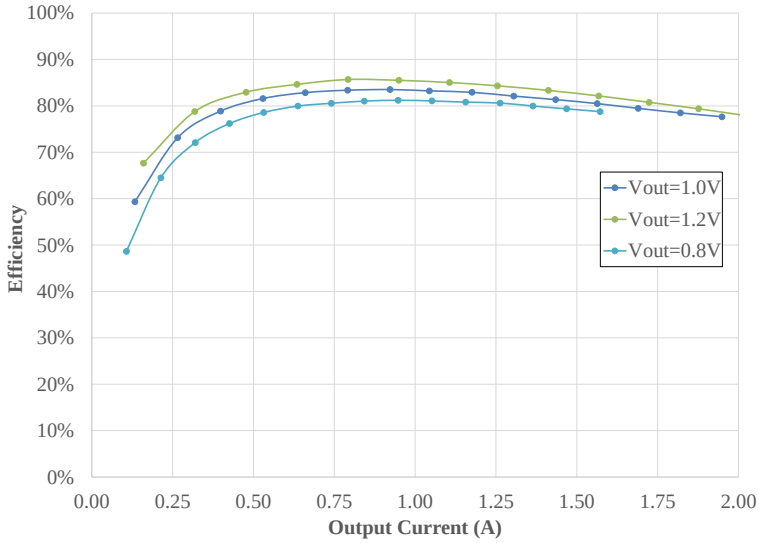

Figure 10 – Measured efficiency vs. output current of the 1st module for three different output voltages (V_{in}=5V, f_{sc}=1000kHz, f_{b2}=20MHz)

Figure 11 illustrates the intermediate voltage V_x when I_o is 2.0 A and f_{sc} is 580 kHz. The peak to peak voltage ripple of V_x is approximately 150 mV with duty cycle of 50%. If you look closely, there is a 20 MHz ripple from the buck stage is superimposed on the 580 kHz ripple from the SC stage. The high frequency ripple would be more pronounced if we utilized a faster oscilloscope.

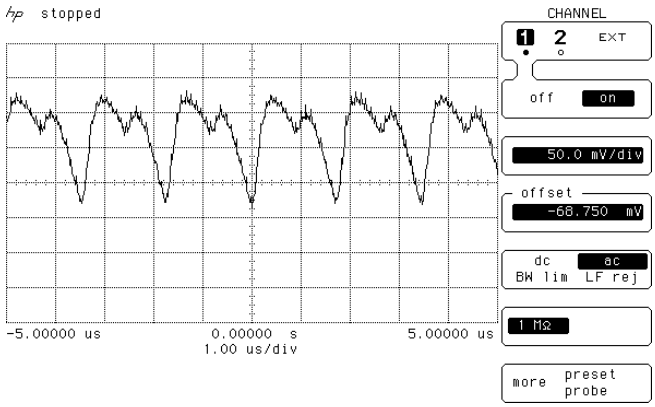

Figure 11 – Voltage ripple at the intermediate node within the 1st module

Figure 12 shows the estimated loss breakdown of the first module based on models detailed in [16]. It can be seen that the dominant losses of the system are capacitive switch losses, resistive switch losses, and resistive interconnect loss. At light load, the loss is dominated by the capacitive losses, while at heavy load, the loss is dominated by the resistive losses. Despite the 20 MHz switching frequency of the buck converter, the commutation losses are low due to the low supply voltage applied to the synchronous buck converter, which is a benefit of the proposed architecture. To gauge the power loss contribution of each stage, Figure 13 shows the efficiency of the SC stage and the buck stage within the first module.

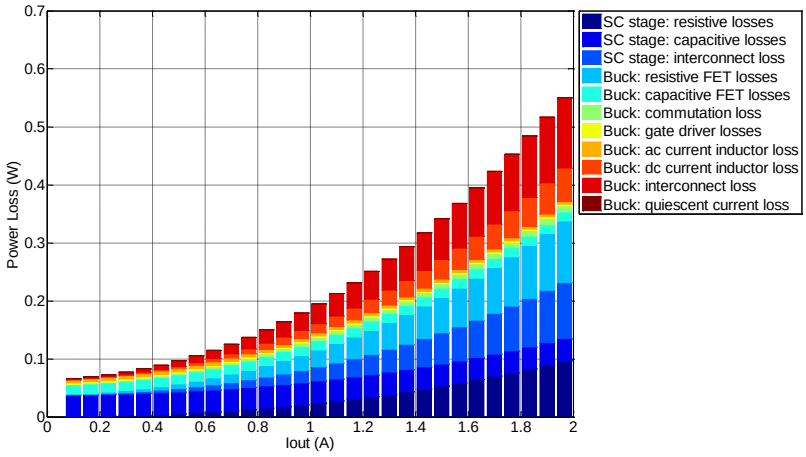

Figure 12 – Estimated power loss breakdown vs. output current (V_{in}=5V, V_o = 1V, f_{sc}=500kHz, f_{b2}=20MHz)

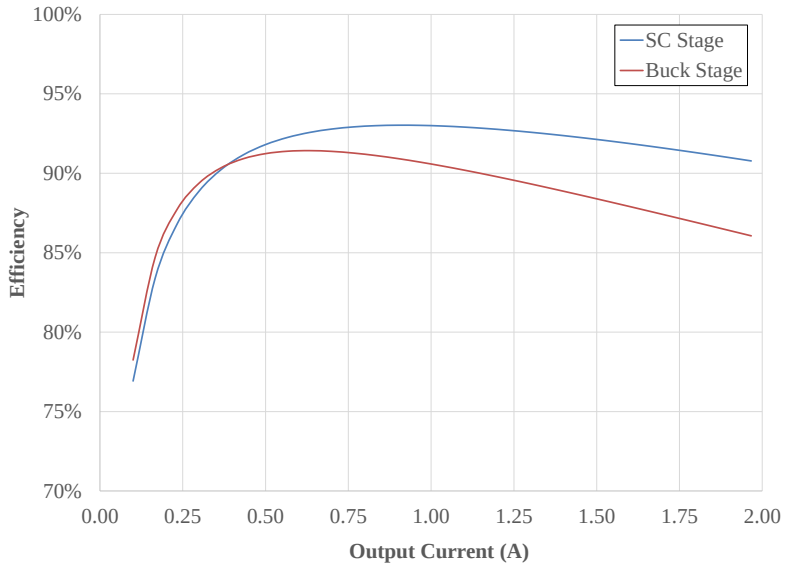

Figure 13 – Estimated efficiency split between the SC stage and the buck stage

Figure 14 illustrates the measured efficiency of the second prototype module with an air-core filter inductor and a magnetic-core filter inductor (3 parallel PFL1005-101MRU). The dotted line is a projection (detailed in [16]) that assumes the magnetic-core inductor has the same dc resistance as the air-core inductor. In this figure, the input voltage is 5.0 V and the output voltage is 1.0 V.

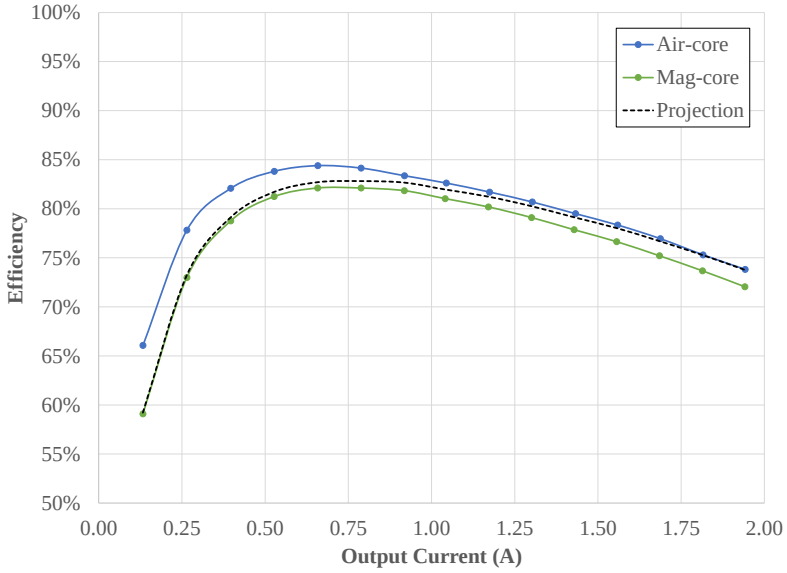

Figure 14 – Magnetic-core inductor vs. air-core inductor of 2nd module (f_{sc}=500kHz, f_{b2}=20MHz)

As can be seen, the efficiency between the projection and system with air-core inductor is quite similar when the output current is above 0.5 A. At light load, however, the deviation in efficiency is as high as 7% at 0.1 A. This behavior is consistent with the addition of core loss. Therefore, the impact on performance using magnetic-core inductors is minor for most load currents even at the second-stage switching frequency of 20 MHz.

The air-core inductor has a height of 1.829 mm with a 2.972 mm x 2.134 mm footprint, whereas the magnetic-core inductors have a total height of 0.71 mm with a 1.14 mm x 0.635 mm total footprint, thereby resulting in a 23-fold reduction in inductor volume using a cored magnetic element for a small efficiency penalty.

To measure the transient response, the second prototype module was loaded with an electronic load. Figure 15 illustrates the response to a load step (between 50 mA and 1 A) with a 16 µs rise/fall time at an input voltage of 3.6 V. The top curve in blue is the intermediate voltage at 500 mV/div, the middle curve in red is the output voltage at 20 mV/div, and the bottom curve in green is the output current at 500 mA/div.

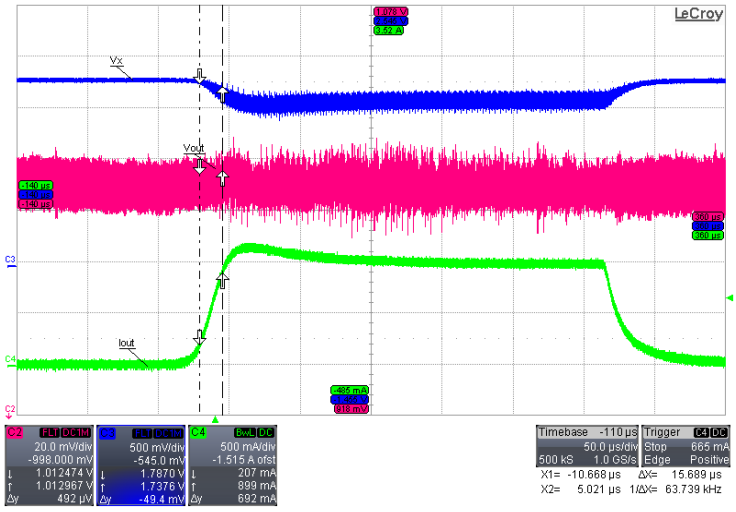

Figure 15 – Measured transient response of the 2nd module to a load current step from 50mA to 1A at an input voltage of 3.6 V

The load step does not produce a noticeable over-shoot or under-shoot because the bandwidth of the regulation stage is very high (approximately 6 MHz). This high achievable control bandwidth (owing to the high switching frequency of the second stage) is a particular benefit of the architecture. The output voltage has a voltage ripple of approximately 20 mV peak-to-peak,

which is mainly due to the small output capacitor used; this could be reduced using additional output capacitance.

There are numerous integrated power converter modules for this general operating range in the marketplace today. Ease of use, reliability, and simplicity (from a PCB footprint perspective) drives their appeal. Table 4 shows a comparison of various commercial power converter modules along with the 1st prototype module from this work.

Part Number	Vendor	Input Voltage (V)	Frequency (MHz)	Peak Efficiency @ Vo=1.2V	Max Output Power (W)	Solution Size (mm^2)	Volume (mm^3)	Power Density ($kW/inch^3$)
FB6832J	Fuji Electric	2.7 - 5.5	2.5	86.5% @ Vin=3.6V	0.36W @ Vo=1.2V	15.66	15.66	0.377
EP5362Q	Enpirion	2.4 - 5.5	5.0	79.0% @ Vin=5.0V	1.20W @ Vo=1.2V	21.00	23.10	0.851
EN5329QI	Enpirion	2.4 - 5.5	3.2	86.0% @ Vin=5.0V	2.40W @ Vo=1.2V	55.00	60.50	0.650
MIC3385	Micrel Semi	2.7 - 5.5	8.0	78.0% @ Vin=5.0V	0.72W @ Vo=1.2V	35.00	31.50	0.375
LTM4601	Linear Tech	4.5 - 28	0.9	88.5% @ Vin=5.0V	14.4W @ Vo=1.2V	290.00	817.80	0.289
LTM4604	Linear Tech	2.35 - 5.5	1.25	85.0% @ Vin=5.0V	4.80W @ Vo=1.2V	185.00	429.20	0.183
This Work	**MIT**	**2.7 - 5.5**	**20.0**	**83.7% @ Vin=5.0V**	**2.40W** @ Vo=1.2V	**17.80**	**17.80**	**2.210**

Table 4 – Comparison of various commercial converter modules and the prototype converter of this work

As can be seen from Table 4, the prototype module has a maximum output power of 2.4 W and consumes a volume of 17.80 mm^3. Consequently, the power density is 2210 $W/inch^3$ with a peak efficiency near 84% at an output voltage of 1.2 V. In comparison, the EN5329QI, which has similar specifications with regard to input voltage range, maximum output current, and efficiency, has a power density of 650 $W/inch^3$. This corresponds to a 3.4-fold improvement in power density as compared to this typical commercial design, and the power density achieved here exceeds (by roughly a factor of two or more) all of the commercial modules of Table 4.

The volume of each module is calculated by multiplying the total solution size, which includes the IC along with its external components, by the tallest component. For example, the solution size of the EN5329QI is 55 mm^2 (i.e. acquired from their website) with a height of 1.1 mm, yielding a volume of 60.50 mm^3. In the case of the prototype power converter, the volume is equal to the size of the module since no external components are required for proper operation.

Figure 16 plots the power density versus switching frequency of the power converter modules from Table 4. As can be seen, the power density increases as the switching frequency increases.

This behavior is the reason there is a continued trend to push up the switching frequency in both industry and academia. The ongoing challenge is then to increase the frequency and decrease the power converter volume without sacrificing efficiency. The architecture and construction method investigated here is beneficial in this regard.

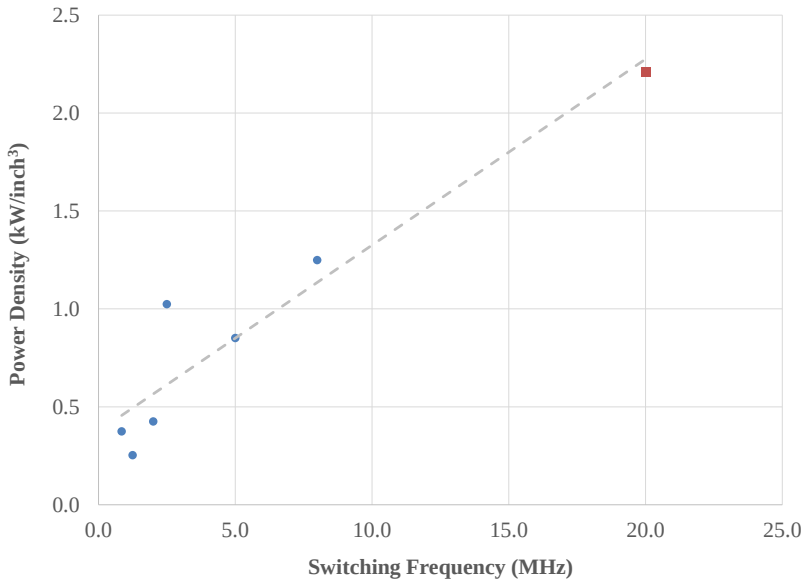

Figure 16 – Power density vs. switching frequency for various modules (This work is at the top right)

It is likely that most or all of the power converters in the commercial modules of Table 4 are synchronous buck converters, though the authors have no direct means of verifying this. In light of this, Table 5 includes a comparative listing of some previous academic work in this space with different power converter topologies.

Reference	[17]	[18]	[19]	[6]	This Work
Publication Year	1997	2011	2012	2012	**2013**
Converter Topology	Cascoded Buck	Buck	Cascoded Buck	Merged two-stage	**Two-stage**
CMOS node	0.15 µm	0.35 µm	0.35 µm	0.18 µm	**0.18 µm**
Input Voltage	3.3V	2.7 - 4.2 V	2.5 - 5.0 V	4.0 - 5.5 V	**2.7 - 5.5 V**
Output Voltage	1.65 V	2.4 V	1.0 - 1.8 V	0.8 - 1.3	**0.6 - 1.2 V**
Switching Frequency	12.8 MHz	5 MHz	1.3 MHz	10 MHz	**20 MHz**
Peak Efficiency (η_{pk})	75%	91%	94%	81%	**84%**
Voltage step-down at η_{pk}	3.3 - 1.65 V	3.3 - 2.4 V	2.5 - 1.8 V	5.0 - 1.3 V	**5.0 - 1.2 V**
Output power range	8.25 - 82.5 mW	0.12 - 1.2 W	18 - 675 mW	0.3 - 0.8 W	**0.2 - 2.4 W**

Table 5 – Comparison of various academic works

The prototype module described here achieves the largest voltage step-down ratio and input voltage range ratio of these comparable works, while operating at a higher switching frequency than many of the other power converters and with comparable efficiencies. This can be attributed in part to the two-stage design and implementation.

VI. CONCLUSION

This paper has presented a two-stage power conversion architecture, design techniques, and packaging approach for integrated power converters operating from battery-scale input voltages and supplying low-voltage outputs. The proposed approach leverages the devices available in low-voltage CMOS processes to achieve higher power density and improved transient response as compared to more conventional power converter designs. The proposed packaging approach yields low-parasitic interconnections of the CMOS die to the passive components, facilitating operation at elevated switching frequencies (20 MHz in the prototype design), and provides a surface-mount "power system in package". The first-generation design operates from an input voltage of 2.7 V to 5.5 V with an output voltage of $\leq$ 1.2 V, and achieves a 2210 W/inch^3 power density with $\geq$ 80% efficiency. It is anticipated that the proposed approach will find application in a range of power converter designs for low-voltage systems.

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REFERENCES

[1] H. Matsuo and K. Harada, "The cascade connection of switching regulators," *IEEE Transactions on Industry Applications,* vol. IA–12, no. 2, pp. 192–198, 1976.

[2] J. Sun, M. Xu, Y. Ying, and F. Lee, "High power density, high efficiency system two-stage power architecture for laptop computers," in *Power Electronics Specialists Conference,* 18-22 June 2006, pp. 1–7.

[3] R.C.N. Pilawa-Podgurski, D.M. Giuliano, and D.J. Perreault, "Merged two-stage power converter architecture with soft charging switched-capacitor energy transfer," in *Power Electronics Specialists Conference*, 2008, pp. 4008–4015.

[4] D. J. Perreault, R. C. N. Pilawa-Podgurski, and D. M. Giuliano, "Power converter with capacitive energy transfer and fast dynamic response," U.S. Patent 8,212,541 B2, July 3, 2012.

[5] R. Guo, Z. Liang, and A. Huang, "A family of multimodes charge pump based dc–dc converter with high efficiency over wide input and output range," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4788–4798, 2012.

[6] R. Pilawa-Podgurski and D. Perreault, "Merged two-stage power converter with soft charging switched-capacitor stage in 180 nm cmos," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 7, pp. 1557–1567, 2012.

[7] B. Mahdavikhah, P. Jain, and A. Prodic, "Digitally controlled multi-phase buck-converter with merged capacitive attenuator," in *Applied Power Electronics Conference and Exposition*, 2012, pp. 1083–1087.

[8] "Factorized power architecture and V-I chips," VICOR, Tech. Rep., 2007.

[9] J. Sun, M. Xu, D. Reusch, and F. Lee, "High efficiency quasi-parallel voltage regulators," in *Applied Power Electronics Conference and Exposition*, February 2008, pp. 811–817.

[10] M. Seeman and S. Sanders, "Analysis and optimization of switched-capacitor dc-dc converters," *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 841–851, 2008.

[11] M. Makowski and D. Maksimovic, "Performance limits of switched-capacitor dc-dc converters," in *Power Electronics Specialists Conference*, vol. 2, 18–22 June 1995, pp. 1215–1221.

[12] F. Waldron, R. Foley, J. Slowey, A. Alderman, B. Narveson, and S. Mathuna, "Technology roadmapping for power supply in package (psip) and power supply on chip (pwrsoc)," *IEEE Transactions on Power Electronics*, vol. 28, no. 9, pp. 4137–4145, 2013.

[13] P. Hazucha, G. Schrom, J. Hahn, B. Bloechel, P. Hack, G. Dermer, S. Narendra, D. Gardner, T. Karnik, V. De, and S. Borkar, "A 233-MHz 80%-87% efficient four-phase dc-dc converter utilizing air-core inductors on package," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 4, pp. 838–845, April 2005.

[14] J. Sun, D. Giuliano, S. Devarajan, J.-Q. Lu, T.P. Chow and R.J. Gutmann, "Fully Monolithic Cellular Buck Converter Design for 3-D Power Delivery," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 17, No. 3, pp. 447-451, March 2009.

[15] T. Takayama and D. Maksimovic, "A power stage optimization method for monolithic dc-dc converters," *2006 IEEE Power Electronics Specialists Conference*, pp. 1-7, June 2006.

[16] D. M. Giuliano, "Miniaturized, low-voltage power converters with fast dynamic response," Ph.D. dissertation, Massachusetts Institute of Technology, 2013.

[17] S. Reynolds, "A dc-dc converter for short-channel cmos technologies," *IEEE Journal of Solid-State Circuits* vol. 32, no. 1, pp. 111–113, 1997.

[18] M. Du, H. Lee, and J. Liu, "A 5-MHz 91% peak-power-efficiency buck regulator with auto-selectable peak- and valley-current control," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 8, pp. 1928–1939, 2011.

[19] H. Nam, Y. Ahn, and J. Roh, "5-V buck converter using 3.3-V standard cmos process with adaptive power transistor driver increasing efficiency and maximum load capacity," *IEEE Transactions on Power Electronics*, vol. 27, no. 1, pp. 463–471, 2012.

[20] G. Schrom, P. Hazucha, F. Paillet, D. Gardner, S. Moon, and T. Karnik, "Optimal design of monolithic integrated dc-dc converters," in *Integrated Circuit Design and Technology*, 14 Aug 2006, pp. 1–3.

APPENDIX

In this appendix, we explore how the achievable switching frequency of dc-dc converters in deep submicron CMOS processes scales with process voltage. For simplicity, we focus on CMOS synchronous buck converters with a switching frequency f_{sw}. Consider how the device-scaling characteristic influences converter performance. As shown in Schrom et al. [20], the MOSFET losses in a synchronous buck converter can be modeled using an effective bridge capacitance C_b and an effective bridge resistance R_b, as illustrated in Figure 17, where W_L, W_H, C_{L0}, C_{H0}, R_{L0}, R_{H0} are the widths, effective specific capacitances, and specific on-resistances of the switches, respectively. Typically, the gate capacitance is the dominant contributor to dynamic loss in low-voltage CMOS processes. Therefore, this model ignores commutation loss.

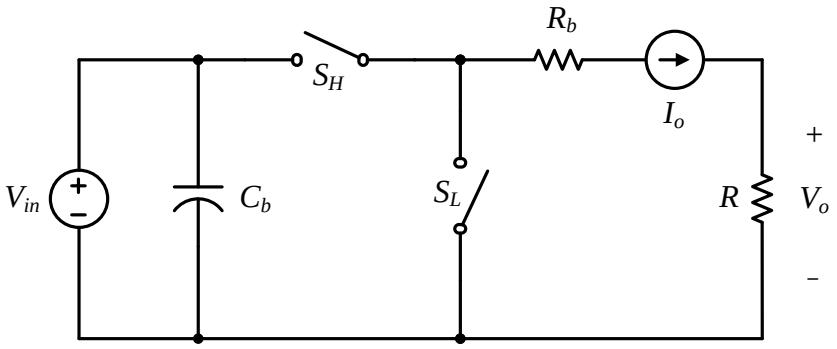

Figure 17 – Buck converter model for calculating energy losses

In this model, we have defined the following parameters as

$$C_b = W_L C_{L0} + W_H C_{H0} \tag{2}$$

and

$$R_b = \frac{R_{L0}}{W_L}(1-D) + \frac{R_{H0}}{W_H} D \quad , \tag{3}$$

where the duty cycle is equal to

$$D = \frac{V_o}{V_{in}} \quad . \tag{4}$$

The optimal width ratio of W_H to W_L can be found by a constrained minimization of C_b at a constant R_b, yielding

$$\alpha = \frac{W_H}{W_L} = \sqrt{\frac{DR_{H0}C_{L0}}{(1-D)R_{L0}C_{H0}}} \quad . \quad [20] \tag{5}$$

Assuming that the power loss is only in the MOSFETs, then the total power loss is a combination of the static loss and dynamic loss given by

$$P_{loss} = C_b V_{in}^2 f_{sw} + R_b I_o^2 = W C_{b0} V_{in}^2 f_{sw} + \frac{R_{b0}}{W} I_o^2 \ , \tag{6}$$

where

$$C_{b0} = \frac{C_b}{W} = \frac{C_{L0} + \alpha C_{H0}}{1+\alpha} \ , \tag{7}$$

and

$$R_{b0} = R_b W = (1+\alpha)\left[(1-D) R_{L0} + \frac{DR_{H0}}{\alpha} \right] . \tag{8}$$

The optimal C_b can be found by minimizing P_{loss} (eqn. (6)), yielding

$$W_{opt} = \frac{I_o}{V_{in}} \sqrt{\frac{R_{b0}}{C_{b0} f_{sw}}} \ , \tag{9}$$

which results in a minimum power loss of

$$P_{loss\,(\min)} = 2 W_{opt} C_{b0} V_{in}^2 f_{sw} = 2 I_o V_{in} \sqrt{R_{b0} C_{b0} f_{sw}} \, . \tag{10}$$

An optimal f_{sw} can be chosen given a desired $P_{loss\,(\min)}$ or, equivalently, a desired efficiency. This optimum is

$$f_{opt} = \frac{P_{loss\,(\min)}^2}{4 I_o^2 V_{in}^2 R_{b0} C_{b0}} \tag{11}$$

Additionally, by combining eqns. (4), (5), (7), (8), and (11), holding I_o and $P_{loss\,(\min)}$ constant, and assuming $R_{H0}C_{H0} \propto V_{in}$ and $R_{L0}C_{L0} \propto V_{in}$, it can be shown that the optimal f_{sw} is

$$f_{opt} \propto \frac{\gamma}{V_{in}^2 (V_{in}\gamma - V_o\gamma + V_o b)(1+\gamma)} \ , \tag{12}$$

where

$$\gamma = \sqrt{\frac{V_o \, b}{V_{in} - V_o}} \, , \tag{13}$$

and

$$b = \frac{R_{P0}C_{P0}}{R_{N0}C_{N0}}. \tag{14}$$

In eqn. (14), b represents a relative performance factor for S_H and S_L. If both devices exhibit the same RC product (e.g., are both NMOS), then b equals one. More typically, S_H is a PMOS and S_L is a NMOS, so b is closer to three. Furthermore, it can be shown empirically that f_{opt} fits the power law

$$f_{opt} = kV_{in}^{\beta}, \tag{15}$$

assuming both β and k are functions of b and V_o, and given $V_{in} > 2V_o$. Figure 18 shows how the exponent β varies as a function of b for various V_o.

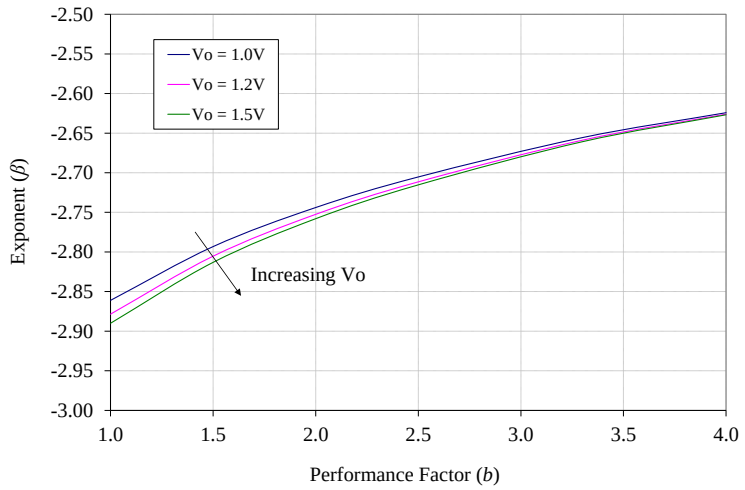

Figure 18 – Exponent β vs. relative performance factor (*b*)

What can be concluded from eqn. (15) and Figure 18 is that f_{opt} increases very rapidly with decreasing V_{in}. For example, if b = 3 and V_o = 1.0 V, then β = -2.67. Therefore, a buck converter with a V_{in} of 1.8 V should be able to switch 15.3 times faster than a buck converter with a V_{in} of 5.0 V with equal power loss in both cases. This leads to less energy storage in the filter elements (L and C) for a given dynamic and static response.