Impedance Control Network Resonant Step-Down DC-DC Converter Architecture

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Abstract— **In this paper, we introduce a step-down resonant dc-dc converter architecture based on the newly-proposed concept of an Impedance Control Network (ICN). The ICN architecture is designed to provide zero-voltage and near-zero-current switching of the power devices, and the proposed approach further uses inverter stacking techniques to reduce the voltages of individual devices. The proposed architecture is suitable for large-step-down, wide-input-range applications such as dc-dc converters for dc distribution in data centers. We demonstrate a first-generation prototype ICN resonant dc-dc converter that can deliver 330 W from a wide input voltage range of 260 V – 410 V to an output voltage of 12 V.**

Keywords—dc/dc converter; resonant converter; high-efficiency converter; wide-range operation; impedance control network; on/off control; burst mode

I. INTRODUCTION

Direct-current (dc) systems are beginning to become more prominent due to the increasing usage of inherently dc devices such as solar photovoltaic (PV) systems, battery systems, LEDs, electronic loads, etc., as well as an effective means of connecting all of these components together through the use of increasingly efficient power electronic converters.

Due to the emergence of dc-based sources and loads, there is a growing need for dc-dc converters that can convert from one dc voltage to another. A particular need is high conversion ratio converters that can take in hundreds of volts and deliver tens of volts efficiently. Furthermore, these converters must be able to maintain high efficiency even if the input voltage varies over a wide range.

For example, take the application of a dc distribution within a building. As internet and cloud-based data and services become more ubiquitous in today's society, more attention is being paid to the amount of energy consumed by the data centers that store and manipulate that information [1]. Therefore, dc distribution (nominally at 380 V dc) is being seriously considered as an alternative to ac distribution in commercial buildings and data centers, as it offers higher efficiency, more effective management of power factor correction, and easier integration of distributed renewable

sources and energy storage [2–4]. Early demonstrations show that 380 V dc distribution architectures can result in energy savings of around 15% over 208 V ac distribution in data centers due to the higher distribution voltage and fewer voltage conversion stages in dc distribution systems [5,6].

A 380 V dc distribution standard is under development in the US and Europe [2-4], and could have a significant impact owing to the large amount of energy consumed in data centers (between 1 and 2% of total electrical energy consumption by some estimates) [1,7,8]. Crucial to the effectiveness of dc distribution, however, are the dc-dc converters that convert the voltage. In data centers, where this dc distribution architecture is expected to see its first deployment [9], the 380 V (actually 260 V - 410 V) will need to be converted to 12 V using a dc-dc converter located in each rack to power the servers. To make this architecture compelling, however, converters that can maintain level output power and high efficiency across the full input voltage range will be needed.

Other applications include the dc-dc bus converters following three-phase power factor correction circuits, microgrid interfaces, and renewable energy sources [10]. These applications use very high voltages that require high voltage rated switches. Therefore, ways to reduce switch stress are also important [11]. These wide-input voltage dc-dc converters could also be applied in applications such as hybrid and electric vehicles (such as for charging and converting among different voltage domains) [12].

II. STATE OF THE ART

Developing technologies to achieve greater efficiency and miniaturization of power converters that deliver energy from high-voltage dc to low-voltage dc loads is challenging, as the high input voltage and large voltage conversion ratios tend to lead to large semiconductor switch and magnetic core losses, and the wide operating range (e.g., input voltage) places constraints on many design techniques.

To reduce switching loss, many power converters utilize soft-switching techniques - zero-voltage switching (ZVS) and/or zero-current switching (ZCS) – in which the switch voltage and/or current are zero at the switching transition. Without soft switching, transistor switching loss can prevent high efficiency from being obtained and also limits power density (owing to the need to operate at low switching frequencies).

Soft-switching techniques often provide high efficiency operation but only under specific operating conditions. Performance tends to degrade greatly when considering requirements of operation across widely varying input voltage. In particular, as the input voltage varies from nominal, the circuit waveforms begin to deviate from desirable characteristics (e.g., ZVS/ZCS is lost, conduction current increases, etc.). This challenge in maintaining high efficiency is tied to both the circuit design and the control methodology.

A. Frequency Control

One common technique used to enable soft-switching in resonant converters (e.g., series, parallel, series-parallel, LLC converters, etc.) is through frequency control. By modulating the converter switching frequency, variations in input voltage can be countered [13-15]. The cost to varying frequency is the potential for increased switching loss when frequency increases, challenges in designing magnetic components and EMI filters, and the potential for circulating currents that do not back off with power.

B. Phase-Shift Control

Another method of control that can be applied to bridge converters at fixed frequency is phase-shift control [16-18]. In this method, multiple inverter legs are phase-shifted from each other to counteract variations in input voltage and maintain output power. Unfortunately, as the inverters are phase shifted from each other, it is possible for asymmetric current waveforms to arise. This asymmetry can increase conduction loss as well as a loss of ZVS. The Full-Bridge ZVS-PWM converter is another topology for high-frequency power applications. Unfortunately, above certain voltages, the switch stress starts to make this topology undesirable [11].

C. Auxiliary Circuits

A third technique for enabling soft-switching is through the use of an auxiliary circuit that can divert current or voltage from the main power switches in order to shape the waveforms necessary for ZCS or ZVS [19,20]. These circuits inherently add component and control complexity and may not always lead to an increase in efficiency across the full operating range.

D. The Proposed Approach

The Impedance Control Network (ICN) architecture presented in this paper is targeted at addressing the above challenges. The ICN technique enables both zero-voltage and near-zero-current switching to be maintained across input voltage variation and output power variation while also reducing switch stress. This particular work focuses on large-step-down applications (from high input voltages to small output voltages, such as needed for data center server power supplies); the only other work exploring ICN techniques [21-23] focused on isolated step-up conversion, which presents very different design considerations and limits. The overall theory and techniques can be applied in numerous applications.

III. THEORY OF THE PROPOSED ARCHITECTURE

Fig. 1 provides a conceptual block diagram of the proposed converter system architecture, which incorporates multiple inverters and one or more rectifiers operated together under phase-shift control, along with a transformation stage
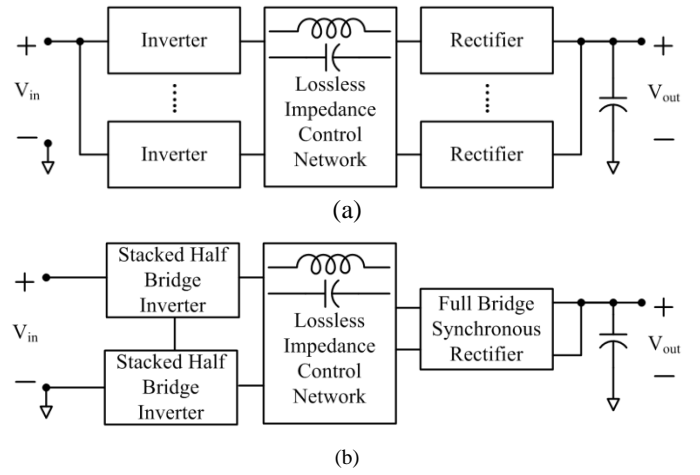

(a)

(b)

Fig. 1. Architecture of the proposed Impedance Control Network (ICN) resonant converter in its (a) most general form, and (b) as pursued here. A plurality of phase-shifted inverters and one or more rectifiers interact through a lossless impedance control network that ensures desirable operating points for the inverter and rectifier blocks.

incorporating an "Impedance Control Network" (ICN). The ICN operates to shape the operating waveforms under phase-shift control to maintain simultaneous ZVS and near ZCS of the transistors across the converter operating range (e.g., across input voltage), minimizing stress and switching loss, which are valuable for achieving high efficiency and power density. We address an implementation of the ICN architecture that targets high, wide-range input voltage and low output voltage. To do so, we exploit an ICN-based system utilizing a "double stacked-bridge" inverter structure and a full bridge synchronous rectifier. We describe each of the subsystems of this converter in the following subsections.

A. Inverter Stage

The inverter structure we chose is that of a "double stacked-bridge" inverter as illustrated in Fig. 2. That is, we employ a stacked full bridge and stack that with a second stacked full bridge. Each half bridge in the double stacked-bridge thus ideally sees only 1/4th the full input voltage (though there is some difference among the individual level
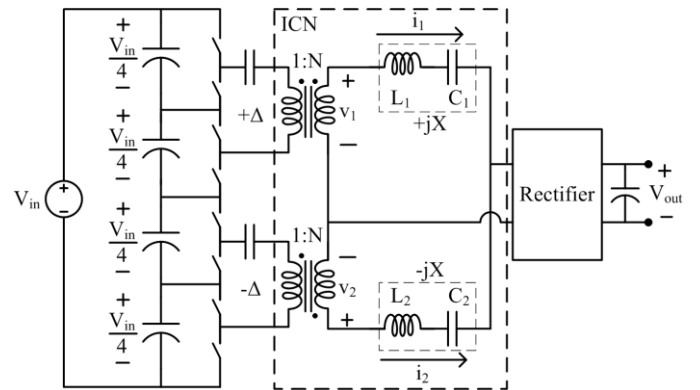

Fig. 2. An ICN resonant converter comprising a pair of stacked bridges that are also stacked. The top inverter is phase shifted by 2Δ ahead of the bottom inverter. The two series LC branches, L_1C_1 and L_2C_2, are selected to have equal and opposite reactances at the switching frequency.

voltages in practice). Operating each of the two stacked-bridge inverters at the desired output frequency (1/T_0), with a delay of half a cycle, $\Delta t = 0.5 \cdot T_0$, between the half bridges and with 50% duty ratios (neglecting ZVS transition time), each generates a symmetric square waveform (or trapezoidal waveform); the relative phase shift between these two generated square waves is used as one of the major control handles in the system. This double "stacked inverter" structure enables synthesis of the desired operating waveforms while keeping individual device voltage ratings low compared to the (high) input voltage, which is valuable for achieving high efficiency.

B. Transformation Stage: Lossless Impedance Control Network

Interfacing the inverters and rectifier is the transformation stage, which uses a novel lossless impedance control network (ICN) and associated controls that allow ZVS and near ZCS to be maintained over a wide input voltage range. The ICN shares some of the features of the Chireix Power Combiner that is sometimes used in RF outphasing power amplifiers [24,25], but operates differently (and with different control behavior) owing to the effect of the input impedance characteristics of the rectifier and its use to maintain ZVS/near ZCS across the operating range.

Fig. 2 shows the architecture employed for the ICN as well as the double stacked-bridge inverter previously mentioned. The output of each inverter is fed into the primary winding of a transformer and the secondary winding of the transformer is connected to a series connection of reactive elements which are in turn coupled to the rectifier. These elements form the impedance control network, and their values are carefully selected. Each series combination serves two distinct purposes. First, they filter out harmonics such that the currents i_1 and i_2 in Fig. 2 will be approximately sinusoidal. Second, to achieve ZVS and near ZCS, the fundamental current must be approximately in phase with the voltage (with current lagging by only enough to ensure ZVS transitions, though we initially treat the case of making them exactly in phase). In order to achieve this, the value of the net reactance in the top branch and the value of the net reactance in the bottom branch of Fig. 2 are selected to be equal in magnitude but opposite in sign (i.e., +jX and –jX) at the switching frequency.

To analyze the power transfer in this system, we consider power transfer through the fundamental components of voltage and current. To do so, the inverters outputs may be modeled by voltage sources representing the fundamental component of their output voltage, and the rectifier can be modeled as an equivalent resistor as shown in Fig. 3. Performing the superposition analysis of Fig. 4, the source voltages and currents can be calculated as:

$$\hat{V}_1 = V e^{j\Delta}, \tag{1}$$

$$\hat{V}_2 = V e^{-j\Delta}, \tag{2}$$

$$\hat{I}_1 = \frac{V}{X}\sin(\Delta) + j\left(\frac{2RV}{X^2}\sin(\Delta) - \frac{V}{X}\cos(\Delta)\right), \tag{3}$$
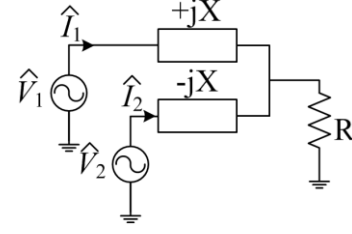

Fig. 3. Simplified representation of the lossless ICN structure coupled with an equivalent resistive load.
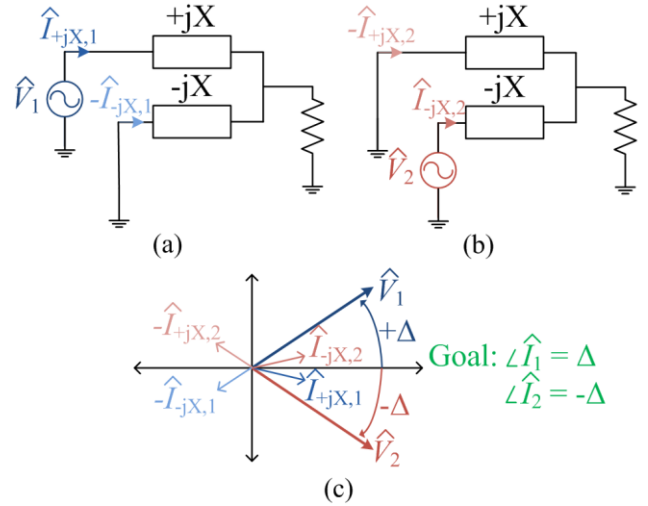

Fig. 4. Superposition analysis of the ICN structure of Fig. 3. By supressing (a) V_2 and (b) V_1 independently, we can easily analyze the current flowing through each reactive component (c).

$$\hat{I}_2 = \frac{V}{X}\sin(\Delta) - j\left(\frac{2RV}{X^2}\sin(\Delta) - \frac{V}{X}\cos(\Delta)\right), \tag{4}$$

where it is assumed each voltage source has the same magnitude, Δ is the phase shift, X is the magnitude of the reactance of each of the two branches of the ICN, and R is the equivalent resistance of the rectifier. For resistive loading of the sources, the angle of $\hat{I}_1$ and $\hat{I}_2$ should be Δ and $-\Delta$, respectively. This is true when

$$\sin(2\Delta) = \frac{X}{R}. \tag{5}$$

Since (5) can be true for more than one angle, consider the effective admittance seen by one of the sources:

$$\hat{Y}_1 = \frac{2R\sin^2(\Delta)}{X^2} + j\left(\frac{2R}{X^2}\sin(\Delta)\cos(\Delta) - \frac{1}{X}\right). \tag{6}$$

Let us replace R with circuit parameters that are well-defined for the circuit such as the input voltage, V_{in}, the output voltage, V_{out}, and the transformer turns ratio, N. First, we see the power delivered by each source is

$$P_1 = P_2 = \frac{1}{2}Re\{\hat{V}_1\hat{I}_1\} = \frac{V^2 R}{X^2}\sin^2(\Delta), \tag{7}$$

where in this case, V for the two stacked half-bridges is

$$V = \frac{NV_{in}}{\pi}. \tag{8}$$

Furthermore, a full bridge rectifier switched in phase with the drive current can be modeled with an equivalent resistance [14]:

$$R = \frac{8V_{out}^2}{\pi^2 P_{out}}. \tag{9}$$

Using conservation of power we can rewrite the equivalent resistance as

$$R = \frac{2V_{out}X}{NV_{in}\sin(\Delta)}. \tag{10}$$

Finally, the effective admittances seen by the two inverters (Y_1 and Y_2) can be expressed as

$$Y_1 = Y_2^* = \frac{4V_{out}\sin\Delta}{NV_{in}X} + j\left(\frac{4V_{out}\cos\Delta}{NV_{in}X} - \frac{1}{X}\right). \tag{11}$$

(By "effective admittance" we mean the ac current to voltage ratio at each inverter output with both inverters active.)

With this design, the effective susceptance seen by the two inverters can be made zero or arbitrarily small when the two inverters are operated with a specific phase shift between them, as shown in Fig. 5. The phase shift at which the susceptance seen by the inverters becomes zero is a function of the input-output voltage conversion ratio and is given by:

$$\Delta = \cos^{-1}\left(\frac{NV_{in}}{4V_{out}}\right). \tag{12}$$

Hence, by varying this phase shift as the input voltage varies, the admittance seen by the inverters can be kept purely conductive across the full input voltage operating range of the dc-dc converter (i.e., inverter currents remaining in phase with inverter voltages). Adjusting frequency or impedance slightly for ZVS transitions, this allows the inverter switches to have simultaneous ZVS and near ZCS capability across the range of voltage conversion ratios, thus reducing switching losses and boosting converter efficiency.

When operated in the manner described above, one can achieve good operation over a wide range of voltage

conversion ratios. At a given switching frequency, the output power of an inverter loaded with a fixed resistor is proportional to the square of the input voltage and the conductance seen by the inverter. In conventional designs, this can often lead to large variations in power delivery with input voltage that must be addressed (e.g., by oversizing the inverter components and/or using frequency control to modulate power). However, since the effective conductance seen by the inverters in our system decreases with voltage (see Fig. 5), the variation in output power can be limited to a narrow range across a wide input voltage range. By combining (7), (8), and (10) and applying trigonometric manipulations, the output power can be expressed as:

$$P_{out} = \frac{NV_{in}\sqrt{16V_{out}^2 - N^2V_{in}^2}}{\pi^2 X}. \tag{13}$$

This enables improved sizing of inverter components and use of fixed-frequency operation, with consequent benefits for efficiency. Furthermore, given the variation in output power with input voltage in (13), the variation can be minimized if the converter is designed to deliver the same output power at its minimum and maximum input voltages, $V_{in,min}$ and $V_{in,max}$, respectively. Therefore, the above design methodology can be mathematically expressed as:

$$P_{out}(V_{in,min}) = P_{out}(V_{in,max}) = P_{out,max} \tag{14}$$

The two equations given by (14) can be used to determine the following closed-form analytical expressions for the transformer turns ratio N and the reactance X of the impedance control network:

$$N = \frac{4V_{out}}{\sqrt{V_{in,min}^2 + V_{in,max}^2}}, \tag{15}$$

$$X = \frac{NV_{in,min}\sqrt{16V_{out}^2 - N^2V_{in,min}^2}}{\pi^2 P_{out,max}} \tag{16}$$

A plot of the theoretical output power of (13) using (15) and (16) with V_{out} of 12 V, $V_{in,min}$ of 260V, $V_{in,max}$ of 410V, and $P_{out,max}$ of 400W is shown in Fig. 6. It can be seen that the actual maximum output power is about 10% greater than the designed maximum output power. To address this, the output power of the converter can be further controlled to values below those in Fig. 6 using a burst (on/off) control strategy in which the operation of the converter is modulated on and off at a frequency much lower than its switching frequency [26,27].
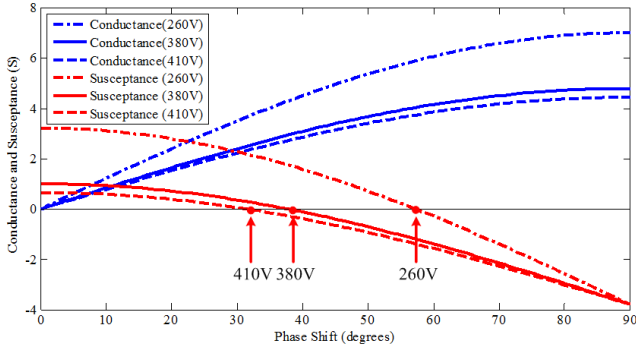

Fig. 5. Effective conductance and susceptance from (11) seen by the two inverters as a function of their relative phase shift for three different input voltage values: 260V, 380V and 410V. For these plots, V_{out} is 12V, N is 0.1, and X is 0.2639Ω. Both inverters see the same conductance, but one sees the negative of the susceptance shown above.
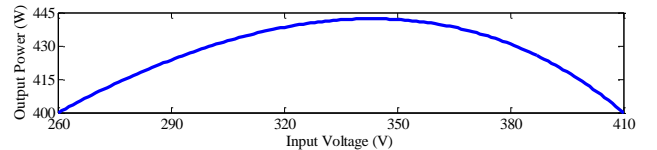

Fig. 6. Variation in output power as a function of input voltage for the ICN converter operated with the phase-shift between two inverters controlled to provide zero effective susceptance of the inverters. With the design parameters of (15) and (16), converter power varies only minimally over the designed output power, $P_{out,max}$, of 400 W throughout the voltage range of operation (i.e., V_{in} = 260 V – 410 V at V_{out} =12V).

On/Off control is desirable because converter losses back off proportionally to power delivered, thus enabling efficient operation to be maintained over a wide power range.

C. Rectification Stage

The final stage of this converter consists of a full bridge rectifier. Such rectifiers can be implemented with a diode bridge. However at such a low output voltage and high output current, device loss would drastically affect the performance and reduce efficiency. Therefore, a synchronous full bridge rectifier is employed and controlled to act as a diode bridge in phase with the current. To further reduce conduction loss presented by the high output current, devices are placed in parallel.

IV. EXPERIMENTAL VALIDATION AND RESULTS

A prototype converter has been developed to experimentally validate the theory of the ICN converter presented in the previous section. Fig. 7 shows the design of a prototype converter implementing the proposed approach. The components used and their values are listed in Table I and the converter specifications are listed in Table II. The output power rating is listed as 300W to account for losses and nonidealities in the circuit but calculations for components is done with an idealized output power rating of 400W.

The inverter switches are realized with EPC2010 GaN-on-Si switches, each controlled with TI LM5114 drivers. The rectifier is a synchronous full bridge realized with EPC2023 GaN switches. In order to increase efficiency, each half-bridge in the full bridge rectifier comprises two parallel half-bridges. Each half-bridge is controlled with TI LM5113 drivers.

A. Transformer Design

The two transformers employed in the circuit of Fig. 7 are identical. They are each designed to conduct a maximum of 4 A_{RMS} in the primary winding and 40 A_{RMS} in the secondary winding. The primary side sees a voltage to above 100V (because the switches operate at a 50% duty ratio). Each will process roughly 200 W of power.

To attain the benefits of planar magnetics (e.g., as described in [28]), the transformer windings are implemented in a printed circuit board (PCB). Given the high turns ratio and secondary current, multiple layers are needed; the best configuration of the layers is discussed in [29-31]. To minimize winding resistance as a result of skin and proximity effect, a fully interleaved structure is optimal. This structure has the primary turns and the secondary turns alternating layers as shown in Fig. 8(a). This pattern also reduces leakage inductance. It is not a design goal to minimize leakage inductance (since it can be used for harmonic filtering); rather an interleaved configuration is selected to minimize the ac resistance.

Given the 500 kHz frequency range, we choose EPCOS N49 material for its low core loss [32]. Available planar core shapes include low profile RM cores, ER cores and low profile E cores. ER cores tend to have lower winding loss and lower leakage but E cores have a higher cross sectional area for magnetic flux. Given that leakage is acceptable and that there
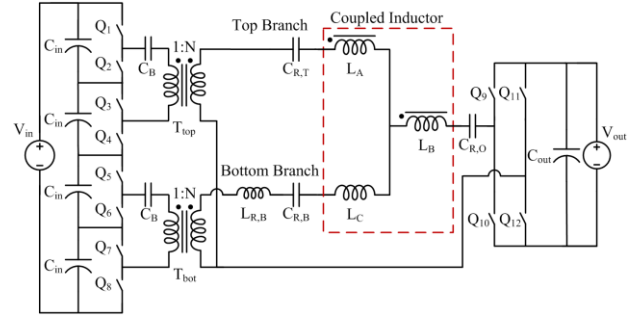

Fig. 7. Proposed implementation of the ICN converter. The ICN incorporates harmonic filtering through the use of resonant tanks as well as two equal but opposite impedances. This structure contains four magnetic structures - two transformers, a coupled inductor (indicated by the red-dashed box), and a resonant inductor.

TABLE I.   COMPONENTS FOR PROTOTYPE CONVERTER

Component	Description	Value
Q_1-Q_8	EPC2010 200V/12A eGaN® FETs	-
Q_9-Q_{12}	EPC2023 30V/60A eGaN® FETs	-
C_B	TDK 250V X7T ceramic	6.6 µF
N	10 turn primary, 1 turn secondary	0.1
T_{top} T_{bot}	EPCOS EILP43-N49, 8 layer, 4 oz PCB winding	42 µH[a]
$C_{R,T}$	TDK 50V X7R ceramic	varies[b]
$L_{R,B}$	MICROMETALS P4848-102, 2 turn, 5mil foil-wrapped winding	130 nH
$C_{R,B}$	TDK 50V NP0 ceramic TDK 50V C0G ceramic	30 nF paralleled w/ 600 nF
L_A	EPCOS EILP18-N49, 4 layer, 5mil foil winding	1 turn	50nH
L_B		1 turn	50 nH
L_C		-	-25nH
$C_{R,O}$	TDK 50V NP0 ceramic	1.13 µF
C_{in}	TDK 250V X7T ceramic Nichicon 350V electrolytic	7.6 µF paralleled w/ 47 µF
C_{out}	TDK 16V X7S ceramic Nichicon 50V electrolytic	1 mF paralleled w/ 560 µF

a. magnetizing inductance seen from primary

b. this capacitance is tuned to match the actual impedance seen in L_A

TABLE II.   CONVERTER SPECIFICATIONS

Parameter	Description	Value
V_{in}	Input voltage range	260 V - 410 V
V_{out}	Output voltage	12 V
P_{out}	Output power rating	300W
f_{sw}	Switching frequency	500 kHz

is a desire to minimize flux density, an EI core shape is selected.

Independent from the core shape is the choice of copper thickness. This depends heavily on frequency and the level of interleaving. From Dowell's equation and approximating the waveforms to be sinusoidal, the optimal ratio of layer thickness to skin depth is given in [33] to be:

$$\Delta_{opt} = \sqrt[4]{\frac{15}{(5p^2 - 1)}} \qquad (17)$$

where p is the number of (consecutive) layers of a primary or secondary winding. The winding structure we consider has

fully interleaved windings such that only one consecutive layer of primary exists followed by only one consecutive layer of secondary. Therefore, the optimal ratio is calculated to be 1.39, and the thickness of the winding should be 1.39 times the skin depth at the operating frequency. The skin depth of 100°C copper at 500 kHz is approximately 108 μm. Therefore, we conclude that the choice of 4 oz copper, which has a thickness of 140 μm, is optimal (i.e., yields the lowest ac loss).

Based on a study of available cores and designs, an ELP43 core half paired with an I43 core (also known as a plate) yielded the lowest losses at 500 kHz. Winding loss is the dominant loss in this design. In order to reduce the losses, we use many layers of conduction, with 8 layers ultimately chosen. Given the dimensions of the EILP43 core set, a finished thickness of 62 mils was chosen in order to avoid any fringing effects from the air gap between the core halves [34,35].

Lastly, a gap is inserted between the two core halves using Kapton tape. This gap is used to lower the magnetizing inductance thereby providing magnetizing current for use in ZVS soft switching of the inverter devices. In this way, the inverter current is the superposition of a sinusoidal waveform created by the ICN network and a triangle waveform created by the transformer magnetizing inductance. This triangle waveform has positive and negative peaks at the switching transition which help maintain ZVS across the full input voltage range. A magnetizing inductance of 42 μH was chosen based on simulations.

To summarize, the transformers are made using EPCOS EILP43-N49 cores with a winding structure implemented in an 8-layer, 4 oz copper PCB. The general structure, which can be seen in Fig. 8(a), includes a 10-turn primary winding and a 1-turn secondary winding. The primary winding is split in half between two series-connected layers. There are two full sets of primary windings which are connected in parallel with each other. In between each layer containing a primary winding is a single-turn secondary winding. The four secondary windings are connected in parallel. Because of the interleaved layers, the transformer provides low loss, but does not provide sufficient leakage inductance as can be seen in the model of Fig. 9. Therefore, $L_{R,B}$ in Fig. 7 is implemented with a 2-turn, foil-wrapped rod core from Micrometals (P4848-102).

B. Coupled Inductor Design

The ICN structure is partially realized through a coupled magnetic structure (outlined in a red-dashed box in Fig. 7) that reduces the loss in the resonant tank magnetic components for the system. In a single magnetic component, one can achieve portions of the ICN reactances as well as an inductor for the output resonant tank (L_B/$C_{R,O}$). An example of how such a winding structure can be implemented is shown in Fig. 8(b) and Fig. 10(a) and the equivalent circuit model is shown in Fig. 10(b). The true winding implementation which is designed to be implemented in PCB is shown in Fig. 8 (b); in the present prototype this is realized using discrete windings constructed from Kapton-insulated foil constructed from two single-turn 5-mil-thick windings on an EILP18-N49 core.

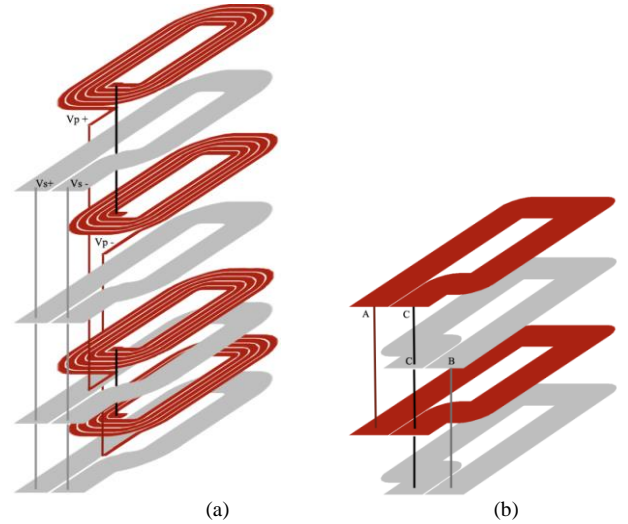For the structure shown in Fig. 10(a), we can mathematically derive the equivalent inductor values shown in

(a)   (b)

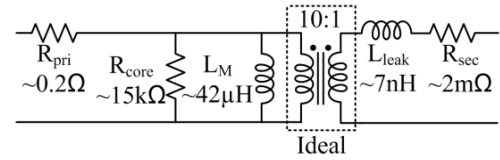Fig. 8. Winding structures for the (a) transformer and (b) coupled inductor.

Fig. 9. Transformer circuit model used in simulation. In this model, R_{pri}, R_{sec}, and L_{leak} are parasitic elements. L_M is the magnetizing inductance that was specifically chosen and R_{core} incorporates the core loss.
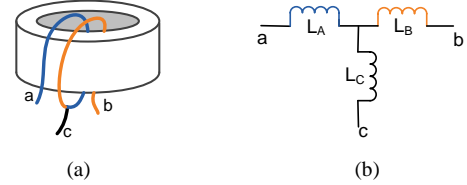

(a)   (b)

Fig. 10. Coupled inductor (a) example implementation and (b) equivalent circuit model. This implementation uses a toroidal magnetic core and each inductor is composed of only one turn. This model is referred to as the "T" model [36, 37]. Inductors L_A, L_B and L_C are the apparent inductors of the T model of the coupled magnetic winding.

Fig. 10(b). Let the specific inductance in (nH per turn^2) of the toroid be A_L. Let there be N_L turns between terminals a and c, and N_L turns between c and b for a center-tapped inductor. Relating this to the equivalent circuit model of Fig. 10(b) we get the following set of equations:

$$L_A + L_C = N_L^2 A_L, \tag{18}$$

$$L_B + L_C = N_L^2 A_L, \tag{19}$$

$$L_A + L_B = 4N_L^2 A_L. \tag{20}$$

Through some manipulation and substitution, each inductance in terms of known parameters N_L and A_L is expressed as:

$$L_A = L_B = 2N_L^2 A_L, \tag{21}$$

$$L_C = -N_L^2 A_L. \tag{22}$$

The negative inductance contributes to the negative impedance in Fig. 2. Because the magnitude of the impedance of L_C is

only half that of L_A, additional capacitors are needed to obtain the full value for -jX.

C. Prototype Performance

In this prototype converter, the inverter stage, magnetic components, and rectifier stage are implemented on separate boards to allow rapid replacement and refinement of the three individual stages. Nonetheless, the approach is compatible with full integration of the components. Fig. 11 shows the top and bottom views of the converter.

Waveforms taken on the bench show promising converter performance and are well matched to the simulation results. The waveforms for the endpoints of the input voltage range are shown in Fig. 12. While the voltage across the secondary of the transformer is shown, the behavior of the inverter switches is still represented. Across the full operating region, we get ZVS and near-ZCS switching as predicted by the design models. The current is fairly sinusoidal at the low end of the input voltage range and begins to square off towards the high end of the input voltage range. We can also see that the phase shift between the inverters decreases as the input voltage increases, reflecting the proposed control method.

Power and efficiency measurements have been taken and are shown in Fig. 13. Note that these measurements do not include control or gating losses but these are negligible compared to the power stage losses. The input power is fairly
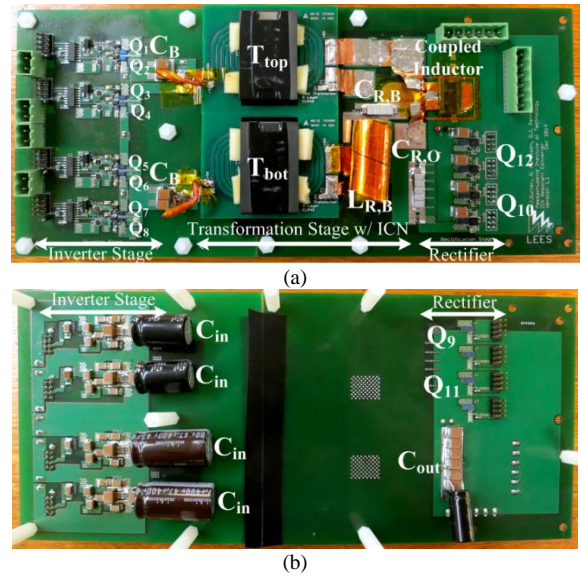

(a)

(b)

Fig. 11. Populated converter showing both (a) top and (b) bottom views.

well matched to the theoretical power shown in Fig. 6. Mismatch can be attributed to small deviations in the turns ratio and impedance from the calculated values of (15) and (16). Impedance mismatching could be tuned through the addition of series capacitance. This characteristic confirms the
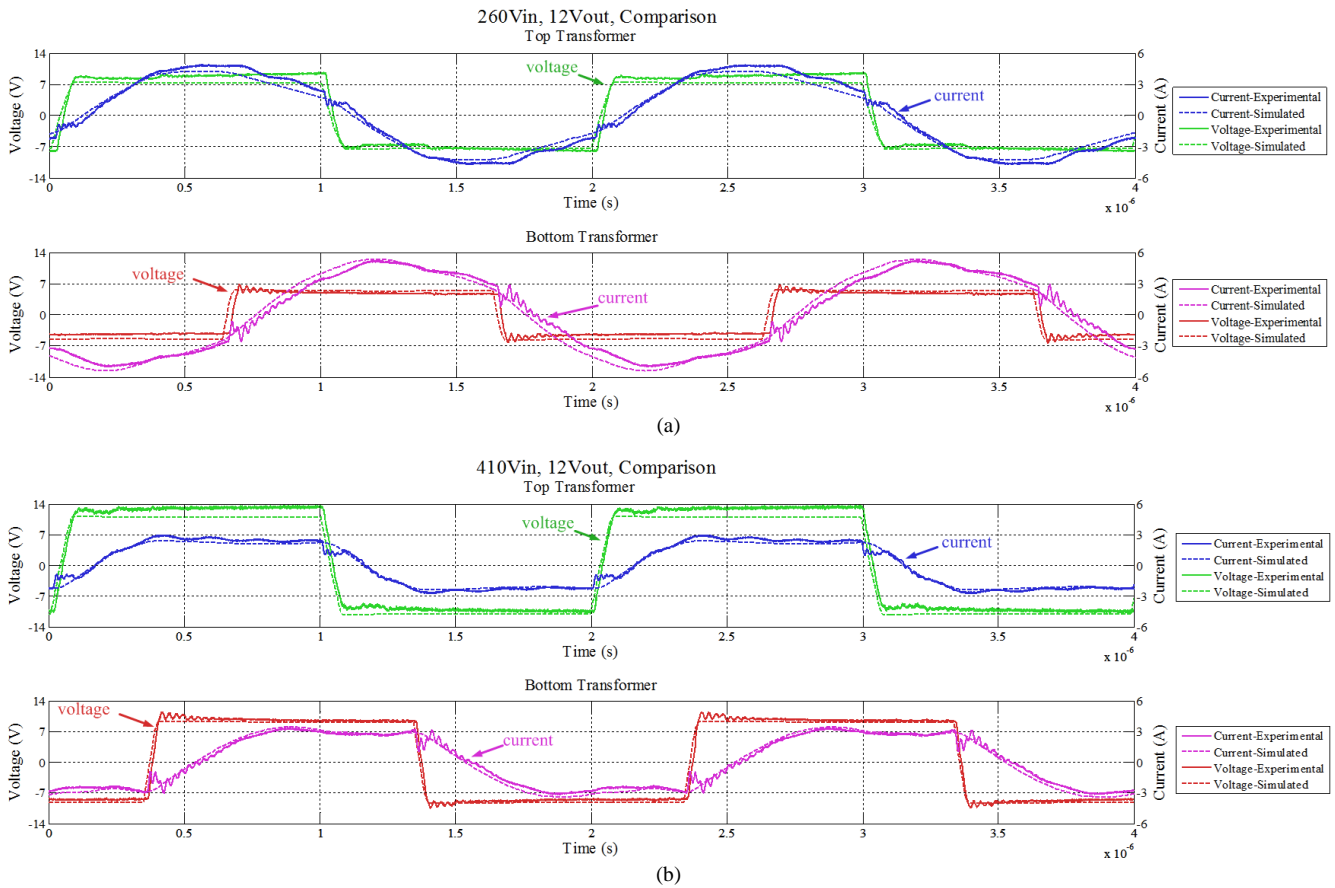

Fig. 12. Simulated and experimental waveforms for input voltages of (a) 260V and (b) 410V. The top pane of each set of waveforms shows the voltage across the secondary of the top transformer and the current into the primary. The second pane shows the voltage across the secondary of the bottom transformer and the current into the primary. For all plots, the solid line is the experimental data and the dashed line is the simulated data.
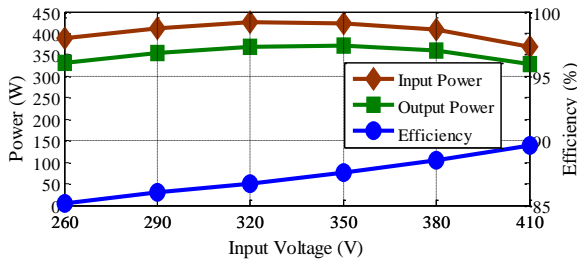
Fig. 13. Experimental results for input power, output power, and efficiency.

theoretical prediction in Section III regarding the ability to provide a very flat power characteristic vs. input voltage. At the same time, the output power is significantly lower than the theoretical prediction. Inefficiencies in the circuit cause the output power to drop below the theoretical value. Theoretical calculations assume lossless components but the real circuit includes several loss mechanisms. In order to understand the dominant loss mechanisms, a loss analysis was performed.

D. Loss Analysis

Figure 14 shows the operating temperature distribution across the voltage range. For this particular prototype, the main loss mechanism is conduction loss as seen in the breakdown of Fig. 15. The total loss is found from the experimental data and the breakdown of the loss is estimated through simulation. Any discrepancy is noted as 'undetermined' and can be due to other loss factors not accounted for in simulation. With an input voltage of 260V, the converter delivers 331.9W to the output and with an input voltage of 410V, the converter delivers 329.2W. Despite delivering roughly the same amount of power, the converter operates much more efficiently at the higher input voltage. This further supports the notion that conduction loss is the dominant loss factor for this prototype because many of the circuit currents are higher for 260V than for 410V. (This loss mechanism is exacerbated by the construction technique used for the prototype.) Thermal imaging (see Fig. 13) also shows that the highest temperature rise is seen beyond the secondary of the transformer, most likely due to the large currents. Ways to improve performance include a greatly refined prototype having a higher degree of integration, optimization of the control and switching dead-time, and fine-tuned impedances.

V. Conclusion

In applications such as 380 V dc distribution in data centers, there is a need for dc-dc converters that can provide large conversion ratios and maintain good operation over a wide range of voltage conversion ratios. In this paper we introduce a resonant power converter architecture that - owing to use of an impedance control network - can maintain desirable operation across a wide voltage conversion ratio. Moreover the use of stacked-bridge techniques enables large voltage conversion ratios to be achieved. We demonstrate this for a 380-to-12 V dc-dc converter for dc distribution that operates across an input voltage range of 260 V to 410 V. The proposed ICN resonant dc-dc converter demonstrates that it accurately matches theoretical predictions and can maintain soft-switching and a flat output power as the input voltage varies.
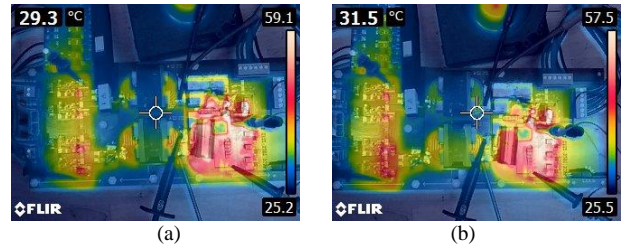

Fig. 14. Thermal images of the board operating at (a) 260V and (b) 410V. A fan can be seen at the top and is intended to keep the output stage (particularly the switching devices) from overheating.
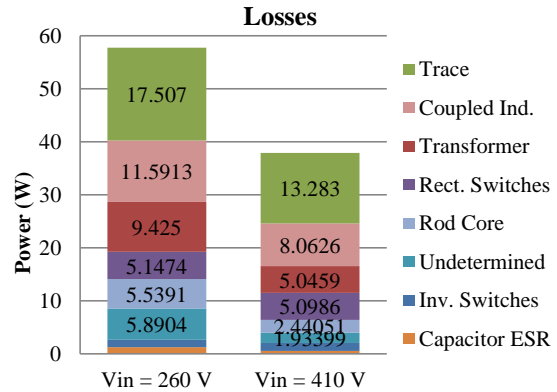

Fig. 15. Breakdown and comparison of loss for input voltages of 260V and 410V. At both of these operating points, the power delivered to the output is approximately equal at around 330W.

VI. Acknowledgment

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