New AC-DC Power Factor Correction Architecture Suitable for High Frequency Operation

Seungbum Lim, *Student Member, IEEE,* David M. Otten, and David J. Perreault, *Fellow, IEEE*

Abstract—This paper presents a novel ac-dc power factor correction (PFC) power conversion architecture for single-phase grid interface. The proposed architecture has significant advantages for achieving high efficiency, good power factor, and converter miniaturization, especially in low-to-medium power applications. The architecture enables twice-line-frequency energy to be buffered at high voltage with a large voltage swing, enabling reduction in the energy buffer capacitor size, and elimination of electrolytic capacitors. While this architecture can be beneficial with a variety of converter topologies, it is especially suited for system miniaturization by enabling designs that operate at high frequency (HF, 3 – 30 MHz). Moreover, we introduce circuit implementations that provide efficient operation in this range. The proposed approach is demonstrated for an LED driver converter operating at a (variable) HF switching frequency (3 – 10 MHz) from 120 V_{ac}, and supplying a 35 V_{dc} output at up to 30 W. The prototype converter achieves high efficiency (92 %) and power factor (0.89), and maintains good performance over a wide load range. Owing to architecture and HF operation, the prototype achieves a high 'box' power density of 50 W/in^3 ('displacement' power density of 130 W/in^3), with miniaturized inductors, ceramic energy buffer capacitors, and a small-volume EMI filter.

Index Terms—ac-dc, high frequency, buck, power factor correction, pfc, power factor, LED, electromagnetic interference, EMI

I. INTRODUCTION

Switched-mode rectifiers for converting power from the single-phase ac grid for dc loads must meet numerous, increasingly stringent requirements. High efficiency has always been a goal of power electronics, and efficiency goals for ac-dc converters continue to rise. Moreover, high power factor (PF) is desirable to best convey real power from the ac grid to a dc load [1]–[3]. While power factor has been traditionally considered important mainly at higher power levels, it is of increasing concern at lower power levels as well (e.g., 10's of watt), as reflected in goals for applications such as light-emitting diode (LED) drivers and laptop chargers [4], [5]. In addition, there has been a long desire for converter miniaturization (e.g., through the use of greatly increased switching frequencies to reduce the volume of energy storage elements [6], [7]). Achieving high reliability/lifetime and high temperature operation (including eliminating use of electrolytic capacitors) is emerging as a further goal in many systems. However, achieving all of these sometimes-conflicting goals – high efficiency, high power factor, miniaturization, and high reliability/lifetime – is particularly challenging, especially at

S. Lim, D. M. Otten, and D. J. Perreault are with the Laboratory for Electromagnetic and Electronic Systems, Massachusetts Institute of Technology, Cambridge, MA 02139 USA (e-mail: sblim@mit.edu).
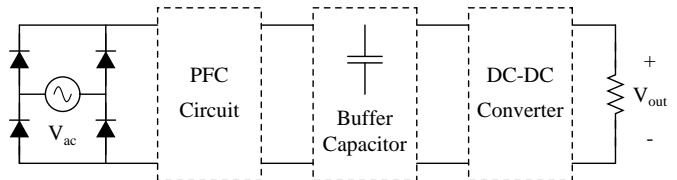

Fig. 1: A conventional ac-dc power converter architecture for moderate-to-high power factor may have a power-factor-correction (PFC) stage (e.g., a boost, flyback, or buck PFC stage), an electrolytic energy buffer capacitor, and a dc-dc conversion stage (e.g, a flyback or forward converter). This approach has limitations in achieving all of high efficiency, high power factor, miniaturization, and high reliability/lifetime demands.

low-to-moderate power levels, motivating development of new approaches.

Section II of the paper reviews and enumerates typical ac-dc converter approaches, and illustrates difficulties in achieving all of the above goals with conventional ac-dc converter approaches. Section III proposes the structure and operation of a new power-factor-correction (PFC) grid interface architecture. The design consideration and trade-offs of the proposed approach are described, and an example simulation is presented with specified design parameters. Section IV describes the detailed characteristics and advantages. The approach is demonstrated in the context of a high-frequency LED driver circuit that converts 120 V_{ac} to 35 V_{dc}. Section V of the paper presents a circuit implementation that leverages the advantages of the proposed architecture to operate efficiently at 3 – 10 MHz, and shows experimental results demonstrating the proposed system. Finally, Section VI concludes the paper.

II. BACKGROUND

For an ac-dc system requiring high power factor, one conventional configuration comprises the cascade of a PFC converter circuit, a large (usually electrolytic) capacitor for buffering twice-line-frequency energy, and a following dc-dc converter providing one or more of: output regulation, voltage transformation, and galvanic isolation, as illustrated in Fig. 1. In this approach, the PFC circuit – often a boost converter, but sometimes a buck or other topology – shapes the input current waveform over the ac-line cycle for high power factor (often providing a sine-wave or clipped-sine-wave input current waveform), with associated twice-line-frequency power fluctuations buffered by its output capacitor.

The following dc-dc converter then takes the voltage across the energy buffer capacitor (i.e., the output voltage of the PFC circuit, which typically has moderate ($5-10\%$) twice-line-frequency voltage ripple), and supplies and regulates the system output voltage.

A boost converter is often selected for the PFC circuit because of its filtered input current, high efficiency, and high power factor capability [1]–[3]. This approach may yield high efficiency and very high power factor, but it is not amenable to converter miniaturization in low dc voltage and low-to-medium power applications, because 1) it is hard to greatly reduce the volume of the boost circuit (e.g., through high-frequency operation) owing to loss limits, large inductance (i.e., high characteristic impedance level), and large parasitic capacitance levels (e.g., large output capacitance of the switch) [6]–[8], and 2) the following dc-dc converter operates at high voltage and has a large step-down voltage conversion ratio, so that it is again difficult to be designed at high frequency with small volume, and 3) the volume of the energy buffer capacitor is large.

One alternative circuit topology for the PFC circuit is a buck converter, which can draw a clipped-sinusoidal current waveform with $0.7-0.95$ power factor, suitable for many applications [9]–[11]. A benefit of the buck PFC circuit for low-output-voltage applications is reduced voltage stress and voltage conversion ratio for the following dc-dc converter. The buck PFC circuit, however, still needs to be operated directly from the ac-line voltage, and thus should be designed with high-voltage active devices (i.e., rated for line voltage). The large characteristic impedance level of the converter and large parasitic capacitance of the high voltage switch and diode devices limit the switching frequency and power density of the buck PFC approach.

Several other PFC configurations are designed to improve the performance of the converter. For example, for the designs illustrated in [12] and [13], the voltage stresses of switches and diodes are reduced by splitting voltage across the energy buffer capacitor to several dc-bus capacitors and/or by utilizing a multilevel cell structure, so that higher efficiency may be achieved with smaller voltage rating devices. Each of these approaches adds benefits in various aspects of the PFC problems, but none of them are particularly suited to major increases in switching frequency for dramatic miniaturization and for elimination of electrolytic capacitors.

The power density of conventional ac-dc converters for low-to-moderate power levels (e.g., $10-100\,\mathrm{W}$) is relatively low (typically $<5\,\mathrm{W/in^3}$ based on a survey of commercial and academic LED driver designs). These converters are dominated by bulky power stage magnetic components, large EMI filters necessary to filter the low frequency switching components (switching frequencies typically <150 kHz), and electrolytic capacitors for buffering twice-line-frequency energy. Their required size results from the conversion architectures and associated topologies used, which impose high individual device and component voltage stresses, high switching loss, and component characteristic impedances, each of which tends to limit high switching frequency operation and converter miniaturization. Moreover, most conventional approaches are

unable to exploit a substantial fraction of the energy storage capacity of their line frequency energy buffer capacitors (since the capacitors operate at small voltage ripple), necessitating the use of large electrolytic capacitors having significant reliability and lifetime constraints. Miniaturization with high performance of PFC converters in this space thus remains a major challenge, and new grid interface PFC architectures and topologies that can overcome these constraints are needed.

Here we propose a new ac-dc conversion architecture and associated circuit implementations that seek to simultaneously address these challenges (e.g., high efficiency, high power factor, miniaturization, and high reliability/lifetime). The approach is suitable for realizing ac-dc converters that switch in the HF range ($3-30$ MHz) with relatively low-voltage components and with zero-voltage switching (ZVS) condition, enabling significant converter size reduction while maintaining high efficiency. Moreover, the proposed approach can achieve reasonably high power factor (e.g., about 0.9, which is sufficient for many applications such as LED driver circuits and laptop power supplies [4], [5]), while dynamically buffering twice-line frequency energy using small capacitors operating with large voltage swings over the ac line voltage cycle. The proposed converter thus shares the benefits of some "third port" architectures for buffering line frequency energy (e.g., [14]–[20]), in that it can achieve high energy storage density without the use of electrolytic capacitors.

III. PROPOSED SYSTEM ARCHITECTURE

The proposed architecture is illustrated in Fig. 2. It comprises a line-frequency rectifier, a stack of capacitors across the rectifier output, a set of regulating converters having inputs connected to capacitors on the capacitor stack and outputs that are regulated to a desired level, and a power-combining converter (or set of power combining converters) that combines the power from the outputs of the regulating converters to provide a single output.

The line-frequency rectifier draws current from the grid during a portion of the cycle, with a waveform controlled by the operation of the regulating converters. The capacitor stack provides most or all of the twice-line-frequency energy buffering, such that the converter can provide high power factor without buffering energy at the system output. One or more of the capacitors in the capacitor stack is relatively small, such that the total capacitor stack voltage can vary over a wide range as the line voltage varies over the line cycle. The input ac current waveform may approximate a clipped sine waveform or a similar waveform providing high power factor, while the total capacitor stack voltage closely follows the amplitude of the line voltage over the portion of the line cycle for which the rectifier conducts.

A set of regulating converters, which have their inputs connected to capacitors of the stack of capacitors, provide regulated outputs. The currents drawn by the (at least) two regulating converters are modulated to draw energy from the capacitors, such that the currents drawn from the capacitor stack results in an input current waveform to the rectifier that provide both high power factor and the total needed energy
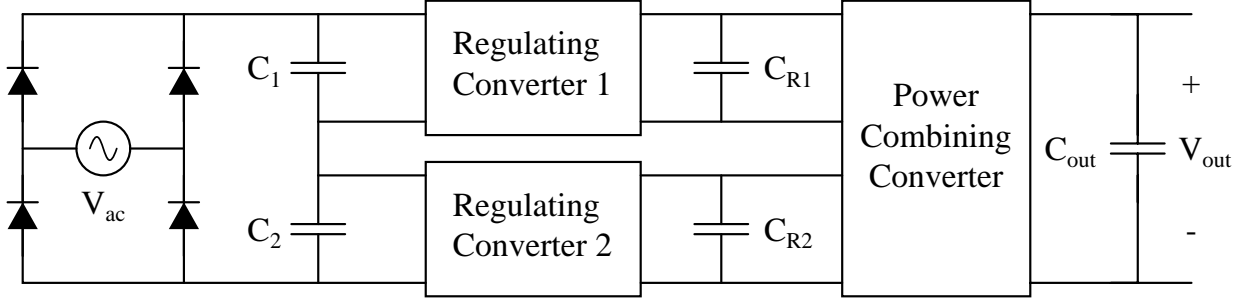
Fig. 2: The proposed grid interface power conversion architecture comprises a line-frequency rectifier, a stack of capacitors, a set of regulating converters, and a power combining converter.
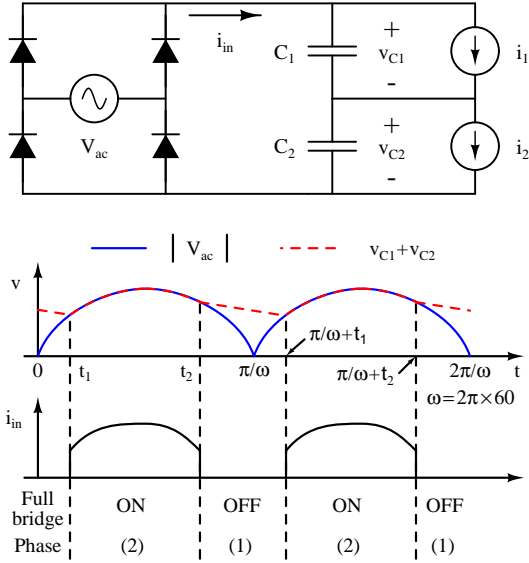

Fig. 3: A simplified front-end circuit model of the proposed architecture with example voltage and current waveforms. The currents i_1 and i_2 models the average current (averaged over a switching cycle of the regulating converters) drawn by regulating converter 1 and regulating converter 2, respectively. The regulating converters modulate their current draw over the line cycle and result in an input current waveform with high power factor.

transfer to support the output. Because the regulating converters operate from voltages that are much smaller than the total line voltage, they can be designed with switches having smaller voltage ratings than otherwise possible (and having lower parasitic capacitance) at much higher frequencies and can be operated at smaller characteristic impedance levels than could a single converter rated at line voltage (e.g., as described in [7], [8]). Many converter topologies can be considered as a regulating converter of the proposed architecture. For example, as described later, the regulating converters may be very effectively implemented using resonant-transition discontinuous-mode inverted buck converters [8], [21]. This topology enables high-frequency (HF, 3 – 30 MHz) operation of the regulating converters with high efficiency, low device voltage stress, small component size, and good control capability.

The power-combining converter has a plurality of inputs connected to the regulating converter outputs, wherein the power-combining converter draws energy from the regulating converter outputs and delivers the combined power to the converter system output. The power-combining converter may provide one or more of: voltage balancing among the regulating converter outputs, galvanic isolation, voltage transformation, a portion of twice-line-frequency energy buffering, and additional regulation of the output. The power-combining converter may be designed as a multi-input converter, or as a set of single-input converters which take inputs connected to ones of the regulating converter outputs and supply a single output. Because the power combining converter operates from a low, narrow-range input voltage, and may not need (in many designs) to provide regulation, it can be designed to be very compact. One possibility in this case is to design it for operation at HF or VHF [6]. Another possibility is to design the power combining converter using switched-capacitor (SC) techniques, as demonstrated here. When the system does not require galvanic isolation, the SC circuit can be designed without magnetic elements, and has benefits including high efficiency and small size [8], [22]–[25].

A. Line-Frequency Energy Buffering

Before introducing an implementation example with a specific regulating and power combining circuit topology, we describe how the proposed ac-dc PFC architecture operates to buffer twice-line-frequency energy with high power factor while supplying the desired dc power to the load.

Fig. 3 shows a simplified model of the front end of the proposed grid interface architecture along with example operating waveforms. The two current sources (i_1 and i_2) model the average currents drawn by the regulating converters over the switching period. The regulating converters and power combining converter are assumed to be ideal (without loss), so that the average powers drawn by regulating converters over the switching period are losslessly combined to supply system load (e.g., $P_{Reg-Con\,1} = v_{c1}(t)\,i_1(t)$, $P_{Reg-Con\,2} = v_{c2}(t)\,i_2(t)$, and $P_{System} = v_{c1}(t)\,i_1(t) + v_{c2}(t)\,i_2(t)$).

The circuit cycles in two phases across a half line cycle. During phase 1, the input ac voltage amplitude is lower than the total voltage of the stacked capacitors; the full-bridge

rectifier is off and there is no current drawn from the grid. During this phase, capacitors C_1 and C_2 are discharged by the regulating converters and the voltage across the capacitor stack decreases. When the input ac voltage amplitude reaches the total capacitor stack voltage, the full-bridge turns on and the circuit enters phase 2.

During phase 2, the total voltage of stack capacitors tracks the rectified ac input voltage, and the input current follows the sum of the currents into C_1 and regulating converter 1 (which is same to the sum of the currents into C_2 and regulating converter 2). When the regulating converters no longer discharge the capacitor stack voltage fast enough to follow the decrease in line voltage, the full-bridge turns off and the circuit enters phase 1.

Assuming that the regulating converters draw currents (averaged over a switching cycle of the regulating converters) $i_1(t)$ and $i_2(t)$, and that the power combining converter combines power (from the two regulating converters) without loss and continuously supplies the required output power $P_o(t)$, the mathematical expressions for each phase are as shown in equations $(1)-(11)$. It should be noted that during phase 2 equations (10)[1] and (11) are calculated from equations $(5)-(9)$, and the $i_1(t)$ and $i_2(t)$ currents result in the pre-defined input current of the system over the line cycle providing good power factor. There are many relations among the stack capacitor values, power level, capacitor voltage variation, regulating converter operating range, and power factor. Thus, selecting appropriate topologies, design values, and operating waveforms is essential.

B. Design Considerations and Trade offs

In this section, we consider sizing of the energy buffer capacitor, and describe its interaction with other system considerations such as input waveform selection. The following

[1]Equation (10) can be derived by differentiating (5) and inserting relations from (6)-(9).

section III-C further illustrates this using simulation with the selected design parameters.

A key design parameter in terms of both size and power factor is selection of the capacitor values C_1 and C_2. A preferred approach – used here – is to size the capacitors asymmetrically (one large, one small), such that one of the capacitors (e.g., C_2) buffers most of the twice-line-frequency energy, while the other capacitor (e.g., C_1) is much smaller, and simply acts as a bypass capacitor for its associated high-frequency switching stage. One capacitor is thus sized principally based on line-frequency energy buffering, while the other is sized principally based on switching frequency considerations.

In this paper we design with small capacitor C_1 and large capacitor C_2, such that the capacitor C_2 mainly buffers the twice-line-frequency energy of the converter. In this case, the voltage of capacitor C_2 fluctuates over the line cycle as it buffers the ac energy, and we select its value such that it can buffer the needed amount of energy at maximum power operation while having an acceptable voltage swing (preferably up to approximately a 2:1 voltage swing, thus utilizing up to approximately 75% of the capacitor energy storage capability). If we make the simplifying assumption of ideal unity power factor, the voltage fluctuation follows equation 12:

ideal power factor

$$1/2\ C_2\ V_{\max}^2\ -\ 1/2\ C_2\ V_{\min}^2\ =\ P_0\ /\ \omega_{\text{ac-line}} \quad (12)$$

As one uses a smaller energy buffer capacitor C_2 or operates with a lower-power-factor waveform, the energy buffer capacitor voltage varies across a wider voltage range over the line cycle. The regulating converter 2 then needs to be operated over this wider voltage range, which can degrade the size and performance of the regulating converters. In contrast, the value of the capacitor C_2 can be selected to be very large so that its voltage swing is small over the line cycle, but results in large buffering capacitor volume and reduces power

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- Phase 1 : $0 < t < t_1$ and $t_2 < t < \pi/\omega$ – full-bridge is off and conducts zero input current

$$i_{in}(t)\ =\ 0 \quad (1)$$

$$P_o(t)\ =\ v_{C1}(t)\ i_1(t)\ +\ v_{C2}(t)\ i_2(t) \quad (2)$$

$$i_{c1}(t)\ =\ C_1\ \frac{dv_{C1}(t)}{dt}\ =\ -i_1(t) \quad (3)$$

$$i_{c2}(t)\ =\ C_2\ \frac{dv_{C2}(t)}{dt}\ =\ -i_2(t) \quad (4)$$

- Phase 2 : $t_1 < t < t_2$ – full-bridge is on and conducts $i_{in}(t)$ input current

$$v_{ac}(t)\ =\ V sin\omega t\ =\ v_{c1}(t)\ +\ v_{c2}(t) \quad (5)$$

$$i_{in}(t)\ =\ i_{c1}(t)\ +\ i_1(t)\ =\ i_{c2}(t)\ +\ i_2(t) \quad (6)$$

$$P_o(t)\ =\ v_{c1}(t)\ i_1(t)\ +\ v_{c2}(t)\ i_2(t) \quad (7)$$

$$i_{c1}(t)\ =\ C_1\frac{dv_{c1}(t)}{dt} \quad (8)$$

$$i_{c2}(t)\ =\ C_2\frac{dv_{c2}(t)}{dt} \quad (9)$$

$$i_1(t)\ =\ \frac{C_1\ C_2\ v_{c2}(t)}{C_2\ v_{c2}(t)\ -\ C_1\ v_{c1}(t)}\ \left[\left(\frac{1}{C_1}+\frac{1}{C_2}\right)i_{in}(t)-\omega V cos\ \omega t\ -\ \frac{P_o(t)}{C_2\ v_{c2}(t)}\right] \quad (10)$$

$$i_2(t)\ =\ \frac{1}{v_{c2}(t)}\ (P_o(t)\ -\ v_{c1}(t)\ i_1(t)) \quad (11)$$

density. Thus, the energy buffer capacitor (C_2) can be scaled down as long as the capacitor voltage swings within the input voltage range of the designed regulating converter. It is the authors' experience that designing the capacitor voltage for an approximately 2:1 (Vmax:Vmin) voltage swing provides a good trade off In practice, one can start with the energy storage prediction of equation (12) as a lower bound to size the capacitance, and then scale the capacitor value up to account for reduced power factor operation (with practical waveforms), to account for capacitor nonlinearity, and to provide design margin.

If the capacitors are sized fully asymmetrically, the other capacitor (e.g., C_1) can be designed to have a small value sufficient to act as an input bypass capacitor of its associated regulating converter such that it filters the converter's switching ripple current. In addition, it should be noted that there is a motivation not to make this capacitor too large, as the capacitor draws an input current component owing to the ac voltage envelope. It is desirable to make this capacitor small enough that this current component is small compared to the active line current that is drawn, as illustrated in equation 13:

$$i_{C1}(t) \quad \text{(when regulating converter 2 is off)}$$
$$= C_1 \frac{dV_{c1}}{dt} = C_1 \omega_{ac-line} V \cos \omega_{ac-line} t \ll P_o/V \quad (13)$$

Based on these considerations, one typically makes the bypass capacitor well more than an order of magnitude smaller than the energy buffer capacitor.

Another key consideration in controlling the converter is to select the desired input current waveform over a line cycle. From the designed input current waveform, the system should operate in periodic steady state over the line cycles such that the voltages across C_1 and C_2 remain within the operating voltage range of the regulating converters, while providing good power factor. In addition to maintaining high power factor, it is desirable to limit the instantaneous peak power processing requirement of the individual converter cells. Of course there are an infinite variety of waveform patterns that can meet these broad goals (for reasonable values of power factor.) One way to perform waveform selection is by iteratively selecting waveforms for given set of design parameters (e.g., capacitor values, power factor, output power P_o, and operating voltage range of the regulating converter) and numerically calculating performance over a half line cycle using $(1)-(11)$.

C. Circuit Simulation

To demonstrate the operation of the proposed architecture, we present time-domain simulations of the system front-end using the model of Fig. 3 and equations $(1)-(11)$. As illustrated in section III-B, there are various trade-off constraints to design the converter; we present a design example and show its operation through simulation.

The simulation is for an ac-dc converter operating from 60 Hz, 120 V_{ac} and supplying 35 V and 30 W of output power; this example matches the experimental prototype described in the following section. Each regulating converter is assumed to be able to operate across a $35-100$ V input voltage range and to be able to deliver power unidirectionally from its input to the power combining circuit (with the power combining converter assumed to combine powers from the regulating converters without loss). Using equations 12 and 13 with the specified power level and operating input voltage range of the regulating converter, the stack capacitors are picked as $C_1 = 1\,\mu F$ and $C_2 = 50\,\mu F$.

To achieve the highest power factor for a given converter voltage operating range, a clipped-sinusoidal current waveform is desirable. However, considering the clipped-sinusoidal input current with other design factors, the regulating converters would be required to process bi-directional power (i.e. negative input current for the regulating converters) for constant output power delivery. To utilize the selected regulating converter topology (uni-directional power flow), we adjusted the input current waveform such that the regulating converters only need to deliver positive current. In consequence, the current of regulating converter 2 turns off when its current hits zero (usually when the ac voltage is high) and during this duration only regulating converter 1 tracks ac input voltage. In this circumstance, to deliver constant power to the load (if we regard C_1 as small capacitor, such that the charging current through C_1 may be neglected), the input current should be $P_o/(V\sin\omega t - V_2(t))$.

Consequently, among many possible input current waveforms, we suggest that of equation 14 as a good one to be used in the system. The detailed current waveform shown in Fig. 4a is derived based on this wave-shape (e.g., with transition points determined through iterative simulations).

$$i_{in} = \begin{cases} 0 & 0 < t < t_1 \text{ and } t_2 < t < \pi/\omega \\ I\sin\omega t & t_1 < t < t_A \text{ and } t_B < t < t_2 \\ P_0/(V\sin\omega t - V_2(t)) & t_A < t < t_B \end{cases} \quad (14)$$

For the proposed design and operating point, the initial voltages on capacitors C_1 and C_2 (at the line zero crossing) are 35 V and 70 V, respectively, for the steady-state operation over the line cycle. Figs. 4 (a)–(f) show the simulation results for this case. Fig. 4a shows the input current waveform programmed to be drawn from the ac line, providing high power factor (about 0.9) and almost constant output power while limiting peak operating power and satisfying the system design constraints of the regulating converters.

With the specified input current waveform and design parameters, the currents of each regulating converter and stack capacitor voltages are calculated from equations $(1)-(11)$ and plotted as shown in Figs. 4b and 4c. As can be seen in Fig. 4b, the current drawn by each regulating converter is always positive (unidirectional power flow). Moreover, as shown in Fig. 4c, the voltages of the two "stack" capacitors vary over the line cycle as they are dynamically charged and discharged by the regulating converters, remaining within the operating voltage range of the selected regulating converters (i.e., $35-100$ V), and the system operates in periodic steady state over the line cycle (i.e., the capacitor voltages are the same at the beginning and end of the half line cycle.)

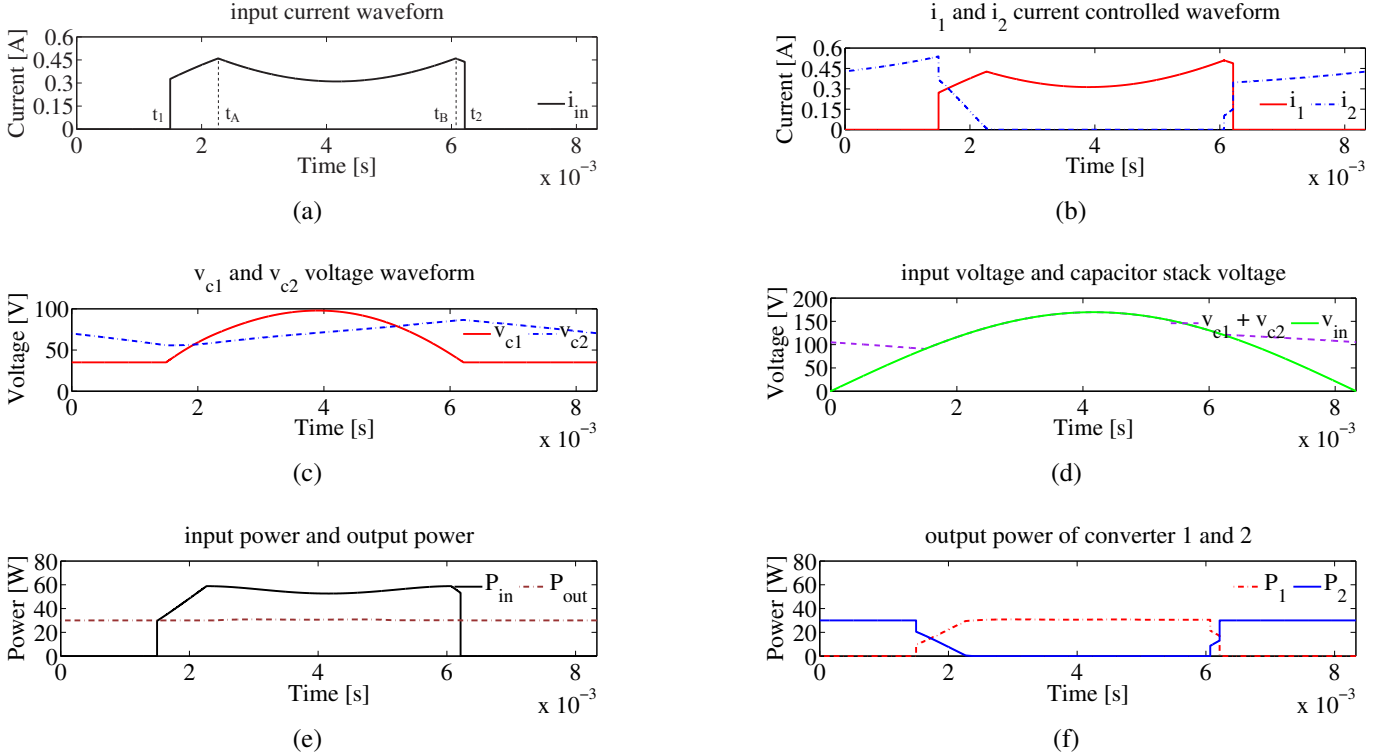Fig. 4d shows the line voltage and total capacitor stack

input current waveform

(a)

i_1 and i_2 current controlled waveform

(b)

v_{c1} and v_{c2} voltage waveform

(c)

input voltage and capacitor stack voltage

(d)

input power and output power

(e)

output power of converter 1 and 2

(f)

Fig. 4: Simulated waveforms illustrating the operation of the proposed PFC when it connects to $120\,\mathrm{V_{ac}}$ $60\,\mathrm{Hz}$ ac line voltage at $\mathrm{P_{out}} = 30\,\mathrm{W}$ with $C_1 = 1\,\mu\mathrm{F}$ and $C_2 = 50\,\mu\mathrm{F}$, respectively. In this simulation, the initial values for $v_{c1,i}$ and $v_{c2,i}$ are assumed to be $35\,\mathrm{V}$ and $70\,\mathrm{V}$, respectively. (a) Input current waveform (a folded-clipped sinusoidal current waveform is selected). (b) Currents i_1 and i_2 (average currents drawn by the regulating converters). (c) Stack capacitor voltages v_{c1} and v_{c2}. (d) ac voltage v_{in} and capacitor stack voltage $v_{c1} + v_{c2}$. (e) Input power $\mathrm{P_{in}}$ and output power $\mathrm{P_{out}}$ (total of power delivered by the regulating converters). The proposed PFC architecture can dynamically buffer the twice-line-frequency energy through modulation of the current drawn by the regulating converters such that the net output power is approximately constant over the line cycle. (f) Power drawn by regulating converters, which total to the output power.

voltage over a half line cycle. From Figs. 4c and 4d it can be seen that the asymmetric sizing of the stack capacitors enables the stack voltage to track the line voltage (when the full-bridge rectifier conducts and draw line current) over a large portion of the line cycle, while also buffering the twice-line-frequency energy (mainly on capacitor C_2).

The input power $\mathrm{P_{in}}$ from the line and the output power $\mathrm{P_{out}}$ (total of the powers drawn from the capacitor stack by the regulating converters) are shown in Fig. 4e. The proposed architecture controls the regulating converters to buffer the twice-line-frequency energy on the stack capacitors, such that the total output power from the two regulating converters is almost constant. As illustrated in Fig. 4f, the two regulating converters split the total power over the line cycle, and each regulating converter has a peak rating corresponding to the total (line-cycle-average) output power of the system.

As illustrated in the above example, the front-end of the proposed architecture accomplishes three functions: First, it draws power from the line at high power factor. Second, it buffers twice-line-frequency energy from the line on the capacitor stack, such that constant power can be delivered to the system output. Lastly, while it is not explicitly shown

above, the front end steps down the large input voltage, and provides narrow-range regulated outputs for the power combining stage.

IV. System Characteristics

A. System Advantages

The proposed grid interface architecture has several advantages. One apparent benefit is the decreased voltage stress to the components in the regulating converters and the power combining converter relative to the line voltage. In comparison to conventional grid interface converters which must be rated for the grid voltage, each regulating converter of the proposed architecture instead operates only up to about half of the grid voltage because of the stacked capacitor structure (with an increased number of "stack" capacitors and regulating converters, this voltage stress may be further reduced as illustrated in the Appendix and Fig. 12.) Moreover, the power combining converter, tied to the regulated outputs of the regulating converters, operates at both low voltage and narrow input voltage range. With the reduced voltage rating, one can design converter with smaller voltage rated

devices which are packed in a smaller package and have improved on-resistance characteristics (e.g., the on-resistance of a transistor is typically proportional to the square of the rated voltage; likewise, flip-chip devices (representing devices with the smallest "packaging" and lowest interconnect parasitics presently achievable) are only available for relatively low-voltage devices (e.g., below 450 V) owing to voltage-based pad limits). Thus, the proposed approach facilitates high-frequency operation and miniaturization of converter with high efficiency.

Furthermore, the proposed ac-dc architecture has significant efficiency and miniaturization advantage for low voltage applications. Compared to the common boost PFC architecture (which steps up the voltage and then steps down with a following high voltage transformation ratio dc-dc converter), large step down conversions are more readily achieved, aided by the stacked nature of the front end conversion system and - in some cases - supplemented by further step down from the power combining converter.

Another advantage is that the architecture enables substantial increases in operating frequency as compared to conventional designs, enabling a further degree of miniaturization. (In fact the driving consideration of the proposed approach is that it is amenable to much higher frequencies than conventional designs, especially for low-voltage outputs at low-to-moderate power levels.) Converters running at high voltages and low currents operate at high impedance levels, and consequently utilize relatively large inductors and small capacitors (e.g., characteristic impedance $Z_0 = \sqrt{L/C}$ scales as V / I). Furthermore, inductor and capacitor values scale down with increasing resonant frequency (e.g., $f = 1/(2\pi\sqrt{LC})$). Thus, for a given topology, increasing frequency beyond a certain point may lead to capacitance values that are too small to be practically achievable (e.g., given parasitics such as parasitic capacitance of switch and diodes), placing a practical bound on frequency and miniaturization. For miniaturization of converters at high voltage and low power, it is preferable to select system architectures and circuit topologies that require relatively low characteristic impedance values (i.e., small inductances and large capacitances) to reduce constraints on scaling up in frequency. The proposed architecture roughly divides the input voltage range of each regulating converter by two, by stacking two regulating converters, and thus decreases the required inductance and increases the allowable capacitance. Higher switching frequencies (bounded by practically achievable capacitance levels) are thus enabled by this approach, such that the converter can be designed with small-size inductors [7], [8]. High frequency operation further helps converter miniaturization with the reduced EMI filter requirements. This consideration is further described in Section V.

In addition to the miniaturized magnetic component sizes attainable through high frequency operation, the proposed PFC architecture enables use of a small-valued energy-buffer capacitor. For a single-phase ac-dc converter with high power factor, the difference between instantaneous input power from the line and constant dc output power (twice-line-frequency energy) should be buffered inside of the converter. This twice-line-frequency energy ($E_b = P_o/\omega_{ac-line}$ for unity power factor) is not related to the switching frequency of the converter, but related to the system power level and the ac line frequency. By utilizing a relatively large voltage swing on the storage capacitors C_1 and/or C_2, a substantial fraction of the energy storage capacity of the capacitor can be used, such that small-valued capacitors can be employed (i.e., the buffered energy is related to the voltage swing on the energy buffering capacitor: t current there. Employing a large swing (i.e., large ΔV) enables film or ceramic capacitors to be employed instead of electrolytic capacitors, which can benefit lifetime, temperature rating, and reliability of the system (though possibly increasing cost).

Lastly, it should be noted that for some power combining topologies and applications (e.g. the switched-capacitor converter shown in Fig. 5 and described hereinafter), one of the two regulating converters can directly supply the system output, and the combining converter only need process a portion of the power. This can be regarded as reducing the redundant processing power in the converter, and contributes to improved efficiency [14].

V. Implementation and Experimental Results

In this section we describe topology selection and design of a highly-miniaturized ac-dc prototype converter for LED drive applications. The converter operates at a (variable) HF switching frequency of $3-10$ MHz from 120 V_{ac}, supplying a 35 V output at up to 30 W. As will be shown, this enables a "box" power density of 50 W / in^3 and a component "displacement" power density exceeding 130 W / in^3, far in excess of typical designs in this space.

A. Topology Selection and Implementation

The proposed architecture enables substantial miniaturization through adoption of greatly increased switching frequencies for the regulating converters. Increases in switching frequency are desirable because the numerical values of inductors and capacitors vary inversely with switching frequency. However, the sizes of passive components do not necessarily decrease monotonically with frequency, owing to magnetic-core loss, magnetic conduction loss, and heat transfer limits [6]. In addition to loss considerations, the practical values of required components can also limit achievable switching frequency (i.e., yielding impractical values compared to inherent parasitics as frequency increases). This is a particular challenges in converters operating at high voltage and low current as described above. Consequently, achieving substantial miniaturization through high frequency operation further relies upon appropriate passives design and careful selection of circuit topology to minimize the demands placed upon the passive components, especially the magnetic components.

To address the design considerations and achieve high efficiency and high power density, the regulating converters are designed as inverted resonant buck converters as shown in Fig. 5. The regulating converter is designed with single switch, diode, and small inductor, and operates around $3-10$ MHz frequency similar to the regulation-stage design illustrated in [7], [8]. It is an "inverted" circuit in the sense that it is designed with "common positives" (i.e., the positive node of

TABLE I: Components of the prototype converter

Stack of Capacitors	
C_1	1 μF X7R Ceramic 100 V
C_2	210 μF (15 μF $\times$ 14) X7S Ceramic 100 V
Regulating Converter	
Q_{R1}, Q_{R2}	GaN switch EPC 2012
D	Schottky diode STPS30120DJF
L	800 nH; 10 turns on a Micrometals P68-106 core
Power Combining Converter	
switch	GaN switch EPC 2012
C_{SC1}, C_{SC2}	20 μF X7R Ceramic 100 V
Control	
Microcontroller	Atmel ATtiny 1634
EMI filter	
L_f	47 μH, Coilcraft 1008PS
C_f	10 nF, Ceramic X7R 200V

the converter's input voltage is common with the positive node of its output voltage.) For much of its operating range, the topology acts like a quasi-square-wave ZVS buck converter with a low ratio of switching to resonant frequency [26]. Each regulating converter takes as an input one of the capacitor voltages (from the stack of capacitors) and provides a regulated voltage across its output capacitor.

This regulating converter design has several benefits. First, it operates efficiently with ZVS or near-ZVS switching conditions across the $35-100$ V wide input voltage range. Second, the single common-referenced switch (referenced to a slowly-moving potential) makes it suitable for operation at HF ($3-30$ MHz). It should be noted that in our prototype converter the regulating converter is designed with a flip-chip Gallium nitride (GaN) on silicon switch, which yields small on-resistance and parasitic capacitance and a compact device size, facilitating high frequency operation. Third, it requires only a single, small-valued inductor. Furthermore, it has very fast response (near single cycle) to input voltage transients and changes in the output current command. Finally, for a given input voltage, the output current is directly related (roughly proportional) to transistor on-time, allowing a variety of control schemes to be employed.

For the power combining converter, we selected an interleaved switched-capacitor (SC) circuit as shown in Fig. 5. The SC circuit draws energy from the two regulating converter outputs and supplies the single system output (which is also the output of one of the regulating converters). This selected SC circuit is an effective choice for high efficiency and power density, because the SC circuit needs not provide regulation in our architecture (as described in sections III and IV), and just transfers charge without voltage regulation [22]. The SC power combining circuit, thus, can be designed with switches and capacitors without magnetics, and can be compactly designed with high efficiency. In the proposed SC circuit, the capacitors C_{SC1} and C_{SC2} transfer charge from capacitor C_{R1} to capacitor C_{R2} and supply the combined power to the load. Since the load is connected across the output of one of the regulating converter, the SC circuit only processes a portion of overall system energy in this design.

Using the selected regulating and power combining converter topologies described above, we implemented an example system, which connects to a $120\,V_{rms}$ ac grid input voltage and supplies up to 30 W power to a 35 V dc load (e.g., an LED string). We utilize the control strategy described and demonstrated in Section III. The system comprises a line-frequency bridge rectifier and a small EMI filter; a stack of two capacitors; a pair of regulating resonant-transition inverted buck converters; and an unregulated SC power-combining converter having two inputs and an output supplying the system output.

For the stack capacitor design, one should be careful to pick appropriate capacitance values. As illustrated in section III, the proposed architecture can dynamically buffer the ac energy with asymmetric capacitors, (e.g., $C_1 = 1\mu$F and $C_2 = 50\,\mu$F at 30 W power level). In selecting practical capacitors, it must be recognized that the capacitance of high-k ceramic capacitors degrades with bias voltage. Consequently, we used a $1\,\mu$F, 100 V X7R capacitance for C_1 and a (nominal) $210\,\mu$F (15μF $\times$ 14), 100 V X7S ceramic capacitance for C_2 (on which the ac energy is mainly buffered).

The ZVS HF driver control circuitry includes high-speed comparators, resistor divider, and logic ICs for each regulating converter as illustrated in Fig. 6. The current of the regulating converter is roughly proportional to the on-time of the switch and thus high-frequency control circuit can be designed in a manner similar to that described in [8]: The controller detects when the switch drain-source voltage is zero or near zero with a fast comparator and turns on the buck switch with ZVS, and then it turns off the switch after a specified switch on time. The details of high frequency driver circuit are further described in [8].

In addition to high-frequency driver circuitry, the system controls the currents of each regulating converter over the line cycle for a given load as illustrated in section III. To modulate the average current drawn by each regulating converter, the on-time of the converter is adjusted at low (line) frequency with a microcontroller (Atmel, ATtiny 1634). The microcontroller detects zero crossing of the ac line voltage, and monitors the capacitor stack voltage (the input voltage of each regulating converter) via a voltage divider and ADC. Then, it sends appropriate switch on-time information to the high-frequency driver circuit of the regulating converters every $80\,\mu$s (On a time scale that is long compared to the switching period of the regulating converter of around $100-300$ ns). Moreover, the microcontroller generates the 30 kHz 50 % duty ratio switching signal (with dead time) for the SC power combining circuit as shown in Fig. 5.

Table I shows the component selection of the prototype converter shown in Figs. 5 and 7. With these components, the regulating converters operate at high frequency with ZVS soft-switching or low-loss near-ZVS switching conditions over their input voltage and power range. The SC circuit is also designed with ceramic capacitors and GaN switches, and operates at a fixed switching frequency of 30 kHz. Fig. 7 shows photographs of the implemented prototype converter.
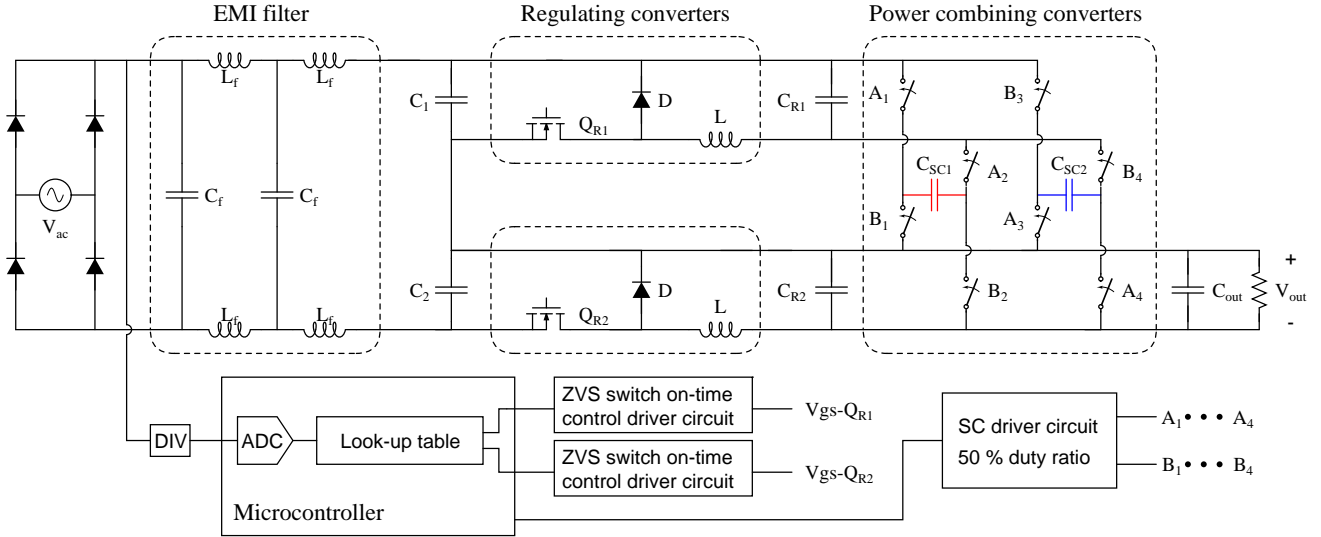
Fig. 5: This figure shows an implementation of the proposed grid interface architecture for non-isolated applications such as LED drivers. The regulating converters are designed as resonant-transition inverted buck converters operating at high frequency $(3-30\,\text{MHz})$. The switch is operated by the comparator based on-time controller described in Fig. 6 and [8] and the switch-on-time is modulated by the microcontroller based on a look-up table. The power combining converter is a switched-capacitor converter operating at moderate frequency (e.g., 30 kHz), and also controlled by the microcontroller with 50 % duty ratio. An implementation of this system is illustrated in Fig. 7.
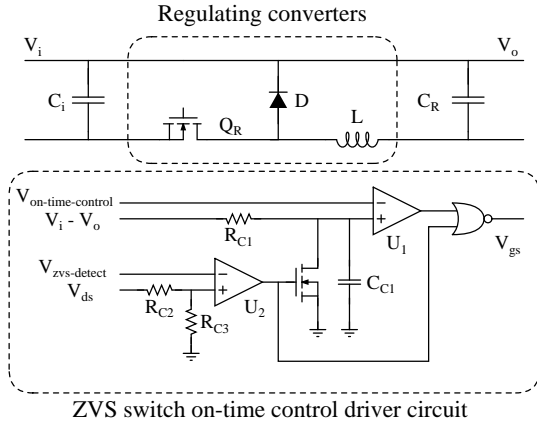

Fig. 6: Schematic of the HF regulation control circuit. This control circuit is designed to regulate the average inductor current by changing the switch on-time, and to operate the HF stage at zero-voltage or near zero-voltage switching conditions. Comparator U1 triggers the switch turn-off event, and comparator U2 triggers the switch turn-on event.

B. Experimental Results

Here we present laboratory test results of the prototype converter. In the test setup, the converter was driven from a $120\,\text{V}_{\text{rms}}$ ac power source (Agilent, 6812B) in to an (almost) fixed 35 V dc voltage (e.g., LED diode strings or Zener diode). Three external 5 V power supplies (Xantrex, XPH series) are used for hotel power of logic components[2]. The voltage,

[2]In separate experiments on an different generation of the design it was determined that the required "hotel power" could be derived from an input-referenced linear regulator and auxiliary windings on the buck inductors for an approximately 1% degradation in system efficiency. This demonstrated that logic power is not a major constraint in this design, but was not further investigated as it is not central to this work.
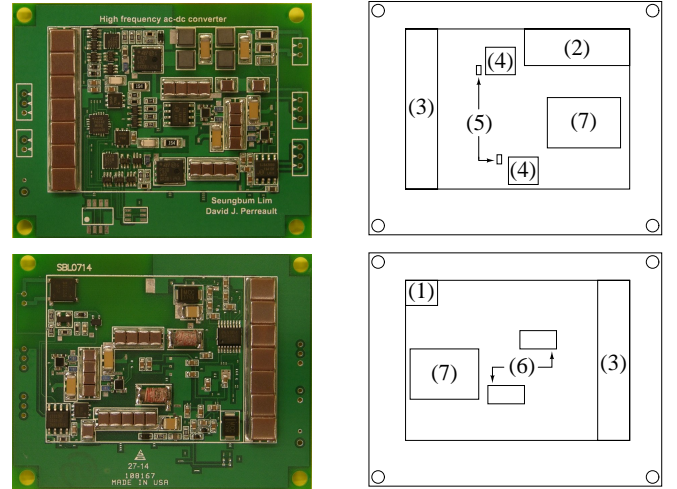

Fig. 7: The prototype converter, implemented on a $1.94\,\text{in(x)} \times 1.39\,\text{in(y)} \times 0.22\,\text{in(z)}$ printed circuit board. This figure shows the front and back side of the PCB illustrating several components: (1) Full-bridge rectifier, (2) EMI filter, (3) Energy buffer capacitor (C_2), (4) regulating converter diode, (5) regulating converter switch, (6) regulating converter inductor, and (7) SC power combining converter.

current, power, and power factor were measured with an ac power meter (Yokogawa, WT1800), and an oscilloscope (Tektronix, MSO4104) and probes (Tektronix, TPP0500 and P5205) were used for measuring the voltage signals of interest.

We first show the converter waveforms. Fig. 8 describes the voltage and current waveforms of the converter over the ac line cycle. Fig. 8 (a) illustrates the measured $120\,\text{V}_{\text{rms}}$ ac line input voltage, and Fig. 8 (b) shows the measured voltages
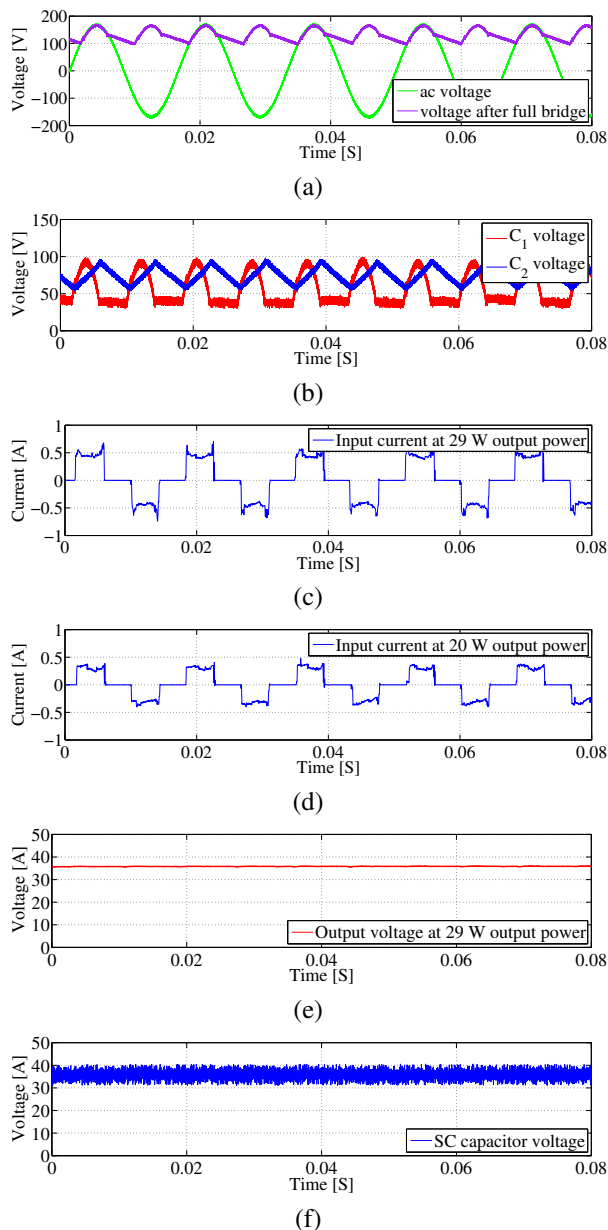
Fig. 8: Operation of the prototype converter from a $120\,\mathrm{V_{ac}}$ line voltage to a $35\,\mathrm{V_{dc}}$ output. Each figure illustrates voltage and/or current waveforms over the ac line cycle: (a) the measured $120\,\mathrm{V_{ac}}$ line input voltage and the measured voltages across the capacitor stack (output of the bridge rectifier) (b) the measured voltages across C_1 and across C_2 for a delivered output power of 29 W (c) the measured input current waveform at 29 W output power (d) the measured input current waveform at 20 W output power (e) the output voltage waveform at 29 W output power (f) the switched capacitor voltage waveform at 29 W output power.

across the capacitor stack, C_1, and C_2 (which buffers the twice-line-frequency energy) at an output power of 29 W. Fig. 8 (c) and (d) illustrate the measured input current waveform at 29 W output power and 20 W output power, respectively. Fig. 8 (e) shows the output voltage of the LED strings, and Fig. 8 (f) describes the voltage of the energy transfer
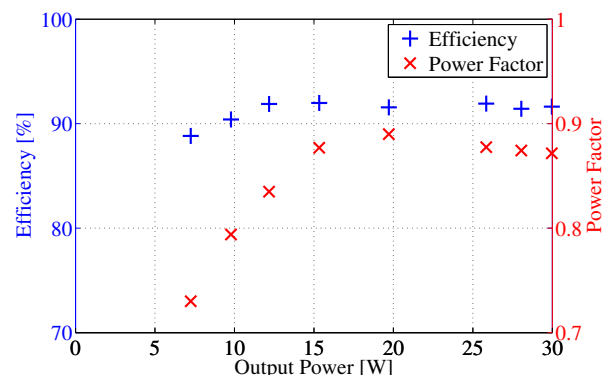

Fig. 9: The efficiency and power factor of the converter are measured across 5:1 load range. The prototype converter shows high efficiency and high power factor (up to 92% efficiency and 0.89 power factor).
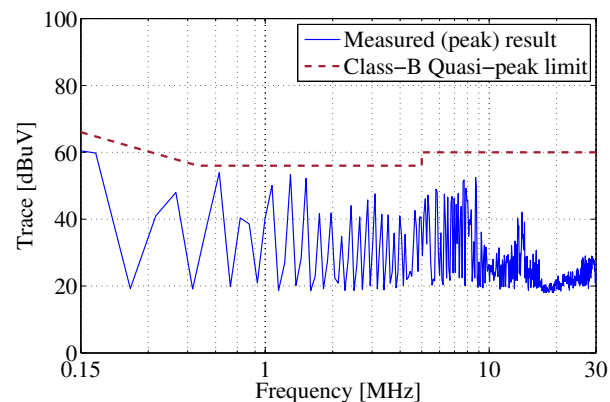

Fig. 10: The conducted electromagnetic interference was tested using standard conducted EMI test procedures with line impedance stabilization networks (LISNs) and a HP 8594E spectrum analyzer. The spectrum was measured for $150\,\mathrm{kHz} - 30\,\mathrm{MHz}$ and meets the CISPR Class B Conducted electromagnetic interference (EMI) Limit.

capacitors(V_{SC1}, V_{SC2}) of the switched capacitor circuit.

It should be noted that the voltage across the energy buffer capacitor C_2 swings with a large voltage ripple (a 50 V swing for approximately a 2:1 voltage variation) over the half-line cycle, and satisfies periodic-steady-state operation over the line cycle. With this large voltage swing, the proposed architecture dynamically buffers twice-line-frequency energy while utilizing approximately 75% of the peak storage capability of the energy buffer capacitor (at full power). In addition, as illustrated in Fig. 8 (c) and (d), the proposed architecture can change the modulating current of each regulating converter, so that it can supply different powers with almost similar conduction duration and power factor.

The voltage, current, power, and power factor were measured with an ac power meter (Yokogawa, WT1800), which nominally provides $\pm 0.3\%$ accuracy, and Fig. 9 shows the efficiency and power factor of the prototype converter over 5:1 load range. The converter achieves both high efficiency and high power factor over this load range (up to 92% efficiency

TABLE II: Performance Comparison

| Reference	[11]	[27]	[28]	[29]	**This work**
Topology	buck PFC + series-parallel(LLC)	flyback PFC + buck/boost	buck-boost	Bridgeless Boost-Asymmetrical Half-Bridge	stacked capacitor + inverted resonant buck + SC
Input voltage	$277-480\,\mathrm{V_{ac}}$	$90-264\,\mathrm{V_{ac}}$	$100-240\,\mathrm{V_{ac}}$	$220\,\mathrm{V_{ac}}$	$120\,\mathrm{V_{ac}}$
Output voltage	$140\,\mathrm{V_{dc}}$	$48\,\mathrm{V_{dc}}$	$48\,\mathrm{V_{dc}}$	$200\,\mathrm{V_{dc}}$	$35\,\mathrm{V_{dc}}$
Output power	$150\,\mathrm{W}$	$33.6\,\mathrm{W}$	$67.2\,\mathrm{W}$	$100\,\mathrm{W}$	$30\,\mathrm{W}$
Switching frequency	150 kHz (PFC), 95 kHz (dc-dc)	200 kHz (PFC), 100 kHz (dc-dc)	40 kHz	47 kHz	$3-10$ MHz (buck dc-dc) 30 kHz (SC)
Inductor	$600\,\mu\mathrm{H}$	$80\,\mu\mathrm{H}$, 1.1 mH	$111\,\mu\mathrm{H}$, 2 mH	$794\,\mu\mathrm{H}$, 1.1 mH, 2 mH	$800\,\mathrm{nH} \times 2$
capacitor	$980\,\mu\mathrm{F}$ electrolytic	$20\,\mu\mathrm{F}$, $0.47\,\mu\mathrm{F}$ film	$1410\,\mu\mathrm{F}$ electrolytic	$6.2\,\mu\mathrm{F}$, $100\,\mu\mathrm{F}$ film	$210\,\mu\mathrm{F}$ ceramic
Peak Efficiency	92 %	87 %	94.5 %	92.4 %	**92 %**
Power factor	$0.9-0.97$	0.99	$0.98-0.99$	0.97	**0.9**
Box Power density	$5.2\,\mathrm{W/in^3}$(estimated)	$2.5\,\mathrm{W/in^3}$(estimated)	$4.5\,\mathrm{W/in^3}$(estimated)	$3\,\mathrm{W/in^3}$(estimated)	$\mathbf{50\,W/in^3}$
Comment		bidirectional converter		Does not fully buffer ac energy; large output ripple	
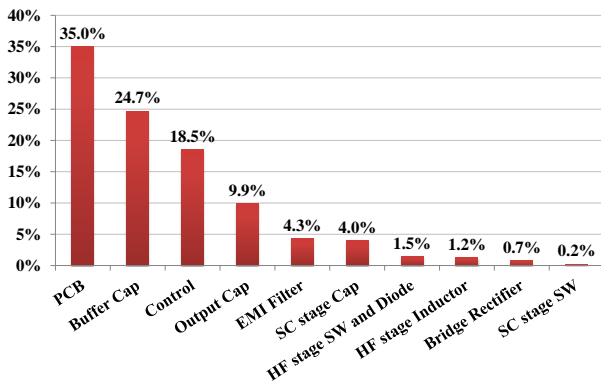
Fig. 11: The prototype converter achieves miniaturization through high frequency operation. This figure describes the volume distribution of the prototype converter. The printed circuit board and energy buffer capacitors contribute the largest portions of the converter volume. The volume of the inductors, and EMI filter are substantially reduced (as compared to typical designs) by high-frequency operation, and take up only a small portion of the converter volume.

and 0.89 power factor).

Converters for grid voltage interface need to meet electromagnetic interference (EMI) requirements. The converter was tested with line impedance stabilization networks (LISNs) and a HP 8594E spectrum analyzer. The spectrum was measured for $150\,\mathrm{kHz}-30\,\mathrm{MHz}$ frequency range and passed the CISPR Class B Conducted electromagnetic interference (EMI) Limit as shown in Fig. 10. This serves to illustrate that HF operation (operating frequencies in the $3-30$ MHz range) is not a barrier to meeting EMI specifications. Indeed, filter volume can be substantially significantly smaller than the designs operating at lower switching frequencies, and shielding can actually be easier, owing to the higher frequencies ripple and small skin depths involved.

The implemented prototype converter is shown in Fig. 7 with $1.94\,\mathrm{in(x)} \times 1.39\,\mathrm{in(y)} \times 0.22\,\mathrm{in(z)}$ box size. The prototype converter thus achieves 50 $\mathrm{W/in^3}$ "box" power density (i.e., Power density = Max Power / "box" volume of the converter). It is notable that this is much higher than the power density found for typical commercial LED drivers (typically below 5 $\mathrm{W/in^3}$ at this power rating). The displacement vol-

ume of the prototype is $0.23\,\mathrm{in^3}$ yielding a "displacement" power density of 130 $\mathrm{W/in^3}$. The volume breakdown of the converter is shown in Fig. 11. The largest contributers to the system volume of the converter are the printed circuit board (0.032 in thickness) itself and the energy buffer capacitor. Owing to the extremely high operating frequency ($\sim 10\mathrm{x}-100\mathrm{x}$ that of typical designs), the relative volume of the inductors, and EMI filter are significantly reduced, and take up only a small portion of the converter volume. As can be seen in Figs. 7 and 11, there is still substantial opportunity to reduce the size by integrating the control circuitry, using a high energy density electrolytic capacitor as C_2 (at the expense of converter lifetime), and designing with a thinner PCB board.

Table II illustrates the performance of the prototype converter relative to recent academic studies for ac-dc LED driver circuits. There are significant differences in power, voltage, functionality, etc. among these various designs, but they still serve as useful points of comparison. As compared to conventional designs, it can be seen that the proposed approach provides far higher operating frequencies ($10-100\mathrm{x}$), has far smaller numerical values and sizes of magnetic components, and achieves much higher power density ($\sim 10\mathrm{x}$). At the same time, it achieves high efficiency and good power factor without the use of electrolytic capacitors.

VI. CONCLUSION

A new single-phase grid interface ac-dc PFC architecture is introduced and experimentally demonstrated. In addition to enabling high efficiency and good power factor, this PFC architecture is particularly advantageous in that it enables extremely high operating frequencies (into the HF range) and reduction in energy buffer capacitor values, each of which contributes to converter miniaturization. The proposed stacked-combined architecture significantly decreases the voltage stress of the active and passive devices and reduces characteristic impedance levels, enabling substantial increases in switching frequency when utilized with appropriate converter topologies. Moreover, good power factor is achieved while dynamically buffering twice-line-frequency ac energy with relatively small capacitors operating with large voltage swing. The prototype converter achieves high efficiency and good power factor over a wide power range, and meets the CISPR Class-B Conducted electromagnetic interference (EMI) Limits. The
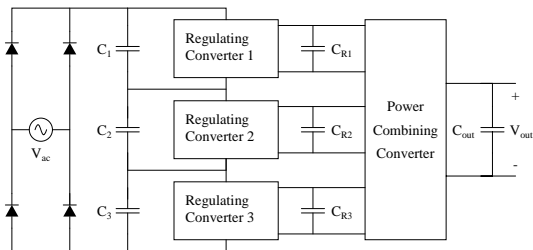
Fig. 12: The proposed architecture can be extended to more than two capacitors in the capacitor stack and other correspondingly other system blocks. This is particularly useful for handling universal ac line interface. Moreover, the number of capacitors and sub-regulating converter may be allowed to vary dynamically depending upon whether the circuit is connected to 120 or 240 V_{ac}.
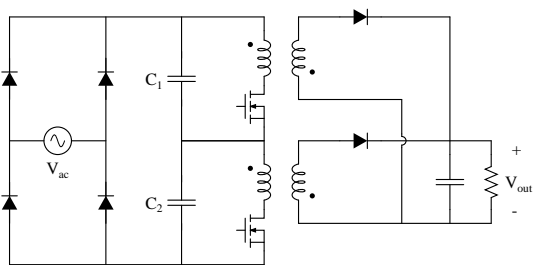

Fig. 13: The stack of flyback converters can regulate output load voltage and combine power to supply single load with connected secondary wires. Two flyback converters need to be modulated over the line cycle to achieve high power factor and buffer ac energy.

prototype converter based on the architecture and selected high-frequency circuit topology demonstrates an approximate factor of 10 reduction in volume compared to typical designs. The prototype has a very high 'box' power density of $50\,\mathrm{W/in^3}$ ('displacement' power density of $130\,\mathrm{W/in^3}$) with miniaturized inductors, a small volume of EMI filter, and ceramic energy buffer capacitors. Lastly, as described in the appendix, the proposed architecture can be realized in various ways (e.g., with alternative topologies) to realize features such as galvanic isolation and universal input range.

VII. APPENDIX

In this appendix, we explore some extensions, alternative realizations and alternative controls for the proposed PFC architecture to meet different application requirements.

A. Architecture Variation for different applications

The proposed architecture can be realized with different configurations and a variety of converter topologies. First, the proposed architecture may provide an interface to universal ac grid voltage while maintaining low device voltage stress through use of an increased number of capacitors and subsystem blocks as shown in Fig. 12. Moreover, the number of capacitors and regulating converters that are used at a given time may be allowed to vary dynamically depending upon whether the circuit is connected to, e.g., 120 or 240 V_{rms}.

This enables greater flexibility of operation, and narrower component operating ranges than could otherwise be achieved.

Secondly, the proposed architecture can be realized so as to provide galvanic isolation in a variety of manners, by utilizing different converter topologies. Either regulating converters or the power combining converter can be designed with an isolated converter topology, but utilizing an isolated power combining converter may be favorable because one can share a single transformer or use a multi-primary/single-secondary winding transformer, and naturally supplying combined powers to the system load. Another promising configuration is designing the system with a stack of isolated regulating converters having parallel-connected outputs, so that the regulating converters regulate the system load voltage and combine power simultaneously. For example, Fig. 13 illustrates the design with a stack of two flyback converters.

B. Control Method

In this paper, each regulating converter is dynamically modulated with look-up table to draw a pre-defined input current wave-shape for a given load power. In addition to the control method described for the prototype converter, there are various methods for controlling regulating converters and power combining converters depending on the selected circuit topology. For instance, regulating converters may supply power solely or simultaneously over some portion of the line cycle, or "slosh" power among the regulating converters for different power combining converter topologies.

One simple control scheme is that each regulating converter fully supplies the output power and regulates the load voltage over some portion of the line cycle. With this control scheme, the power combining converter may be selected as a non-regulating and fixed voltage transformation topology with high efficiency and high power density as illustrated in [30]–[32].

ACKNOWLEDGMENT

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Seungbum Lim (S'10) received the B.S. degree in electrical engineering from Seoul National University, Seoul, Korea, in 2010 and the S.M. degree in electrical engineering from the Massachusetts Institute of Technology, Cambridge, in 2012, where he is currently working toward the Ph.D. degree in the Laboratory of Electromagnetic and Electronic Systems.

His research interests include power electronics, resonant converters, soft-switching techniques, and RF power ampliers.

David M. Otten received the B.S. and S.M. degrees from the Massachusetts Institute of Technology, in 1973 and 1974 respectively.

In 1974 he joined the MIT Electric Power Systems Engineering Laboratory (EPSEL) as a staff engineer. Since 1984 he has been a Principal Research Engineer in the renamed Laboratory for Electromagnetic and Electronic System (LEES) at MIT. His research interests include instrumentation, power electronics, and the micromouse robot contest.
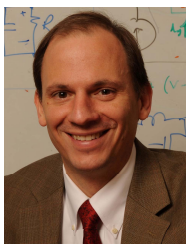
David J. Perreault (S'91-M'97-SM'06-F'13) received the B.S. degree from Boston University, Boston, MA, and the S.M. and Ph.D. degrees from the Massachusetts Institute of Technology, Cambridge, MA. In 1997 he joined the MIT Laboratory for Electromagnetic and Electronic Systems as a Postdoctoral Associate, and became a Research Scientist in the laboratory in 1999. In 2001, he joined the MIT Department of Electrical Engineering and Computer Science, where he is presently Professor and Associate Department Head. His research interests include design, manufacturing, and control techniques for power electronic systems and components, and in their use in a wide range of applications. He also consults widely in industry, and is co-founder of Eta Devices, a startup company focusing on high-efficiency RF power amplifiers. Dr. Perreault received the Richard M. Bass Outstanding Young Power Electronics Engineer Award from the IEEE Power Electronics Society, an ONR Young Investigator Award, and the SAE Ralph R. Teetor Educational Award, and is co-author of six IEEE prize papers.