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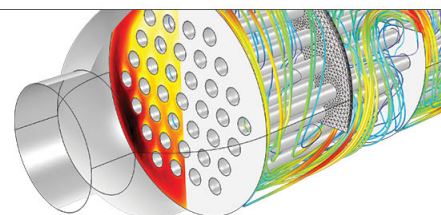
# Effective lifetimes exceeding 300 $\mu$s in gettered *p*-type epitaxial kerfless silicon for photovoltaics

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We evaluate defect concentrations and investigate the lifetime potential of *p*-type single-crystal kerfless silicon produced via epitaxy for photovoltaics. In gettered material, low interstitial iron concentrations (as low as $(3.2 \pm 2.2) \times 10^9 \, \mathrm{cm}^{-3}$) suggest that minority-carrier lifetime is not limited by dissolved iron. An increase in gettered lifetime from $<20$ to $>300 \, \mu$s is observed after increasing growth cleanliness. This improvement coincides with reductions in the concentration of Mo, V, Nb, and Cr impurities, but negligible change in the low area-fraction ($<5\%$) of dislocated regions. Device simulations indicate that the high bulk lifetime of this material could support solar cell efficiencies $>23\%$. © 2013 AIP Publishing LLC. [http://dx.doi.org/10.1063/1.4844915]

Kerfless crystalline silicon (c-Si) represents a promising approach to reduce the cost of solar-cell manufacturing by producing wafers directly from gaseous or molten silicon, avoiding ingot crystallization and wire-sawing.[1–6] Kerfless materials could reduce silicon consumption by $\sim 10 \times$ relative to ingot c-Si technology with high-efficiency thin devices.[6] Kerfless materials could also streamline the manufacturing process, obviate the use of some consumables, reduce factory cost, and allow for potentially non-planar modules with thin-wafer production.[4,6]

While a variety of approaches are available for kerfless wafer production,[1–4,6] we posit that attempts to commercialize kerfless wafers have historically been inhibited by low bulk minority-carrier lifetime ($\tau_{\mathrm{bulk}}$). Wafers from vertical ribbon growth processes[2] contain average dislocation densities of $10^4 - >10^6 \, \mathrm{cm}^{-2}$,[7–9] which in combination with metal impurities including iron,[7] limit minority-carrier lifetime and device performance (record efficiencies: 18.2% edge-defined film-fed growth, 17.8% string ribbon).[9,10] Given the strong dependence of manufacturing[6,11] and installation[12] costs on module efficiency, we stress the risk of bulk-defect-induced efficiency reductions to offset the cost savings of a kerfless process.

In this contribution, we evaluate the gettering response of kerfless epitaxial (epi) silicon and characterize defects in the material. Wafers grown from gas on porous silicon were introduced as the Canon ELTRAN process for integrated-circuit applications.[3,13] Epitaxial silicon is grown atop a porous release bilayer at an average rate of $>4 \, \mu$m/min,[3,14] with a low structural defect density of approximately $\leq 10^4 \, \mathrm{cm}^2$.[15–17] The epi silicon is exfoliated, leaving a single-crystal kerfless c-Si wafer and reusable substrate (over 50 cycles demonstrated).[3,14] Epi kerfless silicon may offer additional performance advantages, such as repeatable *n*- and *p*-type doping that is tunable through the wafer thickness.[17]

Solar cell efficiency results up to 20.6% have been reported with epi silicon;[18] however, the maximum reported effective lifetimes ($\tau_{\mathrm{eff}}$) of approximately 150 $\mu$s, on *n*-type

wafers,[19] may limit device efficiency. Even for thin wafers, $\tau_{\mathrm{bulk}}$ requirements increase for high-efficiency devices.[20,21] For a planar high-efficiency device architecture with a 50 $\mu$m thick substrate, our PC1D simulation[22] predicts $\tau_{\mathrm{bulk}} > 340 \, \mu$s (diffusion length $\sim 20 \times$ wafer thickness)[20] is required for maximum efficiency. Interdigitated back-contact architectures, as employed in commercial devices exceeding 24% efficiency, have more stringent requirements, $\tau_{\mathrm{bulk}} > 5 \, \mathrm{ms}$, for maximum efficiency.[23]

Herein, we demonstrate that kerfless epi silicon can achieve the $\tau_{\mathrm{bulk}}$ required to support planar cell architectures with efficiencies $>23\%$. Wafers are produced in two generations ("Gen I" and "Gen II" henceforth) with growth system contamination control increasing by generation. After gettering with both standard and extended processes at an injection level ($\Delta n$) of $10^{15} \, \mathrm{cm}^{-3}$, $\tau_{\mathrm{eff}}$ is $<20 \, \mu$s in Gen I material while $\tau_{\mathrm{eff}}$ is improved to $>300 \, \mu$s in Gen II. We perform injection-dependent lifetime measurements to determine the concentration and performance-impact of interstitial iron and conclude that this defect is not the principal performance-limit in either generation of gettered material. The wafer surface area fraction of high ($>10^5 \, \mathrm{cm}^{-2}$) dislocation density is comparable between generations (both cases $<5\%$), suggesting that structural defects are not responsible for the observed lifetime improvement. Via bulk mass spectrometry, we evaluate the concentrations of metal impurities and hypothesize that reduced concentrations of slowly-diffusing impurities incorporated during growth may enable the lifetime improvement observed in the second generation of material.

As samples for this study, boron-doped *p*-type kerfless wafers are epitaxially grown to a thickness of 55–110 $\mu$m. Gen II material is produced in an upgraded growth system that has been developed for industrial production with improved impurity management in system components and greater automation. As-grown wafers are exfoliated and laser-cut into approximately $4 \times 4 \, \mathrm{cm}^2$ samples. Bulk resistivity is measured with a four-point probe (Keithley 4200, Cascade Microtech probe), yielding 0.50 $\Omega$ cm (Gen I) and 1.79 $\Omega$ cm (Gen II), with doping concentrations[24] and carrier diffusivities subsequently calculated.

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First, we describe the processing and characterization performed on the material. Injection-dependent $\tau_{\text{eff}}$ is measured by quasi-steady-state photoconductance (QSSPC) and transient photoconductance decay (PCD) (Sinton WCT-120) with $Al_2O_3$ surface passivation.[25,26] After chemical polishing and RCA cleaning, 20 nm of $Al_2O_3$ is deposited on both sides with thermal atomic-layer-deposition at $200\,^\circ$C (Cambridge NanoTech Savannah 200).[27–29] Samples are then annealed in $N_2$ for 10 min at approximately $350\,^\circ$C.[28]

To account for the amount of illumination that is absorbed by each sample during lifetime measurements, a thickness-dependent "optical constant" is calculated (0.59–0.65) using a PC1D[22] model for the short-circuit current of a sample under illumination from a Sinton WCT-120 flash lamp.[26,30] The model assumes a 20 nm passivation layer with an index of refraction of 1.63.[31] To minimize noise in the data, 50 measurements are averaged for high lifetime ($>100\,\mu$s) samples. Error bounds for lifetime are $\pm 10\%$.[32] Lifetime values are reported at an injection condition of $\Delta n = 10^{15}\,\text{cm}^{-3}$ unless otherwise specified.

To estimate $\tau_{\text{bulk}}$, the surface recombination velocity (SRV) of our $Al_2O_3$ passivation is evaluated[28] by comparing a $\tau_{\text{eff}}$ of 1.43 ms measured with a double-side polished $253\,\mu$m 3 $\Omega$ cm float zone wafer after chemical polishing (to match the preparation of the kerfless samples), to the intrinsic $\tau_{\text{bulk}}$ per the model of Richter *et al.*[33] The resulting SRV of 8.1 cm/s is applied at all injection-levels for the kerfless samples, although doping and surface differences may modify the result.[29] We note, however, that interstitial iron concentration ($[Fe_i]$) measurements are insensitive to SRV if it is unaffected by illumination and sufficiently passivating.

Phosphorus-diffusion gettering in a $POCl_3$ tube furnace (Tystar Tytan 3800) is performed after as-grown passivation and RCA cleaning followed by a HF dip. Two-sided gettering is performed on free-standing wafers. Two processes are tested: A standard process with a 25 min $845\,^\circ$C plateau followed by pull-out and free cooling to room temperature, and low-temperature anneal (LTA)[34] process with the same plateau, but with cooling at $\sim 2.6\,^\circ$C/min to a 2 h $575\,^\circ$C anneal. The latter profile is inspired by the time-temperature-transformation diagram for dissolved iron in silicon[35] and tests for available gains from optimization of the standard process to reduce $[Fe_i]$. A sheet resistance of $75^{+11}_{-20}$ $\Omega$/sq is measured on the front and back of a single sample after the standard process and $77^{+10}_{-11}$ $\Omega$/sq after the LTA. The emitter is removed following gettering by chemical polishing (8 $\mu$m removed). Samples are re-passivated following the procedure above for post-gettering measurements.

To measure $[Fe_i]$, $\tau_{\text{eff}}$ is measured after illumination to dissociate iron-boron pairs ($Fe_i$-$B_s$) (20 flashes, Semilab WT-2000) and subsequent $Fe_i$-$B_s$ re-association (approximately 1 h Gen 1, 3.5 h Gen II).[26,36,37] Figure 1 shows the injection-level dependent lifetime of Gen II samples after dissociation and re-association, with the estimated bulk lifetime from our estimated SRV. For $[Fe_i]$ measurement, we compare lifetimes at $\Delta n = 10^{15}\,\text{cm}^{-3}$, above the "crossover point" discussed in Macdonald *et al.*[37,38] Capture cross sections for electrons and holes are taken as $\sigma_n = 5.0 \times 10^{-15}\,\text{cm}^2$ and $\sigma_p = 3.0 \times 10^{-15}$ $\text{cm}^2$ or for $Fe_i$-$B_s$ pairs and $\sigma_n = 1.3 \times 10^{-14}\,\text{cm}^2$ and $\sigma_p = 7.0 \times 10^{-17}\,\text{cm}^2$ for $Fe_i$.[37,39,40]

Lifetimes for the kerfless samples are quoted with $Fe_i$-$B_s$ pairs dissociated (illuminated). Five measurements are averaged to avoid re-dissociation of $Fe_i$-$B_s$ pairs during "dark" Gen II lifetime measurements for $[Fe_i]$, although 50 measurements are averaged in Figure 1. Error bounds for $[Fe_i]$ are calculated assuming $\pm 1.5\%$ uncertainty for repeated lifetime measurements[32] and random propagation through the $[Fe_i]$ calculation.[41]

Next, we examine the impact of three potential lifetime-limiting defects in each generation of kerfless epi material. First, we evaluate the role of dissolved iron, a common performance-limiting defect in kerfless ribbon materials.[7,42] In Gen I material after standard gettering, we measure a $\tau_{\text{eff}}$ of $12 \pm 1.2\,\mu$s, an implied open circuit voltage ($V_{OC}$) at 1 sun of 647 mV, and an $[Fe_i]$ of $(5.0 \pm 7.4) \times 10^{10}\,\text{cm}^{-3}$ in a 52 $\mu$m thick sample. The LTA process results in an $[Fe_i]$ of $(3.0 \pm 9.8) \times 10^{10}\,\text{cm}^{-3}$, but yields a reduced $\tau_{\text{eff}}$ of $9 \pm 0.9\,\mu$s and implied-$V_{OC}$ of 628 mV in a 57 $\mu$m sample. The change in $[Fe_i]$ between processes is inconclusive, as the observed change is within the calculated error. After standard gettering of Gen II material, $\tau_{\text{eff}}$ is $342 \pm 34\,\mu$s, implied-$V_{OC}$ is 710 mV, and $[Fe_i]$ is $(2.5 \pm 0.23) \times 10^{10}\,\text{cm}^{-3}$ with a 95 $\mu$m sample (Figure 1). With the LTA process, $\tau_{\text{eff}}$ is $313 \pm 31\,\mu$s, implied-$V_{OC}$ is 713 mV, and $[Fe_i]$ is $(3.2 \pm 2.2) \times 10^9\,\text{cm}^{-3}$ with an 80 $\mu$m sample. Although the standard process provides a higher $\tau_{\text{eff}}$ than the LTA, $\tau_{\text{bulk}}$ is nearly equivalent, arising from different surface lifetimes due to different sample thicknesses. We note that the Gen II LTA sample is not centered during QSSPC measurements to maximize $\tau_{\text{eff}}$. When centered, the Gen II LTA $\tau_{\text{eff}}$ is $294 \pm 29\,\mu$s.

To identify the performance impact of $Fe_i$, we compare $\tau_{\text{bulk}}$ against the maximum lifetime obtainable with a given $[Fe_i]$.[40,43] Estimated $\tau_{\text{bulk}}$, calculated with our estimate of SRV, for champion samples after gettering and illumination are shown in Figure 2. Dashed lines show the estimated lifetime limits from Auger and radiative recombination[32] and a simplified[44] Shockley-Read-Hall recombination model at $Fe_i$ per the *QSS-Model* from Cuevas.[45] The data suggests that
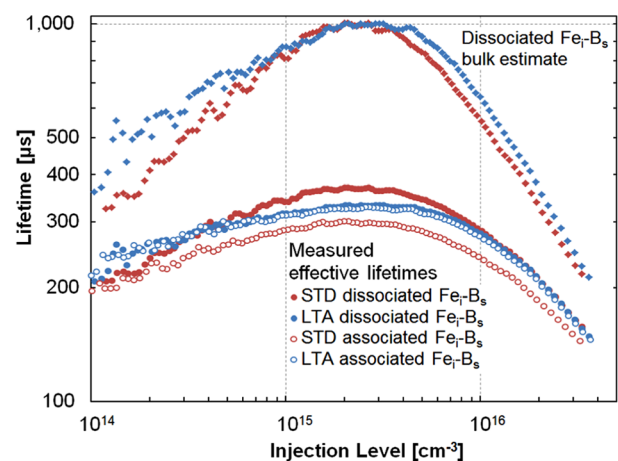


FIG. 1. Effective minority-carrier lifetimes of champion Gen II samples after P-diffusion gettering (standard process red; LTA blue) as a function of injection-level with dissociated (full symbols) and associated (open symbols) $Fe_i$-$B_s$ pairs. Lifetime decay and the "crossover point" can be observed with the standard process after $Fe_i$-$B_s$ re-association, while the LTA process does not indicate significant $[Fe_i]$. The estimated bulk lifetime is shown with SRV = 8.1 cm/s.

defects other than $Fe_i$ limit bulk minority-carrier lifetimes in both Gen I and Gen II materials after gettering because $\tau_{bulk}$ values are well below the $Fe_i$-limited lifetime[40,43] and $\tau_{bulk}$ is not improved with the LTA process.

The estimated $\tau_{bulk}$ is improved by approximately two orders of magnitude in Gen II relative to Gen I material. With similar $[Fe_i]$, a reduction of another lifetime-limiting defect is suggested (Figure 2). Structural defects are one possibility and are believed to originate in single-crystal epi wafers from incomplete pore closure during porous silicon annealing.[15,46] Stacking faults and dislocations are revealed in portions of Gen I (1 cm$^2$) and Gen II (4 cm$^2$) samples after gettering[47] and analyzed with an optical microscope and counting software.[48] The wafer surface area covered by regions of high ($>10^5$ cm$^{-2}$) dislocation density, a predictor of performance loss,[8,49] of both Gen I and Gen II materials are comparable ($<5\%$), and thus deemed not to be the defect responsible for the dramatic increase in lifetime between generations.

Next, we consider the role of impurity species besides iron. Inductively coupled plasma mass spectrometry (ICP-MS, Fraunhofer Center for Silicon Photovoltaics) is performed to measure the concentrations of 20 impurity elements before gettering in approximately 1 g of Gen I and $>2$ g of Gen II material (1 and 2 ICP-MS samples respectively). Gen II material exhibits reduced concentrations of deleterious impurities[50] that are slowly-diffusing and may prove difficult to getter:[51] Molybdenum (82% reduction to detection limit), Vanadium (59% reduction), and Niobium (40% reduction).[52] Chromium also decreased in Gen II material (91% reduction); however, the difference in post-gettering performance between generations leads us to suspect the aforementioned species. No change above the error of the measurement was detected for the other impurities tested (Mg, Al, P, Ti, Mn, Fe, Ni, Co, Cu, Zn, Zr, Ag, Sn, W, and Au). The evidence suggests that a reduction of slowly-diffusing impurities in the as-grown material may be critical for the observed lifetime improvement in Gen II material.

In light of this analysis, we comment on the ultimate lifetime potential of epi material in comparison to industry-standard ingot multicrystalline silicon (mc-Si). The area fraction of high ($>10^5$ cm$^{-2}$) dislocation density is low ($<5\%$), suggesting that dislocations may be less of a lifetime limitation for epi than even small-grained mc-Si.[53] We note that mc-Si wafers obtain similarly low $[Fe_i] \leq 10^{10}$ cm$^{-3}$ directly after low-temperature annealing,[53,54] yet average effective lifetimes are shown to be limited to 200 $\mu$s.[54] In addition, the absence of grain boundaries in epi material eliminates a potential source of open-circuit voltage loss.[55] Future work will elucidate the performance impact of structural defects in kerfless epi. However, we hypothesize that the control of impurities, especially through substrate re-uses, may be the crucial determinant of lifetime for this material.

Finally, we estimate the performance potential of epi-based solar cells using a PC1D[22] simulation for a high-efficiency device architecture (Table I), and explore the optimal epi wafer thickness. The device includes a lightly-doped 120 $\Omega$/sq emitter with low series and contact resistance, and a locally contacted and passivated rear.[56] PC1D was used to simulate this 2-D architecture with cell-area-normalized values for rear contact resistance and reflectance, as is done by default in PC1D for external reflectivity.

With a 50 $\mu$m wafer, the simulation indicates that the excess electron density at the maximum-power point is approximately $1.4 \times 10^{15}$ cm$^{-3}$ in the bulk of the device with high lifetime material.[20,21,57] The $\tau_{eff}$ of the champion standard gettering Gen II sample is $357 \pm 36$ $\mu$s after illumination at $\Delta n = 1.4 \times 10^{15}$ cm$^{-3}$, resulting in an estimated $\tau_{bulk}$ of 924 $\mu$s assuming a SRV of 8.1 cm/s (Figure 1). This lifetime in the bulk of the device achieves an estimated efficiency of 22.4% with a 50 $\mu$m wafer and $>23\%$ with increased wafer thicknesses (Figure 3(a)). Lower-performance material, $\tau_{bulk} = 50$ $\mu$s, provides reduced cell performance and optimum thickness relative to the Gen II material due to diffusion length limitations.[21]

A cost-performance[11,68] model explores trade-offs between efficiency, wafer thickness, and manufacturing yield for kerfless silicon (Figure 3(b)). Without input from our industrial collaborators, we have estimated an optimum wafer thickness for cost of 50–60 $\mu$m for Gen II material. Yields for the separate wafer, cell, and module manufacturing steps are $\varphi = 54.47 \times t^{0.111}$ based on free standing wafers during cell processing,[11,69] and a wafer production throughput multiplier is $\lambda = 36.38 \times t^{-0.917}$,[15] with $t$ as the
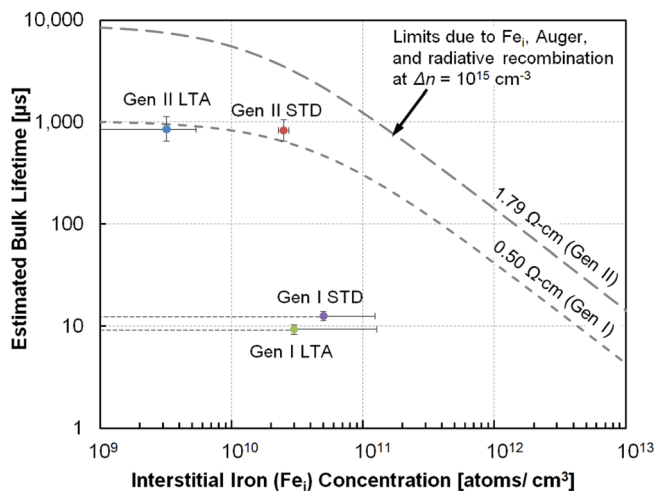


FIG. 2. Estimated bulk minority-carrier lifetimes of two generations of kerfless wafers after P-diffusion gettering compared to theoretical lifetime limits at $\Delta n = 10^{15}$ cm$^{-3}$. An approximate two orders of magnitude improvement in $\tau_{bulk}$ after gettering is observed for Gen II relative to Gen I material. The minimal impact of the LTA processes and difference between the realized and theoretical lifetime limits suggest that defects other than $Fe_i$ limit post-gettering lifetimes.

TABLE I. Solar cell simulation input parameters

| Parameter | Value | Reference |
|---|---|---|
| Front external reflectivity [%] | 5.0 | 58 |
| Front/rear internal reflectance [%] | 92.5/95.0 | 59 and 60 |
| Series/shunt resistance [$\Omega$ cm$^2$] | 0.3/10 000 | 61–63 |
| Front/rear contact resistance [$\Omega$ cm$^2$] | 0.027/0.027 | 64 and 65 |
| Effective front/rear SRV [cm/s] | 2000/30 | 20, 28, 29, and 60 |
| Wafer doping [cm$^{-3}$] | $p$, $3 \times 10^{16}$ | |
| Peak emitter doping [cm$^{-3}$] | $n$, $5 \times 10^{19}$ | 65–67 |
| Emitter sheet resistance [$\Omega$/sq] | 120.2 | 63, 65, and 66 |

**(a)**



**(b)**
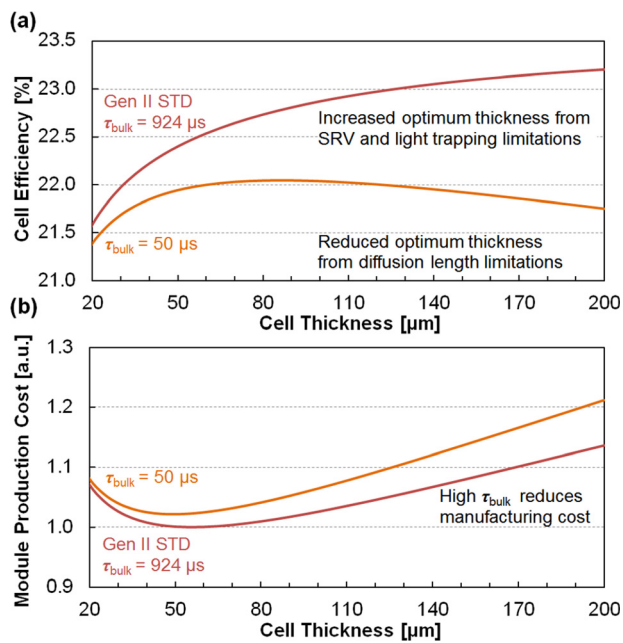
FIG. 3. (a) The lifetime of the Gen II material (red line) after a standard gettering process is sufficient to achieve simulated cell efficiencies of >23% (22.4% with a 50 $\mu$m wafer) with a high-efficiency device architecture. (b) Estimated manufacturing cost (in \$/W) normalized to the minimum obtained. The predicted optimum thickness for cost is 50–60 $\mu$m. Lower performance material with $\tau_{bulk} = 50\,\mu$s (orange line) provides a lower efficiency and optimum thickness while increasing manufacturing cost.

wafer thickness in microns. We observe a cost minimum from the trade-off of efficiency and yield, which both favor thicker wafers, and silicon usage and throughput, which both favor thinner wafers. While precise values will vary depending on process details, this calculation highlights the need for high-yield manufacturing processes, good light trapping, and good surface passivation to minimize thickness and sufficient $\tau_{bulk}$ to maximize efficiency.

In conclusion, effective minority-carrier lifetimes >300 $\mu$s at $\Delta n = 10^{15}\,\mathrm{cm}^{-3}$ are demonstrated in epitaxially grown kerfless silicon after gettering. $Fe_i$ concentrations of $(2.5 \pm 0.23) \times 10^{10}\,\mathrm{cm}^{-3}$ are measured with a standard gettering process and $(3.2 \pm 2.2) \times 10^{9}\,\mathrm{cm}^{-3}$ after a low-temperature anneal in the second generation of material. Our analysis suggests that lifetime in both generations of material is not limited by interstitial iron after gettering. We observed a low area fraction (<5%) of high (>$10^{5}\,\mathrm{cm}^{-2}$) structural-defect density in both generations of material. We hypothesize that reductions in the concentration of slowly-diffusing metal impurities may enable the approximately two orders of magnitude lifetime improvement observed in Gen II material. Our cost-performance model estimates that the achieved lifetimes could support cell efficiencies >23% and suggests an optimum thickness regime of 50–60 $\mu$m for cost. We note that as successive generations of PV silicon materials become "cleaner," there is a need to develop and employ defect characterization tools that can determine the identities and impacts of low concentrations of performance-limiting impurities.[70]

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