

10.7 A +10dBm 2.4GHz Transmitter with sub-400pW Leakage and 43.7% System Efficiency

Arun Paidimarri, Nathan Ickes, Anantha Chandrakasan

Massachusetts Institute of Technology, Cambridge, MA

Extreme energy constraints inherent in many exciting new wireless sensing applications (such as [1-3]) virtually dictate that such systems operate with extremely low duty cycles, harvesting and storing energy over long periods of time before waking up to perform brief measurement and communication tasks. However, such duty cycling only works if the sleep power of the system is less than the average power available from the power source, which may only be as much as a few nA. In this work, we present an RF transmitter designed to operate in an extremely low duty-cycle industrial monitoring system. The primary challenges are achieving high efficiency in the active mode while transmitting as high as +10dBm and simultaneously minimizing the leakage during the sleep mode. We address these in a +10dBm Bluetooth Low Energy (BLE) transmitter test-chip through 1) low voltage design (0.68V) for switching power and short-circuit power reduction, 2) extensive power gating of unused blocks and 3) a negative- V_{GS} biasing technique for PA leakage reduction without affecting its on-performance.

Typically, high- V_T power switches are used to power gate low- V_T active circuits [1]. But, the switch resistance, which is in the direct path of active current, degrades on-performance. Increasing switch size will in turn increase leakage. Negative gate-biasing of the gating switch has been shown to give significant leakage reduction [3]. However, in this work, we study the effect of negative-gate biasing of the low- V_T active device itself, thereby eliminating a switch in the direct path of active current and simultaneously reducing leakage. This is especially useful for the PA in our work, which operates at +10dBm and is the largest active power consumer.

Fig. 13.7.1 shows the measured drain current ($I_{D,PA}$) and gate current ($I_{G,PA}$) of the NMOS PA transistor as a function of the negative gate bias applied. The 65nm CMOS transistor, because of its thin gate oxide, has significant gate leakage. It is exponential with the gate bias. The drain current, which is the sum of sub-threshold current and gate leakage, decreases exponentially with increasing gate bias while the sub-threshold current is dominant, but increases as gate leakage becomes larger. The red curve (in solid) shows the achievable total PA leakage assuming the negative bias is supplied by an ideal $-1/2$ charge pump ($I_{LEAK} = I_{D,PA} - 1/2 I_{G,PA}$). The minimum, 430pA, occurs at $-200mV$ and represents a $30\times$ reduction in leakage. Fig. 13.7.1 also shows a histogram of the minimum ($I_{D,PA} - 1/2 I_{G,PA}$) current for 25 measured chips. Simulations indicate that the minimum leakage points range from $-150mV$ to $-300mV$, which implies that a $-1/2$ charge pump generating $V_{NEG} = -1/2 V_{IN}$ is sufficient. Low V_{DD} ensures device reliability even with V_{NEG} biasing ($V_{DD} - V_{NEG} < 1.2V$).

Fig. 13.7.2 shows the complete TX system block diagram. The RF signal path has a 12MHz crystal oscillator feeding a divided 1MHz clock to an integer-N PLL. The PLL provides 2MHz-spaced BLE channels at 2.4GHz. The PLL output is then buffered onto a +10dBm power amplifier. The TX applies direct modulation to the VCO control voltage for 1Mbps GFSK. A digital baseband, running at 6MHz, implements an SPI interface and BLE packet generation logic including CRC, data whitening and Gaussian pulse shaping. A voltage doubler charge pump running at 3MHz provides V_{DOUB} ($\approx 1.2V$) to enable high-Q RF capacitor banks for use in VCO frequency tuning and matching network tuning.

The TX also implements extensive power gating. The RF transistor in the PA uses negative gate biasing for leakage reduction without RF performance degradation. A 32Hz gate-leakage-based oscillator drives the $-1/2$ charge pump to generate V_{NEG} . All other blocks have either a PMOS or NMOS thick-oxide high- V_T power switch. Simulations show that driving an NMOS power switch with V_{DOUB} and V_{NEG} instead of V_{DD} and GND results in $10\times$ smaller voltage drop in active mode and $10\times$ lower sleep leakage. Similarly, PMOS power switches are turned on strongly using V_{NEG} in the active mode. In sleep-mode, the voltage doubler is off and V_{DOUB} settles to V_{DD} .

Fig. 13.7.3 shows a detailed circuit diagram for the fully integrated PA signal chain. In order to provide +10dBm output power, the PA employs a pi-match network to bring the 50Ω antenna impedance down to 20Ω . It also employs a NMOS-only inductively degenerated architecture to allow the drain node to swing above and below V_{DD} . The PA is DC-biased through R_0 . Sleep-mode is enabled by a single near minimum-sized switch M_1 , which presents negligible loading. In order to maximize efficiency, a resonant buffer stage drives the PA. Resonant (as opposed to

inverter) drive allows the main PA transistor M_0 to be upsized with minimal power penalty. The resonant buffer transistor M_2 itself is driven by an inverter buffer chain with a 0 to V_{DOUB} swing. The strong drive allows M_2 to be $25\times$ smaller than M_0 , thereby reducing power in the inverters. This VCO buffer presents minimal capacitive loading to the VCO (min-sized inverter M_4 - M_5).

Fig. 13.7.3 also shows an example of a block that requires a PMOS power switch. It shows the design of capacitor banks. INV_3 drives M_7 to connect / disconnect capacitor C_7 . If INV_3 were NMOS power-gated, the gate leakage of M_7 would go through, leading to a leakage as high as 2.5nA (FF corner simulation). On the other hand, adding a power switch in series with M_7 would lower the Q of the capacitor bank. Instead, the PMOS power switch shown keeps leakage below 5pA.

An efficient negative voltage charge pump is key to achieving good leakage reduction in the PA. It must supply around 260pA of current at around $-200mV$. The charge pump, shown in Fig. 13.7.4 achieves this with $>90\%$ charge transfer efficiency. Its quiescent current is reduced by operating at a very low frequency (less than 100Hz). Such a low frequency is efficiently generated with the gate-leakage based timer [4] shown in Fig. 13.7.4. It oscillates at 32Hz and consumes 14pA. Gate leakage of core transistors are the current sources in the circuit. Nodes V_1 and V_2 alternately charge up to the switching threshold of an inverter. At low swing, the current source stays constant and the frequency of the oscillator is $f = I_{GATE} / (2C * V_{TH,INV})$. At low supply voltages, the shoot-through current is negligible, enabling the low power consumption in spite of the slow rise times of V_1 and V_2 .

Fig. 13.7.7 shows the die photo of the TX fabricated in a 65nm LP CMOS process. The die area is $2.5 \times 2.5mm^2$ while the core area is $1.6mm^2$. The crystal oscillator, PLL and VCO consume $32\mu W$, $132\mu W$ and $510\mu W$ respectively. The VCO buffer consumes $102\mu W$ while the resonant buffer draws 1mW. The PA delivers a wide range of output powers ranging from +10.9dBm down to -5dBm depending on the supply voltage and bias voltage applied to it. Fig. 13.7.5 plots the overall TX efficiency for various V_{DD} values. At 0.68V, it generates an output power of +10.9dBm with a PA efficiency of 46.4% and overall TX efficiency of 43.7%. At a lower voltage of 0.25V, the PA has a peak efficiency of 47.2% while delivering 2.6dBm with the TX efficiency at 31.6%. Fig. 13.7.5 also plots the spectrum of 1Mbps GFSK modulation. The adjacent channel power is well below the BLE spec. The TX was able to successfully communicate with a commercial off-the-shelf BLE receiver from Texas Instruments.

Fig. 13.7.6 shows leakage measurements of the full TX. The pie chart breaks down the contribution of the various components with the PA being the dominant one. The total leakage power is around 370pW. Fig. 13.7.6 also shows the measurement of total TX leakage at various temperatures. This experiment was performed bypassing the gate leakage oscillator in order to characterize the true minimum power points. At high temperatures, the effectiveness of the leakage management techniques is better because the sub-threshold current at $V_{NEG} = 0$ is higher while the gate leakage is relatively constant with temperature. For example, at $+80^\circ C$, there is a $100\times$ reduction in leakage current at an optimal V_{NEG} of $-300mV$.

In conclusion, a 2.4GHz BLE-compatible transmitter architecture for use in ultra-low duty cycle applications has been presented. Low voltage operation, extensive power gating and a negative gate biasing technique help in achieving a peak TX efficiency of 43.7% at an output power of +10.9dBm while also reaching a leakage power of 370pW, for an on/off ratio of 7.6×10^7 .

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References:

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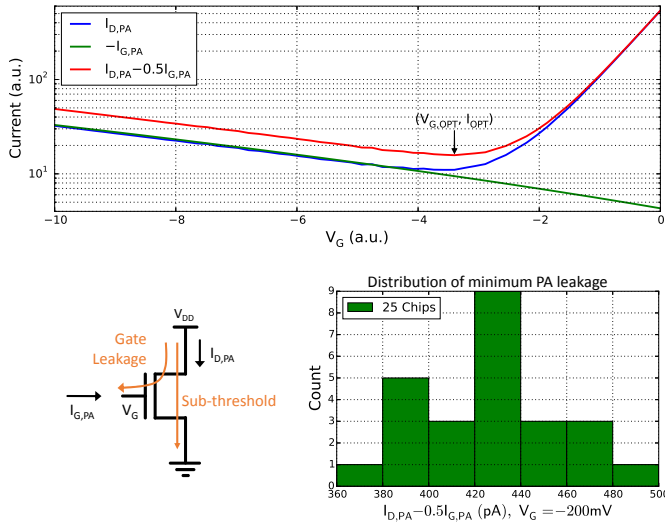


Figure 13.7.1: Measured drain and gate currents for the PA showing minimum leakage point and its distribution across 25 measured chips.

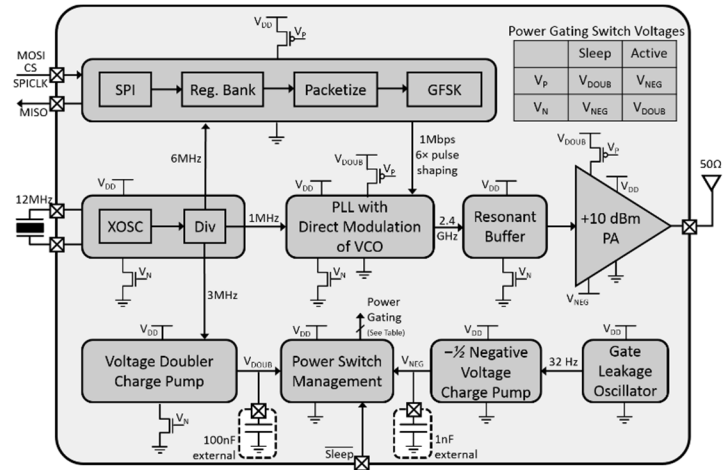


Figure 13.7.2: Block diagram of the transmitter showing RF signal chain, power gating switches and leakage management blocks.

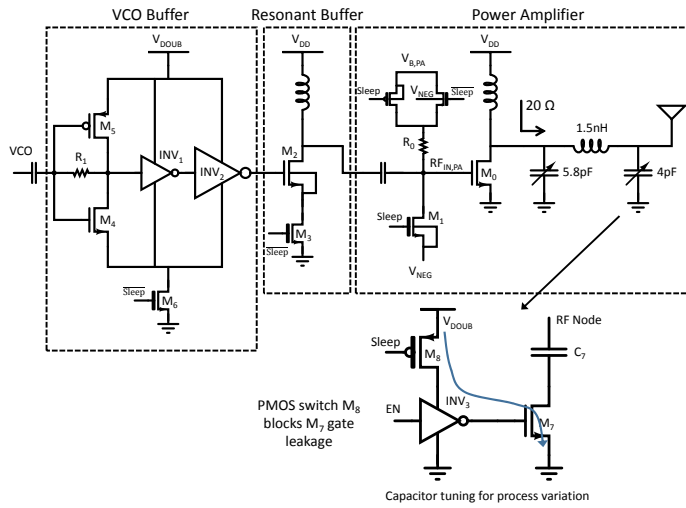


Figure 13.7.3: RF signal chain from VCO to the antenna showing the VCO buffer running from V_{DOUB} , the resonant buffer, the power amplifier and capacitor bank tuning.

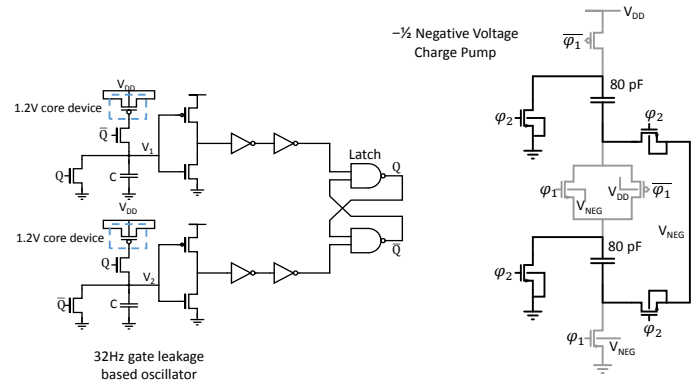


Figure 13.7.4: Gate-leakage oscillator that provides the clock for the negative voltage charge pump that generates V_{NEG} . All devices are thick-oxide devices except for the gate-leakage current sources.

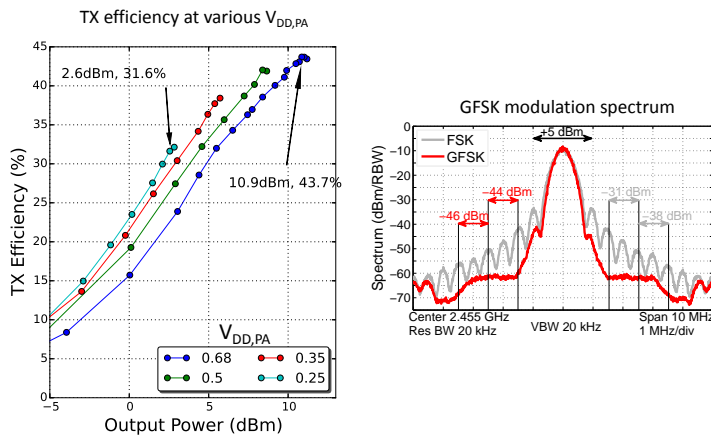


Figure 13.7.5: RF performance of the transmitter showing overall transmit efficiency at various $V_{DD,PA}$ values. Also shown is the 1Mbps GFSK spectrum from the transmitter.

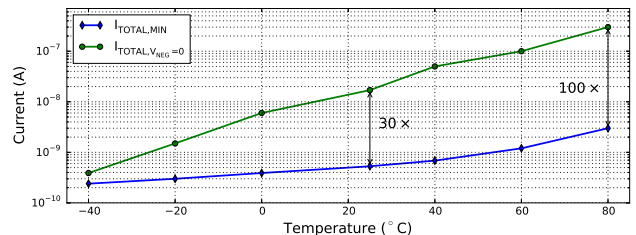
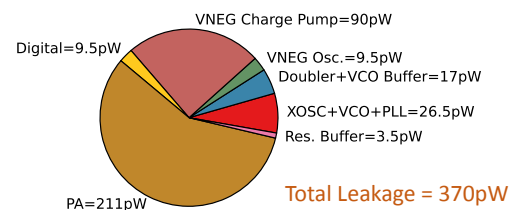


Figure 13.7.6: Pie chart with the contribution of various blocks to system leakage and variation of the minimum leakage with temperature.

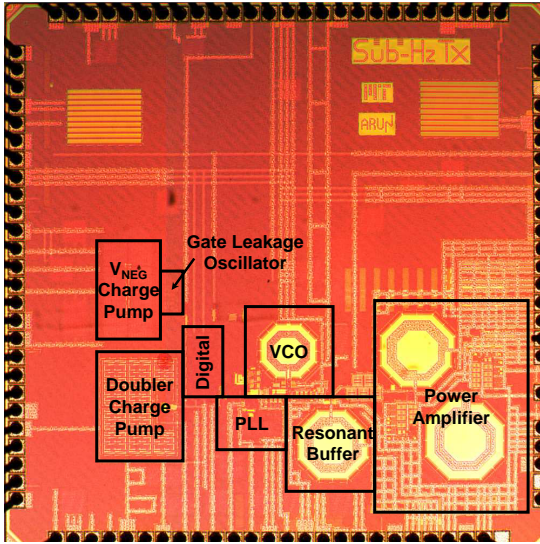


Figure 13.7.7: Die photo of the transmitter fabricated in 65nm LP CMOS. Die size is 2.5×2.5mm² and core area is 1.6mm².