Resonant Body Transistors in Standard CMOS Technology

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Abstract- This work presents Si-based electromechanical resonators fabricated at the transistor level of a standard SOI CMOS technology and realized without the need for any post-processing or packaging. These so-called Resonant Body Transistors (RBTs) are driven capacitively and sensed by piezoresistively modulating the drain current of a Field Effect Transistor (FET). First generation devices operating at 11.1-11.5 GHz with footprints of 3μm×5μm are demonstrated. These unreleased bulk acoustic resonators are completely buried within the CMOS stack and acoustic energy at resonance is confined using Acoustic Bragg Reflectors (ABRs). The complimentary TCE of Si/SiO₂ in the resonator and the surrounding ABRs results in a temperature stability TCF of <3 ppm/K. Comparative behavior of devices is also discussed to analyze the effect of fabrication variations and active sensing.

I. INTRODUCTION

A. Multi-GHz Si-based resonators

RF MEMS resonators offer an attractive alternative to more traditional LC tanks, off-chip Quartz crystals, and SAW devices due to their high Q, small footprint, and capacity for intimate integration with CMOS. This leads to reduced parasitics from on and off-chip routing for high frequency operation, smaller size and weight, and decreased power consumption by alleviating constraints for impedance matching networks [1,2].

A second criterion of interest in RF MEMS resonators is that of scaling to high frequencies. The past decade has seen a continuous push towards multi-GHz frequencies for applications including personal navigation (94 GHz) and short distance LAN (60 GHz), imaging, and high-definition video links. A majority of MEMS resonators rely on passive transduction mechanisms such as electrostatic and piezoelectric transduction to sense acoustic resonance. However, in these passive systems, parasitic feed-through increasingly becomes dominant over the resonance signal at higher frequencies, necessitating the exploration of a different sensing mechanism.

The concept of active FET-sensing in MEMS devices has been around since Nathanson's Resonant Gate Transistor in 1967 [3]. In Si-based resonators, FET sensing has been demonstrated up to 113 MHz [4] and in piezoelectric GaN-based resonators, up to 2 MHz [5]. The authors have previously demonstrated Resonant Body Transistors (RBTs) [6,7,8] with internal dielectric drive and Field Effect Transistor (FET) sensing up to 37 GHz (Fig. 1). FET-sensing has thus been shown to reach order of magnitude higher frequencies than possible with passive resonators due to the active amplification of the resonance signal before the
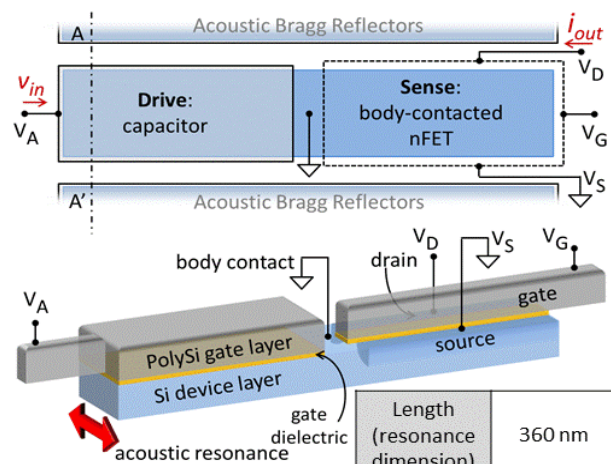

Fig.1: Top and 3D views of Si-based MEMS-CMOS resonator excluding Acoustic Bragg Reflectors (ABR). Bulk acoustic waves are driven capacitively on the left, and sensed as a piezoresistive modulation of the FET drain current on the right. Details of FET layout and doping layers not shown.

Length (resonance dimension)	360 nm
Width	2.5 µm
# ABR pairs	7
Device footprint	5 µm × 3 µm
Capacitor doping	p or n-type
FET type	Body contacted nFET
FET W/L	10.3

presence of parasitics. In the case of Si-based devices, performance of FET-sensed resonators can be further enhanced by integration into CMOS technology to harness its high f_T, high yield transistors and to substantially reduce parasitics from routing and bond-pads to the device.

B. CMOS Integration of MEMS resonators

Integration of MEMS resonators with the CMOS stack presents a number of challenges to the performance of the MEMS devices. CMOS-based MEMS devices are broadly classified into two categories, MEMS-first devices and MEMS-last devices. MEMS-first devices are typically designed in the front-end-of-line (FEOL) stack with access to high performance materials such as Silicon and high-k dielectrics with a high thermal budget. However, these MEMS devices require a release etch at the end of the CMOS process which can affect the performance and yield of the surrounding circuitry while increasing overall process complexity [9,10].

On the other hand, MEMS-last devices are usually fabricated in the back-end-of-line (BEOL) of the process, making the release step easier and decreasing the overall chip

footprint due to vertical stacking [11]. However BEOL materials such as metals and low-quality dielectrics as well as the constrained thermal budget limit device performance and maximum resonance frequency. Another type of MEMS-last devices includes those that are fabricated on top of a complete CMOS die in a separate custom MEMS process [12,13]. This approach can reduce system footprint and introduce non-CMOS materials, but are subject to increased process complexity and cost from additional masks.

One approach to address the above demerits of integration is the design of MEMS resonators in FEOL CMOS which can be realized without any post-processing or packaging (Fig. 2). In this work, IBM's 32SOI process was chosen for its high f_T transistors, the manufacturability of small feature sizes down to <60 nm and the presence of the buried oxide (BOX) layer for acoustic localization of vibrations in the Si device layer.

C. Unreleased Resonators for CMOS Integration

The MEMS resonators developed here are unreleased to avoid extra complexity and cost while maintaining high yields. Furthermore, anchor losses remain the dominant loss mechanism in high-frequency released resonators as they operate beyond the Akhiezer regime of phonon-phonon scattering, in the Landau-Rumer regime where such scattering results in negligible energy loss [14,15]. Development of unreleased resonators to avoid such anchor losses thus becomes an attractive option not only for CMOS-integrated resonators but also for scaling of MEMS resonators to higher frequencies.

Two constituent building blocks are thus required for the development of CMOS-integrated resonators:

1. A Si-based transducer operating efficiently in the GHz frequency regime.

2. A solid-state mechanism to confine acoustic vibrations within the resonant cavity in a completely unreleased environment, using CMOS compatible materials.

These challenges are addressed in the following sections using dielectric transduction and Acoustic Bragg Reflectors.

II. RBTs in IBM's 32SOI technology

Due to material restrictions in CMOS, electrostatic transduction is considered to take advantage of the gate stack. Using the high quality of the gate dielectric, the RBTs designed and fabricated in this process are driven electrostatically and sensed using a body-contacted analog FET (Fig. 1). Structurally, the drive capacitor consists of PolySi gate material and a p-doped or n-doped SCS device layer acting as capacitor plates with the SiON gate dielectric between them [16]. On the sense side, a foundry-provided nFET is modified to incorporate it within the resonant cavity along with the drive capacitor on the same device layer.

In operation, the FET is biased into saturation while grounding the body separately from the source to reduce feed-through. A small AC voltage is superimposed on top of a DC bias to generate a squeezing force on the capacitor dielectric which translates into longitudinal strain through the Poisson effect. At resonance, the strain in the nFET channel on the sensing side modulates the mobility, resulting in an AC output
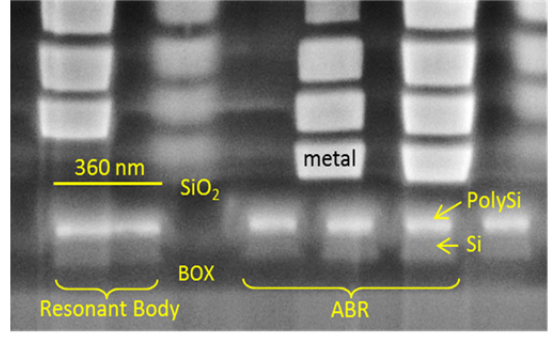

Fig. 2: SEM of CMOS stack obtained using FIB. The resonant cavity comprising of the SCS device layer and ABRs are seen at the bottom of the stack, fully buried under the metal layers.

current. In Si piezoresistive sensing provides a 10× boost in sensing as compared to capacitive sensing. Furthermore, the decoupling of the drive and sense mechanisms reduces the feed-through parasitics.

The principle of Acoustic Bragg Reflectors (ABRs) was used to define the acoustic cavity in these resonators. In the case of longitudinal waves, the acoustic impedance Z_{ac} is defined in terms of the effective Young's modulus E_{eff}, the acoustic velocity c, the Poisson ratio ν and mass density ρ as

$$Z_{ac} = \frac{E_{eff}}{c} = \sqrt{\frac{(1-\nu)\rho E}{(1+\nu)(1-2\nu)}}$$

ABRs consist of alternating materials with mismatched acoustic velocity, Z_{ac} patterned around the resonator, resulting in reflection of a majority of the acoustic energy back onto the resonant cavity. The resultant reflection coefficient along any surface when each of these materials contains a quarter wavelength $(\lambda/4)$ at the resonance frequency is given by $R = (Z_1 - Z_2)/(Z_1 + Z_2)$. The net reflectivity increases with the number of reflecting surfaces; every pair of alternating materials can be considered one pair of ABRs. The acoustic mismatch offered by various combinations of materials from the CMOS stack was considered for the design of ABRs. In this design, Si/SiO$_2$ was chosen as the material combination for ABRs as these materials occur in the Shallow Trench Isolation (STI) structures offered in this technology (Fig. 2). The acoustic impedance mismatch between Si and SiO$_2$ is $Z_{rel} = Z_{Si}/Z_{SiO2} \sim 1.47$ and the resultant reflectivity achieved using 7 pairs of ABRs is $R \sim 99.4\%$ based on 1D analysis [17].

At resonance, longitudinal acoustic vibrations are set up in the resonant cavity along with the ABRs. A sinusoidal standing wave is formed in the resonance cavity which decays exponentially in the ABR region with a decay length dependent on material properties. The first ABR was placed at a three quarter-wavelength $(3\lambda/4)$ distance from the resonant cavity based on DRC restrictions of the process which affects the reflection solid angle and consequently the quality factor Q of the resonator.

In the course of design of these resonators, several parameters of the foundry-provided nFETs were modified. Standard FET doping layers which define the source/drain and body doping were changed to allow ABRs to be designed as
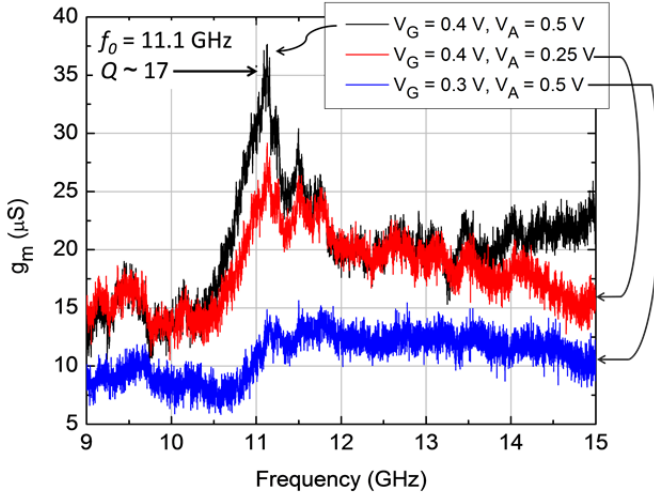
Fig. 3: Frequency response of an nFET-ncap resonator showing a resonance frequency of 11.1 GHz, Q~17. The back gate voltage V_A modulates the gain at resonance verifying the mechanical nature of the resonance peak.

close to the devices as possible. The shapes of the active device region of the SOI process and Poly gate regions were modified to create longitudinal bar like structures for definition of the resonant cavity. The number of metal contacts was reduced to reduce distortion of the resonant mode of vibrations.

III. EXPERIMENTAL RESULTS

Devices were fabricated at IBM's fabrication facility and realized without any post-processing or packaging. They were tested in a standard two-port configuration in a Cascade PMC200 RF probe system. SOLT calibration was carried out followed by measurement of open and short structures on the die to de-embed all of the routing up to the first metal level. All RF measurements were carried out at room temperature with -21.9 dBm input power, 30 Hz BW and no averaging using an Agilent PNA-X N5245A. The overall input to output transconducantance is obtained from the de-embedded Y parameters as $g_m = \frac{i_{out}}{v_{in}} = Y_{21} - Y_{12}$ as per the definition for a MOSFET [18].

A. RF Measurements

The frequency response of the input to output transconductance of an nFET-ncap device is shown in Fig. 3. The device shows a resonance frequency of 11.1 GHz with a Q ~17 extracted from FWHM. The amplitude of the resonance peak changes with the drive capacitor voltage V_A verifying the mechanical nature of the resonance peak. Similarly, changing the front gate voltage V_G results in a change to the drain current I_D, and therefore to the measured g_m of the device. The DC power consumed at the operating point is 35 µW for a device footprint of 3 µm × 5 µm.

Fig. 4 shows the frequency and phase response of pcap-nFET device designed on the same die which demonstrates a resonance frequency of 11.54 GHz with Q~24. In this device, the entire SCS layer is p-doped and the drive capacitor is p-doped instead of n-doped as in the nFET-ncap device. The
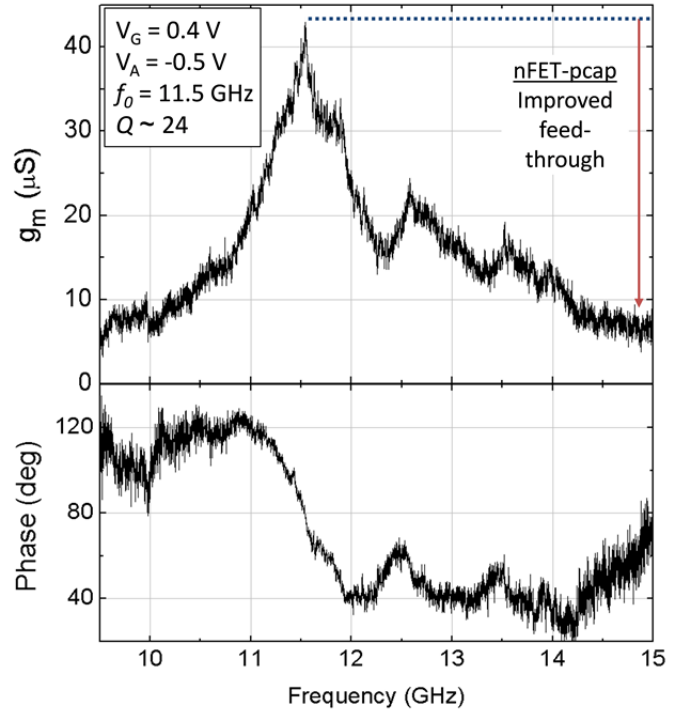

Fig. 4: Frequency response nFET-pcap with improved feed-through relative to the nFET-ncap device. Phase at resonance ~85 degrees.

parasitic reverse-biased diode in the nFET-ncap device increases feed-through with respect to the nFET-pcap device. Both of these devices driven with an n-doped or p-doped capacitors were designed with identical geometry but show different resonance frequencies possibly due to stress liners, degenerate doping leading to differences in acoustic velocity and fabrication differences between n–type and n-type doping which give rise to geometric differences. Devices with variations in ABRs were also fabricated in this process and are discussed in [8].

B. Active vs. Passive Sensing

Some passive devices using electrostatic drive and sense were also designed in this process to compare the relative performance of passive vs. active resonators (Fig. 5). 2-port RF measurements of these devices show no discernible resonance peak with respect to the feed-through, highlighting the importance of FET sensing at these frequencies.

C. Discussion of Performance

The Q of the RBTs is comparable to that of CMOS-integrated LC tanks at similar frequencies with the MEMS resonators approximately 10^4 smaller in footprint. However, compared to other acoustic resonators, the Q of these devices shows room for improvement. The acoustic properties of these devices can be precisely designed and simulated if material properties and dimensions of the FEOL stack are available. Accurate knowledge of the acoustic impedance and velocity of the STI fill material is critical to the design of ABRs for maximum reflectivity at the desired frequency. A deviation in properties such as density and Young's modulus make the ABR design mismatched to the resonator at the
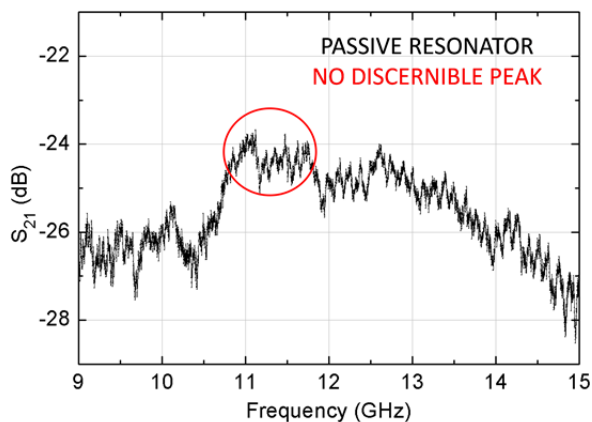
Fig. 5: Frequency sweep of a passive device with pcap drive and sense, showing no discernible peak around the designed resonance frequency of 12 GHz. Inset shows 3D structure of device in this process.
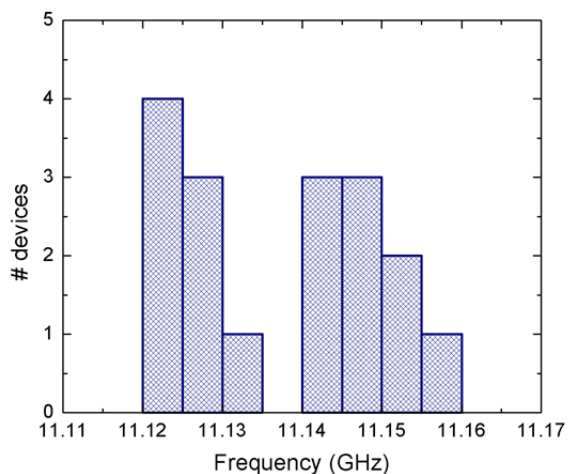

Fig. 6: Histogram showing the distribution of devices based on their frequency of operation for the same designed frequency. Variations are on the order of 0.1-0.5%.

resonance frequency, resulting in reduced gain, Q and an altered resonance frequency. The increased thickness and induced strain from the stress liners further affect the acoustic properties of the resonant cavity. Similarly, the dimensions and location and processing method of the silicide contacts to the PolySi gate and the source/ drain regions affect the aspect ratio and the mode shape in the thickness dimension resulting in spurious modes. Copper contacts made to the source/drain regions may produce "anchoring points" or different boundary conditions from those offered by the low-k dielectric (SiCOH) surrounding the resonant cavity [16]. Several of these parameters and properties of the FEOL stack were unknown or could not be shared by the foundry resulting in compromised device performance in first-generation devices.

Another set of structures which strongly affect device performance are the Copper layers appearing vertically above the resonator due to CMP fill generation. These form ABRs in the vertical direction due to the acoustic mismatch between the SiCOH and Cu layers leading to thickness spurious modes. These layers can be excluded from future designs or patterned to create 3D Bragg reflectors around these structures.

D. Fabrication Variations and Yield

The yield of FETs in the process was nearly 100%, which came as a wonderful surprise for these first-generation MEMS-CMOS devices. This emphasizes the merits of CMOS integration to harness the high yield of standard CMOS processes for MEMS design. The variation in the resonance frequency of these devices, designed with identical resonance dimensions is around 0.1-0.5%, shown in Fig. 6, and is attributed to lithographic process variations. On the electrical side, these variations are in the form of the variance in FET V_T, I_D, C_{Ox} and R_s which affect the drive and sense efficiency, the gain at resonance, and electrical contribution to the total Q. On the fabrication side, geometric or material variations from mask misalignments, sidewall slope and roughness, film thickness, stress layers and variation in material acoustic properties affect the resonance frequency and Q.

Some of these variations may be mitigated by mechanically coupling these resonators which has been shown to improve the feed-through, suppress spurious modes, and improve gain at resonance with the tradeoff of a larger overall footprint [19,20].

IV. TEMPERATURE STABILITY

Thermal stability is an important characteristic of any resonator required for reliable operation in oscillators, filters, sensors, and other communication and navigation systems. Si resonators typically exhibit temperature coefficient of frequency (TCF) of -20 to -30 ppm/K but use of materials with positive temperature coefficient of Young's modulus (TCE) such as SiO_2 has been demonstrated for thermal compensation [21]. The CMOS-integrated resonators presented in this work are inherently surrounded by SiO_2 in the STI fill used to define ABRs and are hence expected to show TCF compensation from the complimentary Si/SiO_2 pairing. The temperature performance of these CMOS-MEMS resonators was thus investigated above room temperature under N_2 purge to avoid ESD events.

The devices were measured at room temperature (300K) and at 340K and 380K. The DC biasing conditions were the same as previous measurements. Ceramic-substrate calibration and on-chip de-embedding were carried out at every temperature with -21.9 dBm input power, 30 Hz BW and no averaging. The fact that resonance peaks exist across temperatures with independent calibrations validate that they arise from the device and not from any artifacts of the RF measurement.

Due to the presence of spurious modes (from CMP fill) in close proximity to the resonance peak and the small value of the frequency shift, the TCF could not be directly extracted from g_m measurement. Numerical modeling techniques were thus used to perform temperature stability analysis. Systems with multiple resonances in the frequency response can be modeled accurately using rational transfer function of the form

$$H(s) = \sum_{k=1}^{\kappa} \frac{R_k}{s-a_k} + D \ .$$

Here $a_k's$ and $R_k's$ are poles and residues respectively, κ is the total number of poles used and it defines the model order. For this model to be physically consistent, it was ensured that the complex poles appear in conjugate pairs and all the poles are stable, i.e. they have negative real part ($\Re a_k < 0$). For our analysis, the model $H(s)$ that minimizes the mismatch between the measured transconductance and output of the model using an optimization framework as described in [22,23].

For the example presented here, de-embedded S-parameters of the resonator measured at the above-mentioned temperatures were used to compute the transconductance g_m. Rational transfer functions with 22 pairs of complex conjugate poles ($\kappa = 44$) each were used to model the transconductance as a function of frequency computed for different temperatures and a high-quality fit was obtained (Fig. 7(a)). Next, the smooth outputs of these models were analyzed to locate the resonant frequencies and their sensitivities to operating temperature. Temperature sensitivities of individual spurious modes were reported in terms of total frequency shift $\frac{\Delta f}{f_0 \Delta T} \left(\frac{ppm}{K} \right)$ instead of TCF (Fig. 7(b)). Error bounds were computed by analyzing the noise in measured data and the RMS error generated by our model. It is noted that the error bounds for high-Q resonances, such as the one at 11.17 GHz, are tighter than the error bounds for low-Q resonances, such as the one at 11.19 GHz.

Two different families of poles were observed- those showing positive TCF indicating oxide-dominated modes and those with negative TCF showing Si-dominated modes. Some modes were observed with sub-ppm TCF which demonstrates almost complete compensation of the thermal properties of Si by the surrounding SiO_2. The CMOS-integrated RBTs achieve thermal compensation for free due to the intrinsic material properties of the CMOS stack. This complimentary nature of the TCE of Si/ SiO_2 provides the opportunity to engineer the TCF of the resonance peak in future designs to either obtain a high TCF for design of temperature sensors or for a low TCF for oscillators and filter design.

V. CONCLUSION

The first CMOS-based unreleased RBTs are demonstrated in IBM's 32SOI process with resonance frequencies between 10-12 GHz, Qs of 15-25 and footprint of less than 5µm×3µm. They are fabricated at the transistor level of the FEOL CMOS stack and are realized without the need for any post-processing or packaging. These devices are the first step towards realizing on-chip acoustic frequency sources with reduced size, power and parasitics in wireless communication, navigation and sensing systems.

Multiple types of resonators were designed in this technology. A comparative analysis and experimental results obtained in this process show the merits of active transduction mechanisms for scaling of resonators to multi-GHz frequencies. Device performance can be further enhanced by characterizing material properties of the CMOS stack,
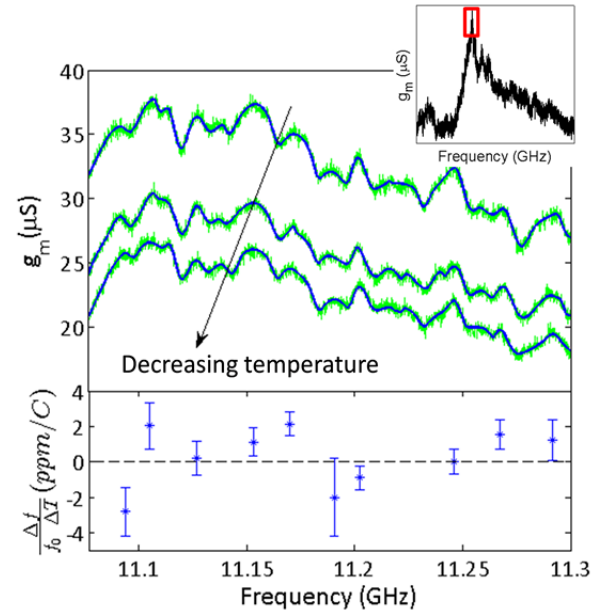

Fig. 7: (a) Zooming in around the measured resonance peak included in inset shows multiple spurious modes that make up the peak. Plot compares measured values of the transconductance and data fitted using rational transfer functions. Light noisy lines show the measured data while the solid dark likes show the output from our model. (b) $\frac{\Delta f}{f_0 \Delta T} \left(\frac{ppm}{K} \right)$ with error bars plotted against frequency.

manipulating the stress liners, silicide and metal layers. With these design parameters, optimization of the CMOS-MEMS RBT can significantly improve the resonance gain, Q, spurious modes suppression, and electrical feed-through. These resonators demonstrate thermal stability as compared to Si-only devices with TCFs between -3 and 3 ppm/C. The complimentary nature of the TCFs of Si and SiO_2 has the potential for TCF manipulation for design of temperature sensors with high TCF or oscillators with sub-ppm/K sensitivity.

Seamless integration into a standard CMOS process obviates the need for complex and costly custom processes for MEMS fabrication. This demonstration of resonators fabricated side-by-side with CMOS circuitry greatly reduces parasitics of off-chip access, constraints of limited IO, and power consumption associated with impedance matching networks. These benefits can provide increased system speed and dynamic range, particularly at RF and mm-wave frequencies of operation.

ACKNOWLEDGMENT

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