11.1 A 3.4pJ FeRAM-Enabled D Flip-Flop in 0.13µm CMOS for Nonvolatile Processing in Digital Systems

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Nonvolatile processing—continuously operating a digital circuit and retaining state through frequent power interruptions—creates new applications for portable electronics operating from harvested energy [1] and high-performance systems managing power by operating "normally off" [2]. To enable these scenarios, energy processing must happen in parallel with information processing. This work makes the following contributions: 1) the design of a nonvolatile D flip-flop (NVDFF) with embedded ferroelectric capacitors (fecaps) that senses data robustly and avoids race conditions; 2) the integration of the NVDFF into the ASIC design flow with a power management unit (PMU) and a simple one-bit interface to brown-out detection circuitry; and 3) a characterization of the NVDFF statistical signal margin and the energy cost of retaining data.

This chip's process technology features embedded ferroelectric capacitors that store data in a charge versus bias voltage hysteresis [3]. This hysteresis is shown in Fig. 1 along with the principle of self-timed sensing. Prior to sensing, the fecaps have been programmed to opposite data states, corresponding to opposite points on the zero bias voltage points of the hysteresis curve. Identical charging currents integrate the difference in remnant charge between the two fecaps onto nodes FET and FEC. The node to first cross the diode voltage drop plus a PMOS threshold will quickly pull the internal node of the sensing latch high. The ferroelectric capacitance is large compared to the internal node of the sensing latch, so a small voltage difference on the high capacitance nodes FET and FEC is converted to a large voltage difference on the latch nodes. In addition to being self-timed, this approach develops sufficient bias (1.1 V) before the fecaps are sensed. Fecap signal dynamics are exponentially sensitive to voltage bias [4], so it is important to avoid the performance penalty associated with sensing at low bias.

The schematic of the nonvolatile latch in Fig. 2 shows the additional transistors for saving data, isolating fecaps during active operation, and protecting fecaps during power loss. This latch is combined as the slave stage with a clocked CMOS master latch to form the NVDFF in Fig. 3. The waveforms show how the ports PG, LD, EQ, and VDDNV need to be sequenced during power interruption. While active, PG=LD=0, and nodes FET and FEC act as a virtual supply for the slave latch. The save operation initiates when PG rises as CK is held low, cutting off VDDNV and enabling a weak pull-down path (M8-M10) to discharge one of the two fecaps (write "0") depending on the data state of the slave latch. The subsequent rise of LD preserves the data in the other fecap, which has already been written to a "1" during the previous restore operation. Prior to power loss, the EQ signal assertion clears floating voltages inside the slave latch, and then the VDDNV rail is discharged to prevent conducting paths to nodes FET/FEC. A complementary sequence is applied after VDD and VDDNV return high for restore. First, PG falls low, and then the PMOS diodes M3 and M4 bias M1 and M2 into their saturation region. The voltage on node PBIAS also sets the threshold at which QT and QC are exposed to FET and FEC. Both the pull-up and pull-down paths for nodes FET/FEC are sized weak so that no more than 10 µA of peak current is drawn by each NVDFF. These issues related to avoiding race conditions, sensing fecaps at high voltage bias, and minimizing peak current prevent the adoption of the conventional ferroelectric DFF based on a pair of fecap dividers [5]. Additionally, the proposed NVDFF consumes 40% less energy (from simulation) because it contains 2 fecaps instead of 4.

Fig. 4 shows the architecture of the nonvolatile state management. A test case FIR filter has all of its volatile DFFs replaced by NVDFFs. Also added are buffer trees for the PG, LD, and EQ signals and a global rail VDDNV that supplies current for the toggling of internal slave latch nodes and FET/FEC. This system works with the energy harvester interface in [6] which provides a VBAT_OK signal that rises only if a sufficient amount of energy exists in the system to restore and save state. Similarly VBAT_OK falls when the system is about to lose its minimum energy reserve. A free running clock that settles before VBAT_OK goes high is also required. The signals VBAT_OK, CLK, and the 1.5 V chip supply are emulated by a pattern generator during chip testing. An on-chip power management unit (PMU) takes the VBAT_OK signal and generates a control signal sequence (see FSM in Fig. 4) whose transitions align to the PMU's clock edges and satisfies the timing constraints in Fig. 3.

The waveform set "A" in Fig. 5 shows the measured output of the test-chip during a power interruption in which all chip VDDs are actively driven to ground. Afterwards, the FIR filter resumes operation with the correct state. The waveform set "B" zooms in on the power-loss event. The FIR values are consistent with the relation in Fig. 4, the provided inputs, and the programmed coefficients (w_1, w_2, w_3) equal to (87, -77, -98). The fall of VBAT_OK passes through a two-register synchronizer and then the FIR filter freezes as the PMU coordinates the save operation. In the 8th cycle after the fall of VBAT_OK, the save completes and the rise of EQ sets all outputs of the FIR filter to "1" (the NVLATCH node is buffered with an inverter). The PMU waits another 2 cycles to let the internal VDDNV rail completely discharge. Then, it is safe to cut off all power to the chip. The waveform set "C" zooms in on the power-restoration. In the 6th cycle after VBAT_OK rises, the correct data has been restored to the FIR filter. In the 10th cycle after VBAT_OK rises, the FIR filter resumes computation with the previously programmed coefficients. In the example of the FIR filter, the parallel save and restore of the NVDFF takes only 10 cycles to resume; whereas a volatile implementation would have required 24 cycles to reprogram the 3 filter coefficients.

The FIR filter has 96 NVDFFs and about 500 gates. For a target application of a microcontroller, approximately 5,000 DFFs need to be retained. The plot in Fig. 6 shows the amount of failures induced in 8 shift registers of 512 NVDFFs (4096 total) when a skew is applied. The NVDFF has a split supply rail, so the sensing current ramps can be perturbed from their nominally identical values. In simulation, the relationship between the skew on VDDNVT/VDDNVC and percentage skew in current ramp rate is roughly linear. The distribution of fails exhibits a Gaussian-like quadratic decrease on a logarithmic vertical scale as the skew is reduced. With zero skew, all NVDFFs in all 5 measured chips (about 21,000 NVDFFs) operate without failure, and extrapolation of the distribution under skew suggests well below 1 ppm failure for the un-skewed NVDFF. The pie chart in Fig. 6 describes the total round-trip save and restore energy for the NVDFF. By measuring the energy in both the context of a shift register (no logic and little interconnect) and the context of an FIR filter, the additional energy cost from nodes glitching in the FIR filter, cycle overheads, and PMU energy can be quantified to 1.780 pJ out of 3.439 pJ.

Fig. 7 shows the die photo, summarizes key parameters, and makes comparison to related work in [7]. The present approach of replacing every volatile DFF with an NVDFF incurs a 49% area overhead in the FIR filter (based on the synthesis report) in exchange for nonvolatile processing capability.

References:
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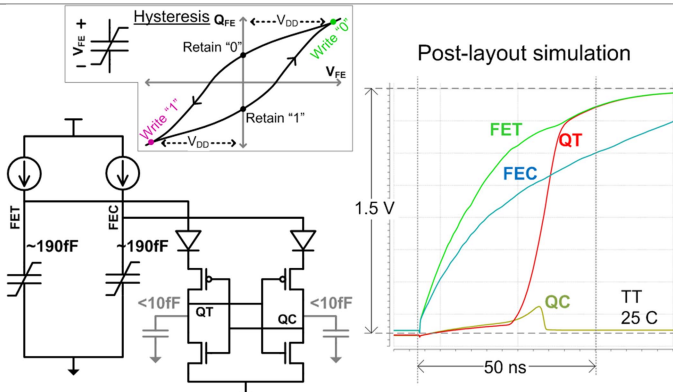
Figure 11.1.1

Hysteresis Q_{FE}

Retain "0"

Write "0"

V_{DD}

Write "1"

Retain "1"

$-V_{DD}$

V_{FE}

Post-layout simulation

1.5 V

FET
FEC
QT
QC

TT
25 C

50 ns

FET ~190fF   FEC ~190fF

<10fF   <10fF

QT   QC

Figure 11.1.1: Principle of self-timed sensing for ferroelectric capacitors through charge sharing

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FeCap read & write circuits

FeCap sense amplifier and slave-stage jam latch

VDDNV

M7

VDD

M1   M2

CK

PBIAS

FET   FEC

M3   FET   PBIAS   FEC

M4   QC   QT   M5   M6

M8   M9

$\overline{D}$ QT   QC   D

M10

PG

SN

LD

FET   FEC   QT   QC

EQ
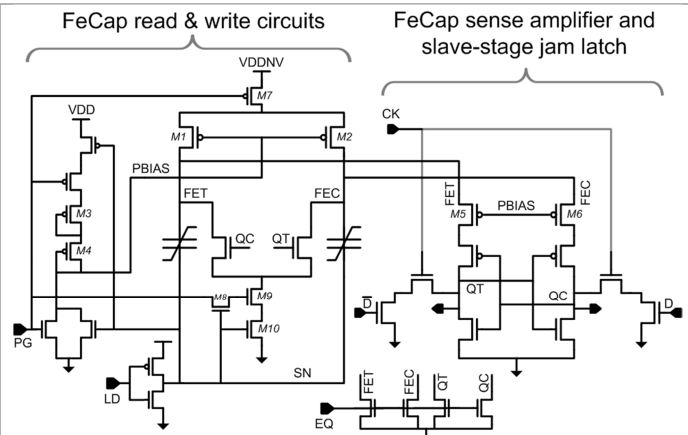
Figure 11.1.2: Schematic of the nonvolatile latch (NVLATCH)

PG, LD, EQ

D   CK

$\overline{CK}$ VDDNV $\overline{D}$ QT

CK

NVLATCH

$\overline{CK}$ D   QC   Q

CK

NVDFF

Mode	PG	LD
Off	1	1
Restore	0	1
Active	0	0
Save	1	0

1.5 V

FEC
FET
QC
QT

VDDNV   VDD

CLK

D   Q

PG

LD

EQ

0 ns   1 us   2 us

Simulation Sequence:

Active

↓

Save (0.25 us)

↓

VDDNV discharge (0.45 us)

↓

Full power off (0.3 us)

↓

VDDNV charge (0.45 us)

↓

Restore (0.25 us)

↓

Active
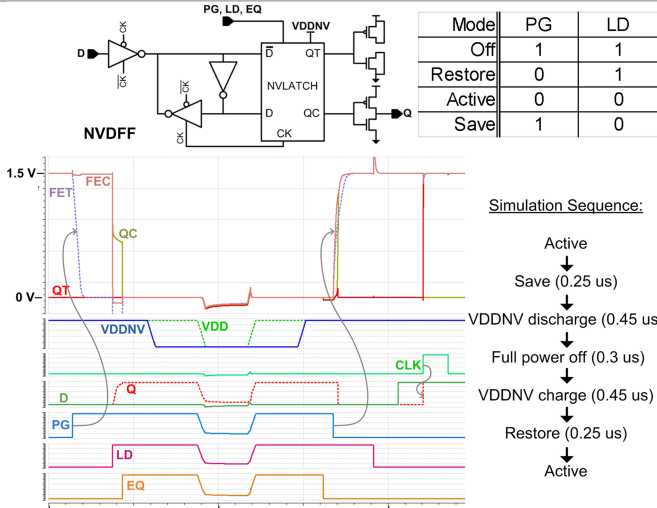
Figure 11.1.3: The nonvolatile D flip-flop (NVDFF) and simulation of its four modes

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T: VDD (1.5 V)

POR

S   Q

R $\overline{Q}$

ENVDDNV
DISVDDNV

PMU

$\overline{rst}$

POR

S   Q

R

LOCK

VDDNV

harvester interface circuits

VBAT_OK

PG, LD, EQ

Digital Circuit

ENCK

VBAT (2 to 5 V)

C_{STOR} (~ 10 uF)

Free Running Clock

CLK Gate

D   Q

Embedded NVDFF

on-chip

PMU FSM:

Reset

Discharge VDDNV

VBAT_OK == 1

Enable VDDNV

Sequence control signals PG, LD, EQ to save NVDFF State

Sequence control signals PG, LD, EQ to restore NVDFF State

Disable CLK

Enable CLK

VBAT_OK == 0

Active Operation

$x[n]$ 8 z^{-1} z^{-1} z^{-1} z^{-1} z^{-1} z^{-1} z^{-1}

w   shift register (24 b) w_1 w_2 w_3

en

clk

Programmable FIR filter testcase

$y[n] = w_3 \times x[n-7] + w_2 \times x[n-6] + w_1 \times x[n-5]$

16   z^{-1} $y[n]$

Figure 11.1.4: A nonvolatile system implementation with NVDFFs in a test-case FIR filter

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Time Stamp = 50.895us

VBAT_OK

CLK

FIR_IN

FIR_OUT

VDDNV

-1   0   -1

power loss

A

VBAT_OK

CLK

FIR_IN   72   120   -2   90   -75   60   45   -111   72   120   -2   90   -75   60   45   -111   72

FIR_OUT   -3776   -13259   2175   6645   -19002   10401   15774   -16470   -3776   -1

FIR output frozen at "-3776"

B

VBAT_OK

CLK

FIR_IN   -75   60   45   -111   72   120   -2   90   -75   60   45   -111   72   120   -2   90

FIR_OUT   -1   -3776   -13259   2175   6645   -19002

FIR output restored to "-3776"

C
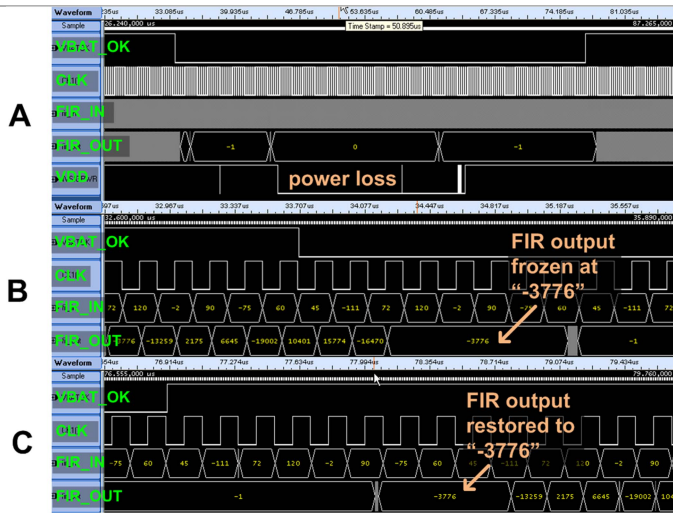
Figure 11.1.5: Logic analyzer waveforms from the test chip undergoing power loss and recovery

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VDDNV

PG   M7

M1   PBIAS   M2

FET   FEC

Skew circuit

VDDNVT   VDDNVC

PG

M1   PBIAS   M2

FET   FEC

NVDFF Shift Register Checkerboard Read Test

failing fraction

Chip 1
Chip 2
Chip 3
Chip 4
Chip 5
Total

0.8   0.9   1   1.1   1.2   1.3   1.4   1.5

Skewed VDDNVT [V] with VDDNVC=1.5V

NVDFF Round-trip Save & Restore Energy, 3.439 pJ Total

FeCap Switching Energy

1.195 pJ 35%

1.780 pJ 52%

0.464 pJ 13%

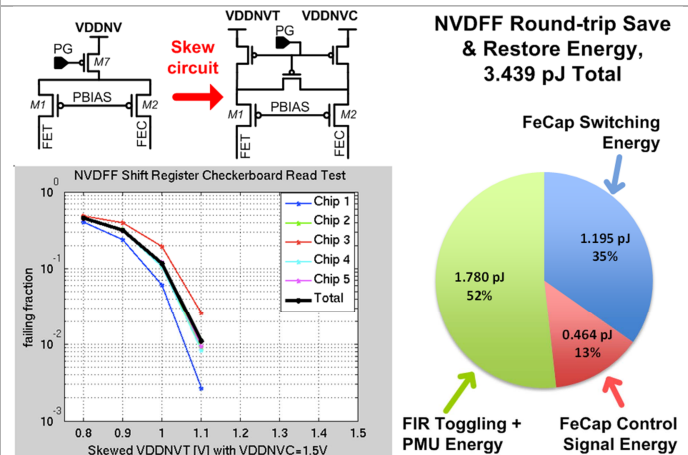FIR Toggling + PMU Energy

FeCap Control Signal Energy

Figure 11.1.6: NVDFF measured properties of statistical margin (from 5 chips) and round-trip energy