Test Structure, Circuits and Extraction Methods to Determine the Radius of Influence of STI and Polysilicon Pattern Density

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***Abstract*—Advanced CMOS processes need new methodologies to extract, characterize and model process variations and their sources. Most prior studies have focused on understanding the effect of local layout features on transistor performance; limited work has been done to characterize medium-range ($\approx$ 10μm to 2mm) pattern density effects. We propose a new methodology to extract the radius of influence, or the range of neighboring layout that should be taken into account in determining transistor characteristics, for shallow trench isolation (STI) and polysilicon pattern density. A test chip, with 130k devices under test (DUTs) and step-like pattern density layout changes, is designed in 65nm bulk CMOS technology as a case study. The extraction result of the measured data suggests that the local layout geometry, within the DUT cell size of 6μm x 8μm, is the dominant contributor to systematic device variation. Across-die medium-range layout pattern densities are found to have a statistically significant and detectable effect, but this effect is small and contributes only 2-5% of the total variation in this technology.**

I. Introduction

Transistor scaling has helped increase the performance of VLSI circuits tremendously over the past decades. As scaling continues, the neighborhood of the layout becomes an important factor in determining MOSFET characteristics. Differences in nearby layout features, such as proximity and density of polysilicon, can systematically introduce variations in two transistors with nominally identical dimensions [1]. In order to design robust and functional circuits, a more complete and accurate variation model is necessary [2]. Much work has been done to identify and characterize variation behaviors. The effort can be roughly divided into three groups as shown in Fig. 1. The first group focuses on variation induced by changes in local layout geometries while keeping the pattern density constant across the chip. The second group focuses on variation induced by changes in regional pattern density while keeping the transistor geometry constant. This work falls into the third group: our goal is to consider variation when both local layout and regional pattern densities are changing and further study the interaction between regions of different pattern density.

The work done by [3–6] falls into the first approach. Pang *et al.* [3] investigate ring oscillator frequency and leakage current variations as a result of different transistor layout geometries, such as finger spacing, orientation, width and length dimension and local polysilicon density. Tsuno *et al.* [4] develop a variation model to capture the effects of gate spacing, shallow

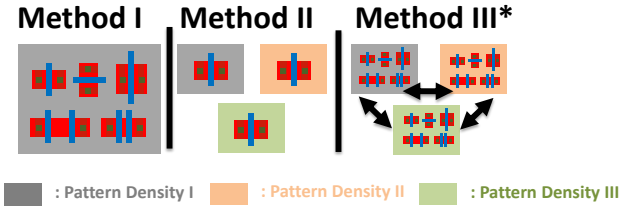

Fig. 1. Methods of transistor variation studies.

trench isolation (STI) width, and interaction between gate-STI distance and STI width on threshold voltage. Gettings *et al.* [5] use a similar set of layout features but extend the analysis to passive components such as interconnect. Sheu *et al.* [6] model the systematic variation in threshold voltage induced by ion scattering due to different proximity of well edges during the implantation process. Ye *et al.* [7], on the other hand, focus on variation studies of the second group. A test structure is designed with different regions of layout style, such as VCO, logic, data paths, and registers, resulting in different regional pattern densities. The difference in pattern densities introduces systematic variation in ring oscillator frequency in different regions of the die.

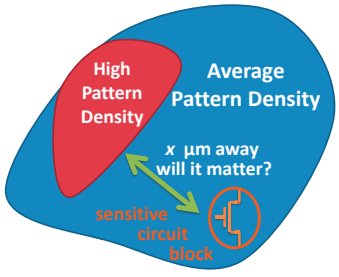

Fig. 2. Systematic variation induced by medium-range interaction between regions of different pattern densities.

The collective pattern density of a region of laid-out features can affect not only the characteristics of transistors within the region but also the characteristics of transistors in the nearby neighborhood. Our goal is to study whether this interaction exists and identify the interaction distance. We define this distance to be the *radius of influence*. The area within a circle having this radius specifies the neighborhood of shapes which

play a part in determining characteristics of a MOSFET. Fig. 2 summarizes our objective. In this case, the largest x, which still has a significant influence on the performance of the sensitive circuit block, is the radius of influence.

This paper is organized as follows with several new contributions. In Section II, we discuss the choices of STI and polysilicon pattern densities as the parameters for variation studies. In Section III, a new test structure with 130k devices under test (DUTs) is described. Micro- and macro-layout strategies are designed to extract the radius of influence. In Section IV, we introduce a novel circuit architecture to enable accurate multiplexed current measurement of every DUT on the die. Methodologies to extract the radius of influence are described in Section V. Hypothetical variation scenarios are defined to demonstrate the variation extraction procedure. Section VI applies the extraction methodology and provides analysis on measured data. An unexpected result of our analysis is that within the die size of 2mm x 3mm, the influence of medium-range ($\approx 10\mu$m to 2mm) pattern density is quite small in this technology. Section VII concludes the paper and provides implications for future design flows based on our results.

II. Design Parameter Choice

In order to study the interaction between regions of different pattern density, a precise definition of pattern density is required. Different pattern densities and layout geometries are used to understand one or more specific variation mechanisms; our design focuses on variation mechanisms associated with STI, etch and rapid thermal anneal.

A. Polysilicon Pattern Density

Several studies have investigated variation in etch due to the differences in local polysilicon layout patterns [8]. The advent of advanced RTA processes, to form shallower drain/source regions to reduce short-channel effect, has furthered the need for such work [9]. The length scale over which thermal equilibrium can be reached is in the millimeter range, meaning the specific thermal profile created by device layout patterns created by device layout patterns may affect all transistors within that range. Kuhn *et al.* [10] show that non-uniformity in polysilicon pattern density translates into non-uniformity in temperature profile during the annealing process. This non-uniformity can influence dopant diffusion and activation processes. However, none of these works has quantified the range of influence.

B. STI Pattern Density

One STI variation concern relates to channel strain induced by STI regions of neighboring layout. The strain changes silicon crystal structure resulting in carrier transport velocity changes. In advanced technologies, intentional strain plays a key role in improving transistor performance [11, 12]. However, as critical dimension shrinks, the distance between neighboring layout features becomes smaller; therefore, unintentional strain induced by neighborhood STI structure can also influence transistor characteristics [13–15].

Research has sought to understand strain induced by STI. Moroz *et al.* [16] experiment with different transistor layouts to quantify variations induced by stress. Kahng and Topaloglu *et al.* [17, 18] exploit possible ways to optimize transistor performance by placing dummy STI, suggesting an increase in performance by 7%-11% without area penalty. In both cases, the authors consider the influence of local STI features and shapes. Our goal is to further such research by investigating whether this strain propagates to nearby transistors and identifying this interaction distance.

III. Test Structure Design

The test structure is proposed to 1) investigate and quantify the longer-range interaction between regions of different pattern densities, and 2) study how the interaction affects transistors with different local geometries. The overall layout strategy is divided into macro- and micro-layout strategies. The macro-layout is concerned with systematic variation due to medium-range surrounding layout scaled by some appropriate weighting function, while the micro-layout is concerned with variations due to different local transistor layout geometries.

A. Macro-layout Design Strategy

The macro-layout strategy is designed to 1) accentuate the spatial interaction between regions of different pattern density, and 2) cover the design space by including combinations of high and low pattern density in both short-range and medium-range pattern density. The entire structure is divided into six different regions of $1mm$ x $1mm$ as shown in Fig. 3. The three red regions study medium-range interaction between different STI pattern densities and the green regions are for studying the interaction related to polysilicon pattern density.

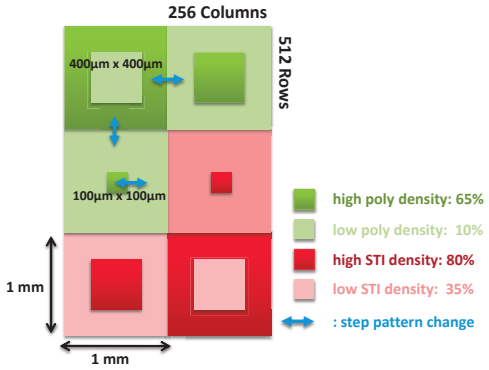

Fig. 3. Test structure layout.

The change in magnitudes of a color (e.g., dark green to light green), indicated by the blue arrows, represent a "step" pattern density change from *high* to *low*. To enable a linear system modeling approach, the layout pattern density impulse response can be generated from the step response [19]. Three layout regions containing different sizes of contrasting pattern densities ensure good coverage of the design space, and enable extraction of two different length scales or radii of influence, both a medium-range and a shorter-range interaction

distance, perhaps arising due to two different physical sources of variation. Each region is $1mm$ x $1mm$ in size. The larger square in each region has dimensions of $400\mu m$ x $400\mu m$, while the smaller square inside each region has dimensions of $100\mu m$ x $100\mu m$. These sizes are our initial guesses as to the radius of influence of pattern density effects: we assume the medium-range pattern density effect is within 1mm and the shorter-range pattern density effect is between 100μm and 400μm.

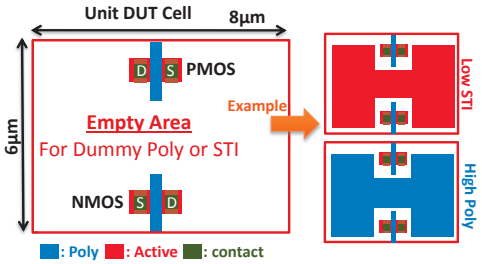

Fig. 4. Test structure building block.

The test structure consists of 512 rows and 256 columns of a unit building block, shown in Fig. 4. Each unit building block is $8\mu m$ wide and $6\mu m$ long, and consists of one NMOS transistor at the bottom and one PMOS transistor at the top. The empty area is to provide flexibility to change pattern density to the desired value in that region according to the specifications of the macro design. Two examples of low STI and high poly pattern densities are shown.

B. Micro-layout Design Strategy

In the micro-layout strategy, we explore different width (W), length (L), active area size (OD), number of poly fingers (#F) and spacing between poly fingers (PO). A design of experiment following a modified centroid composite design, with unevenly dividing spaces of factors (e.g. width: 200μm $\rightarrow$ 400μm $\rightarrow$ 1000μm), is shown in Table I. Table II shows the row layout pattern of the test structure; the number corresponds to the type of DUT. This three-row block is repeated both vertically and horizontally to make up the overall test structure. An addition of row 1 is added on the top to complete the 512 rows. The rows are patterned such that the test chip consists of many spatial separation distances for the canonical DUT types.

TABLE I
MICRO-LAYOUT DESIGN STRATEGY

DUT	W (nm)	L (nm)	OD (nm)	# F	PO (nm)
1	200	60	195	1	N/A
2	400	60	195	1	N/A
3	200	60	500	1	N/A
4	200	180	195	1	N/A
5	200	180	195	2	220
6	200	180	195	3	220
7	1000	60	195	1	N/A
8	200	1000	195	1	N/A
9	1000	1000	295	1	N/A
10	200	180	195	2	500

TABLE II
DUT ROW LAYOUT PATTERN

Row	DUT Pattern							
1	1	1	3	2	1	4	2	2
2	7	5	6	8	10	5	6	9
3	1	1	3	2	1	4	2	2

IV. Test Circuit Design and Architecture

Our proposed test circuit design uses a new hierarchical access scheme to allow a large number of measurable DUTs with dense spatial sampling. Hierarchical accessing concepts have been presented in the past to study transistor variation with some limitations [20, 21]. The test circuit presented in [20] requires at least two access transistors per DUT, while our new scheme requires only two access transistors for every 128 DUTs. At the same time, our test circuit also eliminates the need for left sensing and left sinking banks in [21] while still maintaining measured current accuracy of better than 1%.

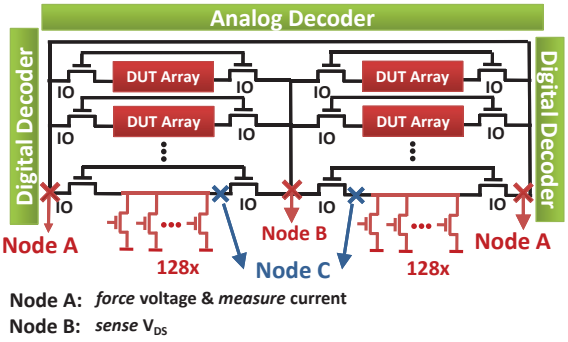

Fig. 5. Hierarchical access scheme, with high area usage efficiency.

A. New Hierarchical Access Scheme

Our new hierarchical access scheme is presented in Fig. 5. The access scheme is analogous to that in memory design, where row and column enables select the DUT on which to perform a measurement. The row decoders are typical digital decoders to enable the rows, but column decoders are analog decoders to apply V_{gs}. Each DUT array consists of 128 DUTs placed in parallel. For NMOS transistors, the sources are connected to ground, and for PMOS the sources are connected to the supply voltage. Two input-output (I/O) devices acting as row-enabling switches are placed across each DUT array. The gate of a DUT in an array is connected to the gates of all DUTs in other arrays which are in the same position as itself, but only within the same side of the test structure. Each of these gate connections forms one column, with a total of 256 columns. With 256 columns and 512 rows, a total of 131,072 DUTs are in the test structure. The new proposed access scheme is a highly efficient hierarchical access scheme in terms of the ratio of DUTs and peripheral transistors at 128:2. Most of the die area is dedicated to DUT layout.

For each DUT measurement, we apply the desired gate voltage to that DUT through the column enable signal; for

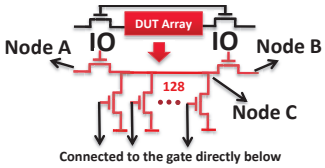

Fig. 6. Gate connections in the area-efficient hierarchical access scheme.

drain voltage, we apply a voltage on *Node A* of the DUT array and sense the voltage on *Node B*. *Node B* is designed to be high impedance to reflect the actual drain voltage on the DUTs. All other DUTs within the same array are turned off by the column decoder switches and all the other DUT arrays are turned off by the row decoder switches.

B. Applied Voltage Accuracy

The accuracy of applied gate voltage, V_{gs}, is ensured by the architecture of the design. Since the current flowing through the applied gate voltage is predominately gate leakage, the voltage difference between the applied gate voltage and the actual gate voltage on the DUTs is insignificant. On the other hand, ensuring an accurate drain voltage is not as trivial. Even though the sensed voltage on *Node B* can closely reflect the actual voltage on *Node C*, the voltage on *Node C* is not necessarily the same as the drain voltage on the selected DUT in a given array. Voltage drops on the wire resistance between *Node C* and the drain of the selected DUT is unavoidable. The current measurement is targeted to have better than 1% accuracy over all regions of transistor operations.

The square-law approximation of transistor current in saturation region is given in (1). W and L are the width and length of the transistor, μC_{ox} is the transconductance, V_t is the threshold voltage, and λ is the channel-length modulation parameter.

$$I_{ds,sat} \approx \frac{1}{2} \cdot \frac{W}{L} \cdot \mu C_{ox} \cdot (V_{gs} - V_t)^2 \cdot (1 + \lambda \cdot V_{ds}) \quad (1)$$

$$\frac{\partial I_{ds,sat}}{\partial V_{ds}} \times \frac{\Delta V_{ds}}{I_{ds,sat}} = \frac{\lambda}{1 + \lambda \cdot V_{ds}} \times \Delta V_{ds} \quad (2)$$

$$ASF_{sat} = \frac{\lambda}{1 + \lambda \cdot V_{ds}} \quad (3)$$

The sensitivity of current change with respect to voltage change is obtained by taking the derivative of current with respect to the drain voltage, V_{ds}. The absolute change in current with respect to change in drain voltage is calculated by (2). We call this multiplication factor the *absolute sensitivity factor* (ASF). Applying the same operations on the linear and subthreshold regions of operations, ASF_{lin} and ASF_{sub} are obtained as shown in (5) and (7).

Linear region:

$$I_{ds,lin} \approx \frac{1}{2} \times \frac{W}{L} \times \mu C_{ox} \times (V_{gs} - V_t) \times V_{ds} \quad (4)$$

$$ASF_{lin} = {V_{ds}}^{-1} \quad (5)$$

Subthreshold region:

$$I_{ds,sub} \approx I_0 \times e^{\frac{V_{gs} - V_t + \eta \cdot V_{ds}}{n \cdot V_t}} \times \left(1 - e^{\frac{-V_{ds}}{V_t}}\right) \quad (6)$$

$$ASF_{sub} = \eta \quad (7)$$

where η is the DIBL coefficient and n is the subthreshold slope ideality parameter. In modern technology, λ is less than 1, and η is between 2 and 3. Using $\lambda = 1$, $\eta = 2$ and $\Delta V_{ds} = 1mV$, as an example, we obtain $ASF_{sub} = 2$, $ASF_{lin} = 10^3$ and $ASF_{sat} = 1$. This result shows that ASF in the linear region dominates that of the other regions. Fig. 7 plots the simulated percentage inaccuracy at $\Delta V_{ds} = 1mV$ in SPICE. As predicted by calculation, the ASF dominates at V_{gs} and low V_{ds}, which is precisely the characteristics of linear region. It also shows that with $\Delta V_{ds} = 1mV$, $\Delta I_{ds}/I_{ds}$ is less than 1% in all regions of operation, satisfying targeted accuracy.

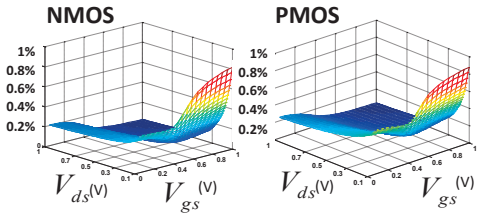

Fig. 7. Simulated (SPICE) current inaccuracy at $\Delta V_{ds} = 1mV$.

The voltage difference between *Node B* and *Node C* can be described in two cases as shown in Fig. 8. In the first case, the DUT to be measured is located at the very right edge of the array. Since all the current flow occurs to the left of the DUT, there is no current flowing into or out of *Node C*. As a result, no voltage drops across the drain of the DUT and *Node C*. In the second case, the DUT to be measured is located at the left edge of the array. In this case, current flow does occur on the right side of the DUT, causing a voltage drop between *Node C* and the drain node. This voltage drop is minimized by applying a negative voltage on the off-DUTs to reduce drain leakage current. The voltage drop on the wire is found to be less than $10\mu V$ in the worst case, thus satisfying the required current accuracy at 1%.

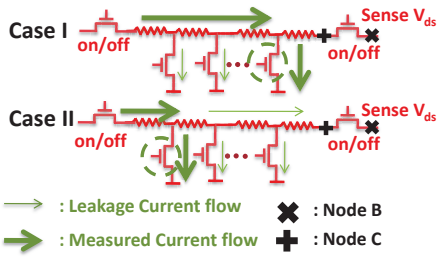

Fig. 8. Drain voltage inaccuracy due to voltage drop.

C. Measured Current Accuracy

The current measurement of every DUT in the test structure is done through *Node A* in Fig. 5. When measuring the

current from one DUT, it is necessary to ensure that the leakage current from all the other DUTs within the same DUT array, and from all the DUTs in other DUT arrays, is not significant compared to the minimum current we want to measure. To ensure that the leakage current from other DUTs within the same array does not affect measurement accuracy, a negative (or above-supply) gate voltage is applied to NDUTs (or PDUTs) and the number of total DUTs is limited to 128 per array to ensure the 1% current accuracy even in the subthreshold region. To minimize leakage from other DUT arrays, I/O devices are used as row enable switches. The off current of I/O devices is many orders of magnitude smaller than the off-current of nominal transistors. The total leakage is reduced to less than 0.5% of the minimum current, $50nA$, that the test circuit is designed to measure.

V. Extraction Methodology

An extraction methodology is developed to determine the radius of influence using spatial samples of our measured data.

A. Effective Pattern Density, filter length and filter

The effective pattern density of a DUT is calculated by averaging the neighboring local pattern density using a weighted function parameterized by the radius of influence. Since the averaging operation is analogous to a low-pass filter operation, the weighted averaging function is referred as a "filter" in this paper. The radius of influence, which parameterizes the filter, is called the "filter length" and is defined to be two times the standard deviation in the case of our Gaussian filter.

B. Scenarios

The extraction methodology is demonstrated using two scenarios: A and B. Under each scenario, a different hypothesis is made regarding the underlying manufacturing physics that contribute to the systematic variation. Two assumptions are made in all scenarios: 1) a Gaussian filter is used as the weighting function, and 2) a linear relationship between the effective pattern density and the measured saturation current is assumed. Gaussian filters are employed here, based on previous success in modeling pattern density effects in other processes such as CMP with approximate Gaussian shape, even when the distance-dependence is not strictly Gaussian [22]. Direct extraction of the impulse response filter shape is an area for future exploration. A simple linear relationship between effective pattern density and measured current is also used, as it will detect even nonlinear dependence if it exists except in highly unlikely cases.

1) Scenario A: The medium-range pattern density effect is assumed to dominate in Scenario A. In this case, the Gaussian filter has a radius of influence larger than the dimension of the unit cells. The effective pattern density and the predicted current can be modeled as a convolution of the local pattern density and a pattern density filter function, as (8) and (9).

$$\rho(x,y) = filter(x,y,\delta) \otimes lpd(x,y) \tag{8}$$

$$I_{predicted} = I_0 + \alpha \times (\rho(x,y) - \rho_0) \tag{9}$$

where $I_{predicted}$ is the predicted current, I_0 is the average measured current of the same type of DUTs, ρ_0 is the average effective pattern density, α is a fitting coefficient and δ is the filter length. Predicted current under Scenario A is calculated by adding the average measured current of the same DUT type to the zero-mean effective pattern density scaled by α.

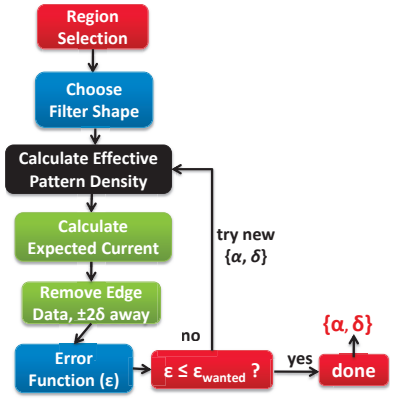

Fig. 9. Extraction procedure under Scenario A.

The extraction procedure can be summarized in Fig. 9. The first step is to choose the fitting type: STI, polysilicon or both. The extraction procedure uses only the measured data of the selected type. Fitting individual pattern density regions first can be used to decouple different systematic effects. The second step is to select a filter shape (in our case, Gaussian). The third step calculates the effective pattern density based on the best guess for the filter length. The pattern density map used here includes not only the local pattern density of the DUT regions, but also includes all known local pattern density in the periphery circuitry. Using the calculated effective pattern density, the fourth step estimates the expected current assuming a linear model. The fifth step selects a set of measured data to be compared to the predicted data using the assumed model. Any data points that are two standard deviations (δ) away from the unknown pattern density are removed to avoid model domain edge effects. The last step calculates the mean-square-error (MSE). A hill-climbing algorithm is used to find an optimal pair (α, δ).

A number of synthetic pattern density maps with added random noise are generated to examine and test this extraction procedure. The noise variance is estimated from our measured data. The extraction procedure is able to extract the correct (α, δ) within 1% for all cases.

2) Scenario B: The effect of local layout features and local layout pattern dominate the systematic variation in Scenario B. In order to extract any additional medium-range pattern density effect, our strategy under Scenario B is to first extract and then remove any variation due to local geometries, and finally use the same extraction procedure as in Scenario A on the residual data. The predicted current can then be described by (10). The added term, $\alpha_1 \cdot f(\chi_{den})$, models the local feature

effect.

$$I_{predicted} = I_0 + \alpha_0 \cdot \{\rho(x,y) - \rho_0\} + \alpha_1 \cdot f(\chi_{den})$$
$$\chi_{den} \in \{H_{STI}, L_{STI}, H_{poly}, L_{poly}\} \quad (10)$$

Using this model, the expected current of two transistors from region of low pattern can be written as (11) and (12). The models only differ in the effective pattern density term.

$$I_{DUT1,L} = I_0 + \alpha_0 \cdot \{\rho_{DUT1,L} - \rho_0\} + \alpha_1 \cdot f(L) \quad (11)$$
$$I_{DUT2,L} = I_0 + \alpha_0 \cdot \{\rho_{DUT2,L} - \rho_0\} + \alpha_1 \cdot f(L) \quad (12)$$

By subtracting out the average measured current ($I_{0,L} = I_0 + \alpha_1 \cdot f(L)$) in the low pattern density region, a term with just the contribution from medium-range effective pattern density can be obtained as shown in (13). Several synthetic test pattern density maps are also generated in this scenario to validate the extraction procedure.

$$I_{DUT1,L} - I_{0,L} = \alpha_0 \cdot \{\rho_{DUT2,L} - \rho_0\} \quad (13)$$

VI. Extraction Result and Analysis

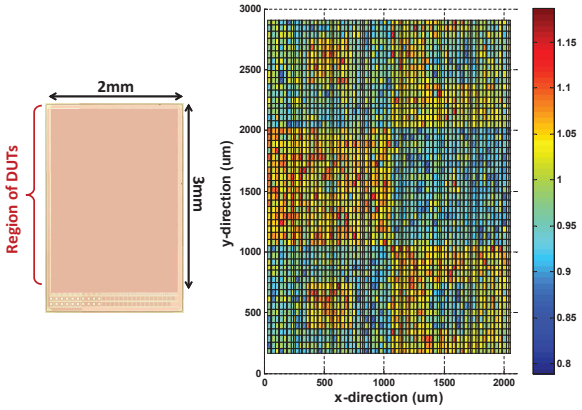

Fig. 10. Die photo (top metal layers cover the DUT region so that the underlying pattern density difference is not visible here) and the saturation current measurement of Type 2 DUTs in one test chip.

After verifying the proposed extraction technique using the synthetic pattern density maps in the previous section, the technique is applied to the measured saturation current of a fabricated die, shown in Fig. 10. All measured current is normalized to the averaged current of all Type 2 DUTs. The figure shows a strong correlation between the measurement result and the DUT local pattern density layout. Moreover, two transistors with the same local geometries in close proximity often have substantially different measured results, indicating significant random variation. Type 2 DUTs, rather than Type 1, are chosen here to extract the radius of influence because they have twice the width of Type 1. This can help accentuate the pattern density effect.

A. STI Pattern Density Analysis

1) Scenario A: The STI pattern density analysis is performed on the bottom two squares of the test structure layout. The left plots of Fig. 11 indicate that the mean of the DUT

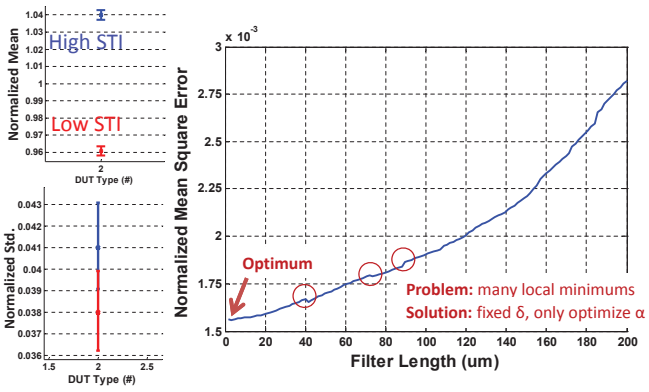

Fig. 11. Mean, standard deviation and extraction result.

current shows a statistically significant difference between high and low pattern density region; the variance deviation does not show a statistically significant (at 95% confidence) difference.

Using the proposed extraction procedure, different initial guesses, (α_0, δ_0), can produce different optimal (α, δ) due to the hill-climbing nature of the extraction methodology. Our approach is to fix the filter length, δ, for each extraction run and search only for the optimal fitting coefficient, α. The MSE of each extraction run is then compared to other runs to find the filter length with minimum MSE. The result of this approach is shown on the right side of Fig. 11, where a few local minima are circled in red. The minimization drives the extracted filter length to the smallest available radius of influence, indicating that the radius is within the size of the unit cell.

Two additional analyses are considered to validate this conclusion. The first analysis is done by subtracting out the predicted current using the extracted filter length from the actual measured data. The residual currents are then plotted on a normplot, as shown in Fig. 12. The second analysis is done by plotting the autocorrelation function with respect to the separation distance between all pairs of transistors on the test structure, shown in Fig. 13. Fig. 12 shows that the measured current deviates from a normplot below 5% and beyond 99%; Fig. 13 shows there could be significant but small correlations at longer distances. Both analyses indicate that a small longer-range effect could be buried under the much-stronger local effect.

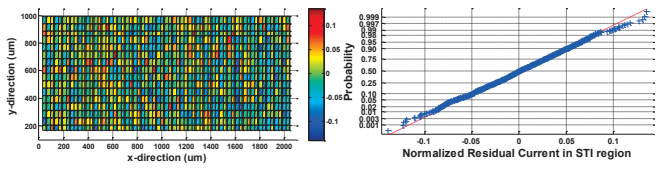

Fig. 12. Analysis I under Scenario A.

The same analysis is done on other DUT types. Fig. 14 shows that for every transistor type, difference in STI pattern density would cause a statistically significant mean difference

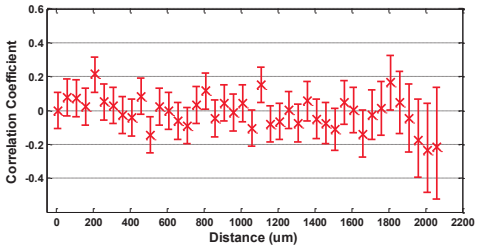

Fig. 13. Analysis II: Pairwise cross-correlation.

in transistor current. Applying the extraction flow to other DUT types also show a similar trend: the minimum MSE occurs when the filter length is within the DUT unit cell, suggesting that the systematic variation is mainly due to local layout features.

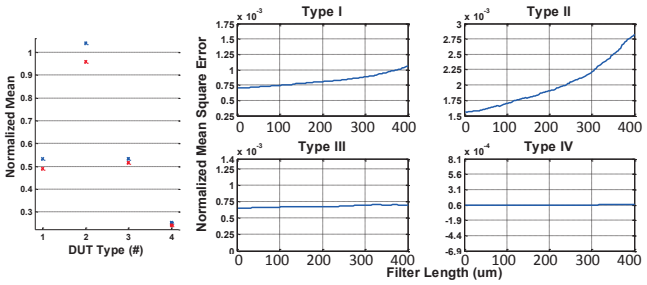

Fig. 14. Analysis on other DUT types under Scenario A.

2) Scenarios B: To prevent the local layout features from overshadowing a possible longer-range pattern density effect, in Scenario B, the effects due to local layout features are modeled and removed from our measurement data first before applying the extraction methodology described in Scenario A. The MSE is plotted against the filter length as shown on the top of Fig. 15. The red line in the figure indicates the total variance of the measured data with the local layout effect removed. In this scenario, we find that a longer filter length is preferred, as the minimum MSE decreases when the filter length increases, in contrast to the trend found in the previous scenario. The percentage improvement in MSE by increasing the filter length from 0μm to 400μm is about 2% (1.56 to 1.529). The bottom plot of Fig. 15 shows the magnitude of the fitting coefficient α at different filter lengths of the extraction result. The coefficient has nonzero but small magnitude for all the fitted filter lengths. The percentage improvement in total variance and the small fitting coefficient indicate that there exists a significant longer range pattern density effect, but the contribution of the effective pattern density term is small. The methodology proposed in Scenario B also confirms that removal of the local layout effect can help reveal hidden longer-range pattern density effect that cannot be found in Scenario A.

Additional analyses are also done to verify the result obtained in Scenario B. The verification focuses on the STI residual current. Fig. 16 shows the normalized residual current of

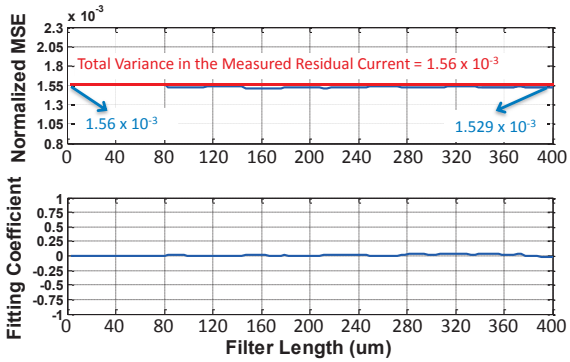

Fig. 15. Analysis under Scenario B.

Type 2 NMOS DUTs and the laid-out STI pattern density map. Different filter lengths are applied to the laid-out STI pattern density to generate corresponding effective STI pattern density maps. The effective pattern density maps are generated by assuming that the unknown regions outside the die area have a flat pattern density of 60%, the average pattern density of the chip. Four such examples are shown in Fig 17. Correlation coefficients are then calculated between the actual measured residual current and the generated effective pattern density maps. The result is shown in in Fig. 18 with bars indicating the 95% confidence interval. As the filter length increases, we notice an increase in correlation coefficient, implying that longer filter lengths have stronger correlations with the residual current maps. Moreover, the percentage variance when the filter length equals to 400μm is about 2%, which matches with our previous filter length extraction method in Scenario B. The range of filter length sweeping is larger in this case because we assume the unknown outside pattern density at 60%. This verification further confirms that there exists a longer range pattern density effect, but the magnitude of influence is small.

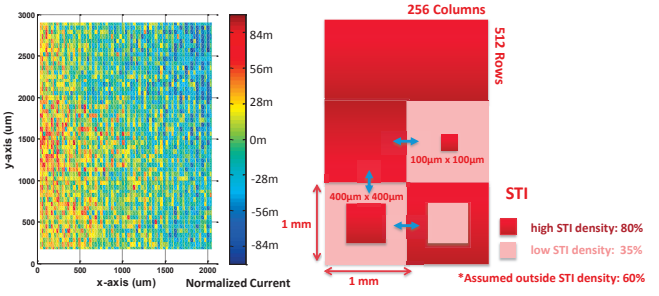

Fig. 16. Normalized residual current of Type 2, NMOS DUTs and the STI pattern density layout map.

B. Poly Pattern Density Analysis

The same analysis is performed on the polysilicon regions to extract the radius of influence. In both scenarios, the extraction procedure suggests that the systematic variation in polysilicon is mainly due to local layout features, with only very small medium range pattern density effects (accounting for less than 5% of observed variance).

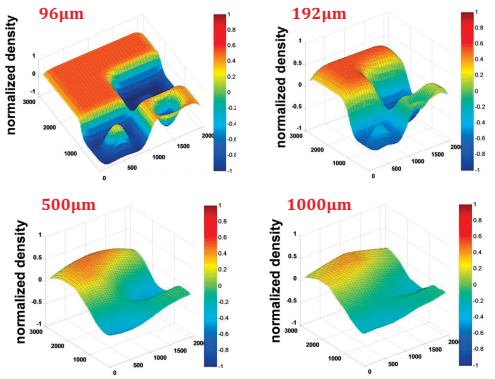

Fig. 17. Effective pattern density maps of STI.

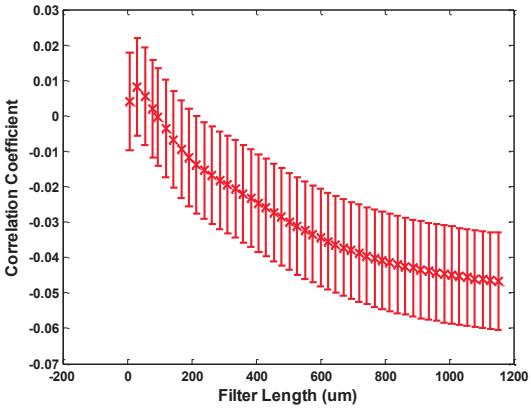

Fig. 18. Correlation between effective STI pattern density and the measured residual current at different filter lengths.

VII. Conclusion and Implications

In this paper, we consider the radius of influence or spatial range of layout which needs to be taken into account when modeling systematic variations affecting a transistor. A new test structure is designed and fabricated to determine this parameter for both STI and polysilicon pattern density. Step pattern density changes are introduced throughout the test structure to accentuate this difference for modeling. The chip consists of 131,072 measurable DUTs for high spatial sampling. A hierarchical access scheme is designed with high efficiency (128:2 in area usage). Since the circuit design is done mostly in the digital domain, it can be scaled to study radius of influence in other technologies.

Extraction procedures under different scenarios are proposed. Each extraction procedure is validated by testing against synthetic pattern density maps. The extraction result of our measured data obtained from a fabricated 65nm technology die, suggests that the radius of influence is primarily within the unit cell size of 6μm x 8μm. The systematic variation induced by medium-range pattern density effect is relatively small. The total variance decomposition, shown in Fig. 19, indicates that the total variance of the transistor saturation current contributed by longer-range pattern density is about 2-5%, while the total variance contributed by local feature differences is 73%. The systematic variation in measured saturation current is mainly due to changes in local layout features for both STI and polysilicon in this technology.

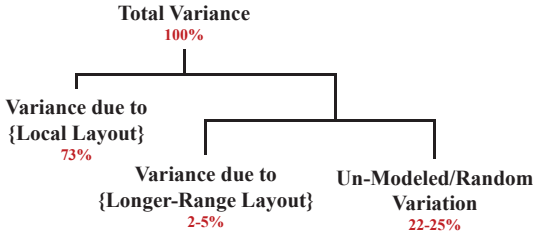

Fig. 19. Total variance decomposition.

These results suggest that post-layout transistor parameter extraction, which takes into account the local features, is sufficient to capture most of the transistor characteristics due to systematic layout difference in this technology. An averaging window that considers medium-range surrounding pattern density can be used to determine additional systematic variance components: in our case, $2-5\%$ of the total variance. On the other hand, since the random variation component can contribute 4-10 times more variance, it may not be necessary to model the longer-range pattern density effect. The design principle introduced in this paper can be applied to study other sources of systematic variation due to pattern layout differences.

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